

ES_LPC407x/8x

Errata sheet LPC407x/8x

Rev. 1.3 — 26 November 2013

Errata sheet

Document information

Info	Content
Keywords	LPC4088FBD208; LPC4088FET208; LPC4088FET180; LPC4088FBD144; LPC4078FBD208; LPC4078FET208; LPC4078FET180; LPC4078FBD144; LPC4078FBD80; LPC4076FET180; LPC4076FBD144; LPC4074FBD144; LPC4074FBD80; LPC4072FBD80, LPC407x, LPC408x, errata
Abstract	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table.</p>



Revision history

Rev	Date	Description
1.3	20131126	<ul style="list-style-type: none">Added IBAT.1.
1.2	20130214	<ul style="list-style-type: none">Added I2C.1.
1.1	20121207	<ul style="list-style-type: none">Added ETHERNET.1.
1	20120924	<ul style="list-style-type: none">Initial version

Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Product identification

The LPC407x/8x devices typically have the following top-side marking:

LPC40xxXXX

xxxxxxx

xxYYWWR[x]

The last digit in the last line (field 'R') will identify the device revision. Note: pre-production parts are marked differently and this system does not apply. This Errata Sheet covers the following revisions of the LPC407x/8x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ETHERNET.1	In Ethernet MII mode, the transmit data TXD3:0 and transmit enable TX_EN incorrectly reference RX_CLK in data transmission.	'-'	Section 3.1
I2C.1	In slave-transmitter mode, the device set in monitor mode must write a dummy value of 0xFF into the DAT register.	'-'	Section 3.2
IBAT.1	Typical lots have about 5 % parts with higher than normal I _{BAT} current when only V _{BAT} power is provided (VDD _{BAT} is grounded).	'-'	Section 3.3

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V _{DD} supply ramps up.	'-'	Section 5.1

3. Functional problems detail

3.1 ETHERNET.1

Introduction:

The Ethernet block contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration. The Ethernet block interfaces between an off-chip Ethernet PHY using the MII (Media Independent Interface) or RMI (reduced MII) protocol and the on-chip MIIM (Media Independent Interface Management) serial bus.

Problem:

In MII mode, the transmit data TXD3:0 and transmit enable TX_EN should reference the TX_CLK from the Ethernet PHY. However, due to a configuration error in the chip, the transmit data TXD3:0 and transmit enable TX_EN reference RX_CLK in data transmission. The consequence of this error is that a small percentage of packets cannot be received by the PHY.

Work-around:

This will be fixed with the next silicon release.

Note: There is no issue in RMI mode operation.

3.2 I2C.1

Introduction:

The I2C monitor mode allows the I2C module to monitor traffic on the I²C-bus without actually participating in traffic or interfering with the I²C-bus.

Problem:

In slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I²C-bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1);    //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for slave-transmitter mode:

```
case 0xA8:      // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:      // data byte in DAT transmitted, ACK received
case 0xC0:      // (last) data byte transmitted, NACK received
case 0xC8:      // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER; //Save data. Data can be processed in Main loop
    LPC_I2C->DAT = 0xFF;              // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;           // clear flag SI
break;
```

3.3 IBAT.1

Introduction:

Two independent power domains ($V_{DD_{REG}}$ domain and V_{BAT} domain) are provided that allow the bulk of the device to have power removed while maintaining operation of the Real Time Clock (RTC). The V_{BAT} pin supplies power only to the RTC domain and is active when V_{BAT} is greater than $V_{DD_{REG}}$. The RTC requires a minimum of power to operate, which can be supplied by an external battery (V_{BAT}). Whenever the device core power ($V_{DD_{REG}}$) is greater than V_{BAT} , $V_{DD_{REG}}$ is used to operate the RTC. When $V_{DD_{REG}}$ is grounded, the I_{BAT} is typically around 1 μA .

Problem:

Typical lots have about 5 % parts with I_{BAT} current as high as about 10 μA when only V_{BAT} is applied ($V_{DD_{REG}}$ is grounded). This is due to a leakage current path in a level shifter in the power domain.

Work-around:

The problematic leakage path is disabled when the part is entered into Deep power-down mode. If the application allows, the customer should put the device into Deep power-down mode before the $V_{DD_{REG}}$ power is grounded; the BOD ISR could potentially be used for this purpose.

4. AC/DC deviations detail

n/a

5. Errata notes

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the V_{DD} level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

7. Contents

1	Product identification	3
2	Errata overview	3
3	Functional problems detail	4
3.1	ETHERNET.1	4
3.2	I2C.1	5
3.3	IBAT.1	6
4	AC/DC deviations detail	7
5	Errata notes	7
5.1	Note.1	7
6	Legal information	8
6.1	Definitions	8
6.2	Disclaimers	8
6.3	Trademarks	8
7	Contents	9

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 November 2013

Document identifier: ES_LPC407X_8X