



## KL36 Sub-Family Data Sheet

Supports the following:

MKL36Z64VLH4, MKL36Z128VLH4,  
MKL36Z256VLH4, MKL36Z256VMP4,  
MKL36Z64VLL4, MKL36Z128VLL4,  
MKL36Z256VLL4, MKL36Z128VMC4,  
MKL36Z256VMC4

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 48 MHz ARM® Cortex-M0+ core
- Memories and memory interfaces
  - Up to 256 KB program flash memory
  - Up to 32 KB RAM
- Clocks
  - 32 kHz to 40 kHz or 3 MHz to 32 MHz crystal oscillator
  - Multi-purpose clock source
- System peripherals
  - Nine low-power modes to provide power optimization based on application requirements
  - 4-channel DMA controller, supporting up to 63 request sources
  - COP Software watchdog
  - Low-leakage wakeup unit
  - SWD interface and Micro Trace buffer
  - Bit Manipulation Engine (BME)
- Security and integrity modules
  - 80-bit unique identification (ID) number per chip
- Human-machine interface
  - Segment LCD controller supporting up to 47 frontplanes and 8 backplanes, or 51 frontplanes and 4 backplanes
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - 16-bit SAR ADC
  - 12-bit DAC
  - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
- Timers
  - Six channel Timer/PWM (TPM)
  - Two 2-channel Timer/PWM (TPM)
  - Periodic interrupt timers
  - 16-bit low-power timer (LPTMR)
  - Real-time clock
- Communication interfaces
  - Two 16-bit SPI modules
  - Two I2C modules
  - I2S (SAI) module
  - One low power UART module
  - Two UART modules

## KL36P121M48SF4



Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: PKL36 and MKL36

# 2 Part identification

## 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 2.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

## 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

**Table 1. Part number fields descriptions**

| Field | Description               | Values   |
|-------|---------------------------|--|
| Q     | Qualification status      | <ul style="list-style-type: none"> <li>• M = Fully qualified, general market flow</li> <li>• P = Prequalification</li> </ul> |
| KL##  | Kinetis family            | <ul style="list-style-type: none"> <li>• KL36</li> </ul>   |
| A     | Key attribute             | <ul style="list-style-type: none"> <li>• Z = Cortex-M0+</li> </ul>   |
| FFF   | Program flash memory size | <ul style="list-style-type: none"> <li>• 64 = 64 KB</li> <li>• 128 = 128 KB</li> <li>• 256 = 256 KB</li> </ul>               |

*Table continues on the next page...*

**Table 1. Part number fields descriptions (continued)**

| Field | Description                 | Values   |
|-------|-----------------------------|--|
| R     | Silicon revision            | <ul style="list-style-type: none"> <li>• (Blank) = Main</li> <li>• A = Revision after main</li> </ul>  |
| T     | Temperature range (°C)      | <ul style="list-style-type: none"> <li>• V = -40 to 105</li> </ul>   |
| PP    | Package identifier          | <ul style="list-style-type: none"> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>• LL = 100 LQFP (14 mm x 14 mm)</li> <li>• MC = 121 MAPBGA (8 mm x 8 mm)</li> </ul> |
| CC    | Maximum CPU frequency (MHz) | <ul style="list-style-type: none"> <li>• 4 = 48 MHz</li> </ul>   |
| N     | Packaging type              | <ul style="list-style-type: none"> <li>• R = Tape and reel</li> </ul>  |

## 2.4 Example

This is an example part number:

MKL36Z256VMC4

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 3.1.1 Example

This is an example of an operating requirement:

| Symbol          | Description               | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V <sub>DD</sub> | 1.0 V core supply voltage | 0.9  | 1.1  | V    |

## 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior:

| Symbol          | Description                              | Min. | Max. | Unit |
|-----------------|--|------|------|------|
| I <sub>WP</sub> | Digital I/O weak pullup/pulldown current | 10   | 130  | μA   |

## 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description                     | Min. | Max. | Unit |
|--------|---------------------------------|------|------|------|
| CIN_D  | Input capacitance: digital pins | —    | 7    | pF   |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.



## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

### 3.8.1 Example 1

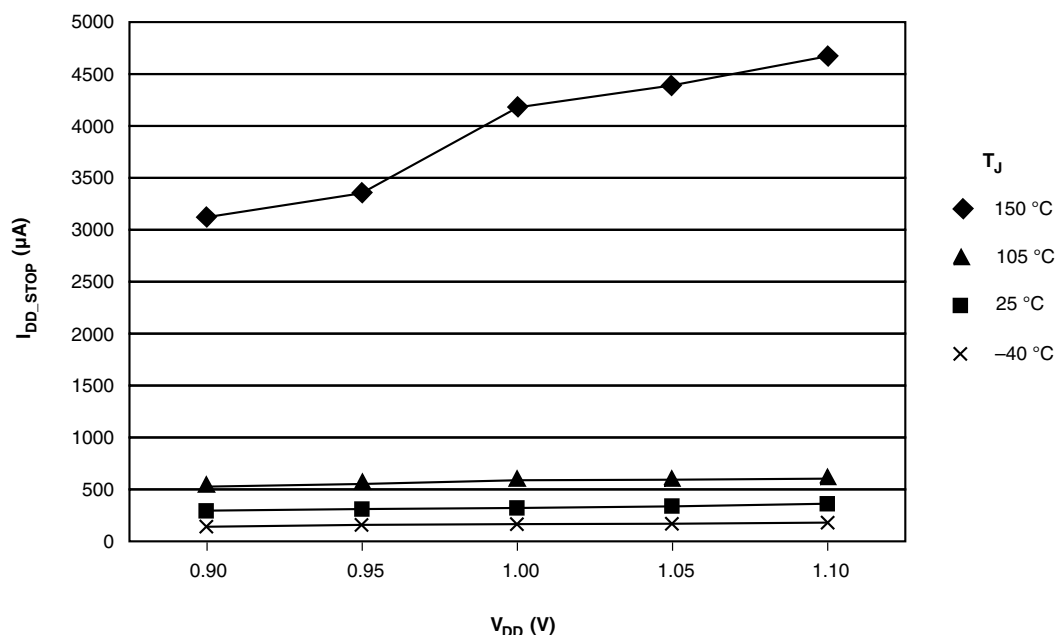
This is an example of an operating behavior that includes a typical value:

| Symbol          | Description                              | Min. | Typ. | Max. | Unit |
|-----------------|--|------|------|------|------|
| I <sub>WP</sub> | Digital I/O weak pullup/pulldown current | 10   | 70   | 130  | μA   |

### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

## Ratings



## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

**Table 2. Typical value conditions**

| Symbol          | Description          | Value | Unit |
|-----------------|----------------------|-------|------|
| T <sub>A</sub>  | Ambient temperature  | 25    | °C   |
| V <sub>DD</sub> | 3.3 V supply voltage | 3.3   | V    |

## 4 Ratings

### 4.1 Thermal handling ratings

**Table 3. Thermal handling ratings**

| Symbol           | Description                   | Min. | Max. | Unit | Notes |
|------------------|-------------------------------|------|------|------|-------|
| T <sub>STG</sub> | Storage temperature           | -55  | 150  | °C   | 1     |
| T <sub>SDR</sub> | Solder temperature, lead-free | —    | 260  | °C   | 2     |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.



2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.2 Moisture handling ratings

**Table 4. Moisture handling ratings**

| Symbol | Description                | Min. | Max. | Unit | Notes |
|--------|----------------------------|------|------|------|-------|
| MSL    | Moisture sensitivity level | —    | 3    | —    | 1     |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 4.3 ESD handling ratings

**Table 5. Moisture handling ratings**

| Symbol    | Description   | Min.  | Max.  | Unit | Notes |
|-----------|---|-------|-------|------|-------|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model     | −2000 | +2000 | V    | 1     |
| $V_{CDM}$ | Electrostatic discharge voltage, charged-device model | −500  | +500  | V    | 2     |
| $I_{LAT}$ | Latch-up current at ambient temperature of 105 °C     | −100  | +100  | mA   |       |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

## 4.4 Voltage and current operating ratings

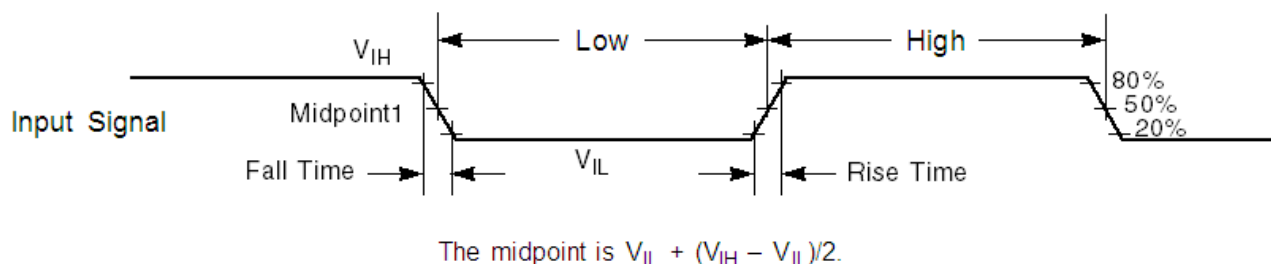
**Table 6. Moisture handling ratings**

| Symbol    | Description   | Min.           | Max.           | Unit |
|-----------|---|----------------|----------------|------|
| $V_{DD}$  | Digital supply voltage  | −0.3           | 3.8            | V    |
| $I_{DD}$  | Digital supply current  | —              | 120            | mA   |
| $V_{IO}$  | IO pin input voltage  | −0.3           | $V_{DD} + 0.3$ | V    |
| $I_D$     | Instantaneous maximum current single pin limit (applies to all port pins) | −25            | 25             | mA   |
| $V_{DDA}$ | Analog supply voltage   | $V_{DD} - 0.3$ | $V_{DD} + 0.3$ | V    |

## 5 General

## 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume the the output pins have the following characteristics.

- $C_L=30$  pF loads
- Slew rate disabled
- Normal drive strength

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

**Table 7. Voltage and current operating requirements**

| Symbol             | Description   | Min.                 | Max.                 | Unit | Notes |
|--------------------|---|----------------------|----------------------|------|-------|
| $V_{DD}$           | Supply voltage  | 1.71                 | 3.6                  | V    |       |
| $V_{DDA}$          | Analog supply voltage   | 1.71                 | 3.6                  | V    |       |
| $V_{DD} - V_{DDA}$ | $V_{DD}$ -to- $V_{DDA}$ differential voltage  | -0.1                 | 0.1                  | V    |       |
| $V_{SS} - V_{SSA}$ | $V_{SS}$ -to- $V_{SSA}$ differential voltage  | -0.1                 | 0.1                  | V    |       |
| $V_{IH}$           | Input high voltage <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li>• <math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul> | $0.7 \times V_{DD}$  | —                    | V    |       |
|                    |   | $0.75 \times V_{DD}$ | —                    | V    |       |
| $V_{IL}$           | Input low voltage <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li>• <math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>  | —                    | $0.35 \times V_{DD}$ | V    |       |
|                    |   | —                    | $0.3 \times V_{DD}$  | V    |       |

Table continues on the next page...

**Table 7. Voltage and current operating requirements (continued)**

| Symbol              | Description  | Min.                 | Max. | Unit | Notes |
|---------------------|--|----------------------|------|------|-------|
| V <sub>HYS</sub>    | Input hysteresis   | $0.06 \times V_{DD}$ | —    | V    |       |
| I <sub>ICIO</sub>   | IO pin negative DC injection current — single pin<br>• $V_{IN} < V_{SS}-0.3V$  | -3                   | —    | mA   | 1     |
| I <sub>ICcont</sub> | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins<br>• Negative current injection | -25                  | —    | mA   |       |
| V <sub>RAM</sub>    | V <sub>DD</sub> voltage required to retain RAM   | 1.2                  | —    | V    |       |

1. All I/O pins are internally clamped to V<sub>SS</sub> through a ESD protection diode. There is no diode connection to V<sub>DD</sub>. If V<sub>IN</sub> greater than V<sub>IO\_MIN</sub> (= V<sub>SS</sub>-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (V_{IO\_MIN} - V_{IN})/|I_{ICIO}|$ .

## 5.2.2 LVD and POR operating requirements

**Table 8. V<sub>DD</sub> supply LVD and POR operating requirements**

| Symbol             | Description  | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|------|------|------|------|-------|
| V <sub>POR</sub>   | Falling V <sub>DD</sub> POR detect voltage                                   | 0.8  | 1.1  | 1.5  | V    | —     |
| V <sub>LVDH</sub>  | Falling low-voltage detect threshold — high range (LVDV = 01)                | 2.48 | 2.56 | 2.64 | V    | —     |
| V <sub>LVW1H</sub> | Low-voltage warning thresholds — high range<br>• Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V    | 1     |
| V <sub>LVW2H</sub> | • Level 2 falling (LVWV = 01)  | 2.72 | 2.80 | 2.88 | V    |       |
| V <sub>LVW3H</sub> | • Level 3 falling (LVWV = 10)  | 2.82 | 2.90 | 2.98 | V    |       |
| V <sub>LVW4H</sub> | • Level 4 falling (LVWV = 11)  | 2.92 | 3.00 | 3.08 | V    |       |
| V <sub>HYSH</sub>  | Low-voltage inhibit reset/recover hysteresis — high range                    | —    | ±60  | —    | mV   | —     |
| V <sub>LVDL</sub>  | Falling low-voltage detect threshold — low range (LVDV=00)                   | 1.54 | 1.60 | 1.66 | V    | —     |
| V <sub>LVW1L</sub> | Low-voltage warning thresholds — low range<br>• Level 1 falling (LVWV = 00)  | 1.74 | 1.80 | 1.86 | V    | 1     |
| V <sub>LVW2L</sub> | • Level 2 falling (LVWV = 01)  | 1.84 | 1.90 | 1.96 | V    |       |
| V <sub>LVW3L</sub> | • Level 3 falling (LVWV = 10)  | 1.94 | 2.00 | 2.06 | V    |       |
| V <sub>LVW4L</sub> | • Level 4 falling (LVWV = 11)  | 2.04 | 2.10 | 2.16 | V    |       |
| V <sub>HYSL</sub>  | Low-voltage inhibit reset/recover hysteresis — low range                     | —    | ±40  | —    | mV   | —     |
| V <sub>BG</sub>    | Bandgap voltage reference  | 0.97 | 1.00 | 1.03 | V    | —     |
| t <sub>LPO</sub>   | Internal low power oscillator period — factory trimmed                       | 900  | 1000 | 1100 | μs   | —     |

1. Rising thresholds are falling threshold + hysteresis voltage

### 5.2.3 Voltage and current operating behaviors

**Table 9. Voltage and current operating behaviors**

| Symbol    | Description  | Min.                             | Max.       | Unit          | Notes |
|-----------|--|----------------------------------|------------|---------------|-------|
| $V_{OH}$  | Output high voltage — Normal drive pad <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -1.5\text{ mA}</math></li> </ul> | $V_{DD} - 0.5$<br>$V_{DD} - 0.5$ | —<br>—     | V<br>V        | 1     |
| $V_{OH}$  | Output high voltage — High drive pad <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -18\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -6\text{ mA}</math></li> </ul>    | $V_{DD} - 0.5$<br>$V_{DD} - 0.5$ | —<br>—     | V<br>V        | 11    |
| $I_{OHT}$ | Output high current total for all ports  | —                                | 100        | mA            |       |
| $V_{OL}$  | Output low voltage — Normal drive pad <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 1.5\text{ mA}</math></li> </ul>    | —<br>—                           | 0.5<br>0.5 | V<br>V        | 1     |
| $V_{OL}$  | Output low voltage — High drive pad <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 18\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 6\text{ mA}</math></li> </ul>       | —<br>—                           | 0.5<br>0.5 | V<br>V        | 1     |
| $I_{OLT}$ | Output low current total for all ports   | —                                | 100        | mA            |       |
| $I_{IN}$  | Input leakage current (per pin) for full temperature range   | —                                | 1          | $\mu\text{A}$ | 22    |
| $I_{IN}$  | Input leakage current (per pin) at 25 °C   | —                                | 0.025      | $\mu\text{A}$ | 2     |
| $I_{IN}$  | Input leakage current (total all pins) for full temperature range  | —                                |            | $\mu\text{A}$ | 2     |
| $I_{OZ}$  | Hi-Z (off-state) leakage current (per pin)   | —                                | 1          | $\mu\text{A}$ |       |
| $R_{PU}$  | Internal pullup resistors  | 20                               | 50         | k $\Omega$    | 33    |

1. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at  $V_{DD} = 3.6\text{ V}$
3. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{SS}$

### 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$  and  $VLLSx \rightarrow RUN$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

**Table 10. Power mode transition operating behaviors**

| Symbol    | Description   | Min. | Typ. | Max. | Unit    | Notes |
|-----------|---|------|------|------|---------|-------|
| $t_{POR}$ | After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip. | —    | —    | 300  | $\mu s$ |       |
|           | • VLLS0 → RUN   | —    | 113  | 124  | $\mu s$ |       |
|           | • VLLS1 → RUN   | —    | 112  | 124  | $\mu s$ |       |
|           | • VLLS3 → RUN   | —    | 53   | 60   | $\mu s$ |       |
|           | • LLS → RUN   | —    | 4.5  | 5.0  | $\mu s$ |       |
|           | • VLPS → RUN  | —    | 4.5  | 5.0  | $\mu s$ |       |
|           | • STOP → RUN  | —    | 4.5  | 5.0  | $\mu s$ |       |

## 5.2.5 Power consumption operating behaviors

**Table 11. Power consumption operating behaviors**

| Symbol         | Description   | Min. | Typ. | Max.     | Unit    | Notes |
|----------------|---|------|------|----------|---------|-------|
| $I_{DDA}$      | Analog supply current   | —    | —    | See note | mA      | 1     |
| $I_{DD\_RUN}$  | Run mode current — all peripheral clocks disabled, code executing from flash  | —    | 5.4  | 7.5      | mA      | 2     |
|                |   | —    | 5.5  | 7.7      | mA      |       |
| $I_{DD\_RUN}$  | Run mode current — all peripheral clocks enabled, code executing from flash   | —    | 6.1  | 8.3      | mA      | 3     |
|                |   | —    | 6.3  | 7.9      | mA      |       |
|                |   | —    | 6.6  | 8.5      | mA      |       |
|                |   | —    | 6.6  | 8.5      | mA      |       |
| $I_{DD\_WAIT}$ | Wait mode high frequency current at 3.0 V — all peripheral clocks disabled    | —    | 4.4  | 6.3      | mA      | 2     |
| $I_{DD\_WAIT}$ | Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled | —    | 3.3  | 5.2      | mA      | 4     |
| $I_{DD\_VLPR}$ | Very-low-power run mode current at 3.0 V — all peripheral clocks disabled     | —    | 292  | 875      | $\mu A$ | 5     |

Table continues on the next page...

**Table 11. Power consumption operating behaviors (continued)**

| Symbol                | Description   | Min.                  | Typ.                                  | Max.                              | Unit | Notes |
|-----------------------|---|-----------------------|---------------------------------------|-----------------------------------|------|-------|
| I <sub>DD_VLPR</sub>  | Very-low-power run mode current at 3.0 V — all peripheral clocks enabled  | —                     | 522                                   | 1225                              | μA   | 6     |
| I <sub>DD_VLPW</sub>  | Very-low-power wait mode current at 3.0 V   | —                     | 261                                   | 777                               | μA   | 7     |
| I <sub>DD_STOP</sub>  | Stop mode current <ul style="list-style-type: none"> <li>at 3.0 V <ul style="list-style-type: none"> <li>-40 °C to 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul> </li> </ul>                    | —<br>—<br>—<br>—<br>— | 312<br>330<br>356<br>393<br>483       | 511<br>543<br>605<br>703<br>938   | μA   |       |
| I <sub>DD_VLPS</sub>  | Very-low-power stop mode current <ul style="list-style-type: none"> <li>at 3.0 V <ul style="list-style-type: none"> <li>-40 °C to 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul> </li> </ul>     | —<br>—<br>—<br>—<br>— | 2.8<br>7.8<br>16.7<br>30.8<br>67.2    | 7.8<br>24.4<br>51.3<br>93<br>192  | μA   |       |
| I <sub>DD_LLS</sub>   | Low-leakage stop mode current <ul style="list-style-type: none"> <li>at 3.0 V <ul style="list-style-type: none"> <li>-40 °C to 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul> </li> </ul>        | —<br>—<br>—<br>—<br>— | 2.0<br>4.2<br>8.1<br>14.5<br>32.0     | 4.3<br>10.1<br>21.1<br>36<br>77   | μA   |       |
| I <sub>DD_VLLS3</sub> | Very-low-leakage stop mode 3 current <ul style="list-style-type: none"> <li>at 3.0 V <ul style="list-style-type: none"> <li>-40 °C to 25 °C</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul> </li> </ul> | —<br>—<br>—<br>—<br>— | 1.5<br>2.9<br>5.7<br>10.1<br>22.0     | 2.9<br>7.1<br>13.3<br>24<br>50    | μA   |       |
| I <sub>DD_VLLS1</sub> | Very-low-leakage stop mode 1 current <ul style="list-style-type: none"> <li>at 3.0V <ul style="list-style-type: none"> <li>-40°C to 25°C</li> <li>at 50°C</li> <li>at 70°C</li> <li>at 85°C</li> <li>at 105°C</li> </ul> </li> </ul>        | —<br>—<br>—<br>—<br>— | 0.65<br>1.27<br>2.57<br>4.86<br>11.50 | 1.4<br>2.6<br>7.9<br>12.6<br>23.3 | μA   |       |

Table continues on the next page...

**Table 11. Power consumption operating behaviors (continued)**

| Symbol                | Description  | Min. | Typ.  | Max.  | Unit | Notes |
|-----------------------|--|------|-------|-------|------|-------|
| I <sub>DD_VLLSO</sub> | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0)<br>• at 3.0 V<br>• -40 °C to 25 °C<br>• at 50 °C<br>• at 70 °C<br>• at 85 °C<br>• at 105 °C | —    | 0.33  | 0.876 | μA   |       |
|                       |  | —    | 0.94  | 2.1   |      |       |
|                       |  | —    | 2.20  | 4.8   |      |       |
|                       |  | —    | 4.47  | 9.2   |      |       |
|                       |  | —    | 11.16 | 22.7  |      |       |
|                       |  | —    |       |       |      |       |
| I <sub>DD_VLLSO</sub> | Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1)<br>• at 3.0 V<br>• -40 °C to 25 °C<br>• at 50 °C<br>• at 70 °C<br>• at 85 °C<br>• at 105 °C | —    | 0.13  | 0.546 | μA   | 8     |
|                       |  | —    | 0.74  | 1.8   |      |       |
|                       |  | —    | 2.01  | 4.5   |      |       |
|                       |  | —    | 4.28  | 8.9   |      |       |
|                       |  | —    | 10.96 | 22.3  |      |       |
|                       |  | —    |       |       |      |       |

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 48MHz core and system clock, 24MHz bus clock, and 24MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
3. 48MHz core and system clock, 24MHz bus clock, and 24MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. 24MHz core and system clock, and 12MHz bus clock and flash clock. MCG configured for FEI mode.
5. 4 MHz core, system clock and 1MHz bus and flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
6. 4 MHz core, system clock and 1MHz bus and flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
7. 4 MHz core, system clock and 1MHz bus and flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
8. No brownout

**Table 12. Low power mode peripheral adders — typical value**

| Symbol                     | Description  | Temperature (°C) |     |     |     |     |     | Unit |
|----------------------------|--|------------------|-----|-----|-----|-----|-----|------|
|                            |  | -40              | 25  | 50  | 70  | 85  | 105 |      |
| I <sub>IREFSTEN4MHZ</sub>  | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56               | 56  | 56  | 56  | 56  | 56  | μA   |
| I <sub>IREFSTEN32KHZ</sub> | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.   | 52               | 52  | 52  | 52  | 52  | 52  | μA   |
| I <sub>IREFSTEN4MHZ</sub>  | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.       | 206              | 228 | 237 | 245 | 251 | 258 | uA   |

Table continues on the next page...

**Table 12. Low power mode peripheral adders — typical value (continued)**

| Symbol                    | Description   | Temperature (°C) |     |     |     |     |     | Unit |
|---------------------------|---|------------------|-----|-----|-----|-----|-----|------|
|                           |   | -40              | 25  | 50  | 70  | 85  | 105 |      |
| I <sub>REFSTEN32KHz</sub> | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> <li>• VLLS1</li> <li>• VLLS3</li> <li>• LLS</li> <li>• VLPS</li> <li>• STOP</li> </ul>  | 440              | 490 | 540 | 560 | 570 | 580 | nA   |
|                           |   | 440              | 490 | 540 | 560 | 570 | 580 |      |
|                           |   | 490              | 490 | 540 | 560 | 570 | 680 |      |
|                           |   | 510              | 560 | 560 | 560 | 610 | 680 |      |
|                           |   | 510              | 560 | 560 | 560 | 610 | 680 |      |
| I <sub>CMP</sub>          | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.   | 22               | 22  | 22  | 22  | 22  | 22  | μA   |
| I <sub>RTC</sub>          | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.  | 432              | 357 | 388 | 475 | 532 | 810 | nA   |
| I <sub>UART</sub>         | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. <ul style="list-style-type: none"> <li>• MCGIRCLK (4 MHz internal reference clock)</li> <li>• OSCERCLK (4 MHz external crystal)</li> </ul>  | 66               | 66  | 66  | 66  | 66  | 66  | μA   |
|                           |   | 214              | 237 | 246 | 254 | 260 | 268 |      |
|                           |   |                  |     |     |     |     |     |      |
| I <sub>TPM</sub>          | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. <ul style="list-style-type: none"> <li>• MCGIRCLK (4 MHz internal reference clock)</li> <li>• OSCERCLK (4 MHz external crystal)</li> </ul> | 86               | 86  | 86  | 86  | 86  | 86  | μA   |
|                           |   | 235              | 256 | 265 | 274 | 280 | 287 |      |
|                           |   |                  |     |     |     |     |     |      |
| I <sub>BG</sub>           | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.  | 45               | 45  | 45  | 45  | 45  | 45  | μA   |

Table continues on the next page...



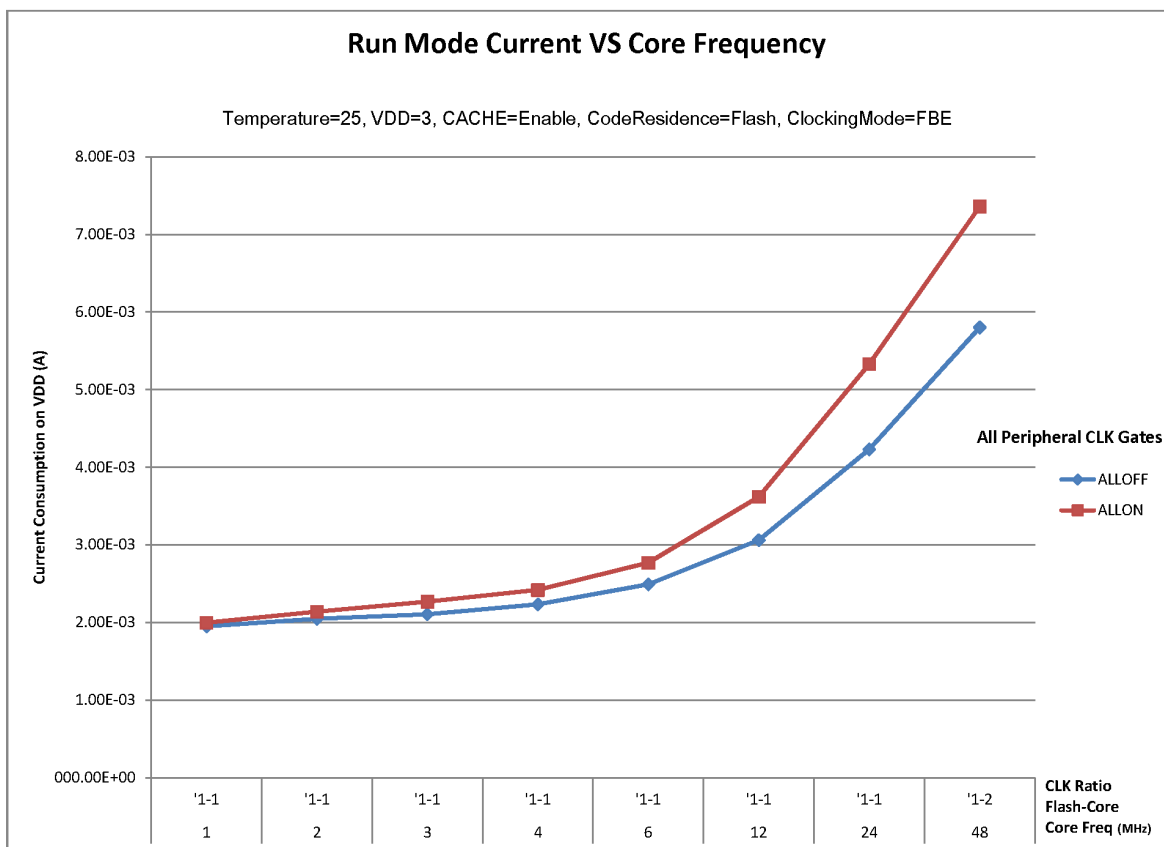
**Table 12. Low power mode peripheral adders — typical value (continued)**

| Symbol           | Description   | Temperature (°C) |     |     |     |     |     | Unit |
|------------------|---|------------------|-----|-----|-----|-----|-----|------|
|                  |   | -40              | 25  | 50  | 70  | 85  | 105 |      |
| I <sub>ADC</sub> | ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>DDA</sub> by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.  | 366              | 366 | 366 | 366 | 366 | 366 | μA   |
| I <sub>LCD</sub> | LCD peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the OSC0_CR[EREFSTEN, EREFSTEN] bits. VIREG disabled, resistor bias network enabled, 1/8 duty cycle, 8 x 36 configuration for driving 288 Segments, 32 Hz frame rate, no LCD glass connected. Includes ERCLK32K (32 kHz external crystal) power consumption. | 5                | 5   | 5   | 5   | 5   | 5   | μA   |

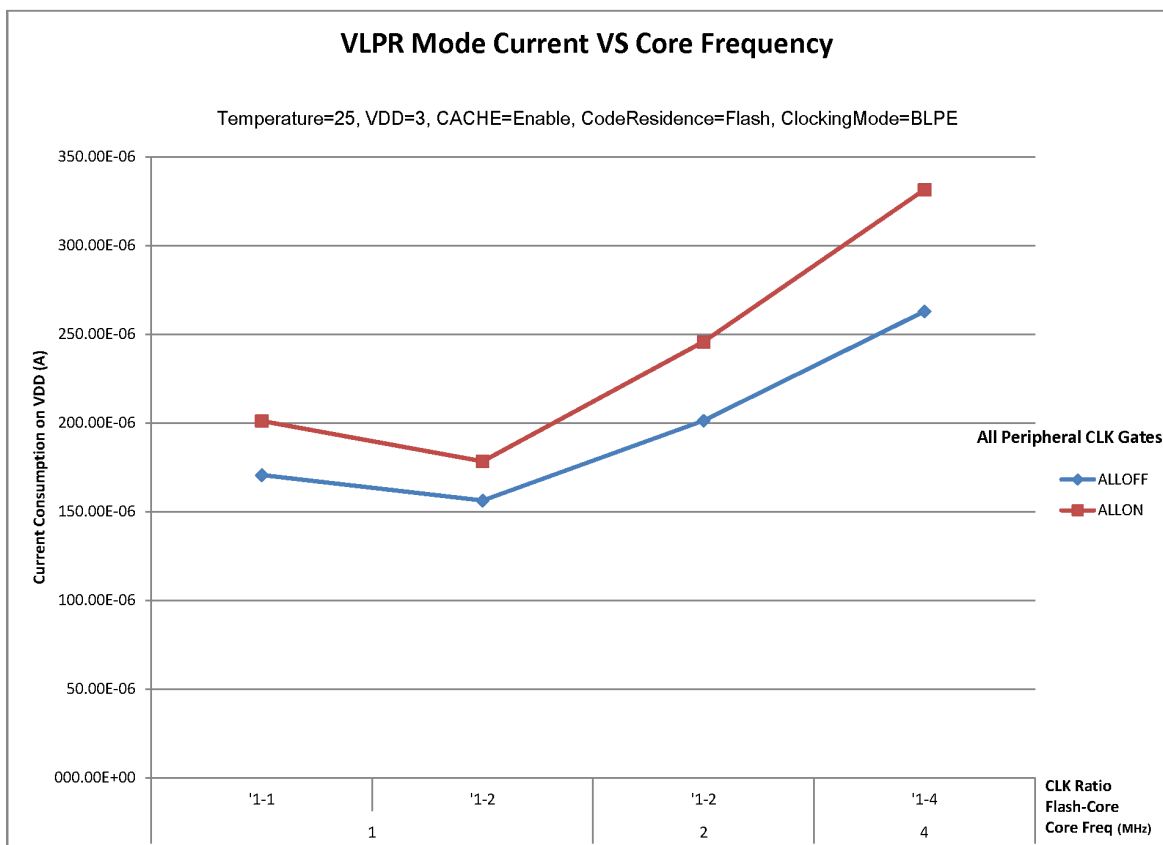
### 5.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 2. Run mode supply current vs. core frequency**



**Figure 3. VLPR mode current vs. core frequency**

## 5.2.6 EMC radiated emissions operating behaviors

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

Table 13. Capacitance attributes

| Symbol            | Description                     | Min. | Max. | Unit |
|-------------------|---------------------------------|------|------|------|
| C <sub>IN_A</sub> | Input capacitance: analog pins  | —    | 7    | pF   |
| C <sub>IN_D</sub> | Input capacitance: digital pins | —    | 7    | pF   |

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

Table 14. Device clock specifications

| Symbol                   | Description   | Min. | Max. | Unit |
|--------------------------|---|------|------|------|
| Normal run mode          |   |      |      |      |
| f <sub>SYS</sub>         | System and core clock   | —    | 48   | MHz  |
| f <sub>BUS</sub>         | Bus clock   | —    | 24   | MHz  |
| f <sub>FLASH</sub>       | Flash clock   | —    | 24   | MHz  |
| f <sub>LPTMR</sub>       | LPTMR clock   | —    | 24   | MHz  |
| VLPR mode <sup>1</sup>   |   |      |      |      |
| f <sub>SYS</sub>         | System and core clock   | —    | 4    | MHz  |
| f <sub>BUS</sub>         | Bus clock   | —    | 1    | MHz  |
| f <sub>FLASH</sub>       | Flash clock   | —    | 1    | MHz  |
| f <sub>LPTMR</sub>       | LPTMR clock   | —    | 24   | MHz  |
| f <sub>ERCLK</sub>       | External reference clock  | —    | 16   | MHz  |
| f <sub>LPTMR_pin</sub>   | LPTMR clock   | —    | 24   | MHz  |
| f <sub>LPTMR_ERCLK</sub> | LPTMR external reference clock  | —    | 16   | MHz  |
| f <sub>osc_hi_2</sub>    | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | —    | 16   | MHz  |
| f <sub>TPM</sub>         | TPM asynchronous clock  | —    | 8    | MHz  |
| f <sub>UART0</sub>       | UART0 asynchronous clock  | —    | 8    | MHz  |

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 5.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, UART, and I<sup>2</sup>C signals.

**Table 15. Device clock specifications**

| Description  | Min. | Max. | Unit             | Notes |
|--|------|------|------------------|-------|
| GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5  | —    | Bus clock cycles | 1     |
| External RESET and NMI pin interrupt pulse width — Asynchronous path               | 100  | —    | ns               | 2     |
| GPIO pin interrupt pulse width — Asynchronous path                                 | 16   | —    | ns               | 2     |
| Port rise and fall time  | —    | 36   | ns               | 3     |

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

**Table 16. Thermal operating requirements**

| Symbol         | Description              | Min. | Max. | Unit |
|----------------|--------------------------|------|------|------|
| T <sub>J</sub> | Die junction temperature | −40  | 125  | °C   |
| T <sub>A</sub> | Ambient temperature      | −40  | 105  | °C   |

### 5.4.2 Thermal attributes

**Table 17. Thermal attributes**

| Board type        | Symbol            | Description  | 121<br>MAPBG<br>A | 100<br>LQFP | 64 LQFP | Unit | Notes |
|-------------------|-------------------|--|-------------------|-------------|---------|------|-------|
| Single-layer (1S) | R <sub>θJA</sub>  | Thermal resistance, junction to ambient (natural convection)     | 94                | 64          | 69      | °C/W | 1     |
| Four-layer (2s2p) | R <sub>θJA</sub>  | Thermal resistance, junction to ambient (natural convection)     | 57                | 51          | 51      | °C/W |       |
| Single-layer (1S) | R <sub>θJMA</sub> | Thermal resistance, junction to ambient (200 ft./min. air speed) | 81                | 54          | 58      | °C/W |       |
| Four-layer (2s2p) | R <sub>θJMA</sub> | Thermal resistance, junction to ambient (200 ft./min. air speed) | 53                | 45          | 44      | °C/W |       |
| —                 | R <sub>θJB</sub>  | Thermal resistance, junction to board                            | 40                | 37          | 33      | °C/W | 2     |
| —                 | R <sub>θJC</sub>  | Thermal resistance, junction to case                             | 30                | 19          | 19      | °C/W | 3     |

*Table continues on the next page...*

**Table 17. Thermal attributes (continued)**

| Board type | Symbol      | Description   | 121<br>MAPBG<br>A | 100<br>LQFP | 64 LQFP | Unit | Notes |
|------------|-------------|---|-------------------|-------------|---------|------|-------|
| —          | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 8                 | 4           | 4       | °C/W | 4     |

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions — Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions — Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions — Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions — Natural Convection (Still Air)*.

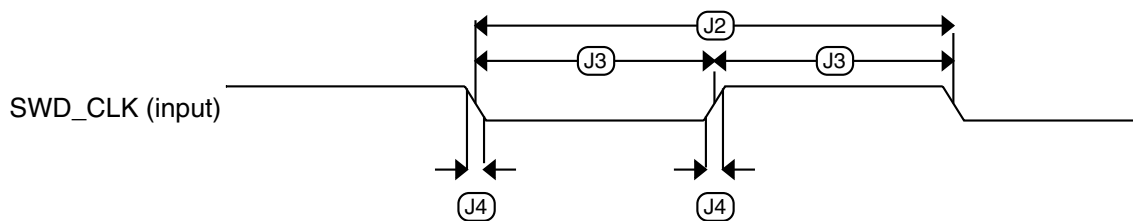
## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

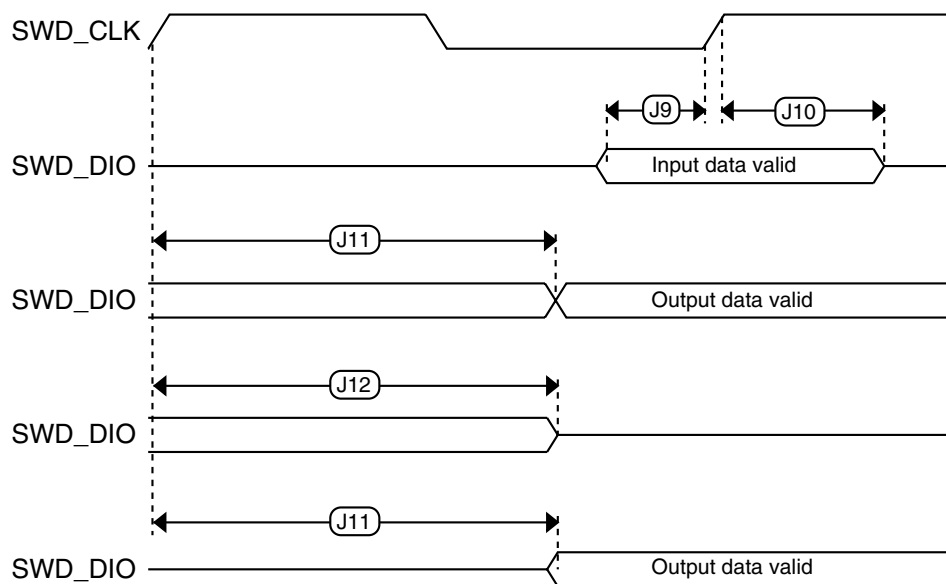
#### 6.1.1 SWD electricals

**Table 18. SWD full voltage range electricals**

| Symbol | Description  | Min. | Max. | Unit |
|--------|--|------|------|------|
|        | Operating voltage  | 1.71 | 3.6  | V    |
| J1     | SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul> | 0    | 25   | MHz  |
| J2     | SWD_CLK cycle period   | 1/J1 | —    | ns   |
| J3     | SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>      | 20   | —    | ns   |
| J4     | SWD_CLK rise and fall times  | —    | 3    | ns   |
| J9     | SWD_DIO input data setup time to SWD_CLK rise  | 10   | —    | ns   |
| J10    | SWD_DIO input data hold time after SWD_CLK rise  | 0    | —    | ns   |
| J11    | SWD_CLK high to SWD_DIO data valid   | —    | 32   | ns   |
| J12    | SWD_CLK high to SWD_DIO high-Z   | 5    | —    | ns   |



**Figure 4. Serial wire clock input timing**



**Figure 5. Serial wire data timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

## 6.3.1 MCG specifications

Table 19. MCG specifications

| Symbol                    | Description  |  | Min.                         | Typ.      | Max.    | Unit                  | Notes    |
|---------------------------|--|--|------------------------------|-----------|---------|-----------------------|----------|
| f <sub>ints_ft</sub>      | Internal reference frequency (slow clock) — factory trimmed at nominal V <sub>DD</sub> and 25 °C   |  | —                            | 32.768    | —       | kHz                   |          |
| f <sub>ints_t</sub>       | Internal reference frequency (slow clock) — user trimmed   |  | 31.25                        | —         | 39.0625 | kHz                   |          |
| Δf <sub>dco_res_t</sub>   | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM]                           |  | —                            | ± 0.3     | ± 0.6   | %f <sub>dco</sub>     | 11       |
| Δf <sub>dco_t</sub>       | Total deviation of trimmed average DCO output frequency over voltage and temperature   |  | —                            | +0.5/-0.7 | ± 3     | %f <sub>dco</sub>     | 1, 22    |
| Δf <sub>dco_t</sub>       | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C                                      |  | —                            | ± 0.4     | ± 1.5   | %f <sub>dco</sub>     | 1, 2     |
| f <sub>intf_ft</sub>      | Internal reference frequency (fast clock) — factory trimmed at nominal V <sub>DD</sub> and 25 °C   |  | —                            | 4         | —       | MHz                   |          |
| Δf <sub>intf_ft</sub>     | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal V <sub>DD</sub> and 25 °C |  | —                            | +1/-2     | ± 3     | %f <sub>intf_ft</sub> | 2        |
| f <sub>intf_t</sub>       | Internal reference frequency (fast clock) — user trimmed at nominal V <sub>DD</sub> and 25 °C  |  | 3                            | —         | 5       | MHz                   |          |
| f <sub>loc_low</sub>      | Loss of external clock minimum frequency — RANGE = 00  |  | (3/5) x f <sub>ints_t</sub>  | —         | —       | kHz                   |          |
| f <sub>loc_high</sub>     | Loss of external clock minimum frequency —   |  | (16/5) x f <sub>ints_t</sub> | —         | —       | kHz                   |          |
| FLL                       |  |  |                              |           |         |                       |          |
| f <sub>fill_ref</sub>     | FLL reference frequency range  |  | 31.25                        | —         | 39.0625 | kHz                   |          |
| f <sub>dco</sub>          | DCO output frequency range   | Low range (DRS = 00)<br>640 × f <sub>fill_ref</sub>  | 20                           | 20.97     | 25      | MHz                   | 3, 43, 4 |
|                           |  | Mid range (DRS = 01)<br>1280 × f <sub>fill_ref</sub> | 40                           | 41.94     | 48      | MHz                   |          |
| f <sub>dco_t_DMx32</sub>  | DCO output frequency   | Low range (DRS = 00)<br>732 × f <sub>fill_ref</sub>  | —                            | 23.99     | —       | MHz                   | 5, 656   |
|                           |  | Mid range (DRS = 01)<br>1464 × f <sub>fill_ref</sub> | —                            | 47.97     | —       | MHz                   |          |
| J <sub>cyc_fill</sub>     | FLL period jitter<br>• f <sub>VCO</sub> = 48 MHz   |  | —                            | 180       | —       | ps                    | 77       |
| t <sub>fill_acquire</sub> | FLL target frequency acquisition time  |  | —                            | —         | 1       | ms                    | 88       |
| PLL                       |  |  |                              |           |         |                       |          |
| f <sub>vco</sub>          | VCO operating frequency  |  | 48.0                         | —         | 100     | MHz                   |          |
| I <sub>pll</sub>          | PLL operating current<br>• PLL at 96 MHz (f <sub>osc_hi_1</sub> = 8 MHz, f <sub>pll_ref</sub> = 2 MHz, VDIV multiplier = 48)                     |  | —                            | 1060      | —       | μA                    | 99       |

Table continues on the next page...



**Table 19. MCG specifications (continued)**

| Symbol          | Description  | Min.       | Typ.        | Max.  | Unit     | Notes |
|-----------------|--|------------|-------------|---|----------|-------|
| $I_{pll}$       | PLL operating current <ul style="list-style-type: none"> <li>PLL at 48 MHz (<math>f_{osc\_hi\_1} = 8</math> MHz, <math>f_{pll\_ref} = 2</math> MHz, VDIV multiplier = 24)</li> </ul> | —          | 600         | —   | $\mu$ A  | 9     |
| $f_{pll\_ref}$  | PLL reference frequency range  | 2.0        | —           | 4.0   | MHz      |       |
| $J_{cyc\_pll}$  | PLL period jitter (RMS) <ul style="list-style-type: none"> <li><math>f_{vco} = 48</math> MHz</li> <li><math>f_{vco} = 100</math> MHz</li> </ul>                                      | —<br>—     | 120         | —<br>—                                      | ps<br>ps | 1010  |
| $J_{acc\_pll}$  | PLL accumulated jitter over 1 $\mu$ s (RMS) <ul style="list-style-type: none"> <li><math>f_{vco} = 48</math> MHz</li> <li><math>f_{vco} = 100</math> MHz</li> </ul>                  | —<br>—     | 1350<br>600 | —<br>—                                      | ps<br>ps | 10    |
| $D_{lock}$      | Lock entry frequency tolerance   | $\pm 1.49$ | —           | $\pm 2.98$                                  | %        |       |
| $D_{unl}$       | Lock exit frequency tolerance  | $\pm 4.47$ | —           | $\pm 5.97$                                  | %        |       |
| $t_{pll\_lock}$ | Lock detector detection time   | —          | —           | $150 \times 10^{-6} + 1075(1/f_{pll\_ref})$ | s        | 1111  |

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. The deviation is relative to the factory trimmed frequency at nominal  $V_{DD}$  and 25 °C,  $f_{ints\_ft}$ .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
4. The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature must be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

### 6.3.2.1 Oscillator DC electrical specifications

**Table 20. Oscillator DC electrical specifications**

| Symbol   | Description    | Min. | Typ. | Max. | Unit | Notes |
|----------|----------------|------|------|------|------|-------|
| $V_{DD}$ | Supply voltage | 1.71 | —    | 3.6  | V    |       |

Table continues on the next page...

**Table 20. Oscillator DC electrical specifications (continued)**

| Symbol             | Description  | Min. | Typ. | Max. | Unit | Notes |
|--------------------|--|------|------|------|------|-------|
| I <sub>DDOSC</sub> | Supply current — low-power mode (HGO=0)                    |      |      |      |      | 1     |
|                    | • 32 kHz   | —    | 500  | —    | nA   |       |
|                    | • 4 MHz  | —    | 200  | —    | μA   |       |
|                    | • 8 MHz (RANGE=01)   | —    | 300  | —    | μA   |       |
|                    | • 16 MHz   | —    | 950  | —    | μA   |       |
|                    | • 24 MHz   | —    | 1.2  | —    | mA   |       |
|                    | • 32 MHz   | —    | 1.5  | —    | mA   |       |
| I <sub>DDOSC</sub> | Supply current — high gain mode (HGO=1)                    |      |      |      |      | 1     |
|                    | • 32 kHz   | —    | 25   | —    | μA   |       |
|                    | • 4 MHz  | —    | 400  | —    | μA   |       |
|                    | • 8 MHz (RANGE=01)   | —    | 500  | —    | μA   |       |
|                    | • 16 MHz   | —    | 2.5  | —    | mA   |       |
|                    | • 24 MHz   | —    | 3    | —    | mA   |       |
|                    | • 32 MHz   | —    | 4    | —    | mA   |       |
| C <sub>x</sub>     | EXTAL load capacitance                                     | —    | —    | —    |      | 2, 3  |
| C <sub>y</sub>     | XTAL load capacitance                                      | —    | —    | —    |      | 2, 3  |
| R <sub>F</sub>     | Feedback resistor — low-frequency, low-power mode (HGO=0)  | —    | —    | —    | MΩ   | 2, 4  |
|                    | Feedback resistor — low-frequency, high-gain mode (HGO=1)  | —    | 10   | —    | MΩ   |       |
|                    | Feedback resistor — high-frequency, low-power mode (HGO=0) | —    | —    | —    | MΩ   |       |
|                    | Feedback resistor — high-frequency, high-gain mode (HGO=1) | —    | 1    | —    | MΩ   |       |
| R <sub>S</sub>     | Series resistor — low-frequency, low-power mode (HGO=0)    | —    | —    | —    | kΩ   |       |
|                    | Series resistor — low-frequency, high-gain mode (HGO=1)    | —    | 200  | —    | kΩ   |       |
|                    | Series resistor — high-frequency, low-power mode (HGO=0)   | —    | —    | —    | kΩ   |       |
|                    | Series resistor — high-frequency, high-gain mode (HGO=1)   | —    | 0    | —    | kΩ   |       |

Table continues on the next page...

**Table 20. Oscillator DC electrical specifications (continued)**

| Symbol     | Description  | Min. | Typ.     | Max. | Unit | Notes |
|------------|--|------|----------|------|------|-------|
| $V_{pp}^5$ | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)  | —    | 0.6      | —    | V    |       |
|            | Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)  | —    | $V_{DD}$ | —    | V    |       |
|            | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0) | —    | 0.6      | —    | V    |       |
|            | Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1) | —    | $V_{DD}$ | —    | V    |       |

1.  $V_{DD}=3.3$  V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3.  $C_x, C_y$  can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected,  $R_F$  is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 21. Oscillator frequency specifications**

| Symbol           | Description   | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|------|------|------|------|-------|
| $f_{osc\_lo}$    | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)               | 32   | —    | 40   | kHz  |       |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)  | 3    | —    | 8    | MHz  |       |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8    | —    | 32   | MHz  |       |
| $f_{ec\_extal}$  | Input clock frequency (external clock mode)   | —    | —    | 48   | MHz  | 1, 2  |
| $t_{dc\_extal}$  | Input clock duty cycle (external clock mode)  | 40   | 50   | 60   | %    |       |
| $t_{cst}$        | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)                             | —    | 750  | —    | ms   | 3, 4  |
|                  | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)                             | —    | 250  | —    | ms   |       |
|                  | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)          | —    | 0.6  | —    | ms   |       |
|                  | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)          | —    | 1    | —    | ms   |       |

1. Other frequency limits may apply when external clock is being used as a reference for FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that—it remains within the limits of DCO input clock frequency when divided by FRDIV.

## Peripheral operating requirements and behaviors

3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG\_S register being set.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 22. NVM program/erase timing specifications**

| Symbol                           | Description                              | Min. | Typ. | Max. | Unit          | Notes |
|----------------------------------|--|------|------|------|---------------|-------|
| $t_{hvp\text{gm}4}$              | Longword Program high-voltage time       | —    | 7.5  | 18   | $\mu\text{s}$ |       |
| $t_{h\text{versscr}}$            | Sector Erase high-voltage time           | —    | 13   | 113  | ms            | 1     |
| $t_{h\text{versblk}128\text{k}}$ | Erase Block high-voltage time for 128 KB | —    | 52   | 452  | ms            | 1     |
| $t_{h\text{versall}}$            | Erase All high-voltage time              | —    | 52   | 452  | ms            | 1     |

1. Maximum time based on expectations at cycling end-of-life.

#### 6.4.1.2 Flash timing specifications — commands

**Table 23. Flash command timing specifications**

| Symbol                                | Description  | Min. | Typ. | Max. | Unit          | Notes |
|---------------------------------------|--|------|------|------|---------------|-------|
| $t_{\text{rd}1\text{blk}128\text{k}}$ | Read 1s Block execution time<br>• 128 KB program flash     | —    | —    | 1.7  | ms            |       |
| $t_{\text{rd}1\text{sec}1\text{k}}$   | Read 1s Section execution time (flash sector)              | —    | —    | 60   | $\mu\text{s}$ | 1     |
| $t_{\text{pgmchk}}$                   | Program Check execution time                               | —    | —    | 45   | $\mu\text{s}$ | 1     |
| $t_{\text{rd}r\text{src}}$            | Read Resource execution time                               | —    | —    | 30   | $\mu\text{s}$ | 1     |
| $t_{\text{pgm}4}$                     | Program Longword execution time                            | —    | 65   | 145  | $\mu\text{s}$ |       |
| $t_{\text{ersblk}128\text{k}}$        | Erase Flash Block execution time<br>• 128 KB program flash | —    | 88   | 600  | ms            | 2     |
| $t_{\text{ersscr}}$                   | Erase Flash Sector execution time                          | —    | 14   | 114  | ms            | 2     |
| $t_{\text{rd}1\text{all}}$            | Read 1s All Blocks execution time                          | —    | —    | 1.8  | ms            |       |
| $t_{\text{rd}o\text{nce}}$            | Read Once execution time                                   | —    | —    | 25   | $\mu\text{s}$ | 1     |
| $t_{\text{pgm}o\text{nce}}$           | Program Once execution time                                | —    | 65   | —    | $\mu\text{s}$ |       |

Table continues on the next page...

**Table 23. Flash command timing specifications (continued)**

| Symbol       | Description                               | Min. | Typ. | Max. | Unit    | Notes |
|--------------|---|------|------|------|---------|-------|
| $t_{ersall}$ | Erase All Blocks execution time           | —    | 175  | 1300 | ms      | 2     |
| $t_{vfykey}$ | Verify Backdoor Access Key execution time | —    | —    | 30   | $\mu$ s | 1     |

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 6.4.1.3 Flash high voltage current behaviors

**Table 24. Flash high voltage current behaviors**

| Symbol        | Description   | Min. | Typ. | Max. | Unit |
|---------------|---|------|------|------|------|
| $I_{DD\_PGM}$ | Average current adder during high voltage flash programming operation | —    | 2.5  | 6.0  | mA   |
| $I_{DD\_ERS}$ | Average current adder during high voltage flash erase operation       | —    | 1.5  | 4.0  | mA   |

### 6.4.1.4 Reliability specifications

**Table 25. NVM reliability specifications**

| Symbol           | Description                            | Min. | Typ. <sup>1</sup> | Max. | Unit   | Notes |
|------------------|--|------|-------------------|------|--------|-------|
| Program Flash    |  |      |                   |      |        |       |
| $t_{nvmretp10k}$ | Data retention after up to 10 K cycles | 5    | 50                | —    | years  |       |
| $t_{nvmretp1k}$  | Data retention after up to 1 K cycles  | 20   | 100               | —    | years  |       |
| $n_{nvmcycp}$    | Cycling endurance                      | 10 K | 50 K              | —    | cycles | 2     |

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40\text{ °C} \leq T_j \leq 125\text{ °C}$ .

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

## 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 26](#) and [Table 27](#) are achievable on the differential pins ADCx\_DP0, ADCx\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

### 6.6.1.1 16-bit ADC operating conditions

**Table 26. 16-bit ADC operating conditions**

| Symbol            | Description                    | Conditions  | Min.           | Typ. <sup>1</sup> | Max.                   | Unit | Notes             |
|-------------------|--------------------------------|---|----------------|-------------------|------------------------|------|-------------------|
| V <sub>DDA</sub>  | Supply voltage                 | Absolute  | 1.71           | —                 | 3.6                    | V    |                   |
| ΔV <sub>DDA</sub> | Supply voltage                 | Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )  | -100           | 0                 | +100                   | mV   | <a href="#">2</a> |
| ΔV <sub>SSA</sub> | Ground voltage                 | Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )  | -100           | 0                 | +100                   | mV   | <a href="#">2</a> |
| V <sub>ADIN</sub> | Input voltage                  | <ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>       | VREFL<br>VREFL | —<br>—            | 31/32 * VREFH<br>VREFH | V    |                   |
| C <sub>ADIN</sub> | Input capacitance              | <ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>      | —<br>—         | 8<br>4            | 10<br>5                | pF   |                   |
| R <sub>ADIN</sub> | Input resistance               |   | —              | 2                 | 5                      | kΩ   |                   |
| R <sub>AS</sub>   | Analog source resistance       | 13-bit / 12-bit modes<br>f <sub>ADCK</sub> < 4 MHz  | —              | —                 | 5                      | kΩ   | <a href="#">3</a> |
| f <sub>ADCK</sub> | ADC conversion clock frequency | ≤ 13-bit mode   | 1.0            | —                 | 18.0                   | MHz  | <a href="#">4</a> |
| f <sub>ADCK</sub> | ADC conversion clock frequency | 16-bit mode   | 2.0            | —                 | 12.0                   | MHz  | <a href="#">4</a> |
| C <sub>rate</sub> | ADC conversion rate            | ≤ 13-bit modes<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time | 20.000         | —                 | 818.330                | Ksps | <a href="#">5</a> |
| C <sub>rate</sub> | ADC conversion rate            | 16-bit mode<br>No ADC hardware averaging<br>Continuous conversions enabled, subsequent conversion time    | 37.037         | —                 | 461.467                | Ksps | <a href="#">5</a> |

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub> = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R<sub>AS</sub>/C<sub>AS</sub> time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.

5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

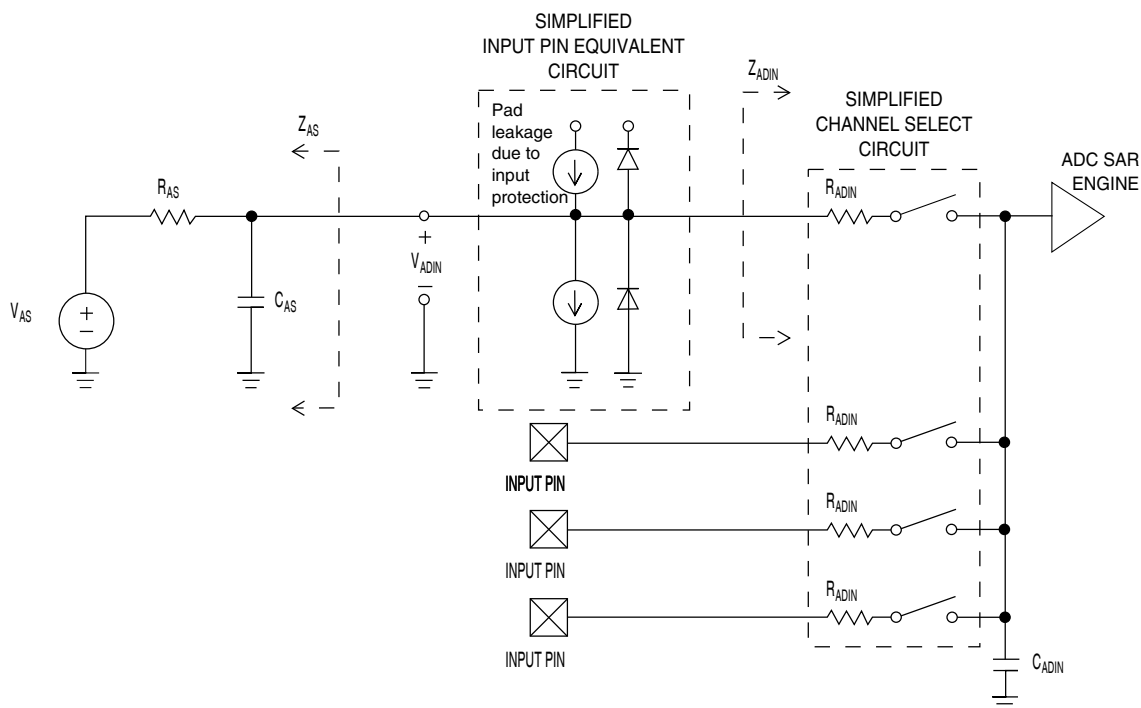


Figure 6. ADC input impedance equivalency diagram

### 6.6.1.2 16-bit ADC electrical characteristics

Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

| Symbol         | Description                   | Conditions <sup>1</sup>  | Min.                     | Typ. <sup>2</sup>        | Max.                         | Unit                     | Notes                     |
|----------------|-------------------------------|--|--------------------------|--------------------------|------------------------------|--------------------------|---------------------------|
| $I_{DDA\_ADC}$ | Supply current                |  | 0.215                    | —                        | 1.7                          | mA                       | 3                         |
| $f_{ADACK}$    | ADC asynchronous clock source | <ul style="list-style-type: none"> <li>ADLPC = 1, ADHSC = 0</li> <li>ADLPC = 1, ADHSC = 1</li> <li>ADLPC = 0, ADHSC = 0</li> <li>ADLPC = 0, ADHSC = 1</li> </ul> | 1.2<br>2.4<br>3.0<br>4.4 | 2.4<br>4.0<br>5.2<br>6.2 | 3.9<br>6.1<br>7.3<br>9.5     | MHz<br>MHz<br>MHz<br>MHz | $t_{ADACK} = 1/f_{ADACK}$ |
|                | Sample Time                   | See Reference Manual chapter for sample times  |                          |                          |                              |                          |                           |
| TUE            | Total unadjusted error        | <ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>   | —<br>—                   | ±4<br>±1.4               | ±6.8<br>±2.1                 | LSB <sup>4</sup>         | 5                         |
| DNL            | Differential non-linearity    | <ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>   | —<br>—                   | ±0.7<br>±0.2             | -1.1 to +1.9<br>-0.3 to 0.5  | LSB <sup>4</sup>         | 5                         |
| INL            | Integral non-linearity        | <ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>   | —<br>—                   | ±1.0<br>±0.5             | -2.7 to +1.9<br>-0.7 to +0.5 | LSB <sup>4</sup>         | 5                         |

Table continues on the next page...

**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

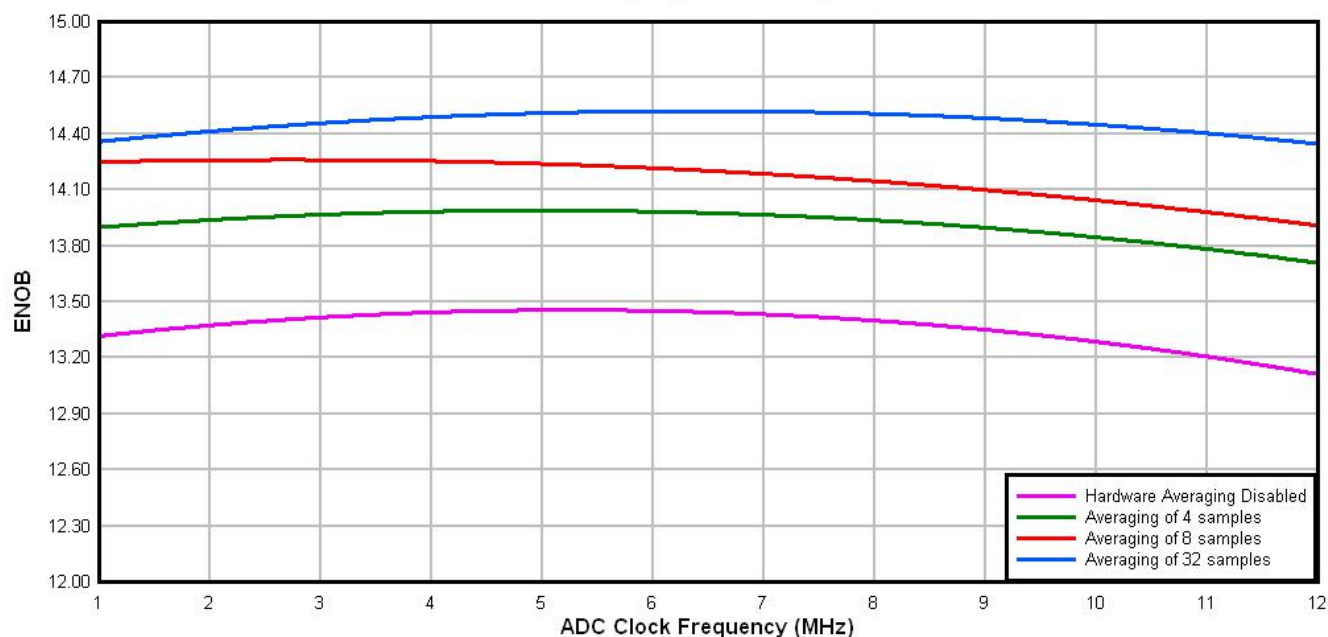
| Symbol       | Description                     | Conditions <sup>1</sup>   | Min.                             | Typ. <sup>2</sup> | Max.           | Unit             | Notes  |
|--------------|---------------------------------|---|----------------------------------|-------------------|----------------|------------------|--|
| $E_{FS}$     | Full-scale error                | <ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>  | —                                | -4                | -5.4           | LSB <sup>4</sup> | $V_{ADIN} = V_{DDA}$<br>5  |
| $E_Q$        | Quantization error              | <ul style="list-style-type: none"> <li>16-bit modes</li> <li><math>\leq 13</math>-bit modes</li> </ul>  | —                                | -1 to 0           | —<br>$\pm 0.5$ | LSB <sup>4</sup> |  |
| ENOB         | Effective number of bits        | 16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul> | 12.8<br>11.9                     | 14.5<br>13.8      | —<br>—         | bits<br>bits     | 6  |
| SINAD        | Signal-to-noise plus distortion | See ENOB  | $6.02 \times \text{ENOB} + 1.76$ |                   |                | dB               |  |
| THD          | Total harmonic distortion       | 16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>                                   | —                                | -94               | —              | dB               | 7  |
| SFDR         | Spurious free dynamic range     | 16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>                                   | 82                               | 95                | —              | dB               | 7  |
| $E_{IL}$     | Input leakage error             |   | $I_{IN} \times R_{AS}$           |                   |                | mV               | $I_{IN}$ = leakage current<br>(refer to the MCU's voltage and current operating ratings) |
|              | Temp sensor slope               | Across the full temperature range of the device   | 1.55                             | 1.62              | 1.69           | mV/°C            | 8  |
| $V_{TEMP25}$ | Temp sensor voltage             | 25 °C   | 706                              | 716               | 726            | mV               | 8  |

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
2. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.



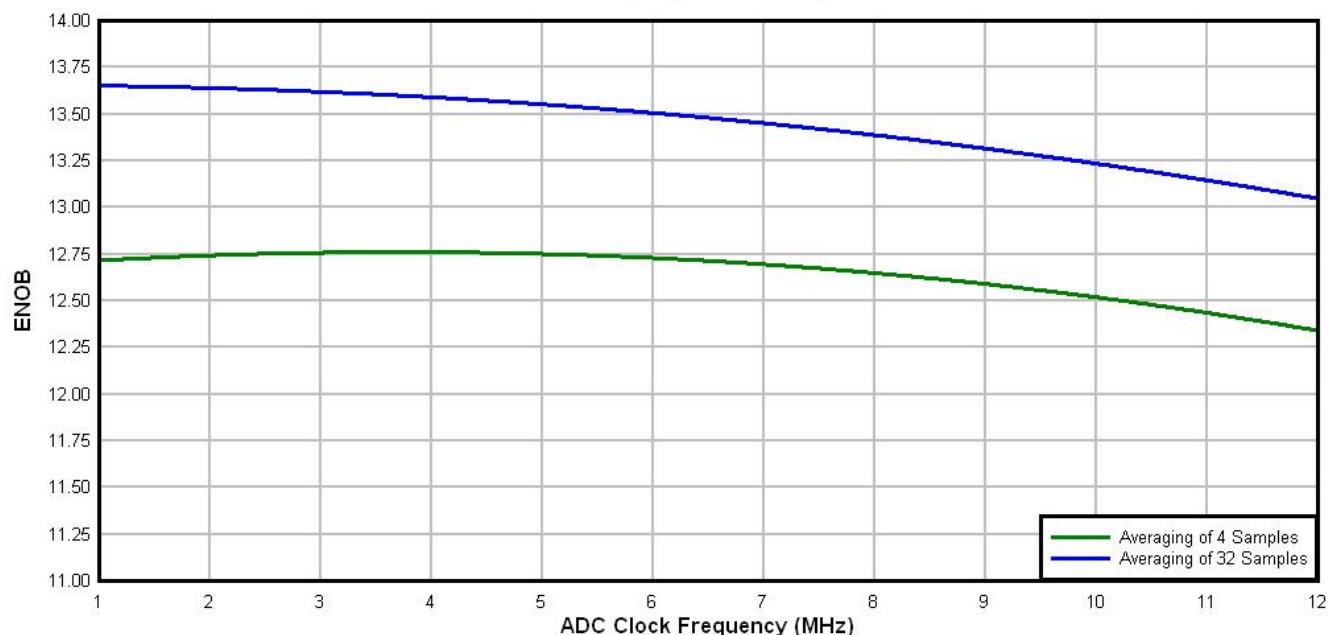
4.  $1 \text{ LSB} = (V_{\text{REFH}} - V_{\text{REFL}})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

**Typical ADC 16-bit Differential ENOB vs ADC Clock**  
100Hz, 90% FS Sine Input



**Figure 7. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**

**Typical ADC 16-bit Single-Ended ENOB vs ADC Clock**  
100Hz, 90% FS Sine Input



**Figure 8. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

## 6.6.2 CMP and 6-bit DAC electrical specifications

**Table 28. Comparator and 6-bit DAC electrical specifications**

| Symbol      | Description   | Min.           | Typ. | Max.     | Unit             |
|-------------|---|----------------|------|----------|------------------|
| $V_{DD}$    | Supply voltage                                      | 1.71           | —    | 3.6      | V                |
| $I_{DDHS}$  | Supply current, High-speed mode (EN=1, PMODE=1)     | —              | —    | 200      | $\mu$ A          |
| $I_{DDL S}$ | Supply current, low-speed mode (EN=1, PMODE=0)      | —              | —    | 20       | $\mu$ A          |
| $V_{AIN}$   | Analog input voltage                                | $V_{SS} - 0.3$ | —    | $V_{DD}$ | V                |
| $V_{AIO}$   | Analog input offset voltage                         | —              | —    | 20       | mV               |
| $V_H$       | Analog comparator hysteresis <sup>1</sup>           |                |      |          |                  |
|             | • CR0[HYSTCTR] = 00                                 | —              | 5    | —        | mV               |
|             | • CR0[HYSTCTR] = 01                                 | —              | 10   | —        | mV               |
|             | • CR0[HYSTCTR] = 10                                 | —              | 20   | —        | mV               |
|             | • CR0[HYSTCTR] = 11                                 | —              | 30   | —        | mV               |
| $V_{CMPOH}$ | Output high   | $V_{DD} - 0.5$ | —    | —        | V                |
| $V_{CMPOI}$ | Output low  | —              | —    | 0.5      | V                |
| $t_{DHS}$   | Propagation delay, high-speed mode (EN=1, PMODE=1)  | 20             | 50   | 200      | ns               |
| $t_{DLS}$   | Propagation delay, low-speed mode (EN=1, PMODE=0)   | 80             | 250  | 600      | ns               |
|             | Analog comparator initialization delay <sup>2</sup> | —              | —    | 40       | $\mu$ s          |
| $I_{DAC6b}$ | 6-bit DAC current adder (enabled)                   | —              | 7    | —        | $\mu$ A          |
| INL         | 6-bit DAC integral non-linearity                    | −0.5           | —    | 0.5      | LSB <sup>3</sup> |
| DNL         | 6-bit DAC differential non-linearity                | −0.3           | —    | 0.3      | LSB              |

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6$  V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$

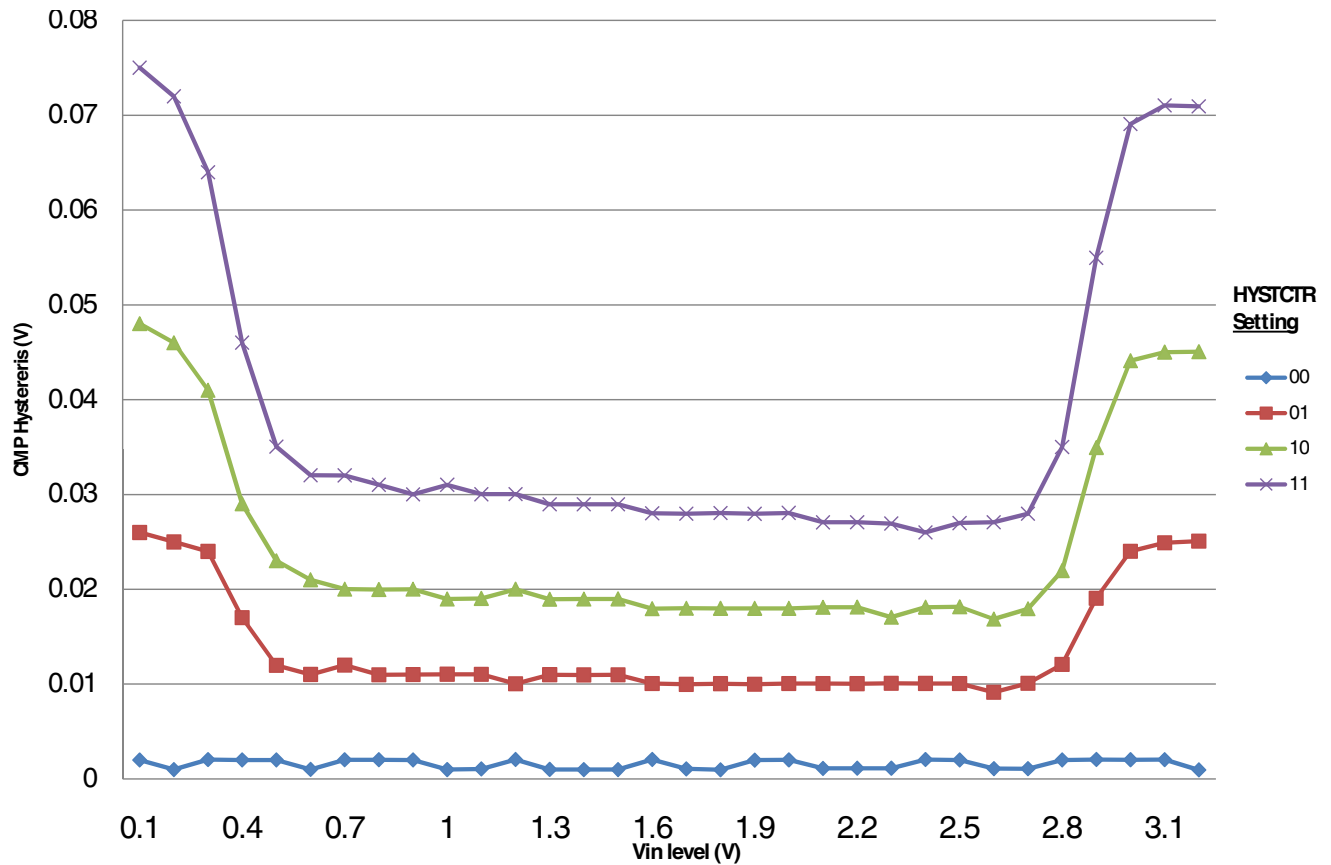


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

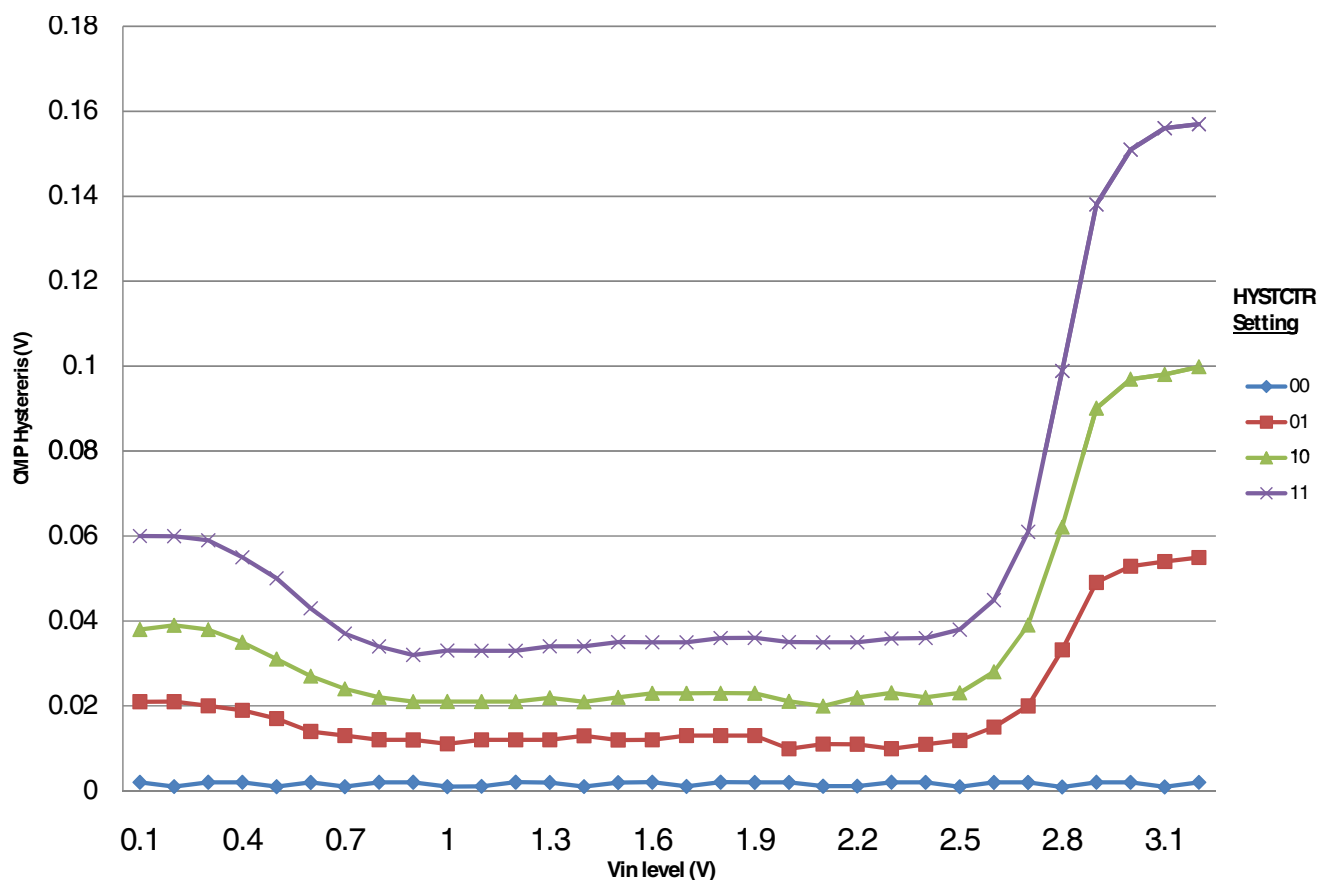


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

Table 29. 12-bit DAC operating requirements

| Symbol     | Description             | Min.                                      | Max. | Unit | Notes |
|------------|-------------------------|---|------|------|-------|
| $V_{DDA}$  | Supply voltage          | 1.71                                      | 3.6  | V    |       |
| $V_{DACR}$ | Reference voltage       | 1.13                                      | 3.6  | V    | 1     |
| $T_A$      | Temperature             | Operating temperature range of the device |      | °C   |       |
| $C_L$      | Output load capacitance | —   | 100  | pF   | 2     |
| $I_L$      | Output load current     | —   | 1    | mA   |       |

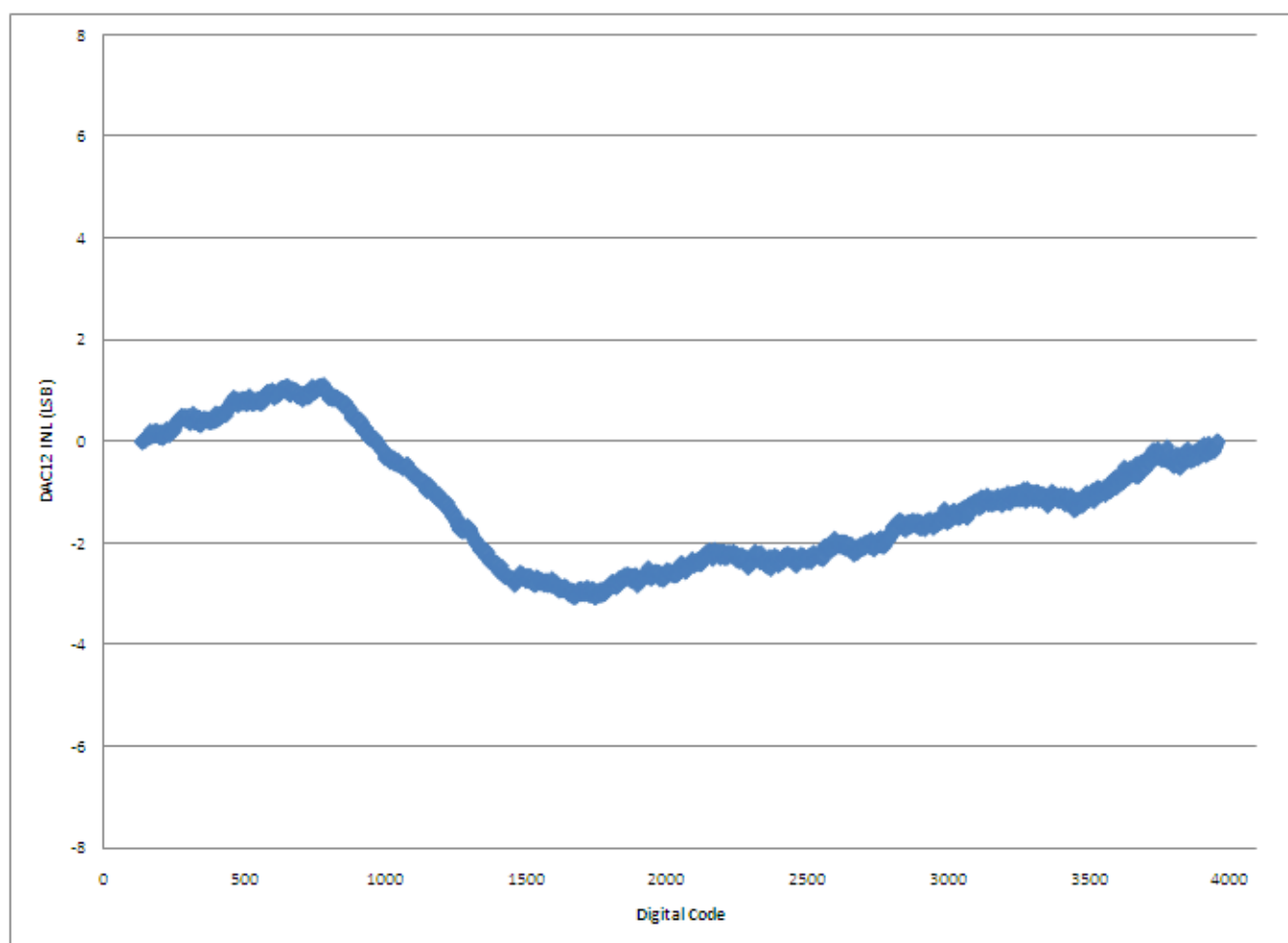
1. The DAC reference can be selected to be  $V_{DDA}$  or the voltage output of the VREF module (VREF\_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

## 6.6.3.2 12-bit DAC operating behaviors

Table 30. 12-bit DAC operating behaviors

| Symbol           | Description   | Min.             | Typ.        | Max.       | Unit       | Notes |
|------------------|---|------------------|-------------|------------|------------|-------|
| $I_{DDA\_DACLP}$ | Supply current — low-power mode   | —                | —           | 250        | $\mu A$    |       |
| $I_{DDA\_DACHP}$ | Supply current — high-speed mode  | —                | —           | 900        | $\mu A$    |       |
| $t_{DACLP}$      | Full-scale settling time (0x080 to 0xF7F) — low-power mode  | —                | 100         | 200        | $\mu s$    | 1     |
| $t_{DACHP}$      | Full-scale settling time (0x080 to 0xF7F) — high-power mode   | —                | 15          | 30         | $\mu s$    | 1     |
| $t_{CCDACLP}$    | Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode  | —                | 0.7         | 1          | $\mu s$    | 1     |
| $V_{dacoutl}$    | DAC output voltage range low — high-speed mode, no load, DAC set to 0x000   | —                | —           | 100        | mV         |       |
| $V_{dacouth}$    | DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF   | $V_{DACR} - 100$ | —           | $V_{DACR}$ | mV         |       |
| INL              | Integral non-linearity error — high speed mode  | —                | —           | $\pm 8$    | LSB        | 2     |
| DNL              | Differential non-linearity error — $V_{DACR} > 2 V$   | —                | —           | $\pm 1$    | LSB        | 3     |
| DNL              | Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$  | —                | —           | $\pm 1$    | LSB        | 4     |
| $V_{OFFSET}$     | Offset error  | —                | $\pm 0.4$   | $\pm 0.8$  | %FSR       | 5     |
| $E_G$            | Gain error  | —                | $\pm 0.1$   | $\pm 0.6$  | %FSR       | 5     |
| PSRR             | Power supply rejection ratio, $V_{DDA} \geq 2.4 V$  | 60               | —           | 90         | dB         |       |
| $T_{CO}$         | Temperature coefficient offset voltage  | —                | 3.7         | —          | $\mu V/C$  | 6     |
| $T_{GE}$         | Temperature coefficient gain error  | —                | 0.000421    | —          | %FSR/C     |       |
| $R_{op}$         | Output resistance (load = 3 k $\Omega$ )  | —                | —           | 250        | $\Omega$   |       |
| SR               | Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul> | 1.2<br>0.05      | 1.7<br>0.12 | —<br>—     | V/ $\mu s$ |       |
| BW               | 3dB bandwidth <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>               | 550<br>40        | —<br>—      | —<br>—     | kHz        |       |

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4 V$
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0 V$ , reference select set for  $V_{DDA}$  (DACx\_CO:DACRFS = 1), high power mode (DACx\_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device



**Figure 11. Typical INL error vs. digital code**

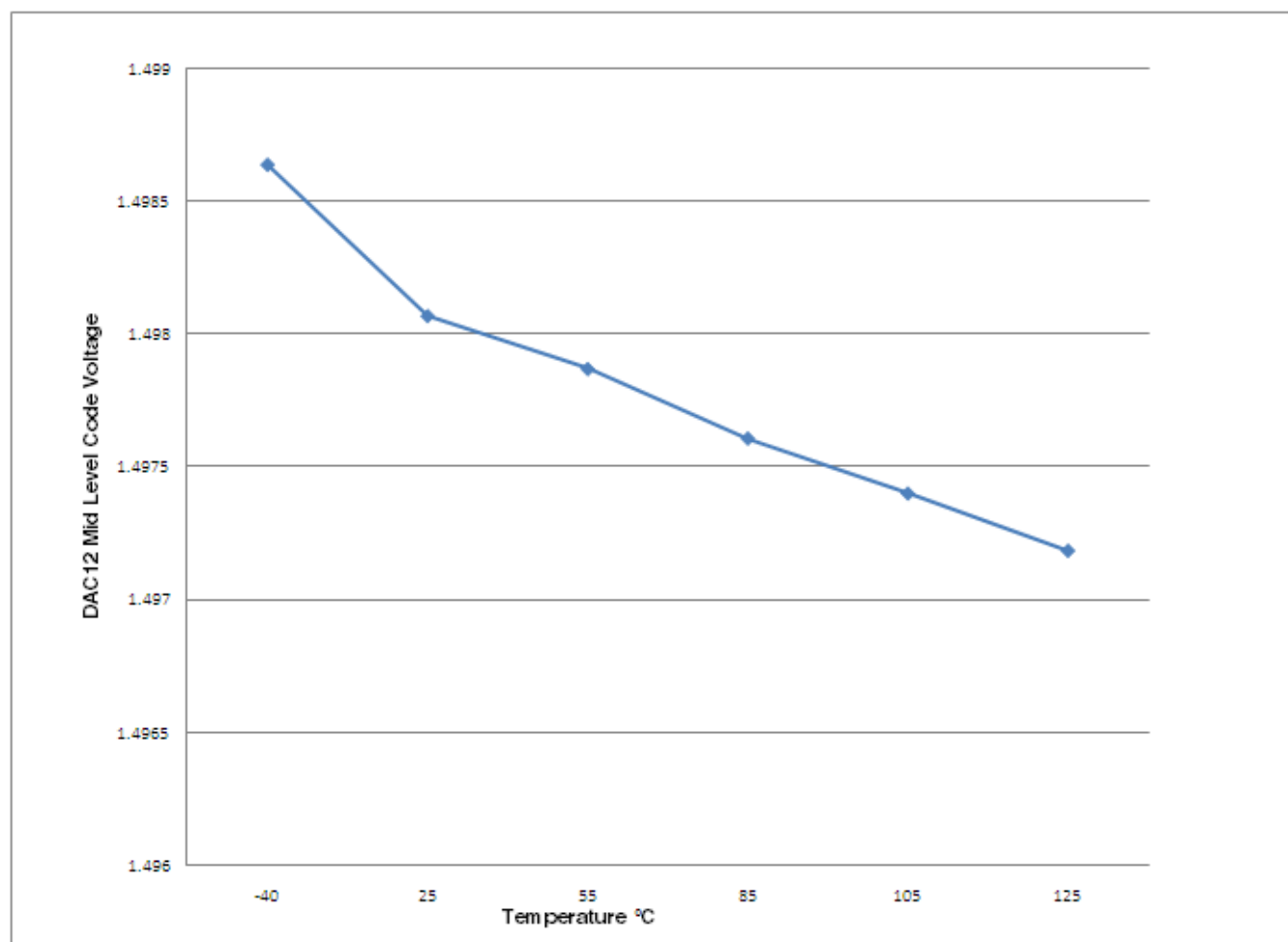


Figure 12. Offset at half scale vs. temperature

## 6.7 Timers

See [General switching specifications](#).

## 6.8 Communication interfaces

### 6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

## Peripheral operating requirements and behaviors

All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 31. SPI master mode timing on slew rate disabled pads**

| Num. | Symbol       | Description                    | Min.                  | Max.                     | Unit        | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1    | $f_{op}$     | Frequency of operation         | $f_{periph}/2048$     | $f_{periph}/2$           | Hz          | 1    |
| 2    | $t_{SPSCK}$  | SPSCK period                   | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns          | 2    |
| 3    | $t_{Lead}$   | Enable lead time               | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 4    | $t_{Lag}$    | Enable lag time                | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 5    | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$     | $1024 \times t_{periph}$ | ns          | —    |
| 6    | $t_{SU}$     | Data setup time (inputs)       | 18                    | —                        | ns          | —    |
| 7    | $t_{HI}$     | Data hold time (inputs)        | 0                     | —                        | ns          | —    |
| 8    | $t_v$        | Data valid (after SPSCK edge)  | —                     | 15                       | ns          | —    |
| 9    | $t_{HO}$     | Data hold time (outputs)       | 0                     | —                        | ns          | —    |
| 10   | $t_{RI}$     | Rise time input                | —                     | $t_{periph} - 25$        | ns          | —    |
|      | $t_{FI}$     | Fall time input                |                       |                          |             |      |
| 11   | $t_{RO}$     | Rise time output               | —                     | 25                       | ns          | —    |
|      | $t_{FO}$     | Fall time output               |                       |                          |             |      |

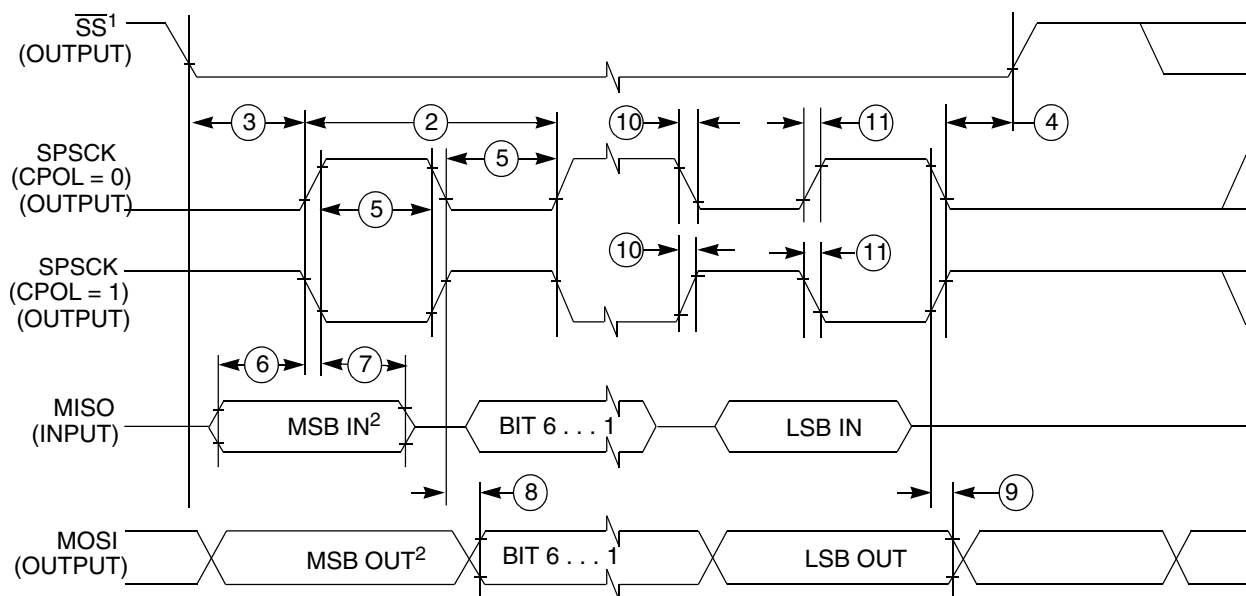
- For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
- $t_{periph} = 1/f_{periph}$

**Table 32. SPI master mode timing on slew rate enabled pads**

| Num. | Symbol       | Description                    | Min.                  | Max.                     | Unit        | Note |
|------|--------------|--------------------------------|-----------------------|--------------------------|-------------|------|
| 1    | $f_{op}$     | Frequency of operation         | $f_{periph}/2048$     | $f_{periph}/2$           | Hz          | 1    |
| 2    | $t_{SPSCK}$  | SPSCK period                   | $2 \times t_{periph}$ | $2048 \times t_{periph}$ | ns          | 2    |
| 3    | $t_{Lead}$   | Enable lead time               | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 4    | $t_{Lag}$    | Enable lag time                | 1/2                   | —                        | $t_{SPSCK}$ | —    |
| 5    | $t_{WSPSCK}$ | Clock (SPSCK) high or low time | $t_{periph} - 30$     | $1024 \times t_{periph}$ | ns          | —    |
| 6    | $t_{SU}$     | Data setup time (inputs)       | 96                    | —                        | ns          | —    |
| 7    | $t_{HI}$     | Data hold time (inputs)        | 0                     | —                        | ns          | —    |
| 8    | $t_v$        | Data valid (after SPSCK edge)  | —                     | 52                       | ns          | —    |
| 9    | $t_{HO}$     | Data hold time (outputs)       | 0                     | —                        | ns          | —    |
| 10   | $t_{RI}$     | Rise time input                | —                     | $t_{periph} - 25$        | ns          | —    |
|      | $t_{FI}$     | Fall time input                |                       |                          |             |      |
| 11   | $t_{RO}$     | Rise time output               | —                     | 36                       | ns          | —    |
|      | $t_{FO}$     | Fall time output               |                       |                          |             |      |

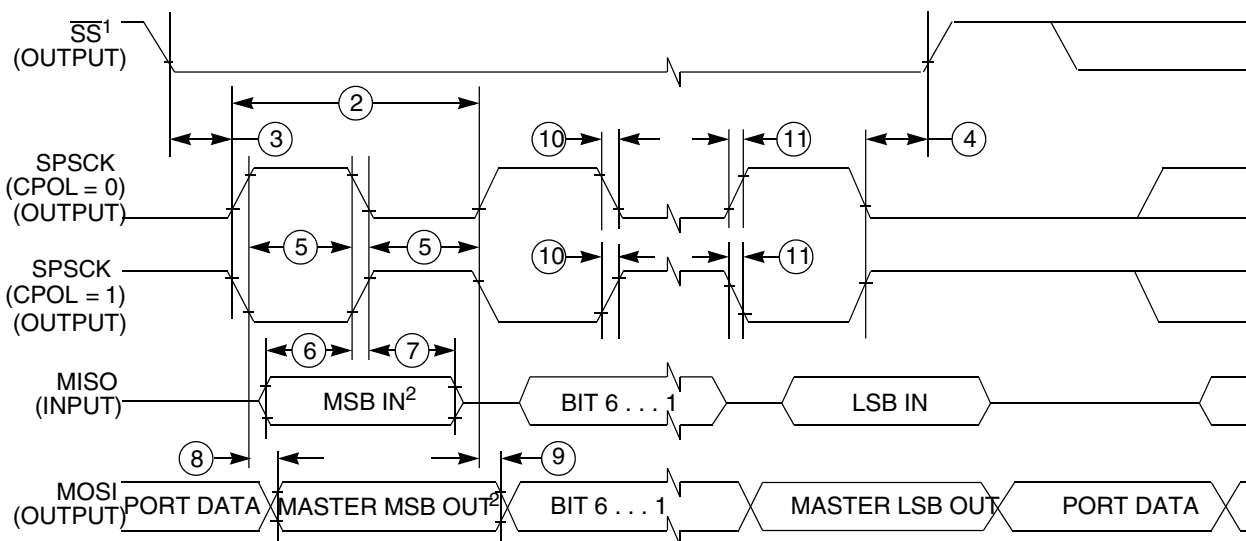
- For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
- $t_{periph} = 1/f_{periph}$





1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA = 0)**



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 1)**

**Table 33. SPI slave mode timing on slew rate disabled pads**

| Num. | Symbol        | Description                     | Min.                  | Max.           | Unit         | Note |
|------|---------------|---------------------------------|-----------------------|----------------|--------------|------|
| 1    | $f_{op}$      | Frequency of operation          | 0                     | $f_{periph}/4$ | Hz           | 1    |
| 2    | $t_{SPSCCK}$  | SPSCCK period                   | $4 \times t_{periph}$ | —              | ns           | 2    |
| 3    | $t_{Lead}$    | Enable lead time                | 1                     | —              | $t_{periph}$ | —    |
| 4    | $t_{Lag}$     | Enable lag time                 | 1                     | —              | $t_{periph}$ | —    |
| 5    | $t_{WSPSCCK}$ | Clock (SPSCCK) high or low time | $t_{periph} - 30$     | —              | ns           | —    |

Table continues on the next page...

**Table 33. SPI slave mode timing on slew rate disabled pads (continued)**

| Num. | Symbol    | Description                  | Min. | Max.              | Unit | Note |
|------|-----------|------------------------------|------|-------------------|------|------|
| 6    | $t_{SU}$  | Data setup time (inputs)     | 2.5  | —                 | ns   | —    |
| 7    | $t_{HI}$  | Data hold time (inputs)      | 3.5  | —                 | ns   | —    |
| 8    | $t_a$     | Slave access time            | —    | $t_{periph}$      | ns   | 3    |
| 9    | $t_{dis}$ | Slave MISO disable time      | —    | $t_{periph}$      | ns   | 4    |
| 10   | $t_v$     | Data valid (after SPSC edge) | —    | 31                | ns   | —    |
| 11   | $t_{HO}$  | Data hold time (outputs)     | 0    | —                 | ns   | —    |
| 12   | $t_{RI}$  | Rise time input              | —    | $t_{periph} - 25$ | ns   | —    |
|      | $t_{FI}$  | Fall time input              |      |                   |      |      |
| 13   | $t_{RO}$  | Rise time output             | —    | 25                | ns   | —    |
|      | $t_{FO}$  | Fall time output             |      |                   |      |      |

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

**Table 34. SPI slave mode timing on slew rate enabled pads**

| Num. | Symbol      | Description                   | Min.                  | Max.              | Unit         | Note |
|------|-------------|-------------------------------|-----------------------|-------------------|--------------|------|
| 1    | $f_{op}$    | Frequency of operation        | 0                     | $f_{periph}/4$    | Hz           | 1    |
| 2    | $t_{SPSC}$  | SPSC period                   | $4 \times t_{periph}$ | —                 | ns           | 2    |
| 3    | $t_{Lead}$  | Enable lead time              | 1                     | —                 | $t_{periph}$ | —    |
| 4    | $t_{Lag}$   | Enable lag time               | 1                     | —                 | $t_{periph}$ | —    |
| 5    | $t_{WSPSC}$ | Clock (SPSC) high or low time | $t_{periph} - 30$     | —                 | ns           | —    |
| 6    | $t_{SU}$    | Data setup time (inputs)      | 2                     | —                 | ns           | —    |
| 7    | $t_{HI}$    | Data hold time (inputs)       | 7                     | —                 | ns           | —    |
| 8    | $t_a$       | Slave access time             | —                     | $t_{periph}$      | ns           | 3    |
| 9    | $t_{dis}$   | Slave MISO disable time       | —                     | $t_{periph}$      | ns           | 4    |
| 10   | $t_v$       | Data valid (after SPSC edge)  | —                     | 122               | ns           | —    |
| 11   | $t_{HO}$    | Data hold time (outputs)      | 0                     | —                 | ns           | —    |
| 12   | $t_{RI}$    | Rise time input               | —                     | $t_{periph} - 25$ | ns           | —    |
|      | $t_{FI}$    | Fall time input               |                       |                   |              |      |
| 13   | $t_{RO}$    | Rise time output              | —                     | 36                | ns           | —    |
|      | $t_{FO}$    | Fall time output              |                       |                   |              |      |

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

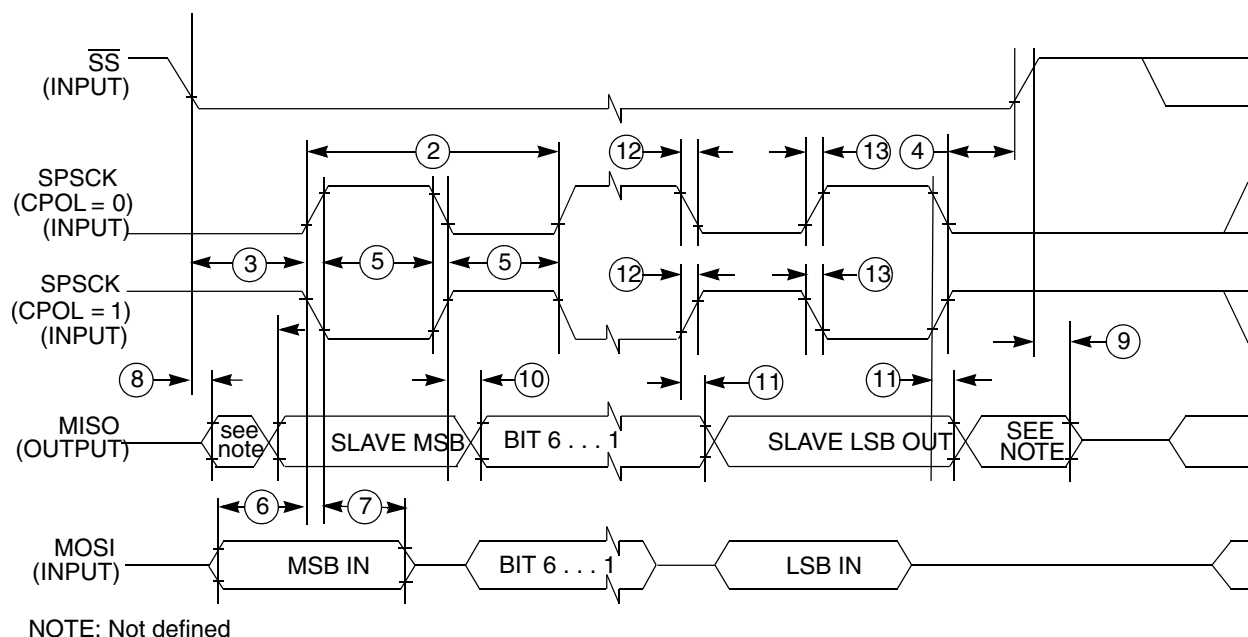


Figure 15. SPI slave mode timing (CPHA = 0)

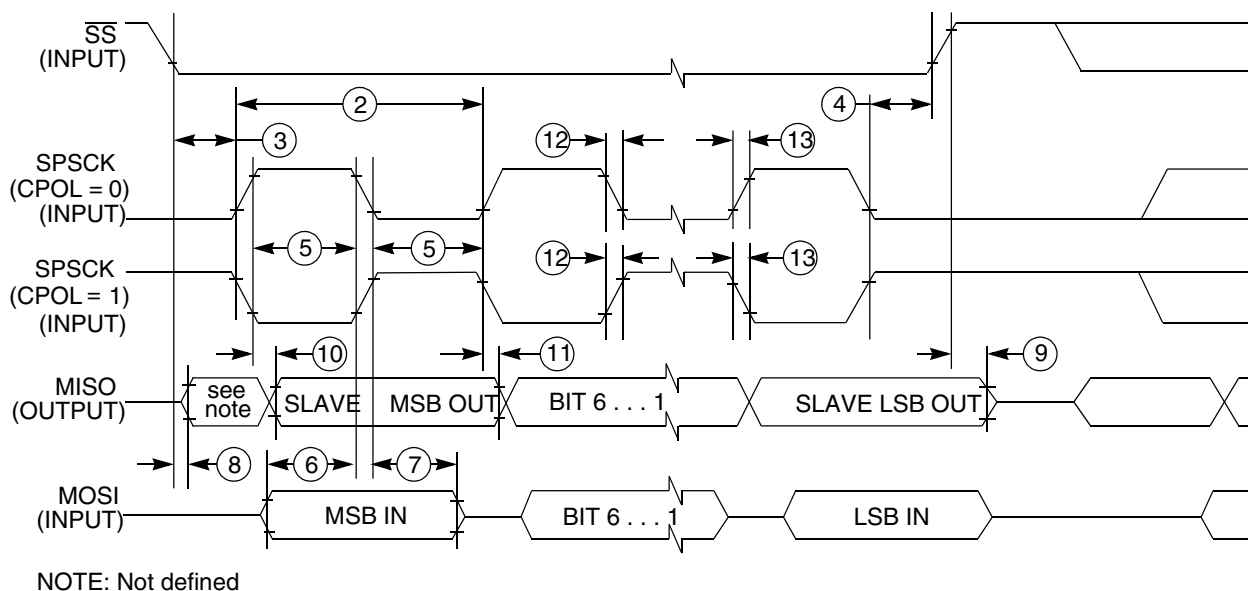


Figure 16. SPI slave mode timing (CPHA = 1)

## 6.8.2 I<sup>2</sup>C

See [General switching specifications](#).

## 6.8.3 UART

See [General switching specifications](#).

## 6.8.4 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

### 6.8.4.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

**Table 35. I2S/SAI master mode timing**

| Num. | Characteristic  | Min. | Max. | Unit        |
|------|---|------|------|-------------|
|      | Operating voltage   | 1.71 | 3.6  | V           |
| S1   | I2S_MCLK cycle time   | 40   | —    | ns          |
| S2   | I2S_MCLK (as an input) pulse width high/low                       | 45%  | 55%  | MCLK period |
| S3   | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)                       | 80   | —    | ns          |
| S4   | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low                      | 45%  | 55%  | BCLK period |
| S5   | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/<br>I2S_RX_FS output valid   | —    | 15.5 | ns          |
| S6   | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/<br>I2S_RX_FS output invalid | 0    | —    | ns          |
| S7   | I2S_TX_BCLK to I2S_TXD valid                                      | —    | 19   | ns          |
| S8   | I2S_TX_BCLK to I2S_TXD invalid                                    | 0    | —    | ns          |
| S9   | I2S_RXD/I2S_RX_FS input setup before<br>I2S_RX_BCLK               | 26   | —    | ns          |
| S10  | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK                    | 0    | —    | ns          |

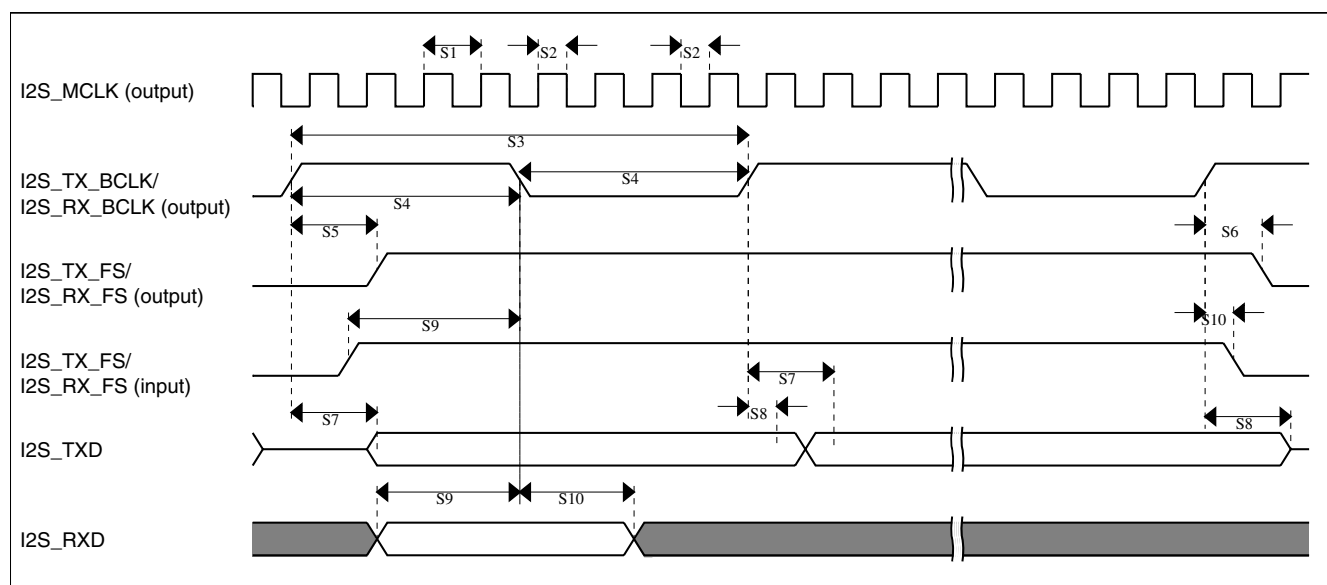


Figure 17. I2S/SAI timing — master modes

Table 36. I2S/SAI slave mode timing

| Num. | Characteristic   | Min. | Max. | Unit        |
|------|--|------|------|-------------|
|      | Operating voltage  | 1.71 | 3.6  | V           |
| S11  | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)                     | 80   | —    | ns          |
| S12  | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)           | 45%  | 55%  | MCLK period |
| S13  | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 10   | —    | ns          |
| S14  | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK   | 2    | —    | ns          |
| S15  | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid                  | —    | 33   | ns          |
| S16  | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid                | 0    | —    | ns          |
| S17  | I2S_RXD setup before I2S_RX_BCLK                               | 10   | —    | ns          |
| S18  | I2S_RXD hold after I2S_RX_BCLK                                 | 2    | —    | ns          |
| S19  | I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup> | —    | 28   | ns          |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

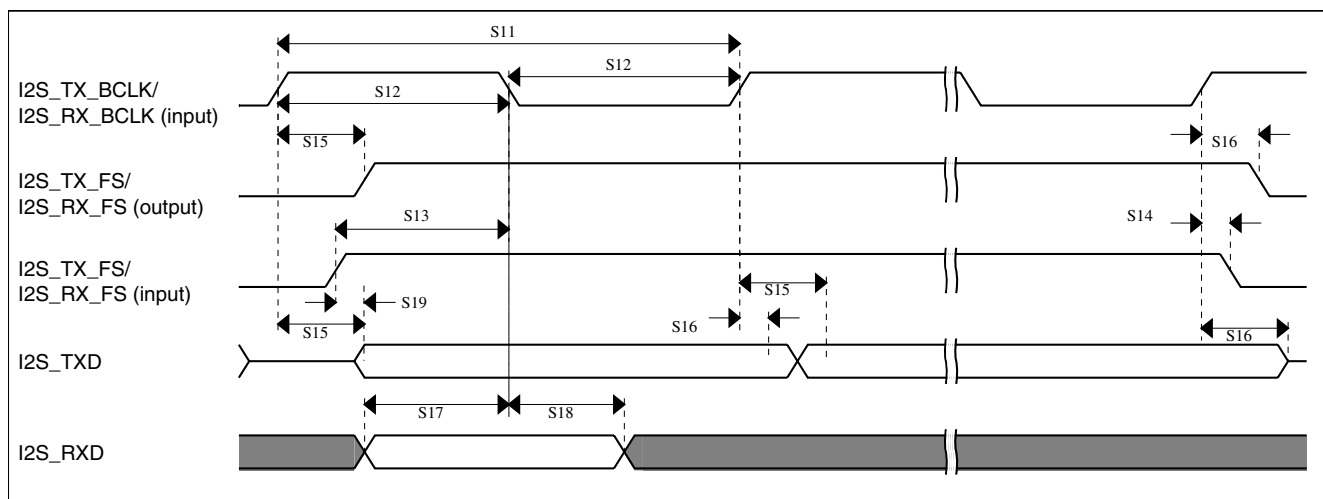


Figure 18. I2S/SAI timing — slave modes

### 6.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 37. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

| Num. | Characteristic  | Min. | Max. | Unit        |
|------|---|------|------|-------------|
|      | Operating voltage   | 1.71 | 3.6  | V           |
| S1   | I2S_MCLK cycle time   | 62.5 | —    | ns          |
| S2   | I2S_MCLK pulse width high/low                                     | 45%  | 55%  | MCLK period |
| S3   | I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)                       | 250  | —    | ns          |
| S4   | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low                      | 45%  | 55%  | BCLK period |
| S5   | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/<br>I2S_RX_FS output valid   | —    | 45   | ns          |
| S6   | I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/<br>I2S_RX_FS output invalid | 0    | —    | ns          |
| S7   | I2S_TX_BCLK to I2S_TXD valid                                      | —    | 45   | ns          |
| S8   | I2S_TX_BCLK to I2S_TXD invalid                                    | 0    | —    | ns          |
| S9   | I2S_RXD/I2S_RX_FS input setup before<br>I2S_RX_BCLK               | 75   | —    | ns          |
| S10  | I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK                    | 0    | —    | ns          |

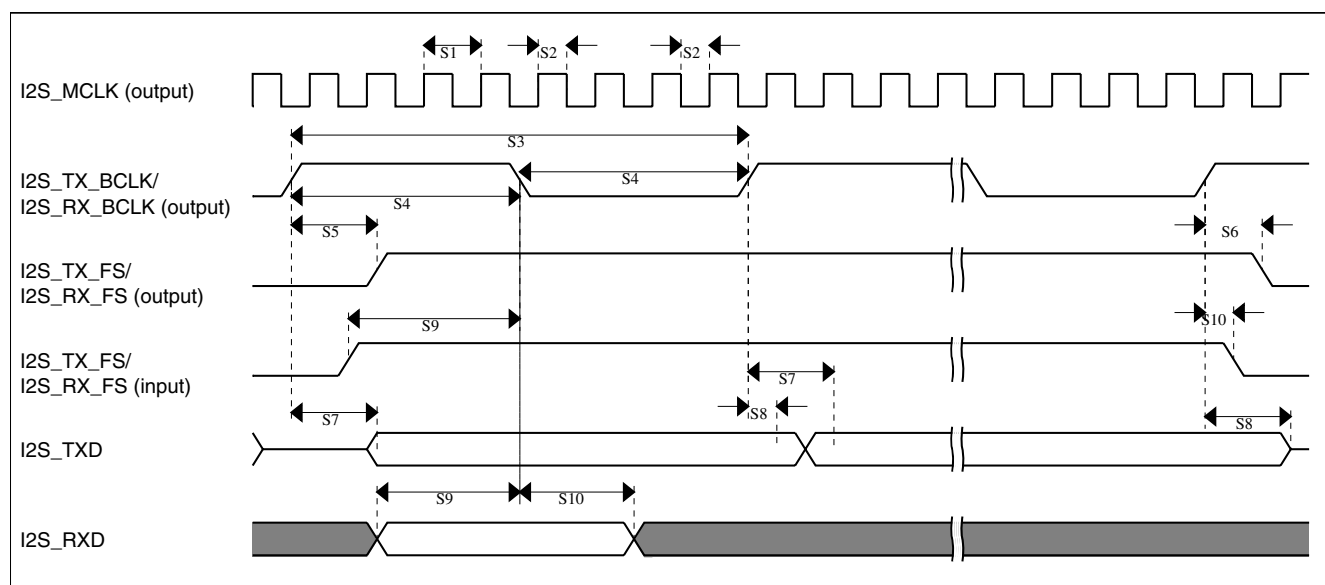


Figure 19. I2S/SAI timing — master modes

Table 38. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

| Num. | Characteristic   | Min. | Max. | Unit        |
|------|--|------|------|-------------|
|      | Operating voltage  | 1.71 | 3.6  | V           |
| S11  | I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)                     | 250  | —    | ns          |
| S12  | I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)           | 45%  | 55%  | MCLK period |
| S13  | I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK | 30   | —    | ns          |
| S14  | I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK   | 2    | —    | ns          |
| S15  | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid                  | —    | 87   | ns          |
| S16  | I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid                | 0    | —    | ns          |
| S17  | I2S_RXD setup before I2S_RX_BCLK                               | 30   | —    | ns          |
| S18  | I2S_RXD hold after I2S_RX_BCLK                                 | 2    | —    | ns          |
| S19  | I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup> | —    | 72   | ns          |

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

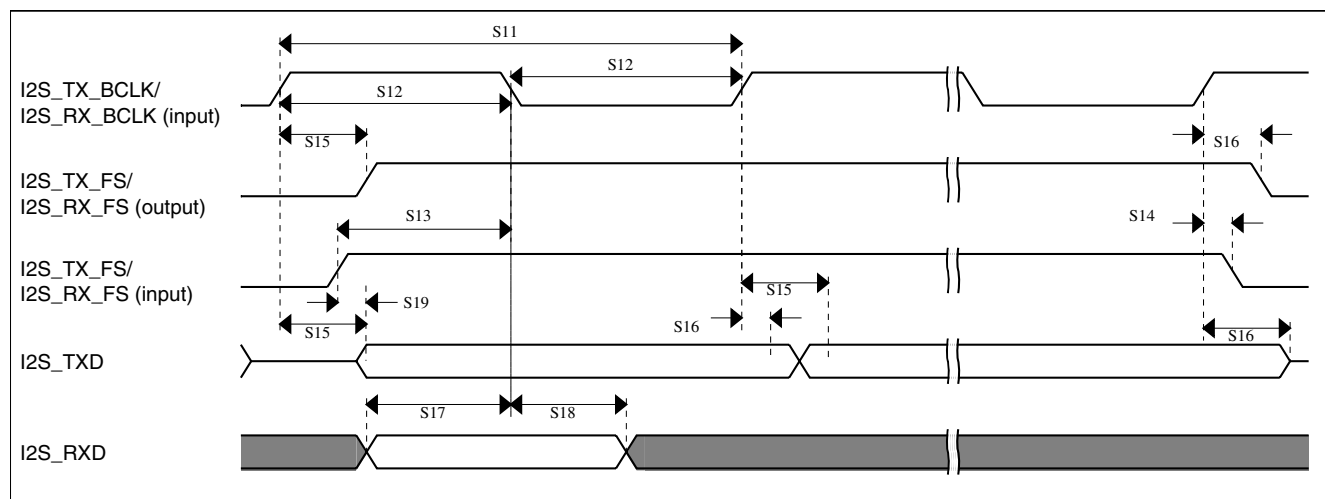


Figure 20. I2S/SAI timing — slave modes

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

Table 39. TSI electrical specifications

| Symbol    | Description  | Min. | Typ. | Max. | Unit |
|-----------|--|------|------|------|------|
| TSI_RUNF  | Fixed power consumption in run mode  | —    | 100  | —    | μA   |
| TSI_RUNV  | Variable power consumption in run mode (depends on oscillator's current selection) | 1.0  | —    | 128  | μA   |
| TSI_EN    | Power consumption in enable mode   | —    | 100  | —    | μA   |
| TSI_DIS   | Power consumption in disable mode  | —    | 1.2  | —    | μA   |
| TSI_TEN   | TSI analog enable time   | —    | 66   | —    | μs   |
| TSI_CREF  | TSI reference capacitor  | —    | 1.0  | —    | pF   |
| TSI_DVOLT | Voltage variation of VP & VM around nominal values                                 | 0.19 | —    | 1.03 | V    |

### 6.9.2 LCD electrical characteristics

Table 40. LCD electricals

| Symbol      | Description         | Min. | Typ. | Max.  | Unit | Notes |
|-------------|---------------------|------|------|-------|------|-------|
| $f_{Frame}$ | LCD frame frequency |      |      |       |      |       |
|             | • GCR[FFR]=0        | 23.3 | —    | 73.1  | Hz   |       |
|             | • GCR[FFR]=1        | 46.6 | —    | 146.2 | Hz   |       |

Table continues on the next page...



**Table 40. LCD electricals (continued)**

| Symbol           | Description   | Min. | Typ. | Max.                | Unit         | Notes |
|------------------|---|------|------|---------------------|--------------|-------|
| $C_{LCD}$        | LCD charge pump capacitance — nominal value   | —    | 100  | —                   | nF           | 1     |
| $C_{BYLCD}$      | LCD bypass capacitance — nominal value  | —    | 100  | —                   | nF           | 1     |
| $C_{Glass}$      | LCD glass capacitance   | —    | 2000 | 8000                | pF           | 2     |
| $V_{IREG}$       | $V_{IREG}$ <ul style="list-style-type: none"> <li>RVTRIM=0000</li> <li>RVTRIM=1000</li> <li>RVTRIM=0100</li> <li>RVTRIM=1100</li> <li>RVTRIM=0010</li> <li>RVTRIM=1010</li> <li>RVTRIM=0110</li> <li>RVTRIM=1110</li> <li>RVTRIM=0001</li> <li>RVTRIM=1001</li> <li>RVTRIM=0101</li> <li>RVTRIM=1101</li> <li>RVTRIM=0011</li> <li>RVTRIM=1011</li> <li>RVTRIM=0111</li> <li>RVTRIM=1111</li> </ul> | —    | 0.91 | —                   | V            | 3     |
| $\Delta_{RTRIM}$ | $V_{IREG}$ TRIM resolution  | —    | —    | 3.0                 | % $V_{IREG}$ |       |
| $I_{VIREG}$      | $V_{IREG}$ current adder — RVEN = 1   | —    | 1    | —                   | $\mu A$      | 4     |
| $I_{RBIAS}$      | RBIAS current adder <ul style="list-style-type: none"> <li>LADJ = 10 or 11 — High load (LCD glass capacitance <math>\leq 8000</math> pF)</li> <li>LADJ = 00 or 01 — Low load (LCD glass capacitance <math>\leq 2000</math> pF)</li> </ul>   | —    | 10   | —                   | $\mu A$      |       |
| $R_{RBIAS}$      | RBIAS resistor values <ul style="list-style-type: none"> <li>LADJ = 10 or 11 — High load (LCD glass capacitance <math>\leq 8000</math> pF)</li> <li>LADJ = 00 or 01 — Low load (LCD glass capacitance <math>\leq 2000</math> pF)</li> </ul>   | —    | 0.28 | —                   | M $\Omega$   |       |
|                  |   | —    | 2.98 | —                   | M $\Omega$   |       |
| VLL1             | VLL1 voltage  | —    | —    | $V_{IREG}$          | V            | 5     |
| VLL2             | VLL2 voltage  | —    | —    | $2 \times V_{IREG}$ | V            | 5     |
| VLL3             | VLL3 voltage  | —    | —    | $3 \times V_{IREG}$ | V            | 5     |
| VLL1             | VLL1 voltage  | —    | —    | $V_{DDA} / 3$       | V            | 6     |
| VLL2             | VLL2 voltage  | —    | —    | $V_{DDA} / 1.5$     | V            | 6     |
| VLL3             | VLL3 voltage  | —    | —    | $V_{DDA}$           | V            | 6     |

1. The actual value used could vary with tolerance.

## Dimensions

- For highest glass capacitance values, LCD\_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
- V<sub>IREG</sub> maximum should never be externally driven to any level other than V<sub>DD</sub> - 0.15 V
- 2000 pF load LCD, 32 Hz frame frequency
- VLL1, VLL2 and VLL3 are a function of V<sub>IREG</sub> only when the regulator is enabled (GCR[RVEN]=1) and the charge pump is enabled (GCR[CPSEL]=1).
- VLL1, VLL2 and VLL3 are a function of V<sub>DDA</sub> only under either of the following conditions:
  - The charge pump is enabled (GCR[CPSEL]=1), the regulator is disabled (GCR[RVEN]=0), and VLL3 = V<sub>DDA</sub> through the internal power switch (GCR[VSUPPLY]=0).
  - The resistor bias string is enabled (GCR[CPSEL]=0), the regulator is disabled (GCR[RVEN]=0), and VLL3 is connected to V<sub>DDA</sub> externally (GCR[VSUPPLY]=1).

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|--|-------------------------------|
| 64-pin LQFP                              | 98ASS23234W                   |
| 64-pin MAPBGA                            | 98ASA00420D                   |
| 100-pin LQFP                             | 98ASS23308W                   |
| 121-pin MAPBGA                           | 98ASA00344D                   |

## 8 Pinout

### 8.1 KL36 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 121 BGA | 100 LQFP | 64 BGA | 64 LQFP | Pin Name | Default  | ALT0    | ALT1 | ALT2      | ALT3     | ALT4       | ALT5      | ALT6     | ALT7    |
|---------|----------|--------|---------|----------|----------|---------|------|-----------|----------|------------|-----------|----------|---------|
| E4      | 1        | A1     | 1       | PTE0     | DISABLED | LCD_P48 | PTE0 | SPI1_MISO | UART1_TX | RTC_CLKOUT | CMP0_OUT  | I2C1_SDA | LCD_P48 |
| E3      | 2        | B1     | 2       | PTE1     | DISABLED | LCD_P49 | PTE1 | SPI1_MOSI | UART1_RX |            | SPI1_MISO | I2C1_SCL | LCD_P49 |
| E2      | 3        | —      | —       | PTE2     | DISABLED | LCD_P50 | PTE2 | SPI1_SCK  |          |            |           |          | LCD_P50 |

| 121<br>BGA | 100<br>LQFP | 64<br>BGA | 64<br>LQFP | Pin Name | Default                             | ALT0                                | ALT1  | ALT2      | ALT3     | ALT4       | ALT5             | ALT6        | ALT7    |
|------------|-------------|-----------|------------|----------|-------------------------------------|-------------------------------------|-------|-----------|----------|------------|------------------|-------------|---------|
| F4         | 4           | —         | —          | PTE3     | DISABLED                            | LCD_P51                             | PTE3  | SPI1_MISO |          |            | SPI1_MOSI        |             | LCD_P51 |
| H7         | 5           | —         | —          | PTE4     | DISABLED                            | LCD_P52                             | PTE4  | SPI1_PCS0 |          |            |                  |             | LCD_P52 |
| G4         | 6           | —         | —          | PTE5     | DISABLED                            | LCD_P53                             | PTE5  |           |          |            |                  |             | LCD_P53 |
| F3         | 7           | —         | —          | PTE6     | DISABLED                            | LCD_P54                             | PTE6  |           |          | I2S0_MCLK  | audioUSB_SOF_OUT |             | LCD_P54 |
| E6         | 8           | —         | 3          | VDD      | VDD                                 | VDD                                 |       |           |          |            |                  |             |         |
| G7         | 9           | C4        | 4          | VSS      | VSS                                 | VSS                                 |       |           |          |            |                  |             |         |
| L6         | —           | —         | —          | VSS      | VSS                                 | VSS                                 |       |           |          |            |                  |             |         |
| H1         | 14          | E1        | 5          | PTE16    | ADC0_DP1/<br>ADC0_SE1               | LCD_P55/<br>ADC0_DP1/<br>ADC0_SE1   | PTE16 | SPI0_PCS0 | UART2_TX | TPM_CLKIN0 |                  |             | LCD_P55 |
| H2         | 15          | D1        | 6          | PTE17    | ADC0_DM1/<br>ADC0_SE5a              | LCD_P56/<br>ADC0_DM1/<br>ADC0_SE5a  | PTE17 | SPI0_SCK  | UART2_RX | TPM_CLKIN1 |                  | LPTMR0_ALT3 | LCD_P56 |
| J1         | 16          | E2        | 7          | PTE18    | ADC0_DP2/<br>ADC0_SE2               | LCD_P57/<br>ADC0_DP2/<br>ADC0_SE2   | PTE18 | SPI0_MOSI |          | I2C0_SDA   | SPI0_MISO        |             | LCD_P57 |
| J2         | 17          | D2        | 8          | PTE19    | ADC0_DM2/<br>ADC0_SE6a              | LCD_P58/<br>ADC0_DM2/<br>ADC0_SE6a  | PTE19 | SPI0_MISO |          | I2C0_SCL   | SPI0_MOSI        |             | LCD_P58 |
| K1         | 18          | G1        | 9          | PTE20    | ADC0_DP0/<br>ADC0_SE0               | LCD_P59/<br>ADC0_DP0/<br>ADC0_SE0   | PTE20 |           | TPM1_CH0 | UART0_TX   |                  |             | LCD_P59 |
| K2         | 19          | F1        | 10         | PTE21    | ADC0_DM0/<br>ADC0_SE4a              | LCD_P60/<br>ADC0_DM0/<br>ADC0_SE4a  | PTE21 |           | TPM1_CH1 | UART0_RX   |                  |             | LCD_P60 |
| L1         | 20          | G2        | 11         | PTE22    | ADC0_DP3/<br>ADC0_SE3               | ADC0_DP3/<br>ADC0_SE3               | PTE22 |           | TPM2_CH0 | UART2_TX   |                  |             |         |
| L2         | 21          | F2        | 12         | PTE23    | ADC0_DM3/<br>ADC0_SE7a              | ADC0_DM3/<br>ADC0_SE7a              | PTE23 |           | TPM2_CH1 | UART2_RX   |                  |             |         |
| F5         | 22          | F4        | 13         | VDDA     | VDDA                                | VDDA                                |       |           |          |            |                  |             |         |
| G5         | 23          | G4        | 14         | VREFH    | VREFH                               | VREFH                               |       |           |          |            |                  |             |         |
| G6         | 24          | G3        | 15         | VREFL    | VREFL                               | VREFL                               |       |           |          |            |                  |             |         |
| F6         | 25          | F3        | 16         | VSSA     | VSSA                                | VSSA                                |       |           |          |            |                  |             |         |
| L3         | 26          | H1        | 17         | PTE29    | CMP0_IN5/<br>ADC0_SE4b              | CMP0_IN5/<br>ADC0_SE4b              | PTE29 |           | TPM0_CH2 | TPM_CLKIN0 |                  |             |         |
| K5         | 27          | H2        | 18         | PTE30    | DAC0_OUT/<br>ADC0_SE23/<br>CMP0_IN4 | DAC0_OUT/<br>ADC0_SE23/<br>CMP0_IN4 | PTE30 |           | TPM0_CH3 | TPM_CLKIN1 |                  |             |         |
| L4         | 28          | H3        | 19         | PTE31    | DISABLED                            |                                     | PTE31 |           | TPM0_CH4 |            |                  |             |         |
| L5         | 29          | —         | —          | VSS      | VSS                                 | VSS                                 |       |           |          |            |                  |             |         |
| K6         | 30          | —         | —          | VDD      | VDD                                 | VDD                                 |       |           |          |            |                  |             |         |
| H5         | 31          | H4        | 20         | PTE24    | DISABLED                            |                                     | PTE24 |           | TPM0_CH0 |            | I2C0_SCL         |             |         |
| J5         | 32          | H5        | 21         | PTE25    | DISABLED                            |                                     | PTE25 |           | TPM0_CH1 |            | I2C0_SDA         |             |         |
| H6         | 33          | —         | —          | PTE26    | DISABLED                            |                                     | PTE26 |           | TPM0_CH5 |            |                  | RTC_CLKOUT  |         |
| J6         | 34          | D3        | 22         | PTA0     | SWD_CLK                             | TSIO_CH1                            | PTA0  |           | TPM0_CH5 |            |                  |             | SWD_CLK |

## Pinout

| 121 BGA | 100 LQFP | 64 BGA | 64 LQFP | Pin Name         | Default                           | ALT0                              | ALT1             | ALT2      | ALT3     | ALT4       | ALT5      | ALT6         | ALT7      |
|---------|----------|--------|---------|------------------|-----------------------------------|-----------------------------------|------------------|-----------|----------|------------|-----------|--------------|-----------|
| H8      | 35       | D4     | 23      | PTA1             | DISABLED                          | TSIO_CH2                          | PTA1             | UART0_RX  | TPM2_CH0 |            |           |              |           |
| J7      | 36       | E5     | 24      | PTA2             | DISABLED                          | TSIO_CH3                          | PTA2             | UART0_TX  | TPM2_CH1 |            |           |              |           |
| H9      | 37       | D5     | 25      | PTA3             | SWD_DIO                           | TSIO_CH4                          | PTA3             | I2C1_SCL  | TPM0_CH0 |            |           |              | SWD_DIO   |
| J8      | 38       | G5     | 26      | PTA4             | NMI_b                             | TSIO_CH5                          | PTA4             | I2C1_SDA  | TPM0_CH1 |            |           |              | NMI_b     |
| K7      | 39       | F5     | 27      | PTA5             | DISABLED                          |                                   | PTA5             |           | TPM0_CH2 |            |           | I2S0_TX_BCLK |           |
| E5      | —        | —      | —       | VDD              | VDD                               | VDD                               |                  |           |          |            |           |              |           |
| G3      | —        | —      | —       | VSS              | VSS                               | VSS                               |                  |           |          |            |           |              |           |
| K3      | 40       | —      | —       | PTA6             | DISABLED                          |                                   | PTA6             |           | TPM0_CH3 |            |           |              |           |
| H4      | 41       | —      | —       | PTA7             | DISABLED                          |                                   | PTA7             |           | TPM0_CH4 |            |           |              |           |
| K8      | 42       | H6     | 28      | PTA12            | DISABLED                          |                                   | PTA12            |           | TPM1_CH0 |            |           | I2S0_TXD0    |           |
| L8      | 43       | G6     | 29      | PTA13            | DISABLED                          |                                   | PTA13            |           | TPM1_CH1 |            |           | I2S0_TX_FS   |           |
| K9      | 44       | —      | —       | PTA14            | DISABLED                          |                                   | PTA14            | SPI0_PCS0 | UART0_TX |            |           | I2S0_RX_BCLK | I2S0_TXD0 |
| L9      | 45       | —      | —       | PTA15            | DISABLED                          |                                   | PTA15            | SPI0_SCK  | UART0_RX |            |           | I2S0_RXD0    |           |
| J10     | 46       | —      | —       | PTA16            | DISABLED                          |                                   | PTA16            | SPI0_MOSI |          |            | SPI0_MISO | I2S0_RX_FS   | I2S0_RXD0 |
| H10     | 47       | —      | —       | PTA17            | DISABLED                          |                                   | PTA17            | SPI0_MISO |          |            | SPI0_MOSI | I2S0_MCLK    |           |
| L10     | 48       | G7     | 30      | VDD              | VDD                               | VDD                               |                  |           |          |            |           |              |           |
| K10     | 49       | H7     | 31      | VSS              | VSS                               | VSS                               |                  |           |          |            |           |              |           |
| L11     | 50       | H8     | 32      | PTA18            | EXTAL0                            | EXTAL0                            | PTA18            |           | UART1_RX | TPM_CLKIN0 |           |              |           |
| K11     | 51       | G8     | 33      | PTA19            | XTAL0                             | XTAL0                             | PTA19            |           | UART1_TX | TPM_CLKIN1 |           | LPTMR0_ALT1  |           |
| J11     | 52       | F8     | 34      | PTA20            | RESET_b                           |                                   | PTA20            |           |          |            |           |              | RESET_b   |
| G11     | 53       | F7     | 35      | PTB0/<br>LLWU_P5 | LCD_P0/<br>ADC0_SE8/<br>TSIO_CH0  | LCD_P0/<br>ADC0_SE8/<br>TSIO_CH0  | PTB0/<br>LLWU_P5 | I2C0_SCL  | TPM1_CH0 |            |           |              | LCD_P0    |
| G10     | 54       | F6     | 36      | PTB1             | LCD_P1/<br>ADC0_SE9/<br>TSIO_CH6  | LCD_P1/<br>ADC0_SE9/<br>TSIO_CH6  | PTB1             | I2C0_SDA  | TPM1_CH1 |            |           |              | LCD_P1    |
| G9      | 55       | E7     | 37      | PTB2             | LCD_P2/<br>ADC0_SE12/<br>TSIO_CH7 | LCD_P2/<br>ADC0_SE12/<br>TSIO_CH7 | PTB2             | I2C0_SCL  | TPM2_CH0 |            |           |              | LCD_P2    |
| G8      | 56       | E8     | 38      | PTB3             | LCD_P3/<br>ADC0_SE13/<br>TSIO_CH8 | LCD_P3/<br>ADC0_SE13/<br>TSIO_CH8 | PTB3             | I2C0_SDA  | TPM2_CH1 |            |           |              | LCD_P3    |
| E11     | 57       | —      | —       | PTB7             | LCD_P7                            | LCD_P7                            | PTB7             |           |          |            |           |              | LCD_P7    |
| D11     | 58       | —      | —       | PTB8             | LCD_P8                            | LCD_P8                            | PTB8             | SPI1_PCS0 | EXTRG_IN |            |           |              | LCD_P8    |
| E10     | 59       | —      | —       | PTB9             | LCD_P9                            | LCD_P9                            | PTB9             | SPI1_SCK  |          |            |           |              | LCD_P9    |
| D10     | 60       | —      | —       | PTB10            | LCD_P10                           | LCD_P10                           | PTB10            | SPI1_PCS0 |          |            |           |              | LCD_P10   |
| C10     | 61       | —      | —       | PTB11            | LCD_P11                           | LCD_P11                           | PTB11            | SPI1_SCK  |          |            |           |              | LCD_P11   |
| B10     | 62       | E6     | 39      | PTB16            | LCD_P12/<br>TSIO_CH9              | LCD_P12/<br>TSIO_CH9              | PTB16            | SPI1_MOSI | UART0_RX | TPM_CLKIN0 | SPI1_MISO |              | LCD_P12   |
| E9      | 63       | D7     | 40      | PTB17            | LCD_P13/<br>TSIO_CH10             | LCD_P13/<br>TSIO_CH10             | PTB17            | SPI1_MISO | UART0_TX | TPM_CLKIN1 | SPI1_MOSI |              | LCD_P13   |

| 121<br>BGA | 100<br>LQFP | 64<br>BGA | 64<br>LQFP | Pin Name                       | Default                             | ALT0                                | ALT1                           | ALT2      | ALT3                 | ALT4                 | ALT5      | ALT6             | ALT7    |
|------------|-------------|-----------|------------|--------------------------------|-------------------------------------|-------------------------------------|--------------------------------|-----------|----------------------|----------------------|-----------|------------------|---------|
| D9         | 64          | D6        | 41         | PTB18                          | LCD_P14/<br>TSIO_CH11               | LCD_P14/<br>TSIO_CH11               | PTB18                          |           | TPM2_CH0             | I2S0_TX_<br>BCLK     |           |                  | LCD_P14 |
| C9         | 65          | C7        | 42         | PTB19                          | LCD_P15/<br>TSIO_CH12               | LCD_P15/<br>TSIO_CH12               | PTB19                          |           | TPM2_CH1             | I2S0_TX_FS           |           |                  | LCD_P15 |
| F10        | 66          | —         | —          | PTB20                          | LCD_P16                             | LCD_P16                             | PTB20                          |           |                      |                      |           | CMP0_OUT         | LCD_P16 |
| F9         | 67          | —         | —          | PTB21                          | LCD_P17                             | LCD_P17                             | PTB21                          |           |                      |                      |           |                  | LCD_P17 |
| F8         | 68          | —         | —          | PTB22                          | LCD_P18                             | LCD_P18                             | PTB22                          |           |                      |                      |           |                  | LCD_P18 |
| E8         | 69          | —         | —          | PTB23                          | LCD_P19                             | LCD_P19                             | PTB23                          |           |                      |                      |           |                  | LCD_P19 |
| B9         | 70          | D8        | 43         | PTC0                           | LCD_P20/<br>ADC0_SE14/<br>TSIO_CH13 | LCD_P20/<br>ADC0_SE14/<br>TSIO_CH13 | PTC0                           |           | EXTRG_IN             | audioUSB_<br>SOF_OUT | CMP0_OUT  | I2S0_TXD0        | LCD_P20 |
| D8         | 71          | C6        | 44         | PTC1/<br>LLWU_P6/<br>RTC_CLKIN | LCD_P21/<br>ADC0_SE15/<br>TSIO_CH14 | LCD_P21/<br>ADC0_SE15/<br>TSIO_CH14 | PTC1/<br>LLWU_P6/<br>RTC_CLKIN | I2C1_SCL  |                      | TPM0_CH0             |           | I2S0_TXD0        | LCD_P21 |
| C8         | 72          | B7        | 45         | PTC2                           | LCD_P22/<br>ADC0_SE11/<br>TSIO_CH15 | LCD_P22/<br>ADC0_SE11/<br>TSIO_CH15 | PTC2                           | I2C1_SDA  |                      | TPM0_CH1             |           | I2S0_TX_FS       | LCD_P22 |
| B8         | 73          | C8        | 46         | PTC3/<br>LLWU_P7               | LCD_P23                             | LCD_P23                             | PTC3/<br>LLWU_P7               |           | UART1_RX             | TPM0_CH2             | CLKOUT    | I2S0_TX_<br>BCLK | LCD_P23 |
| F7         | 74          | E3        | 47         | VSS                            | VSS                                 | VSS                                 |                                |           |                      |                      |           |                  |         |
| E7         | —           | E4        | —          | VDD                            | VDD                                 | VDD                                 |                                |           |                      |                      |           |                  |         |
| A11        | 75          | C5        | 48         | VLL3                           | VLL3                                | VLL3                                |                                |           |                      |                      |           |                  |         |
| A10        | 76          | A6        | 49         | VLL2                           | VLL2                                | VLL2/<br>LCD_P4                     | PTC20                          |           |                      |                      |           |                  | LCD_P4  |
| A9         | 77          | B5        | 50         | VLL1                           | VLL1                                | VLL1/<br>LCD_P5                     | PTC21                          |           |                      |                      |           |                  | LCD_P5  |
| B11        | 78          | B4        | 51         | VCAP2                          | VCAP2                               | VCAP2/<br>LCD_P6                    | PTC22                          |           |                      |                      |           |                  | LCD_P6  |
| C11        | 79          | A5        | 52         | VCAP1                          | VCAP1                               | VCAP1/<br>LCD_P39                   | PTC23                          |           |                      |                      |           |                  | LCD_P39 |
| A8         | 80          | B8        | 53         | PTC4/<br>LLWU_P8               | LCD_P24                             | LCD_P24                             | PTC4/<br>LLWU_P8               | SPI0_PCS0 | UART1_TX             | TPM0_CH3             | I2S0_MCLK |                  | LCD_P24 |
| D7         | 81          | A8        | 54         | PTC5/<br>LLWU_P9               | LCD_P25                             | LCD_P25                             | PTC5/<br>LLWU_P9               | SPI0_SCK  | LPTMR0_<br>ALT2      | I2S0_RXD0            |           | CMP0_OUT         | LCD_P25 |
| C7         | 82          | A7        | 55         | PTC6/<br>LLWU_P10              | LCD_P26/<br>CMP0_IN0                | LCD_P26/<br>CMP0_IN0                | PTC6/<br>LLWU_P10              | SPI0_MOSI | EXTRG_IN             | I2S0_RX_<br>BCLK     | SPI0_MISO | I2S0_MCLK        | LCD_P26 |
| B7         | 83          | B6        | 56         | PTC7                           | LCD_P27/<br>CMP0_IN1                | LCD_P27/<br>CMP0_IN1                | PTC7                           | SPI0_MISO | audioUSB_<br>SOF_OUT | I2S0_RX_FS           | SPI0_MOSI |                  | LCD_P27 |
| A7         | 84          | —         | —          | PTC8                           | LCD_P28/<br>CMP0_IN2                | LCD_P28/<br>CMP0_IN2                | PTC8                           | I2C0_SCL  | TPM0_CH4             | I2S0_MCLK            |           |                  | LCD_P28 |
| D6         | 85          | —         | —          | PTC9                           | LCD_P29/<br>CMP0_IN3                | LCD_P29/<br>CMP0_IN3                | PTC9                           | I2C0_SDA  | TPM0_CH5             | I2S0_RX_<br>BCLK     |           |                  | LCD_P29 |
| C6         | 86          | —         | —          | PTC10                          | LCD_P30                             | LCD_P30                             | PTC10                          | I2C1_SCL  |                      | I2S0_RX_FS           |           |                  | LCD_P30 |
| C5         | 87          | —         | —          | PTC11                          | LCD_P31                             | LCD_P31                             | PTC11                          | I2C1_SDA  |                      | I2S0_RXD0            |           |                  | LCD_P31 |
| B6         | 88          | —         | —          | PTC12                          | LCD_P32                             | LCD_P32                             | PTC12                          |           |                      | TPM_CLKIN0           |           |                  | LCD_P32 |
| A6         | 89          | —         | —          | PTC13                          | LCD_P33                             | LCD_P33                             | PTC13                          |           |                      | TPM_CLKIN1           |           |                  | LCD_P33 |
| D5         | 90          | —         | —          | PTC16                          | LCD_P36                             | LCD_P36                             | PTC16                          |           |                      |                      |           |                  | LCD_P36 |

## Pinout

| 121<br>BGA | 100<br>LQFP | 64<br>BGA | 64<br>LQFP | Pin Name          | Default               | ALT0                  | ALT1              | ALT2      | ALT3     | ALT4     | ALT5      | ALT6 | ALT7    |
|------------|-------------|-----------|------------|-------------------|-----------------------|-----------------------|-------------------|-----------|----------|----------|-----------|------|---------|
| C4         | 91          | —         | —          | PTC17             | LCD_P37               | LCD_P37               | PTC17             |           |          |          |           |      | LCD_P37 |
| B4         | 92          | —         | —          | PTC18             | LCD_P38               | LCD_P38               | PTC18             |           |          |          |           |      | LCD_P38 |
| D4         | 93          | C3        | 57         | PTD0              | LCD_P40               | LCD_P40               | PTD0              | SPI0_PCS0 |          | TPM0_CH0 |           |      | LCD_P40 |
| D3         | 94          | A4        | 58         | PTD1              | LCD_P41/<br>ADC0_SE5b | LCD_P41/<br>ADC0_SE5b | PTD1              | SPI0_SCK  |          | TPM0_CH1 |           |      | LCD_P41 |
| C3         | 95          | C2        | 59         | PTD2              | LCD_P42               | LCD_P42               | PTD2              | SPI0_MOSI | UART2_RX | TPM0_CH2 | SPI0_MISO |      | LCD_P42 |
| B3         | 96          | B3        | 60         | PTD3              | LCD_P43               | LCD_P43               | PTD3              | SPI0_MISO | UART2_TX | TPM0_CH3 | SPI0_MOSI |      | LCD_P43 |
| A3         | 97          | A3        | 61         | PTD4/<br>LLWU_P14 | LCD_P44               | LCD_P44               | PTD4/<br>LLWU_P14 | SPI1_PCS0 | UART2_RX | TPM0_CH4 |           |      | LCD_P44 |
| A2         | 98          | C1        | 62         | PTD5              | LCD_P45/<br>ADC0_SE6b | LCD_P45/<br>ADC0_SE6b | PTD5              | SPI1_SCK  | UART2_TX | TPM0_CH5 |           |      | LCD_P45 |
| B2         | 99          | B2        | 63         | PTD6/<br>LLWU_P15 | LCD_P46/<br>ADC0_SE7b | LCD_P46/<br>ADC0_SE7b | PTD6/<br>LLWU_P15 | SPI1_MOSI | UART0_RX |          | SPI1_MISO |      | LCD_P46 |
| A1         | 100         | A2        | 64         | PTD7              | LCD_P47               | LCD_P47               | PTD7              | SPI1_MISO | UART0_TX |          | SPI1_MOSI |      | LCD_P47 |
| F1         | 10          | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| F2         | 11          | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| G1         | 12          | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| G2         | 13          | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| J3         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| H3         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| K4         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| L7         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| J9         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| J4         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| H11        | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| F11        | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| A5         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| B5         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| A4         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| B1         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| C2         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| C1         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| D2         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| D1         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |
| E1         | —           | —         | —          | NC                | NC                    | NC                    |                   |           |          |          |           |      |         |

## 8.2 KL36 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL36 Signal Multiplexing and Pin Assignments](#).

|   | 1     | 2                 | 3                 | 4     | 5     | 6     | 7                 | 8                              | 9     | 10    | 11               |   |
|---|-------|-------------------|-------------------|-------|-------|-------|-------------------|--------------------------------|-------|-------|------------------|---|
| A | PTD7  | PTD5              | PTD4/<br>LLWU_P14 | NC    | NC    | PTC13 | PTC8              | PTC4/<br>LLWU_P8               | VLL1  | VLL2  | VLL3             | A |
| B | NC    | PTD6/<br>LLWU_P15 | PTD3              | PTC18 | NC    | PTC12 | PTC7              | PTC3/<br>LLWU_P7               | PTC0  | PTB16 | VCAP2            | B |
| C | NC    | NC                | PTD2              | PTC17 | PTC11 | PTC10 | PTC6/<br>LLWU_P10 | PTC2                           | PTB19 | PTB11 | VCAP1            | C |
| D | NC    | NC                | PTD1              | PTD0  | PTC16 | PTC9  | PTC5/<br>LLWU_P9  | PTC1/<br>LLWU_P6/<br>RTC_CLKIN | PTB18 | PTB10 | PTB8             | D |
| E | NC    | PTE2              | PTE1              | PTE0  | VDD   | VDD   | VDD               | PTB23                          | PTB17 | PTB9  | PTB7             | E |
| F | NC    | NC                | PTE6              | PTE3  | VDDA  | VSSA  | VSS               | PTB22                          | PTB21 | PTB20 | NC               | F |
| G | NC    | NC                | VSS               | PTE5  | VREFH | VREFL | VSS               | PTB3                           | PTB2  | PTB1  | PTB0/<br>LLWU_P5 | G |
| H | PTE16 | PTE17             | NC                | PTA7  | PTE24 | PTE26 | PTE4              | PTA1                           | PTA3  | PTA17 | NC               | H |
| J | PTE18 | PTE19             | NC                | NC    | PTE25 | PTA0  | PTA2              | PTA4                           | NC    | PTA16 | PTA20            | J |
| K | PTE20 | PTE21             | PTA6              | NC    | PTE30 | VDD   | PTA5              | PTA12                          | PTA14 | VSS   | PTA19            | K |
| L | PTE22 | PTE23             | PTE29             | PTE31 | VSS   | VSS   | NC                | PTA13                          | PTA15 | VDD   | PTA18            | L |
|   | 1     | 2                 | 3                 | 4     | 5     | 6     | 7                 | 8                              | 9     | 10    | 11               |   |

**Figure 21. KL36 121-pin BGA pinout diagram**

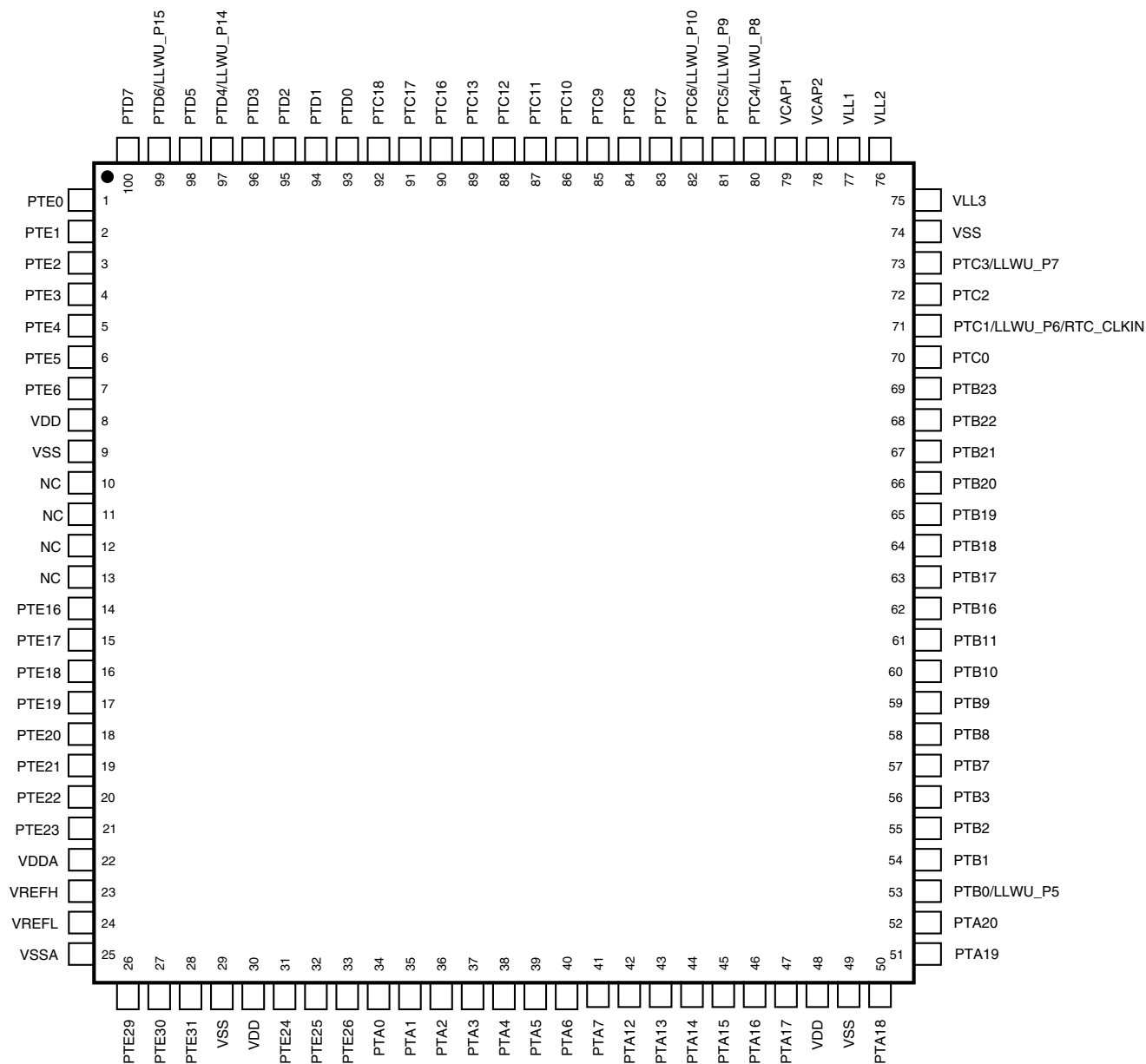


Figure 22. KL36 100-pin LQFP pinout diagram



|   | 1     | 2                 | 3                 | 4     | 5     | 6                              | 7                 | 8                |   |
|---|-------|-------------------|-------------------|-------|-------|--------------------------------|-------------------|------------------|---|
| A | PTE0  | PTD7              | PTD4/<br>LLWU_P14 | PTD1  | VCAP1 | VLL2                           | PTC6/<br>LLWU_P10 | PTC5/<br>LLWU_P9 | A |
| B | PTE1  | PTD6/<br>LLWU_P15 | PTD3              | VCAP2 | VLL1  | PTC7                           | PTC2              | PTC4/<br>LLWU_P8 | B |
| C | PTD5  | PTD2              | PTD0              | VSS   | VLL3  | PTC1/<br>LLWU_P6/<br>RTC_CLKIN | PTB19             | PTC3/<br>LLWU_P7 | C |
| D | PTE17 | PTE19             | PTA0              | PTA1  | PTA3  | PTB18                          | PTB17             | PTC0             | D |
| E | PTE16 | PTE18             | VSS               | VDD   | PTA2  | PTB16                          | PTB2              | PTB3             | E |
| F | PTE21 | PTE23             | VSSA              | VDDA  | PTA5  | PTB1                           | PTB0/<br>LLWU_P5  | PTA20            | F |
| G | PTE20 | PTE22             | VREFL             | VREFH | PTA4  | PTA13                          | VDD               | PTA19            | G |
| H | PTE29 | PTE30             | PTE31             | PTE24 | PTE25 | PTA12                          | VSS               | PTA18            | H |
|   | 1     | 2                 | 3                 | 4     | 5     | 6                              | 7                 | 8                |   |

**Figure 23. KL36 64-pin BGA pinout diagram**

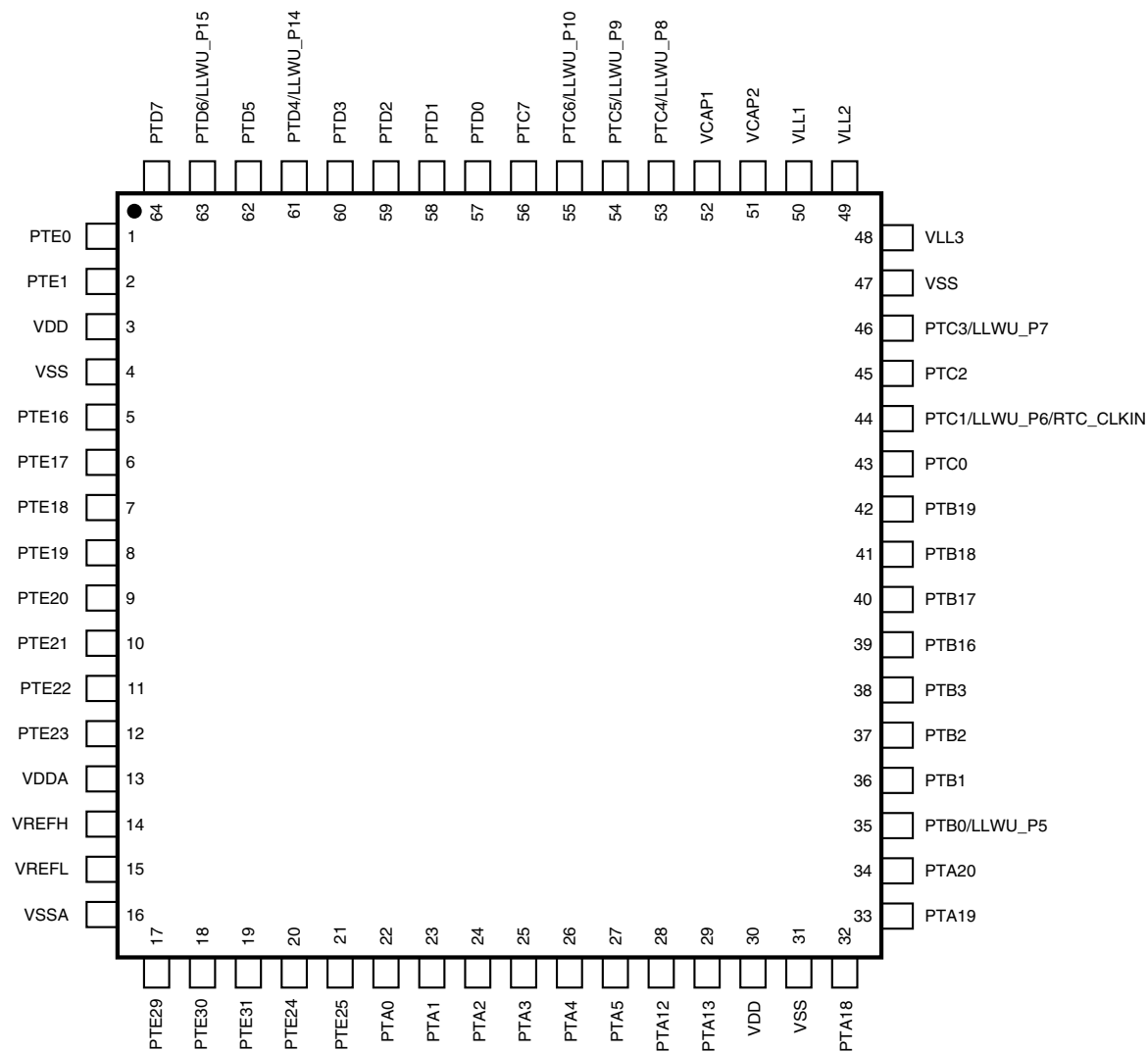


Figure 24. KL36 64-pin LQFP pinout diagram

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