OVERVIEW

This application note describes how to install and to use the µVision2 target debugger with an OCDS/JTAG interface. The PC printer port is used to connect to the JTAG interface on the target system.

With the OCDS interface you can download your application into the RAM of your target system. Starting the application or performing single steps is possible when the application is located in RAM or in ROM. When it is located in ROM, a monitor program must be linked to the application, which enables the debugger to access the instruction pointer.

SUPPORTED DEVICES

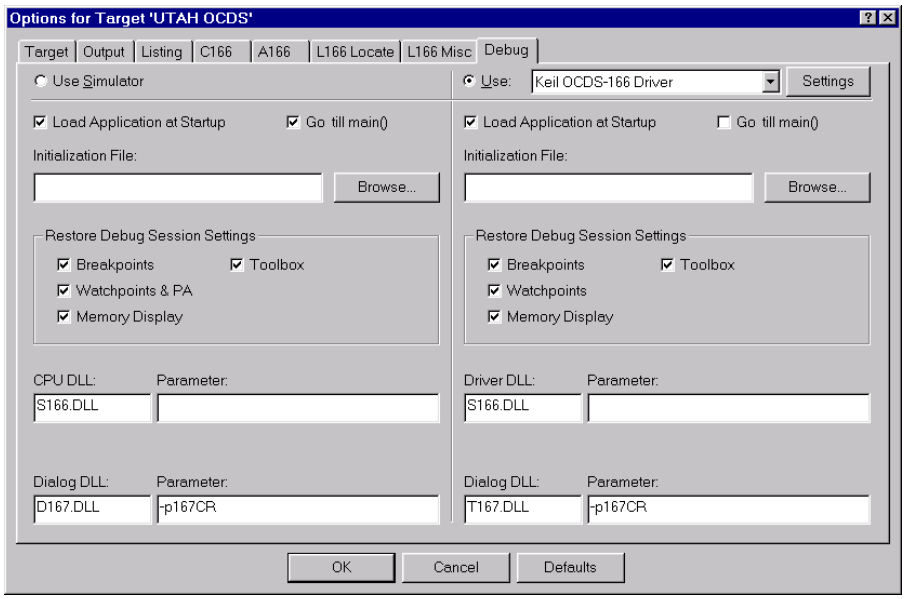
This driver has been tested with an Infineon 165UTAH/161U EASY UTAH board. Other CPU's such as XC161 or XC164 have a slightly different OCDS interface and are currently not supported by this driver. However, these and other derivatives of the 166 microcontroller family with OCDS interface will be supported very soon. Therefore, please check for newer versions of this application note on www.keil.com.

INSTALLATION

The OCDS interface requires the installation of an OCDS/JTAG printer port driver. This driver is part of this Application Note (please unzip the support files in APNT_146.ZIP) and installed with SETUP.EXE that is provided in the folder **OCDSPrinterPortDriver**. Please start this setup program and follow the instructions on the screen.

CONFIGURATION OF THE UVISION2 DEBUGGER

The Keil OCDS-166 driver is selected in the µVision2 dialog **Project – Options for Target – Debug** as shown below. Since the µVision2 debugger allows you debugging with different drivers, this driver needs to be selected for each µVision2 project target.



NOTE

If this driver is not available or cannot be selected you need to update the Keil C166 Compiler package or you need to add one line in the TOOLS.INI file.

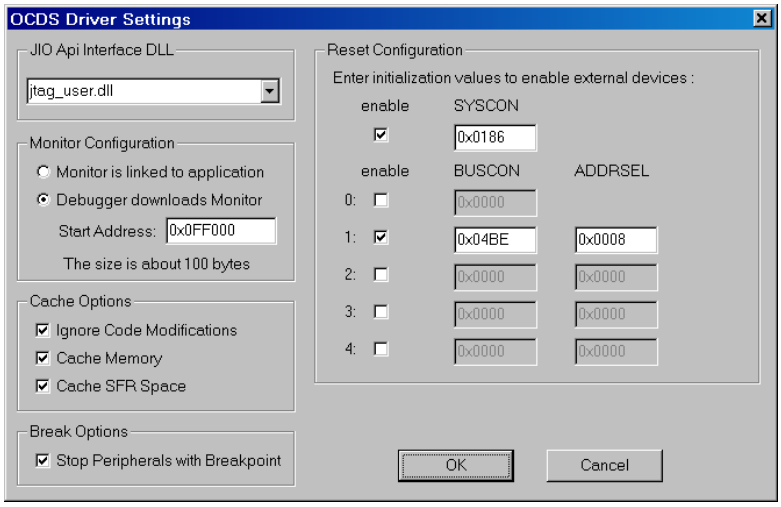
[C166]

...

TDRV1=OCDS\CBC166.DLL ("Keil OCDS-166 Driver")

In any case, you must have at least C166 Version 4.15 or higher.

You need to configure the driver. Click **Settings** to open dialog Keil OCDS-166 Driver Settings. For debugging with the C165UTAH board you need to enter the following parameters.


OCDS Driver Settings
JIO Api Interface DLL
jtag_user.dll
Monitor Configuration
Monitor is linked to application
Debugger downloads Monitor
Start Address: 0x0FF000
The size is about 100 bytes
Cache Options
Ignore Code Modifications
Cache Memory
Cache SFR Space
Break Options
Stop Peripherals with Breakpoint
Reset Configuration
Enter initialization values to enable external devices :
enable
SYSCON
0x0186
enable
BUSCON
ADDRSEL
0:
0x0000
1:
0x04BE
0x0008
2:
0x0000
0x0000
3:
0x0000
0x0000
4:
0x0000
0x0000
OK
Cancel

Parameter Description of the OCDS-166 Driver Settings Dialog

JIO API Interface DLL: Currently only the one **jtag_user.dll** is available. This DLL uses the PC printer port as OCDS/JTAG interface. Future versions may support different wigglers.

Monitor Configuration: The OCDS interface on the C165 UTAH requires a small Monitor program that supports read/write of the instruction pointer. This Monitor requires only about 100 bytes code and uses the TRAP interrupt vector 8 (address 20H). There are two methods to provide this Monitor:

- **Monitor is linked to application:** You have linked the monitor to your application; in this case the application can be downloaded into RAM or can be programmed into (Flash) ROM. (Note: The Monitor program that needs to be linked will be available in a future version of this Application Note).

- **Debugger downloads Monitor:** Your application does not contain the monitor. This is the recommended methode when the application is downloaded into RAM. You need also to specify the start address of the monitor. The start address 0 is not allowed. We recommend to use the end of the RAM area as start address for the monitor to avoid conflicts with your application. You need also to reserve the TRAP interrupt vector location 8 (address range 20H – 23H) with the L166 RESERVE directive. This address range should be entered under **Options for Target – Debug – L166 Misc – Reserve.**

Cache Options: These controls improve the performance of the µVision2 debugger. The default setting is configured for maximum performance. The sub-options are described below:

Ignore Code Modifications: µVision2 assumes that downloaded program code does not change during program execution. Disable this option for self modifying code.

Cache Memory: µVision2 assumes that the memory content does not change when the user program halts. Disable this option to see memory changes from memory mapped peripherals when you do not single step or execute the user program code.

Cache SFR Space: µVision2 assumes that the memory content in the SFR area 0xF000 – 0xF1FF and 0xFE00 – 0xFFFF does not change when the user program halts. Disable this option to see memory changes from peripherals that are mapped into the SFR space when you do not single step or execute the user program code. This option is similar to **Cache Memory**.

Break Options: Stop Peripherals with Breakpoint selects that all on-chip peripherals (e.g. timers) are disconnected from CPU clock when the user application is stopped manually or because of a breakpoint.

Reset Configuration: When you download an application (or the monitor) into RAM that is connected to a chip select line other than 0, the bus system (BUSCONx and ADDRSELx) needs to be initialized to enable the address window for the RAM device. Enter correct values for your target system.

KNOWN PROBLEMS

- Currently there is no way to stop the CPU after a reset without executing the first instruction at address 0. In most hardware designs, there is (Flash) ROM connected to chip select 0 (CS0) and RAM to CS1. Therefore, the first instruction in the ROM must be a valid instruction which must not cause any traps or system lock up. The Easy UTAH board is shipped with a preprogrammed flash device and even erased EPROM or flash devices do not cause a problem. Problems may arise when no device is active on the bus at address 0 or when the device contains random data.

- When you download and start your application in external RAM which is not connected to chip-select 0 and you press the reset button on the target system, the system crashes. This is because only chip-select 0 is active after a reset and the RAM cannot be accessed in this case. This does not apply if you press the reset button within the µVision2 debugger.

- When starting the target debugger, the OCDS initialization time of the EASY UTAH board is very long (about 5 seconds) because the JTAG reset signal is delayed with a MAX 707 reset circuit.

PROGRAM EXAMPLE

You can find an example application for a C165 EASY UTAH board in the folder:
Keil\C166\Examples\Boards\Infineon EASY UTAH\UTAH_Blinky.Uv2

CONCLUSION

Using the OCDS interface with the Keil µVision2 debugger is simple and powerful. Compared to the Keil Monitor-166 the OCDS debugger provides the following benefits:

- High upload and download speed
- The 166 Serial Interface is fully available to the user application
- Access Breakpoints can trigger on read or write accesses in user code without scarifying execution speed of the user program.
- The RESET command in the µVision2 debugger generates a real CPU reset that fully resets all peripherals.
- During execution of the user application the memory of the target system can be read or modified.

In the USA:
Keil Software, Inc.
1501 10th Street, Suite 110
Plano, TC 75074
USA

Sales: 800-348-8051
Phone: 972-312-1107
FAX: 972-312-1159

E-mail: sales.us@keil.com
support.us@keil.com

Internet: http://www.keil.com/

In Europe:
Keil Elektronik GmbH
Bretonischer Ring 15
D-85630 Grasbrunn b. Munchen
Germany

Phone: (49) (089) 45 60 40 - 0
FAX: (49) (089) 46 81 62

E-mail: sales.intl@keil.com
support.intl@keil.com