



Product List

SM5964C25, 25 MHz 64KB internal flash MCU
SM5964C40, 40 MHz 64KB internal flash MCU

Description

The SM5964 series product is an 8 - bit single chip micro controller with 64KB flash & 1K byte RAM embedded. It has In-System Programming (ISP) function and is a derivative of the 8052 micro controller family. It has 5-channel SPWM build-in. User can access on-chip expanded RAM with easier and faster way by its 'bank mapping direct addressing mode' scheme. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 64K byte flash memory either for program or for data or mixed.

To program the on-chip flash memory, a commercial writer is available to do it in parallel programming method. The on-chip flash memory can be programmed in either parallel or serial interface with its ISP feature.

Ordering Information

yywww
SM5964ihhk

yy: year, ww:week
v: version identifier { , A, B, ...}
i: process identifier
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}

Postfix	Package	Pin/Pad Configuration	Dimension
P	40L PDIP	page 2	page 24
J	44L PLCC	page 2	page 25
Q	44L QFP	page 2	page 26

Features

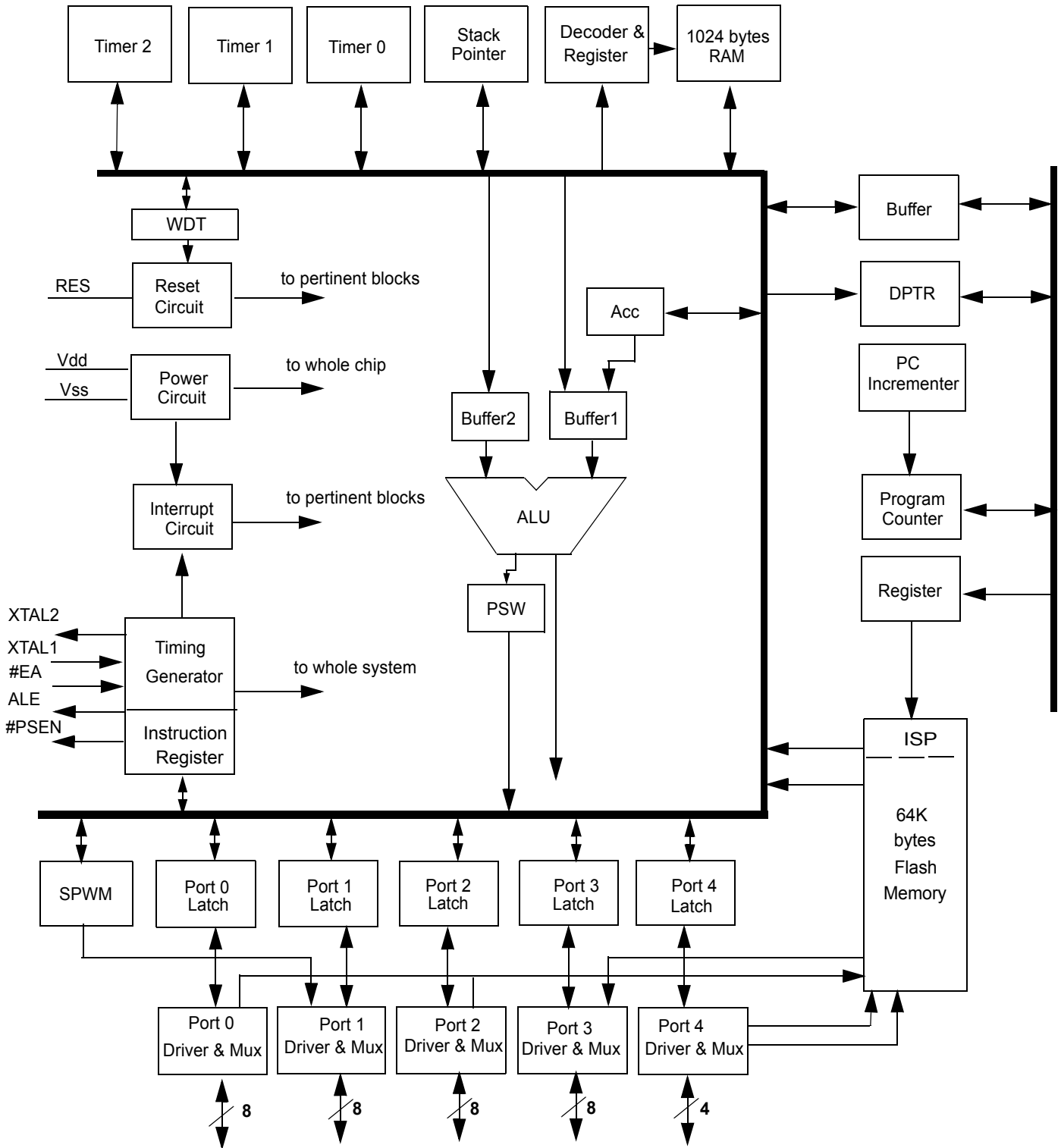
- Working voltage: 4.5V through 5.5V
- General 8052 family compatible
- 12 clocks per machine cycle
- 64K byte on chip flash memory with In-System Programming (ISP) capability
- 1024 byte on chip data RAM
- Three 16 bit Timers/Counters
- One Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Industrial Level
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
 - Idle mode and Power down mode
 - Code protection function
 - Low EMI (inhibit ALE)
 - Reset with address \$0000 blank initiate ISP service program
 - ISP service program space configurable in N*512byte (N=0 to 8) size
 - Bank mapping direct addressing mode for access on-chip RAM
- Five channel Specific PWM (SPWM) build-in with P1.3 ~ P1.7

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Block Diagram



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July 2002

Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0/T2		i/o	bit 0 of port 1 & timer 2 clock out
2	41	3	P1.1/T2EX		i/o	bit 1 of port 1 & timer 2 control
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3/SPWM0		i/o	bit 3 of port 1 & SPWM Channel 0
5	44	6	P1.4/SPWM1		i/o	bit 4 of port 1 & SPWM Channel 1
6	1	7	P1.5/SPWM2		i/o	bit 5 of port 1 & SPWM Channel 2
7	2	8	P1.6/SPWM3		i/o	bit 6 of port 1 & SPWM Channel 3,
8	3	9	P1.7/SPWM4		i/o	bit 7 of port 1 & SPWM Channel 4
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receive data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	8	14	P3.2/#INT0	L/ -	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	L/ -	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
15	11	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	12	18	P3.6/#WR	L/ -	i/o	bit 6 of port 3 & ext. memory write
17	13	19	P3.7/#RD	L/ -	i/o	bit 7 of port 3 & ext. memory read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of external memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of external memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of external memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of external memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of external memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of external memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of external memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of external memory address
29	26	32	#PSEN	L	o	program storage enable
30	27	33	ALE	-	o	address latch enable
31	29	35	#EA	L	i	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of external memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of external memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of external memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of external memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of external memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of external memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of external memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of external memory
40	38	44	VDD			Drive Voltage
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of Port 4

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Special Function Register (SFR)

The address \$80 to \$FF can be accessed by direct addressing mode only.

Address \$80 to \$FF is SFR area.

The following table list the SFRs which are identical to general 8052 as well as SM5964 Extension SFRs.

\$F8										\$FF
\$F0	B				ISPAH	ISPAL	ISPAD	ISPC		\$F7
\$E8										\$EF
\$E0	ACC									\$E7
\$D8	P4									\$DF
\$D0	PSW									\$D7
\$C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2				\$CF
\$C0										\$C7
\$B8	IP								SCONF	\$BF
\$B0	P3									\$B7
\$A8	IE				SPWMD4					\$AF
\$A0	P2			SPWMC	SPWMD0	SPWMD1	SPWMD2	SPWMD3		\$A7
\$98	SCON	SBUF		P1CON					WDTC	\$9F
\$90	P1									\$97
\$88	TCON	TMOD	TL0	TL1	TH0	TH1				\$8F
\$80	P0	SP	DPL	DPH		RCON	DBANK	PCON		\$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM5964

Addr	SFR	Reset	7	6	5	4	3	2	1	0
85H	RCON	*****00							RAMS1	RAMS0
86H	DBANK	0***0001	BSE				BS3	BS2	BS1	BS0
9BH	P1CON	0000***	SPWM4E	SPWM3E	SPWM2E	SPWM1E	SPWM0E			
9FH	WDTC	0*0**000	WDTE	Reserve	CLEAR			PS2	PS1	PS0
A3H	SPWMC	*****00							FPDIV1	FPDIV0
A4H	SPWMD0	00H	SPWMD0.4	SPWMD0.3	SPWMD0.2	SPWMD0.1	SPWMD0.0	BRM0.2	BRM0.1	BRM0.0
A5H	SPWMD1	00H	SPWMD1.4	SPWMD1.3	SPWMD1.2	SPWMD1.1	SPWMD1.0	BRM1.2	BRM1.1	BRM1.0
A6H	SPWMD2	00H	SPWMD2.4	SPWMD2.3	SPWMD2.2	SPWMD2.1	SPWMD2.0	BRM2.2	BRM2.1	BRM2.0
A7H	SPWMD3	00H	SPWMD3.4	SPWMD3.3	SPWMD3.2	SPWMD3.1	SPWMD3.0	BRM3.2	BRM3.1	BRM3.0
ACH	SPWMD4	00H	SPWMD4.4	SPWMD4.3	SPWMD4.2	SPWMD4.1	SPWMD4.0	BRM4.2	BRM4.1	BRM4.0
BFH	SCONF	0****010	WDR					ISPE	OME	ALEI
C9H	T2MOD	*****00	*	*	*	*	*	*	T2OE	DCEN
D8H	P4	****1111					P4.3	P4.2	P4.1	P4.0

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Addr	SFR	Reset	7	6	5	4	3	2	1	0
F4H	ISPF AH	00H	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
F5H	ISPF AL	00H	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
F6H	ISPF D	00H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F7H	ISPC	0*****00	START						F1	F0

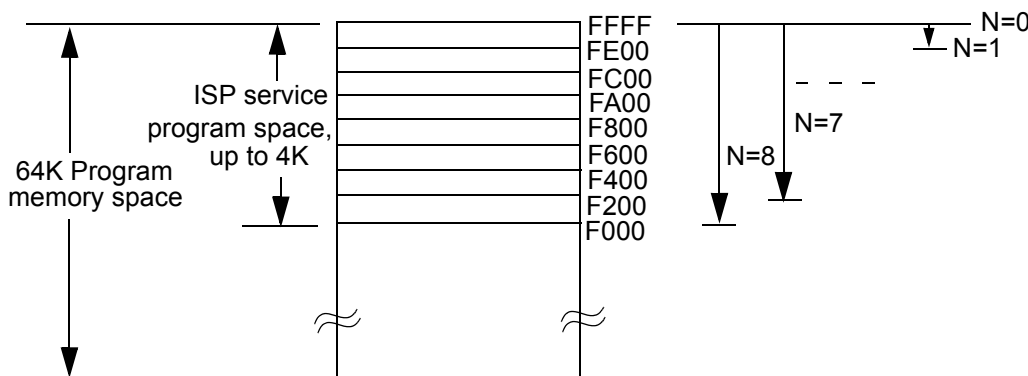
Extension Function Description

1. Memory Structure

The SM5964 is the general 8052 hardware core to integrate the ISP function module as a single chip micro controller. Its memory structure follows general 8052 structure.

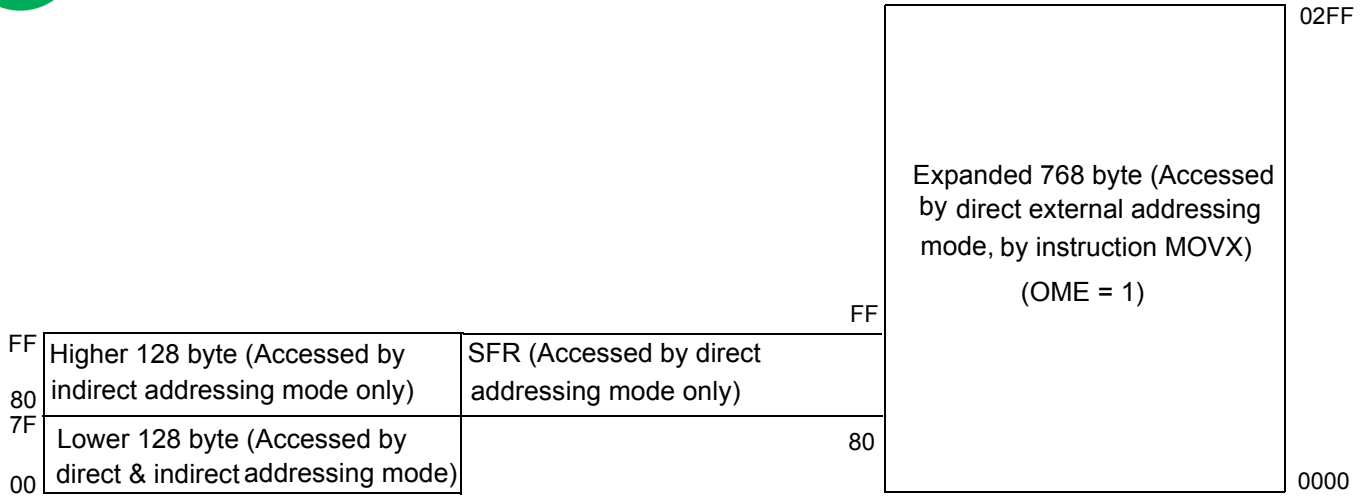
1.1 Program Memory

The SM5964 has 64K byte on-chip flash memory which used as general program memory, on which include up to 4K byte specific ISP service program memory space. The address range for the 64K byte is \$0000 to \$FFFF. The address range for the ISP service program is \$F000 to \$FFFF. The ISP service program size can be partitioned as N blocks of 512 byte (N=0 to 8). When N=0 means no ISP service program space available, total 64K byte memory used as program memory. When N=1 means memory address \$FE00 to \$FFFF reserved for ISP service program. When N=2 means memory address \$FC00 to \$FFFF reserved for ISP service program,...etc. Value N can be set and programmed into SM5964 by writer.



1.2 Data Memory

The SM5964 has 1K bytes on-chip RAM, 256 bytes of it are the same as general 8052 internal memory structure while the expanded 768 bytes on-chip RAM can be accessed by external memory addressing method (by instruction MOVX.) or by bank mapping direct addressing mode.



1.2.1 Data Memory - Lower 128 byte (\$00 to \$7F, Bank 0 & Bank 1)

Data Memory \$00 to \$FF is the same as 8052.
 The address \$00 to \$7F can be accessed by direct and indirect addressing modes.
 Address \$00 to \$1F is register area.
 Address \$20 to \$2F is memory bit area.
 Address \$30 to \$7F is for general memory area.

1.2.2 Data Memory - Higher 128 byte (\$80 to \$FF, Bank 2 & Bank 3)

The address \$80 to \$FF can be accessed by indirect addressing mode or by bank mapping direct addressing mode.
 Address \$80 to \$FF is data area.

1.2.3 Data Memory - Expanded 768 bytes (\$0000 to \$02FF, Bank 4 ~ Bank 15)

From external address \$0000 to \$02FF is the on-chip expanded RAM area, total 768 bytes. This area can be accessed by external direct addressing mode (by instruction MOVX) or by bank mapping direct addressing mode.

If the address of instruction MOVX @DPTR is larger than \$02FF then SM5964 will generate the external memory control signal automatically. The bit 1 (OME) of special function register \$BF (SCONF) can enable or disable this expanded 768 byte RAM. The default setting of OME bit is 1 (enable).

The address space of instruction MOVX @Ri, i=0,1 is determined by bit 1 & bit 0 (RAMS1, RAMS0) of special function register \$85 (RCON). The default setting of RAMS1, RAMS0 bits is 00 (page0).

One page of data RAM is 256 byte.

RAMS1, RAMS0=00, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$0000 to \$00FF (page 0)
 RAMS1, RAMS0=01, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$0100 to \$01FF (page 1)
 RAMS1, RAMS0=10, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$0200 to \$02FF (page 2)
 RAMS1, RAMS0=11, Rn of instruction MOVX @Ri, i=0,1 mapping to expanded RAM address \$XY00 to \$XYFF which high byte address specified by port 2. (SM5964 will generate the external memory control signal automatically).

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1.3 Bank mapping direct addressing mode:

We provide RAM bank address '40H~7FH' as mapping window which allow user access all the 1K on-chip RAM through this RAM bank address.

Table with 6 columns: BS3, BS2, BS1, BS0, 040h~07fh mapping address, Note. It lists 16 different bank mappings and their corresponding RAM addresses.

With this bank mapping scheme, user can access entire 1k byte on-chip RAM with direct addressing method. That means using the window area (\$040~\$07F), user can access any bank (64 byte) data of 1k byte on-chip RAM space which is selected by BS[0:3] of data bank control register (DBANK, \$86).

For example, user write #30h to \$101 address:

```
MOV DBANK, #88H ; set bank mapping $040~$07f to $0100~$013f
MOV A, #30H ; store #30H to A
MOV 41H, A ; write #30H to $0101 address
```

Data Bank Control Register (DBANK, \$86)

Table showing bit-7 to bit-0 for DBANK register. Columns include BSE, Unused, BS3, BS2, BS1, BS0. Rows show Read / Write and Reset value.

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Data bank select enable bit BSE = 1 enables the data bank select function

Data bank select enable bit BSE = 0 disables the data bank select function

BS[3:0] setting will map \$040~\$07F RAM space to entire 1k byte on-chip RAM space.

Internal RAM Control Register (RCON, \$85)

	bit-7						bit-0	
	Unused	Unused	Unused	Unused	Unused	Unused	RAMS1	RAMS0
Read / Write:	-	-	-	-	-	-	R/W	R/W
Reset value:	*	*	*	*	*	*	0	0

SM5964 has 768 byte on-chip RAM which can be accessed by external memory addressing method only. (By instruction MOVX). The address space of instruction MOVX @Rn is determined by bit 1 and bit 0 (RAMS1, RAMS0) of RCON. The default setting of RAMS1, RAMS0 bits is 00 (page0).

System Control Register (SCONF, \$BF)

	bit-7					bit-0		
	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	0	0

WDR: Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1

ISPE: ISP function enable bit

OME: 768 byte on-chip RAM enable bit

ALEI: ALE output inhibit bit, to reduce EMI

Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

The bit 1 (OME) of SCONF can enable or disable the on-chip expanded 768 byte RAM. The default setting of OME bit is 1 (enable).

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

2. Port 4 for PLCC or QFP package:

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.



Port4 (P4, \$D8)

	bit-7				bit-0			
	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Read / Write:	-	-	-	-	R/W	R/W	R/W	R/W
Reset value:	*	*	*	*	1	1	1	1

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

3. In-System Programming (ISP) Function

The SM5964 can generate flash control signal by internal hardware circuit. User utilize flash control register, flash address register and flash data register to perform the ISP function without removing the SM5964 from the system.

The SM5964 provides internal flash control signals which can do flash program/chip erase/page erase/protect functions. User need to design and use any kind of interface which SM5964 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

3.1 ISP Service Program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the SM5964 for the ISP purpose.

The ISP service program were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between SM5964 and host device which output data to the SM5964. For example, if user utilize UART interface to receive/transmit data between SM5964 and host device, the ISP service program should include baud rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under SM5964 active or idle mode. It can not be initiated under power down mode.

3.2. Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range \$F000 to \$FFFF. It can be divided as blocks of N*512 byte. (N=0 to 8). When N=0 means no ISP function, all of 64K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 512 byte while the rest of 63.5K byte flash memory can be used as program memory. The maximum ISP service program allowed is 4K byte when N=8. Under such configuration, the usable program memory space is 60K byte.

After N determined, SM5964 will reserve the ISP service program space downward from the top of the program address \$FFFF. The start address of the ISP service program located at \$Fx00 while x is an even number, depending on the lock bit N. Please see page 5 program memory diagram for this ISP service program space structure.

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The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash not been protected, the content of ISP service program still can be read. If the flash been protected, the overall content of flash program memory space including ISP service program space can not be read.

3.3 Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user need to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when SM5964 was in system.

3.4 Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are two ways to do so:

- (1) Blank reset. Hardware reset with first flash address blank (\$0000=#FFH) will load the PC with start address of ISP service program.
- (2) Execute jump instruction can load the start address of the ISP service program to PC.

User can initiate general 8052 INT function to initiate the ISP service program. After ISP service program executed, user need to reset the SM5964, either by hardware reset or by WDT, or jump to the address \$0000 to re-start the firmware program.

ISP Registers - ISPF AH, ISPF AL, ISPF D and ISPF C

ISP Flash Address-High Register (ISPF AH, \$F4)

	bit-7				bit-0			
	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA15 ~ FA8: flash address-high for ISP function

ISP Flash Address-Low Register (ISPF AL, \$F5)

	bit-7				bit-0			
	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FA7 ~ FA0: flash address-low for ISP function

The ISPF AH & ISPF AL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPF AH & ISPF AL registers

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overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

ISP Flash Data Register (ISPF, \$F6)

	bit-7						bit-0	
	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

FD7 ~ FD0: flash data for ISP function

The ISPF provide the 8-bit data for ISP function.

ISP Flash Control Register (ISPC, \$F7)

	bit-7						bit-0	
	START	Unused	Unused	Unused	Unused	Unused	ISPF1	ISPF0
Read / Write:	R/W	-	-	-	-	-	R/W	R/W
Reset value:	0	*	*	*	*	*	0	0

F[1: 0]: ISP function select bit

START: ISP function start bit

= 1: start ISP function which indicated by bit 1, bit 0 (F1, F0)

= 0: no operation

The START bit is read-only by default, software must write three specific values 55H, AAH and 55H sequentially to the ISPF register to enable the START bit write attribute. That is:

```
MOV ISPF, #55H
MOV ISPF, #AAH
MOV ISPF, #55H
```

Any attempt to set START bit will not be allowed without the procedure above.

After START bit set to 1 then the SM5964 hardware circuit will latch address and data bus and hold the program counter until the START bit reset to 0 when ISP function finished. User does not need to check START bit status by software method.

F[1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase
11	Chip erase

F[1:0]: ISP function select bit



One page of flash memory is 512 byte.

To perform byte program/page erase ISP function, user need to specify flash address at first. When performing page erase function, SM5964 will erase entire page which flash address indicated by ISPF AH & ISPF AL registers located within the page.

e.g. flash address: \$XYMN
page erase function will erase from \$XY00 to \$X(Y+1)FF (Y:even number), or
page erase function will erase from \$X(Y-1) 00 to \$XYFF (Y:odd number)

To perform the chip erase ISP function, SM5964 will erase all the flash program memory except the ISP service program space, also, SM5964 will un-protect the flash memory automatically. To perform chip protect ISP function, the SM5964 flash memory content will be read #00H.

```
e.g. ISP service program to do the byte program - to program #22H to the address $1005H
MOV SCONF,#04H ; enable SM5964 ISP function
MOV ISPF AH,#10H ; set flash address-high, 10H
MOV ISPF AL,#05H ; set flash address-low, 05H
MOV ISPF D,#22H ; set flash data to be programmed, data = 22H
MOV ISPC,#80H ; start to program #22H to the flash address $1005H
; after byte program finished, START bit of ISPC will be reset to 0 automatically
; program counter then point to the next instruction
```

ISP Registers - System Control Register (SCONF,\$BF)

Table with 8 columns (bit-7 to bit-0) and 3 rows (Read / Write, Reset value) for SCONF register bits: WDR, Unused, Unused, Unused, Unused, ISPE, OME, ALEI.

The bit 2 (ISPE) of SCONF is ISP enable bit. User can enable overall SM5964 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0.

The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally.

4. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway.

The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the selected time base source clock which set by PS2~PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM5964 been reset, either hardware reset or WDT reset.

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To reset the WDT is done by setting 1 to the CLEAR bit of WDTC. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

4.1 Watch Dog Timer Registers: WDTC and SCONF

Watch Dog Timer Register- WDT Control Register (WDTC, \$9F)

	bit-7					bit-0		
	WDTE	Reserve	CLEAR	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0

WDTE: Watch Dog Timer enable bit
CLEAR: Watch Dog Timer counter clear bit
PS[2:0]: clock source divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register (SCONF, \$BF)

	bit-7					bit-0		
	WDR	Unused	Unused	Unused	Unused	ISPE	OME	ALEI
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	*	*	*	0	0	0

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened



5. Reduce EMI Function

The SM5964 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

6. Specific Pulse Width Modulation (SPWM)

The Specific Pulse Width Modulation (SPWM) module has five 8-bit channels, each channel contains a 8-bit wide SPWM data register (SPWMD) to decide number of continuous pulses within a SPWM frame cycle.

6.1 SPWM Function Description:

Each 8-bit SPWM channel is composed of an 8-bit register which contains a 5-bit SPWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. The value programmed in the 5-bit SPWM portion will determine the pulse length of the output. The 3-bit BRM portion will generate and insert certain narrow pulses among an 8-SPWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. The usage of the BRM is to generate equivalent 8-bit resolution SPWM type DAC with reasonably high repetition rate through 5-bit SPWM clock speed. The PDIV[1:0] settings of SPWMC (\$A3) register are dividant of Fosc to be SPWM clock, Fosc/2^(PDIV[1:0]+1). The SPWM output cycle frame repetition rate (frequency) equals (SPWM clock)/32 which is [Fosc/2^(PDIV[1:0]+1)]/32.

6.2 SPWM Registers - P1CON, SPWMC, SPWMR[4:0]

SPWM Registers - Port1 Configuration Register (P1CON, \$9B)

								bit-0
	SPWM4E	SPWM3E	SPWM2E	SPWM1E	SPWM0E	Unused	Unused	Unused
Read / Write:	R/W	R/W	R/W	R/W	R/W	-	-	-
Reset value:	0	0	0	0	0	*	*	*

SPWM[4:0]E: When the bit set to one, the corresponding SPWM pin is active as SPWM function. When the bit reset to zero, the corresponding SPWM pin is active as I/O pin. Five bits are cleared upon reset.

SPWM Registers - SPWM Control Register (SPWMC, \$A3)

								bit-0
	Unused	Unused	Unused	Unused	Unused	Unused	PDIV1	PDIV0
Read / Write:	-	-	-	-	-	-	R/W	R/W
Reset value:	*	*	*	*	*	*	0	0

PDIV[1:0]: These two bits is 2's power parameter to form a frequency divider for input clock.



PDIV1	PDIV0	Divider	SPWM clock, Fosc=20MHz	SPWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

SPWM Data Register (SPWMD[4:0], \$AC, \$A4 ~\$A7)

	bit-7				bit-0			
	SPWMD [4:0]4	SPWMD [4:0]3	SPWMD [4:0]2	SPWMD [4:0]1	SPWMD [4:0]0	BRM [4:0]2	BRM [4:0]1	BRM [4:0]0
Read / Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

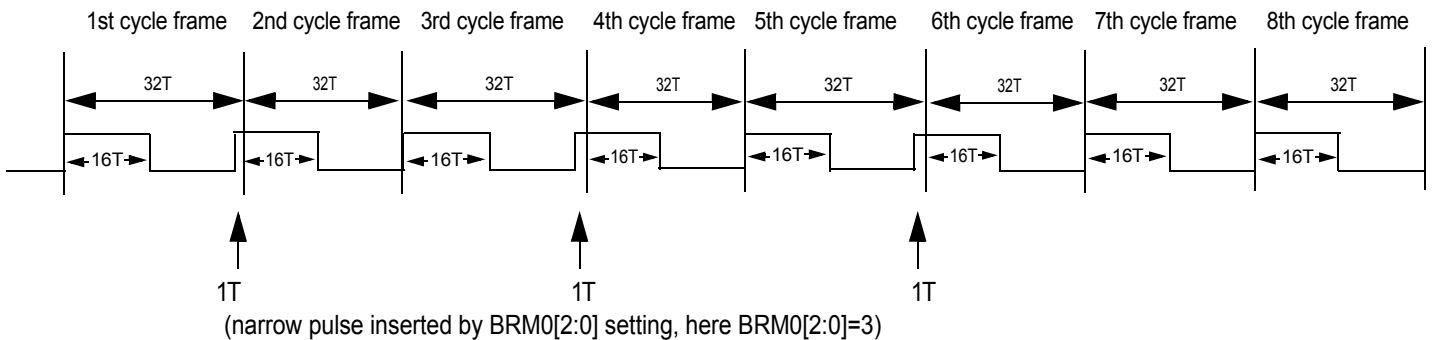
SPWMD[4:0][4:0]: content of SPWM Data Register. It determines duty cycle of SPWM output waveform.

BRM[4:0][2:0]: will insert certain narrow pulses among an 8-SPWM-cycle frame

N = BRM[4:0][2:0]	Number of SPWM cycles inserted in an 8-cycle frame
XX1	1
X1X	2
1XX	4

Example of SPWM timing diagram:

```
MOV SPWMD0, #83H ; SPWMD0[4:0]=10h (=16T high, 16T low), BRM0[2:0] = 3
MOV P1CON, #08H ; Enable P1.3 as PWM output pin
```



SPWM clock = $1 / T = F_{osc} / 2^{(PDIV+1)}$
 The SPWM output cycle frame frequency = $SPWM\ clock / 32 = [F_{osc} / 2^{(PDIV+1)}] / 32$

If user use $F_{osc}=20MHz$, $PDIV[1:0]$ of $SPWMC=\#03H$, then
 $SPWM\ clock = 20MHz / 2^4 = 20MHz / 16 = 1.25MHz$
 $SPWM\ output\ cycle\ frame\ frequency = (20MHz / 2^4) / 32 = 39.1KHz$

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Operating Conditions

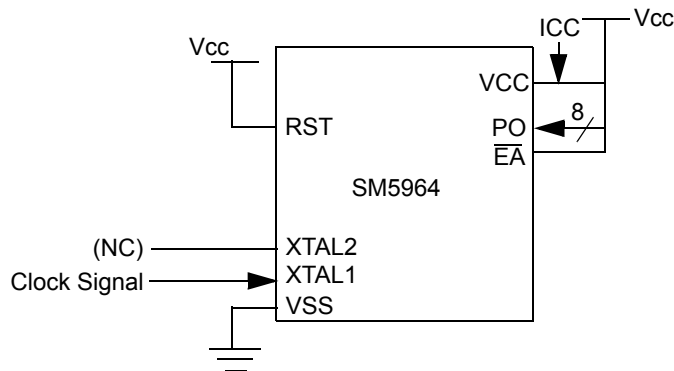
Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	°C	Ambient temperature under bias
TS	Storage temperature	-55	25	155	°C	
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc 16	Oscillator Frequency	3.0	16	16	MHz	For 5V application
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	"
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	"
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	"
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		± 10	uA	0.45V<Vin<Vcc
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

ICC Active mode test circuit



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AC Characteristics

(16/25/40 MHZ, operating conditions; CL for Port 0, ALE and PSEN Outputs=150uF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	f osc 16			Variable f osc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T - 10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

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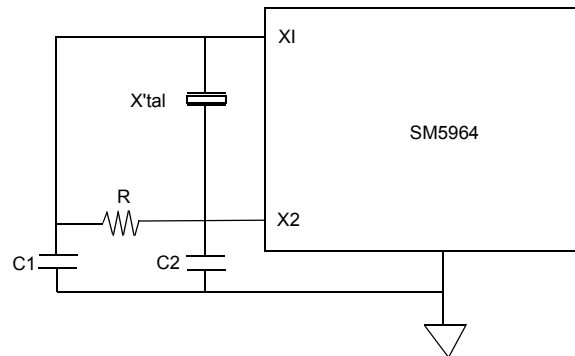
ISP Test Conditions

(40 MHz, typical operating conditions, valid for SM5964 series)

Symbol	MAX	Remark
Chip erase	1500ms	V _{CC} = 5V
Page erase	10ms	“
Program	30us	“
Protect	400us	“

Application Reference

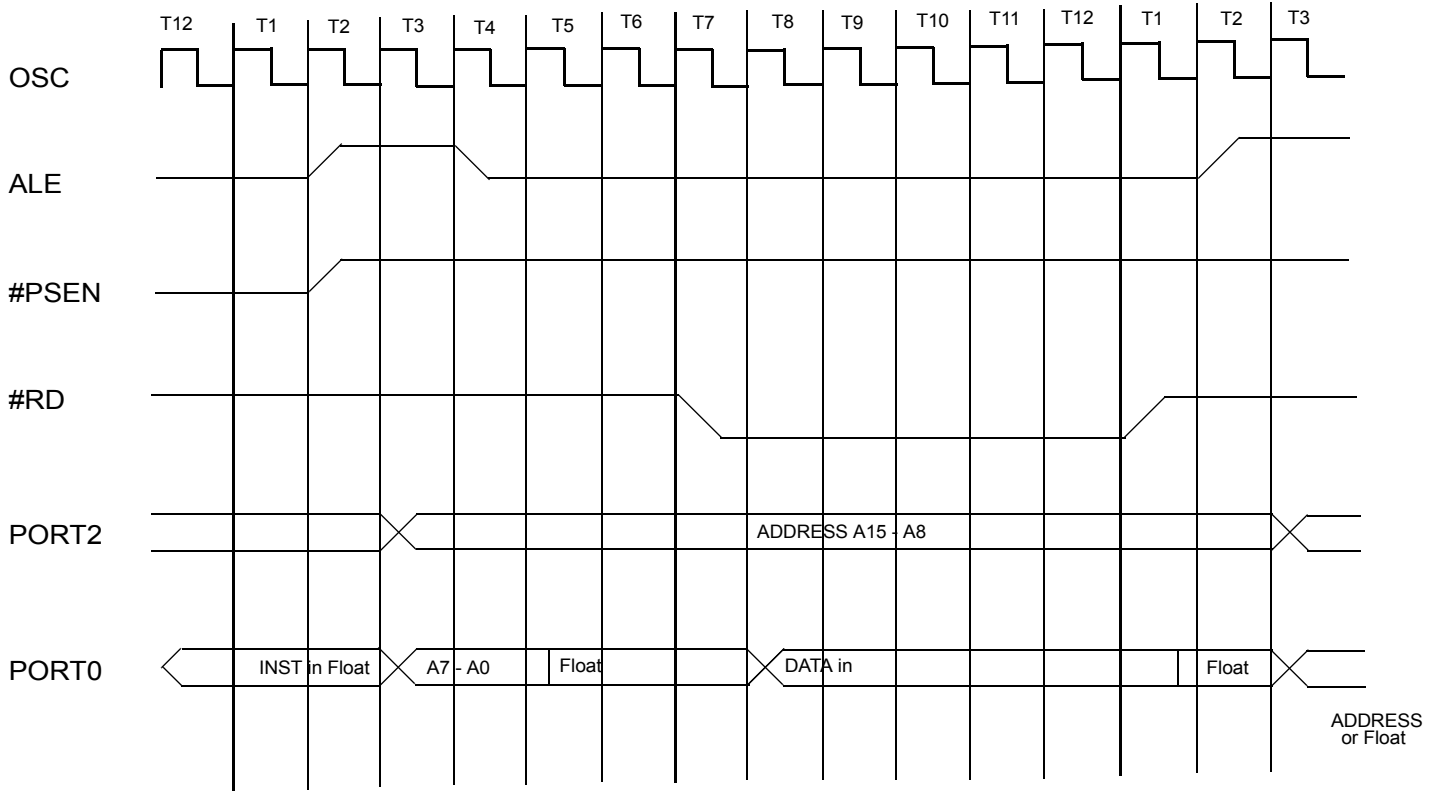
Valid for SM5964				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ



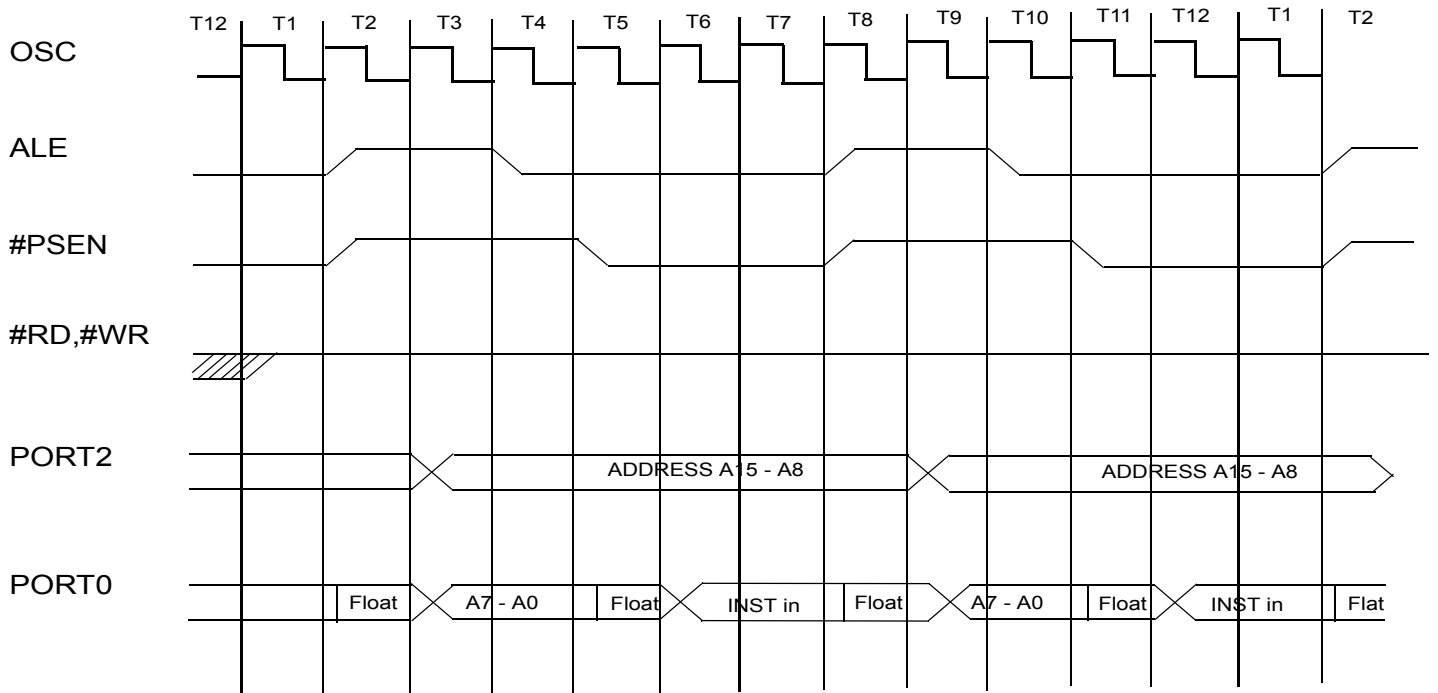
Note: Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacture for appropriate value of external components. Please see SM5964 application note for details.



Data Memory Read Cycle Timing



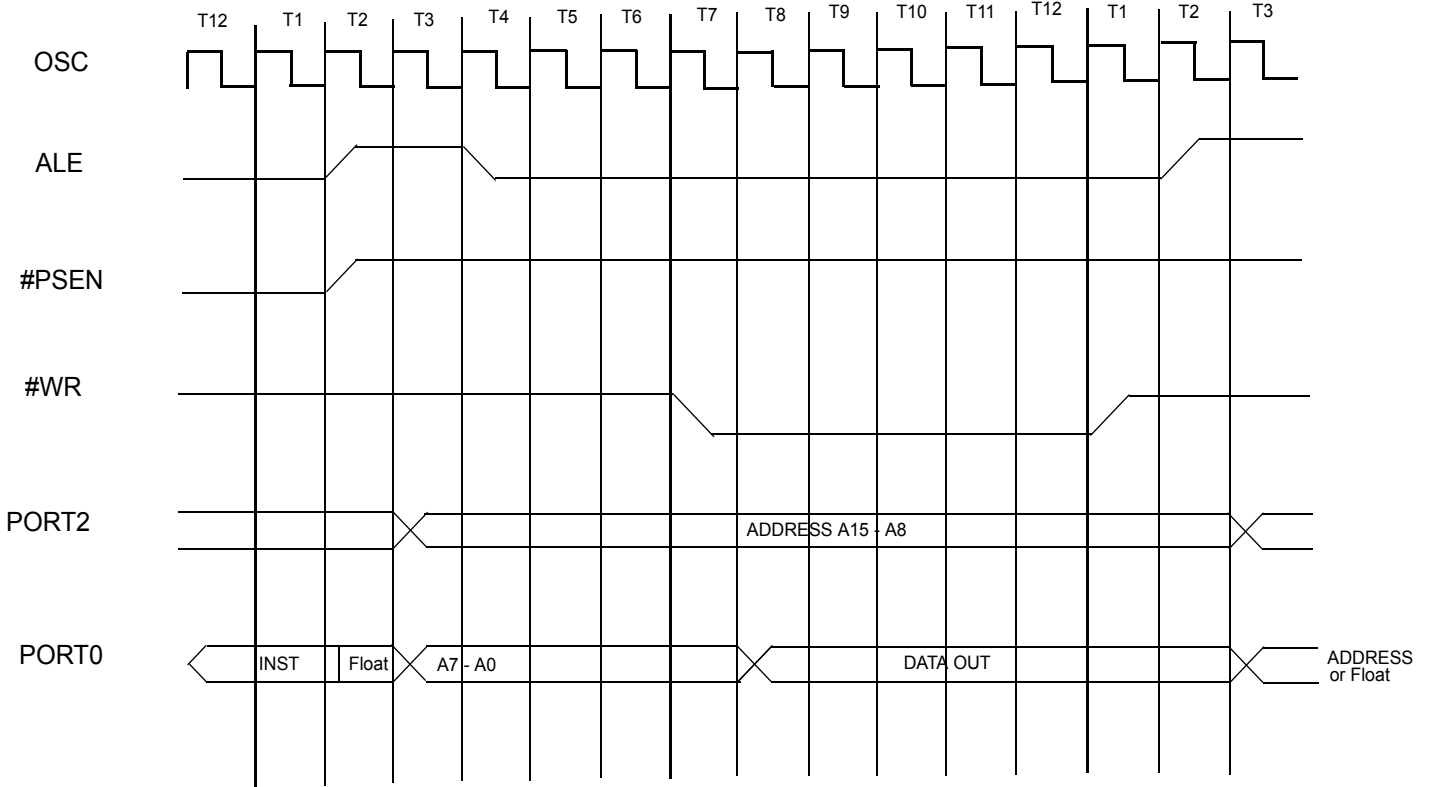
Program Memory Read Cycle Timing



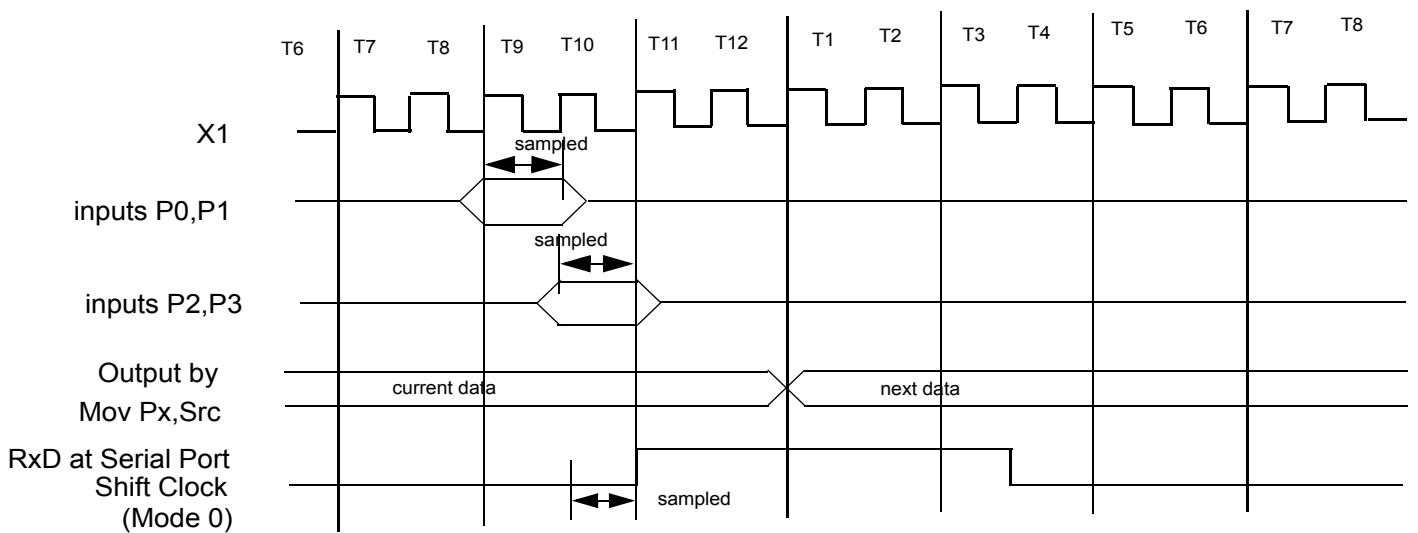
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Data Memory Write Cycle Timing



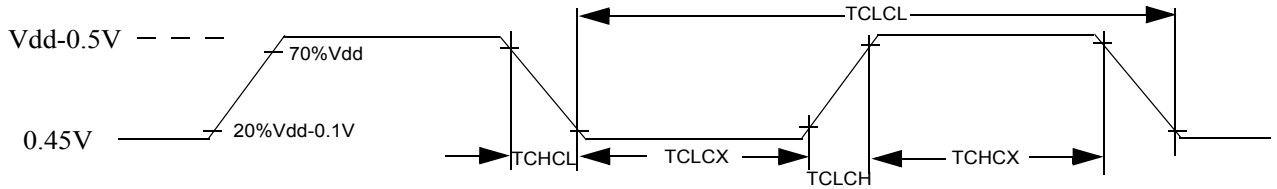
I/O Ports Timing



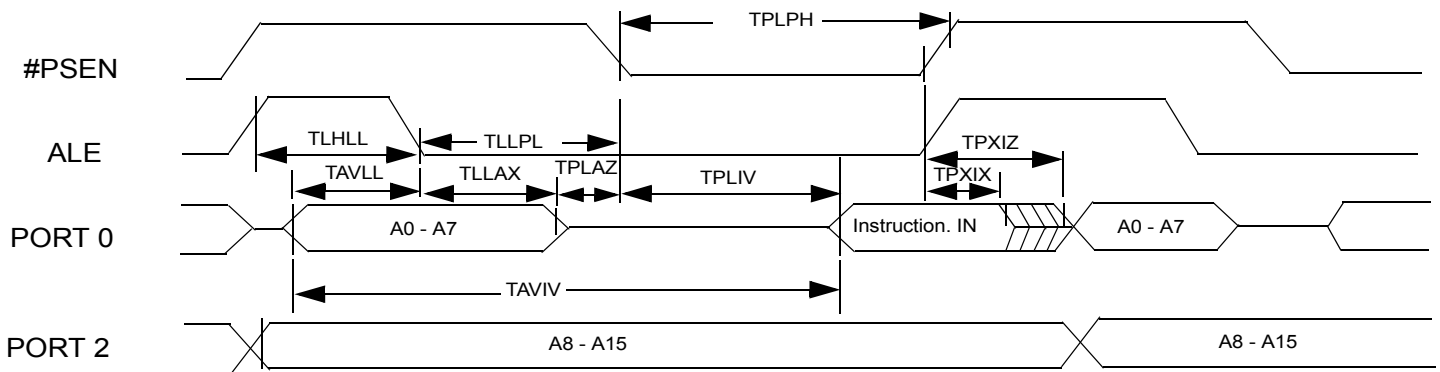
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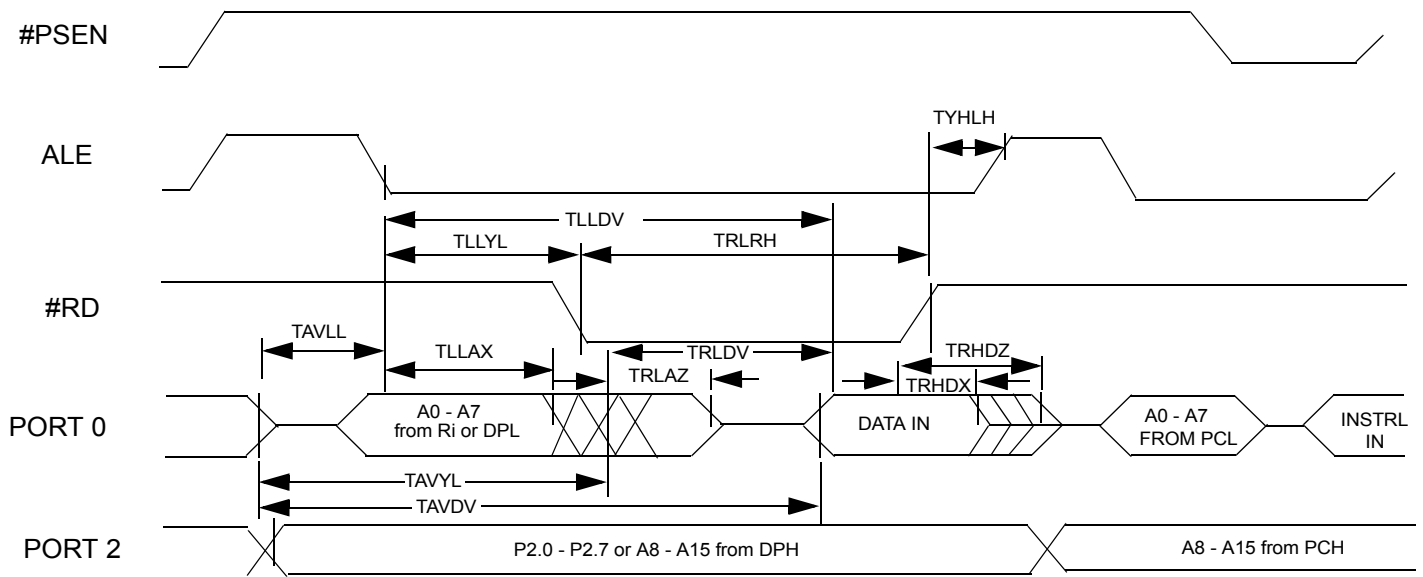
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



Tm.I External Program Memory Read Cycle



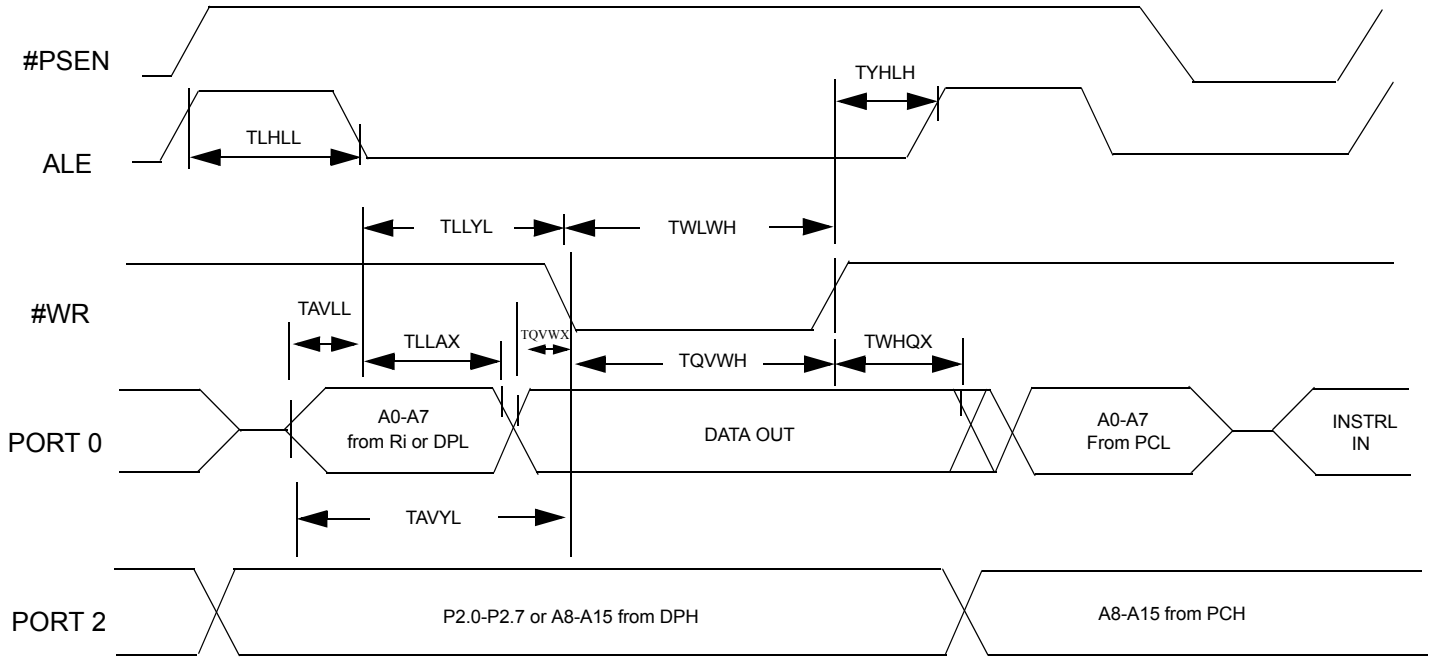
Tm.II External Data Memory Read Cycle



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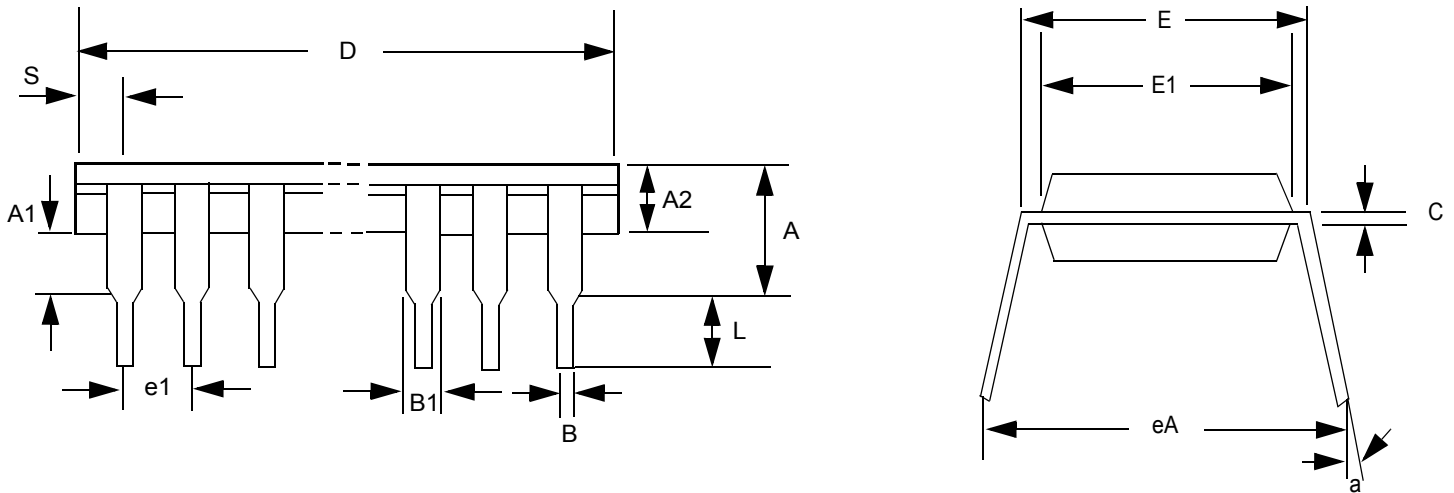


Tm.III External Data Memory Write Cycle





40L 600mil PDIP Information



Note:

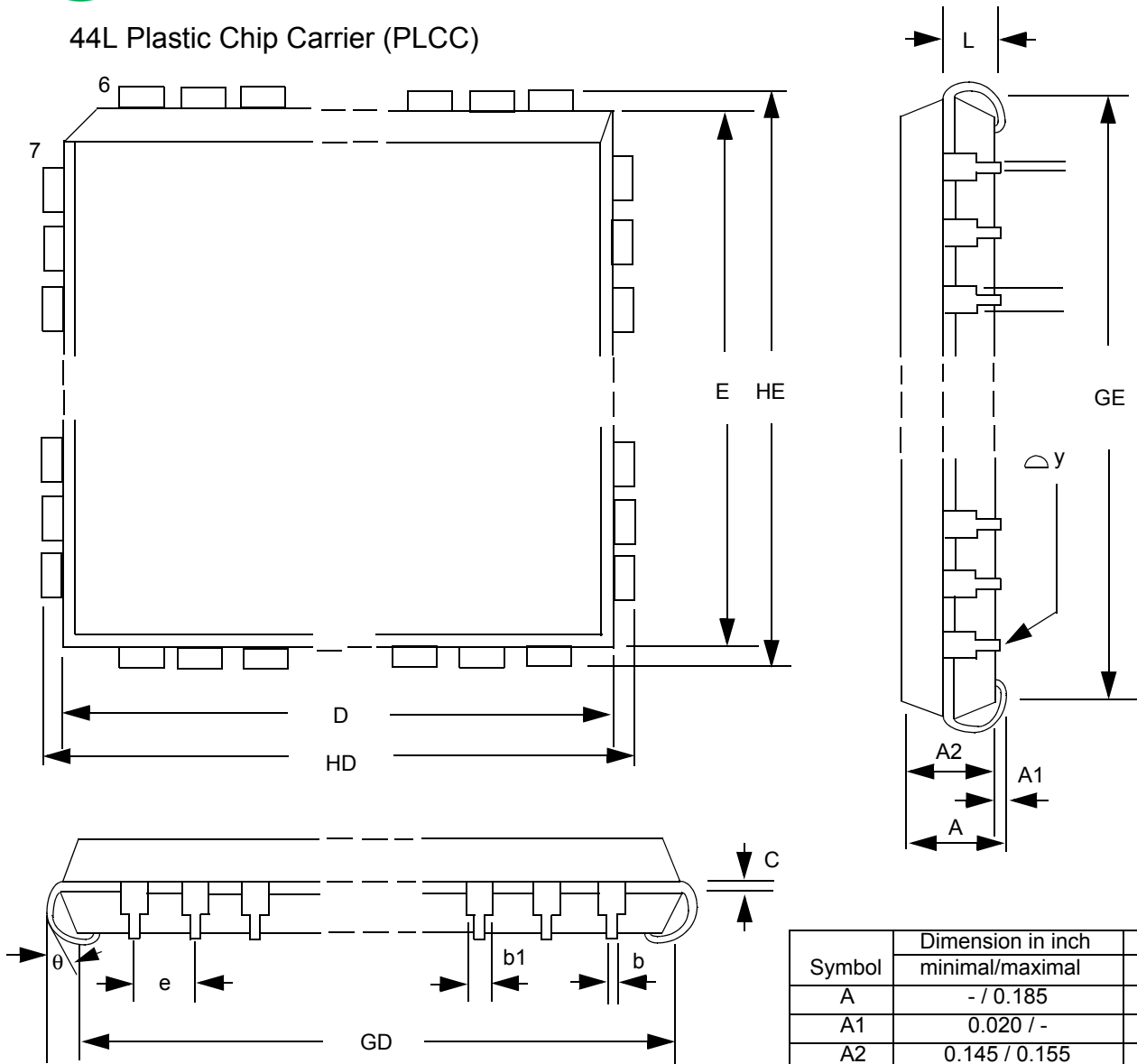
1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include inter lead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dam bar protrusion/infusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual

Symbol	Dimension in inch	Dimension in mm
	minimal/maximal	minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0 / 15	0 / 15
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29



July 2002

44L Plastic Chip Carrier (PLCC)



Note:

1. Dimension D & E does not include inter lead flash.
2. Dimension b1 does not include dam bar protrusion/ intrusion.
3. Controlling dimension: Inch
4. General appearance spec. should base on final visual inspection spec.

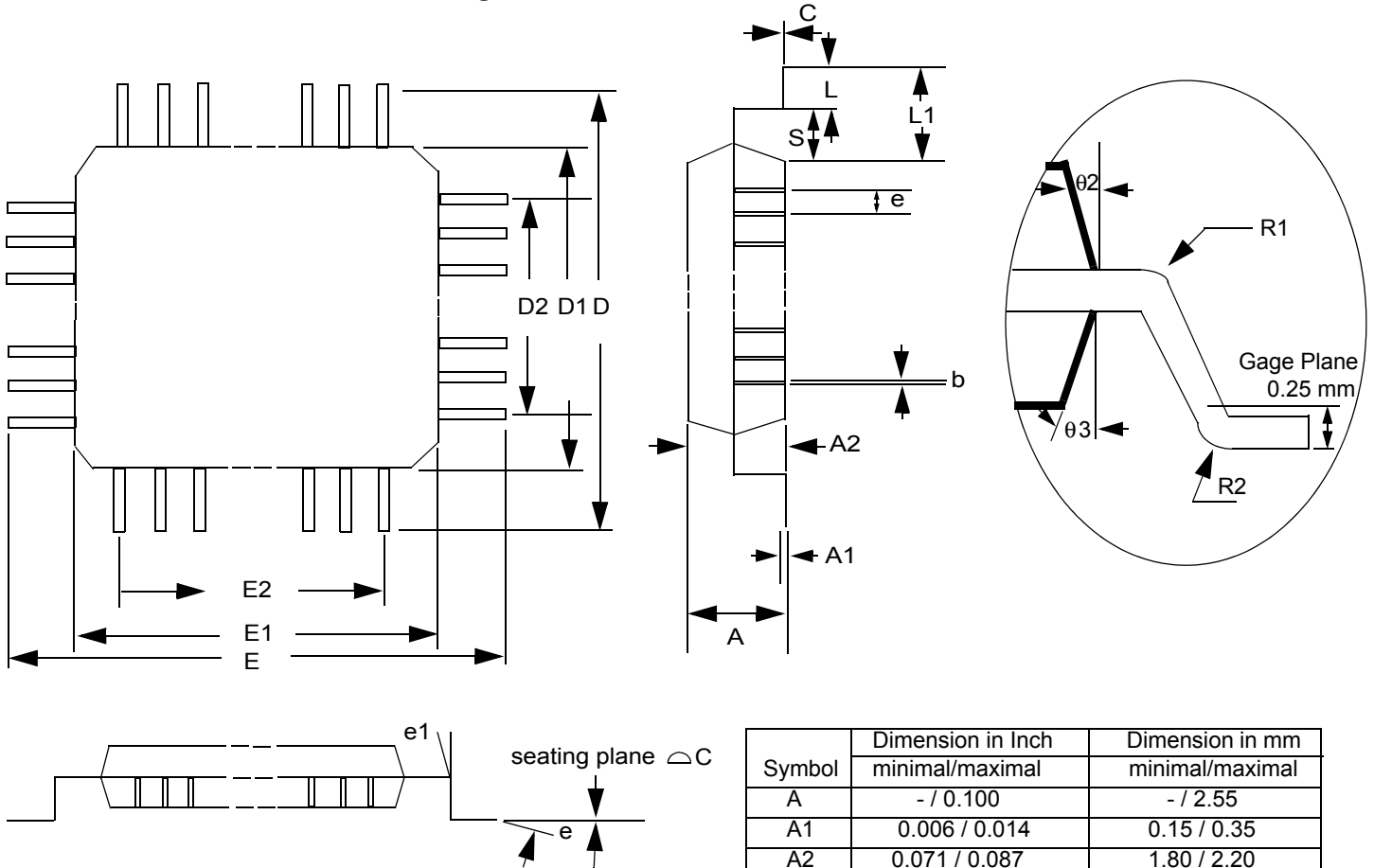
Symbol	Dimension in inch		Dimension in mm	
	minimal/maximal		minimal/maximal	
A	- / 0.185		- / 4.70	
A1	0.020 / -		0.51 / -	
A2	0.145 / 0.155		3.68 / 3.94	
b1	0.026 / 0.032		0.66 / 0.81	
b	0.016 / 0.022		0.41 / 0.56	
C	0.008 / 0.014		0.20 / 0.36	
D	0.648 / 0.658		16.46 / 16.71	
E	0.648 / 0.658		16.46 / 16.71	
e	0.050 BSC		1.27 BSC	
GD	0.590 / 0.630		14.99 / 16.00	
GE	0.590 / 0.630		14.99 / 16.00	
HD	0.680 / 0.700		17.27 / 17.78	
HE	0.680 / 0.700		17.27 / 17.78	
L	0.090 / 0.110		2.29 / 2.79	
θ	- / 0.004		- / 0.10	
$\triangle y$	/		/	

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July 2002

44L Plastic Quad Flat Package



Note:

Dimension D1 and E1 do not include mold protrusion. Allowance protrusion is 0.25mm per side.
 Dimension D1 and E1 do include mold mismatch and are determined datum plane.
 Dimension b does not include dam bar protrusion. Allowance dam bar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dam bar cannot be located on the lower radius or the lead foot.

Symbol	Dimension in Inch	Dimension in mm
	minimal/maximal	minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
△ C	0.004	0.10

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eMCU writer list		
Company	Contact info	Programmer Model Number
<u>Advantech</u> 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	LabTool - 48 (1 * 1) LabTool - 848 (1*8)
<u>Caprillon</u> P.O. Box 461 KaoHsiung, Taiwan, ROC Web site: http://www.market.net.tw/~ cap/	Tel:07-3865061 Fax:07-3865421 E-mail: cap@market.net.tw	UNIV2000
<u>Hi-Lo</u> 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Web site: http://www.hilosystems.com.tw	Tel:02-87923301 Fax:02-87923285 E-mai: support@hilosystems.com.tw	All - 11 (1*1) Gang - 08 (1*8)
<u>Leap</u> 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Web site: http://www.leap.com.tw	Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	ChipStation (1*1) SU - 2000 (1*8)
<u>Xeltek Electronic Co., Ltd</u> 338 Hongwu Road, Nanjing, China 210002 Web site: http://www.xeltek-cn.com	Tel:+86-25-4408399, 4543153-206 E-mail: xelclw@jlonline.com , xelgbw@jlonline.com	Superpro/2000 (1*1) Superpro/680 (1*1) Superpro/280 (1*1) Superpro/L+(1*1)



July 2002

Feedback / Inquiry:

To : SyncMOS Technologies, Inc.	From : _____
Attn : MKT / Customer Service Dept.	Company : _____
Fax : 886-3-579-2960	Dept, Section : _____
: 886-3-578-0493	Position Title : _____
Tel : 886-3-579-2987	Inquiry Date : _____
: 886-3-578-3344 # 2667	Ref No : _____

Description:

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