D80530

8-bit Microcontroller Core

The D80530 core implements a fast, single-chip, 8-bit microcontroller that executes all ASM51 instructions. It has the same instruction set as the 80C31, but its Dallas architecture executes operations an average of 2.5 times faster.

The D80530 provides software and hardware interrupts, a serial communications interface, extra timer features, and power management.

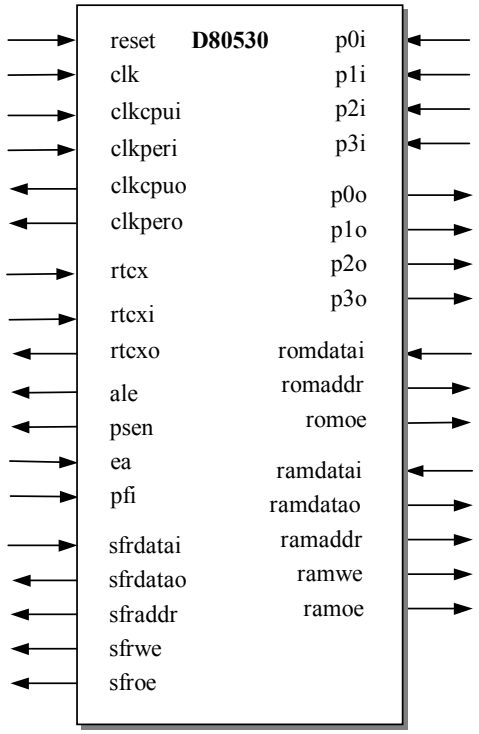
The microcode-free, strictly synchronous design was developed for reuse in ASICs and FPGAs. Scan insertion is straightforward.

Applications

The D80530 can be utilized for a variety of applications including:

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and vide

Symbol



Features

- 8-bit Control Unit
- 8-bit Arithmetic-Logic Unit
- 32-bit Input/Output ports
- Three 16-bit Timer/Counters
- Two Serial Peripheral Interfaces in full duplex mode
- Three priority/Fourteen source Interrupt Controller
- 27-bit Programmable Watchdog Timer
- Internal Data Memory interface can address up to 256 bytes of Read/Write Data Memory space
- External Memory Interface
  - Can address up to 64 K bytes of External Program Memory space and up to 64 K bytes of External Data Memory space
  - Can address up to 64 K bytes of External Data Memory Space
  - Dual Data Pointer
  - Variable length MOVX to access fast/slow RAM/peripherals
- Services up to 67 External Special Function Registers
- Power Management Features
  - EMI reduction mode disables ALE
  - Early-warning power-fail interrupt
- Real Time Clock

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Functional Description

The D80530 core is partitioned into modules as shown above and described below.

Core Engine

The D80530 engine is composed of four components:

- Control unit
- Arithmetic-logic unit
- Memory control unit
- RAM and SFR control unit

The D80530 engine allows to fetch instructions from program memory and to execute using RAM or SFR.

The Arithmetic-logic unit serves:

- 8 bit arithmetic operations
- 8 bit logical operations
- Boolean manipulations
- 8 x 8 bit multiplication
- 8 / 8 bit division

The RAM and SFR control unit:

- Can address up to 256 bytes of Read/Write Data Memory Space
- Serves the Interface for off-core Special Function Registers

The Memory control unit:

- Can address up to 64 K bytes of External Program Memory Space
- Can address up to 64 K bytes of External Data Memory Space

Timer 0 and 1

Timers 0 and 1 are nearly identical. Timers 0 and 1 both have four modes. They are:

- 13-bit Timer/counter
- 16-bit Timer/counter
- 8-bit timer/counter with auto reload
- Two 8-bit timers

The later mode is available to Timer 0 only. Each timer can also serve as a counter of external pulses (1 to 0 transition) on the corresponding T0 or T1 pin. One other option is to gate the timer/counter using an external control signal. This allows the timer to measure the pulse width of external signals.

Timer 2

Timer 2 has several abilities not found in Timers 0 and 1. However, it does not offer the 13-bit and dual 8-bit modes. Thus it runs in 16-bit mode at all times. Also note that instead of offering 8-bit auto-reload mode, Timer 2 has a 16-bit auto-reload mode. This mode uses the Timer Capture registers to hold the reload values.

Serial 0 and 1

The D80530 core provides two fully independent serial ports for simultaneous communication over two channels. The serials can operate in identical or different modes and communication speeds. Each serial port is capable of both synchronous and asynchronous modes. In synchronous mode, the microcontroller generates the clock and operates in a half-duplex mode. In asynchronous mode, full duplex operation is available. Receive data is buffered in a holding register. This allows the serial to receive an incoming word before software has read the previous value.

Each port provides four operating modes. These offer different communication protocols and baud rates:

- Synchronous mode, fixed baud rate
- 8-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- 9-bit UART mode, variable baud rate

Interrupt Service Routine

The D80530 core improves three-priority interrupt system. There are 14 interrupt sources. Each source has an independent priority bit, flag, interrupt vector, and enable. In addition, interrupts can be globally enabled or disabled.

Ports

The D80530 provides four I/O ports. Port 0 – Port 3 are an 8-bit bi-directional I/O ports with separated inputs and outputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memories.

Port 1 also serves the special features like external interrupt inputs, Serial 1 interface, and Timer 2 inputs.

Port 2 emits the high-order address byte during fetches from external program memory that use 16-bit addresses (MOVX @DPTR).

Port 3 also serves the special features like read and write strobes for external data memory, Serial 0 interface, Timer 0 and Timer 1 inputs.

Power Management Unit

The D80530 core has several features relate to power consumption and management.

The range of features is shown below

- Power management modes IDLE and STOP
- Early-warning power-fail interrupt
- EMI reduction mode disables ALE

Devices, which incorporate the precision voltage reference, have the ability to generate power-fail interrupt. The microcontroller has input of the power-fail interrupt. This early warning of supply voltage allows the system time to save critical parameters in nonvolatile memory and put external functions in a safe state.

The D80530 provides two modes that allow power conservation. They are similar, but have different merits and drawbacks. These modes are IDLE and STOP.

IDLE mode suspends all engine processing by holding the program counter in a static state. No program values are fetched and no processing occurs. This saves considerable power versus full operation. All clocks remain active so the timers, Watchdog, and Serial Port functions are all working. Since all clocks are running, the engine can exit the IDLE mode using any of the interrupt sources. There are two ways to exit the IDLE mode. First, any enabled interrupt will cause an exit. The IDLE mode can also be removed using a reset.

STOP mode is the lowest power state that D80530 core can enter. This is achieved by stopping all on-core clocks, resulting in a fully static condition. No processing is possible, timers are stopped, and no serial communication is possible. Processor operation will halt on the instruction that sets the STOP bit. The STOP mode can be exited in two ways. First a non-clocked interrupt such as the external interrupt or power-fail interrupt. A second method of exiting STOP mode is with an external reset.

Watchdog Timer

The Watchdog Timer is a user programmable clock counter that can serve as a time-base generator, an event timer, or a system supervisor. The timer is driven by the main system clock that is supplied to a series of dividers. The watchdog counter has 27-bit width. The divider output is selectable, and determines the interval between time-outs. When the time-out is reached, an interrupt flag will be set, and if enabled, a reset will occur. The interrupt flag will cause an interrupt to occur if its individual enable bit is set and the global interrupt enable is set.

Real Time Clock

The real time clock implements a real time count with a resolution of 1/256th second. It allows the user to read seconds, minutes, hours, day of the week and the date. The date is represented by a 16-bit number, which value is interpreted by the user software. The RTC enables a count of 179 years. The RTC features an alarm function which may be used to generate interrupts at a given time during a day or periodically. These interrupts may be used to resume operation from the STOP mode at a given time

Performance

The architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most instructions have the same number of cycles as bytes. The D80530 uses 4 clocks per cycle. This leads to performance improvement of rate 2.5x (in terms of MIPS) with respect to the Intel device working with the same clock frequency (the original 8051 had a 12-clock architecture. A machine cycle needed 12 clocks and most instructions were either one or two machine cycles. Thus except for the MUL and DIV instructions, the 8051 used either 12 or 24 clocks for each instruction. Furthermore, each cycle in the 8051 used two memory fetches. In many cases the second fetch was dummy, and extra clocks were wasted).

The table below illustrates the speed advantage of the D80530 over the standard 8051. A speed advantage of 3 means that the D80530 performs the same instruction three times faster that the 8051.

Speed advantage	Number of instructions	Number of opcodes
3	53	160
2	2	2
2.4	16	37
1.5	38	54
1	2	2
Average: 2.5	Sum: 111	Sum: 255

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The D80530 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 and Dallas DS80C320 chips, and the results compared with the core's simulation outputs.

Deliverables

The core includes everything required for successful implementation:

- VHDL or Verilog RTL
- Post-synthesis EDIF netlist (netlist license)
- Testbench (self checking)
- Vectors for testing the core
- Place & Route Scripts (netlist license)
- Synthesis and simulation scripts
- Constraint file
- Instantiation templates
- Documentation

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This core developed by the processor experts at Evatronix SA.