

Extended 8-bit Microcontroller with Serial Communication Interfaces

1. Description

The TSC87251G1A products are derivatives of the TEMIC Microcontroller family based on the extended 8-bit C251 Architecture. This family of products is tailored to 8-bit microcontroller applications requiring an increased instruction throughput, a reduced operating frequency or a larger addressable memory space. The architecture can provide a significant code size reduction when compiling C programs while fully preserving the legacy of C51 assembly routines.

The TSC87251G1A derivatives are pin-out and software compatible with standard 80C51/Fx/Rx with extended on-chip data memory (1 Kbyte RAM), on-chip memory (16 Kbytes EPROM/OTPROM) and up to 256 Kbytes of external code and data.

They provide transparent enhancements to Intel's 87C251Sx family with an additional Synchronous Serial Link Controller (SSLC supporting I²C, μ Wire and SPI protocols), a Keyboard interrupt interface and Power Monitoring and Management features.

Notes:

This Datasheet provides the technical description of the TSC87251G1A derivatives. For further information on the device usage, please request the TSC80251 Programmers' Guide and the TSC80251G1 Design Guide.

For information on the Mask ROM and ROMless devices, please refer to the TSC87251G1D Datasheet.

2. Typical Applications

- ISDN terminals
- High-Speed modems
- PABX (SOHO)
- Networking
- Line cards
- Computer peripherals
- Printers
- Plotters
- Scanners
- Banking machines
- Barcode readers
- Smart cards readers
- High-end digital monitors
- High-end joysticks



Purchase of TEMIC I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

3. Features

- Pin-Out and software compatibility with standard 80C51 products and 80C51FA/FB/RA/RB
- Plug-in replacement of Intel's 80C251Sx
- C251 core: Intel's MCS[®]251 step A compliance
 - 125 ns Instruction cycle time at 16 MHz
 - 40-byte Register File
 - Registers Accessible as Bytes, Words or Dwords
 - Six-stage instruction Pipeline
 - 16-bit Internal Code Fetch
- Enriched C51 Instruction Set
 - 16-bit and 32-bit ALU
 - Compare and Conditional Jump Instructions
 - Expanded Set of Move Instructions
- Linear Addressing
- 1 Kbyte of on-chip RAM
- External memory space (Code/Data) programmable from 64 Kbytes to 256 Kbytes
- TSC87251G1A: 16 Kbytes of on-chip EPROM/OTPROM (production with TSC83251G1D: on-chip masked ROM version)
- SINGLE-PULSE Programming Algorithm
- Four 8-bit parallel I/O Ports (Ports 0, 1, 2 and 3 of the standard 80C51)
- Serial I/O Port: full duplex UART (80C51 compatible) with independent Baud Rate Generator
- SSLC: Synchronous Serial Link Controller
 - I²C master only protocol
 - μ Wire and SPI master only protocol
- Three 16-bit Timers/Counters (Timers 0, 1 and 2 of the standard 80C51)
- EWC: Event and Waveform Controller
 - Compatible with Intel's Programmable Counter Array (PCA)
 - Common 16-bit Timer/Counter reference with four possible clock sources ($F_{osc}/4$, $F_{osc}/12$, Timer 1 and external input)
 - Five modules with four programmable modes:
 - 16-bit software Timer/Counter
 - 16-bit Timer/Counter Capture Input and software pulse measurement
 - High-speed output and 16-bit software Pulse Width Modulation (PWM)
 - 8-bit hardware PWM without overhead
 - 16-bit Watchdog Timer/Counter capability
- Secured 14-bit Hardware Watchdog Timer
- Power Monitoring and Management
 - Power-Fail reset
 - Power-On reset (integrated on the chip)
 - Power-Off flag (cold and warm resets)
 - Software programmable system clock
 - Idle and Power-Down modes
- Keyboard interrupt interface on Port 1
- ONCE mode and full speed Real-Time In-Circuit Emulation support (Third Party Vendors)
- Speed ranges:
 - 0 to 16 MHz
- Supply ranges:
 - 5 V \pm 10 %
- Temperature ranges:
 - Commercial (0°C to +70°C)
 - Industrial (-40°C to +85°C)
 - Option: extended range (-55°C to +125°C)
- Packages:
 - PDIL 40, PLCC 44
 - UV-Window CQPJ 44
 - Options: known good dice and ceramic packages

4. Block Diagram

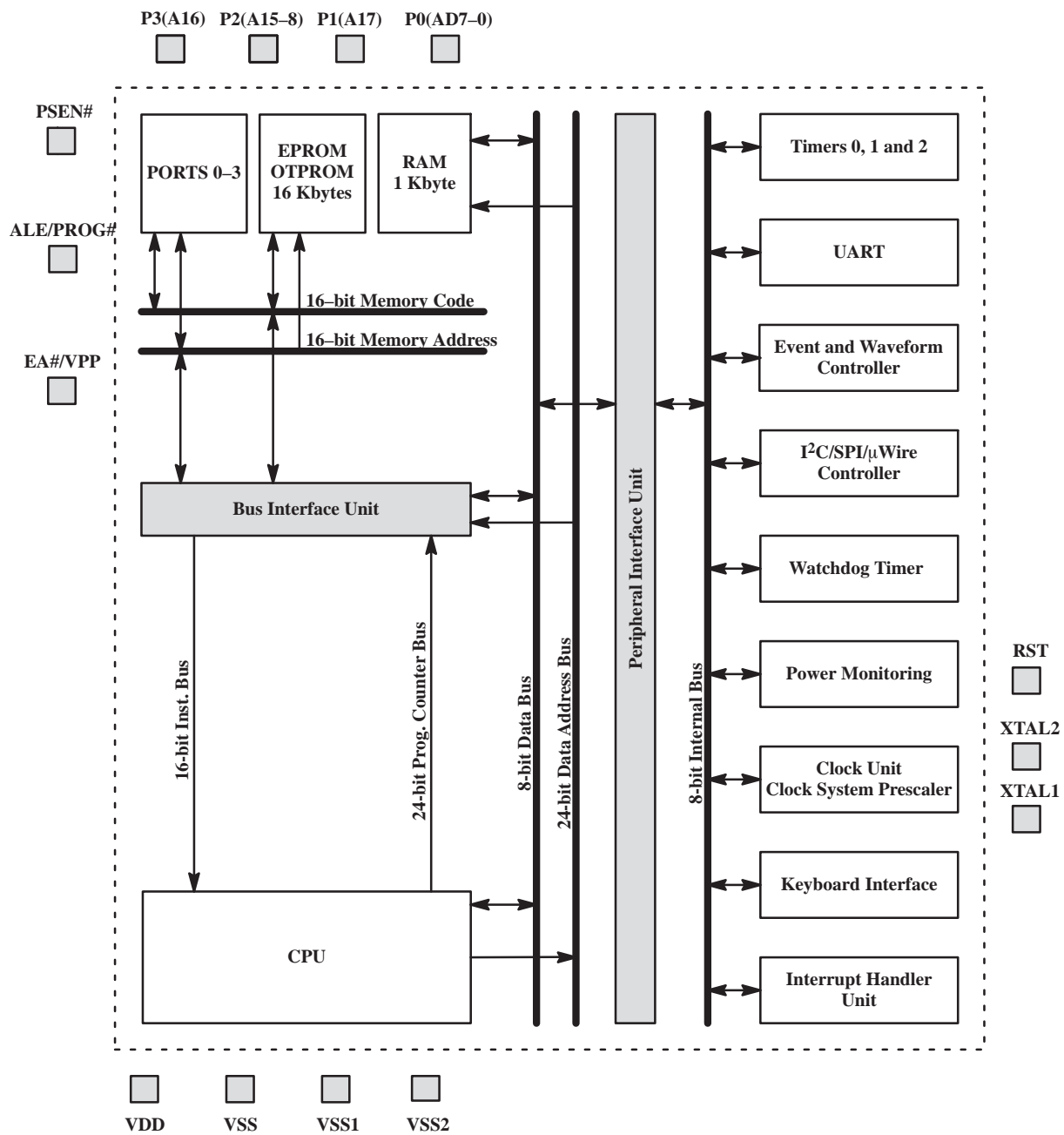


Figure 1. TSC87251G1A Block Diagram

5. Pin Description

5.1. Pinout

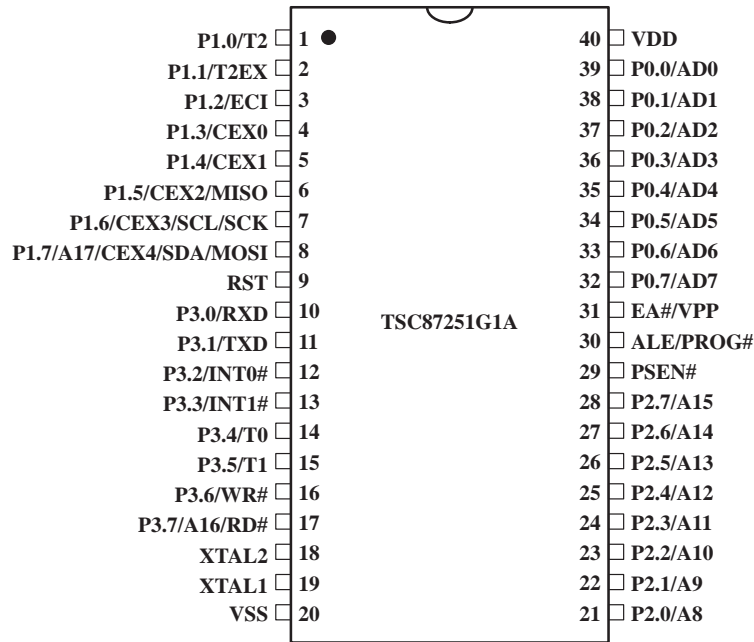


Figure 2. TSC87251G1A 40-pin DIP package

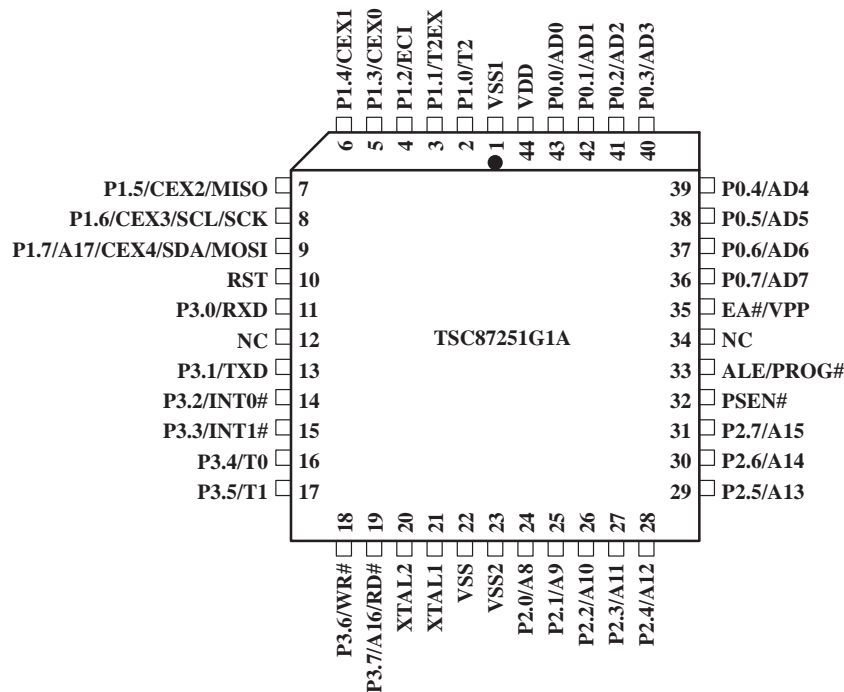


Figure 3. TSC87251G1A 44-pin PLCC/CQPJ Package

Table 1. TSC87251G1A Pin Assignment

| DIP | PLCC | Name | DIP | PLCC | Name |
|-----|------|------------------------|-----|------|-----------|
| | 1 | VSS1 | | 23 | VSS2 |
| 1 | 2 | P1.0/T2 | 21 | 24 | P2.0/A8 |
| 2 | 3 | P1.1/T2EX | 22 | 25 | P2.1/A9 |
| 3 | 4 | P1.2/ECI | 23 | 26 | P2.2/A10 |
| 4 | 5 | P1.3/CEX0 | 24 | 27 | P2.3/A11 |
| 5 | 6 | P1.4/CEX1 | 25 | 28 | P2.4/A12 |
| 6 | 7 | P1.5/CEX2/MISO | 26 | 29 | P2.5/A13 |
| 7 | 8 | P1.6/CEX3/SCL/SCK | 27 | 30 | P2.6/A14 |
| 8 | 9 | P1.7/A17/CEX4/SDA/MOSI | 28 | 31 | P2.7/A15 |
| 9 | 10 | RST | 29 | 32 | PSEN# |
| 10 | 11 | P3.0/RXD | 30 | 33 | ALE/PROG# |
| | 12 | NC | | 34 | NC |
| 11 | 13 | P3.1/TXD | 31 | 35 | EA#/VPP |
| 12 | 14 | P3.2/INT0# | 32 | 36 | P0.7/AD7 |
| 13 | 15 | P3.3/INT1# | 33 | 37 | P0.6/AD6 |
| 14 | 16 | P3.4/T0 | 34 | 38 | P0.5/AD5 |
| 15 | 17 | P3.5/T1 | 35 | 39 | P0.4/AD4 |
| 16 | 18 | P3.6/WR# | 36 | 40 | P0.3/AD3 |
| 17 | 19 | P3.7/A16/RD# | 37 | 41 | P0.2/AD2 |
| 18 | 20 | XTAL2 | 38 | 42 | P0.1/AD1 |
| 19 | 21 | XTAL1 | 39 | 43 | P0.0/AD0 |
| 20 | 22 | VSS | 40 | 44 | VDD |

5.2. Signals

Table 2. TSC87251G1A Signal Descriptions

| Signal Name | Type | Description | Alternate Function |
|----------------------|------|--|--------------------|
| A17 | O | 18th Address Bit Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13). | P1.7 |
| A16 | O | 17th Address Bit Output to memory as 17th external address bit (A16) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13). | P3.7 |
| A15:8 ⁽¹⁾ | O | Address Lines Upper address lines for the external bus. | P2.7:0 |
| AD7:0 ⁽¹⁾ | I/O | Address/Data Lines Multiplexed lower address lines and data for the external memory. | P0.7:0 |
| ALE | O | Address Latch Enable ALE signals the start of an external bus cycle and indicates that valid address information are available onlines A16/A17 and A7:0. An external latch can use ALE to demultiplex the address from address/databus. | |
| CEX4:0 | O | PCA Input/Output pins CEXx are input signals for the PCA capture mode and output signals for the PCA compare and PWM modes. | P1.7:3 |
| EA# | I | External Access Enable EA# directs program memory accesses to on-chip or off-chip code memory. For EA#= 0, all program memory accesses are off-chip. For EA#= 1, an access is on-chip EPROM/OTPROM if the address is within the range of the on-chip EPROM/OTPROM; otherwise the access is off-chip. The value of EA# is latched at reset. | |

| Signal Name | Type | Description | Alternate Function |
|-------------|------|--|--------------------|
| ECI | O | PCA External Clock input ECI is the external clock input to the 16-bit PCA timer. | P1.2 |
| MISO | I/O | SPI Master Input Slave Output line When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller. | P1.5 |
| MOSI | I/O | SPI Master Output Slave Input line When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller. | P1.7 |
| INT1:0# | I | External Interrupts 0 and 1. INT1#/INT0# inputs set IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits IT1:0 are cleared, bits IE1:0 are set by a low level on INT1#/INT0# | P3.3:2 |
| P0.0:7 | I/O | Port 0 P0 is an 8-bit open-drain bidirectional I/O port. | AD7:0 |
| P1.0:7 | I/O | Port 1 P1 is an 8-bit bidirectional I/O port with internal pull-ups. P1 provides interrupt capability for a keyboard interface. | |
| P2.0:7 | I/O | Port 2 P2 is an 8-bit bidirectional I/O port with internal pull-ups. | A15:8 |
| P3.0:7 | I/O | Port 3 P3 is an 8-bit bidirectional I/O port with internal pull-ups. | |
| PROG# | O | Programming Pulse input The programming pulse is applied to this input for programming the on-chip EPROM/OTPROM. | |
| PSEN# | O | Program Store Enable/Read signal output PSEN# is asserted for a memory address range that depends on bits RD0 and RD1 in UCONFIG0 byte (see Table 13). | |
| RD# | O | Read or 17th Address Bit (A16) Read signal output to external data memory depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13). | P3.7 |
| RST | I | Reset input to the chip Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation. | |
| RXD | I/O | Receive Serial Data RXD sends and receives data in serial I/O mode 0 and receives data in serial modes I/O 1, 2 and 3. | P3.0 |
| SCL | I/O | I²C Serial Clock SCL outputs the serial clock to slave peripherals. | P1.6 |
| SCK | I/O | SPI Serial Clock SCK outputs clock to the slave peripheral. | P1.6 |
| SDA | I/O | I²C Serial Data SDA is the bidirectional I ² C data line. | P1.7 |
| T1:0 | I/O | Timer 1:0 External Clock Inputs When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count. | |

| Signal Name | Type | Description | Alternate Function |
|-------------|------|---|--------------------|
| T2 | I/O | Timer 2 Clock Input/Output For the timer 2 capture mode, T2 is the external clock input. For the Timer 2 clock-out mode, T2 is the clock output. | P1.0 |
| T2EX | I | Timer 2 External Input In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 register to be reloaded. In the up-down counter mode, this signal determines the count direction: 1= up, 0= down. | P1.1 |
| TXD | I/O | Transmit Serial Data TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3. | P3.1 |
| VDD | PWR | Digital Supply Voltage Connect this pin to +5V or +3V supply voltage. | |
| VSS | GND | Circuit Ground Connect this pin to ground. | |
| VSS1 | GND | Secondary Ground 1 This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC87251G1A as a pin-for-pin replacement for a 8xC51 product, VSS1 can be unconnected without loss of compatibility. Not available on DIP package. | |
| VSS2 | GND | Secondary Ground 2 This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC87251G1A as a pin-for-pin replacement for a 8xC51 product, VSS2 can be unconnected without loss of compatibility. Not available on DIP package. | |
| VPP | I | Programming Supply Voltage The programming supply voltage is applied to this input for programming the on-chip EPROM/OTPROM | |
| WR# | O | Write Write signal output to external memory. | P3.6 |
| XTAL1 | I | Input to the on-chip inverting oscillator amplifier To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing. | |
| XTAL2 | O | Output of the on-chip inverting oscillator amplifier To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected. | |

Note:

1. The description of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the non-page mode chip configuration. If the chip is configured in page mode operation, port 0 carries the lower address bits (A7:0) while port 2 carries the upper address bits (A15:8) and the data (D7:0).

6. Address Spaces

The TSC87251G1A implements four different address spaces:

- On-chip EPROM/OTPROM program/code memory
- On-chip RAM data memory
- Special Function Registers (SFRs)
- Configuration array

6.1. Program/Code Memory

The TSC87251G1A implements 16 Kbytes of on-chip EPROM/OTPROM for program/code memory. Figure 4 shows the split of the internal and external program/code memory spaces. If EA# is tied to a high level, the 16-Kbyte on-chip program/code memory is mapped in the lower part of segment FF: where the C251 core jumps after reset. The rest of the program/code memory space is mapped to the external memory. If EA# is tied to a low level, the internal program/code memory is not used and all the accesses are directed to the external memory.

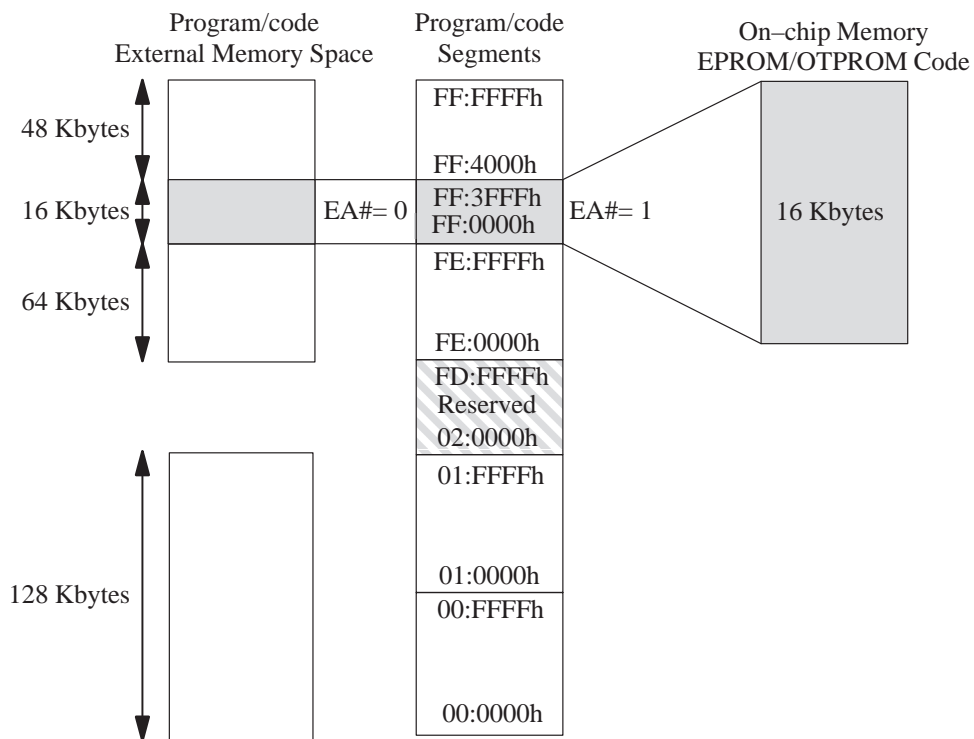


Figure 4. Program/Code Memory Mapping

Notes:

Special care should be taken when the Program Counter (PC) increments:

- If the program executes exclusively from on-chip code memory (not from external memory), beware of executing code from the upper eight bytes of the on-chip EPROM (FF:3FF8h–FF:3FFFh). Because of its pipeline capability, the TSC87251G1A may attempt to prefetch code from external memory (at an address above FF:3FFFh) and thereby disrupt I/O Ports 0 and 2. Fetching code constants from these 8 bytes does not affect Ports 0 and 2.
- When PC reaches the end of segment FF:, it loops to the reset address FF:0000h (for compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).

6.2. Data Memory

The TSC87251G1A implements 1 Kbyte of on-chip data RAM. Figure 5 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on-chip RAM located from 20h to FFh is bit addressable. This on-chip RAM is not accessible through the program/code memory space.

For faster computation with the on-chip EPROM code of the TSC87251G1A, its upper 8 Kbytes are also mapped in the upper part of the region 00: if the On-Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure 7). However, if EA# is tied to a low level, the TSC87251G1A derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 8 Kbytes of the lower 16 Kbytes of the segment FF:). If EMAP# bit is set, the on-chip EPROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on-chip memory mapped onto are redirected to the external memory.

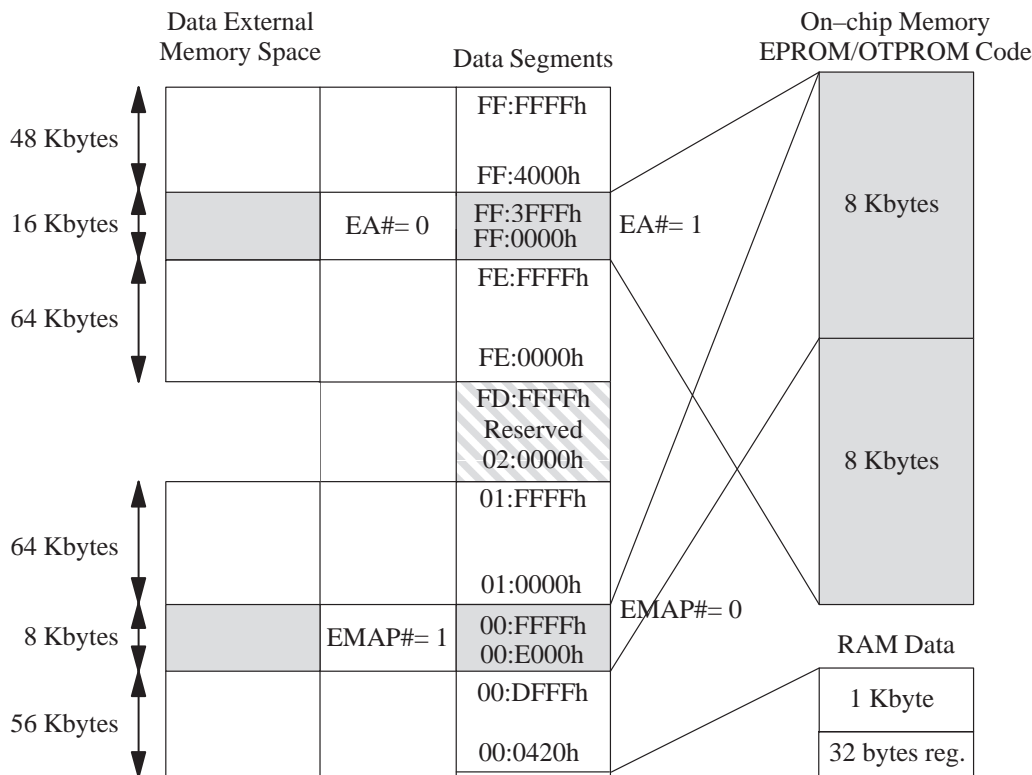


Figure 5. Data Memory Mapping

6.3. Special Function Registers

The Special Function Registers (SFRs) of the TSC87251G1A derivatives fall into the categories detailed in Table 3 to Table 11.

SFRs are placed in a reserved on-chip memory region S: which is not represented in the data memory mapping (Figure 5). The relative addresses within S: of these SFRs are provided together with their reset values in Table 12. They are upward compatible with the SFRs of the standard 80C51 and the Intel's 80C251Sx family. In this table, the C251 core registers are in italics and are described in the TSC80251 Programmer's Guide. The other SFRs are described in the TSC80251G1 Design Guide. All the SFRs are bit-addressable using the C251 instruction set.

Table 3. C251 Core SFRs

| Mnemonic | Name | Mnemonic | Name |
|--------------------|----------------------------|---------------------|---|
| ACC ⁽¹⁾ | Accumulator | SPH ⁽¹⁾ | Stack Pointer High – MSB of SPX |
| B ⁽¹⁾ | B Register | DPL ⁽¹⁾ | Data Pointer Low byte – LSB of DPTR |
| PSW | Program Status Word | DPH ⁽¹⁾ | Data Pointer High byte – MSB of DPTR |
| PSW1 | Program Status Word 1 | DPXL ⁽¹⁾ | Data Pointer Extended Low byte of DPX – Region number |
| SP ⁽¹⁾ | Stack Pointer – LSB of SPX | | |

Note:

1. These SFRs can also be accessed by their corresponding registers in the register file.

Table 4. I/O Port SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|--------|----------|--------|
| P 0 | Port 0 | P 2 | Port 2 |
| P 1 | Port 1 | P 3 | Port 3 |

Table 5. Timers SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|-------------------------------|----------|--|
| TL0 | Timer/Counter 0 Low Byte | TMOD | Timer/Counter 0 and 1 Modes |
| TH0 | Timer/Counter 0 High Byte | T2CON | Timer/Counter 2 Control |
| TL1 | Timer/Counter 1 Low Byte | T2MOD | Timer/Counter 2 Mode |
| TH1 | Timer/Counter 1 High Byte | RCAP2L | Timer/Counter 2 Reload/Capture Low Byte |
| TL2 | Timer/Counter 2 Low Byte | RCAP2H | Timer/Counter 2 Reload/Capture High Byte |
| TH2 | Timer/Counter 2 High Byte | WDTRST | WatchDog Timer Reset |
| TCON | Timer/Counter 0 and 1 Control | | |

Table 6. Serial I/O Port SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|--------------------|----------|-------------------|
| SCON | Serial Control | SADDR | Slave Address |
| SBUF | Serial Data Buffer | BRL | Baud Rate Reload |
| SADEN | Slave Address Mask | BDRCON | Baud Rate Control |

Table 7. SSLC SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|----------------------------|----------|---------------------------------------|
| SSCON | Synchronous Serial control | SSCS | Synchronous Serial Control and Status |
| SSDAT | Synchronous Serial Data | SSBR | Synchronous Serial Bit Rate |

Table 8. Event Waveform Control SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|---|----------|--|
| CCON | EWC-PCA Timer/Counter Control | CCAP1L | EWC-PCA Compare Capture Module 1 Low Register |
| CMOD | EWC-PCA Timer/Counter Mode | CCAP2L | EWC-PCA Compare Capture Module 2 Low Register |
| CL | EWC-PCA Timer/Counter Low Register | CCAP3L | EWC-PCA Compare Capture Module 3 Low Register |
| CH | EWC-PCA Timer/Counter High Register | CCAP4L | EWC-PCA Compare Capture Module 4 Low Register |
| CCAPM0 | EWC-PCA Timer/Counter Mode 0 | CCAP0H | EWC-PCA Compare Capture Module 0 High Register |
| CCAPM1 | EWC-PCA Timer/Counter Mode 1 | CCAP1H | EWC-PCA Compare Capture Module 1 High Register |
| CCAPM2 | EWC-PCA Timer/Counter Mode 2 | CCAP2H | EWC-PCA Compare Capture Module 2 High Register |
| CCAPM3 | EWC-PCA Timer/Counter Mode 3 | CCAP3H | EWC-PCA Compare Capture Module 3 High Register |
| CCAPM4 | EWC-PCA Timer/Counter Mode 4 | CCAP4H | EWC-PCA Compare Capture Module 4 High Register |
| CCAP0L | EWC-PCA Compare Capture Module 0 Low Register | | |

Table 9. System Management SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|------------------|----------|--------------|
| PCON | Power Control | PFILT | Power Filter |
| POWM | Power Management | CKRL | Clock Reload |

Table 10. Interrupt SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|-----------------------------------|----------|-----------------------------------|
| IE0 | Interrupt Enable Control 0 | IPL0 | Interrupt Priority Control Low 0 |
| IE1 | Interrupt Priority Control 1 | IPH1 | Interrupt Priority Control High 1 |
| IPH0 | Interrupt Priority Control High 0 | IPL1 | Interrupt Priority Control Low 1 |

Table 11. Keyboard Interface SFRs

| Mnemonic | Name | Mnemonic | Name |
|----------|-------------------------------|----------|------------------------|
| P1IE | Port 1 Input Interrupt Enable | P1LS | Port 1 Level Selection |
| PIF | Port 1 Flag | | |

Table 12. SFR Addresses and Reset Values

| | 0/8 | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | 7/F | |
|-----|---------------------------------|----------------------------------|---------------------------------|---------------------------------|----------------------------------|---------------------|---------------------------------|-------------------|-----|
| F8h | | CH 0000 0000 | CCAP0H 0000 0000 | CCAP1H 0000 0000 | CCAP2H 0000 0000 | CCAP3H 0000 0000 | CCAP4H 0000 0000 | | FFh |
| F0h | B ⁽¹⁾ 0000 0000 | | | | | | | | F7h |
| E8h | | CL 0000 0000 | CCAP0L 0000 0000 | CCAP1L 0000 0000 | CCAP2L 0000 0000 | CCAP3L 0000 0000 | CCAP4L 0000 0000 | | EFh |
| E0h | ACC ⁽¹⁾ 0000 0000 | | | | | | | | E7h |
| D8h | CCON 00X0 0000 | CMOD 00XX X000 | CCAPM0 X000 0000 | CCAPM1 X000 0000 | CCAPM2 X000 0000 | CCAPM3 X000 0000 | CCAPM4 X000 0000 | | DFh |
| D0h | PSW ⁽¹⁾ 0000 0000 | PSW1 ⁽¹⁾ 0000 0000 | | | | | | | D7h |
| C8h | T2CON 0000 0000 | T2MOD XXXX XX00 | RCAP2L 0000 0000 | RCAP2H 0000 0000 | TL2 0000 0000 | TH2 0000 0000 | | | CFh |
| C0h | | | | | | | | | C7h |
| B8h | IPL0 X000 0000 | SADEN 0000 0000 | | | | | SPH ⁽¹⁾ 0000 0000 | | BFh |
| B0h | P3 1111 1111 | IE1 XX0X XXX0 | IPL1 XX0X XXX0 | IPH1 XX0X XXX0 | | | | IPH0 X000 0000 | B7h |
| A8h | IE0 0000 0000 | SADDR 0000 0000 | | | | | | | AFh |
| A0h | P2 1111 1111 | | | | | | WDTRST 1111 1111 | | A7h |
| 98h | SCON 0000 0000 | SBUF XXXX XXXX | BRL 0000 0000 | BDRCON XXX0 0000 | P1LS 0000 0000 | P1IE 0000 0000 | PIF 0000 0000 | | 9Fh |
| 90h | P1 1111 1111 | | SSBR 0000 0000 | SSCON 0000 0000 | SSCS (2) | SSDAT 0000 0000 | | | 97h |
| 88h | TCON 0000 0000 | TMOD 0000 0000 | TL0 0000 0000 | TL1 0000 0000 | TH0 0000 0000 | TH1 0000 0000 | CKRL 0000 1000 | POWM 0XXX 0XXX | 8Fh |
| 80h | P0 1111 1111 | SP 0000 0111 | DPL ⁽¹⁾ 0000 0000 | DPH ⁽¹⁾ 0000 0000 | DPXL ⁽¹⁾ 0000 0001 | | PFILT XXXX XXXX | PCON 0000 0000 | 87h |
| | 0/8 | 1/9 | 2/A | 3/B | 4/C | 5/D | 6/E | 7/F | |

reserved

Notes:

1. These registers are described in the TSC80251 Programmer's Guide (C251 core registers).
2. In read and write modes, SSCS is splitted in two separate registers. SSCS reset value is 1111 1000 in read mode and 0000 0000 in write mode.

6.4. Configuration Bytes

The TSC87251G1A derivatives provide user design flexibility by configuring certain operating features at device reset. These features fall into the following categories:

- external memory interface (page mode, address bits, programmed wait states and the address range for RD#, WR#, and PSEN#)
- source mode/binary mode opcodes
- selection of bytes stored on the stack by an interrupt
- mapping of the upper portion of on-chip code memory to region 00:

Two user configuration bytes CONFIG0 (see Figure 6) and CONFIG1 (see Figure 7) provide the information.

For TSC87251G1A devices, configuration information is stored in on-chip separate memory (see paragraph 8. “EPROM Programming”). Whatever the EA# level, the configuration information is retrieved from this on-chip memory.

CONFIG0

Configuration Byte 0

| | | | | | | | |
|---|---|-----|-------|-----|-----|-------|-----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | WSA | XALE# | RD1 | RD0 | PAGE# | SRC |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|---|
| 7 | – | Reserved Set this bit when writing to CONFIG0. |
| 6 | – | Reserved Set this bit when writing to CONFIG0. |
| 5 | WSA | Wait State A bits Clear to generate one wait state for all memory region except 01:. Set for no wait states for all memory region except 01:. |
| 4 | XALE# | Extend ALE bit Clear to extend the duration of the ALE pulse from T_{OSC} to $3 \times T_{OSC}$. Set to minimize the duration of the ALE pulse to $1 \times T_{OSC}$. |
| 3 | RD1 | Memory Signal Select bits Specify a 18-bit, 17-bit or 16-bit external address bus and the usage of RD#, WR# and PSEN# signals (see Table 13). |
| 2 | RD0 | |
| 1 | PAGE# | Page Mode Select bit Clear to select the faster page mode with A15:8/D7:0 on Port 2 and A7:0 on Port 0. Set to select the non-page mode ⁽¹⁾ with A15:8 on Port 2 and A7:0/D7:0 on Port 0. |
| 0 | SRC | Source Mode/Binary Mode Select bit Clear to select the binary mode. Set to select the source mode. |

Note:

1. This selection provides compatibility with the standard 80C51 hardware which is multiplexing the address LSB and the data on Port 0.

Figure 6. Configuration Byte 0

CONFIG1

Configuration Byte 1

| | | | | | | | |
|---|---|---|------|-----|---|---|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | INTR | WSB | - | - | EMAP# |

| Bit Number | Bit Mnemonic | Description |
|------------|--------------|--|
| 7 | - | Reserved Set this bit when writing to CONFIG1. |
| 6 | - | Reserved Set this bit when writing to CONFIG1. |
| 5 | - | Reserved Set this bit when writing to CONFIG1. |
| 4 | INTR | Interrupt Mode bit⁽¹⁾ Clear so that the interrupts push two bytes onto the stack (the two lower bytes of the PC register). Set so that the interrupts push four bytes onto the stack (the three bytes of the PC register and the PSW1 register). |
| 3 | WSB | Wait State B bit Clear to generate one wait state for memory region 01:. Set for no wait states for memory region 01:. |
| 2 | - | Reserved Set this bit when writing to CONFIG1. |
| 1 | - | Reserved Set this bit when writing to CONFIG1. |
| 0 | EMAP# | On-Chip Code Memory Map bit Clear to map the upper 8 Kbytes of on-chip code memory (at FF:2000h–FF:3FFFh) to the data space (at 00:E000h–00:FFFFh). Set not to map the upper 8 Kbytes of on-chip code memory (at FF:2000h–FF:3FFFh) to the data space. |

Note:

- Two or four bytes are transparently popped according to INTR when using the RETI instruction. INTR must be set if interrupts are used with code executing outside region FF:.

Figure 7. Configuration Byte 1

Table 13. Address Ranges and Usage of RD#, WR# and PSEN# Signals

| RD1 | RD0 | P1.7 | P3.7/RD# | PSEN# | WR# | External Memory |
|-----|-----|---------|-------------------------------------|---|--|------------------------------|
| 0 | 0 | A17 | A16 | Read signal for all external memory locations | Write signal for all external memory locations | 256 Kbytes |
| 0 | 1 | I/O pin | A16 | Read signal for all external memory locations | Write signal for all external memory locations | 128 Kbytes |
| 1 | 0 | I/O pin | I/O pin | Read signal for all external memory locations | Write signal for all external memory locations | 64 Kbytes |
| 1 | 1 | I/O pin | Read signal for regions 00: and 01: | Read signal for regions FE: and FF: | Write signal for all external memory locations | 2 × 64 Kbytes ⁽¹⁾ |

Note:

- This selection provides compatibility with the standard 80C51 hardware which has separate external memory spaces for data and code.

7. Instruction Set Summary

This section contains tables that summarize the instruction set. For each instruction there is a short description, its length in bytes, and its execution time in states (one state time is equal to two system clock cycles). There are two concurrent processes limiting the effective instruction throughput:

- Instruction Fetch
- Instruction Execution

Table 20 to Table 34 assume code executing from on-chip memory, then the CPU is fetching 16-bit at a time and this is never limiting the execution speed.

If the code is fetched from external memory, a pre-fetch queue will store instructions ahead of execution to optimize the memory bandwidth usage when slower instructions are executed. However, the effective speed may be limited depending on the average size of instructions (for the considered section of the program flow). The maximum average instruction throughput is provided by Table 14 depending on the external memory configuration (from Page Mode to Non-Page Mode and the maximum number of wait states). If the average size of instructions is not an integer, the maximum effective throughput is found by pondering the number of states for the neighbor integer values.

Table 14. Minimum Number of States per Instruction for given Average Sizes

| Average size of Instructions (bytes) | Page Mode (states) | Non-Page Mode (states) | | |
|--------------------------------------|--------------------|------------------------|--------------|---------------|
| | | 0 Wait State | 1 Wait State | 2 Wait States |
| 1 | 1 | 2 | 3 | 4 |
| 2 | 2 | 4 | 6 | 8 |
| 3 | 3 | 6 | 9 | 12 |
| 4 | 4 | 8 | 12 | 16 |
| 5 | 5 | 10 | 15 | 20 |

If the average execution time of the considered instructions is larger than the number of states given by Table 14, this larger value will prevail as the limiting factor. Otherwise, the value from Table 14 must be taken. This is providing a fair estimation of the execution speed but only the actual code execution can provide the final value.

7.1. Notation for Instruction Operands

Table 15 to Table 19 provide Notation for Instruction Operands.

Table 15. Notation for Direct Addressing

| Direct Address | Description | C251 | C51 |
|----------------|--|------|-----|
| dir8 | A direct 8-bit address. This can be a memory address (00h-7Fh) or a SFR address (80h-FFh). It is a byte (default), word or double word depending on the other operand. | ✓ | ✓ |
| dir16 | A 16-bit memory address (00:0000h-00:FFFFh) used in direct addressing. | ✓ | |

Table 16. Notation for Immediate Addressing

| Immediate Address | Description | C251 | C51 |
|----------------------|---|------|-----|
| #data | An 8-bit constant that is immediately addressed in an instruction | ✓ | ✓ |
| #data16 | A 16-bit constant that is immediately addressed in an instruction | ✓ | |
| #0data16 #1data16 | A 32-bit constant that is immediately addressed in an instruction. The upper word is filled with zeros (#0data16) or ones (#1data16). | ✓ | |
| #short | A constant, equal to 1, 2, or 4, that is immediately addressed in an instruction. | ✓ | |

Table 17. Notation for Bit Addressing

| Direct Address | Description | C251 | C51 |
|----------------|---|------|-----|
| bit51 | A directly addressed bit (bit number= 00h-FFh) in memory or an SFR. Bits 00h-7Fh are the 128 bits in byte locations 20h-2Fh in the on-chip RAM. Bits 80h-FFh are the 128 bits in the 16 SFRs with addresses that end in 0h or 8h, S:80h, S:88h, S:90h, ..., S:F0h, S:F8h. | | ✓ |
| bit | A directly addressed bit in memory locations 00:0020h-00:007Fh or in any defined SFR. | ✓ | |

Table 18. Notation for Destination in Control Instructions

| Direct Address | Description | C251 | C51 |
|----------------|--|------|-----|
| rel | A signed (two's complement) 8-bit relative address. The destination is -128 to +127 bytes relative to the next instruction's first byte. | ✓ | ✓ |
| addr11 | An 11-bit target address. The target is in the same 2-Kbyte block of memory as the next instruction's first byte. | | ✓ |
| addr16 | A 16-bit target address. The target can be anywhere within the same 64-Kbyte region as the next instruction's first byte. | | ✓ |
| addr24 | A 24-bit target address. The target can be anywhere within the 16-Mbyte address space. | ✓ | |

Table 19. Notation for Register Operands

| Register | Description | C251 | C51 |
|---|---|------|-----|
| @Ri | A memory location (00h-FFh) addressed indirectly via byte registers R0 or R1 | | ✓ |
| Rn n | Byte register R0-R7 of the currently selected register bank Byte register index: n= 0-7 | | ✓ |
| Rm Rmd Rms m, md, ms | Byte register R0-R15 of the currently selected register file Destination register Source register Byte register index: m, md, ms= 0-15 | ✓ | |
| WRj WRjd WRjs @WRj @WRj +dis16 j, jd, js | Word register WR0, WR2, ..., WR30 of the currently selected register file Destination register Source register A memory location (00:0000h-00:FFFFh) addressed indirectly through word register WR0-WR30, is the target address for jump instructions. A memory location (00:0000h-00:FFFFh) addressed indirectly through word register (WR0-WR30) + 16-bit signed (two's complement) displacement value Word register index: j, jd, js= 0-30 | ✓ | |
| DRk DRkd DRks @DRk @DRk +dis16 k, kd, ks | Dword register DR0, DR4, ..., DR28, DR56, DR60 of the currently selected register file Destination register Source register A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register DR0-DR28, DR56 and DR60, is the target address for jump instruction A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register (DR0-DR28, DR56, DR60) + 16-bit (two's complement) signed displacement value Dword register index: k, kd, ks= 0, 4, 8..., 28, 56, 60 | ✓ | |

7.2. Size and Execution Time for Instruction Families

Table 20. Summary of Add and Subtract Instructions

| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
|----------------------|------------------------------|--|-------------|------------------|----------------------------------|------------------|
| | | | Bytes | States | Bytes | States |
| Add | | ADD <dest>, <src> | | | dest opnd ← dest opnd + src opnd | |
| Subtract | | SUB <dest>, <src> | | | dest opnd ← dest opnd – src opnd | |
| Add with Carry | | ADDC <dest>, <src> | | | (A) ← (A) + src opnd + (CY) | |
| Subtract with Borrow | | SUBB <dest>, <src> | | | (A) ← (A) – src opnd – (CY) | |
| ADD | A, Rn | Register to ACC | 1 | 1 | 2 | 2 |
| | A, dir8 | Direct address to ACC | 2 | 1 ⁽²⁾ | 2 | 1 ⁽²⁾ |
| | A, @Ri | Indirect address to ACC | 1 | 2 | 2 | 3 |
| | A, #data | Immediate data to ACC | 2 | 1 | 2 | 1 |
| ADD / SUB | Rmd, Rms | Byte register to/from byte register | 3 | 2 | 2 | 1 |
| | WRjd, WRjs | Word register to/from word register | 3 | 3 | 2 | 2 |
| | DRkd, DRks | Dword register to/from dword register | 3 | 5 | 2 | 4 |
| | Rm, #data | Immediate 8-bit data to/from byte register | 4 | 3 | 3 | 2 |
| | WRj, #data16 | Immediate 16-bit data to/from word register | 5 | 4 | 4 | 3 |
| | DRk, #0data16 | 16-bit unsigned immediate data to/from dword register | 5 | 6 | 4 | 5 |
| | Rm, dir8 | Direct address (on-chip RAM or SFR) to/from byte register | 4 | 3 ⁽²⁾ | 3 | 2 ⁽²⁾ |
| | WRj, dir8 | Direct address (on-chip RAM or SFR) to/from word register | 4 | 4 | 3 | 3 |
| | Rm, dir16 | Direct address (64K) to/from byte register | 5 | 3 ⁽³⁾ | 4 | 2 ⁽³⁾ |
| | WRj, dir16 | Direct address (64K) to/from word register | 5 | 4 ⁽⁴⁾ | 4 | 3 ⁽⁴⁾ |
| | Rm, @WRj | Indirect address (64K) to/from byte register | 4 | 3 ⁽³⁾ | 3 | 2 ⁽³⁾ |
| | Rm, @DRk | Indirect address (16M) to/from byte register | 4 | 4 ⁽³⁾ | 3 | 3 ⁽³⁾ |
| ADDC / SUBB | A, Rn | Register to/from ACC with carry | 1 | 1 | 2 | 2 |
| | A, dir8 | Direct address (on-chip RAM or SFR) to/from ACC with carry | 2 | 1 ⁽²⁾ | 2 | 1 ⁽²⁾ |
| | A, @Ri | Indirect address to/from ACC with carry | 1 | 2 | 2 | 3 |
| | A, #data | Immediate data to/from ACC with carry | 2 | 1 | 2 | 1 |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
4. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 21. Summary of Increment and Decrement Instructions

| Increment | | INC <dest> | dest opnd ← dest opnd + 1 | | | |
|------------|------------------------------|--|----------------------------------|------------------|-------------|------------------|
| Increment | | INC <dest>, <src> | dest opnd ← dest opnd + src opnd | | | |
| Decrement | | DEC <dest> | dest opnd ← dest opnd – 1 | | | |
| Decrement | | DEC <dest>, <src> | dest opnd ← dest opnd – src opnd | | | |
| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
| | | | Bytes | States | Bytes | States |
| INC DEC | A | ACC by 1 | 1 | 1 | 1 | 1 |
| | Rn | Register by 1 | 1 | 1 | 2 | 2 |
| | dir8 | Direct address (on-chip RAM or SFR) by 1 | 2 | 2 ⁽²⁾ | 2 | 2 ⁽²⁾ |
| | @Ri | Indirect address by 1 | 1 | 3 | 2 | 4 |
| INC DEC | Rm, #short | Byte register by 1, 2, or 4 | 3 | 2 | 2 | 1 |
| | WRj, #short | Word register by 1, 2, or 4 | 3 | 2 | 2 | 1 |
| INC | DRk, #short | Double word register by 1, 2, or 4 | 3 | 4 | 2 | 3 |
| DEC | DRk, #short | Double word register by 1, 2, or 4 | 3 | 5 | 2 | 4 |
| INC | DPTR | Data pointer by 1 | 1 | 1 | 1 | 1 |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x= 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 22. Summary of Compare Instructions

| Compare | | CMP <dest>, <src> | dest opnd – src opnd | | | |
|----------|------------------------------|---|----------------------|------------------|-------------|------------------|
| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
| | | | Bytes | States | Bytes | States |
| CMP | Rmd, Rms | Register with register | 3 | 2 | 2 | 1 |
| | WRjd, WRjs | Word register with word register | 3 | 3 | 2 | 2 |
| | DRkd, DRks | Dword register with dword register | 3 | 5 | 2 | 4 |
| | Rm, #data | Register with immediate data | 4 | 3 | 3 | 2 |
| | WRj, #data16 | Word register with immediate 16-bit data | 5 | 4 | 4 | 3 |
| | DRk, #0data16 | Dword register with zero-extended 16-bit immediate data | 5 | 6 | 4 | 5 |
| | DRk, #1data16 | Dword register with one-extended 16-bit immediate data | 5 | 6 | 4 | 5 |
| | Rm, dir8 | Direct address (on-chip RAM or SFR) with byte register | 4 | 3 ⁽¹⁾ | 3 | 2 ⁽¹⁾ |
| | WRj, dir8 | Direct address (on-chip RAM or SFR) with word register | 4 | 4 | 3 | 3 |
| | Rm, dir16 | Direct address (64K) with byte register | 5 | 3 ⁽²⁾ | 4 | 2 ⁽²⁾ |
| | WRj, dir16 | Direct address (64K) with word register | 5 | 4 ⁽³⁾ | 4 | 3 ⁽³⁾ |
| | Rm, @WRj | Indirect address (64K) with byte register | 4 | 3 ⁽²⁾ | 3 | 2 ⁽²⁾ |
| | Rm, @DRk | Indirect address (16M) with byte register | 4 | 4 ⁽²⁾ | 3 | 3 ⁽²⁾ |

Notes:

1. If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
2. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
3. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 23. Summary of Logical Instructions (1/2)

| Logical AND ⁽¹⁾ | ANL <dest>, <src> | dest opnd ← dest opnd ∧ src opnd | | | | |
|-------------------------------------|------------------------------|---|-------------|------------------|-------------|------------------|
| Logical OR ⁽¹⁾ | ORL <dest>, <src> | dest opnd ← dest opnd ∨ src opnd | | | | |
| Logical Exclusive OR ⁽¹⁾ | XRL <dest>, <src> | dest opnd ← dest opnd ⊕ src opnd | | | | |
| Clear ⁽¹⁾ | CLR A | (A) ← 0 | | | | |
| Complement ⁽¹⁾ | CPL A | (A) ← \bar{A} | | | | |
| Rotate Left | RL A | (A) _{n+1} ← (A) _n , n= 0..6 (A) ₀ ← (A) ₇ | | | | |
| Rotate Left Carry | RLC A | (A) _{n+1} ← (A) _n , n= 0..6 (CY) ← (A) ₇ (A) ₀ ← (CY) | | | | |
| Rotate Right | RR A | (A) _{n-1} ← (A) _n , n= 7..1 (A) ₇ ← (A) ₀ | | | | |
| Rotate Right Carry | RRC A | (A) _{n-1} ← (A) _n , n= 7..1 (CY) ← (A) ₀ (A) ₇ ← (CY) | | | | |
| Mnemonic | <dest>, <src> ⁽²⁾ | Comments | Binary Mode | | Source Mode | |
| | | | Bytes | States | Bytes | States |
| ANL ORL XRL | A, Rn | register to ACC | 1 | 1 | 2 | 2 |
| | A, dir8 | Direct address (on-chip RAM or SFR) to ACC | 2 | 1 ⁽³⁾ | 2 | 1 ⁽³⁾ |
| | A, @Ri | Indirect address to ACC | 1 | 2 | 2 | 3 |
| | A, #data | Immediate data to ACC | 2 | 1 | 2 | 1 |
| | dir8, A | ACC to direct address | 2 | 2 ⁽⁴⁾ | 2 | 2 ⁽⁴⁾ |
| | dir8, #data | Immediate 8-bit data to direct address | 3 | 3 ⁽⁴⁾ | 3 | 3 ⁽⁴⁾ |
| | Rmd, Rms | Byte register to byte register | 3 | 2 | 2 | 1 |
| | WRjd, WRjs | Word register to word register | 3 | 3 | 2 | 2 |
| | Rm, #data | Immediate 8-bit data to byte register | 4 | 3 | 3 | 2 |
| | WRj, #data16 | Immediate 16-bit data to word register | 5 | 4 | 4 | 3 |
| | Rm, dir8 | Direct address to byte register | 4 | 3 ⁽³⁾ | 3 | 2 ⁽³⁾ |
| | WRj, dir8 | Direct address to word register | 4 | 4 | 3 | 3 |
| | Rm, dir16 | Direct address (64K) to byte register | 5 | 3 ⁽⁵⁾ | 4 | 2 ⁽⁵⁾ |
| | WRj, dir16 | Direct address (64K) to word register | 5 | 4 ⁽⁶⁾ | 4 | 3 ⁽⁶⁾ |
| | Rm, @WRj | Indirect address (64K) to byte register | 4 | 3 ⁽⁵⁾ | 3 | 2 ⁽⁵⁾ |
| | Rm, @DRk | Indirect address (16M) to byte register | 4 | 4 ⁽⁵⁾ | 3 | 3 ⁽⁵⁾ |
| CLR | A | Clear ACC | 1 | 1 | 1 | 1 |
| CPL | A | Complement ACC | 1 | 1 | 1 | 1 |
| RL | A | Rotate ACC left | 1 | 1 | 1 | 1 |
| RLC | A | Rotate ACC left through CY | 1 | 1 | 1 | 1 |
| RR | A | Rotate ACC right | 1 | 1 | 1 | 1 |
| RRC | A | Rotate ACC right through CY | 1 | 1 | 1 | 1 |

Notes:

- Logical instructions that affect a bit are in Table 29.
- A shaded cell denotes an instruction in the C51 Architecture.
- If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
- If this instruction addresses an I/O Port (Px, x= 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.
- If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
- If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 24. Summary of Logical Instructions (2/2)

| | | |
|------------------------|------------|---|
| Shift Left Logical | SLL <dest> | <dest> ₀ ← 0 <dest> _{n+1} ← <dest> _n , n = 0..msb-1 (CY) ← <dest> _{msb} |
| Shift Right Arithmetic | SRA <dest> | <dest> _{msb} ← <dest> _{msb} <dest> _{n-1} ← <dest> _n , n = msb..1 (CY) ← <dest> ₀ |
| Shift Right Logical | SRL <dest> | <dest> _{msb} ← 0 <dest> _{n-1} ← <dest> _n , n = msb..1 (CY) ← <dest> ₀ |
| Swap | SWAP A | A _{3:0} ↔ A _{7:4} |

| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
|----------|------------------------------|--|-------------|--------|-------------|--------|
| | | | Bytes | States | Bytes | States |
| SLL | Rm | Shift byte register left through the MSB | 3 | 2 | 2 | 1 |
| | WRj | Shift word register left through the MSB | 3 | 2 | 2 | 1 |
| SRA | Rm | Shift byte register right | 3 | 2 | 2 | 1 |
| | WRj | Shift word register right | 3 | 2 | 2 | 1 |
| SRL | Rm | Shift byte register left | 3 | 2 | 2 | 1 |
| | WRj | Shift word register left | 3 | 2 | 2 | 1 |
| SWAP | A | Swap nibbles within ACC | 1 | 2 | 1 | 2 |

Note:

1. A shaded cell denotes an instruction in the C51 Architecture.

Table 25. Summary of Multiply, Divide and Decimal-adjust Instructions

| | | |
|---------------------------------------|-----------------------------|---|
| Multiply | MUL AB MUL <dest>, <src> | (B:A) ← (A)×(B) extended dest opnd ← dest opnd × src opnd |
| Divide | DIV AB | (A) ← Quotient ((A)/(B)) (B) ← Remainder ((A)/(B)) |
| Divide | DIV <dest>, <src> | ext. dest opnd high ← Quotient (dest opnd/src opnd) ext. dest opnd low ← Remainder (dest opnd/src opnd) |
| Decimal-adjust ACC for Addition (BCD) | DA A | IF [[(A) _{3:0} > 9] ∨ [(AC)= 1]] THEN (A) _{3:0} ← (A) _{3:0} + 6 !affects CY; IF [[(A) _{7:4} > 9] ∨ [(CY)= 1]] THEN (A) _{7:4} ← (A) _{7:4} + 6 |

| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
|----------|------------------------------|--|-------------|--------|-------------|--------|
| | | | Bytes | States | Bytes | States |
| MUL | AB | Multiply A and B | 1 | 5 | 1 | 5 |
| | Rmd, Rms | Multiply byte register and byte register | 3 | 6 | 2 | 5 |
| | WRjd, WRjs | Multiply word register and word register | 3 | 12 | 2 | 11 |
| DIV | AB | Divide A and B | 1 | 10 | 1 | 10 |
| | Rmd, Rms | Divide byte register and byte register | 3 | 11 | 2 | 10 |
| | WRjd, WRjs | Divide word register and word register | 3 | 21 | 2 | 20 |
| DA | A | Decimal adjust ACC | 1 | 1 | 1 | 1 |

Note:

1. A shaded cell denotes an instruction in the C51 Architecture.

Table 26. Summary of Move Instructions (1/3)

| | | |
|--------------------------|--------------------|---------------------------------------|
| Move to High word | MOVH <dest>, <src> | dest opnd _{31:16} ← src opnd |
| Move with Sign extension | MOVS <dest>, <src> | dest opnd ← src opnd with sign extend |
| Move with Zero extension | MOVZ <dest>, <src> | dest opnd ← src opnd with zero extend |
| Move Code | MOVC A, <src> | (A) ← src opnd |
| Move eXtended | MOVX <dest>, <src> | dest opnd ← src opnd |

| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
|----------|------------------------------|---|-------------|------------------|-------------|------------------|
| | | | Bytes | States | Bytes | States |
| MOVH | DRk, #data16 | 16-bit immediate data into upper word of dword register | 5 | 3 | 4 | 2 |
| MOVS | WRj, Rm | Byte register to word register with sign extension | 3 | 2 | 2 | 1 |
| MOVZ | WRj, Rm | Byte register to word register with zeros extension | 3 | 2 | 2 | 1 |
| MOVC | A, @A +DPTR | Code byte relative to DPTR to ACC | 1 | 6 ⁽³⁾ | 1 | 6 ⁽³⁾ |
| | A, @A +PC | Code byte relative to PC to ACC | 1 | 6 ⁽³⁾ | 1 | 6 ⁽³⁾ |
| MOVX | A, @Ri | Extended memory (8-bit address) to ACC ⁽²⁾ | 1 | 4 | 1 | 5 |
| | A, @DPTR | Extended memory (16-bit address) to ACC ⁽²⁾ | 1 | 3 ⁽⁴⁾ | 1 | 3 ⁽⁴⁾ |
| | @Ri, A | ACC to extended memory (8-bit address) ⁽²⁾ | 1 | 4 | 1 | 4 |
| | @DPTR, A | ACC to extended memory (16-bit address) ⁽²⁾ | 1 | 4 ⁽³⁾ | 1 | 4 ⁽³⁾ |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. Extended memory addressed is in the region specified by DPXL (reset value= 01h).
3. If this instruction addresses external memory location, add N+1 to the number of states (N: number of wait states).
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).

Table 27. Summary of Move Instructions (2/3)

| | | |
|---------------------|-------------------|----------------------|
| Move ⁽¹⁾ | MOV <dest>, <src> | dest opnd ← src opnd |
|---------------------|-------------------|----------------------|

| Mnemonic | <dest>, <src> ⁽²⁾ | Comments | Binary Mode | | Source Mode | |
|---------------|--|---|-------------|------------------|-------------|------------------|
| | | | Bytes | States | Bytes | States |
| MOV | A, Rn | Register to ACC | 1 | 1 | 2 | 2 |
| | A, dir8 | Direct address (on-chip RAM or SFR) to ACC | 2 | 1 ⁽³⁾ | 2 | 1 ⁽³⁾ |
| | A, @Ri | Indirect address to ACC | 1 | 2 | 2 | 3 |
| | A, #data | Immediate data to ACC | 2 | 1 | 2 | 1 |
| | Rn, A | ACC to register | 1 | 1 | 2 | 2 |
| | Rn, dir8 | Direct address (on-chip RAM or SFR) to register | 2 | 1 ⁽³⁾ | 3 | 2 ⁽³⁾ |
| | Rn, #data | Immediate data to register | 2 | 1 | 3 | 2 |
| | dir8, A | ACC to direct address | 2 | 2 ⁽³⁾ | 2 | 2 ⁽³⁾ |
| | dir8, Rn | Register to direct address | 2 | 2 ⁽³⁾ | 3 | 3 ⁽³⁾ |
| | dir8, dir8 | Direct address to direct address | 3 | 3 ⁽⁴⁾ | 3 | 3 ⁽⁴⁾ |
| | dir8, @Ri | Indirect address to direct address | 2 | 3 ⁽³⁾ | 3 | 4 ⁽³⁾ |
| | dir8, #data | Immediate data to direct address | 3 | 3 ⁽³⁾ | 3 | 3 ⁽³⁾ |
| | @Ri, A | ACC to indirect address | 1 | 3 | 2 | 4 |
| | @Ri, dir8 | Direct address to indirect address | 2 | 3 ⁽³⁾ | 3 | 4 ⁽³⁾ |
| | @Ri, #data | Immediate data to indirect address | 2 | 3 | 3 | 4 |
| DPTR, #data16 | Load Data Pointer with a 16-bit constant | 3 | 2 | 3 | 2 | |

Notes:

1. Instructions that move bits are in Table 29.
2. Move instructions from the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. Apply note 3 for each dir8 operand.

Table 28. Summary of Move Instructions (3/3)

| Move ⁽¹⁾ MOV <dest>, <src> dest opnd ← src opnd | | | | | | |
|--|---|---|------------------|------------------|------------------|------------------|
| Mnemonic | <dest>, <src> ⁽²⁾ | Comments | Binary Mode | | Source Mode | |
| | | | Bytes | States | Bytes | States |
| MOV | Rmd, Rms | Byte register to byte register | 3 | 2 | 2 | 1 |
| | WRjd, WRjs | Word register to word register | 3 | 2 | 2 | 1 |
| | DRkd, DRks | Dword register to dword register | 3 | 3 | 2 | 2 |
| | Rm, #data | Immediate 8-bit data to byte register | 4 | 3 | 3 | 2 |
| | WRj, #data16 | Immediate 16-bit data to word register | 5 | 3 | 4 | 2 |
| | DRk, #0data16 | zero-ext 16bit immediate data to dword register | 5 | 5 | 4 | 4 |
| | DRk, #1data16 | one-ext 16bit immediate data to dword register | 5 | 5 | 4 | 4 |
| | Rm, dir8 | Direct address to byte register | 4 | 3 ⁽³⁾ | 3 | 2 ⁽³⁾ |
| | WRj, dir8 | Direct address to word register | 4 | 4 | 3 | 3 |
| | DRk, dir8 | Direct address to dword register | 4 | 6 | 3 | 5 |
| | Rm, dir16 | Direct address (64K) to byte register | 5 | 3 ⁽⁴⁾ | 4 | 2 ⁽⁴⁾ |
| | WRj, dir16 | Direct address (64K) to word register | 5 | 4 ⁽⁵⁾ | 4 | 3 ⁽⁵⁾ |
| | DRk, dir16 | Direct address (64K) to dword register | 5 | 6 ⁽⁶⁾ | 4 | 5 ⁽⁶⁾ |
| | Rm, @WRj | Indirect address (64K) to byte register | 4 | 3 ⁽⁴⁾ | 3 | 2 ⁽⁴⁾ |
| | Rm, @DRk | Indirect address (16M) to byte register | 4 | 4 ⁽⁴⁾ | 3 | 3 ⁽⁴⁾ |
| | WRjd, @WRjs | Indirect address (64K) to word register | 4 | 4 ⁽⁵⁾ | 3 | 3 ⁽⁵⁾ |
| | WRj, @DRk | Indirect address (16M) to word register | 4 | 5 ⁽⁵⁾ | 3 | 4 ⁽⁵⁾ |
| | dir8, Rm | Byte register to direct address | 4 | 4 ⁽³⁾ | 3 | 3 ⁽³⁾ |
| | dir8, WRj | Word register to direct address | 4 | 5 | 3 | 4 |
| | dir8, DRk | Dword register to direct address | 4 | 7 | 3 | 6 |
| | dir16, Rm | Byte register to direct address (64K) | 5 | 4 ⁽⁴⁾ | 4 | 3 ⁽⁴⁾ |
| | dir16, WRj | Word register to direct address (64K) | 5 | 5 ⁽⁵⁾ | 4 | 4 ⁽⁵⁾ |
| | dir16, DRk | Dword register to direct address (64K) | 5 | 7 ⁽⁶⁾ | 4 | 6 ⁽⁶⁾ |
| | @WRj, Rm | Byte register to indirect address (64K) | 4 | 4 ⁽⁴⁾ | 3 | 3 ⁽⁴⁾ |
| | @DRk, Rm | Byte register to indirect address (16M) | 4 | 5 ⁽⁴⁾ | 3 | 4 ⁽⁴⁾ |
| | @WRjd, WRjs | Word register to indirect address (64K) | 4 | 5 ⁽⁵⁾ | 3 | 4 ⁽⁵⁾ |
| | @DRk, WRj | Word register to indirect address (16M) | 4 | 6 ⁽⁵⁾ | 3 | 5 ⁽⁵⁾ |
| | Rm, @WRj +dis16 | Indirect with 16-bit dis (64K) to byte register | 5 | 6 ⁽⁴⁾ | 4 | 5 ⁽⁴⁾ |
| | WRj, @WRj +dis16 | Indirect with 16-bit dis (64K) to word register | 5 | 7 ⁽⁵⁾ | 4 | 6 ⁽⁵⁾ |
| | Rm, @DRk +dis24 | Indirect with 16-bit dis (16M) to byte register | 5 | 7 ⁽⁴⁾ | 4 | 6 ⁽⁴⁾ |
| | WRj, @WRj +dis24 | Indirect with 16-bit dis (16M) to word register | 5 | 8 ⁽⁵⁾ | 4 | 7 ⁽⁵⁾ |
| | @WRj +dis16, Rm | Byte register to indirect with 16-bit dis (64K) | 5 | 6 ⁽⁴⁾ | 4 | 5 ⁽⁴⁾ |
| @WRj +dis16, WRj | Word register to indirect with 16-bit dis (64K) | 5 | 7 ⁽⁵⁾ | 4 | 6 ⁽⁵⁾ | |
| @DRk +dis24, Rm | Byte register to indirect with 16-bit dis (16M) | 5 | 7 ⁽⁴⁾ | 4 | 6 ⁽⁴⁾ | |
| @DRk +dis24, WRj | Word register to indirect with 16-bit dis (16M) | 5 | 8 ⁽⁵⁾ | 4 | 7 ⁽⁵⁾ | |

Notes:

1. Instructions that move bits are in Table 29.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

Table 29. Summary of Bit Instructions

| | | |
|----------------------------------|----------------|---|
| Clear Bit | CLR <dest> | dest opnd ← 0 |
| Set Bit | SETB <dest> | dest opnd ← 1 |
| Complement Bit | CPL <dest> | dest opnd ← $\bar{\text{bit}}$ |
| AND Carry with Bit | ANL CY, <src> | $(\text{CY}) \leftarrow (\text{CY}) \wedge \text{src opnd}$ |
| AND Carry with Complement of Bit | ANL CY, /<src> | $(\text{CY}) \leftarrow (\text{CY}) \wedge \bar{\text{src opnd}}$ |
| OR Carry with Bit | ORL CY, <src> | $(\text{CY}) \leftarrow (\text{CY}) \vee \text{src opnd}$ |
| OR Carry with Complement of Bit | ORL CY, /<src> | $(\text{CY}) \leftarrow (\text{CY}) \vee \bar{\text{src opnd}}$ |
| Move Bit to Carry | MOV CY, <src> | $(\text{CY}) \leftarrow \text{src opnd}$ |
| Move Bit from Carry | MOV <dest>, CY | dest opnd ← (CY) |

| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
|----------|------------------------------|--------------------------------------|-------------|------------------|-------------|------------------|
| | | | Bytes | States | Bytes | States |
| CLR | CY | Clear carry | 1 | 1 | 1 | 1 |
| | bit51 | Clear direct bit | 2 | 2 ⁽³⁾ | 2 | 2 ⁽³⁾ |
| | bit | Clear direct bit | 4 | 4 ⁽³⁾ | 3 | 3 ⁽³⁾ |
| SETB | CY | Set carry | 1 | 1 | 1 | 1 |
| | bit51 | Set direct bit | 2 | 2 ⁽³⁾ | 2 | 2 ⁽³⁾ |
| | bit | Set direct bit | 4 | 4 ⁽³⁾ | 3 | 3 ⁽³⁾ |
| CPL | CY | Complement carry | 1 | 1 | 1 | 1 |
| | bit51 | Complement direct bit | 2 | 2 ⁽³⁾ | 2 | 2 ⁽³⁾ |
| | bit | Complement direct bit | 4 | 4 ⁽³⁾ | 3 | 3 ⁽³⁾ |
| ANL | CY, bit51 | And direct bit to carry | 2 | 1 ⁽²⁾ | 2 | 1 ⁽²⁾ |
| | CY, bit | And direct bit to carry | 4 | 3 ⁽²⁾ | 3 | 2 ⁽²⁾ |
| | CY, /bit51 | And complemented direct bit to carry | 2 | 1 ⁽²⁾ | 2 | 1 ⁽²⁾ |
| | CY, /bit | And complemented direct bit to carry | 4 | 3 ⁽²⁾ | 3 | 2 ⁽²⁾ |
| ORL | CY, bit51 | Or direct bit to carry | 2 | 1 ⁽²⁾ | 2 | 1 ⁽²⁾ |
| | CY, bit | Or direct bit to carry | 4 | 3 ⁽²⁾ | 3 | 2 ⁽²⁾ |
| | CY, /bit51 | Or complemented direct bit to carry | 2 | 1 ⁽²⁾ | 2 | 1 ⁽²⁾ |
| | CY, /bit | Or complemented direct bit to carry | 4 | 3 ⁽²⁾ | 3 | 2 ⁽²⁾ |
| MOV | CY, bit51 | Move direct bit to carry | 2 | 1 ⁽²⁾ | 2 | 1 ⁽²⁾ |
| | CY, bit | Move direct bit to carry | 4 | 3 ⁽²⁾ | 3 | 2 ⁽²⁾ |
| | bit51, CY | Move carry to direct bit | 2 | 2 ⁽³⁾ | 2 | 2 ⁽³⁾ |
| | bit, CY | Move carry to direct bit | 4 | 4 ⁽³⁾ | 3 | 3 ⁽³⁾ |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x= 0–3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x= 0–3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 30. Summary of Exchange, Push and Pop Instructions

| Exchange bytes | XCH A, <src> | (A) ↔ src opnd | | | | |
|----------------|------------------------------|--|-------------|------------------|-------------|------------------|
| Exchange Digit | XCHD A, <src> | (A) _{3:0} ↔ src opnd _{3:0} | | | | |
| Push | PUSH <src> | (SP) ← (SP) + 1; ((SP)) ← src opnd; (SP) ← (SP) + size (src opnd) - 1 | | | | |
| Pop | POP <dest> | (SP) ← (SP) - size (dest opnd) + 1; dest opnd ← ((SP)); (SP) ← (SP) - 1 | | | | |
| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
| | | | Bytes | States | Bytes | States |
| XCH | A, Rn | ACC and register | 1 | 3 | 2 | 4 |
| | A, dir8 | ACC and direct address (on-chip RAM or SFR) | 2 | 3 ⁽³⁾ | 2 | 3 ⁽³⁾ |
| | A, @Ri | ACC and indirect address | 1 | 4 | 2 | 5 |
| XCHD | A, @Ri | ACC low nibble and indirect address (256 bytes) | 1 | 4 | 2 | 5 |
| PUSH | dir8 | Push direct address onto stack | 2 | 2 ⁽²⁾ | 2 | 2 ⁽²⁾ |
| | #data | Push immediate data onto stack | 4 | 4 | 3 | 3 |
| | #data16 | Push 16-bit immediate data onto stack | 5 | 5 | 4 | 5 |
| | Rm | Push byte register onto stack | 3 | 4 | 2 | 3 |
| | WRj | Push word register onto stack | 3 | 5 | 2 | 4 |
| | DRk | Push double word register onto stack | 3 | 9 | 2 | 8 |
| POP | dir8 | Pop direct address (on-chip RAM or SFR) from stack | 2 | 3 ⁽²⁾ | 2 | 3 ⁽²⁾ |
| | Rm | Pop byte register from stack | 3 | 3 | 2 | 2 |
| | WRj | Pop word register from stack | 3 | 5 | 2 | 4 |
| | DRk | Pop double word register from stack | 3 | 9 | 2 | 8 |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x= 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 31. Summary of Conditional Jump Instructions (1/2)

| Jump conditional on status | Jcc rel | (PC) ← (PC) + size (instr); IF [cc] THEN (PC) ← (PC) + rel | | | | |
|----------------------------|------------------------------|---|----------------------------|--------------------|----------------------------|--------------------|
| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode ⁽²⁾ | | Source Mode ⁽²⁾ | |
| | | | Bytes | States | Bytes | States |
| JC | rel | Jump if carry | 2 | 1/4 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JNC | rel | Jump if not carry | 2 | 1/4 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JE | rel | Jump if equal | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JNE | rel | Jump if not equal | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JG | rel | Jump if greater than | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JLE | rel | Jump if less than, or equal | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JSL | rel | Jump if less than (signed) | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JSLE | rel | Jump if less than, or equal (signed) | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JSG | rel | Jump if greater than (signed) | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |
| JSGE | rel | Jump if greater than or equal (signed) | 3 | 2/5 ⁽³⁾ | 2 | 1/4 ⁽³⁾ |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.

Table 32. Summary of Conditional Jump Instructions (2/2)

| Jump if bit | JB <src>, rel | (PC) ← (PC) + size (instr); IF [src opnd= 1] THEN (PC) ← (PC) + rel | | | | |
|---------------------------------|------------------------------|--|----------------------------|------------------------|----------------------------|-----------------------|
| Jump if not bit | JNB <src>, rel | (PC) ← (PC) + size (instr); IF [src opnd= 0] THEN (PC) ← (PC) + rel | | | | |
| Jump if bit and clear | JBC <dest>, rel | (PC) ← (PC) + size (instr); IF [dest opnd= 1] THEN dest opnd ← 0 (PC) ← (PC) + rel | | | | |
| Jump if accumulator is zero | JZ rel | (PC) ← (PC) + size (instr); IF [(A)= 0] THEN (PC) ← (PC) + rel | | | | |
| Jump if accumulator is not zero | JNZ rel | (PC) ← (PC) + size (instr); IF [(A) ≠ 0] THEN (PC) ← (PC) + rel | | | | |
| Compare and jump if not equal | CJNE <src1>, <src2>, rel | (PC) ← (PC) + size (instr); IF [src opnd1 < src opnd2] THEN (CY) ← 1 IF [src opnd1 ≥ src opnd2] THEN (CY) ← 0 IF [src opnd1 ≠ src opnd2] THEN (PC) ← (PC) + rel | | | | |
| Decrement and jump if not zero | DJNZ <dest>, rel | (PC) ← (PC) + size (instr); dest opnd ← dest opnd -1; IF [∅ (Z)] THEN (PC) ← (PC) + rel | | | | |
| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode ⁽²⁾ | | Source Mode ⁽²⁾ | |
| | | | Bytes | States | Bytes | States |
| JB | bit51, rel | Jump if direct bit is set | 3 | 2/5 ⁽³⁾⁽⁶⁾ | 3 | 2/5 ⁽³⁾⁽⁶⁾ |
| | bit, rel | Jump if direct bit of 8-bit address location is set | 5 | 4/7 ⁽³⁾⁽⁶⁾ | 4 | 3/6 ⁽³⁾⁽⁶⁾ |
| JNB | bit51, rel | Jump if direct bit is not set | 3 | 2/5 ⁽³⁾⁽⁶⁾ | 3 | 2/5 ⁽³⁾⁽⁶⁾ |
| | bit, rel | Jump if direct bit of 8-bit address location is not set | 5 | 4/7 ⁽³⁾⁽⁶⁾ | 4 | 3/6 ⁽³⁾ |
| JBC | bit51, rel | Jump if direct bit is set & clear bit | 3 | 4/7 ⁽⁵⁾⁽⁶⁾ | 3 | 4/7 ⁽⁵⁾⁽⁶⁾ |
| | bit, rel | Jump if direct bit of 8-bit address location is set and clear | 5 | 7/10 ⁽⁵⁾⁽⁶⁾ | 4 | 6/9 ⁽⁵⁾⁽⁶⁾ |
| JZ | rel | Jump if ACC is zero | 2 | 2/5 ⁽⁶⁾ | 2 | 2/5 ⁽⁶⁾ |
| JNZ | rel | Jump if ACC is not zero | 2 | 2/5 ⁽⁶⁾ | 2 | 2/5 ⁽⁶⁾ |
| CJNE | A, dir8, rel | Compare direct address to ACC and jump if not equal | 3 | 2/5 ⁽³⁾⁽⁶⁾ | 3 | 2/5 ⁽³⁾⁽⁶⁾ |
| | A, #data, rel | Compare immediate to ACC and jump if not equal | 3 | 2/5 ⁽⁶⁾ | 3 | 2/5 ⁽⁶⁾ |
| | Rn, #data, rel | Compare immediate to register and jump if not equal | 3 | 2/5 ⁽⁶⁾ | 4 | 3/6 ⁽⁶⁾ |
| | @Ri, #data, rel | Compare immediate to indirect and jump if not equal | 3 | 3/6 ⁽⁶⁾ | 4 | 4/7 ⁽⁶⁾ |
| DJNZ | Rn, rel | Decrement register and jump if not zero | 2 | 2/5 ⁽⁶⁾ | 3 | 3/6 ⁽⁶⁾ |
| | dir8, rel | Decrement direct address and jump if not zero | 3 | 3/6 ⁽⁴⁾⁽⁶⁾ | 3 | 3/6 ⁽⁴⁾⁽⁶⁾ |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. If this instruction addresses an I/O Port (Px, x= 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x= 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.
5. If this instruction addresses an I/O Port (Px, x= 0-3), add 3 to the number of states. Add 5 if it addresses a Peripheral SFR.
6. In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.

Table 33. Summary of unconditional Jump Instructions

| | | |
|---------------|--------------|--|
| Absolute jump | AJMP <src> | (PC) ← (PC) +2; (PC) _{10:0} ← src opnd |
| Extended jump | EJMP <src> | (PC) ← (PC) + size (instr); (PC) _{23:0} ← src opnd |
| Long jump | LJMP <src> | (PC) ← (PC) + size (instr); (PC) _{15:0} ← src opnd |
| Short jump | SJMP rel | (PC) ← (PC) +2; (PC) ← (PC) +rel |
| Jump indirect | JMP @A +DPTR | (PC) _{23:16} ← FFh; (PC) _{15:0} ← (A) + (DPTR) |
| No operation | NOP | (PC) ← (PC) +1 |

| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
|----------|------------------------------|------------------------------------|-------------|----------------------|-------------|----------------------|
| | | | Bytes | States | Bytes | States |
| AJMP | addr11 | Absolute jump | 2 | 3 ⁽²⁾ (3) | 2 | 3 ⁽²⁾ (3) |
| EJMP | addr24 | Extended jump | 5 | 6 ⁽²⁾ (4) | 4 | 5 ⁽²⁾ (4) |
| | @DRk | Extended jump (indirect) | 3 | 7 ⁽²⁾ (4) | 2 | 6 ⁽²⁾ (4) |
| LJMP | @WRj | Long jump (indirect) | 3 | 6 ⁽²⁾ (4) | 2 | 5 ⁽²⁾ (4) |
| | addr16 | Long jump (direct address) | 3 | 5 ⁽²⁾ (4) | 3 | 5 ⁽²⁾ (4) |
| SJMP | rel | Short jump (relative address) | 2 | 4 ⁽²⁾ (4) | 2 | 4 ⁽²⁾ (4) |
| JMP | @A +DPTR | Jump indirect relative to the DPTR | 1 | 5 ⁽²⁾ (4) | 1 | 5 ⁽²⁾ (4) |
| NOP | | No operation (Jump never) | 1 | 1 | 1 | 1 |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 3 to the number of states if the destination address is external.

Table 34. Summary of Call and Return Instructions

| | | |
|---------------------------------|-------------|--|
| Absolute call | ACALL <src> | (PC) ← (PC) +2; push (PC) _{15:0} ; (PC) _{10:0} ← src opnd |
| Extended call | ECALL <src> | (PC) ← (PC) + size (instr); push (PC) _{23:0} ; (PC) _{23:0} ← src opnd |
| Long call | LCALL <src> | (PC) ← (PC) + size (instr); push (PC) _{15:0} ; (PC) _{15:0} ← src opnd |
| Return from subroutine | RET | pop (PC) _{15:0} |
| Extended return from subroutine | ERET | pop (PC) _{23:0} |
| Return from interrupt | RETI | IF [INTR= 0] THEN pop (PC) _{15:0} IF [INTR= 1] THEN pop (PC) _{23:0} ; pop (PSW1) |
| Trap interrupt | TRAP | (PC) ← (PC) + size (instr); IF [INTR= 0] THEN push (PC) _{15:0} IF [INTR= 1] THEN push (PSW1); push (PC) _{23:0} |

| Mnemonic | <dest>, <src> ⁽¹⁾ | Comments | Binary Mode | | Source Mode | |
|----------|------------------------------|-------------------------------------|-------------|-----------------------|-------------|-----------------------|
| | | | Bytes | States | Bytes | States |
| ACALL | addr11 | Absolute subroutine call | 2 | 9 ⁽²⁾ (3) | 2 | 9 ⁽²⁾ (3) |
| ECALL | @DRk | Extended subroutine call (indirect) | 3 | 14 ⁽²⁾ (3) | 2 | 13 ⁽²⁾ (3) |
| | addr24 | Extended subroutine call | 5 | 14 ⁽²⁾ (3) | 4 | 13 ⁽²⁾ (3) |
| LCALL | @WRj | Long subroutine call (indirect) | 3 | 10 ⁽²⁾ (3) | 2 | 9 ⁽²⁾ (3) |
| | addr16 | Long subroutine call | 3 | 9 ⁽²⁾ (3) | 3 | 9 ⁽²⁾ (3) |
| RET | | Return from subroutine | 1 | 7 ⁽²⁾ | 1 | 7 ⁽²⁾ |
| ERET | | Extended subroutine return | 3 | 9 ⁽²⁾ | 2 | 8 ⁽²⁾ |
| RETI | | Return from interrupt | 1 | 7 ⁽²⁾ (4) | 1 | 7 ⁽²⁾ (4) |
| TRAP | | Jump to the trap interrupt vector | 2 | 12 ⁽⁴⁾ | 1 | 11 ⁽⁴⁾ |

Notes:

1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination/return address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 5 to the number of states if INTR= 1.

8. EPROM Programming

8.1. Internal ROM Features

The internal ROM of the TSC87251G1A products contains five different areas:

- Code Memory
- Configuration Bytes
- Lock Bits
- Encryption Array
- Signature Bytes

8.1.1. EPROM/OTPROM Devices

All the Internal ROM but the Signature Bytes of the TSC87251G1A products is made of EPROM cells. The Signature Bytes of the TSC87251GxD products are made of Mask ROM.

The TSC87251G1A products are programmed and verified in the same manner as TEMIC's TSC87251G1 and TSC87251A1A, using a SINGLE-PULSE algorithm, which programs at VPP= 12.75V using only one 100 μs pulse per byte. This results in a programming time of less than 5 seconds for the 16 Kbytes on-chip code memory.

The EPROM of TSC87251G1A products in Window CQPJ is erasable by Ultra-Violet radiation (UV). UV erasure set all the EPROM memory cells to one and allows a reprogramming. The quartz window must be covered with an opaque label when the device is in operation. This is not so much to protect the EPROM array from inadvertent erasure, as to protect the RAM and other on-chip logic. Allowing light to impinge on the silicon die during device operation may cause a logical malfunction.

Note:

Erasure of the EPROM begins to occur when the chip is exposed to light wavelength shorter than 4000Å. Since sunlight and fluorescent light have wavelength in this range, exposure to these light sources over an extended time (1 week in sunlight or 3 years in room-level fluorescent lighting) could cause inadvertent erasure.

The TSC87251G1A products in plastic packages are One Time Programmable (OTP). Then an EPROM cell cannot be reset by UV once programmed to zero.

8.1.2. Security Features

In some microcontrollers applications, it is desirable that the user program code be secured from unauthorized access. The TSC87251G1A offers two kinds of protection for program code stored in the on-chip array:

- Program code in the on-chip Code Memory is encrypted when read out for verification if the Encryption Array is programmed.
- A three-level lock bit system restricts external access to the on-chip code memory.

8.1.3. Lock Bit System

The TSC87251G1A products implement 3 levels of security for User's program as described in Table 35.

The first level locks the programming of the User's internal Code Memory, the Configuration Bytes and the Encryption Array.

The second level locks the verifying of the User's internal Code Memory. It is always possible to verify the Configuration Bytes and the Lock Bits. It is never possible to verify the Encryption Array.

The third level locks the external execution.

Table 35. Lock bits Programming

| Level | Lock bits LB[2:0] | Internal Execution | External Execution | Verification | Programming | External PROM read (MOVC) |
|----------|-------------------|--------------------|--------------------|-----------------------|-------------|---------------------------|
| 0 | 000 | Enable | Enable | Enable ⁽¹⁾ | Enable | Enable ⁽²⁾ |
| 1 | 001 | Enable | Enable | Enable ⁽¹⁾ | Disable | Disable |
| 2 | 011 | Enable | Enable | Disable | Disable | Disable |
| 3 | 111 | Enable | Disable | Disable | Disable | Disable |
| Reserved | Other | x | x | x | x | x |

Notes:

1. Returns encrypted data if Encryption Array is programmed.
2. Returns non encrypted data.

Level 1 should be set before programming Level 2; Level 2 should be set before programming Level 3.

The security level may be verified according to Table 36.

Table 36. Lock bits Verifying

| Level | Lock bits Data ⁽¹⁾ |
|-------|-------------------------------|
| 0 | xxxxx000 |
| 1 | xxxxx001 |
| 2 | xxxxx01x |
| 3 | xxxxx1xx |

Note:

1. x means don't care.

8.1.4. Encryption Array

The TSC87251G1A products include a 128-byte Encryption Array located in non-volatile memory outside the memory address space. During verification of the on-chip code memory, the seven low-order address bits also address the Encryption Array. As the byte of the code memory is read, it is exclusive-NOR'ed (XNOR) with the key byte from the Encryption Array. If the Encryption Array is not programmed (still all 1s), the user program code is placed on the data bus in its original, unencrypted form. If the Encryption Array is programmed with key bytes, the user program code is encrypted and cannot be used without knowledge of the key byte sequence.

To preserve the secrecy of the encryption key byte sequence, the Encryption Array can not be verified.

Cautions:

1. When a MOVC instruction is executed, the content of the ROM is not encrypted. In order to fully protect the user program code, the lock bit level 1 (see Table 1) must always be set when encryption is used.
2. If the encryption feature is implemented, the portion of the on-chip code memory that does not contain program code should be filled with "random" byte values to prevent the encryption key sequence from being revealed.

8.2. Signature Bytes

The TSC87251G1A products contain factory-programmed Signature Bytes. These bytes are located in non-volatile memory outside the memory address space at 30h, 31h, 60h and 61h. To read the Signature Bytes, perform the procedure described in section 8.4., "Verify Algorithm", using the verify signature mode (see Table 39). Signature byte values are listed in Table 37.

Table 37. Signature Bytes (Electronic ID)

| | | Signature Address | Signature Data |
|--------------|---------------------|-------------------|----------------|
| Vendor | TEMIC | 30h | 58h |
| Architecture | C251 | 31h | 40h |
| Memory | 16K EPROM/OTPROM | 60h | FBh |
| Revision | First (TSC8x251G1A) | 61h | FFh |

8.3. Programming Algorithm

Figure 8 shows the hardware setup needed to program the TSC87251G1A EPROM areas:

- The chip has to be put under reset and maintained in this state until the completion of the programming sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the programming sequence (see below).
- The voltage on the EA# pin must be set to VDD.
- The programming mode is selected according to the code applied on Port 0 (see Table 38). It has to be applied until the completion of this programming operation.
- The programming address is applied on Ports 1 and 3 which are respectively the Most Significant Byte (MSB) and the Least Significant Byte (LSB) of the address.
- The programming data are applied on Port 2.
- The EPROM Programming is done by raising the voltage on the EA# pin to VPP, then by generating a low level pulse on ALE/PROG# pin.
- The voltage on the EA# pin must be lowered to VDD before completing the programming operation.
- It is possible to alternate programming and verifying operation (See paragraph 8.4.). Please make sure the voltage on the EA# pin has actually been lowered to VDD before performing the verifying operation.
- PSEN# and the other control signals have to be released to complete a sequence of programming operations or a sequence of programming and verifying operations.

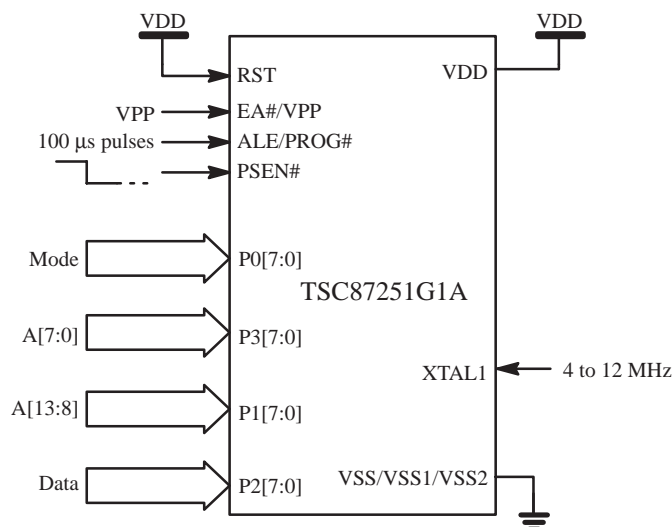


Figure 8. Setup for EPROM Programming

Table 38. Programming Modes

| ROM Area ⁽¹⁾ | RST | EA#/VPP | PSEN# | ALE/PROG# ⁽²⁾ | P0 | P2 | P1(MSB) P3(LSB) |
|-------------------------|-----|---------|-------|--------------------------|-----|------|--|
| On-chip Code Memory | 1 | VPP | 0 | 1 Pulse | 68h | Data | 16-bit Address 0000h-3FFFh (16K) |
| Configuration Bytes | 1 | VPP | 0 | 1 Pulse | 69h | Data | CONFIG0: 0080h CONFIG1: 0081h |
| Lock Bits | 1 | VPP | 0 | 1 Pulse | 6Bh | X | LB0: 0001h LB1: 0002h LB2: 0003h |
| Encryption Array | 1 | VPP | 0 | 1 Pulse | 6Ch | Data | 0000h-007Fh |

Notes:

1. Signature Bytes are not user-programmable.
2. The ALE/PROG# pulse waveform is shown in Figure 24 page 46.

8.4. Verify Algorithm

Figure 9 shows the hardware setup needed to verify the TSC87251G1A EPROM areas:

- The chip has to be put under reset and maintained in this state until the completion of the verifying sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the verifying sequence (see below).
- The voltage on the EA# pin must be set to VDD and ALE must be set to a high level.
- The Verifying Mode is selected according to the code applied on Port 0. It has to be applied until the completion of this verifying operation.
- The verifying address is applied on Ports 1 and 3 which are respectively the MSB and the LSB of the address.
- Then device is driving the data on Port 2.
- It is possible to alternate programming and verification operation (see paragraph 8.3.). Please make sure the voltage on the EA# pin has actually been lowered to VDD before performing the verifying operation.
- PSEN# and the other control signals have to be released to complete a sequence of verifying operations or a sequence of programming and verifying operations.

Table 39. Verifying Modes

| ROM Area ⁽¹⁾ | RST | EA#/VPP | PSEN# | ALE/PROG# | P0 | P2 | P1(MSB) P3(LSB) |
|-------------------------|-----|---------|-------|-----------|-----|------|-------------------------------------|
| On-chip code memory | 1 | 1 | 0 | 1 | 28h | Data | 16-bit Address 0000h-3FFFh (16K) |
| Configuration Bytes | 1 | 1 | 0 | 1 | 29h | Data | CONFIG0: 0080h CONFIG1: 0081h |
| Lock Bits | 1 | 1 | 0 | 1 | 2Bh | Data | 0000h |
| Signature Bytes | 1 | 1 | 0 | 1 | 29h | Data | 0030h, 0031h, 0060h, 0061h |

Note:

1. To preserve the secrecy of on-chip code memory when encrypted, the Encryption Array can not be verified.

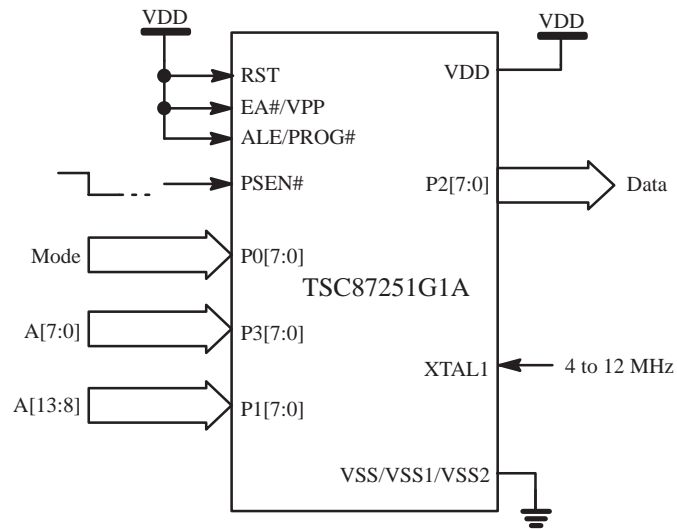


Figure 9. Setup for EPROM Verifying

9. Absolute Maximum Rating and Operating Conditions

9.1. Absolute Maximum Rating

Table 40. Absolute Maximum Ratings

| | |
|---|----------------|
| ● Storage Temperature | -65 to +150°C |
| ● Voltage on any other Pin to VSS | -0.5 to +6.5 V |
| ● Voltage on EA#/VPP Pin to VSS | 0 to +13.0 V |
| ● I _{OL} per I/O Pin | 15 mA |
| ● Power Dissipation | 1.5 W |

9.2. Operating Conditions

Table 41. Operating Conditions

| | |
|----------------------------------|--------------|
| ● Ambient Temperature Under Bias | |
| Commercial | 0 to +70°C |
| Industrial | -40 to +85°C |
| ● V _{DD} | 4.5 to 5.5 V |

Note:

Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

10. DC Characteristics – Commercial & Industrial

Table 42. DC Characteristics; $V_{DD}= 4.5$ to 5.5 V, $T_A= -40$ to $+85^\circ\text{C}$

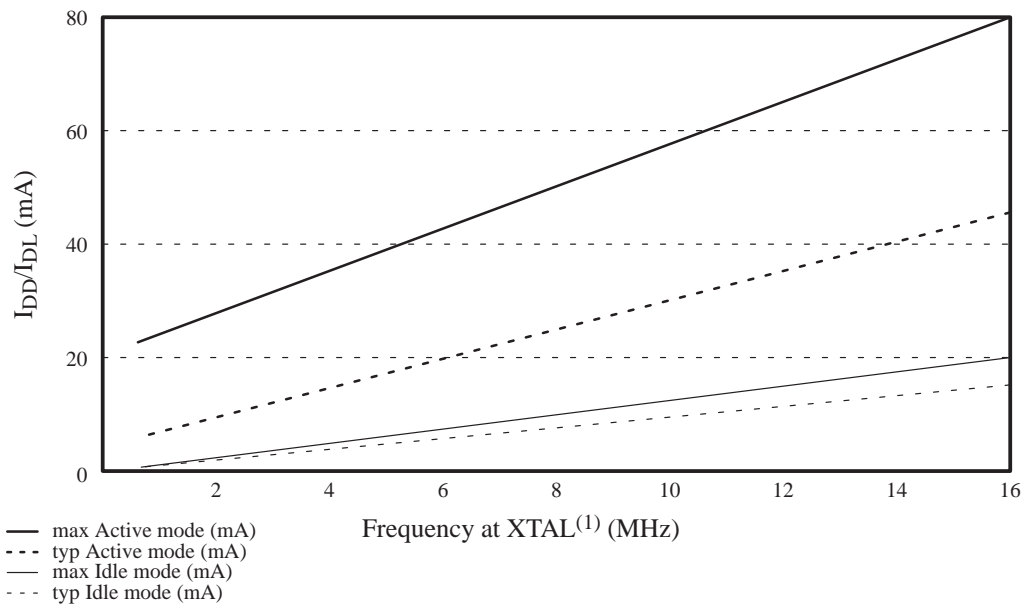
| Symbol | Parameter | Min | Typical ⁽⁴⁾ | Max | Units | Test Conditions |
|-----------------|---|--|------------------------|--------------------|------------------|--|
| V_{IL} | Input Low Voltage (except EA#, SCL, SDA) | -0.5 | | $0.2V_{DD} - 0.1$ | V | |
| $V_{IL1}^{(5)}$ | Input Low Voltage (SCL, SDA) | -0.5 | | $0.3V_{DD}$ | V | |
| V_{IL2} | Input Low Voltage (EA#) | 0 | | $0.2V_{DD} - 0.3$ | V | |
| V_{IH} | Input high Voltage (except XTAL1, RST, SCL, SDA) | $0.2V_{DD} + 0.9$ | | $V_{DD} + 0.5$ | V | |
| $V_{IH1}^{(5)}$ | Input high Voltage (XTAL1, RST, SCL, SDA) | $0.7V_{DD}$ | | $V_{DD} + 0.5$ | V | |
| V_{OL} | Output Low Voltage (Ports 1, 2, 3) | | | 0.3 0.45 1.0 | V | $I_{OL}= 100 \mu\text{A}^{(1)(2)}$ $I_{OL}= 1.6 \text{ mA}^{(1)(2)}$ $I_{OL}= 3.5 \text{ mA}^{(1)(2)}$ |
| V_{OL1} | Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address) | | | 0.3 0.45 1.0 | V | $I_{OL}= 200 \mu\text{A}^{(1)(2)}$ $I_{OL}= 3.2 \text{ mA}^{(1)(2)}$ $I_{OL}= 7.0 \text{ mA}^{(1)(2)}$ |
| V_{OH} | Output high Voltage (Ports 1, 2, 3, ALE, PSEN#) | $V_{DD} - 0.3$ $V_{DD} - 0.7$ $V_{DD} - 1.5$ | | | V | $I_{OH}= -10 \mu\text{A}^{(3)}$ $I_{OH}= -30 \mu\text{A}^{(3)}$ $I_{OH}= -60 \mu\text{A}^{(3)}$ |
| V_{OH1} | Output high Voltage (Port 0, Port 2 in Page Mode during External Address) | $V_{DD} - 0.3$ $V_{DD} - 0.7$ $V_{DD} - 1.5$ | | | V | $I_{OH}= -200 \mu\text{A}$ $I_{OH}= -3.2 \text{ mA}$ $I_{OH}= -7.0 \text{ mA}$ |
| V_{RST+} | Reset threshold on | | 3.7 | | V | |
| V_{RST-} | Reset threshold off | | 3.3 | | V | |
| V_{RET} | V_{DD} data retention limit | | | 1.8 | V | |
| I_{ILO} | Logical 0 Input Current (Ports 1, 2, 3) | | | - 50 | μA | $V_{IN}= 0.45 \text{ V}$ |
| I_{LI} | Input Leakage Current (Port 0) | | | ± 10 | μA | $0.45 \text{ V} < V_{IN} < V_{DD}$ |
| I_{TL} | Logical 1-to-0 Transition Current (Ports 1, 2, 3) | | | - 650 | μA | $V_{IN}= 2.0 \text{ V}$ |
| R_{RST} | RST Pull-Down Resistor | 40 | 170 | 225 | $\text{k}\Omega$ | |
| C_{IO} | Pin Capacitance | | 10 | | pF | $T_A= 25^\circ\text{C}$ |
| I_{DD} | Operating Current | | 35 | 65 | mA | $F_{OSC}= 12 \text{ MHz}$ |
| | | | 45 | 80 | mA | $F_{OSC}= 16 \text{ MHz}$ |
| I_{DL} | Idle Mode Current | | 10 | 15 | mA | $F_{OSC}= 12 \text{ MHz}$ |
| | | | 15 | 20 | mA | $F_{OSC}= 16 \text{ MHz}$ |
| I_{PD} | Power-Down Current | | 10 | 20 | μA | $V_{RET} < V_{DD} < 5.5 \text{ V}$ |
| V_{PP} | Programming Supply Voltage | 12.5 | | 13 | V | $T_A= 0$ to $+40^\circ\text{C}$ |
| I_{PP} | Programming Supply Current | | | 75 | mA | $T_A= 0$ to $+40^\circ\text{C}$ |

Notes:

- Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

| | |
|--|-----------------------|
| Maximum I_{OL} per port pin: | 10 mA |
| Maximum I_{OL} per 8-bit port: | Port 0 26 mA |
| | Ports 1-3 15 mA |
| Maximum Total I_{OL} for all: | Output Pins ... 71 mA |

If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
- Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
- Typical values are obtained using $V_{DD}=5\text{ V}$ and $T_A=25^\circ\text{C}$ with no guarantee. They are not tested and there is not guarantee on these values.
- The input threshold voltage of SCL and SDA meets the I²C specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.



Note:

- The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

Figure 10. I_{DD}/I_{DL} versus Frequency; $V_{DD}=4.5$ to 5.5 V

10.1. DC Characteristics: I_{DD} , I_{DL} and I_{PD} Test Conditions

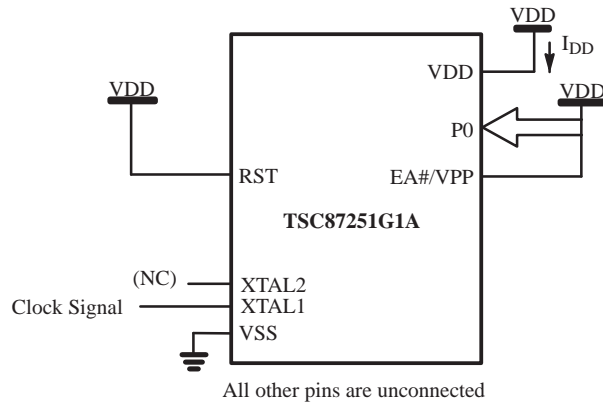


Figure 11. I_{DD} Test Condition, Active Mode

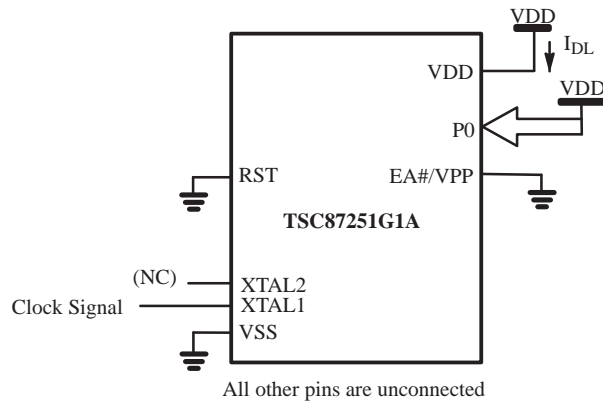


Figure 12. I_{DL} Test Condition, Idle Mode

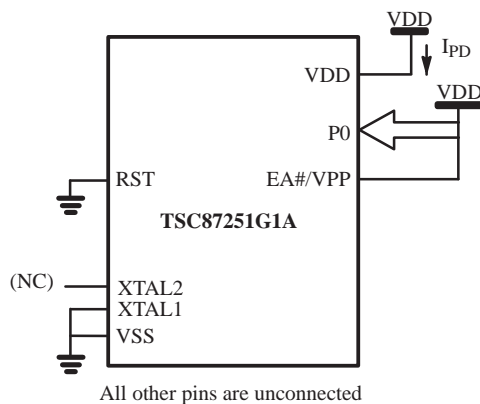


Figure 13. I_{PD} Test Condition, Power-Down Mode

11. AC Characteristics – Commercial & Industrial

11.1. AC Characteristics – External Bus Cycles

Definition of symbols

Table 43. External Bus Cycles Timing Symbol Definitions

| Signals | | Conditions | |
|---------|-----------|------------|-----------------|
| A | Address | H | High |
| D | Data In | L | Low |
| L | ALE | V | Valid |
| Q | Data Out | X | No Longer Valid |
| R | RD#/PSEN# | Z | Floating |
| W | WR# | | |

Timings

Test conditions: capacitive load on all pins= 50 pF.

Table 44 lists AC timing parameters for the TSC87251G1A with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and or by extending ALE. In these tables, Note 2 marks parameters affected by one ALE wait state, and Note 3 marks parameters affected by one PSEN#/RD#/WR# wait state.

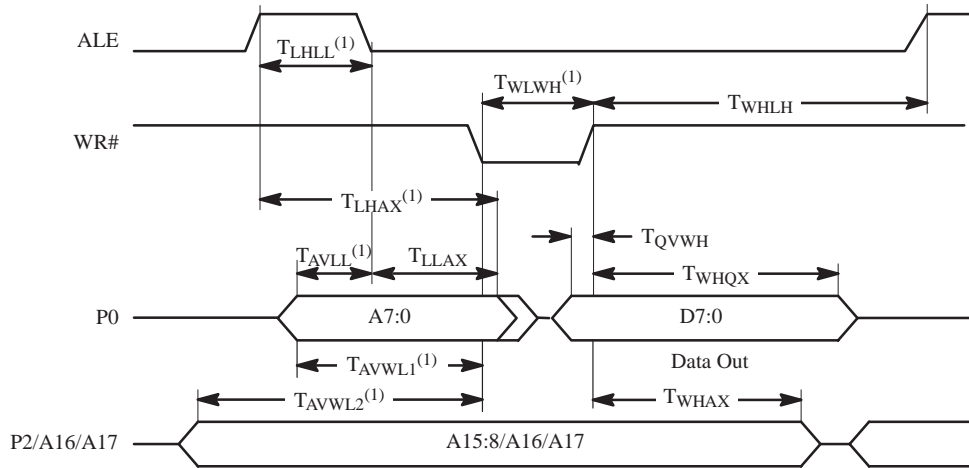
Figure 14 to Figure 19 show the bus cycles with the timing parameters.

Table 44. Bus Cycles AC Timings; $V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to 85°C

| Symbol | Parameter | 16 MHz | | FOSC Variable | | Unit |
|----------------------------------|--|--------|-----|------------------------|------------------------|----------------------|
| | | Min | Max | Min | Max | |
| T _{OSC} | 1/F _{OSC} | 63 | | | | ns |
| T _{LHLL} | ALE Pulse Width | 53 | | T _{OSC} -10 | | ns ⁽²⁾ |
| T _{AVLL} | Address Valid to ALE Low | 43 | | T _{OSC} -20 | | ns ⁽²⁾ |
| T _{LLAX} | Address hold after ALE Low | 43 | | T _{OSC} -20 | | ns |
| T _{RLRH} ⁽¹⁾ | RD#/PSEN# Pulse Width | 45 | | T _{OSC} -18 | | ns ⁽³⁾ |
| T _{RHRL} | RD#/PSEN# High to RD#/PSEN# Low | 53 | | T _{OSC} -10 | | ns |
| T _{WLWH} | WR# Pulse Width | 45 | | T _{OSC} -18 | | ns ⁽³⁾ |
| T _{LLRL} ⁽¹⁾ | ALE Low to RD#/PSEN# Low | 53 | | T _{OSC} -10 | | ns |
| T _{LHAX} | ALE High to Address Hold | 105 | | 2×T _{OSC} -20 | | ns ⁽²⁾ |
| T _{RLDV} ⁽¹⁾ | RD#/PSEN# Low to Valid Data | | 43 | | T _{OSC} -20 | ns ⁽³⁾ |
| T _{RHDX} ⁽¹⁾ | Data Hold After RD#/PSEN# High | 0 | | 0 | | ns |
| T _{RHAX} ⁽¹⁾ | Address Hold After RD#/PSEN# High | 0 | | 0 | | ns |
| T _{RLAZ} ⁽¹⁾ | RD#/PSEN# Low to Address Float | | 2 | | 2 | ns |
| T _{RHDZ1} | Instruction Float After RD#/PSEN# High | | 43 | | T _{OSC} -20 | ns |
| T _{RHDZ2} | Data Float After RD#/PSEN# High | | 43 | | T _{OSC} -20 | ns |
| T _{RHLH1} | RD#/PSEN# high to ALE High (Instruction) | 48 | | T _{OSC} -15 | | ns |
| T _{RHLH2} | RD#/PSEN# high to ALE High (Data) | 173 | | 3×T _{OSC} -15 | | ns |
| T _{WHLH} | WR# High to ALE High | 173 | | 3×T _{OSC} -15 | | ns |
| T _{AVDV1} | Address (P0) Valid to Valid Data In | | 190 | | 3×T _{OSC} -60 | ns ⁽²⁾⁽³⁾ |
| T _{AVDV2} | Address (P2) Valid to Valid Data In | | 273 | | 4×T _{OSC} -60 | ns ⁽²⁾⁽³⁾ |
| T _{AVDV3} | Address (P0) Valid to Valid Instruction In | | 128 | | 3×T _{OSC} -60 | ns |
| T _{AXDX} | Data Hold after Address Hold | 0 | | 0 | | ns |
| T _{AVRL} ⁽¹⁾ | Address Valid to RD# Low | 101 | | 2×T _{OSC} -24 | | ns ⁽²⁾ |
| T _{AVWL1} | Address (P0) Valid to WR# Low | 101 | | 2×T _{OSC} -24 | | ns ⁽²⁾ |
| T _{AVWL2} | Address (P2) Valid to WR# Low | 158 | | 3×T _{OSC} -30 | | ns ⁽²⁾ |
| T _{WHQX} | Data Hold after WR# High | 43 | | T _{OSC} -20 | | ns |
| T _{QVWH} | Data Valid to WR# High | 38 | | T _{OSC} -25 | | ns ⁽³⁾ |
| T _{WHAX} | WR# High to Address Hold | 105 | | 2×T _{OSC} -20 | | ns |

Notes:

1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add 2×T_{OSC}.
3. If a wait state is added by extending RD#/PSEN#/WR#, add 2×T_{OSC}.

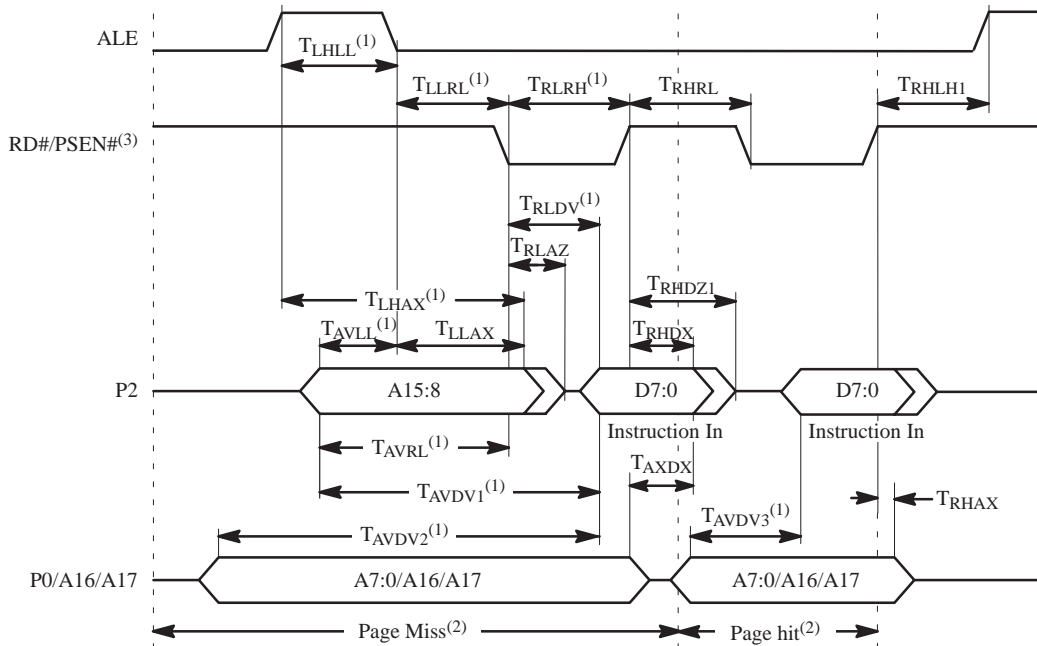


Note:

1. The value of this parameter depends on wait states. See Table 44.

Figure 16. External Bus Cycle: DataWrite (Non-Page Mode)

Waveforms in Page Mode



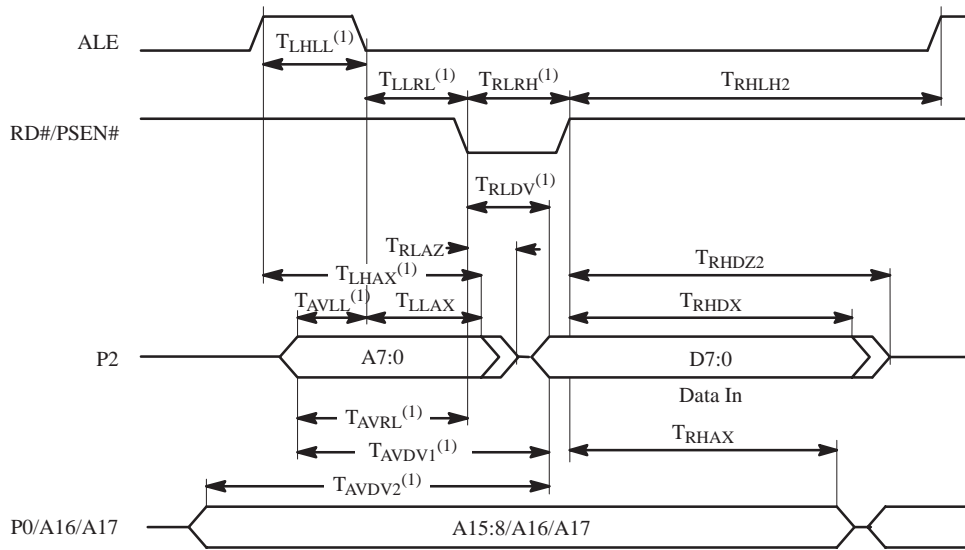
Notes:

1. The value of this parameter depends on wait states. See Table 44.

2. A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2 \times T_{OSC}$); a page miss requires two states ($4 \times T_{OSC}$).

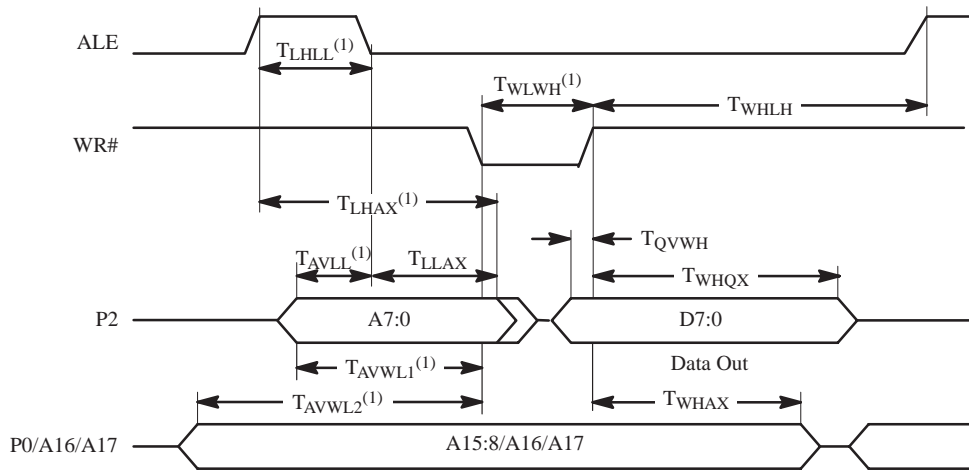
3. During a sequence of page hits, PSEN# toggles between each byte fetching.

Figure 17. External Bus Cycle: Code Fetch (Page Mode)



Note:
 1. The value of this parameter depends on wait states. See Table 44.

Figure 18. External Bus Cycle: Data Read (Page Mode)



Note:
 1. The value of this parameter depends on wait states. See Table 44.

Figure 19. External Bus Cycle: Data Write (Page Mode)

11.2. AC Characteristics – Serial Port in Shift Register Mode

Definition of symbols

Table 45. Serial Port Timing Symbol Definitions

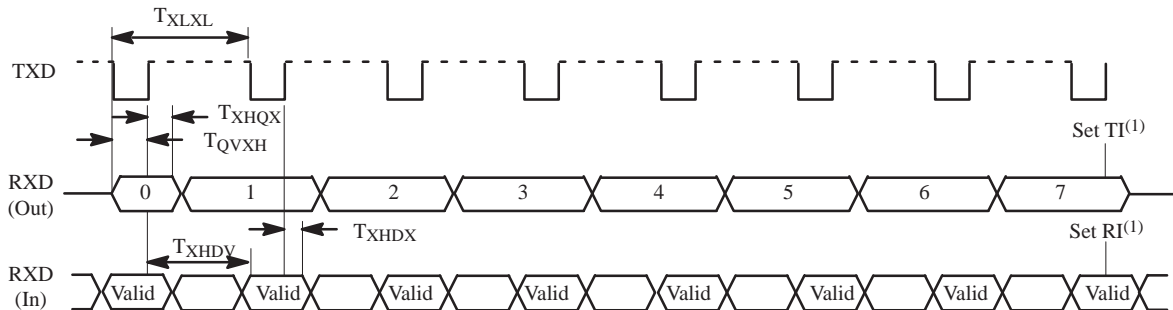
| Signals | | Conditions | |
|---------|----------|------------|-----------------|
| D | Data In | H | High |
| Q | Data Out | L | Low |
| X | Clock | V | Valid |
| | | X | No Longer Valid |

Timings

Table 46. Serial Port AC Timing –Shift Register Mode; $V_{DD}= 4.5$ to 5.5 V, $T_A= -40$ to 85°C

| Symbol | Parameter | 16 MHz | | FOSC Variable | | Unit |
|-------------|--|--------|-----|---------------------------|---------------------------|------|
| | | Min | Max | Min | Max | |
| T_{XLXL} | Serial Port Clock Cycle Time | 756 | | $12 \times T_{OSC}$ | | ns |
| T_{QVXH} | Output Data Setup to Clock Rising Edge | 620 | | $12 \times T_{OSC} - 136$ | | ns |
| T_{XHQX} | Output Data hold after Clock Rising Edge | 510 | | $10 \times T_{OSC} - 120$ | | ns |
| T_{XHDX} | Input Data Hold after Clock Rising Edge | 0 | | 0 | | ns |
| T_{XHDTV} | Clock Rising Edge to Input Data Valid | | 500 | | $10 \times T_{OSC} - 130$ | ns |

Waveforms



Note:

1. T_I and R_I are set during $SIP1$ of the peripheral cycle following the shift of the eight bit.

Figure 20. Serial Port Waveforms – Shift Register Mode

11.3. AC Characteristics – SSLC: I²C Interface

Timings

Table 47. I²C Interface AC Timing; V_{DD}= 4.5 to 5.5 V, T_A= -40 to 85°C

| Symbol | Parameter | INPUT | | OUTPUT | |
|-----------------------|---|--------------------------------------|--------|--|-----------------------|
| | | Min | Max | Min | Max |
| T _{HD; STA} | Start condition hold time | 14×T _C LCL ⁽⁴⁾ | | 4.0 μs ⁽¹⁾ | |
| T _{LOW} | SCL low time | 16×T _C LCL ⁽⁴⁾ | | 4.7 μs ⁽¹⁾ | |
| T _{HIGH} | SCL high time | 14×T _C LCL ⁽⁴⁾ | | 4.0 μs ⁽¹⁾ | |
| T _{RC} | SCL rise time | | 1 μs | | – ⁽²⁾ |
| T _{FC} | SCL fall time | | 0.3 μs | | 0.3 μs ⁽³⁾ |
| T _{SU; DAT1} | Data set-up time | 250 ns | | 20×T _C LCL ⁽⁴⁾ – T _{RD} | |
| T _{SU; DAT2} | SDA set-up time (before repeated START condition) | 250 ns | | 1 μs ⁽¹⁾ | |
| T _{SU; DAT3} | SDA set-up time (before STOP condition) | 250 ns | | 8×T _C LCL ⁽⁴⁾ | |
| T _{HD; DAT} | Data hold time | 0 ns | | 8×T _C LCL ⁽⁴⁾ – T _{FC} | |
| T _{SU; STA} | Repeated START set-up time | 14×T _C LCL ⁽⁴⁾ | | 4.7 μs ⁽¹⁾ | |
| T _{SU; STO} | STOP condition set-up time | 14×T _C LCL ⁽⁴⁾ | | 4.0 μs ⁽¹⁾ | |
| T _{BUF} | Bus free time | 14×T _C LCL ⁽⁴⁾ | | 4.7 μs ⁽¹⁾ | |
| T _{RD} | SDA rise time | | 1 μs | | – ⁽²⁾ |
| T _{FD} | SDA fall time | | 0.3 μs | | 0.3 μs ⁽³⁾ |

Notes:

- At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
- Determined by the external bus-line capacitance and the external bus-line pull-up resistor; this must be < 1 μs.
- Spikes on the SDA and SCL lines with a duration of less than 3×T_CLCL will be filtered out. Maximum capacitance on bus-lines SDA and SCL= 400 pF.
- T_CLCL= T_{OSC}= one oscillator clock period.

Waveforms

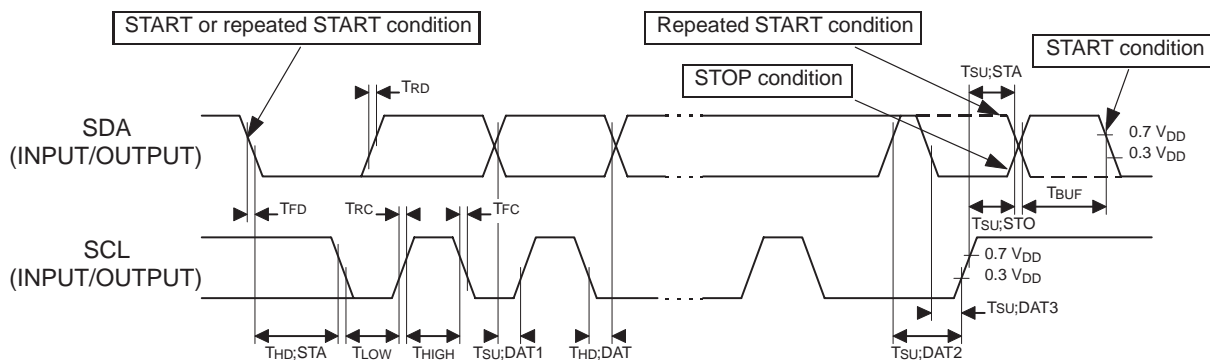


Figure 21. I²C Waveforms

11.4. AC Characteristics – SSLC: SPI Interface

Definition of symbols

Table 48. SPI Interface Timing Symbol Definitions

| Signals | | Conditions | |
|---------|----------|------------|-----------------|
| C | Clock | H | High |
| I | Data In | L | Low |
| O | Data Out | V | Valid |
| | | X | No Longer Valid |

Timings

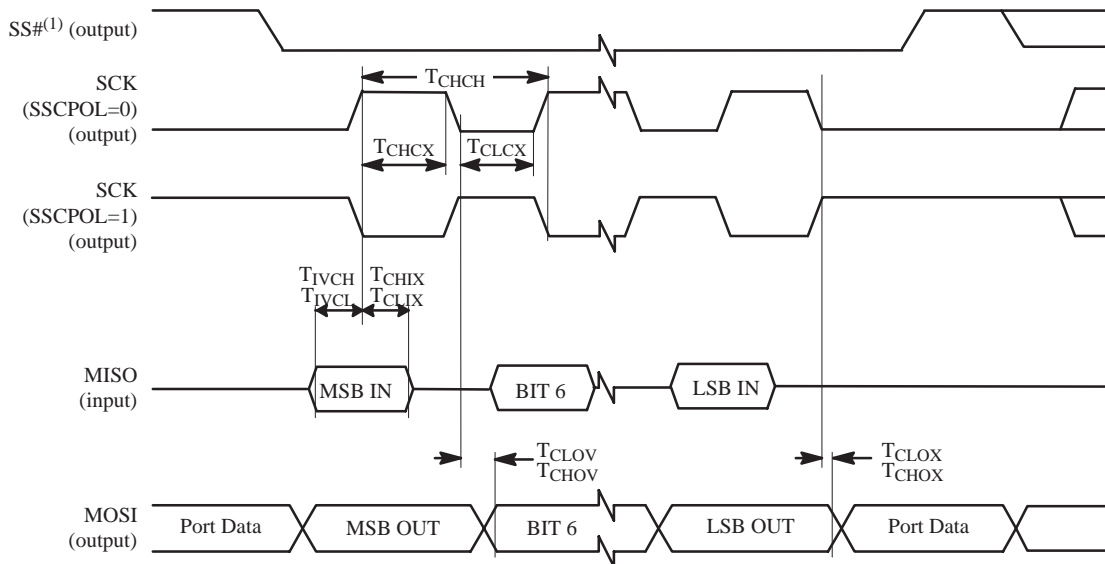
Table 49. SPI Interface AC Timing; $V_{DD}= 4.5$ to 5.5 V, $T_A= -40$ to 85°C

| Symbol | Parameter | Min | Max | Unit |
|----------------------------------|--|-----|-----|---------------|
| Master mode⁽¹⁾ | | | | |
| T_{CHCH} | Clock Period | 4 | | T_{OSC} |
| T_{CHCX} | Clock High Time | 1.6 | | T_{OSC} |
| T_{CLCX} | Clock Low Time | 1.6 | | T_{OSC} |
| T_{IVCL}, T_{IVCH} | Input Data Valid to Clock Edge | 50 | | ns |
| T_{CLIX}, T_{CHIX} | Input Data Hold after Clock Edge | 50 | | ns |
| T_{CLOV}, T_{CHOV} | Output Data Valid after Clock Edge | | 65 | ns |
| T_{CLOX}, T_{CHOX} | Output Data Hold Time after Clock Edge | 0 | | ns |
| T_{ILIH} | Input Data Rise Time | | 2 | μs |
| T_{IHIL} | Input Data Fall Time | | 2 | μs |
| T_{OLOH} | Output Data Rise time | | 50 | ns |
| T_{OHOL} | Output Data Fall Time | | 50 | ns |

Notes:

1. Capacitive load on all pins= 100 pF in master mode.

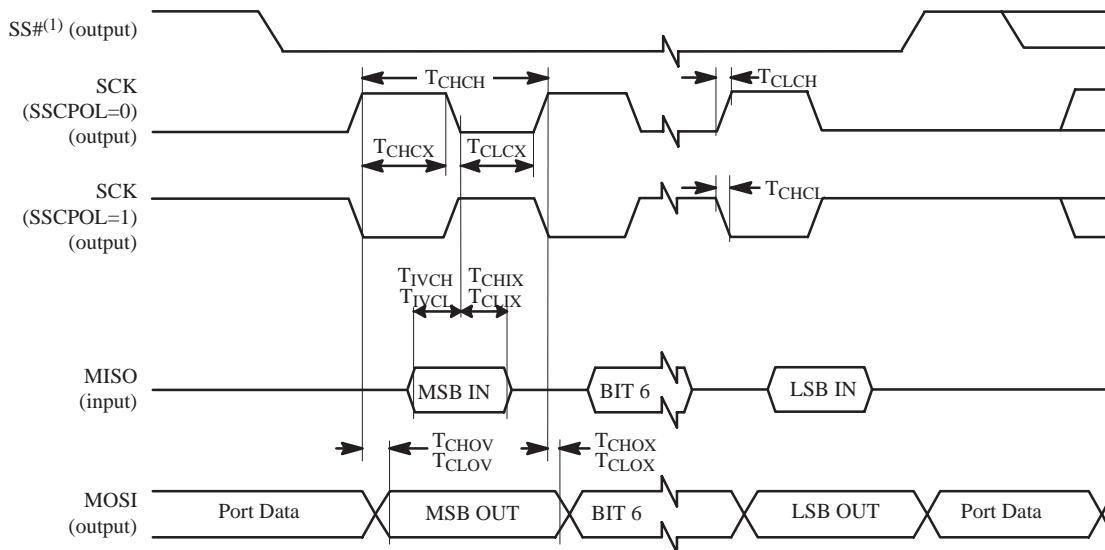
Waveforms



Note:

1. SS# handled by software.

Figure 22. SPI Master Waveforms (SSCPHA= 0)



Note:

1. SS# handled by software.

Figure 23. SPI Master Waveforms (SSCPHA= 1)

11.5. AC Characteristics – EPROM Programming and Verifying

Definition of symbols

Table 50. EPROM Programming & Verifying Timing Symbol Definitions

| Signals | | Conditions | |
|---------|----------------------------|------------|-----------------|
| A | Address | H | High |
| E | Enable: mode set on Port 0 | L | Low |
| Q | Data Out | V | Valid |
| | | X | No Longer Valid |
| | | Z | Floating |

Timings

Table 51. EPROM Programming and Verifying AC timings; $V_{DD}= 4.5$ to 5.5 V, $T_A= 0$ to 40°C

| Symbol | Parameter | Min | Max | Unit |
|--------------------|------------------------------|---------------------|---------------------|------|
| T _{Osc} | XTAL1 Frequency | 83.5 | 250 | ns |
| T _{AVGL} | Address Setup to PROG# low | 48×T _{Osc} | | |
| T _{GHAX} | Address Hold after PROG# low | 48×T _{Osc} | | |
| T _{DVGL} | Data Setup to PROG# low | 48×T _{Osc} | | |
| T _{GHDX} | Data Hold after PROG# | 48×T _{Osc} | | |
| T _{EHSH} | ENABLE High to VPP | 48×T _{Osc} | | |
| T _{SHGL} | VPP Setup to PROG# low | 10 | | μs |
| T _{GHSL} | VPP Hold after PROG# | 10 | | μs |
| T _{SLLEL} | ENABLE Hold after VPP | 0 | | |
| T _{GLGH} | PROG# Width | 90 | 110 | μs |
| T _{AVQV} | Address to Data Valid | | 48×T _{Osc} | |
| T _{AXQX} | Address to Data Invalid | 0 | | ns |
| T _{ELQV} | ENABLE low to Data Valid | | 48×T _{Osc} | |
| T _{EHQZ} | Data Float after ENABLE | 0 | 48×T _{Osc} | |

Waveforms

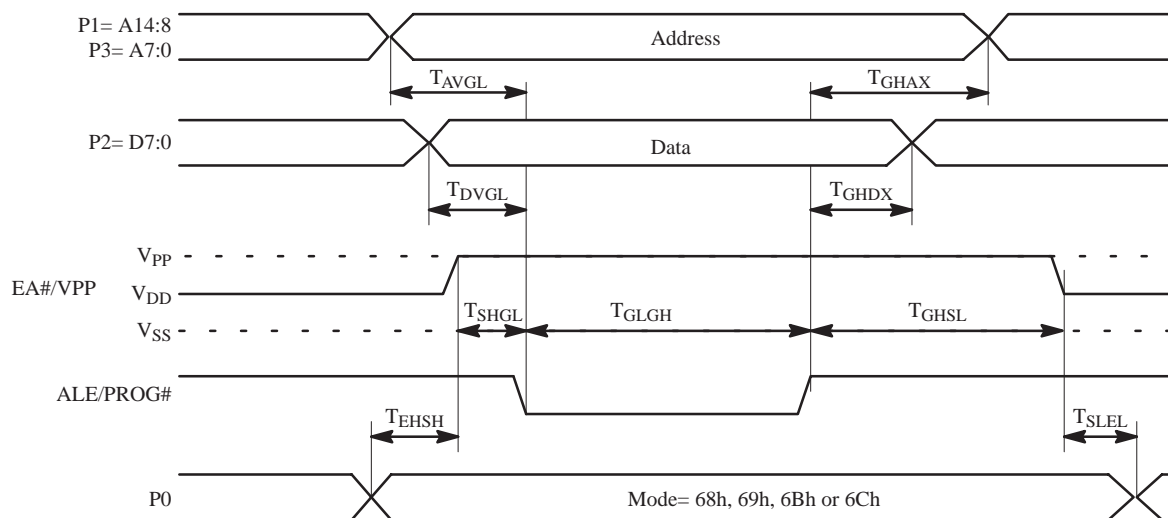


Figure 24. EPROM Programming Waveforms

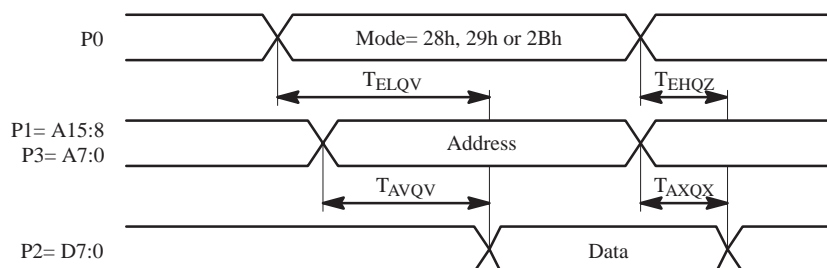


Figure 25. EPROM Verifying Waveforms

11.6. AC Characteristics – External Clock Drive and Logic Level References

Definition of symbols

Table 52. External Clock Timing Symbol Definitions

| Signals | |
|---------|-------|
| C | Clock |

| Conditions | |
|------------|-----------------|
| L | Low |
| H | High |
| X | No Longer Valid |

Timings

Table 53. External Clock AC Timings; $V_{DD}= 4.5$ to 5.5 V, $T_A= -40$ to $+85^\circ\text{C}$

| Symbol | Parameter | Min | Max | Unit |
|-------------------|----------------------|-----|-----|------|
| F _{OSC} | Oscillator Frequency | | 24 | MHz |
| T _{CHCX} | High Time | 10 | | ns |
| T _{CLCX} | Low Time | 10 | | ns |
| T _{CLCH} | Rise Time | 3 | | ns |
| T _{CHCL} | Fall Time | 3 | | ns |

Waveforms

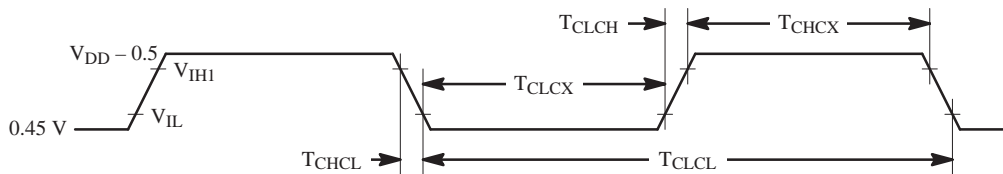
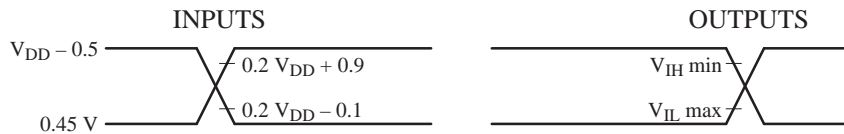


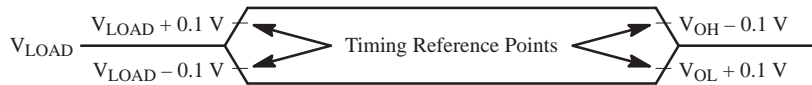
Figure 26. External Clock Waveform



Note:

During AC testing, all inputs are driven at $V_{DD} - 0.5$ V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 27. AC Testing Input/Output Waveforms



Note:

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

Figure 28. Float Waveforms

12. Packages

12.1. List of Packages

- PDIL 40
- PLCC 44
- CQPJ 44

12.2. PDIL 40 – Mechanical Outline

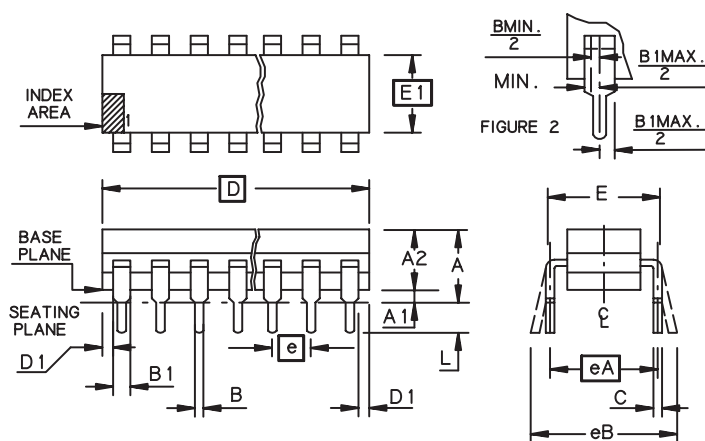


Figure 29: Plastic Dual In Line

Table 54: PDIL Package Size

| | MM | | INCH | |
|----|--------------|-------|-------------|-------|
| | Min | Max | Min | Max |
| A | – | 5.08 | – | .200 |
| A1 | 0.38 | – | .015 | – |
| A2 | 3.18 | 4.95 | .125 | .195 |
| B | 0.36 | 0.56 | .014 | .022 |
| B1 | 0.76 | 1.78 | .030 | .070 |
| C | 0.20 | 0.38 | .008 | .015 |
| D | 50.29 | 53.21 | 1.980 | 2.095 |
| E | 15.24 | 15.87 | .600 | .625 |
| E1 | 12.32 | 14.73 | .485 | .580 |
| e | 2.54 B.S.C. | | .100 B.S.C. | |
| eA | 15.24 B.S.C. | | .600 B.S.C. | |
| eB | – | 17.78 | – | .700 |
| L | 2.93 | 3.81 | .115 | .150 |
| D1 | 0.13 | – | .005 | – |

12.3. PLCC 44 – Mechanical Outline

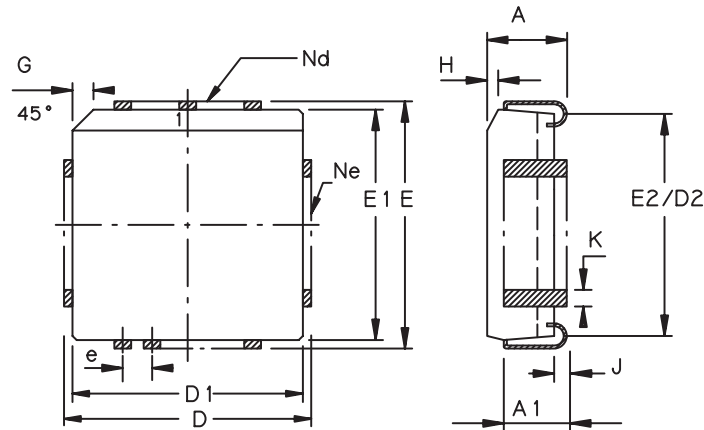


Figure 30: Plastic Lead Chip Carrier

Table 55: PLCC Package Size

| | MM | | INCH | |
|----|----------|-------|----------|------|
| | Min | Max | Min | Max |
| A | 4.20 | 4.57 | .165 | .180 |
| A1 | 2.29 | 3.04 | .090 | .120 |
| D | 17.40 | 17.65 | .685 | .695 |
| D1 | 16.44 | 16.66 | .647 | .656 |
| D2 | 14.99 | 16.00 | .590 | .630 |
| E | 17.40 | 17.65 | .685 | .695 |
| E1 | 16.44 | 16.66 | .647 | .656 |
| E2 | 14.99 | 16.00 | .590 | .630 |
| e | 1.27 BSC | | .050 BSC | |
| G | 1.07 | 1.22 | .042 | .048 |
| H | 1.07 | 1.42 | .042 | .056 |
| J | 0.51 | – | .020 | – |
| K | 0.33 | 0.53 | .013 | .021 |
| Nd | 11 | | 11 | |
| Ne | 11 | | 11 | |

12.4. CQPJ 44 with Window – Mechanical Outline

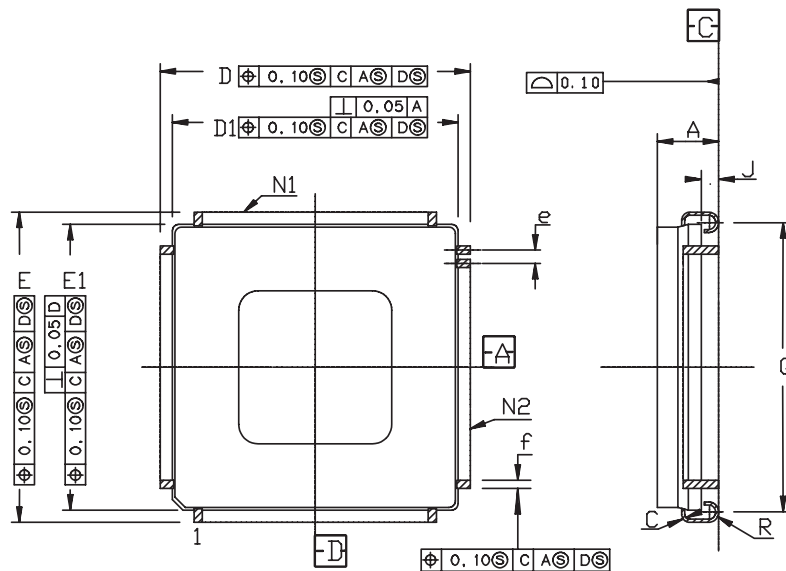


Figure 31: Ceramic Quad Pack J

Table 56: CQPJ Package size

| | MM | | INCH | |
|---------|----------|-------|----------|------|
| | Min | Max | Min | Max |
| A | – | 4.90 | – | .193 |
| C | 0.15 | 0.25 | .006 | .010 |
| D – E | 17.40 | 17.55 | .685 | .691 |
| D1 – E1 | 16.36 | 16.66 | .644 | .656 |
| e | 1.27 TYP | | .050 TYP | |
| f | 0.43 | 0.53 | .017 | .021 |
| J | 0.86 | 1.12 | .034 | .044 |
| Q | 15.49 | 16.00 | .610 | .630 |
| R | 0.86 TYP | | .034 TYP | |
| N1 | 11 | | 11 | |
| N2 | 11 | | 11 | |

13. Ordering Information

13.1. TSC87251G1A OTP (Step A)

High Speed Versions 4.5 to 5.5 V, Commercial and Industrial

| TEMIC Part Number | ROM | Description |
|-------------------|-------------|--|
| TSC87251G1A-16CA | 16K OTP ROM | 16 MHz, Commercial 0° to 70°C, PDIL 40 |
| TSC87251G1A-16CB | 16K OTP ROM | 16 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC87251G1A-16IA | 16K OTP ROM | 16 MHz, Industrial -40° to 85°C, PDIL 40 |
| TSC87251G1A-16IB | 16K OTP ROM | 16 MHz, Industrial -40° to 85°C, PLCC 44 |

13.2. TSC87251G1A EPROM – UV Window package (Step A)

High Speed Versions 4.5 to 5.5 V, Industrial

| TEMIC Part Number | ROM | Description |
|-------------------|-----------|---|
| TSC87251G1A-16IC | 16K EPROM | 16 MHz, Industrial -40° to 85°C, window CQPJ 44 |

13.3. TSC80251G1D ROMless (Step D)

High Speed Versions 4.5 to 5.5 V, Commercial and Industrial

| TEMIC Part Number ⁽²⁾ | ROM | Description |
|----------------------------------|---------|---|
| TSC80251G1D-24CA | ROMless | 24 MHz, Commercial 0° to 70°C, PDIL 40 |
| TSC80251G1D-24CB | ROMless | 24 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC80251G1D-24CED | ROMless | 24 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack ⁽¹⁾ |
| TSC80251G1D-16CA | ROMless | 16 MHz, Commercial 0° to 70°C, PDIL 40 |
| TSC80251G1D-16CB | ROMless | 16 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC80251G1D-16CED | ROMless | 16 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack ⁽¹⁾ |
| TSC80251G1D-16IA | ROMless | 16 MHz, Industrial -40° to 85°C, PDIL 40 |
| TSC80251G1D-16IB | ROMless | 16 MHz, Industrial -40° to 85°C, PLCC 44 |

Low Voltage Versions 2.7 to 5.5 V, Commercial

| TEMIC Part Number ⁽²⁾ | ROM | Description |
|----------------------------------|---------|--|
| TSC80251G1D-L12CB | ROMless | 12 MHz, Commercial, PLCC 44 |
| TSC80251G1D-L12CED | ROMless | 12 MHz, Commercial, VQFP 44, Dry pack ⁽¹⁾ |

13.4. TSC83251G1D Mask ROM (Step D)

High Speed Versions 4.5 to 5.5 V, Commercial and Industrial

| TEMIC Part Number ⁽²⁾ | ROM | Description |
|----------------------------------|-------------|---|
| TSC251G1Dxxx-24CA | 16K MaskROM | 24 MHz, Commercial 0° to 70°C, PDIL 40 |
| TSC251G1Dxxx-24CB | 16K MaskROM | 24 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC251G1Dxxx-24CED | 16K MaskROM | 24 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack ⁽¹⁾ |
| TSC251G1Dxxx-16CA | 16K MaskROM | 16 MHz, Commercial 0° to 70°C, PDIL 40 |
| TSC251G1Dxxx-16CB | 16K MaskROM | 16 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC251G1Dxxx-16CED | 16K MaskROM | 16 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack ⁽¹⁾ |
| TSC251G1Dxxx-16IA | 16K MaskROM | 16 MHz, Industrial -40° to 85°C, PDIL 40 |
| TSC251G1Dxxx-16IB | 16K MaskROM | 16 MHz, Industrial -40° to 85°C, PLCC 44 |

Low Voltage Versions 2.7 to 5.5 V, Commercial

| TEMIC Part Number ⁽²⁾ | ROM | Description |
|----------------------------------|-------------|---|
| TSC251G1Dxxx-L12CB | 16K MaskROM | 12 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC251G1Dxxx-L12CED | 16K MaskROM | 12 MHz, Commercial 0° to 70°C, VQFP 44, Dry pack ⁽¹⁾ |

Notes:

1. Dry Pack mandatory for VQFP package.
2. xxx: means ROM code, is Cxxx in case of encrypted code.

13.5. Options (Please consult TEMIC sales)

- ROM code encryption
- Tape & Real or Dry Pack
- Known good dice
- Ceramic packages
- Extended temperature range: -55°C to +125°C

13.6. Starter Kit

| TEMIC Part Number | Description |
|-------------------|----------------------|
| TSC80251-SK | TSC80251 Starter Kit |

13.7. Product Marking

Mask ROM versions

| |
|---|
| TEMIC Customer Part number Temic Part number ® INTEL'97 YYWW . Lot Number |
|---|

ROMless versions

| |
|---|
| TEMIC Temic Part number ® INTEL'97 YYWW . Lot Number |
|---|

OTP versions

| |
|---|
| TEMIC Temic Part number ® INTEL'95 YYWW . Lot Number |
|---|