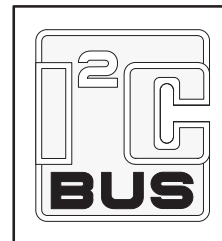# DATA SHEET

I²C
BUS

## 87C524/87C528

# 80C51 8-bit microcontrollers

16K/32K, 512 OTP, I²C, watchdog timer

Product specification

1999 Jul 23

**Philips**
**Semiconductors**

PHILIPS

**PHILIPS**

## 80C51 8-bit microcontrollers
## 16K/32K, 512 OTP, I²C, watchdog timer

## DESCRIPTION

The 87C528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C528 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C528—32k bytes ROM
- 83C524—16k bytes ROM
- 80C528—ROMless version of the 83C528
- 87C528—32k bytes EPROM
- 87C524—16k bytes EPROM

This device provides architectural enhancements that make it applicable in a variety of applications in consumer, telecom and general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

The 87C528 contains a 32k × 8 EPROM and the 87C524 contains a 16k x 8 EPROM. Both devices have a 512 × 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multi-source, two-priority-level, nested interrupt structure, two serial interfaces (UART and I²C-bus), and on-chip oscillator and timing circuits.

In addition, the 87C524/87C528 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

## FEATURES

- 80C51 instruction set
  - 512 × 8 RAM
  - Memory addressing capability 64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer with oscillator
  - Full duplex UART
  - I²C serial interface
- Power control modes:
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Extended temperature ranges
- EPROM code protection
- OTP package available
- 16 MHz speed at $V_{CC}$ = 5 V

## ORDERING INFORMATION

| EPROM | TEMPERATURE °C RANGE AND PACKAGE | FREQ (MHz) | Drawing Number |
|---|---|---|---|
| P87C528EBP N | 0 to +70, Plastic Dual In-line Package | 16 | SOT129-1 |
| P87C528EBA A | 0 to +70, Plastic Leaded Chip Carrier | 16 | SOT187-2 |
| P87C528EBB B | 0 to +70, Plastic Quad Flat Pack | 16 | SOT307-2 |
| P87C528EFP N | −40 to +85, Plastic Dual In-line Package | 16 | SOT129-1 |
| P87C528EFB B | −40 to +85, Plastic Quad Flat Pack | 16 | SOT307-2 |
| P87C524EBA A | 0 to +70, Plastic Leaded Chip Carrier | 16 | SOT187-2 |
| P87C524EBB B | 0 to +70, Plastic Quad Flat Pack | 16 | SOT307-2 |

**NOTE:**
1. For ROM & ROMless devices, see data sheet P8X524/528.

## 80C51 8-bit microcontrollers
### 16K/32K, 512 OTP, I$^2$C, watchdog timer
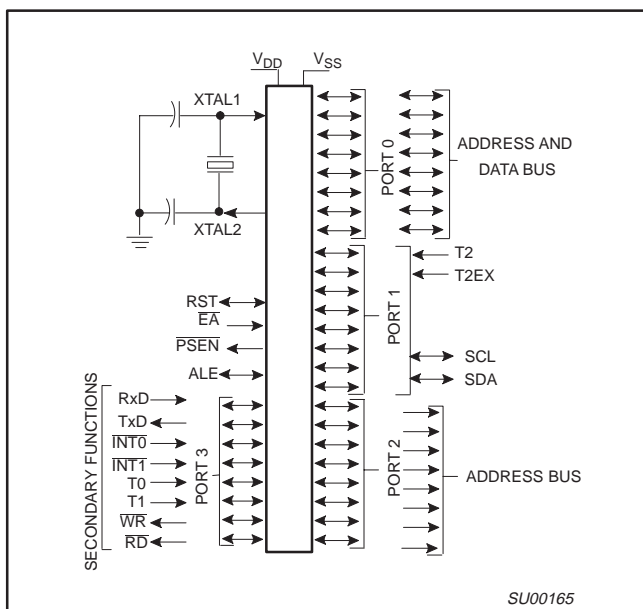
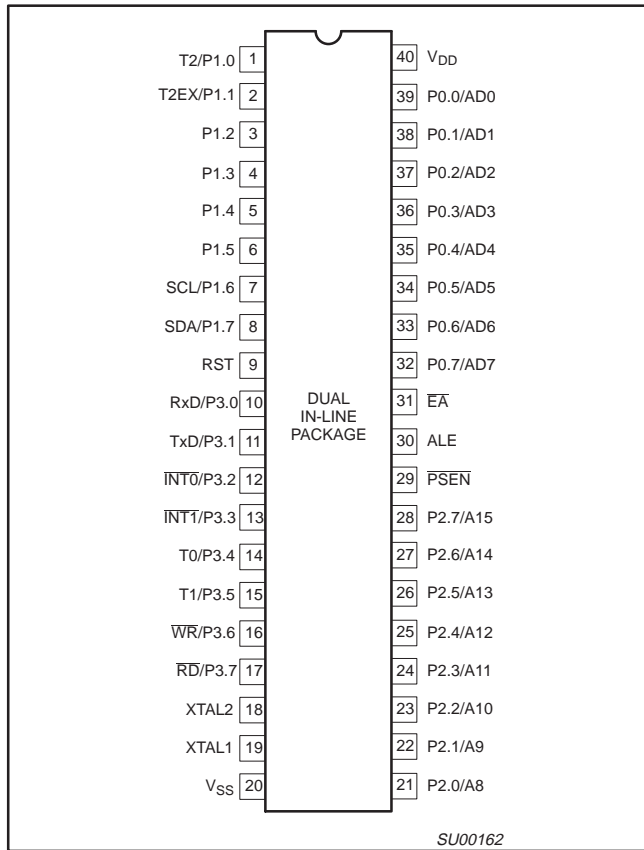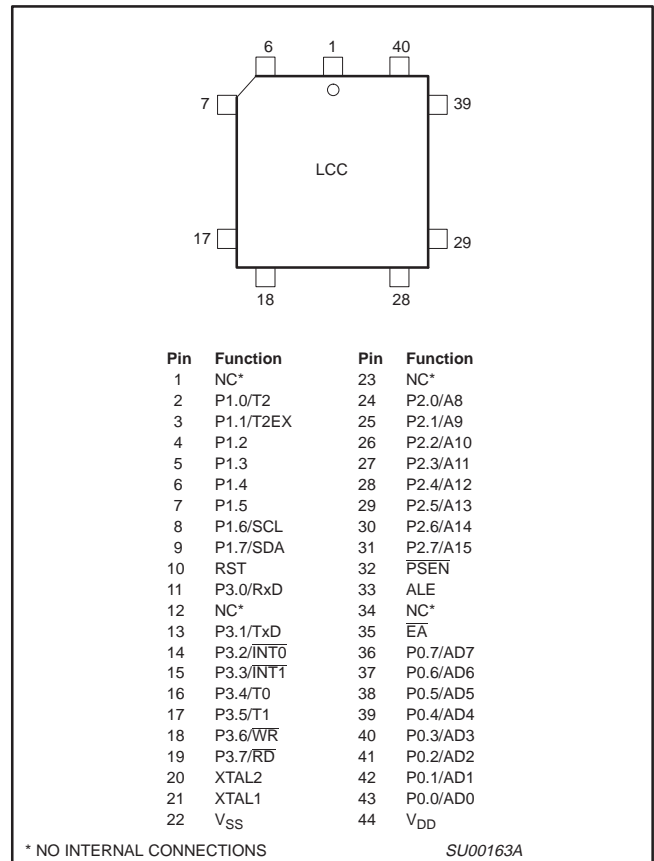### 87C524/87C528

## BLOCK DIAGRAM
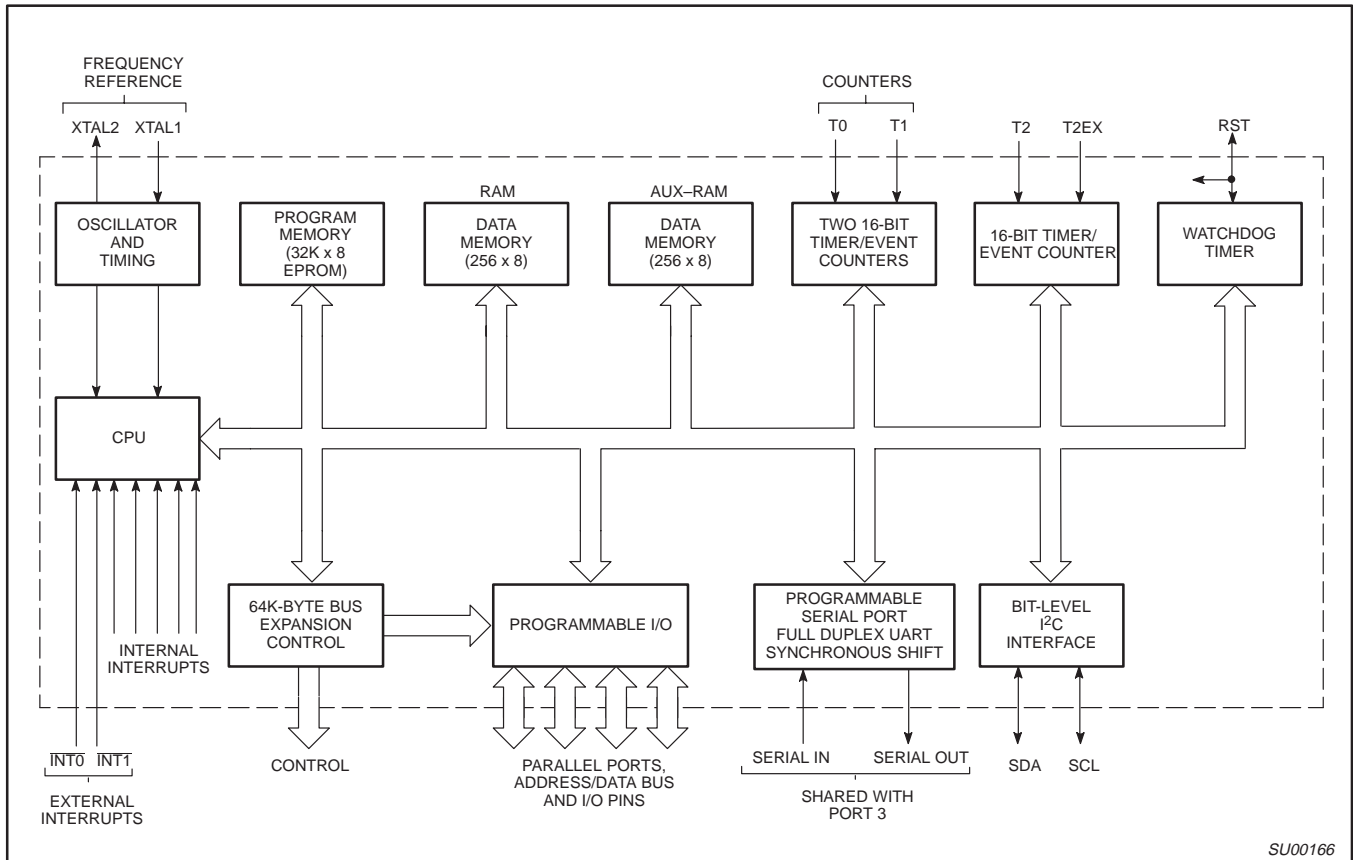


SU00166

## LOGIC SYMBOL



SU00165

## 80C51 8-bit microcontrollers
## 16K/32K, 512 OTP, I²C, watchdog timer

## 87C524/87C528

### PIN CONFIGURATIONS

| | | DUAL IN-LINE PACKAGE | | |
|---|---|---|---|---|
| T2/P1.0 | 1 | | 40 | V$_{DD}$ |
| T2EX/P1.1 | 2 | | 39 | P0.0/AD0 |
| P1.2 | 3 | | 38 | P0.1/AD1 |
| P1.3 | 4 | | 37 | P0.2/AD2 |
| P1.4 | 5 | | 36 | P0.3/AD3 |
| P1.5 | 6 | | 35 | P0.4/AD4 |
| SCL/P1.6 | 7 | | 34 | P0.5/AD5 |
| SDA/P1.7 | 8 | | 33 | P0.6/AD6 |
| RST | 9 | | 32 | P0.7/AD7 |
| RxD/P3.0 | 10 | | 31 | $\overline{EA}$ |
| TxD/P3.1 | 11 | | 30 | ALE |
| $\overline{INT0}$/P3.2 | 12 | | 29 | $\overline{PSEN}$ |
| $\overline{INT1}$/P3.3 | 13 | | 28 | P2.7/A15 |
| T0/P3.4 | 14 | | 27 | P2.6/A14 |
| T1/P3.5 | 15 | | 26 | P2.5/A13 |
| $\overline{WR}$/P3.6 | 16 | | 25 | P2.4/A12 |
| $\overline{RD}$/P3.7 | 17 | | 24 | P2.3/A11 |
| XTAL2 | 18 | | 23 | P2.2/A10 |
| XTAL1 | 19 | | 22 | P2.1/A9 |
| V$_{SS}$ | 20 | | 21 | P2.0/A8 |

SU00162

### PLASTIC LEADED CHIP CARRIER
### PIN FUNCTIONS

LCC

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC* | 23 | NC* |
| 2 | P1.0/T2 | 24 | P2.0/A8 |
| 3 | P1.1/T2EX | 25 | P2.1/A9 |
| 4 | P1.2 | 26 | P2.2/A10 |
| 5 | P1.3 | 27 | P2.3/A11 |
| 6 | P1.4 | 28 | P2.4/A12 |
| 7 | P1.5 | 29 | P2.5/A13 |
| 8 | P1.6/SCL | 30 | P2.6/A14 |
| 9 | P1.7/SDA | 31 | P2.7/A15 |
| 10 | RST | 32 | $\overline{PSEN}$ |
| 11 | P3.0/RxD | 33 | ALE |
| 12 | NC* | 34 | NC* |
| 13 | P3.1/TxD | 35 | $\overline{EA}$ |
| 14 | P3.2/$\overline{INT0}$ | 36 | P0.7/AD7 |
| 15 | P3.3/$\overline{INT1}$ | 37 | P0.6/AD6 |
| 16 | P3.4/T0 | 38 | P0.5/AD5 |
| 17 | P3.5/T1 | 39 | P0.4/AD4 |
| 18 | P3.6/$\overline{WR}$ | 40 | P0.3/AD3 |
| 19 | P3.7/$\overline{RD}$ | 41 | P0.2/AD2 |
| 20 | XTAL2 | 42 | P0.1/AD1 |
| 21 | XTAL1 | 43 | P0.0/AD0 |
| 22 | V$_{SS}$ | 44 | V$_{DD}$ |

* NO INTERNAL CONNECTIONS

SU00163A

## 80C51 8-bit microcontrollers
### 16K/32K, 512 OTP, I²C, watchdog timer

### 87C524/87C528

## PLASTIC QUAD FLAT PACK
## PIN FUNCTIONS
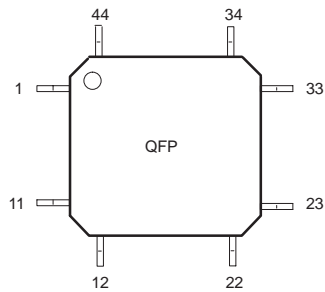


| Pin | Function | Pin | Function |
|-----|----------|-----|----------|
| 1 | P1.5 | 23 | P2.5/A13 |
| 2 | P1.6/SCL | 24 | P2.6/A14 |
| 3 | P1.7/SDA | 25 | P2.7/A15 |
| 4 | RST | 26 | $\overline{PSEN}$ |
| 5 | P3.0/RxD | 27 | ALE |
| 6 | NC* | 28 | NC* |
| 7 | P3.1/TxD | 29 | $\overline{EA}$ |
| 8 | P3.2/$\overline{INT0}$ | 30 | P0.7/AD7 |
| 9 | P3.3/$\overline{INT1}$ | 31 | P0.6/AD6 |
| 10 | P3.4/T0 | 32 | P0.5/AD5 |
| 11 | P3.5/T1 | 33 | P0.4/AD4 |
| 12 | P3.6/$\overline{WR}$ | 34 | P0.3/AD3 |
| 13 | P3.7/$\overline{RD}$ | 35 | P0.2/AD2 |
| 14 | XTAL2 | 36 | P0.1/AD1 |
| 15 | XTAL1 | 37 | P0.0/AD0 |
| 16 | $V_{SS}$ | 38 | $V_{DD}$ |
| 17 | NC* | 39 | NC* |
| 18 | P2.0/A8 | 40 | P1.0/T2 |
| 19 | P2.1/A9 | 41 | P1.1/T2EX |
| 20 | P2.2/A10 | 42 | P1.2 |
| 21 | P2.3/A11 | 43 | P1.3 |
| 22 | P2.4/A12 | 44 | P1.4 |

* NO INTERNAL CONNECTIONS          SU00164

## 80C51 8-bit microcontrollers
16K/32K, 512 OTP, I$^2$C, watchdog timer

### PIN DESCRIPTIONS

| MNEMONIC | PIN NO. | | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|---|
| | DIP | LCC | QFP | | |
| V$_{SS}$ | 20 | 22 | 16 | I | **Ground:** circuit ground potential. |
| V$_{DD}$ | 40 | 44 | 38 | I | **Power Supply:** +5 V power supply pin during normal operation, Idle mode and Power-down mode. |
| P0.0–0.7 | 39–32 | 43–36 | 37–30 | I/O | **Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. |
| P1.0–P1.7 | 1–8 | 2–9 | 40–44 1–3 | I/O | **Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which have open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I$_{IL}$). Port 1 can sink/source one TTL (4 LSTTL) inputs. Port 1 receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2: |
| | 1 | 2 | 40 | I | **T2 (P1.0):** Timer/counter 2 external count input (following edge triggered). |
| | 2 | 3 | 41 | I | **T2EX (P1.1):** Timer/counter 2 trigger input. |
| | 7 | 8 | 2 | I/O | **SCL (P1.6):** I$^2$C serial port clock line. |
| | 8 | 9 | 3 | I/O | **SDA (P1.7):** I$^2$C serial port data line. |
| P2.0–P2.7 | 21–28 | 24–31 | 18–25 | I/O | **Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I$_{IL}$). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. |
| P3.0–P3.7 | 10–17 | 11, 13–19 | 5, 7–13 | I/O | **Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I$_{IL}$). Port 3 also serves the special features of the SC80C51 family, as listed below: |
| | 10 | 11 | 5 | I | **RxD (P3.0):** Serial input port |
| | 11 | 13 | 7 | O | **TxD (P3.1):** Serial output port |
| | 12 | 14 | 8 | I | **$\overline{INT0}$ (P3.2):** External interrupt |
| | 13 | 15 | 9 | I | **$\overline{INT1}$ (P3.3):** External interrupt |
| | 14 | 16 | 10 | I | **T0 (P3.4):** Timer 0 external input |
| | 15 | 17 | 11 | I | **T1 (P3.5):** Timer 1 external input |
| | 16 | 18 | 12 | O | **$\overline{WR}$ (P3.6):** External data memory write strobe |
| | 17 | 19 | 13 | O | **$\overline{RD}$ (P3.7):** External data memory read strobe |
| RST | 9 | 10 | 4 | I/O | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V$_{SS}$ permits a power-on reset using only an external capacitor to V$_{DD}$. After a watchdog timer overflow, this pin is pulled high while the internal reset signal is active. |
| ALE | 30 | 33 | 27 | I/O | **Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. |
| $\overline{PSEN}$ | 29 | 32 | 26 | O | **Program Store Enable:** The read strobe to external program memory. When the device is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory. |
| $\overline{EA}$ | 31 | 35 | 29 | I | **External Access Enable:** $\overline{EA}$ must be externally held low during RESET to enable the device to fetch code from external program memory locations 0000H to 7FFFH. If $\overline{EA}$ is held high during RESET, the device executes from internal program memory unless the program counter contains an address greater than 7FFFH. $\overline{EA}$ is don't care after RESET. |
| XTAL1 | 19 | 21 | 15 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 18 | 20 | 14 | O | **Crystal 2:** Output from the inverting oscillator amplifier. |

**Table 1.    8XC524/8XC528 Special Function Registers**

| SYMBOL | DESCRIPTION | DIRECT ADDRESS | BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION | | | | | | | | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MSB | | | | | | | LSB | |
| ACC* | Accumulator | E0H | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | 00H |
| B* | B register | F0H | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | 00H |
| DPTR:<br>  DPH<br>  DPL | Data pointer (2 bytes):<br>  Data pointer high<br>  Data pointer low | <br>83H<br>82H | | | | | | | | | <br>00H<br>00H |
| | | | AF | AE | AD | AC | AB | AA | A9 | A8 | |
| IE*# | Interrupt enable | A8H | EA | ES1 | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 | 00H |
| | | | BF | BE | BD | BC | BB | BA | B9 | B8 | |
| IP*# | Interrupt priority | B8H | – | PS1 | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 | x0000000B |
| | | | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 | |
| P0* | Port 0 | 80H | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FFH |
| | | | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | |
| P1* | Port 1 | 90H | SDA | SEL | – | – | – | – | T2EX | T2 | FFH |
| | | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| P2* | Port 2 | A0H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | FFH |
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| P3* | Port 3 | B0H | RD | WR | T1 | T0 | INT1 | INT0 | TxD | RxD | FFH |
| PCON | Power control | 87H | SMOD | – | – | – | GF1 | GF0 | PD | IDL | 0xxx0000B |
| | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| PSW* | Program status word | D0H | CY | AC | F0 | RS1 | RS0 | OV | F1 | P | 00H |
| RCAP2H# | Capture high | CBH | | | | | | | | | 00H |
| RCAP2L# | Capture low | CAH | | | | | | | | | 00H |
| SBUF | Serial data buffer | 99H | | | | | | | | | xxxxxxxxB |
| | | | 9F | 9E | 9D | 9C | 9B | 9A | 99 | 98 | |
| SCON* | Serial controller | 98H | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | 00H |
| S1BIT# | Serial I2C data | D9H/RD | SDI | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x0000000B |
| | | WR | SD0 | X | X | X | X | X | X | X | 0xxxxxxxB |
| S1INT# | Serial I2C interrupt | DAH | INT | X | X | X | X | X | X | X | 0xxxxxxxB |
| | | | DF | DE | DD | DC | DB | DA | D9 | D8 | |
| S1SCS*# | Serial I2C control | D8H/RD | SDI | SCI | CLH | BB | RBF | WBF | STR | ENS | xxxx0000B |
| | | WR | SD0 | SC0 | CLH | X | X | X | STR | ENS | 00xxxx00B |
| SP | Stack pointer | 81H | | | | | | | | | 07H |
| | | | 8F | 8E | 8D | 8C | 8B | 8A | 89 | 88 | |
| TCON* | Timer control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00H |
| | | | CF | CE | CD | CC | CB | CA | C9 | C8 | |
| T2CON*# | Timer 2 control | C8H | TF2 | EXF2 | RCLK | TCLK | EXEN2 | TR2 | C/T2 | CP/RL2 | 00H |
| TH0<br>TH1<br>TH2#<br>TL0<br>TL1<br>TL2#<br>T3# | Timer high 0<br>Timer high 1<br>Timer high 2<br>Timer low 0<br>Timer low 1<br>Timer low 2<br>Watchdog timer | 8CH<br>8DH<br>CDH<br>8AH<br>8BH<br>CCH<br>FFH | | | | | | | | | 00H<br>00H<br>00H<br>00H<br>00H<br>00H<br>00H |
| TMOD | Timer mode | 89H | GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 | 00H |
| WDCON# | Watchdog control | A5H | | | | | | | | | A5H |

\*   SFRs are bit addressable.
\#   SFRs are modified from or added to the 80C51 SFRs.

## Table 2.  Internal and External Program Memory Access with Security Bit Set

| INSTRUCTION | ACCESS TO INTERNAL PROGRAM MEMORY | ACCESS TO EXTERNAL PROGRAM MEMORY |
|---|---|---|
| MOVC in internal program memory | YES | YES |
| MOVC in external program memory | NO | YES |

## INTERNAL DATA MEMORY

The internal data memory is divided into three physically separated segments: 256 bytes of RAM, 256 bytes of AUX-RAM, and a 128 bytes special function area. These can be addressed each in a different way.
– RAM 0 to 127 can be addressed directly and indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
– RAM 128 to 255 can only be addressed indirectly as in the 80C51. Address pointers are R0 and R1 of the selected register bank.
– AUX-RAM 0 to 255 is indirectly addressed in the same way as external data memory with the MOVX instructions. Address pointers are R0, R1 of the selected register bank and DPTR. An access to AUX-RAM 0 to 255 will not affect ports P0, P2, P3.6 and P3.7.

An access to external data memory locations higher than 255 will be performed with the MOVX DPTR instructions in the same way as in the 8051 structure, so with P0 and P2 as data/address bus and P3.6 and P3.7 as write and read timing signals. Note that these external data memory cannot be accessed with R0 and R1 as address pointer.

## TIMER 2

Timer 2 is functionally equal to the Timer 2 of the 8052AH. Timer 2 is a 16-bit timer/counter. These 16 bits are formed by two special function registers TL2 and TH2. Another pair of special function register RCAP2L and RCAP2H form a 16-bit capture register or a 16-bit reload register. Like Timer 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/T2N in the special function register T2CON. It has three operating modes: capture, autoload, and baud rate generator mode which are selected by bits in T2CON.

## WATCHDOG TIMER T3

The watchdog timer consists of an 11-bit prescaler and an 8-bit timer formed by special function register T3. The prescaler is incremented by an on-chip oscillator with a fixed frequency of 1MHz. The maximum tolerance on this frequency is –50% and +100%. The 8-bit timer increments every 2048 cycles of the on-chip oscillator. When a timer overflow occurs, the microcontroller is reset and a reset output pulse of $16 \times 2048$ cycles of the on-chip oscillator is generated at pin RST. The internal RESET signal is not inhibited when the external RST pin is kept low by, for example, an external reset circuit. The RESET signal drives port 1, 2, 3 into the high state and port 0 into the high impedance state.

The watchdog timer is controlled by one special function register WDCON with the direct address location A5H. WDCON can be read and written by software. A value of A5H in WDCON halts the on-chip oscillator and clears both the prescaler and timer T3. After the RESET signal, WDCON contains A5H. Every value other than A5H in WDCON enables the watchdog timer. When the watchdog timer is enabled, it runs independently of the XTAL-clock.

Timer T3 can be read on the fly. Timer T3 can only be written if WDCON contains the value 5AH. A successful write operation to T3 will clear the prescaler and WDCON, leaving the watchdog enabled and preventing inadvertent changes of T3. To prevent an overflow of the watchdog timer, the user program has to reload the watchdog timer within periods that are shorter than the programmed watchdog timer internal. This time interval is determined by an 8-bit value that has to be loaded in register T3 while at the same time the prescaler is cleared by hardware.

$$\text{Watchdog timer interval} = \frac{[256 - (T3)] \times 2048}{on - chip\ oscillator\ frequency}$$

## BIT-LEVEL I$^2$C INTERFACE

This bit-level serial I/O interface supports the I$^2$C-bus. P1.6/SCL and P1.7/SDA are the serial I/O pins. These two pins meet the I$^2$C specification concerning the input levels and output drive capability. Consequently, these pins have an open drain output configuration. All the four modes of the I$^2$C-bus are supported:
– master transmitter
– master receiver
– slave transmitter
– slave receiver

The advantages of the bit-level I$^2$C hardware compared with a full software I$^2$C implementation are:
– the hardware can generate the SCL pulse
– Testing a single bit (RBF respectively, WBF) is sufficient as a check for error free transmission.

The bit-level I$^2$C hardware operates on serial bit level and performs the following functions:
– filtering the incoming serial data and clock signals
– recognizing the START condition
– generating a serial interrupt request SI after reception of a START condition and the first falling edge of the serial clock
– recognizing the STOP condition
– recognizing a serial clock pulse on the SCL line
– latching a serial bit on the SDA line (SDI)
– stretching the SCL LOW period of the serial clock to suspend the transfer of the next serial data bit
– setting Read Bit Finished (RBF) when the SCL clock pulse has finished and Write Bit Finished (WBF) if there is no arbitration loss detected (i.e., SDA = 0 while SDO = 1)
– setting a serial clock Low-to-High detected (CLH) flag
– setting a Bus Busy (BB) flag on a START condition and clearing this flag on a STOP condition
– releasing the SCL line and clearing the CLH, RBF and WBF flags to resume transfer of the next serial data bit
– generating an automatic clock if the single bit data register S1BIT is used in master mode.

The following functions must be done in software:
– handling the I$^2$C START interrupts
– converting serial to parallel data when receiving
– converting parallel to serial data when transmitting
– comparing the received slave address with its own
– interpreting the acknowledge information
– guarding the I$^2$C status if RBF or WBF = 0.

Additionally, if acting as master:
– generating START and STOP conditions

– handling bus arbitration

– generating serial clock pulses if S1BIT is not used.

Three SFRs control the bit-level I²C interface: S1INT, S1BIT and
S1SCS.

## INTERRUPT SYSTEM

The interrupt structure of the 8XC528 is the same as that used in the
80C51, but includes two additional interrupt sources: one for the
third timer/counter, T2, and one for the I²C interface. The interrupt
enable and interrupt priority registers are IE and IP.

### IE: Interrupt Enable Register

This register is located at address A8H. Refer to Table 3.

**IE SFR (A8H)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EA | ES1 | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

### IP: Interrupt Priority Register

This register is located at address B8H. Refer to Table 4.

**IP SFR (B8H)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | PS1 | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

### Table 3.  Description of IE Bits

| MNEMONIC | BIT | FUNCTION |
|---|---|---|
| EA | IE.7 | General enable/disable control:<br>0 = **NO** interrupt is enabled.<br>1 = **ANY** individually enabled interrupt will be accepted. |
| ES1 | IE.6 | Enable **bit-level I₂C I/O** interrupt |
| ET2 | IE.5 | Enable **Timer 2** interrupt |
| ES | IE.4 | Enable **Serial Port** interrupt |
| ET1 | IE.3 | Enable **Timer 1** interrupt |
| EX1 | IE.2 | Enable **External** interrupt 1 |
| ET0 | IE.1 | Enable **Timer 0** interrupt |
| EX0 | IE.0 | Enable **External** interrupt 0 |

### Table 4.  Description of IP Bits

| MNEMONIC | BIT | FUNCTION |
|---|---|---|
| – | IP.7 | **Reserved.** |
| PS1 | IP.6 | **Bit-level I²C** interrupt priority level |
| PT2 | IP.5 | **Timer 2** interrupt priority level |
| PS | IP.4 | **Serial Port** interrupt priority level |
| PT1 | IP.3 | **Timer 1** interrupt priority level |
| PX1 | IP.2 | **External Interrupt 1** priority level |
| PT0 | IP.1 | **Timer 0** interrupt priority level |
| PX0 | IP.0 | **External Interrupt 0** priority level |

The interrupt vector locations and the interrupt priorities are:

| Source | | Priority within Level |
|---|---|---|
| Vector | Address | |
| 0003H | IE0 | Highest |
| 002BH | TF2+EXF2 | |
| 0053H | SI (I²C) | |
| 000BH | TF0 | |
| 0013H | IE1 | |
| 001BH | TF1 | |
| 0023H | RI+TI | Lowest |

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

## RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-up, the voltage on V$_{DD}$ and RST must come up at the same time for a proper start-up.

## IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

## POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. The power-down mode can be terminated by a RESET in the same way as in the 80C51 or in addition by one of two external interrupts, INT0 or INT1. A termination with an external interrupt does not affect the internal data memory and does not affect the special function registers. This makes it possible to exit power-down without changing the port output levels. To terminate the power-down mode with an external interrupt $\overline{INT0}$ or $\overline{INT1}$ must be switched to level-sensitive and must be enabled. The external interrupt input signal $\overline{INT0}$ and $\overline{INT1}$ must be kept low until the oscillator has restarted and stabilized. An instruction following the instruction that puts the device in the power-down mode will be executed. A reset generated by the watchdog timer terminates the power-down mode in the same way as an external RESET, and only the contents of the on-chip RAM are preserved. The control bits for the reduced power modes are in the special function register PCON.

## DESIGN CONSIDERATIONS

At power-on, the voltage on V$_{DD}$ and RST must come up at the same time for a proper start-up.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory.

Table 5 shows the state of I/O ports during low current operating modes.

### Table 5. External Pin Status During Idle and Power-Down Modes

| MODE | PROGRAM MEMORY | ALE | $\overline{PSEN}$ | PORT 0 | PORT 1 | PORT 2 | PORT 3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power-down | External | 0 | 0 | Float | Data | Data | Data |

### ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

| PARAMETER | RATING | UNIT |
|---|---|---|
| Operating temperature under bias | 0 to +70, or −40 to +85 | °C |
| Storage temperature range | −65 to +150 | °C |
| Voltage on any other pin to V$_{SS}$ | −0.5 to V$_{DD}$ +0.5 | V |
| Input, output current on any two pins | ±10 | mA |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1.0 | W |

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V$_{SS}$ unless otherwise noted.

## 80C51 8-bit microcontrollers
## 16K/32K, 512 OTP, I²C, watchdog timer

## 87C524/87C528

### DC ELECTRICAL CHARACTERISTICS

$T_{amb}$ = 0°C to +70°C ($V_{DD}$ = 5 V ±10%), −40°C to +85°C ($V_{DD}$ = 5 V ±10%), $V_{SS}$=0 V

| SYMBOL | PARAMETER | PART TYPE | TEST CONDITIONS | LIMITS MIN | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage, except $\overline{EA}$, P1.6/SCL, P1.7/SDA | 0°C to 70°C<br>−40°C to +85°C | | −0.5<br>−0.5 | $0.2V_{CC}$−0.1<br>$0.2V_{CC}$−0.15 | V<br>V |
| $V_{IL1}$ | Input low voltage to $\overline{EA}$ | 0°C to 70°C<br>−40°C to +85°C | | 0<br>0 | $0.2V_{CC}$−0.3<br>$0.2V_{CC}$−0.35 | V<br>V |
| $V_{IL2}$ | Input low voltage to P1.6/SCL, P1.7/SDA[5] | | | −0.5 | 0.3 V | V |
| $V_{IH}$ | Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA | 0°C to 70°C<br>−40°C to +85°C | | $0.2V_{CC}$+0.9<br>$0.2V_{CC}$+1.0 | $V_{CC}$+0.5<br>$V_{CC}$+0.5 | V<br>V |
| $V_{IH1}$ | Input high voltage, XTAL1, RST | 0°C to 70°C<br>−40°C to +85°C | | $0.7V_{CC}$<br>$0.7V_{CC}$+0.1 | $V_{CC}$+0.5<br>$V_{CC}$+0.5 | V<br>V |
| $V_{IH2}$ | Input high voltage, P1.6/SCL, P1.7/SDA[5] | | | 3.0 | 6.0 | V |
| $V_{OL}$ | Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA[1] | | $I_{OL}$ = 1.6 mA[1] | | 0.45 | V |
| $V_{OL1}$ | Output low voltage, port 0, ALE, $\overline{PSEN}$[1] | | $I_{OL}$ = 3.2 mA[1] | | 0.45 | V |
| $V_{OL2}$ | Output low voltage, P1.6/SCL, P1.7/SDA | | $I_{OL}$ = 3.0 mA[1] | | 0.4 | V |
| $V_{OH}$ | Output high voltage, ports 1, 2, 3 | | $I_{OH}$ = −60 µA<br>$I_{OH}$ = −25 µA | 2.4<br>$0.75V_{CC}$ | | V<br>V |
| $V_{OH1}$ | Output high voltage, Port 0 in external bus mode, ALE, $\overline{PSEN}$, RST | | $I_{OH}$ = −800 µA<br>$I_{OH}$ = −300 µA | 2.4<br>$0.75V_{CC}$ | | V<br>V |
| $I_{IL}$ | Logical 0 input current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA | 0°C to 70°C<br>−40°C to +85°C | $V_{IN}$ = 0.45 V | | −50<br>−75 | µA<br>µA |
| $I_{TL}$ | Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA | 0°C to 70°C<br>−40°C to +85°C | See Note 3 | | −650<br>−750 | µA<br>µA |
| $I_{IL1}$ | Input leakage current, port 0 | | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | | ±10 | µA |
| $I_{IL2}$ | Input leakage current, P1.6/SCL, P1.7/SDA | | 0 V<Vi<6.0 V<br>0 V<$V_{CC}$<6.0 V | | ±10 | µA<br>µA |
| $I_{CC}$ | Power supply current: | | See Note 4 | | | |
| | Active mode @ 16 MHz | 0ºC to 70ºC<br>−40ºC to +85ºC | | | 25<br>35 | mA |
| | Idle mode @ 16 MHz | 0ºC to 70ºC<br>−40ºC to +85ºC | | | 5<br>6 | mA |
| | Power down mode | | | | 50 | µA |
| $R_{RST}$ | Internal reset pull-down resistor | | | 50 | 300 | kΩ |
| $C_{IO}$ | Pin Capacitance | | | | 10 | pF |

**NOTES:**
1. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port and port 2 pins when these pins make 1-to-0 transactions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows: 10 mA per port pin, port 0 total (all bits) 26 mA, ports 1, 2, and total each (all bits) 15 mA.
2. Capacitive loading on Ports 0 and 2 may cause the $V_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
3. Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when $V_{IN}$ is approximately 2 V.
4. See Figures 10 through 13 for $I_{CC}$ test conditions.
5. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5 V will be recognized as a logic 0 while an input voltage above 3.0 V will be recognized as a logic 1.

## AC ELECTRICAL CHARACTERISTICS[1, 2]

| SYMBOL | FIGURE | PARAMETER | | 16MHz CLOCK | | VARIABLE CLOCK | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $1/t_{CLCL}$ | 1 | Oscillator frequency: **Speed Versions** 87C528 P878C528EXX | | | | 3.5 | 16 | MHz |
| $t_{LHLL}$ | 1 | ALE pulse width | | 85 | | $2t_{CLCL}-40$ | | ns |
| $t_{AVLL}$ | 1 | Address valid to ALE low | | 8 | | $t_{CLCL}-55$ | | ns |
| $t_{LLAX}$ | 1 | Address hold after ALE low | | 28 | | $t_{CLCL}-35$ | | ns |
| $t_{LLIV}$ | 1 | ALE low to valid instruction in | | | 150 | | $4t_{CLCL}-100$ | ns |
| $t_{LLPL}$ | 1 | ALE low to $\overline{PSEN}$ low | | 23 | | $t_{CLCL}-40$ | | ns |
| $t_{PLPH}$ | 1 | $\overline{PSEN}$ pulse width | | 143 | | $3t_{CLCL}-45$ | | ns |
| $t_{PLIV}$ | 1 | $\overline{PSEN}$ low to valid instruction in | | | 83 | | $3t_{CLCL}-105$ | ns |
| $t_{PXIX}$ | 1 | Input instruction hold after $\overline{PSEN}$ | | 0 | | 0 | | ns |
| $t_{PXIZ}$ | 1 | Input instruction float after $\overline{PSEN}$ | | | 38 | | $t_{CLCL}-25$ | ns |
| $t_{AVIV}$ | 1 | Address to valid instruction in | | | 208 | | $5t_{CLCL}-105$ | ns |
| $t_{PLAZ}$ | 1 | $\overline{PSEN}$ low to address float | | | 10 | | 10 | ns |
| **Data Memory** | | | | | | | | |
| $t_{RLRH}$ | 2, 3 | $\overline{RD}$ pulse width | | 275 | | $6t_{CLCL}-100$ | | ns |
| $t_{WLWH}$ | 2, 3 | $\overline{WR}$ pulse width | | 275 | | $6t_{CLCL}-100$ | | ns |
| $t_{RLDV}$ | 2, 3 | $\overline{RD}$ low to valid data in | | | 148 | | $5t_{CLCL}-165$ | ns |
| $t_{RHDX}$ | 2, 3 | Data hold after $\overline{RD}$ | | 0 | | 0 | | ns |
| $t_{RHDZ}$ | 2, 3 | Data float after $\overline{RD}$ | | | 55 | | $2t_{CLCL}-70$ | ns |
| $t_{LLDZ}$ | 2, 3 | ALE low to valid data in | | | 350 | | $8t_{CLCL}-150$ | ns |
| $t_{AVDV}$ | 2, 3 | Address to valid data in | | | 398 | | $9t_{CLCL}-165$ | ns |
| $t_{LLWL}$ | 2, 3 | ALE low to $\overline{RD}$ or $\overline{WR}$ low | | 138 | 238 | $3t_{CLCL}-50$ | $3t_{CLCL}+50$ | ns |
| $t_{AVWL}$ | 2, 3 | Address valid to $\overline{WR}$ low or $\overline{RD}$ low | | 120 | | $4t_{CLCL}-130$ | | ns |
| $t_{QVWX}$ | 2, 3 | Data valid to $\overline{WR}$ transition | | 3 | | $t_{CLCL}-60$ | | ns |
| $t_{WHQX}$ | 2, 3 | Data hold after $\overline{WR}$ | | 13 | | $t_{CLCL}-50$ | | ns |
| $t_{RLAZ}$ | 2, 3 | $\overline{RD}$ low to address float | | | 0 | | 0 | ns |
| $t_{WHLH}$ | 2, 3 | $\overline{RD}$ or $\overline{WR}$ high to ALE high | | 23 | 103 | $t_{CLCL}-40$ | $t_{CLCL}+40$ | ns |
| **External Clock** | | | | | | | | |
| $t_{CHCX}$ | 6 | High time | | 20 | | 20 | | ns |
| $t_{CLCX}$ | 6 | Low time | | 20 | | 20 | | ns |
| $t_{CLCH}$ | 6 | Rise time | | | 20 | | 20 | ns |
| $t_{CHCL}$ | 6 | Fall time | | | 20 | | 20 | ns |
| **Shift Register** | | | | | | | | |
| $t_{XLXL}$ | 4 | Serial port clock cycle time | | 750 | | $12t_{CLCL}$ | | ns |
| $t_{QVXH}$ | 4 | Output data setup to clock rising edge | | 492 | | $10t_{CLCL}-133$ | | ns |
| $t_{XHQX}$ | 4 | Output data hold after clock rising edge | | 8 | | $2t_{CLCL}-117$ | | ns |
| $t_{XHDX}$ | 4 | Input data hold after clock rising edge | | 0 | | 0 | | ns |
| $t_{XHDV}$ | 4 | Clock rising edge to input data valid | | | 492 | | $10t_{CLCL}-133$ | ns |

**NOTES:**
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.

## AC ELECTRICAL CHARACTERISTICS – I$^2$C INTERFACE

| SYMBOL | PARAMETER | INPUT | OUTPUT | I$^2$C SPECIFICATION |
|---|---|---|---|---|
| **SCL TIMING CHARACTERISTICS** | | | | |
| $t_{HD;STA}$ | START condition hold time | $\geq 14\ t_{CLCL}$[1] | Note 2 | $\geq 4.0\mu s$ |
| $t_{LOW}$ | SCL LOW time | $\geq 16\ t_{CLCL}$ | Note 2 | $\geq 4.7\mu s$ |
| $t_{HIGH}$ | SCL HIGH time | $\geq 14\ t_{CLCL}$[1] | $\geq 80\ t_{CLCL}$[3] | $\geq 4.0\mu s$ |
| $t_{RC}$ | SCL rise time | $\leq 1\mu s$[1] | Note 5 | $\leq 1.0\mu s$ |
| $t_{FC}$ | SCL fall time | $\leq 0.3\mu s$[1] | $\leq 0.3\mu s$[6] | $\leq 0.3\mu s$ |
| **SDA TIMING CHARACTERISTICS** | | | | |
| $t_{SU;DAT1}$ | Data set-up time | $\geq 250ns$ | Note 2 | $\geq 250ns$ |
| $t_{HD;DAT}$ | Data hold time | $\geq 0ns$ | Note 2 | $\geq 0ns$ |
| $t_{SU;STA}$ | Repeated START set-up time | $\geq 14\ t_{CLCL}$[1] | Note 2 | $\geq 4.7\mu s$ |
| $t_{SU;STO}$ | STOP condition set-up time | $\geq 14\ t_{CLCL}$[1] | Note 2 | $\geq 4.0\mu s$ |
| $t_{BUF}$ | Bus free time | $\geq 14\ t_{CLCL}$[1] | Note 2 | $\geq 4.7\mu s$ |
| $t_{RD}$ | SDA rise time | $\leq 1\mu s$[4] | Note 5 | $\leq 1.0\mu s$ |
| $t_{FD}$ | SDA fall time | $\leq 0.3\mu s$[4] | $\leq 0.3\mu s$[6] | $\leq 0.3\mu s$ |

**NOTES:**

1. At $f_{CLK}$ = 3.5MHz, this evaluates to $14 \times 286ns = 4\mu s$, i.e., the bit-level I$^2$C interface can respond to the I$^2$C protocol for $f_{CLK} \geq 3.5$ MHz.
2. This parameter is determined by the user software, it has to comply with the I$^2$C.
3. This value gives the autoclock pulse length which meets the I$^2$C specification for the specified XTAL clock frequency range. Alternatively, the SCL pulse may be timed by software.
4. Spikes on SDA and SCL lines with a duration of less than $4 \times f_{CLK}$ will be filtered out.
5. The rise time is determined by the external bus line capacitance and pull-up resistor, it must be $\leq 1\mu s$.
6. The maximum capacitance on bus lines SDA and SCL is 400pF.

## 80C51 8-bit microcontrollers
### 16K/32K, 512 OTP, I²C, watchdog timer

**87C524/87C528**

### EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always
't' (= time). The other characters, depending on their positions,
indicate the name of a signal or the logical status of that signal. The
designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I  – Instruction (program memory contents)
L – Logic level low, or ALE

P – $\overline{\text{PSEN}}$
Q – Output data
R – $\overline{\text{RD}}$ signal
t  – Time
V – Valid
W– $\overline{\text{WR}}$ signal
X – No longer a valid logic level
Z – Float

**Examples:** $t_{AVLL}$ = Time for address valid to ALE low.
$t_{LLPL}$ = Time for ALE low to $\overline{\text{PSEN}}$ low.
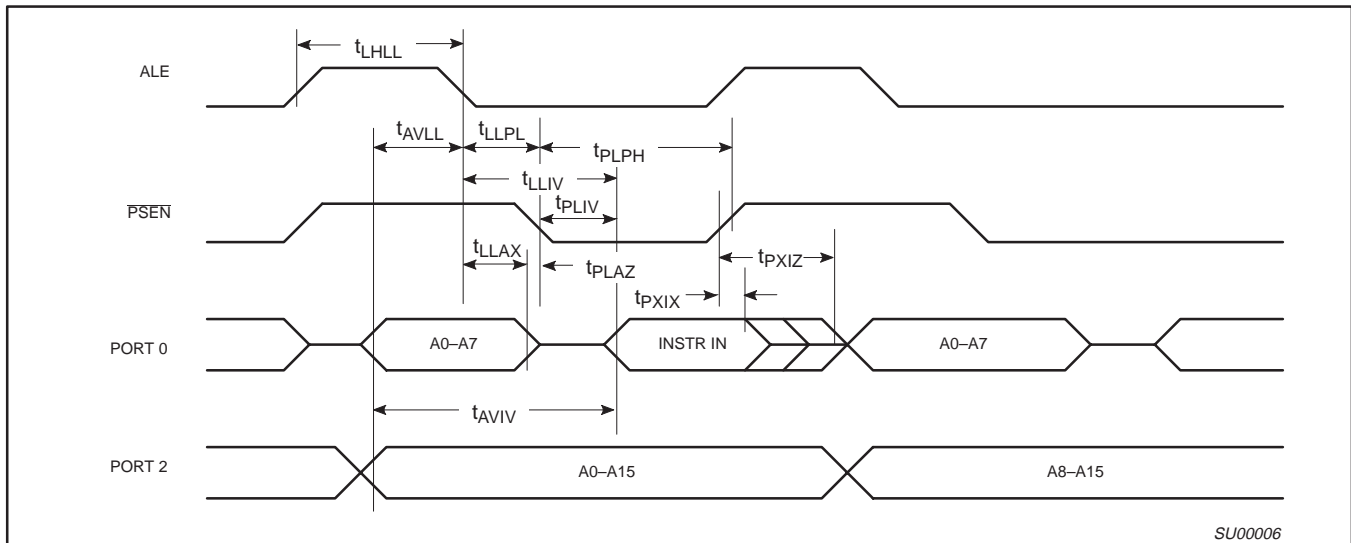


**Figure 1.  External Program Memory Read Cycle**
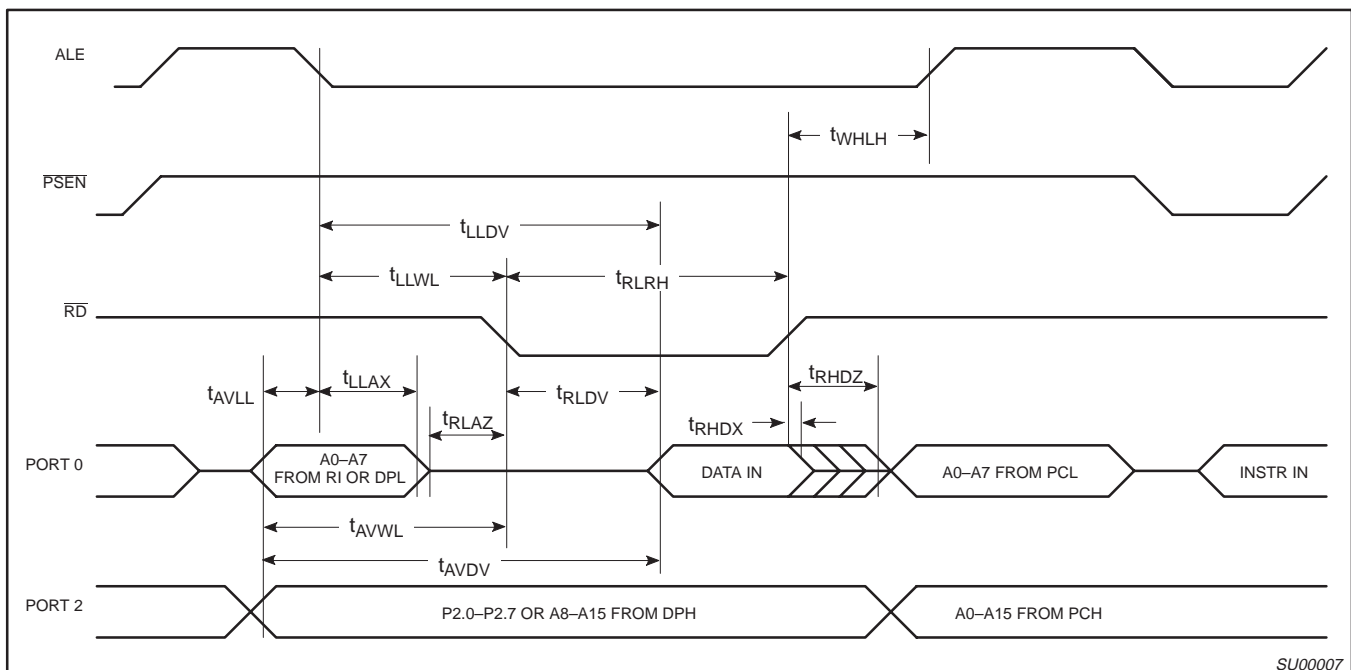


**Figure 2.  External Data Memory Read Cycle**

## 80C51 8-bit microcontrollers
### 16K/32K, 512 OTP, I²C, watchdog timer
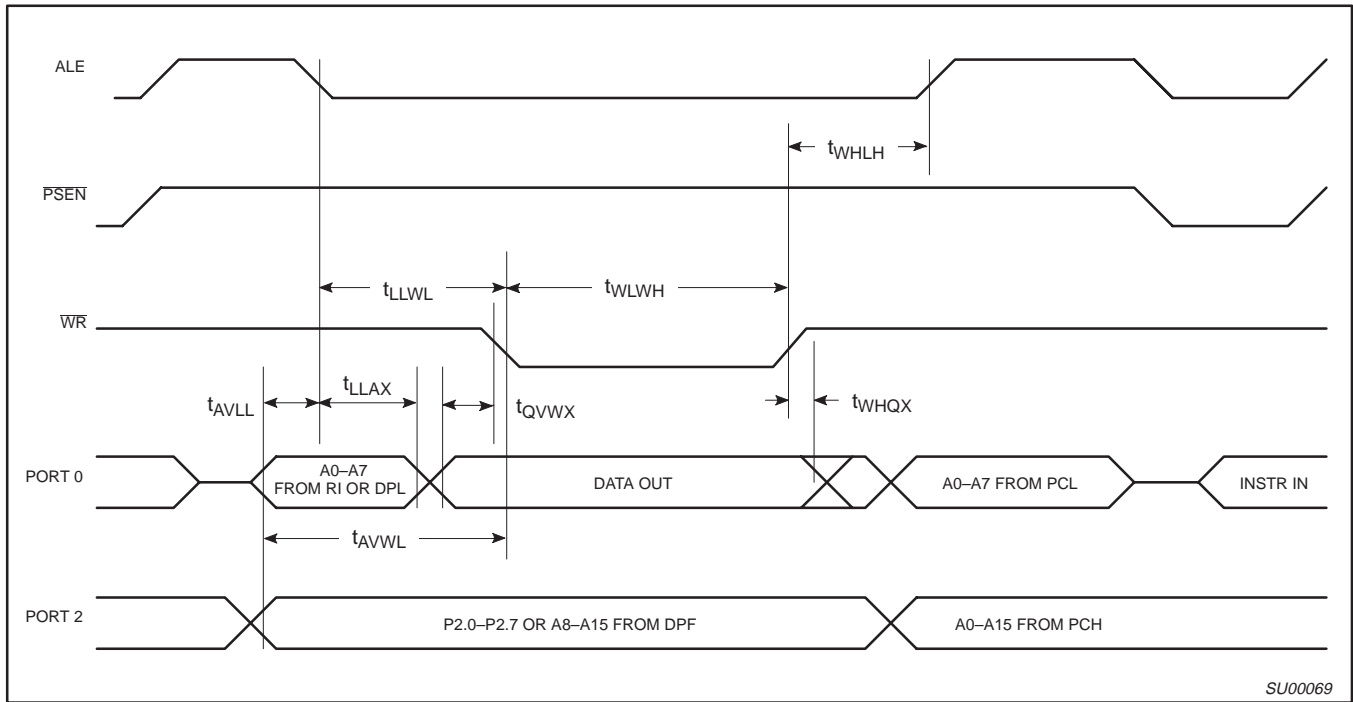
**Figure 3.  External Data Memory Write Cycle**
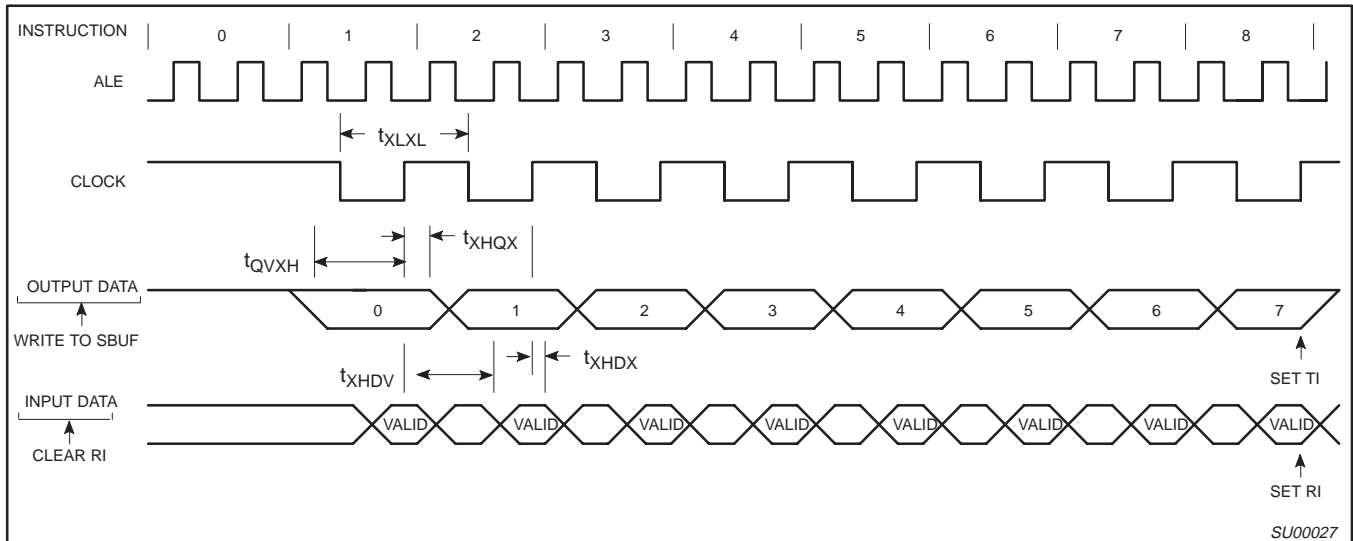


**Figure 4.  Shift Register Mode Timing**
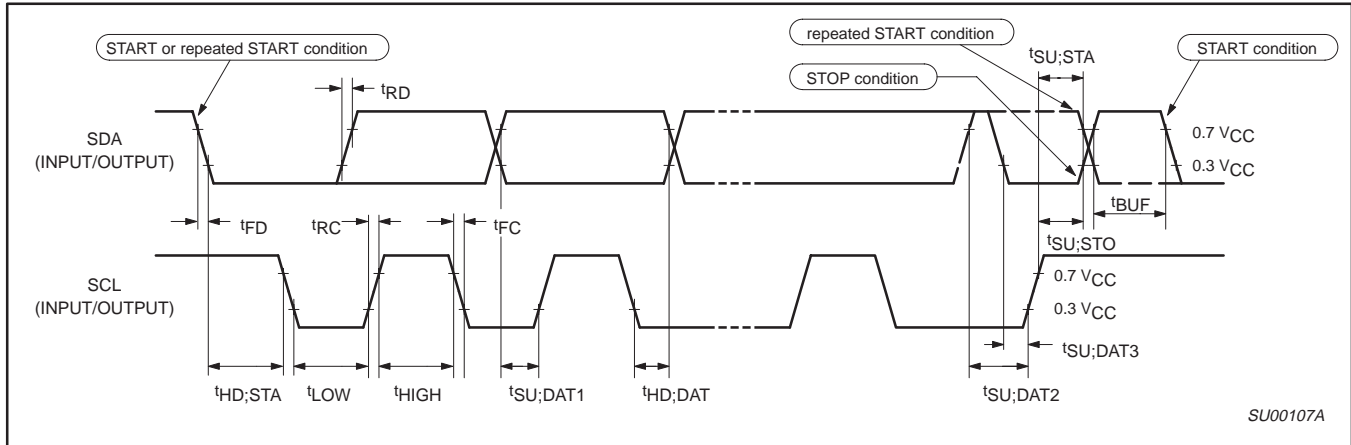
**Figure 5.  Timing SIO1 (I$^2$C) Interface**
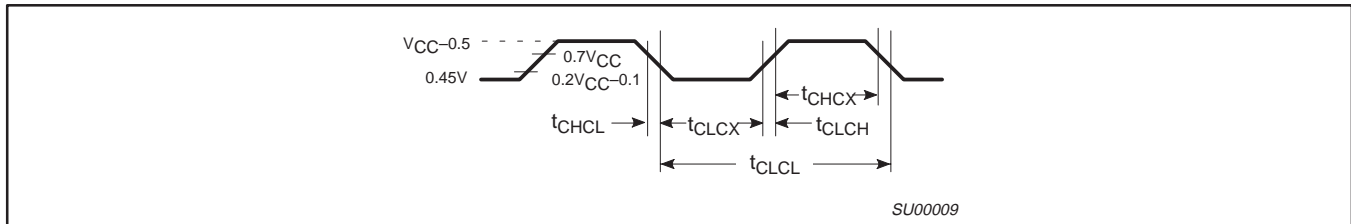


**Figure 6.  External Clock Drive**
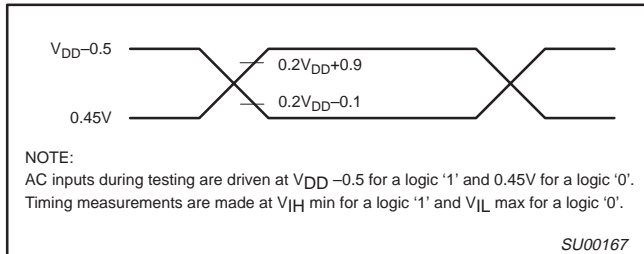


NOTE:
AC inputs during testing are driven at $V_{DD}$ −0.5 for a logic '1' and 0.45V for a logic '0'.
Timing measurements are made at $V_{IH}$ min for a logic '1' and $V_{IL}$ max for a logic '0'.

SU00167

**Figure 7.  AC Testing Input/Output**
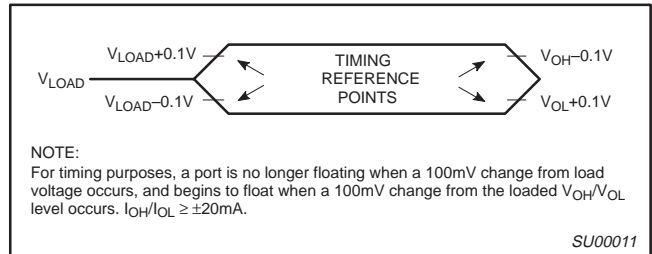


NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OH}/I_{OL} \geq \pm20mA$.

SU00011

**Figure 8.  Float Waveform**
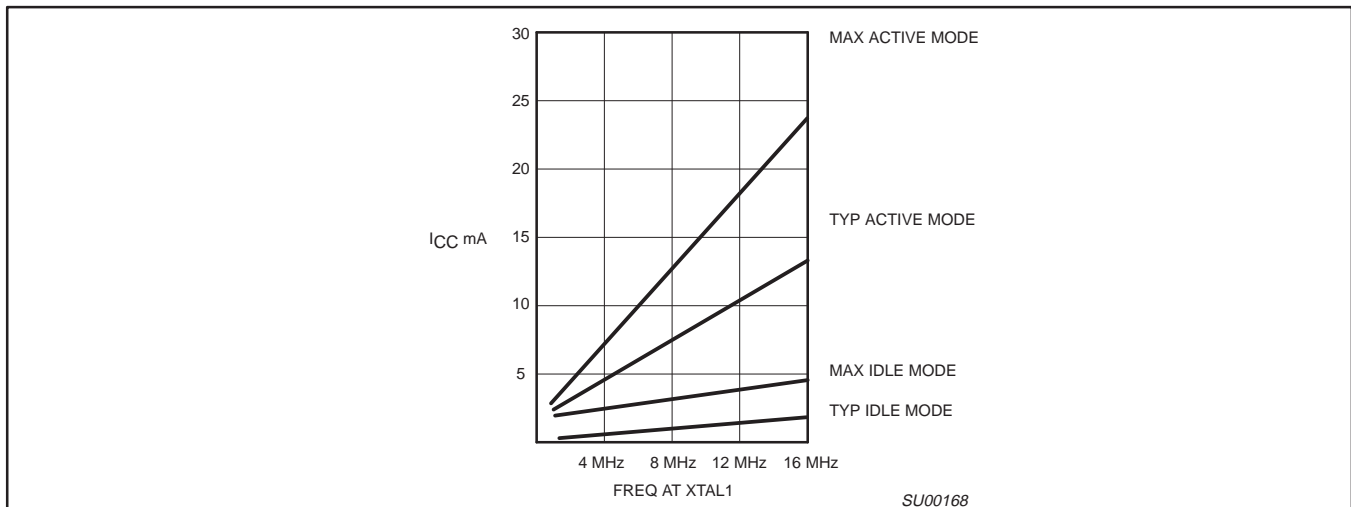


**Figure 9.  I$_{CC}$ vs. FREQ.**
**Valid only within frequency specifications of the device under test**
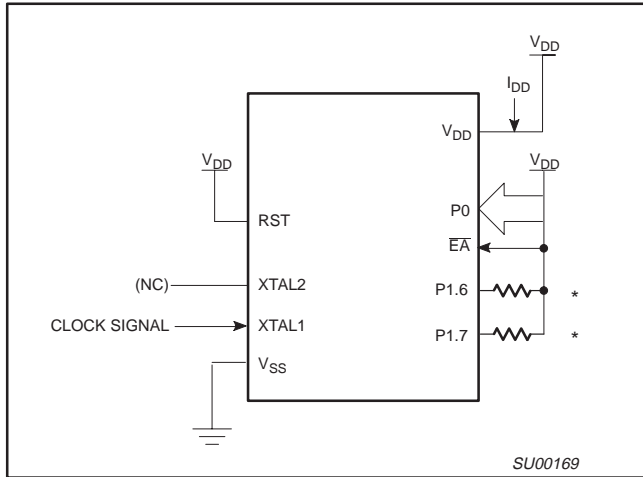
**Figure 10. I_DD Test Condition, Active Mode**
**All other pins are disconnected**
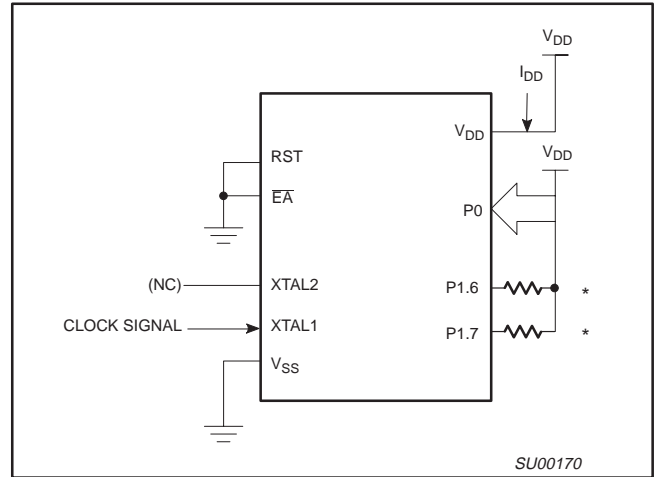


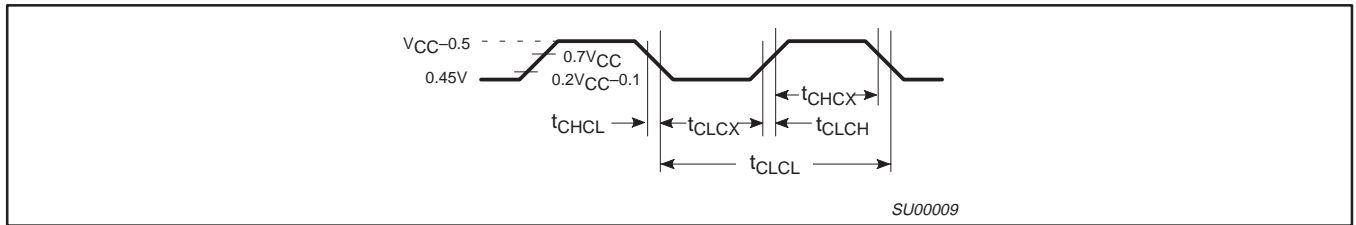**Figure 11. I_DD Test Condition, Idle Mode**
**All other pins are disconnected**



**Figure 12. Clock Signal Waveform for**
**I_DD Tests in Active and Idle Modes**
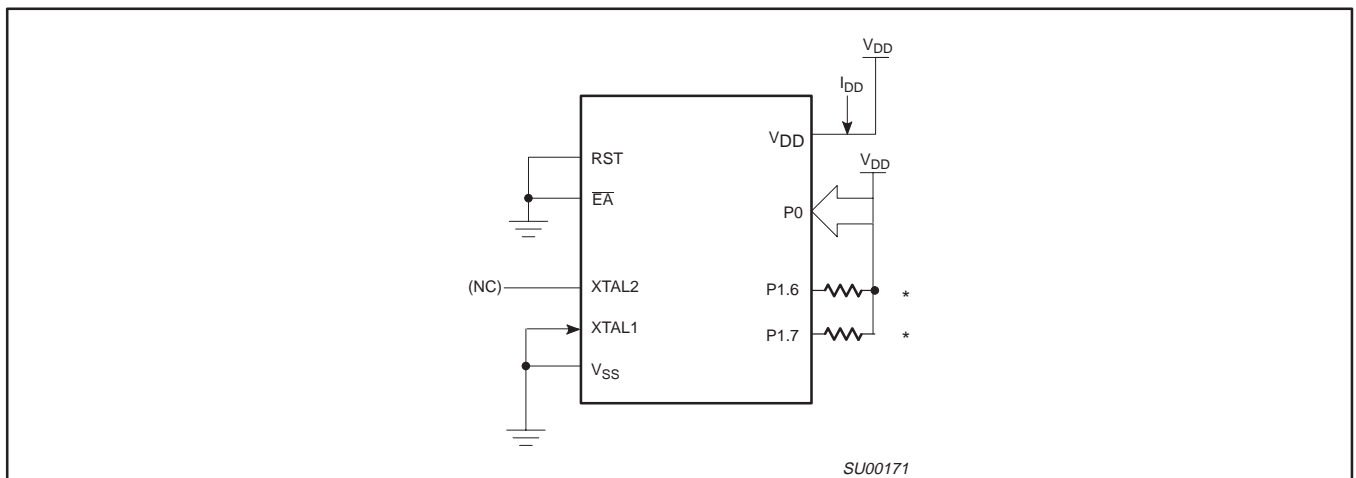**t_CLCH = t_CHCL = 5ns**



**Figure 13. I_DD Test Condition, Power Down Mode**
**All other pins are disconnected. V_DD = 2V to 5.5V**

**NOTE:**
* Ports 1.6 and 1.7 should be connected to V_DD through resistors of sufficiently high value such that the sink current into these pins does not exceed the I_OL1 specifications.

## EPROM CHARACTERISTICS FOR 87C528

The 87C528 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for $V_{PP}$ (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C528 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C528 manufactured by Philips.

Table 6 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 14 and 15. Figure 16 shows the circuit configuration for normal program memory verification.

### Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 14. Note that the 87C528 is running with a 4 to 6MHz oscillator The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1, 2 and 3, as shown in Figure 14. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 6 are held at the 'Program Code Data' levels indicated in Table 6. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 15.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 3FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to 90 above the maximum specified $V_{PP}$ level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The $V_{PP}$ source should be well regulated and free of glitches and overshoot.

### Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1, 2 and 3 as shown in Figure 16. The other pins are held at the 'Verify Code Data' levels indicated in Table 6. The contents of the address location will be emitted on port 0. External pull ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

### Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031 H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips
(031H) = 9BH indicates 87C528

## Program Lock Bits

The 87C528 has 3 programmable lock bits that will provide different levels of protection for the on-chip code and data (see Table 7).

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

## Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 6, and which satisfies the timing specifications, is suitable.

### Table 6. EPROM Programming Modes

| MODE | RST | PSEN | ALE/$\overline{PROG}$ | $\overline{EA}/V_{PP}$ | P2.7 | P2.6 | P3.7 | P3.6 |
|---|---|---|---|---|---|---|---|---|
| Read signature | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Program code data | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 1 |
| Verify code data | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| Pgm encryption table | 1 | 0 | 0* | $V_{PP}$ | 1 | 0 | 1 | 0 |
| Pgm lock bit 1 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 1 | 1 |
| Pgm lock bit 2 | 1 | 0 | 0* | $V_{PP}$ | 1 | 1 | 0 | 0 |
| Pgm lock bit 3 | 1 | 0 | 0* | $V_{PP}$ | 0 | 1 | 0 | 1 |

**NOTES:**

1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. $V_{PP}$ = 12.75 V ±0.25 V.
3. Vcc = 5 V ±10% during programming and verification.
* ALE/$\overline{PROG}$ receives 25 programming pulses while $V_{PP}$ is held at 12.75 V. Each programming pulse is low for 100 µs (±10 µs) and high for a minimum of 10 µs.

80C51 8-bit microcontrollers
16K/32K, 512 OTP, I$^2$C, watchdog timer

87C524/87C528

## EPROM CHARACTERISTICS FOR 87C524

The 87C524 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V$_{PP}$ (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses.

The 87C524 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C524 manufactured by Philips.

Table 6 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 14 and 15. Figure 16 shows the circuit configuration for normal program memory verification.

### Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 14. Note that the 87C524 is running with a 4 to 6 MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1, 2 and 3, as shown in Figure 14. The code byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 specified in Table 6 are held at the 'Program Code Data' levels indicated in Table 6. The ALE/$\overline{PROG}$ is pulsed low 25 times as shown in Figure 15.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 3FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the $\overline{EA}$/V$_{PP}$ pin must not be allowed to go above the maximum specified V$_{PP}$ level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V$_{PP}$ source should be well regulated and free of glitches and overshoot.

### Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1, 2 and 3 as shown

in Figure 16. The other pins are held at the 'Verify Code Data' levels indicated in Table 6. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

### Program Lock Bits

The 87C524 has 3 programmable lock bits that will provide different levels of protection for the on-chip code and data (see Table 7).

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

### Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by
        Philips
(031H) =  9DH indicates 87C524

## Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 6, and which satisfies the timing specifications, is suitable.

## Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm$^2$. Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm$^2$ rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

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™Trademark phrase of Intel Corporation.

### Table 7. Program Lock Bits

| PROGRAM LOCK BITS[1,2] | | | |
|---|---|---|---|
| | LB1 | LB2 | LB3 | PROTECTION DESCRIPTION |
| 1 | U | U | U | No Program Lock features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.) |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from Internal memory, EA is jumped and latched on Reset, and further programming of the EPROM Is disabled. |
| 3 | P | P | U | Same as 2, also verify is disabled. |
| 4 | P | P | P | Same as 3, external execution is disabled. Internal data RAM is not accessible. |

**NOTES:**
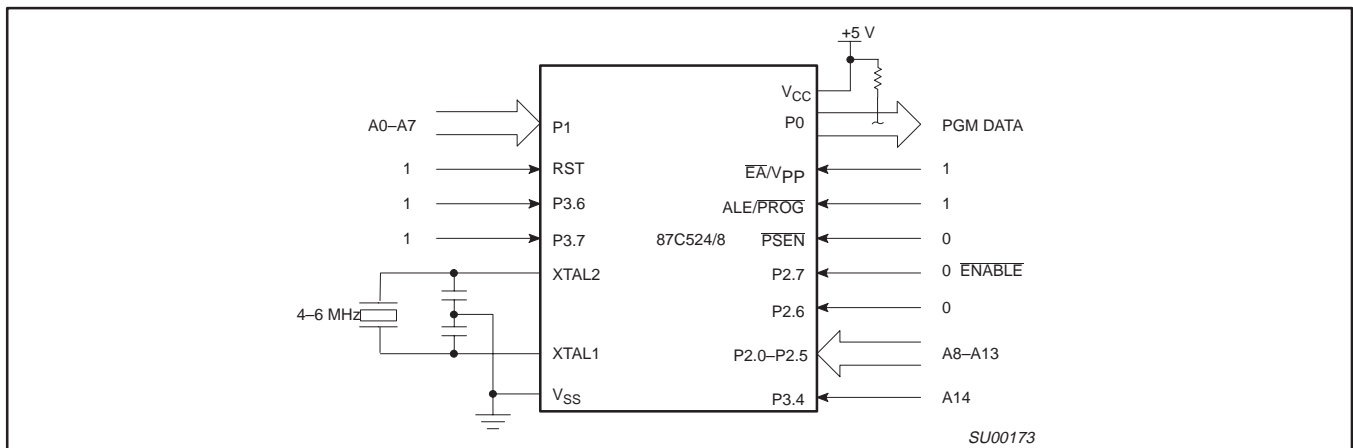1. P - programmed.  U - unprogrammed.
2. Any other combination of the lock bits is not defined.
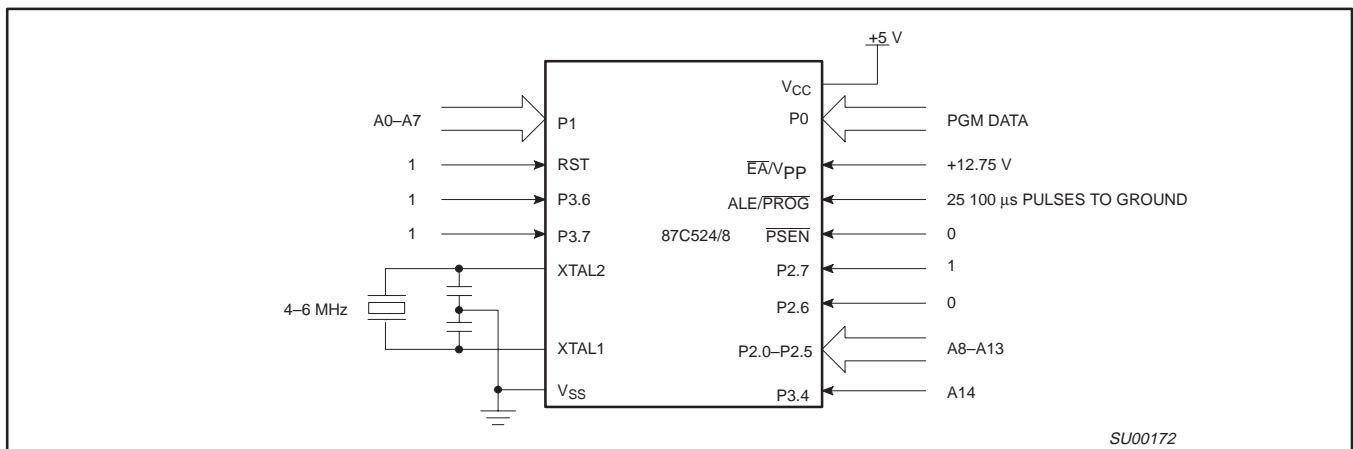


**Figure 14.  Programming Configuration**
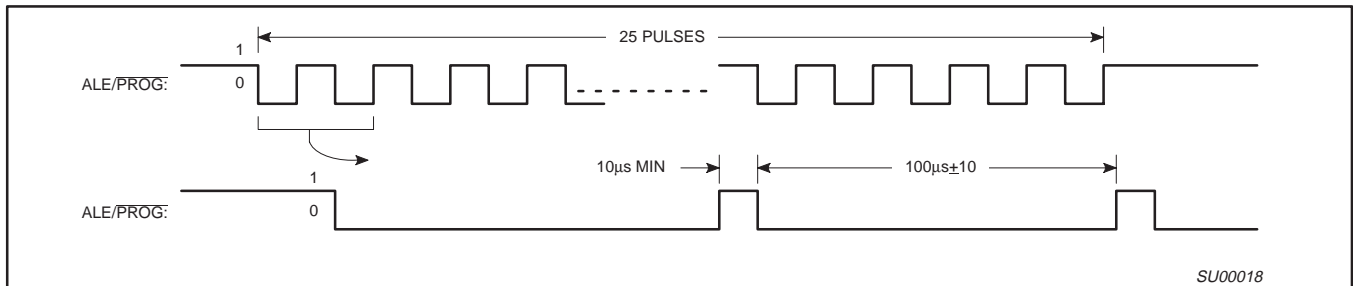


**Figure 15.  $\overline{\text{PROG}}$ Waveform**
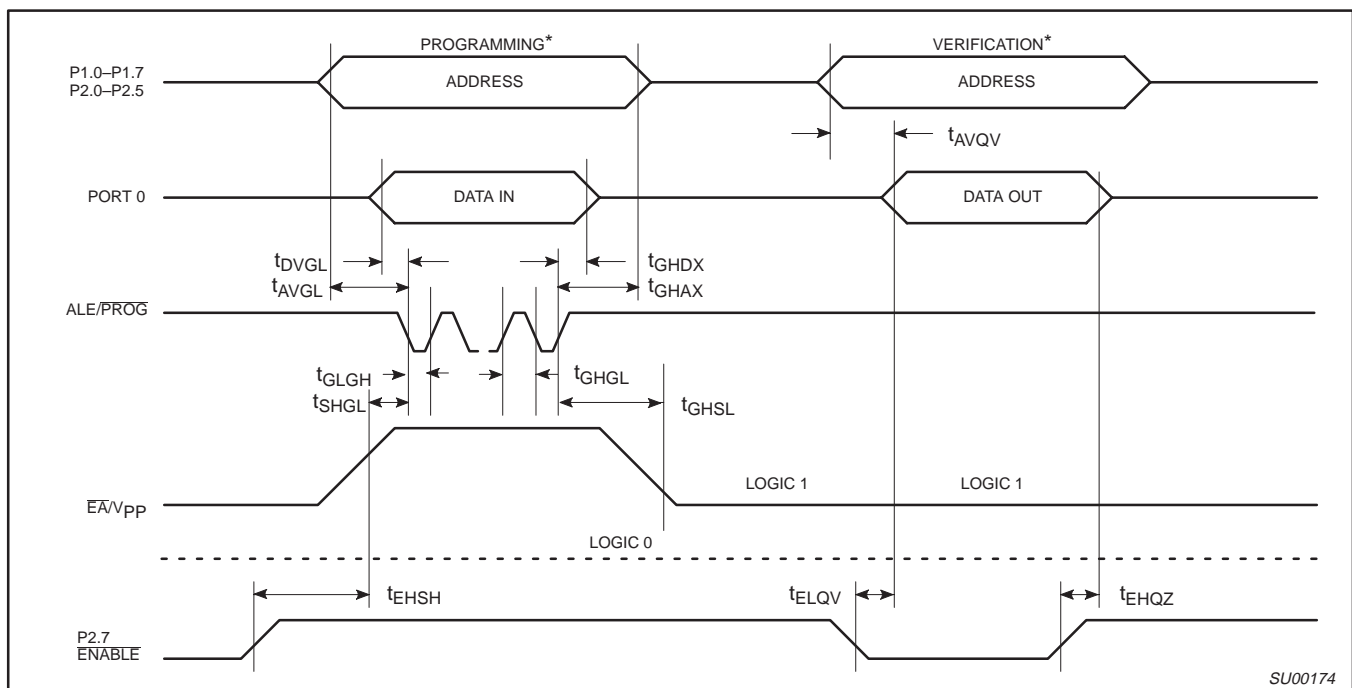


**Figure 16.  Program Verification**

## EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb}$ = 21°C to +27°C, Vcc = 5 V±10%, $V_{SS}$ = 0 V (See Figure 17)

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{PP}$ | Programming supply voltage | 12.5 | 13.0 | V |
| $I_{PP}$ | Programming supply current | | 50 | mA |
| $1/t_{CLCL}$ | Oscillator frequency | 4 | 6 | MHz |
| $t_{AVGL}$ | Address setup to $\overline{PROG}$ low | $48t_{CLCL}$ | | |
| $t_{GHAX}$ | Address hold after $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{DVGL}$ | Data setup to $\overline{PROG}$ low | $48t_{CLCL}$ | | |
| $t_{GHDX}$ | Data hold after $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{EHSH}$ | P2.7 ($\overline{ENABLE}$) high to $V_{PP}$ | $48t_{CLCL}$ | | |
| $t_{SHGL}$ | $V_{PP}$ setup to $\overline{PROG}$ low | 10 | | μs |
| $t_{GHSL}$ | $V_{PP}$ hold after $\overline{PROG}$ | 10 | | μs |
| $t_{GLGH}$ | $\overline{PROG}$ width | 90 | 110 | μs |
| $t_{AVQV}$ | Address to data valid | | $48t_{CLCL}$ | |
| $t_{ELQZ}$ | $\overline{ENABLE}$ low to data valid | | $48t_{CLCL}$ | |
| $t_{EHQZ}$ | Data float after $\overline{ENABLE}$ | 0 | $48t_{CLCL}$ | |
| $t_{GHGL}$ | $\overline{PROG}$ high to $\overline{PROG}$ low | 10 | | μs |



**NOTE:**
* FOR PROGRAMMING VERIFICATION SEE FIGURE 14.
  FOR VERIFICATION CONDITIONS SEE FIGURE 16.

**Figure 17. EPROM Programing and Verification**

Purchase of Philips I2C components conveys a license under the Philips' I2C patent to use the components in the I2C system provided the system conforms to the I2C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

## 80C51 8-bit microcontrollers
### 16K/32K, 512 OTP, I$^2$C, watchdog timer

**87C524/87C528**

**DIP40:** plastic dual in-line package; 40 leads (600 mil)

SOT129-1
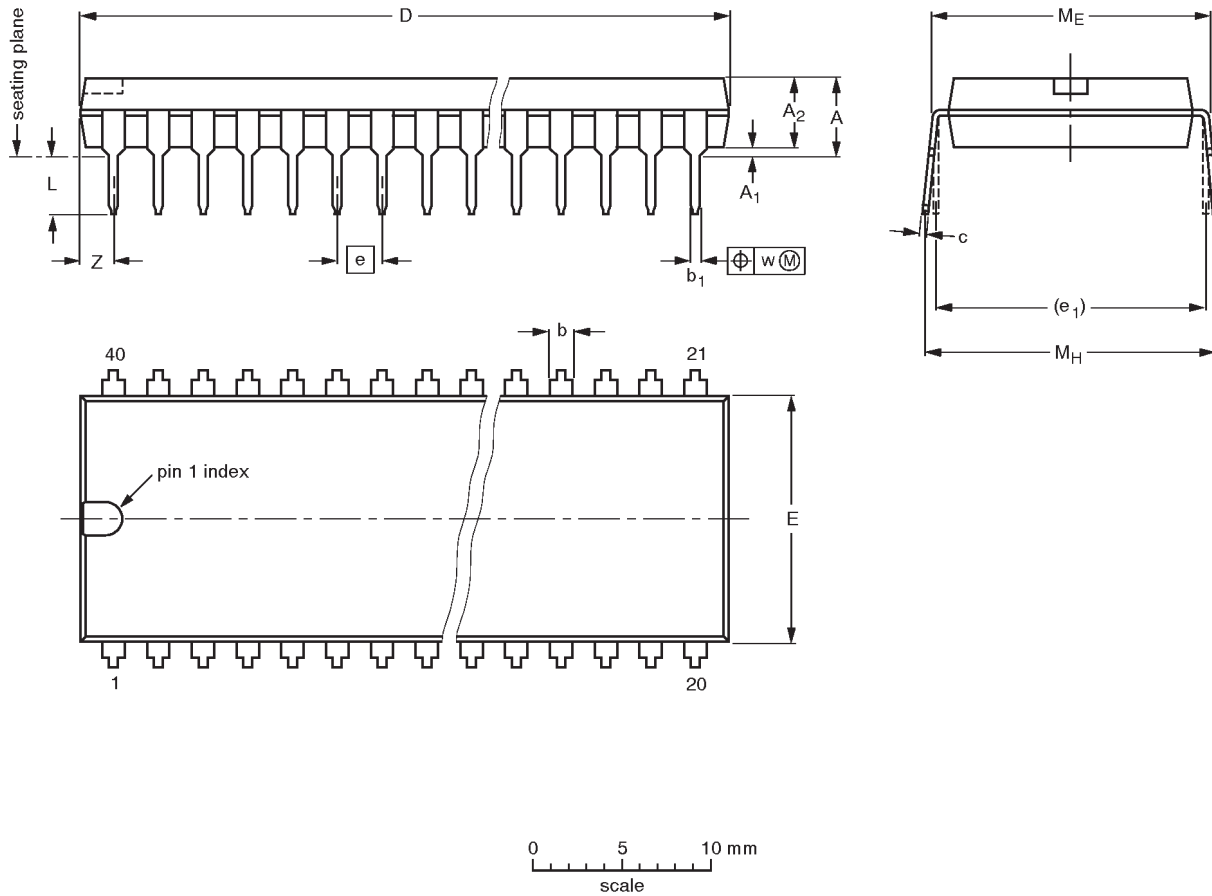


**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A$_1$ min. | A$_2$ max. | b | b$_1$ | c | D [1] | E [1] | e | e$_1$ | L | M$_E$ | M$_H$ | w | Z [1] max. |
|------|--------|------------|------------|---|-------|---|-------|-------|---|-------|---|-------|-------|---|------------|
| mm | 4.7 | 0.51 | 4.0 | 1.70 1.14 | 0.53 0.38 | 0.36 0.23 | 52.50 51.50 | 14.1 13.7 | 2.54 | 15.24 | 3.60 3.05 | 15.80 15.24 | 17.42 15.90 | 0.254 | 2.25 |
| inches | 0.19 | 0.020 | 0.16 | 0.067 0.045 | 0.021 0.015 | 0.014 0.009 | 2.067 2.028 | 0.56 0.54 | 0.10 | 0.60 | 0.14 0.12 | 0.62 0.60 | 0.69 0.63 | 0.01 | 0.089 |

**Note**

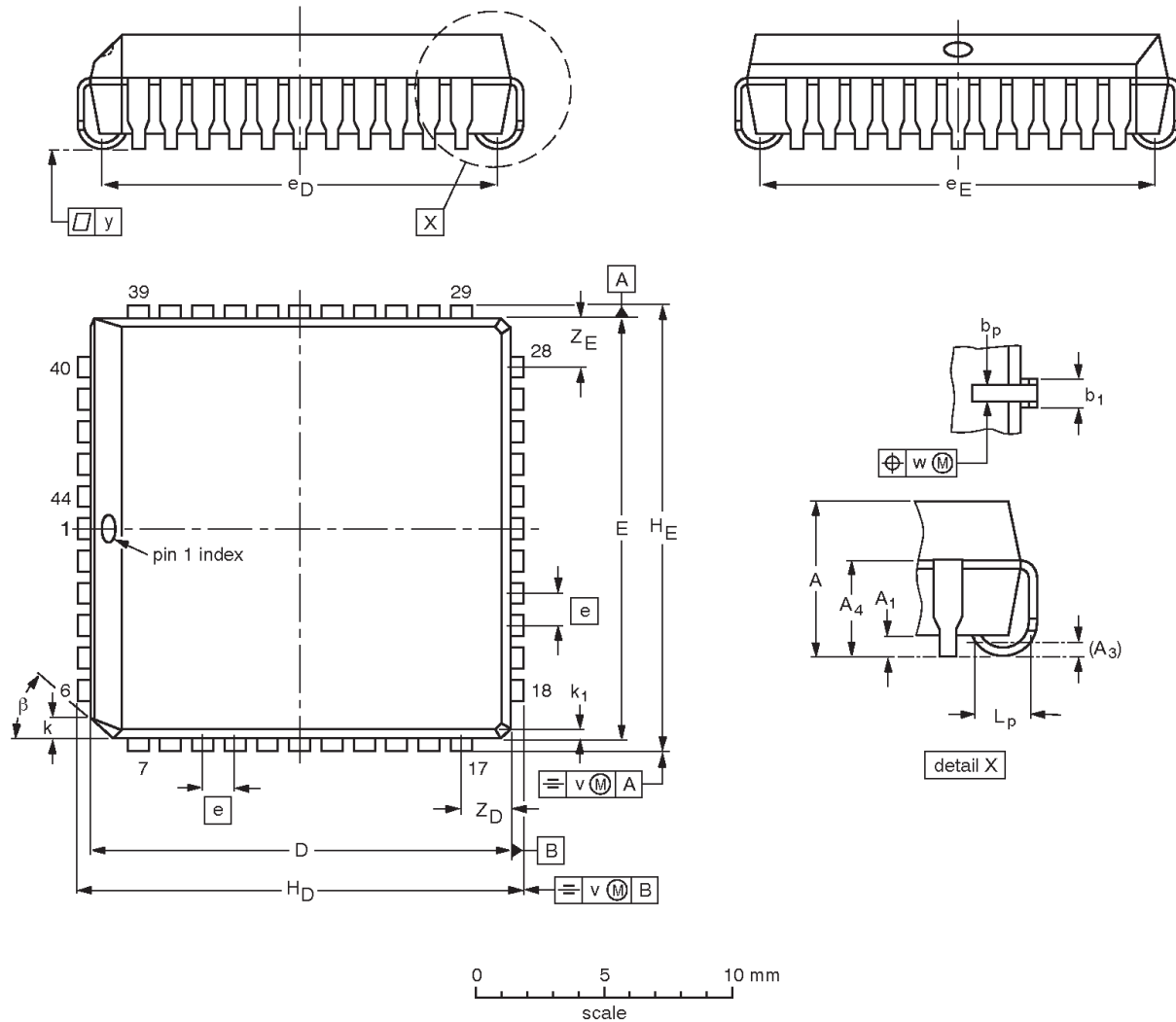1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|------|---------------------|------------|
| | IEC | JEDEC | EIAJ | | |
| SOT129-1 | 051G08 | MO-015AJ | | | ~~92-11-17~~ 95-01-14 |

# 80C51 8-bit microcontrollers
## 16K/32K, 512 OTP, I²C, watchdog timer

**PLCC44:    plastic leaded chip carrier; 44 leads**                                          **SOT187-2**



**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT | A | A₁ min. | A₃ | A₄ max. | b_p | b₁ | D(1) | E(1) | e | e_D | e_E | H_D | H_E | k | k₁ max. | L_p | v | w | y | Z_D(1) max. | Z_E(1) max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57 4.19 | 0.51 | 0.25 | 3.05 | 0.53 0.33 | 0.81 0.66 | 16.66 16.51 | 16.66 16.51 | 1.27 | 16.00 14.99 | 16.00 14.99 | 17.65 17.40 | 17.65 17.40 | 1.22 1.07 | 0.51 | 1.44 1.02 | 0.18 | 0.18 | 0.10 | 2.16 | 2.16 | 45° |
| inches | 0.180 0.165 | 0.020 | 0.01 | 0.12 | 0.021 0.013 | 0.032 0.026 | 0.656 0.650 | 0.656 0.650 | 0.05 | 0.630 0.590 | 0.630 0.590 | 0.695 0.685 | 0.695 0.685 | 0.048 0.042 | 0.020 | 0.057 0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.
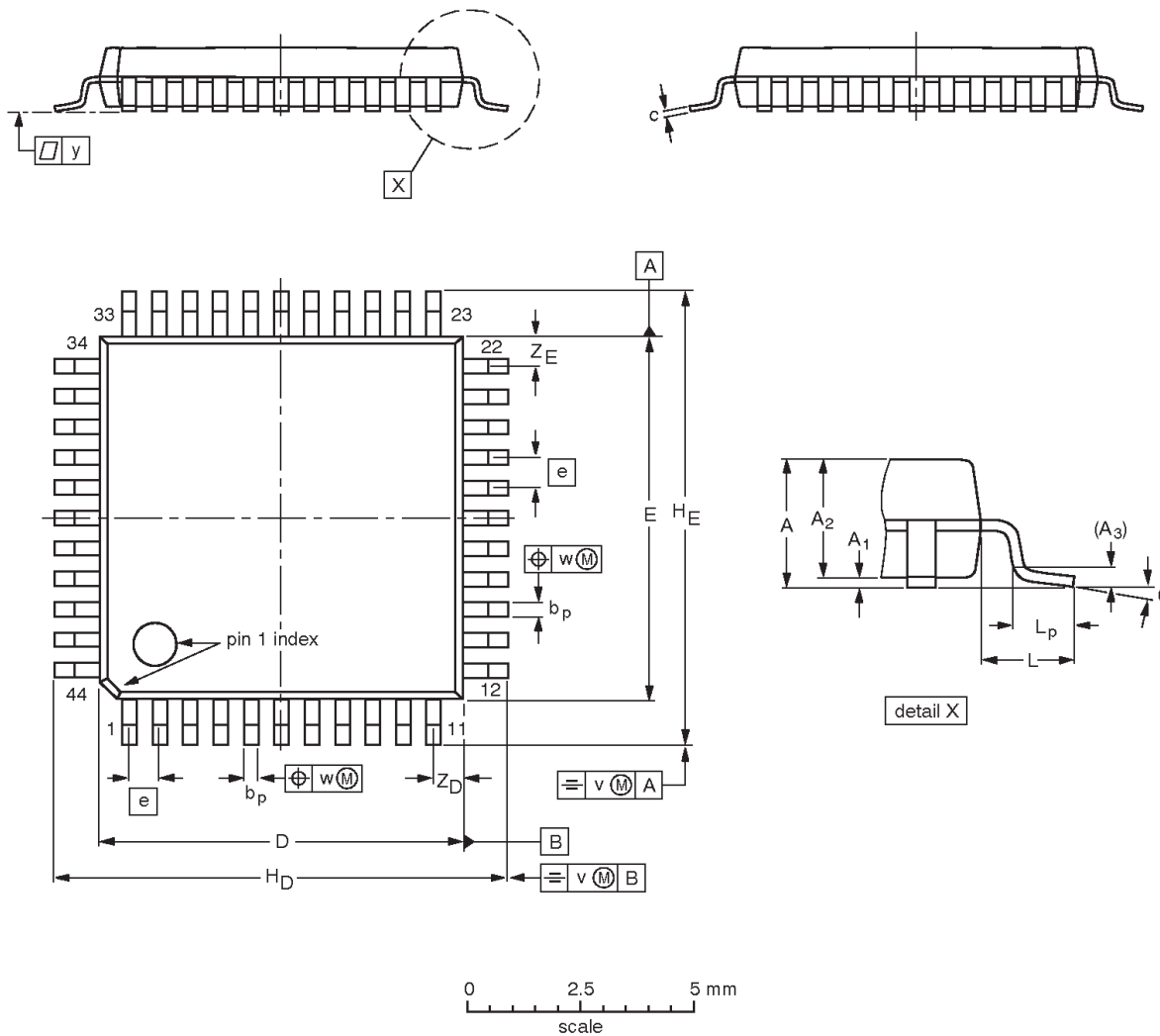
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT187-2 | 112E10 | MO-047AC | | | | ~~95-02-25~~ 97-12-16 |

# 80C51 8-bit microcontrollers
## 16K/32K, 512 OTP, I²C, watchdog timer

**87C524/87C528**

**QFP44:** plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

**SOT307-2**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D⁽¹⁾ | E⁽¹⁾ | e | H_D | H_E | L | Lₚ | v | w | y | Z_D⁽¹⁾ | Z_E⁽¹⁾ | θ |
|------|--------|-----|-----|-----|-----|-----|------|------|-----|------|------|-----|------|------|------|-----|--------|--------|-----|
| mm | 2.10 | 0.25 0.05 | 1.85 1.65 | 0.25 | 0.40 0.20 | 0.25 0.14 | 10.1 9.9 | 10.1 9.9 | 0.8 | 12.9 12.3 | 12.9 12.3 | 1.3 | 0.95 0.55 | 0.15 | 0.15 | 0.1 | 1.2 0.8 | 1.2 0.8 | 10° 0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|------|--|---------------------|------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT307-2 | | | | | | ~~95-02-04~~ 97-08-01 |

**NOTES**

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1]   Please consult the most recently issued datasheet before initiating or completing a design.

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**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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