W79E834/W79E833/W79E832 Data Sheet

winbond

8-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

W79E834 series are an 8-bit Turbo 51 microcontroller which has Flash EPROM which can be programmed by ICP (In Circuit Program) or by writer. The instruction sets of the W79E834 series are fully compatible with the standard 8052. W79E834 series contain a **8K/4K/2K** bytes of main Flash EPROM; a **256** bytes of RAM; **256** bytes AUX-RAM (W79E834 only); three 8-bit bi-directional, one 2-bit bi-directional and bit-addressable I/O ports; **two** 16-bit timer/counters; **8/4**-channel multiplexed 10-bit A/D converter; **4**-channel 10-bit PWM; one timer with input capture units; two serial ports that include a SPI and an enhanced full duplex serial port. These peripherals are supported by **13** sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside W79E834 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

2. FEATURES

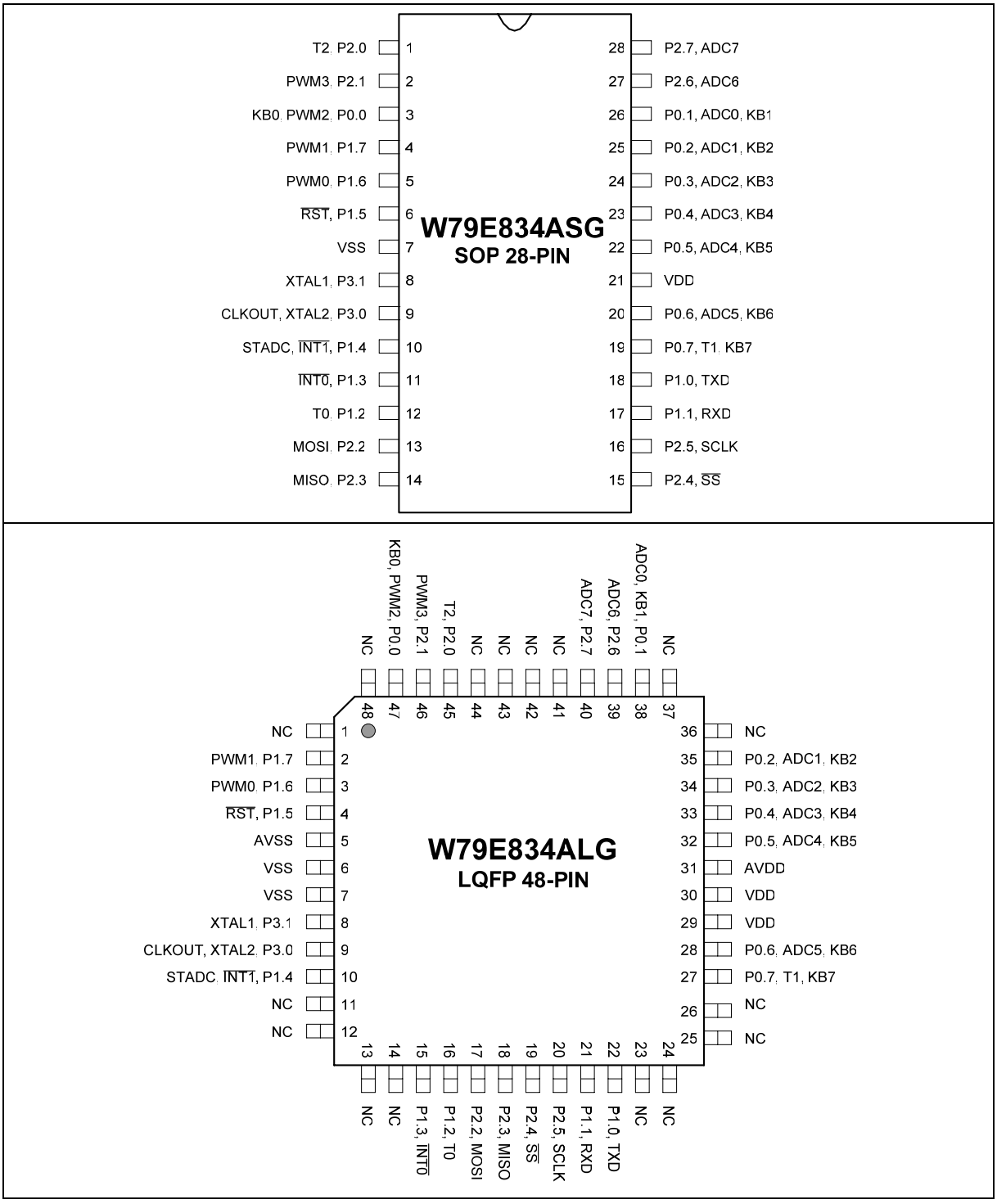
- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 20MHz when VDD=4.5V to 5.5V, 12MHz when VDD=2.7V to 5.5V.
- 8K/4K/2K bytes of Flash EPROM (AP Flash EPROM), with ICP and External Writer programmable mode.
- **256** bytes of on-chip RAM.
- **256** bytes of on-chip AUX-RAM (W79E834 only).
- Instruction-set compatible with MSC-51.
- On-chip configurable RC oscillator (6MHz)
- Three 8-bit bi-directional and one 2-bit bi-directional port.
- **Two** 16-bit timer/counters.
- One Timer with three inputs captures capability.
- **13** interrupts source with four levels of priority.
- One enhanced full duplex serial port with framing error detection and automatic address recognition.
- The 4 outputs mode and TTL/Schmitt trigger selectable Port.
- Programmable Watchdog Timer.
- **Four**-channel 10-bit PWM (Pulse Width Modulator).
- **Eight/Four**-channel multiplexed with 10-bits A/D converter.
- One SPI with master/slave capability.
- Eight keypad interrupt inputs.
- Built-in power management.
- LED drive capability (20mA) on all port pins.
- Low Voltage Detect interrupt and reset.
- Code protection.
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
  - ICP(In Circuit Programming) writer
- Packages:
  - Lead Free (RoHS) SOP 28: W79E834ASG
  - Lead Free (RoHS) LQFP 48: W79E834ALG
  - Lead Free (RoHS) SOP 28: W79E833ASG
  - Lead Free (RoHS) SOP 28: W79E832ASG

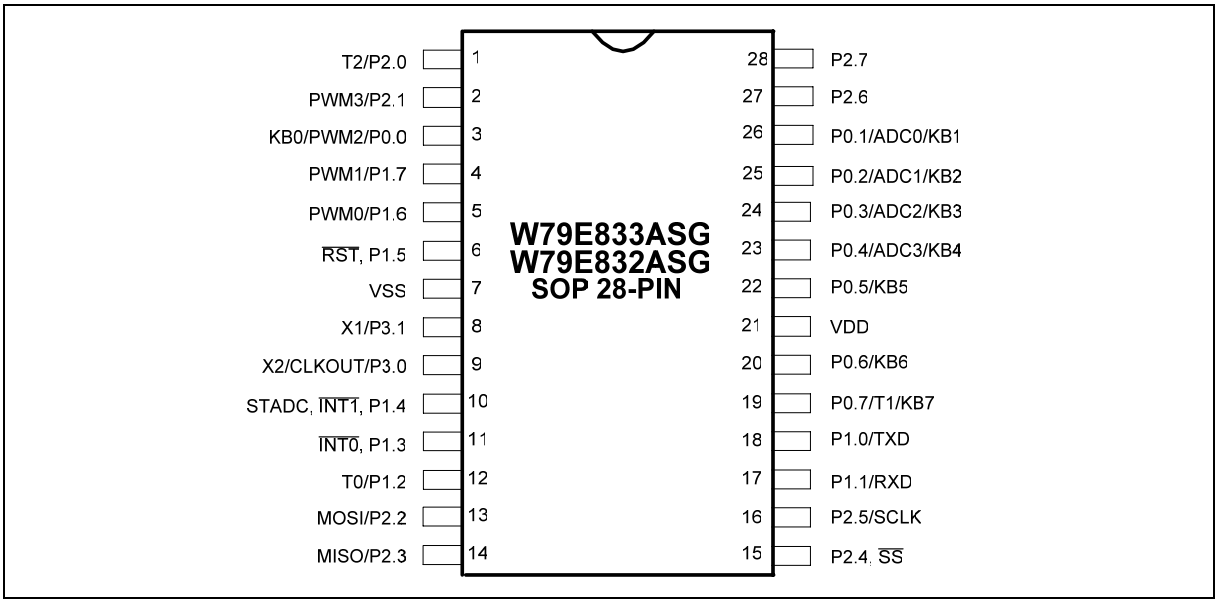
3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

PART NO.	EPROM FLASH SIZE	RAM	AUX RAM	ADC	PWM	PACKAGE	REMARK
W79E834ASG	8KB	256B	256B	8x10Bit	4x10Bit	SOP-28 Pin	
W79E834ALG	8KB	256B	256B	8x10Bit	4x10Bit	LQFP-48 Pin	
W79E833ASG	4KB	256B	0B	4x10Bit	4x10Bit	SOP-28 Pin	
W79E832ASG	2KB	256B	0B	4x10Bit	4x10Bit	SOP-28 Pin	

4. PIN CONFIGURATION




W79E833ASG
W79E832ASG
SOP 28-PIN
T2/P2.0
PWM3/P2.1
KB0/PWM2/P0.0
PWM1/P1.7
PWM0/P1.6
RST, P1.5
VSS
X1/P3.1
X2/CLKOUT/P3.0
STADC, INT1, P1.4
INT0, P1.3
T0/P1.2
MOSI/P2.2
MISO/P2.3
1
2
3
4
5
6
7
8
9
10
11
12
13
14
28
27
26
25
24
23
22
21
20
19
18
17
16
15
P2.7
P2.6
P0.1/ADC0/KB1
P0.2/ADC1/KB2
P0.3/ADC2/KB3
P0.4/ADC3/KB4
P0.5/KB5
VDD
P0.6/KB6
P0.7/T1/KB7
P1.0/TXD
P1.1/RXD
P2.5/SCLK
P2.4, SS

5. PIN DESCRIPTION

SYMBOL	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3 (ICP MODE)	TYPE	DESCRIPTIONS
P3.1	X1			I	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock or configurable i/o pin.
P3.0	X2/CLKOUT			O	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin.
VDD				P	POWER SUPPLY: Supply voltage for operation.
VSS				P	GROUND: Ground potential.
P0.0	PWM2	KB0		I/O	Port0: Support 4 mode output and 2 mode input. Multifunction pins for T1, PWM2, ADC0-5, /KB0-7, Data and Clock (for ICP).
P0.1	ADC0	KB1		I/O	
P0.2	ADC1	KB2		I/O	
P0.3	ADC2	KB3		I/O	
P0.4	ADC3	KB4	Data	I/O	
P0.5	ADC4 (note)	KB5	Clock	I/O	
P0.6	ADC5 (note)	KB6		I/O	
P0.7	T1	KB7		I/O	
P1.0	TXD			I/O	Port1: Support 4 mode output and 2 mode input. Multifunction pins for /RST, TXD & RXD (Uart), T0, /INT0-1, PWM0-1, STADC, and HV (for ICP).
P1.1	RXD			I/O	
P1.2	T0			I/O	
P1.3	/INT0			I/O	
P1.4	/INT1	STADC		I/O	
P1.5	$\overline{\text{RST}}$		HV	I	
P1.6	PWM0			I/O	
P1.7	PWM1			I/O	
P2.0	T2			I/O	Port2: Support 4 mode output and 2 mode input. Multifunction pins for T2, PWM3, MOSI, MISO, /SS, SCLK, ADC6-7.
P2.1	PWM3			I/O	
P2.2	MOSI			I/O	
P2.3	MISO			I/O	
P2.4	$\overline{\text{SS}}$			I/O	
P2.5	SCLK			I/O	
P2.6	ADC6 (note)			I/O	
P2.7	ADC7 (note)			I/O	

- **TYPE:** P: power, I: input, O: output, I/O: bi-directional.
- **Note:** W79E834 supports 8 ADC channels, ADC0-7. W79E833/2 supports only 4 ADC channels, ADC0-3.

6. FUNCTIONAL DESCRIPTION

W79E834 series architecture consist of a 4T 8051 core controller surrounded by various registers, **8K/4K/2K** bytes Flash EPROM, **256** bytes of RAM, **256** bytes Aux RAM (W79E834 only), three general purpose I/O ports, two timer/counters, one UART serial port, one SPI, one timer with input capture units, 4 channel PWM with 10-bit counter, **8/4**-channel multiplexed with 10-bit ADC analog input, Flash EPROM program by Writer and ICP.

6.1 On-Chip Flash EPROM

W79E834 series include one **8K/4K/2K** bytes of main Flash EPROM for application program when operating the in-circuit programming features by the Flash EPROM itself which need Writer or ICP program board to program the Flash EPROM. This ICP (In-Circuit Programming) feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-circuit programming feature makes it possible that the end-user is able to easily update the system firmware by themselves without opening the chassis.

6.2 I/O Ports

W79E834 series have three 8-bit and one 2-bit port, up to 25 I/O pins and 1 input pin (/RST is input only) using on-chip oscillator & /RST is input only by reset options. All ports can be used as four outputs mode when it may set by PxM1.y and PxM2.y registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Serial I/O

W79E834 series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on W79E834 series can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

The device also consists of another serial interface, SPI. This is a full duplex, synchronous communication bus supporting 2 operating modes: Master and Slave mode. It has a transfer complete flag. It also support overrun and mode fault status, and write collision protection mechanism.

6.4 Timers

The device has total three 16-bit timers; two 16-bit timers that have functions similar to the timers of the 8032 family, and third timer is capable to function as timer and also provide capture support. When used as timers, user has a choice to set 12 or 4 clocks per count that emulates the timing of the original 8032. Each timer's count value is stored in two SFR locations that can be written or read by software. There are also some other SFRs associated with the timers that control their mode and operation.

6.5 Interrupts

The Interrupt structure in W79E834 series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The data pointer in W79E834 series is similar to standard 8052 that have dual 16-bit Data Pointers (DPTR) by setting DPS of AUXR1.0. The figure of dual DPRT is as below diagram.

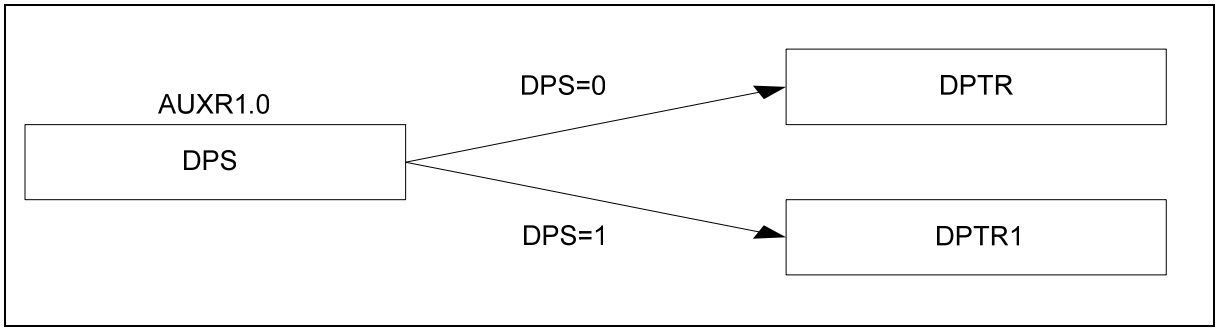


Figure 6- 1: Data Pointer

6.7 Architecture

W79E834 series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E834. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in W79E834. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

W79E834 series have a **256** bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

W79E834 series have an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM. Hence the size of the stack is limited by the size of this RAM.

6.7.7 MOVX AUX RAM (W79E834 only)

W79E834 have a 256 bytes AUX RAM of data space SRAM which is read/write accessible and is memory mapped. This on-chip SRAM is reached by the MOVX instruction. It is not used for executable memory. There is no conflict or overlap as they use different addressing modes and separate instructions.

6.8 Power Management

Power Management like the standard 8051/52, the W79E834 series have IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU is stopped while the timers, serial ports and interrupt block continue to operate. In POWER DOWN mode, all of the peripheral clocks are stopped, and chip operation stops completely. This mode consumes the least amount of power.

7. MEMORY ORGANIZATION

W79E834 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

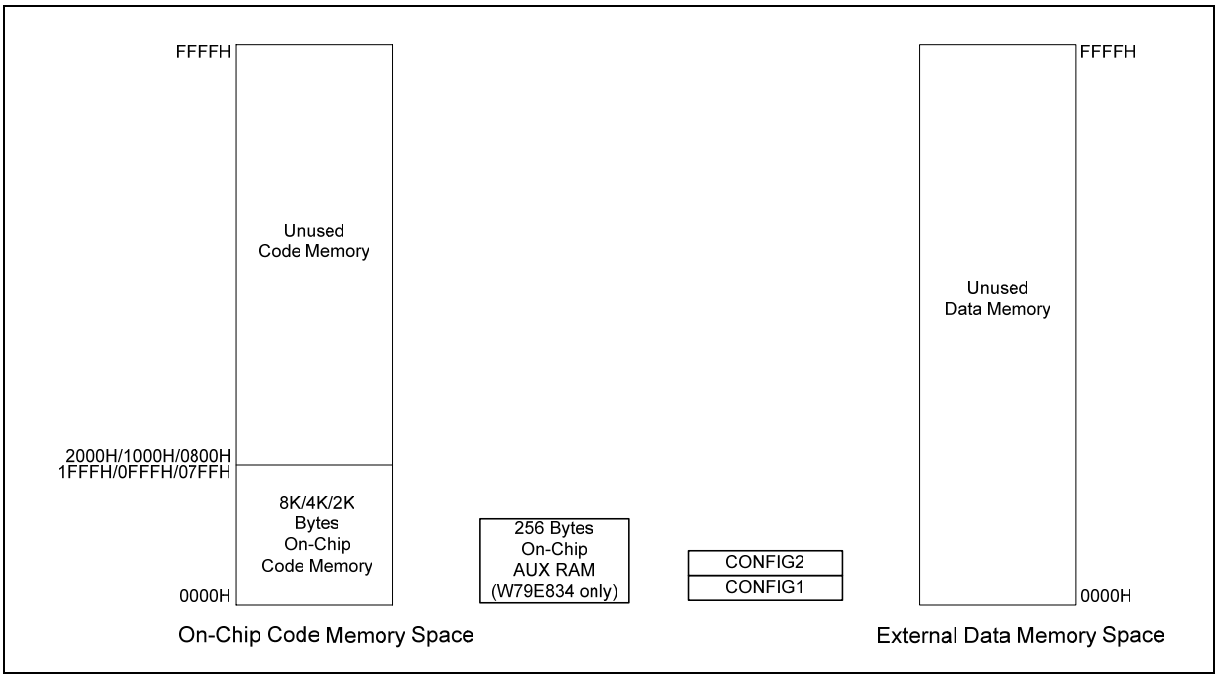


Figure 7-1: W79E834 series Memory Map

7.1 Program Memory (on-chip Flash)

The Program Memory on W79E834 series can be up to **8K/4K/2K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Memory (accessed by MOVX) (W79E834 only)

W79E834 can read/write 256 bytes AUX RAM by the MOVX instruction. The data memory region is from 0000H to 00FFH.

7.3 Scratch-pad RAM and Register Map

As mentioned before, W79E834 series have separate Program and Data Memory areas. The on-chip 256 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

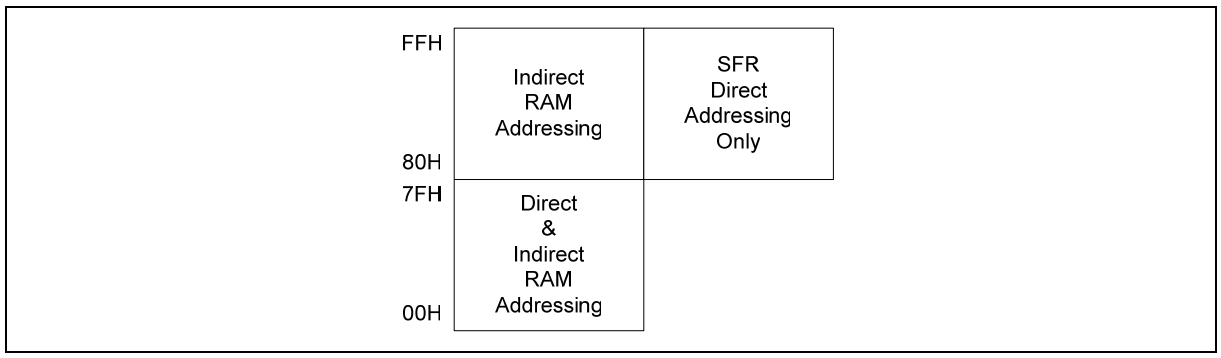


Figure 7-2: W79E834 series RAM and SFR Memory Map

Since the scratch-pad RAM is only 256 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

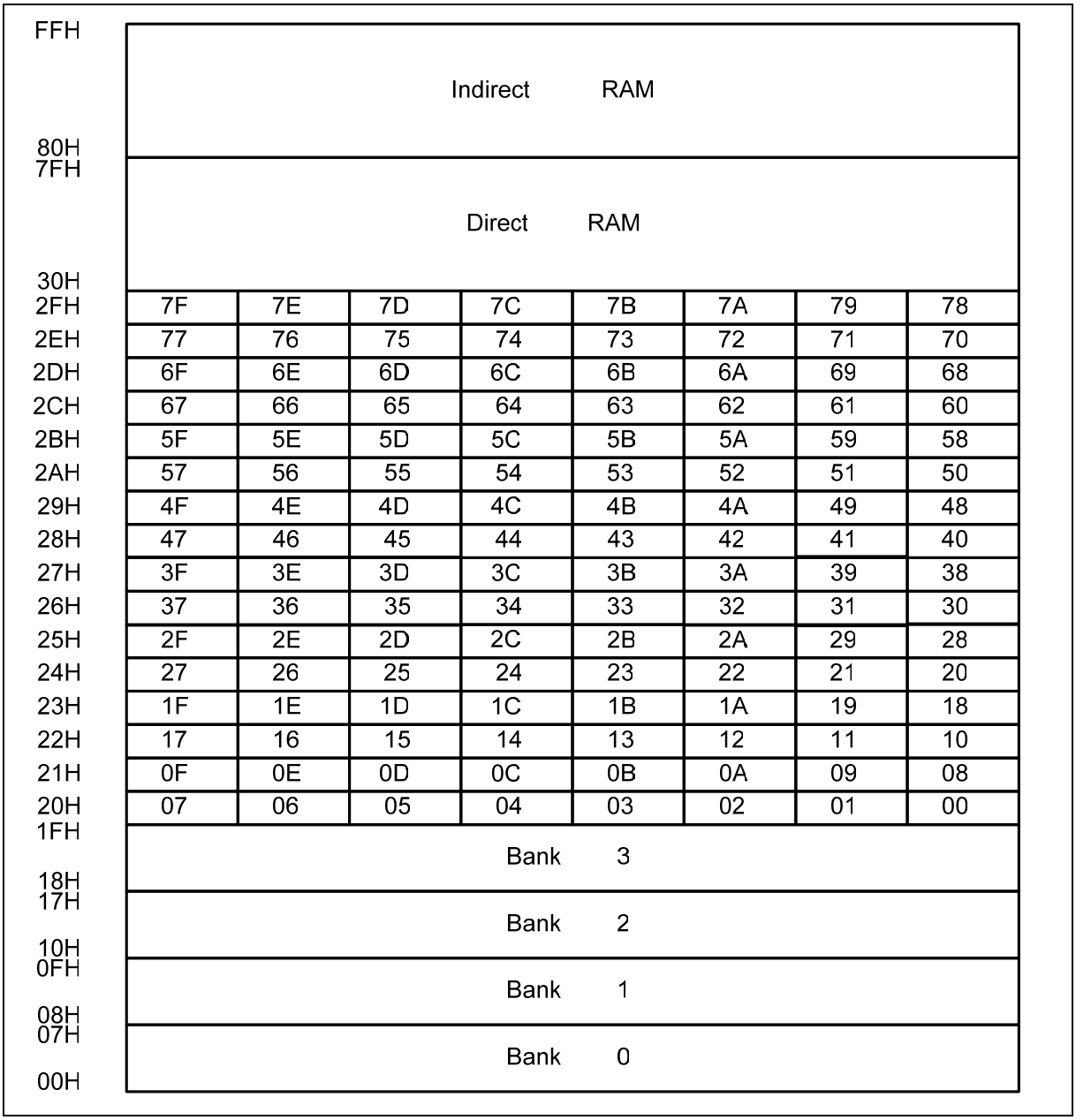


Figure 7-3: Scratch-pad RAM

7.3.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at any one time W79E834 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

7.3.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

7.3.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8. SPECIAL FUNCTION REGISTERS

W79E834 series use Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where we wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. W79E834 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

8.1 SFR Location Table

F8	**IP1**							
F0	**B**			SPCR	SPSR	SPDR	PADIDS	IP1H
E8	**EIE**							
E0	**ACC**	ADCCON	ADCH		CCL0	CCH0	CCL1	CCH1
D8	**WDCON**	PWMPL	PWM0L	PWM1L	PWMCON1	PWM2L	PWM3L	
D0	**PSW**	PWMPH	PWM0H	PWM1H		PWM2H	PWM3H	PWMCON3
C8	**T2CON**	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0								TA
B8	**IP0**	SADEN						
B0	**P3**	P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	**IE**	SADDR						
A0	**P2**	KBI	AUXR1	CAPCON0	CAPCON1		CCL2	CCH2
98	**SCON**	SBUF					P3M1	P3M2
90	**P1**					DIVM		
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	**P0**	SP	DPL	DPH				PCON

Table 8- 1: Special Function Register Location Table

Note: 1. The SFRs in the column with dark borders are bit-addressable

2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses.

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
IP1	INTERRUPT PRIORITY 1	F8H	(FF) PCAP	(FE) PT2	(FD) PPWM	(FC) PWDI	(FB) PSPI	(FA) -	(F9) PKB	(F8) -	0000 0X0XB
IP1H	INTERRUPT HIGH PRIORITY 1	F7H	PCAPH	PT2H	PPWMH	PWDIH	PSPIH	-	PKBH	-	0000 0X0XB
PADIDS	PORT ADC DIGITAL INPUTS DISABLE	F6H	PADIDS.7 (W79E834 only)	PADIDS.6 (W79E834 only)	PADIDS.5 (W79E834 only)	PADIDS.4 (W79E834 only)	PADIDS.3	PADIDS.2	PADIDS.1	PADIDS.0	XXXX XXXXB
SPDR	SERIAL PERIPHERAL DATA REGISTER	F5H	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0	XXXXXXXXB
SPSR	SERIAL PERIPHERAL STATUS REGISTER	F4H	SPIF	WCOL	SPIOVF	MODF	DRSS	-	-	-	0000 0XXXB
SPCR	SERIAL PERIPHERAL CONTROL REGISTER	F3H	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0	0000 0100B
B	B REGISTER	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
EIE	INTERRUPT ENABLE 1	E8H	(EF) ECPTF	(EE) ET2	(ED) EPWM	(EC) EWDI	(EB) ESPI	(EA) -	(E9) EKB	(E8) -	0000 0X0XB
CCH1	INPUT CAPTURE 1 HIGH	E7H	CCH1.7	CCH1.6	CCH1.5	CCH1.4	CCH1.3	CCH1.2	CCH1.1	CCH1.0	0000 0000B
CCL1	INPUT CAPTURE 1 LOW	E6H	CCL1.7	CCL1.6	CCL1.5	CCL1.4	CCL1.3	CCL1.2	CCL1.1	CCL1.0	0000 0000B
CCH0	INPUT CAPTURE 0 HIGH	E5H	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0	0000 0000B
CCL0	INPUT CAPTURE 0 LOW	E4H	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0	0000 0000B
ADCH	ADC CONVERTER RESULT	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	XXXXXXXXB
ADCCON	ADC CONTROL REGISTER	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	AADR2 (W79E834 only)	AADR1	AADR0	XX00 0000B
ACC	ACCUMULATOR	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
PWM3L	PWM 3 LOW BITS REGISTER	DEH	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0	0000 0000B
PWM2L	PWM 2 LOW BITS REGISTER	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	0000 0000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	load	PWMF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I	0000 0000B
PWM1L	PWM 1 LOW BITS REGISTER	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0x00B Watchdog reset: 0x000100B Power on reset 0x000000B
PWMCON3	PWM CONTROL REGISTER 3	D7H	PWM3OE	PWM2OE	PWM1OE	PWM0OE	-	-	FP1	FP0	0000 XX00B

Continued

SYMBOL	DEFINITION	ADDRESS	MSB			BIT ADDRESS, SYMBOL				LSB	RESET
PWM3H	PWM 3 HIGH BITS REGISTER	D6H	-	-	-	-	-	-	PWM3.9	PWM3.8	XXXX XX00B
PWM2H	PWM 2 HIGH BITS REGISTER	D5H	-	-	-	-	-	-	PWM2.9	PWM2.8	XXXX XX00B
PWM1H	PWM 1 HIGH BITS REGISTER	D3H	-	-	-	-	-	-	PWM1.9	PWM1.8	XXXX XX00B
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	XXXX XX00B
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	XXXX XX00B
PSW	PROGRAM STATUS WORD	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B
TH2	TIMER 2 MSB	CDH	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0	0000 0000B
TL2	TIMER 2 LSB	CCH	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0	0000 0000B
RCAP2H	TIMER 2 RELOAD MSB	CBH	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0	0000 0000B
RCAP2L	TIMER 2 RELOAD LSB	CAH	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0	0000 0000B
T2MOD	TIMER 2 MODE	C9H	ENLD	IICEN2	ICEN1	ICEN0	T2CR	-	-	-	0000 0XXXB
T2CON	TIMER 2 CONTROL	C8H	TF2	-	-	-	-	TR2	-	CMP/$\dot{R}\dot{L}\dot{2}$	0XXX X0X0B
TA	TIMED ACCESS PROTECTION	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	0000 0000B
SADEN	SLAVE ADDRESS MASK	B9H	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0	0000 0000B
IP0	INTERRUPT PRIORITY	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	X000 0000B
IP0H	INTERRUPT HIGH PRIORITY	B7H	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H	X000 0000B
P2M2	PORT 2 OUTPUT MODE 2	B6H	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0	0000 0000B
P2M1	PORT 2 OUTPUT MODE 1	B5H	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0	0000 0000B
P1M2	PORT 1 OUTPUT MODE 2	B4H	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	00X0 0000B
P1M1	PORT 1 OUTPUT MODE 1	B3H	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	00X0 0000B
P0M2	PORT 0 OUTPUT MODE 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	0000 0000B
P0M1	PORT 0 OUTPUT MODE 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	0000 0000B
P3	PORT3	B0H	-	-	-	-	-	-	X1	X2/CLKOUT	XXXX XX00B
SADDR	SLAVE ADDRESS	A9H	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0	0000 0000B
IE	INTERRUPT ENABLE	A8H	(AF) EA	(AE) EADC	(AD) EBO	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B
CCH2	INPUT CAPTURE 2 HIGH	A7H	CCH2.7	CCH2.6	CCH2.5	CCH2.4	CCH2.3	CCH2.2	CCH2.1	CCH2.0	0000 0000B
CCL2	INPUT CAPTURE 2 LOW	A6H	CCL2.7	CCL2.6	CCL2.5	CCL2.4	CCL2.3	CCL2.2	CCL2.1	CCL2.0	0000 0000B

Continued

SYMBOL	DEFINITION	ADDRESS	MSB		BIT ADDRESS, SYMBOL					LSB	RESET
CAPCON1	CAPTURE CONTROL 1	A4H	-	-	ENF2	ENF1	ENF0	CPTF2	CPTF1	CPTF0	XX00 0000B
CAPCON0	CAPTURE CONTROL 0	A3H	CCT2.1	CCT2.0	CCT1.1	CCT1.0	CCT0.1	CCT0.0	CCLD.1	CCLD.0	0000 0000B
AUXR1	AUX FUNCTION REGISTER	A2H	KBF	BOD	BOI	LPBOV	SRST	ADCEN	RCCLK	DPS	0000 0000B
KBI	KEYBOARD INTERRUPT	A1H	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0	0000 0000B
P2	PORT 2	A0H	(A7) AD7 (W79E834 only)	(A6) AD6 (W79E834 only)	(A5) SCLK	(A4) /SS	(A3) MISO	(A2) MOSI	(A1) PWM3	(A0) T2	11111111B
P3M2	PORT 3 OUTPUT MODE 2	9FH	-	-	-	-	-	ENCLK	P3M2.1	P3M2.0	XXXX X000B
P3M1	PORT 3 OUTPUT MODE 1	9EH	P3S	P2S	P1S	P0S	T1OE	T0OE	P3M1.1	P3M1.0	0000 0000B
SBUF	SERIAL BUFFER	99H	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0	XXXXXXXXB
SCON	SERIAL CONTROL	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
DIVM	UC CLOCK DIVIDE REGISTER	95H	DIVM.7	DIVM.6	DIVM.5	DIVM.4	DIVM.3	DIVM.2	DIVM.1	DIVM.0	0000 0000B
P1	PORT 1	90H	(97) PWM1	(96) PWM0	(95) /RST	(94) /INT1	(93) /INT0	(92) T0	(91) RXD	(90) TXD	1111 1111B
CKCON	CLOCK CONTROL	8EH	-	CCDIV.1	CCDIV.0	T1M	T0M	-	-	-	X000 0XXXB
TH1	TIMER HIGH 1	8DH	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0	0000 0000B
TH0	TIMER HIGH 0	8CH	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0	0000 0000B
TL1	TIMER LOW 1	8BH	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0	0000 0000B
TL0	TIMER LOW 0	8AH	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0	0000 0000B
TMOD	TIMER MODE	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0000 0000B
TCON	TIMER CONTROL	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	POWER CONTROL	87H	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL	00XX 0000B
DPH	DATA POINTER HIGH	83H	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0	0000 0000B
DPL	DATA POINTER LOW	82H	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0	0000 0000B
SP	STACK POINTER	81H	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0	0000 0111B
P0	PORT 0	80H	(87) T1 KB7	(86) AD5 (W79E834 only) KB6	(85) AD4 (W79E834 only) KB5	(84) AD3 KB4	(83) AD2 KB3	(82) AD1 KB2	(81) AD0 KB1	(80) PWM2 KB0	1111 1111B

Table 8- 2: Special Function Register

8.2 SFR Detail Bit Descriptions

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P0.7	T1 or KB7 pin or I/O pin by alternative.
6	P0.6	ADC5 (W79E834 only) or KB6 or I/O pin by alternative.
5	P0.5	ADC4 (W79E834 only) or KB5 or Clock (ICP function) pin or I/O pin by alternative.
4	P0.4	ADC3 or KB4 or Data (ICP function) pin or I/O pin by alternative.
3	P0.3	ADC2 or KB3 pin or I/O pin by alternative.
2	P0.2	ADC1 or KB2 pin or I/O pin by alternative.
1	P0.1	ADC0 or KB1 pin or I/O pin by alternative.
0	P0.0	PWM 2 or KB0 pin or I/O pin by alternative.

Note: The initial value of the port is set by CONFIG1.PRHI bit. The default setting for CONFIG1.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG1.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer. This is the high byte of the DPTR 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.

Continued

BIT	NAME	FUNCTION
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	CCDIV[1:0]		T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7	-	Reserved.
6~5	CCDIV.1~0	Timer 2 clock select: CCDIV[1] CCDIV[0] 0 0 : Timer 2 clock = Fosc 0 1 : Timer 2 clock = Fosc/4 1 0 : Timer 2 clock = Fosc/16 1 1 : Timer 2 clock = Fosc/32
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks.
2~0	-	Reserved.

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P1.7	PWM 1 pin or I/O pin by alternative.
6	P1.6	PWM 0 pin or I/O pin by alternative.
5	P1.5	$\overline{RST}$ pin or Input Pin by alternative.
4	P1.4	$\overline{INT1}$ interrupt or STADC or I/O pin by alternative.
3	P1.3	$\overline{INT0}$ interrupt or I/O pin by alternative.
2	P1.2	Timer 0 or I/O pin by alternative.
1	P1.1	RXD of Serial port or I/O pin by alternative..
0	P1.0	TXD of Serial port or I/O pin by alternative..

DIVIDER CLOCK

Bit:	7	6	5	4	3	2	1	0
	DIVM.7	DIVM.6	DIVM.5	DIVM.4	DIVM.3	DIVM.2	DIVM.1	DIVM.0

Mnemonic: DIVM Address: 95h

BIT	NAME	FUNCTION
7-0	DIVM.[7:0]	The DIVM register is clock divider of uC. Refer OSCILLATOR chapter.

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.

Continued

BIT	NAME	FUNCTION
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM0, SM1: Mode Select bits

MODE	SM0	SM1	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7-0	SBUF.[7:0]	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 3 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P3S	P2S	P1S	P0S	T1OE	T0OE	P3M1.1	P3M1.0

Mnemonic: P3M1 Address: 9Eh

BIT	NAME	FUNCTION
7	P3S	1: Enables Schmitt trigger inputs on Port 3.
6	P2S	1: Enables Schmitt trigger inputs on Port 2.
5	P1S	1: Enables Schmitt trigger inputs on Port 1.

Continued

BIT	NAME	FUNCTION
4	P0S	1: Enables Schmitt trigger inputs on Port 0.
3	T1OE	1: The P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
2	T0OE	1: The P1.2 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one half of the Timer 0 overflow rate.
1	P3M1.1	To control the output configuration of P3.1.
0	P3M1.0	To control the output configuration of P3.0.

PORT 3 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENCLK	P3M2.1	P3M2.0

Mnemonic: P3M2 Address: 9Fh

BIT	NAME	FUNCTION
7~3	-	Reserved
2	ENCLK	1: To use the on-chip RC oscillator, a clock output is enabled on the XTAL2 pin.
1	P3M2.1	See as below table.
0	P3M2.0	See as below table.

Port Output Configuration Settings:

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P3M1.PxS=0, TTL input P3M1.PxS=1, Schmitt input
1	1	Open Drain

PORT 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P2.7	ADC7 pin or I/O pin by alternative.
6	P2.6	ADC6 pin or I/O pin by alternative.
5	P2.5	SCLK pin or I/O pin by alternative.
4	P2.4	$\overline{SS}$ pin or I/O pin by alternative.
3	P2.3	MISO pin or I/O pin by alternative.
2	P2.2	MOSI pin or I/O pin by alternative.
1	P2.1	PWM3 pin or I/O pin by alternative.
0	P2.0	T2 pin or I/O pin by alternative.

KEYBOARD INTERRUPT

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	ADCEN	RCCLK	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function. 1: This prevents brownout detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power Down mode. 1: When BOD is enable, the 1/16 time will be turned on Brown Out detect circuit by Power Down mode. When uC is entry Power Down mode, the BOD will enable internal RC OSC(500KHZ)
3	SRST	Software reset: 1: Reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	RCCLK	0: The CPU clock is used as ADC clock. 1: The internal RC clock/2 is used as ADC clock.
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1.

CAPTURE CONTROL 0 REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCT2		CCT1		CCT0		CCLD	

Mnemonic: CAPCON0 Address: A3h

BIT	NAME	FUNCTION
7~6	CCT2.1~0	Capture 2 edge select: 00 : Rising edge trigger. 01 : Falling edge trigger. 10 : Both rising and falling edge trigger. 11 : Reserved.

Continued

BIT	NAME	FUNCTION
5~4	CCT1.1~0	Capture 1 edge select: 00 : Rising edge trigger. 01 : Falling edge trigger. 10 : Both rising and falling edge trigger. 11 : Reserved.
3~2	CCT0.1~0	Capture 0 edge select: 00 : Rising edge trigger. 01 : Falling edge trigger. 10 : Both rising and falling edge trigger. 11 : Reserved
1~0	CCLD.1~0	Reload trigger select: 00 : Timer 2 overflow. 01 : Reload by capture 0 block. 10 : Reload by capture 1 block. 11 : Reload by capture 2 block.

CAPTURE CONTROL 1 REGISTER

Bit:	7	6	5	4	3	2	1	0
	-		ENF2	ENF1	ENF0	CPTF2	CPTF1	CPTF0

Mnemonic: CAPCON1 Address: A4h

BIT	NAME	FUNCTION
7~6	-	Reserved.
5	ENF2	Enable filter for capture input 2.
4	ENF1	Enable filter for capture input 1.
3	ENF0	Enable filter for capture input 0.
2	CPTF2	External capture/reload 2 interrupt flag.
1	CPTF1	External capture/reload 1 interrupt flag.
0	CPTF0	External capture/reload 0 interrupt flag.

Programming note: When using digital filter function, user is recommended to enable digital filter (CAPCON1.ENF* bit) first prior to enable input capture (T2MOD.ICEN*) to avoid false trigger.

INPUT CAPTURE 2 LOW REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCL2.7	CCL2.6	CCL2.5	CCL2.4	CCL2.3	CCL2.2	CCL2.1	CCL2.0

Mnemonic: CCL2 Address: A6h

BIT	NAME	FUNCTION
7~0	CCL2.7~0	Capture 2 low byte.

INPUT CAPTURE 2 HIGH REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCH2.7	CCH2.6	CCH2.5	CCH2.4	CCH2.3	CCH2.2	CCH2.1	CCH2.0

Mnemonic: CCH2 Address: A7h

BIT	NAME	FUNCTION
7~0	CCH2.7~0	Capture 2 high byte.

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

PORT 3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.1-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7~2	-	Reserved.
1	P3.1	X1 or I/O pin by alternative.
0	P3.0	X2 or CLKOUT or I/O pin by alternative.

PORT 0 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1 Address: B1h

BIT	NAME	FUNCTION
7-0	P0M1	To control the output configuration of P0 bits [7:0]

PORT 0 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2 Address: B2h

BIT	NAME	FUNCTION
7-0	P0M2	To control the output configuration of P0 bits [7:0]

PORT 1 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	P1M1.6	-	P1M1.4	P1M1.31	P1M1.2	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

BIT	NAME	FUNCTION
7-0	P1M1	To control the output configuration of P1 bits [7:0]

PORT 1 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

BIT	NAME	FUNCTION
7-0	P1M2	To control the output configuration of P1 bits [7:0]

PORT 2 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P2M1.7	P2M1.6	P2M1.5	P2M1.4	P2M1.3	P2M1.2	P2M1.1	P2M1.0

Mnemonic: P2M1 Address: B5h

BIT	NAME	FUNCTION
7-0	P2M1	To control the output configuration of P2 bits [1:0]

PORT 2 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P2M2.7	P2M2.6	P2M2.5	P2M2.4	P2M2.3	P2M2.2	P2M2.1	P2M2.0

Mnemonic: P2M2 Address: B6h

BIT	NAME	FUNCTION
1-0	P2M2	To control the output configuration of P2 bits [7:0]

INTERRUPT HIGH PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PADCH	1: To set interrupt high priority of ADC is highest priority level.
5	PBOH	1: To set interrupt high priority of Brown Out Detector is highest priority level.
4	PSH	1: To set interrupt high priority of Serial port 0 is highest priority level.
3	PT1H	1: To set interrupt high priority of Timer 1 is highest priority level.
2	PX1H	1: To set interrupt high priority of External interrupt 1 is highest priority level.
1	PT0H	1: To set interrupt high priority of Timer 0 is highest priority level.
0	PX0H	1: To set interrupt high priority of External interrupt 0 is highest priority level.

INTERRUPT PRIORITY 0

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PBO	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PADC	1: To set interrupt priority of ADC is higher priority level.
5	PBO	1: To set interrupt priority of Brown Out Detector is higher priority level.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

TIMER 2 CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF2	-	-	-	-	TR2	-	CP/$\overline{RL2}$

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in compare mode. It is cleared only by software. Software can also set this bit.
6~3	-	Reserved.
2	TR2	Timer 2 Run Control: This bit enables/disables the operation of timer 2. Halting this will preserve the current count in TH2, TL2.
1	-	Reserved.
0	CMP/$\overline{RL2}$	Compare/Reload Select: This bit determines whether the compare or reload function will be used for timer 2. If the bit is 0 then auto reload will occur when timer 2 overflows. And reload will be from RCAP register if ENLD = 1, else the timer 2 will be reloaded with 0. If this bit is 1, when timer 2 value matches RCAP value, timer 2 will reset to 0.

TIMER 2 MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	ENLD	ICEN2	ICEN1	ICEN0	T2CR	-	-	-

Mnemonic: T2MOD Address: C9h

BIT	NAME	FUNCTION
7	ENLD	Enable reload from RCAP2 registers to timer 2 counters.
6	ICEN2	Capture 2 External Enable: This bit enables the capture/reload function on the T2 pin. An edge trigger (programmable by CAPCON0.CCT2[1:0] bits) detected on the T2 pin will result in capture from free running timer 2 counters to input capture 2 registers, and reload from RCAP2 registers to timer 2 counters if ENLD = 1 and CMP/RL2 = 0.
5	ICEN1	Capture 1 External Enable: This bit enables the capture/reload function on the T1 pin. An edge trigger (programmable by CAPCON0.CCT1[1:0] bits) detected on the T1 pin will result in capture from free running timer 2 counters to input capture 1 registers, and reload from RCAP2 registers to timer 2 counters if ENLD = 1 and CMP/RL2 = 0.

Continued

BIT	NAME	FUNCTION
4	ICEN0	Capture 0 External Enable: This bit enables the capture/reload function on the T0 pin. An edge trigger (programmable by CAPCON0.CCT0[1:0] bits) detected on the T0 pin will result in capture from free running timer 2 counters to input capture 0 registers, and reload from RCAP2 registers to timer 2 counters if ENLD = 1 and CMP/RL2 = 0.
3	T2CR	Timer 2 Capture Reset: In the Timer 2 Capture Mode this bit enables/disables hardware automatically reset timer 2 while the value in TL2 and TH2 have been transferred into the capture register.
2~0	-	Reserved.

TIMER 2 RELOAD LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

BIT	NAME	FUNCTION
7-0	RCAP2L	Timer 2 Reload LSB: This register is LSB of a 16-bit reload value when timer 2 is configured in reload mode. During compare mode, this register is a compare register. See CMP/RL2 for reload/compare mode.

TIMER 2 RELOAD MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

BIT	NAME	FUNCTION
7-0	RCAP2H	Timer 2 Reload MSB: This register is MSB of a 16-bit reload value when timer 2 is configured in reload mode. During compare mode, this register is a compare register. See CMP/RL2 for reload/compare mode.

TIMER 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

TIMER 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

BIT	NAME	FUNCTION
7-0	TL2	Timer 2 LSB.

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4~3	RS1~RS0	Register bank select bits.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM COUNTER HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7-2	-	Reserved.
1-0	PWMP.[9:8]	The PWM Counter Register bits 9~8.

PWM 0 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM0.9~8	The PWM 0 Register bit 9~8.

PWM 1 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM1.9	PWM1.8

Mnemonic: PWM1H Address: D3h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM1.9~8	The PWM1 Register bit 9~8.

PWM 2 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM2.9	PWM2.8

Mnemonic: PWM2H Address: D5h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM2.9~8	The PWM2 Register bit 9~8.

PWM 3 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM3.9	PWM3.8

Mnemonic: PWM3H Address: D6h

BIT	NAME	FUNCTION
7~2	-	Reserved.
1~0	PWM3.9~8	The PWM3 Register bit 9~8.

PWM CONTROL REGISTER 3

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	PWM1OE	PWM0OE	-	-	FP1	FP0

Mnemonic: PWMCON3 Address: D7h

BIT	NAME	FUNCTION
7	PWM3OE	PWM3 output enable bit. 0: PWM3 output disabled. 1: PWM3 output enabled.
6	PWM2OE	PWM2 output enable bit. 0: PWM2 output disabled. 1: PWM2 output enabled.
5	PWM1OE	PWM1 output enable bit. 0: PWM1 output disabled. 1: PWM1 output enabled.
4	PWM0OE	PWM0 output enable bit. 0: PWM0 output disabled. 1: PWM0 output enabled.
3~2	-	Reserved.
1~0	FP1~0	Select PWM frequency pre-scale select bits. The clock source of pre-scaler is in phase with Fosc if PWMRUN=1, otherwise it is disabled.

FP1~0: PWM Prescaler select bits:

FP[1:0]	FPWM
00	Fosc
01	Fosc/2
10	Fosc/4
11	Fosc/16

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.
5~4	WD1~WD0	Watchdog Timer times selected.

Continued

BIT	NAME	FUNCTION
3	WDIF	Watchdog Timer Interrupt flag: 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.
2	WTRF	Watchdog Timer Reset flag: 1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.
1	EWRST	0: Disable Watchdog Timer Reset. 1: Enable Watchdog Timer Reset.
0	WDCLR	Reset Watchdog Timer: This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt (if EWDI (IE.4) is set), and 512 clocks after that a watchdog timer reset will be generated (if EWRST is set). This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x000000B on a power-on-reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on all resets.

All the bits in this SFR have unrestricted read access. WDRUN, WD0, WD1, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```
TA          REG         C7H
WDCON       REG         D8H
MOV         TA, #AAH                ; To access protected bits
MOV         TA, #55H
SETB        WDCON.0                 ; Reset watchdog timer
ORL         WDCON, #00110000B       ; Select 26 bits watchdog timer
MOV         TA, #AAH
MOV         TA, #55H
ORL         WDCON, #00000010B       ; Enable watchdog timer reset
```

PWM COUNTER LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.1

Mnemonic: PWMPL Address: D9h

BIT	NAME	FUNCTION
7~0	PWMP	PWM Counter Low Bits Register.

PWM 0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.1

Mnemonic: PWM0L Address: DAh

BIT	NAME	FUNCTION
7~0	PWM0	PWM 0 Low Bits Register.

PWM 1 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1L Address: DBh

BIT	NAME	FUNCTION
7~0	PWM1	PWM 1 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	PWMF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and Comparators are never loaded to counter and Comparator registers. 1: The PWMP register will be load value to counter register after counter underflow, and hardware will clear by next clock cycle.
5	PWMF	PWM underflow flag. 0: No underflow. 1: PWM 10-bit down counter underflows (PWM interrupt is requested if PWM interrupt is enabled).
4	CLRPWM	1: Clear 10-bit PWM counter to 000H. It is automatically cleared by hardware.
3	PWM3I	0: PWM3 output is non-inverted. 1: PWM3 output is inverted.

Continued

BIT	NAME	FUNCTION
2	PWM2I	0: PWM2 output is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 output is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 output is non-inverted. 1: PWM0 output is inverted.

PWM 2 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7:0	PWM2	PWM 2 Low Bits Register.

PWM 3 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3L Address: DEh

BIT	NAME	FUNCTION
7~0	PWM3	PWM 3 Low Bits Register.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

BIT	NAME	FUNCTION
7-0	ACC	The A or ACC register is the standard 8052 accumulator.

ADC CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	ADDR2 (W79E834 only)	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

BIT	NAME	FUNCTION
7~6	ADC.1~0	The ADC conversion result.
5	ADCEX	Enable STADC-triggered conversion: 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.4).
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. Notes: 1. It is recommended to clear ADCI ***before*** ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel. 2. Software clearing of ADCS will abort conversion in progress. 3. ADC cannot start a new conversion while ADCS or ADCI is high.
2~0	AADR2~0	The ADC input select. AADR2 bit applicable to W79E834 only.

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

ADDR2, AADR1, AADR0: ADC Analog Input Channel select bits:
These bits can only be changed when ADCI and ADCS are both zero.

AADR2 (W79E834 ONLY)	AADR1	AADR0	SELECTED ANALOG CHANNEL
0	0	0	ADC0 (P0.1)
0	0	1	ADC1 (P0.2)
0	1	0	ADC2 (P0.3)
0	1	1	ADC3 (P0.4)
1	0	0	ADC4 (P0.5) (W79E834 only)
1	0	1	ADC5 (P0.6) (W79E834 only)
1	1	0	ADC6 (P2.6) (W79E834 only)
1	1	1	ADC7 (P2.7) (W79E834 only)

ADC CONVERTER RESULT REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: E2h

BIT	NAME	FUNCTION
7~0	ADC.9~2	The ADC conversion result.

INPUT CAPTURE 0 LOW REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCL0.7	CCL0.6	CCL0.5	CCL0.4	CCL0.3	CCL0.2	CCL0.1	CCL0.0

Mnemonic: CCL0 Address: E4h

BIT	NAME	FUNCTION
7~0	CCL0	Capture 0 low byte.

INPUT CAPTURE 0 HIGH REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCH0.7	CCH0.6	CCH0.5	CCH0.4	CCH0.3	CCH0.2	CCH0.1	CCH0.0

Mnemonic: CCH0 Address: E5h

BIT	NAME	FUNCTION
7~0	CCH0	Capture 0 high byte.

INPUT CAPTURE 1 LOW REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCL1.7	CCL1.6	CCL1.5	CCL1.4	CCL1.3	CCL1.2	CCL1.1	CCL1.0

Mnemonic: CCL1 Address: E6h

BIT	NAME	FUNCTION
7~0	CCL1	Capture 1 low byte.

INPUT CAPTURE 1 HIGH REGISTER

Bit:	7	6	5	4	3	2	1	0
	CCH1.7	CCH1.6	CCH1.5	CCH1.4	CCH1.3	CCH1.2	CCH1.1	CCH1.0

Mnemonic: CCH1 Address: E7h

BIT	NAME	FUNCTION
7~0	CCH1	Capture 1 high byte.

INTERRUPT ENABLE REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	ECPTF	ET2	EPWM	EWDI	ESPI	-	EKB	-

Mnemonic: EIE Address: E8h

BIT	NAME	FUNCTION
7	ECPTF	0: Disable capture interrupts. 1: Enable capture interrupts.
6	ET2	0: Disable Timer 2 Interrupt. 1: Enable Timer 2 Interrupt.
5	EPWM	0: Disable PWM Interrupt when PWM down counter underflow. 1: Enable PWM Interrupt when PWM down counter underflow.
4	EWDI	0: Disable Watchdog Timer Interrupt. 1: Enable Watchdog Timer Interrupt.
3	ESPI	0: Disable SPI Interrupt. 1: Enable SPI Interrupt.
2	-	Reserved.
1	EKB	0: Disable Keypad Interrupt. 1: Enable Keypad Interrupt.
0	-	Reserved.

B REGISTER

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

BIT	NAME	FUNCTION
7-0	B	The B register is the standard 8052 register that serves as a second accumulator.

SERIAL PERIPHERAL CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	SSOE	SPE	LSBFE	MSTR	CPOL	CPHA	SPR1	SPR0

Mnemonic: SPCR Address: F3h

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7</td><td>SSOE</td><td>Slave Select Output Enable Bit.
The $\overline{SS}$ output feature is enabled only in master mode by asserting the SSOE bit. $\overline{SS}$ input not effected by SSOE when the device in slave mode.
0: $\overline{SS}$ input (with mode fault).
1: $\overline{SS}$ output (no mode fault).
<table>
<tr><th>DRSS</th><th>SSOE</th><th>Master Mode</th><th>Slave Mode</th></tr>
<tr><td>0</td><td>0</td><td>$\overline{SS}$ input (With Mode Fault)</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
<tr><td>0</td><td>1</td><td>Reserved</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
<tr><td>1</td><td>0</td><td>$\overline{SS}$ General purpose I/O (No Mode Fault)</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
<tr><td>1</td><td>1</td><td>$\overline{SS}$ output (No Mode Fault)</td><td>$\overline{SS}$ Input (Not affected by SSOE)</td></tr>
</table></td></tr>
<tr><td>6</td><td>SPE</td><td>Serial Peripheral System Enable Bit:
When the SPE bit is set, SPI block functions is enable. When MODF is set, SPE always reads 0.
0: SPI system disabled.
1: SPI system enabled.</td></tr>
<tr><td>5</td><td>LSBFE</td><td>LSB - First Enable:
This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0: Data is transferred least significant bit first.
1: Data is transferred most significant bit first.</td></tr>
<tr><td>4</td><td>MSTR</td><td>Master Mode Select Bit:
It is customary to have an external pull-up resistor on lines that are driven by open-drain devices.
0: Slave mode.
1: Master mode</td></tr>
<tr><td>3</td><td>CPOL</td><td>Clock Polarity Bit:
When the clock polarity bit is cleared and data is not being transferred, the SCK pin of the master device has a steady state low value. When CPOL is set, SCK idles high.</td></tr>
<tr><td>2</td><td>CPHA</td><td>Clock Phase Bit:
The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPHA bit selects one of two different clocking protocols.</td></tr>
</table>

Continued

BIT	NAME	FUNCTION
1~0	SPR1~0	SPI Baud Rate Selection Bits: These bits specify the SPI baud rates.

SPR1	SPR0	Divider
0	0	Reserved
0	1	16
1	0	64
1	1	128

Note: In master mode, a change of LSBFE, MSTR, CPOL, CPHA and SPR [1:0] will abort a transmission in progress and force the SPI system into idle state.

SERIAL PERIPHERAL STATUS REGISTER

Bit:	7	6	5	4	3	2	1	0
	SPIF	WCOL	SPOVF	MODF	DRSS	-	-	-

Mnemonic: SPSR Address: F4h

BIT	NAME	FUNCTION
7	SPIF	SPI Interrupt Complete Flag: SPIF is set upon completion of data transfer between this device and external device or when new data has been received and copied to the SPDR. If SPIF goes high, and if ESPI (located at EIE.3) is set, a serial peripheral interrupt is generated. SPIF is clear by software, by writing a 0.
6	WCOL	Write Collision Bit: Clearing the WCOL bit is accomplished by software writing a 0. 0: No write collision. 1: Write collision.
5	SPOVF	SPI overrun flag: SPIOVF is set if a new character is received before a previously received character is read from SPDR. Once this bit is set, it will prevent SPDR register from accepting new data. It must be cleared before any new data can be written. This flag is cleared by software, by writing a 0. 0: No overrun. 1: Overrun detected.
4	MODF	SPI Mode Error Interrupt Status Flag: Clearing this bit is by software writing a 0. 0: No mode fault. 1: Mode fault.
3	DRSS	Data Register Slave Select: Refer to above table in SPCR register.
2~0	-	Reserved.

SERIAL PERIPHERAL DATA I/O REGISTER

Bit:	7	6	5	4	3	2	1	0
	SPD.7	SPD.6	SPD.5	SPD.4	SPD.3	SPD.2	SPD.1	SPD.0

Mnemonic: SPDR Address: F5h

BIT	NAME	FUNCTION
7-0	SPDR	SPDR is used when transmitting or receiving data on serial bus.

PORT ADC DIGITAL INPUT DISABLE

Bit:	7	6	5	4	3	2	1	0
	PADIDS.7 (W79E834 only)	PADIDS.6 (W79E834 only)	PADIDS.5 (W79E834 only)	PADIDS.4 (W79E834 only)	PADIDS.3	PADIDS.2	PADIDS.1	PADIDS.0

Mnemonic: PADIDS Address: F6h

BIT	NAME	FUNCTION
7	PADIDS.7	P2.7 digital input disable bit (W79E834 only). 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 7.
6	PADIDS.6	P2.6 digital input disable bit (W79E834 only). 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 6.
5	PADIDS.5	P0.6 digital input disable bit (W79E834 only). 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 5.
4	PADIDS.4	P0.5 digital input disable bit (W79E834 only). 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 4.
3	PADIDS.3	P0.4 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 3.
2	PADIDS.2	P0.3 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 2.
1	PADIDS.1	P0.2 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 1.
0	PADIDS.0	P0.1 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 0.

Note : This SFR is a write-only register.

INTERRUPT HIGH PRIORITY 1

Bit:	7	6	5	4	3	2	1	0
	PCAPH	PT2H	PPWMH	PWDIH	PSPIH	-	PKBH	-

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	PCAPH	1: To set interrupt high priority of Capture 0/1/2 as highest priority level.
6	PT2H	1: To set interrupt high priority of Timer 2 is highest priority level.
5	PPWMH	1: To set interrupt high priority of PWM's underflow is highest priority level.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3	PSPIH	1: To set interrupt high priority of SPI is highest priority level.
2	-	Reserved.
1	PKBH	1: To set interrupt high priority of Keypad is highest priority level.
0	-	Reserved.

INTERRUPT PRIORITY 1

Bit:	7	6	5	4	3	2	1	0
	PCAP	PT2	PPWM	PWDI	PSPI	-	PKB	-

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	PCAP	1: To set interrupt priority of Capture 0/1/2 as higher priority level.
6	PT2	1: To set interrupt priority of Timer 2 is higher priority level.
5	PPWM	1: To set interrupt priority of PWM's underflow is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3	PSPI	1: To set interrupt priority of SPI is higher priority level.
2	-	Reserved.
1	PKB	1: To set interrupt priority of Keypad is higher priority level.
0	-	Reserved.

9. INSTRUCTION SET

The W79E834 series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly the same. However, the timing of these instructions is different in two ways. Firstly, the machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Secondly, it can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can fetch twice per machine cycle (i.e., six clocks per fetch).

The timing differences create an advantage for the W79E834 series. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the W79E834 series reduce the number of dummy fetches and wasted cycles, and therefore improves overall efficiency, compared to the standard 8051/52.

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3
ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5

Continued

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3

Continued

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
DEC DPTR	A5	1	2	8	24	3
MUL AB	A4	1	5	20	48	2.4
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3
ANL A, R6	5E	1	1	4	12	3
ANL A, R7	5F	1	1	4	12	3
ANL A, @R0	56	1	1	4	12	3
ANL A, @R1	57	1	1	4	12	3
ANL A, direct	55	2	2	8	12	1.5
ANL A, #data	54	2	2	8	12	1.5
ANL direct, A	52	2	2	8	12	1.5
ANL direct, #data	53	3	3	12	24	2
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3

Continued

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
ORL A, @R1	47	1	1	4	12	3
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3

Continued

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5

Continued

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3

Continued

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	6	24	3
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
LCALL addr16	12	3	4	16	24	1.5
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
LJMP addr16	02	3	4	16	24	1.5
JMP @A+DPTR	73	1	2	6	24	3
SJMP rel	80	2	3	12	24	2
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2

Continued

OP-CODE	HEX CODE	BYTES	W79E834 SERIES MACHINE CYCLE	W79E834 SERIES CLOCK CYCLES	8032 CLOCK CYCLES	W79E834 SERIES VS. 8032 SPEED RATIO
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

Table 9-1: Instruction Set for W79E834 series

9.1 Instruction Timing

This section is important because some applications use software instructions to generate timing delays. It also provides more information about timing differences between the W79E834 series and the standard 8051/52.

In W79E834 series, each machine cycle is four clock periods long. Each clock period is called a state, and each machine cycle consists of four states: C1, C2 C3 and C4, in order. Both clock edges are used for internal timing, so the duty cycle of the clock should be as close to 50% as possible to avoid timing conflicts.

The W79E834 series perform one op-code fetch per machine cycle, so, in most instructions, the number of machine cycles required is equal to the number of bytes in the instruction. There are 256 available op-codes. 128 of them are single-cycle instructions, so many op-codes are executed in just four clocks period. Some of the other op-codes are two-cycle instructions, and most of these have two-byte op-codes. However, there are some instructions that have one-byte instructions yet take two cycles to execute. One important example is the MOVX instruction.

In the standard 8052, the MOVX instruction is always two machine cycles long. However, in the W79E834 series each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8052. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8052 in terms of clock periods.

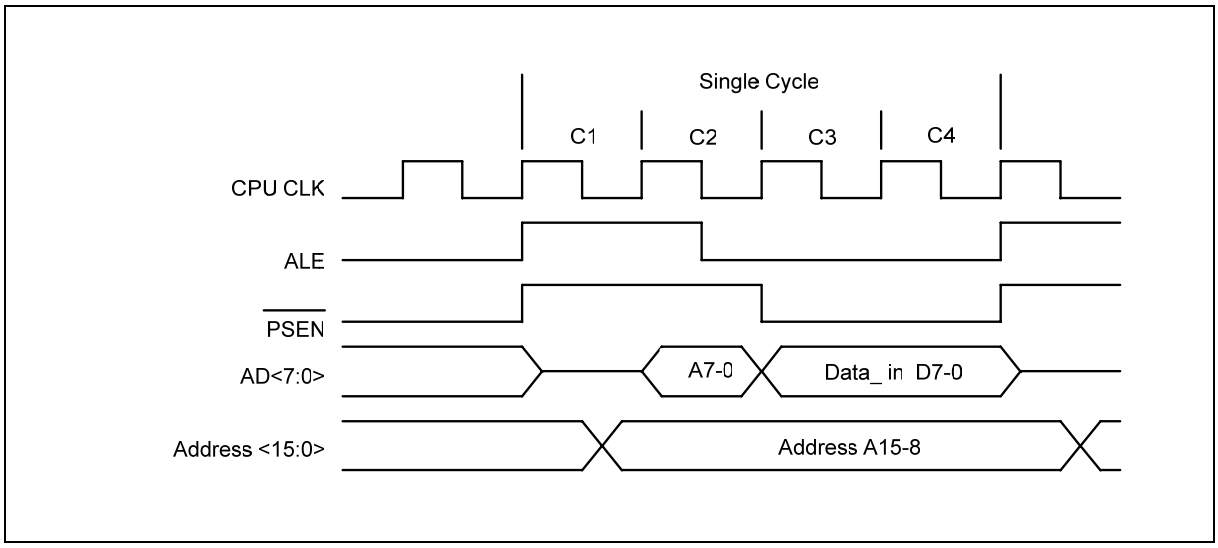


Figure 9-1: Single Cycle Instruction Timing

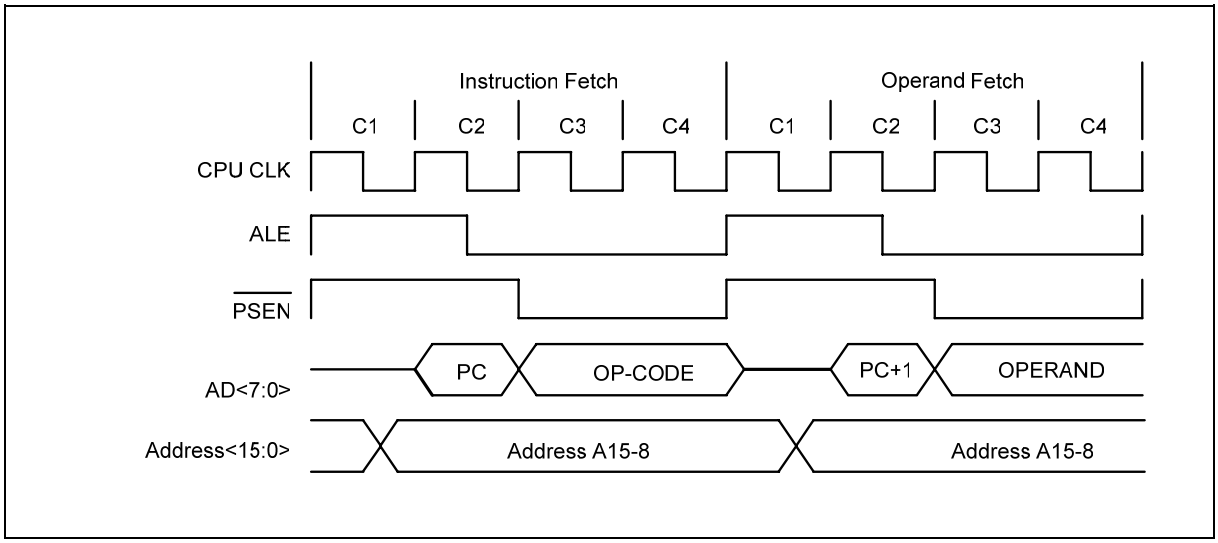


Figure 9-2: Two Cycles Instruction Timing

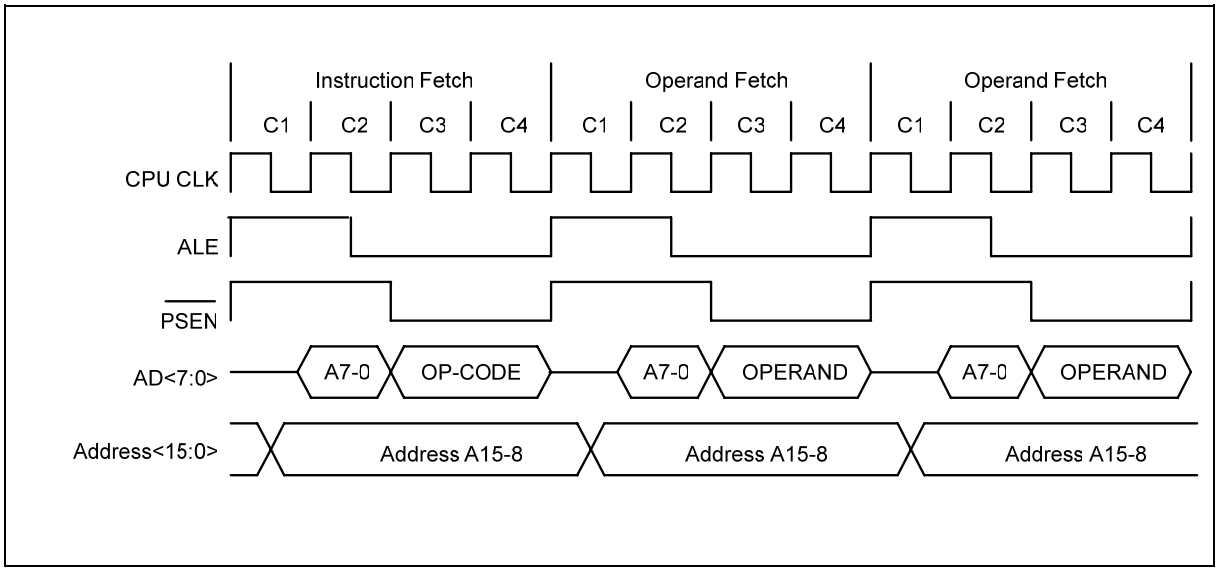


Figure 9-3: Three Cycles Instruction Timing

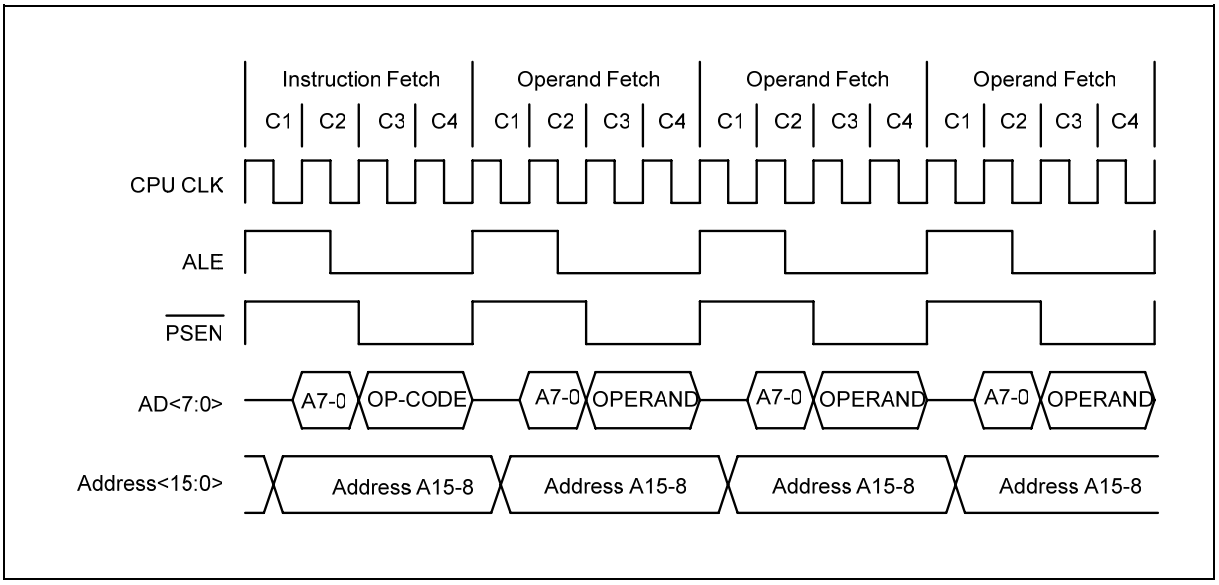


Figure 9-4: Four Cycles Instruction Timing

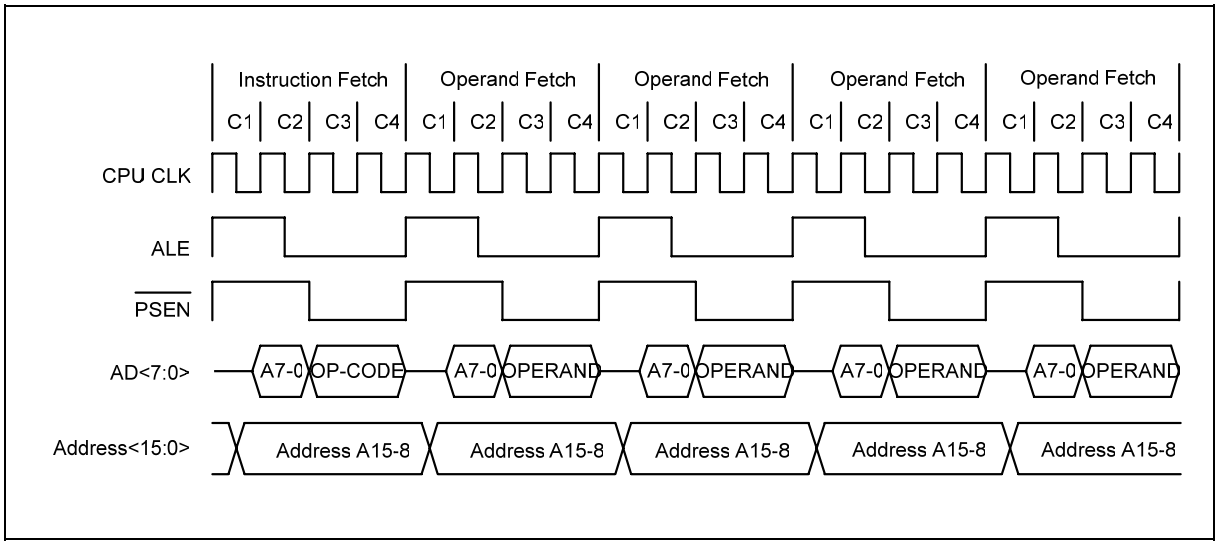


Figure 9-5: Five Cycles Instruction Timing

10. POWER MANAGEMENT

W79E834 series are provided with idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections, followed by a discussion of resets.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle Mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a low on the external /RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held low for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When W79E834 series are exiting from an Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

10.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The W79E834 series will exit the Power Down mode with a reset or by an external interrupt pin. An external reset can be used to exit the Power down state. The low on /RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power down mode are external interrupts, keyboard interrupt (KBI), brownout reset (BOR), and ADC. Note that for ADC waking up from powerdown, the device need to run on internal rc and software perform start ADC prior to powerdown.

The W79E834 series can be waken up from the Power Down mode by forcing an external interrupt pin activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then either a low-level or a falling-edge at external interrupt pin will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

11. RESET CONDITIONS

The user has several hardware related options for placing W79E834 series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. The sources of resets are external reset, power-on-reset, watchdog timer reset and software reset (brownout is also able to reset the device if enabled).

11.1 External Reset

The device continuously samples the /RST pin at state C4 of every machine cycle. Therefore the /RST pin must be held low for at least 2 machine cycles to ensure detection of a valid /RST low. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as /RST is 0. Even after /RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

11.2 Power-On Reset (POR)

The software must clear the POR flag after reading it. Otherwise it will not be possible to correctly determine future reset sources. If the power fails, then the device will once again go into reset state. When the power returns to the proper operating levels, the device will again perform a power on reset delay and set the POR flag.

11.3 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

11.4 S/W reset

User can software reset the device by setting SRST bit in SFR AUXR1.

11.5 Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The SFRs have FFh written into them which puts the port pins in a high state.

For SFR reset value, see SFR description table section.

The WDCON SFR bits are set or cleared in reset condition depending on the source of the reset.

WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0x00B Watchdog reset: 0x00 0100B Power on reset 0x000000B

The WTRF bit WDCON.2 is set when the Watchdog timer causes a reset. A power on reset will also clear this bit. The EWRST bit WDCON.1 is cleared by all resets. This disables the Watchdog timer resets.

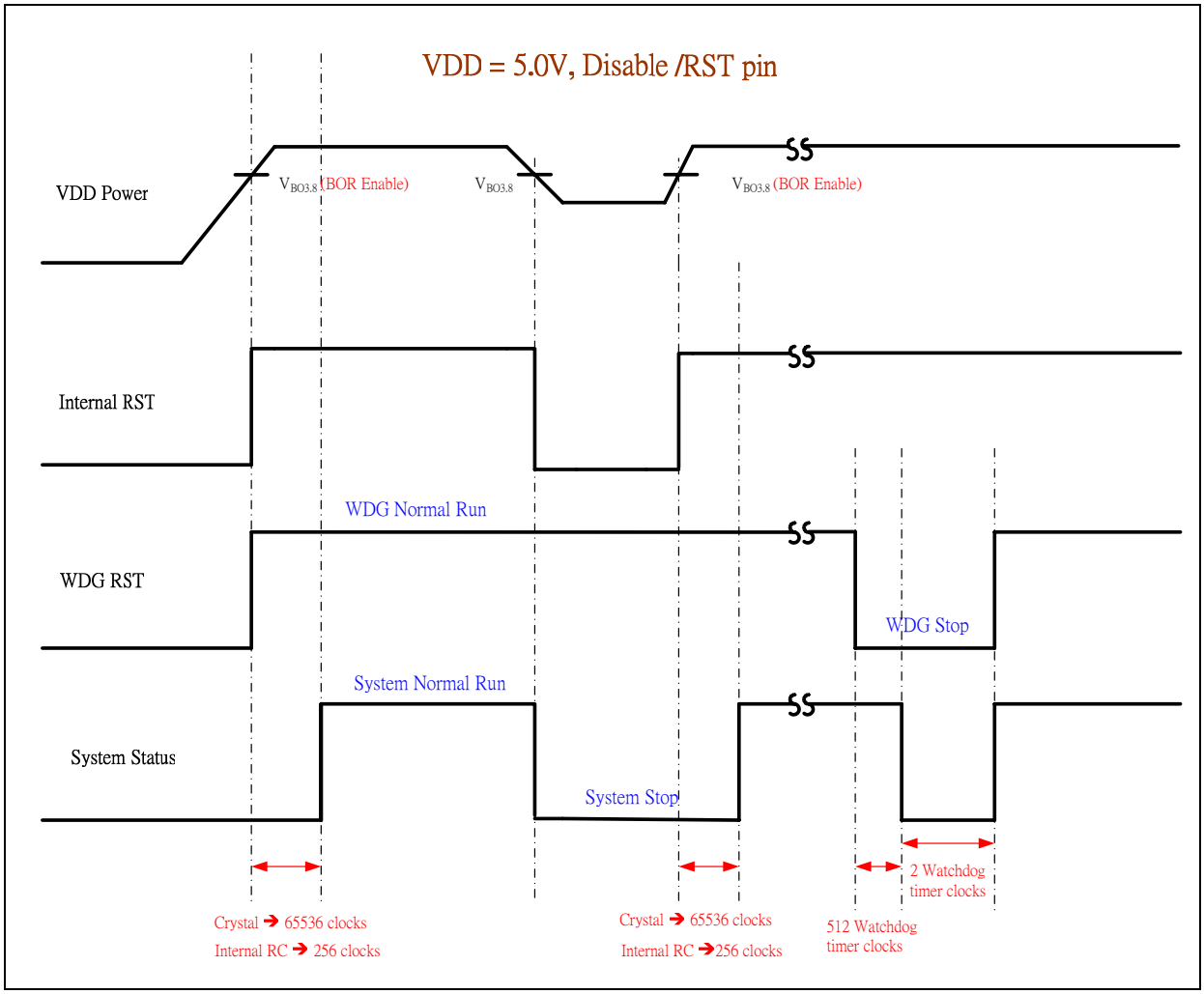


Figure 11-1: Internal reset and VDD monitor timing diagram

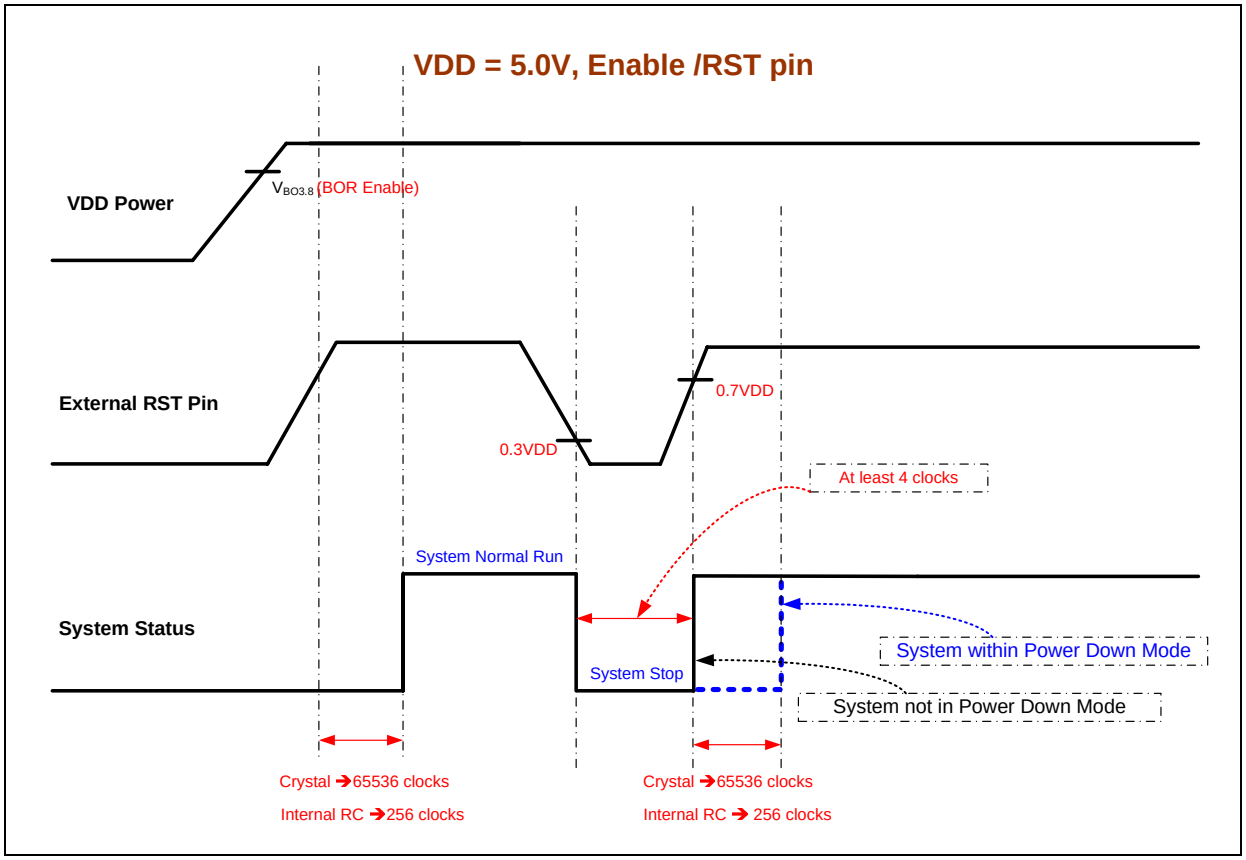


Figure 11-2: External reset timing diagram

12. INTERRUPTS

W79E834 series have four priority level interrupts structure with 13 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

12.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1 (SFR TCON). The bits IE0 and IE1 in TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The timer 2 interrupt is generated through TF2 (timer 2 overflow/compare match). The hardware does not clear these flags when a timer 2 interrupt is executed.

The capture interrupt is generated through logical OR CPTF0-2 flags. CPTF0-2 flags are set by capture/reload events. The hardware does not clear these flags when the capture interrupt is executed. Software has to resolve the cause of the interrupt among CPTF0-2, and clear the appropriate flag.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

SPI asserts interrupt flag, SPIF, upon completion of data transfer with an external device. If SPI interrupt is enabled (ESPI at EIE.3), a serial peripheral interrupt is generated. SPIF flag is software clear, by writing a 0. MODF and SPIOVF also will generate interrupt if occur. They share the same vector address as SPIF.

Keyboard interrupt is generated when any of the keypad connected to P0 pins is pressed. Each keypad interrupt can be individually enabled or disabled. User will have to software clear the flag bit.

PWM interrupt is generated when its' 10-bit down counter underflows. PWMF flag is set and PWM interrupt is generated if enabled. PWMF is set by hardware and can only be cleared by software.

The ADC can generate interrupt after finished ADC converter. There is one interrupt source, which is obtained by the ADCI bit in the ADCCON SFR. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBO (IE.5) and global interrupt enable are set.

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Brownout Interrupt	002Bh
-	0033h	KBI Interrupt	003Bh
Timer 2 Overflow	0043h	SPI Interrupt	004Bh
Watchdog Timer	0053h	ADC Interrupt	005Bh
-	0063h	Capture Interrupt	006Bh
PWM Interrupt	0073h	-	007Bh

Table 12- 1: W79E834 series interrupt vector table

12.2 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low and lowest. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table 12- 2: Four-level interrupts priority.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being execute.

3. The current instruction does not involve a write to IE, EIE, IP0, IP0H, IP1 or IPH1 registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on Table 12- 3: Summary of interrupt sources. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

W79E834 series use a four priority level interrupt structure. This allows great flexibility in controlling the handling of the interrupt sources.

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPXH	IPX	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 12- 2: Four-level interrupts priority

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE or EIE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

Table below summarizes the interrupt sources, flag bits, vector address, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

SOURCE	FLAG	VECTOR ADDRESS	ENABLE BIT	FLAG CLEARED BY	PRIORITY BIT	ARBITRATION RANKING	POWER-DOWN WAKEUP
External Interrupt 0	IE0	0003H	EX0 (IE.0)	Hardware, Software	IP0H.0, IP0.0	1(highest)	Yes
Brownout Detect	BOF	002BH	EBO (IE.5)	Hardware	IP0H.5, IP0.5	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (EIE.4)	Software	IP1H.4, IP1.4	3	Yes
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	Hardware, Software	IP0H.1, IP0.1	4	No
SPI	SPIF + MODF + SPIOVF	004BH	ESPI (EIE.3)	Software	IP1H.3, IP1.3	5	No
A/D Converter	ADCI	005BH	EADC (IE.6)	Software	IP0H.6, IP0.6	6	Yes
External Interrupt 1	IE1	0013H	EX1 (IE.2)	Hardware, Software	IP0H.2, IP0.2	7	Yes
KBI	KBF	003BH	EKB (EIE.1)	Software	IP1H.1, IP1.1	8	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	Hardware, Software	IP0H.3, IP0.3	9	No
Serial Port	RI + TI	0023H	ES (IE.4)	Software	IP0H.4, IP0.4	10	No
Timer 2 Overflow/ Match	TF2	0043H	ET2 (EIE.6)	Software	IP1H.6, IP1.6	11	No
Capture	CPTF0-2	006BH	ECPTF (EIE.7)	Software	IP1H.7, IP1.7	12	No
PWM	PWMF	0073H	EPWM (EIE.5)	Software	IP1H.5, IP1.5	13 (lowest)	No

Table 12- 3: Summary of interrupt sources

Note: 1. The Watchdog Timer and ADC Converter can wake up Power Down Mode when its clock source is used internal RC.

12.3 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{\text{INT0}}$ to RI+TI, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all

three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, EIE, IP0, IP0H, IP1 or IP1H and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, EIE, IP0, IP0H, IP1 or IP1H access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycle is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

12.4 Interrupt Inputs

W79E834 series have two individual interrupt inputs as well as the Keyboard Interrupt function. The latter is described separately elsewhere in this section. Two interrupt inputs are identical to those present on the standard 80C51 microcontroller.

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITn = 0, external interrupt n is triggered by a detected low at the INTn pin. If ITn = 1, external interrupt n is edge triggered. In this mode if successive samples of the INTn pin show a high in one cycle and a low in the next cycle, interrupt request flag IEn in TCON is set, causing an interrupt request.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is high for at least one machine cycle, and then hold it low for at least one machine cycle. This is to ensure that the transition is seen and that interrupt request flag IEn is set. IEn is automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source must hold the request active until the requested interrupt is actually generated. If the external interrupt is still asserted when the interrupt service routine is completed another interrupt will be generated. It is not necessary to clear the interrupt flag IEn when the interrupt is level sensitive, it simply tracks the input pin level.

If an external interrupt is enabled when the device is put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation. Refer to the section on Power Management for details.

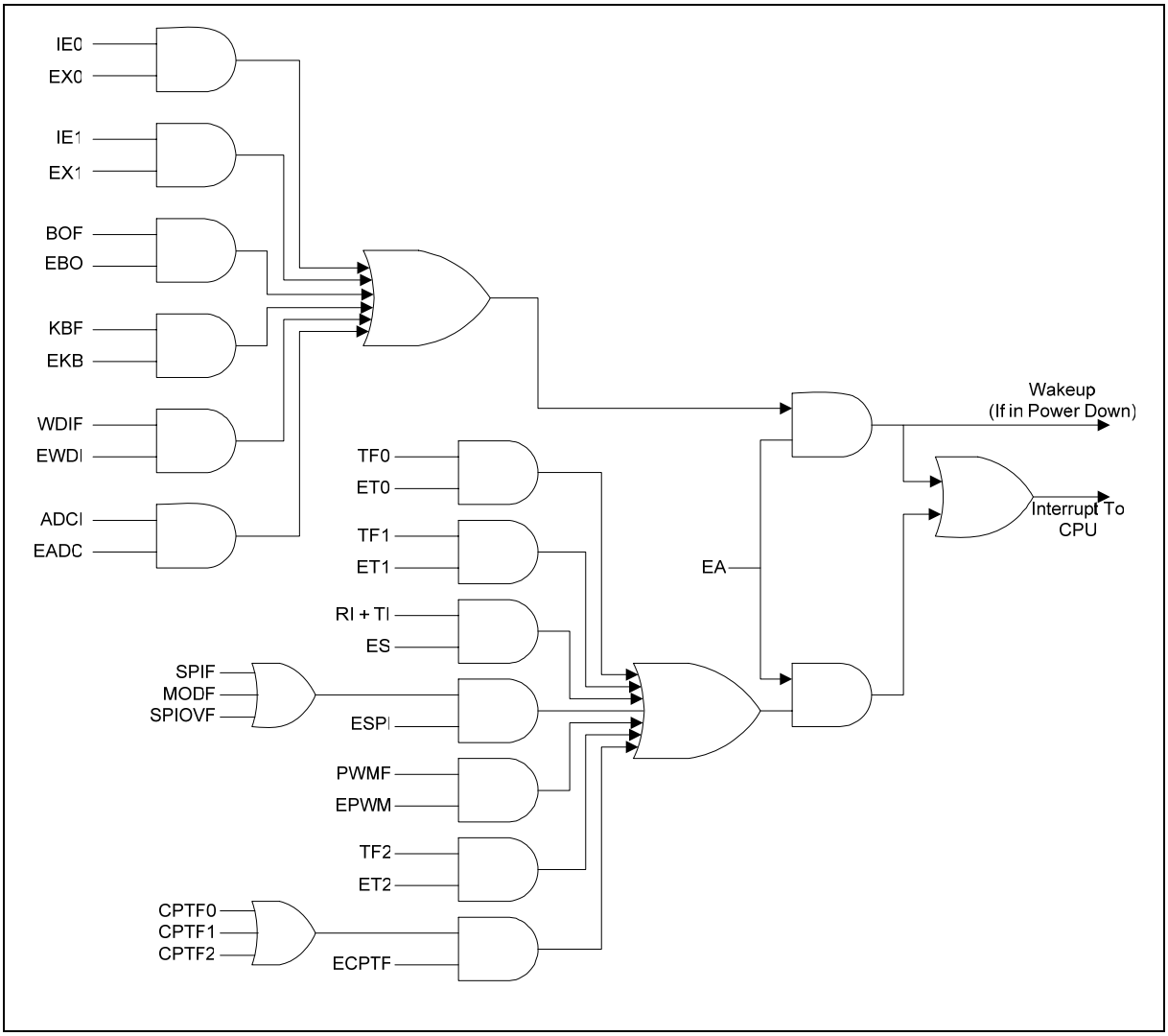


Figure 12- 1: Interrupt inputs

13. PROGRAMMABLE TIMERS/COUNTERS

W79E834 series have two 16-bit programmable timer/counters and one programmable Watchdog Timer. The Watchdog Timer is operationally quite different from the other two timers.

13.1 TIMER/COUNTERS 0 & 1

W79E834 series have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

13.2 Time-Base Selection

W79E834 series provide users with two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on W79E834 series and the standard 8051 can be matched. This is the default mode of operation of the W79E834 series timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bit in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

13.3 MODE 0

In Mode 0, the timer/counters act as an 8-bit counter with a 5-bit, divide by 32 pre-scale. In this mode we have a 13-bit timer/counter. The 13-bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock is increments count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set and either GATE = 0 or $\overline{INTx}$ = 1. When C/$\overline{T}$ is set to 0, then it will count clock cycles, and if C/$\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P1.2) for timer 0 and T1 (P0.7) for timer 1. When the 13-bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur.

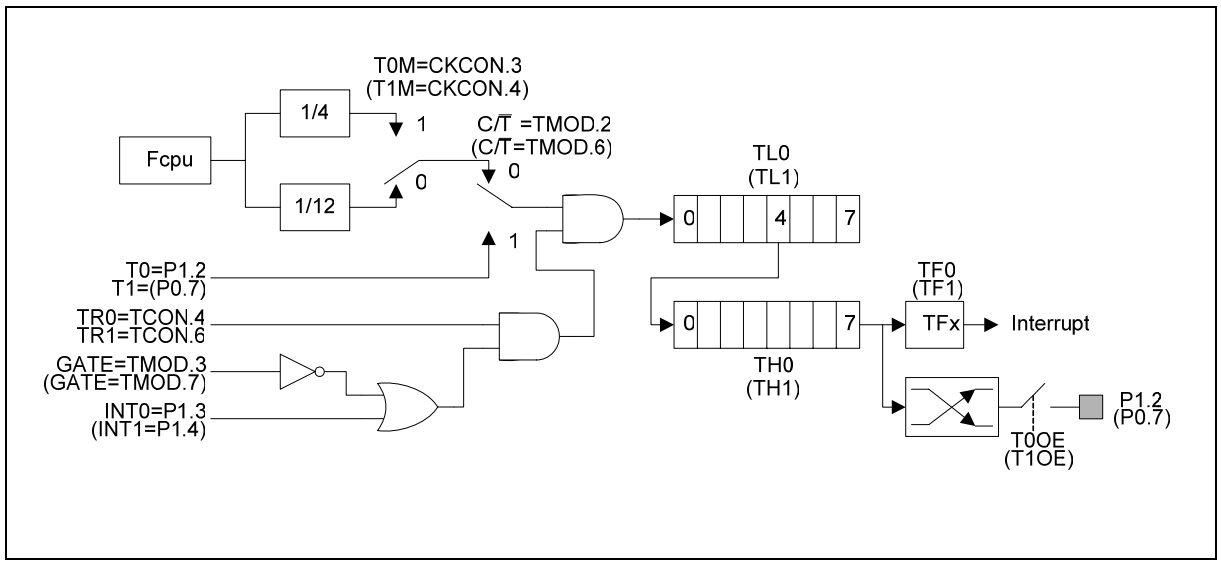


Figure 13- 1: Timer 0/1 Mode 0

13.4 MODE 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

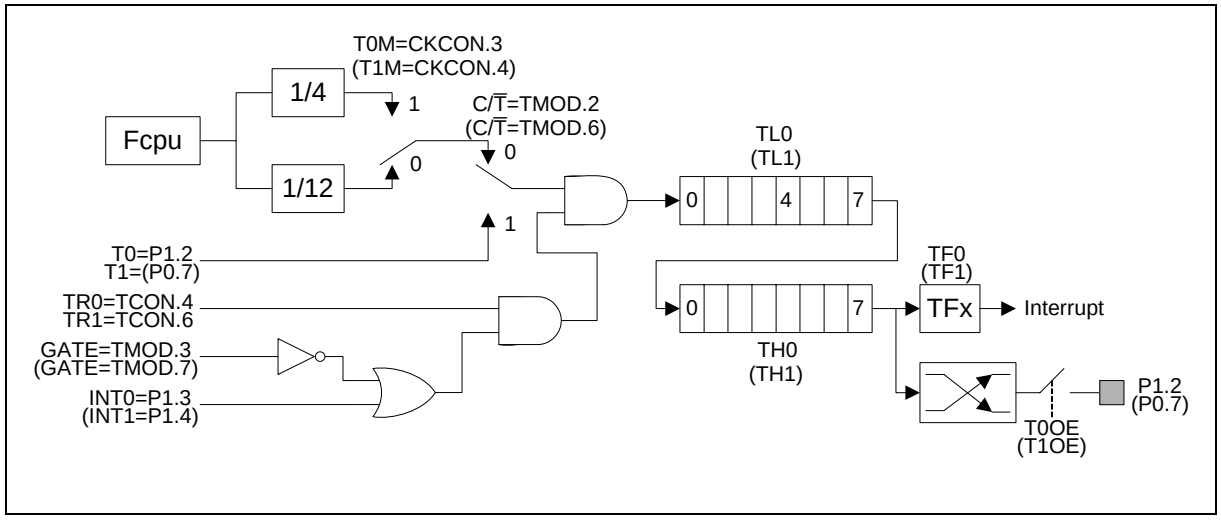


Figure 13- 2: Timer 0/1 Mode 1

13.5 MODE 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as an 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{\text{INTx}}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

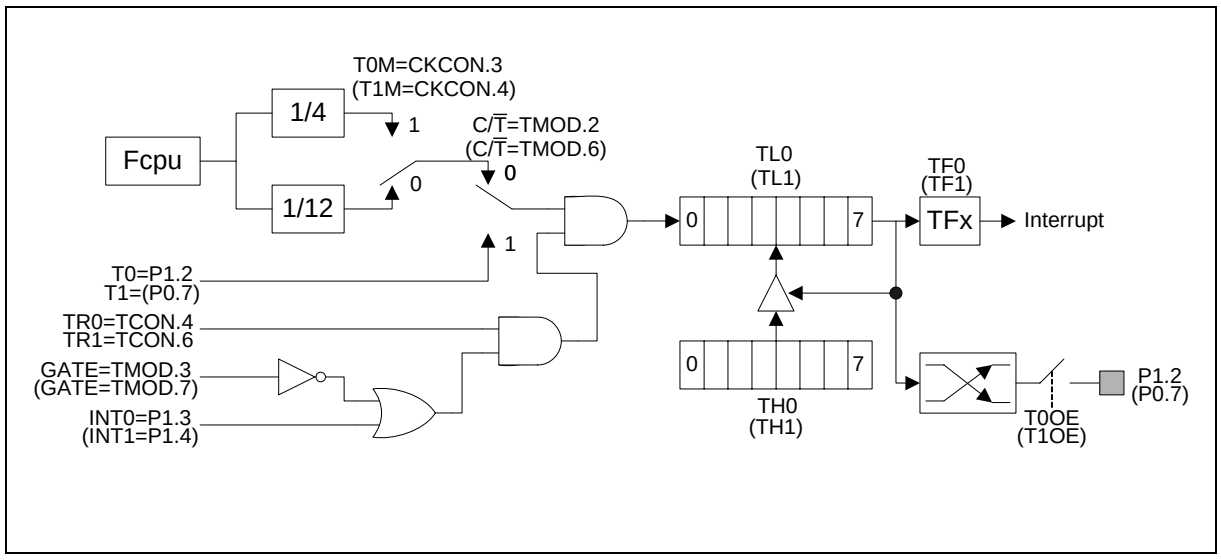


Figure 13- 3: Timer 0/1 Mode 2 (8-bit Auto-reload Mode)

13.6 MODE 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. TL0 uses the Timer/Counter 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0-2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

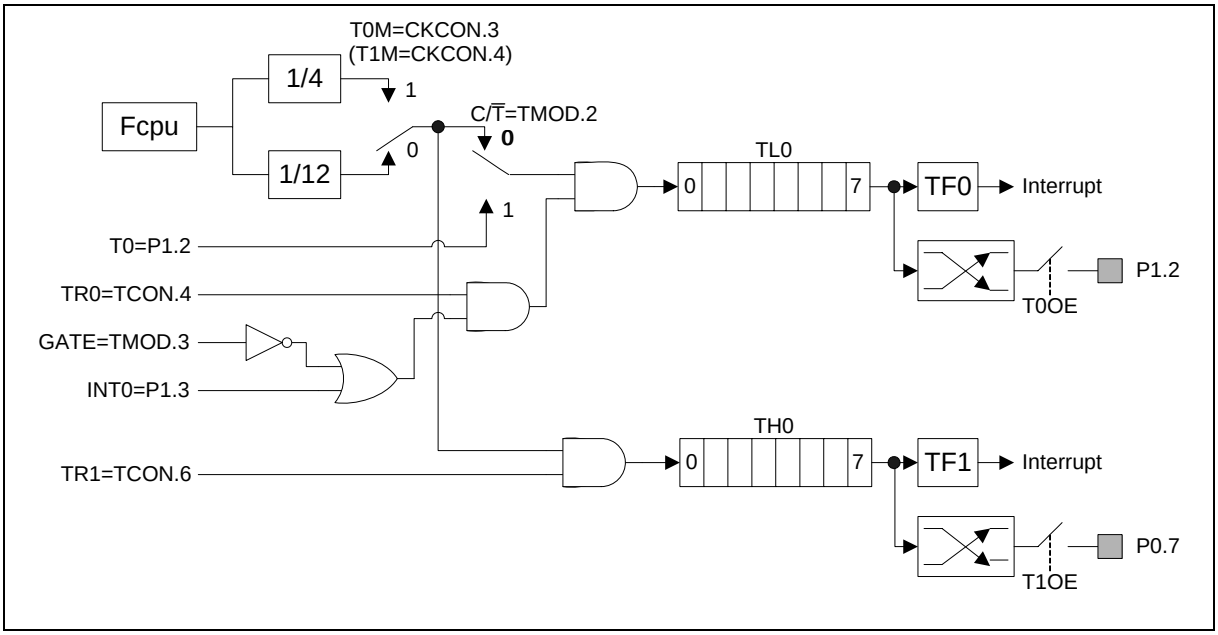


Figure 13- 4: Timer 0/1 Mode 3 (Two 8-bit Counters)

14. WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

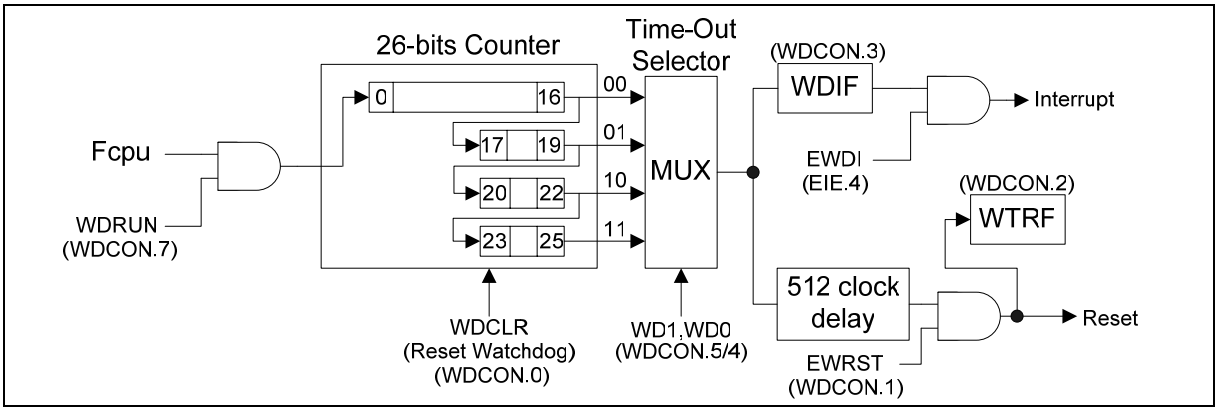


Figure 14- 1: Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If

any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock speed. The reset will occur, when enabled, 512 clocks after the time-out has occurred.

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 10 MHZ
0	0	2^{17}	131072	13.11 mS
0	1	2^{20}	1048576	104.86 mS
1	0	2^{23}	8388608	838.86 mS
1	1	2^{26}	67108864	6710.89 mS

Table 14- 1: Time-out values for the Watchdog timer

The Watchdog Timer will be disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state.

The control bits that support the Watchdog Timer are discussed on the following section.

14.1 WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWRST = 0, then this bit will not be affected by the Watchdog Timer.

EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

14.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The WDRUN, WD0, WD1, EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

15. TIMER2/INPUT CAPTURE MODULES

Timer/Counter 2 is a 16 bit up counter which is configured by the T2MOD register and controlled by the T2CON register. Timer/Counter 2 is also equipped with 3 input captures and reloads capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 crystal oscillator is divided by 1,4,16 or 32 (selectable with CCDIV.1~0 in CKCON SFR). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

15.1 Capture Mode

The capture modules are function to detect and measure pulse width and period of a square wave. It supports 3 capture inputs and digital noise rejection filter. The modules are configured by CAPCON0 and CAPCON1 SFR registers. Input Capture 0, 1 & 2 have their own edge detector but share with one timer i.e. Timer 2. The Input Capture pins are in the structure with Schmitt trigger. For this operation it basically consists of;

- 3 capture module function blocks
- Timer 2 block

Each capture module block consists of 2 bytes capture registers, noise filter and programmable edge triggers. Noise Filter is used to filter the unwanted glitch or pulse on the trigger input pin. The noise filter can be enabled through bit ENFx (CAPCON1). If enabled, the capture logic required to sample 4 consecutive same capture input value in order to recognize an edge as a capture event. A possible implementation of digital noise filter is as follow;

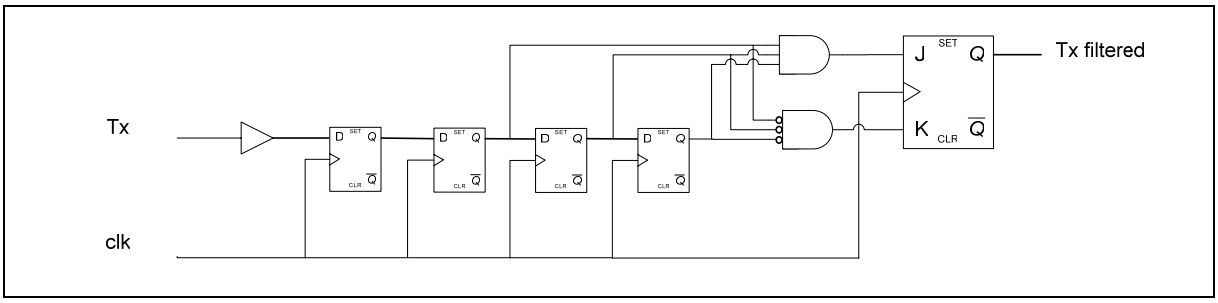


Figure 15- 1: Noise filter

The interval between pulses requirement for input capture is 1 machine cycle width, which is the same as the pulse width required to guarantee a trigger for all trigger edge mode. For less than 3 system clocks, anything less than 3 clocks will not have any trigger and pulse width of 3 or more but less than 4 clocks will trigger but will not guarantee 100% because input sampling is at stage C3 of the machine cycle.

The trigger option is programmable through CCTx.1~0 (CAPCON0). It supports positive edge, negative edge and both edge triggers. Each capture module consists of an enable, ICEN0-2.

[Note: x=0/1/2, for capture 0/1/2 block].

Programming note: When using digital filter function user is recommended to enable digital filter (CAPCON1.ENF* bit) first prior to enable input capture (T2MOD.ICEN*) to avoid false trigger.

Timer/Counter 2 serves as a 16 bit up counter. It supports reload and compared modes. More details are described in next sections.

Capture blocks are trigger by external pins T0, T1 and T2, respectively. If ICENx is enabled, each time the external pin trigger, the content of the free running 16 bits counter, TL2 & TH2 (from Timer 2 block) will be captured/transferred into the capture registers, CCLx and CCHx, depending which external pin trigger. This action also causes the CPTFx flag bit in CAPCON1 to be set, which will also generate an interrupt (if enabled by ECPTF bit in SFR EIE.7). The CPTF0-2 flags are logical “OR” to the interrupt module. Flag is set by hardware and clear by software. Software will have to resolve on the priority of the interrupt flags.

Setting the T2CR bit (T2MOD.3), will allow hardware to reset timer 2 automatically after the value of TL2 and TH2 have been captured. Priority is given to T2CR to reset counter after capture the timer value into the capture register.

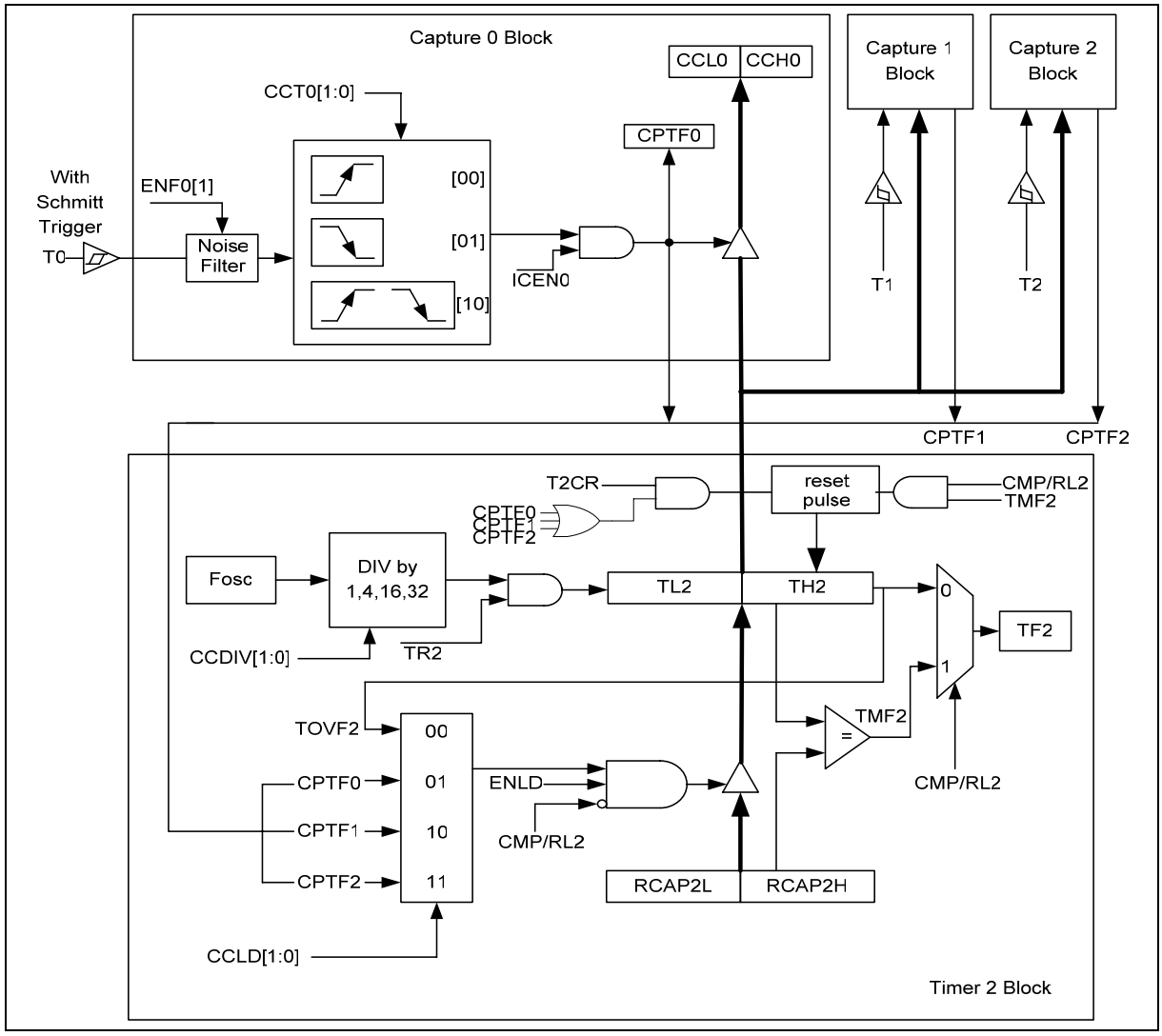


Figure 15- 2: Timer2/capture modules

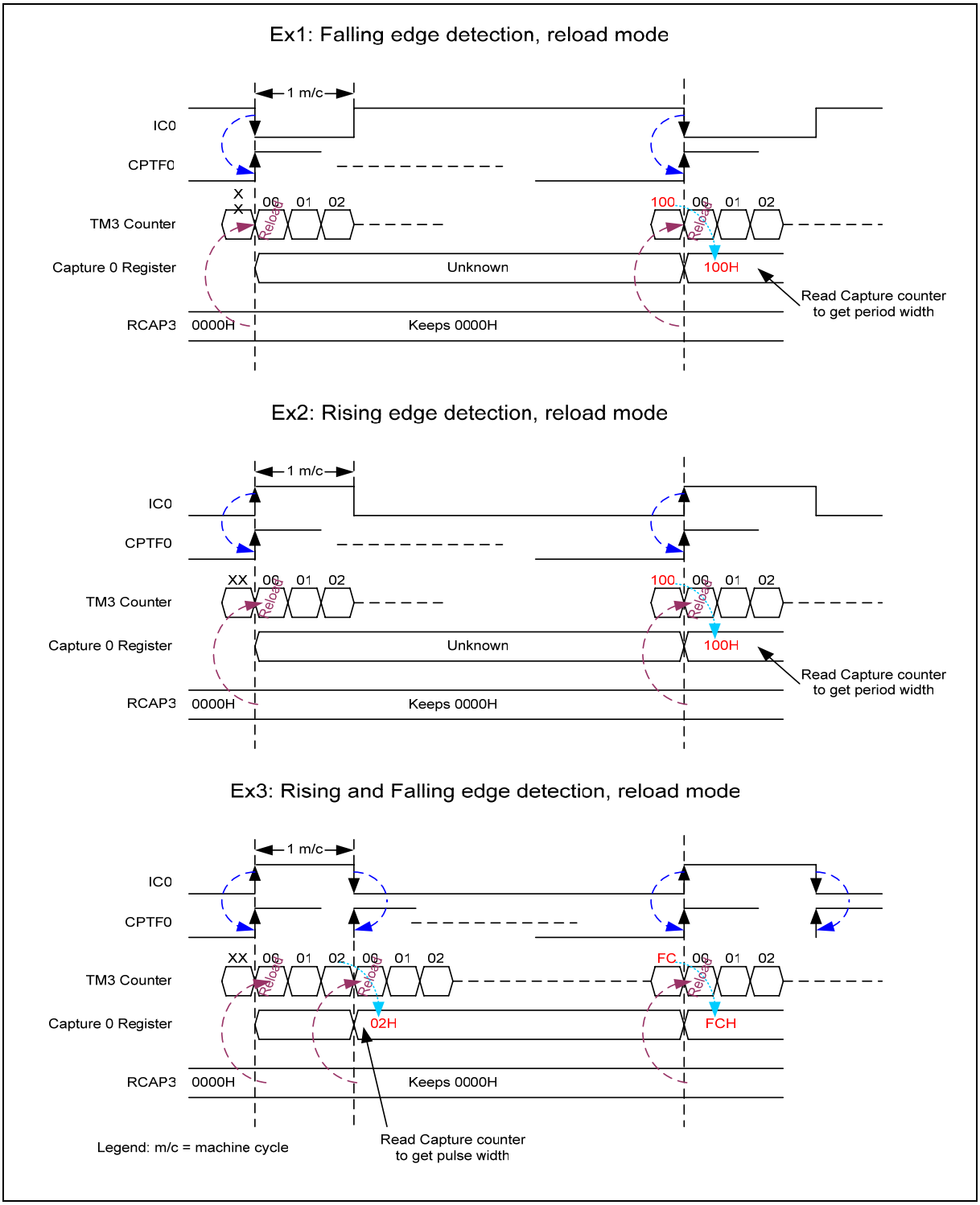


Figure 15- 3: Timing diagram for Input Capture

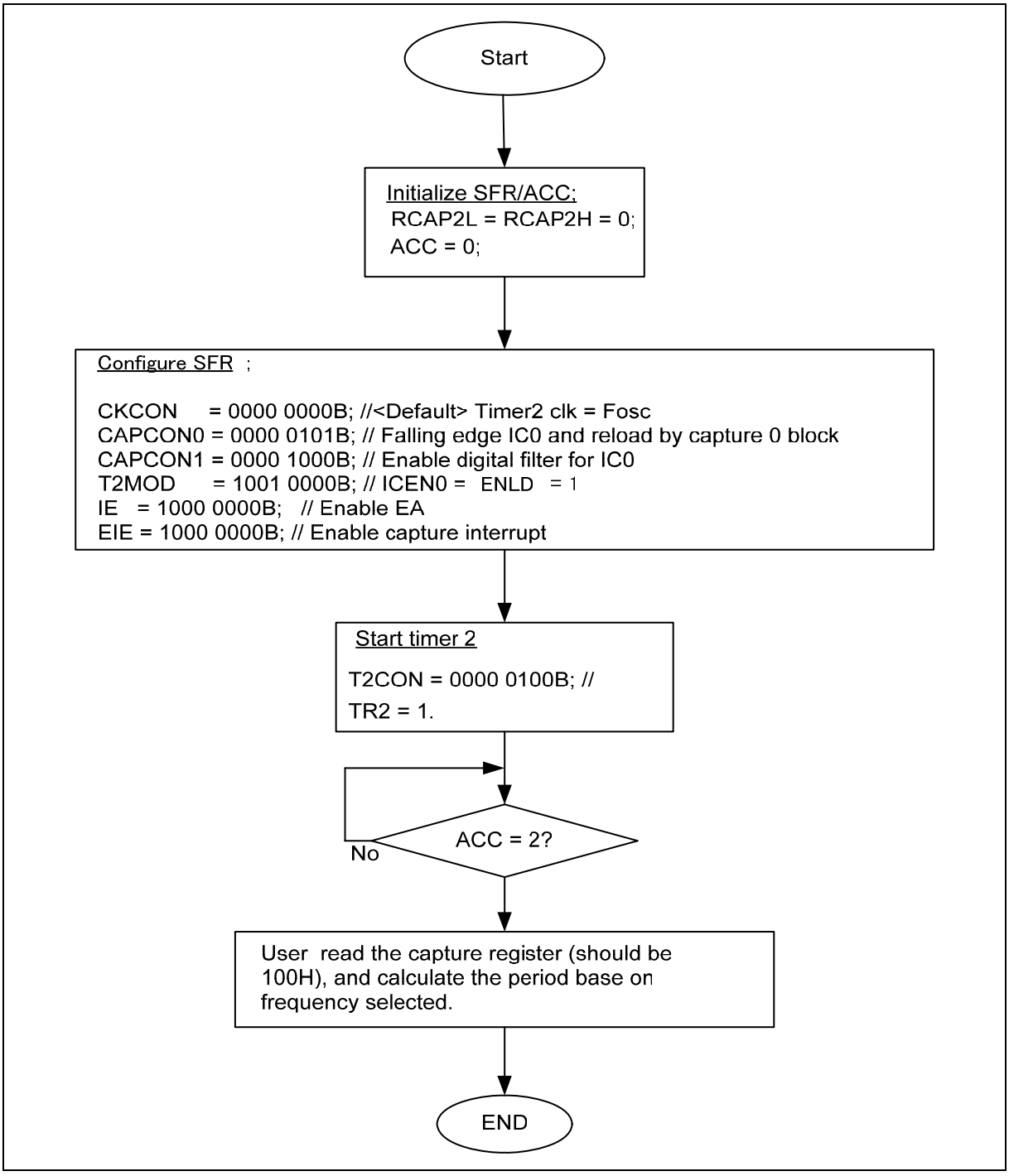


Figure 15- 4: Program flow for measurement with T0 between pulses with falling edge detection (ACC is incremented in interrupt service routine).

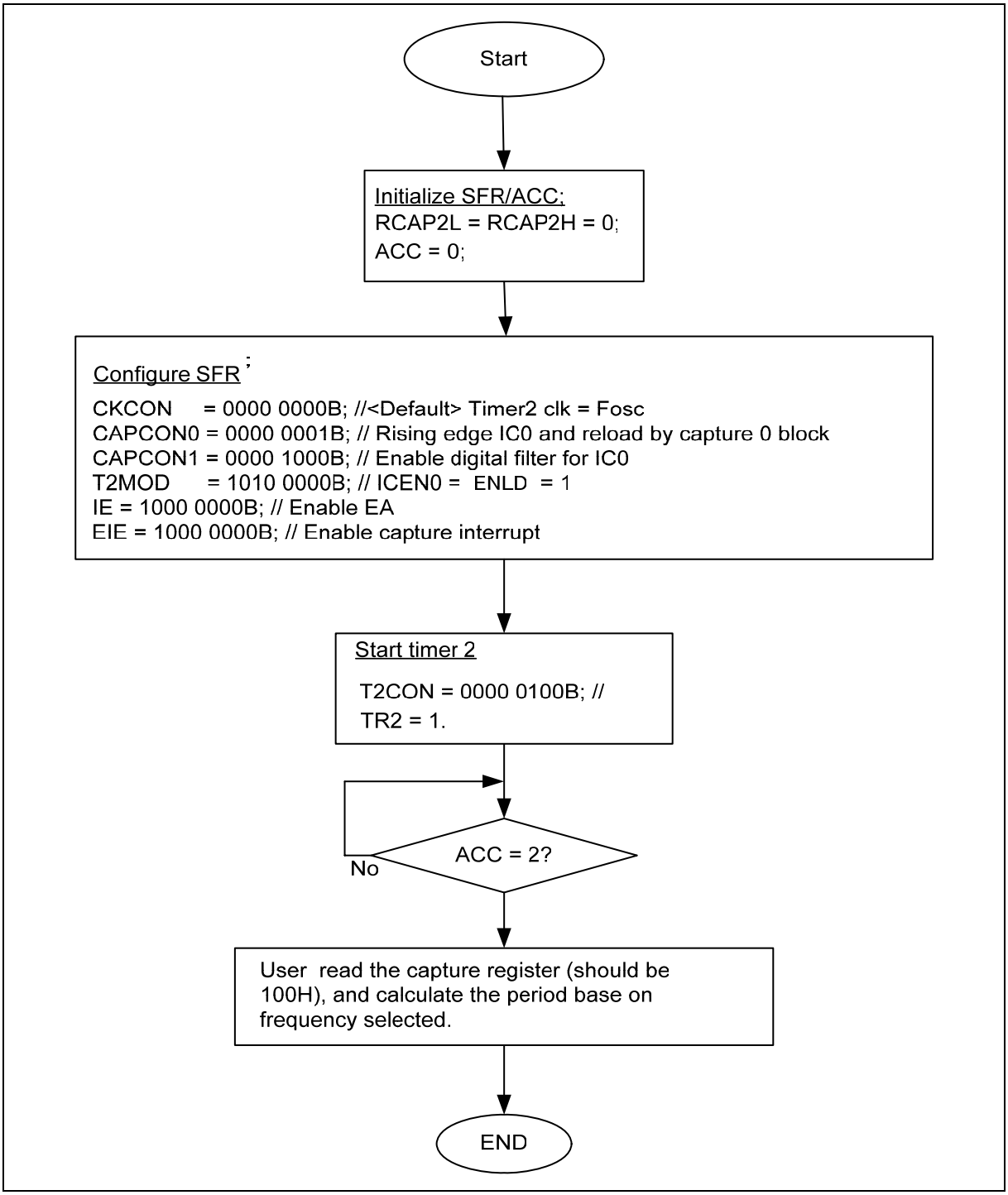


Figure 15- 5: Program flow for measurement with T0 between pulses with rising edge detection (ACC is incremented in interrupt service routine).

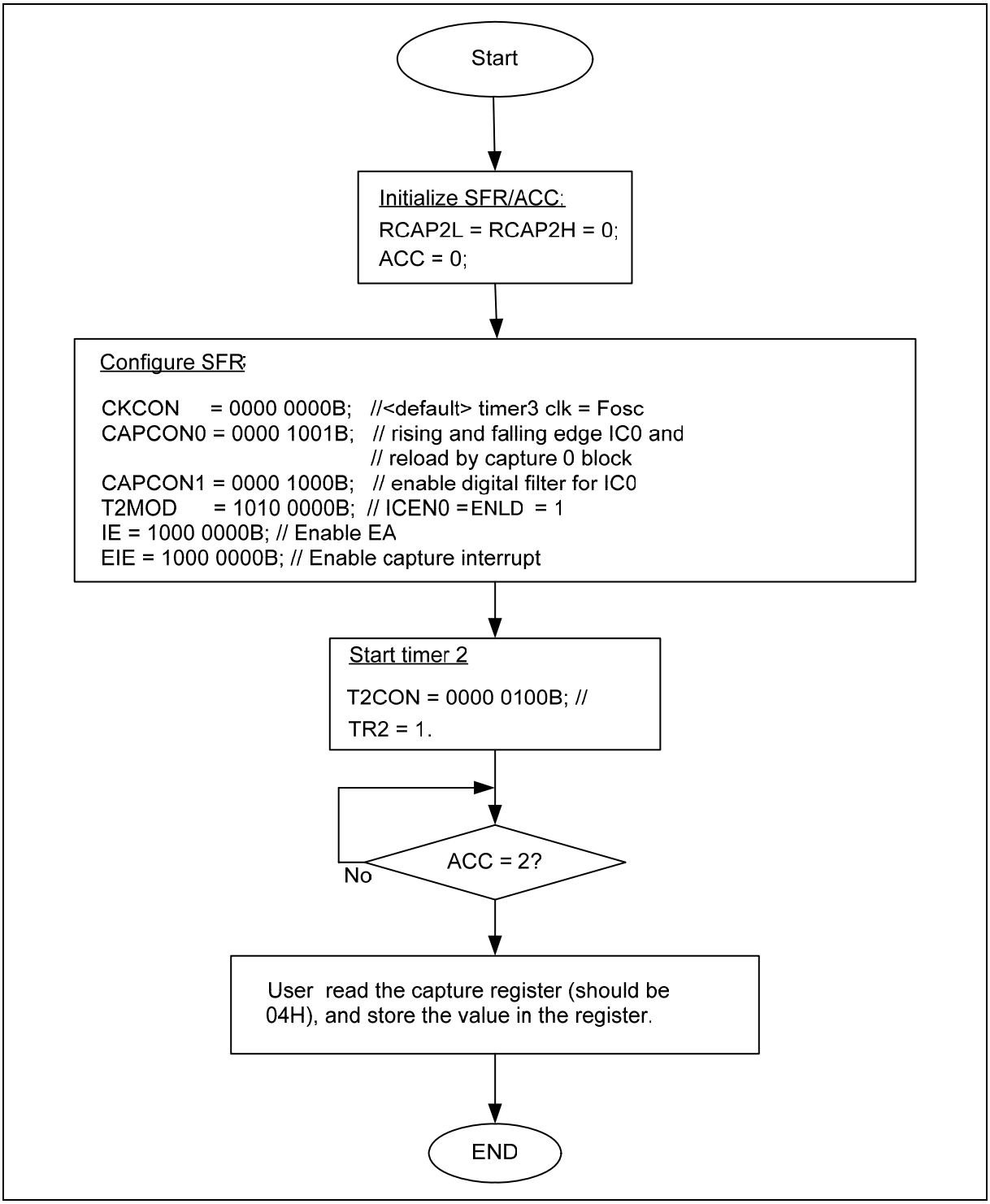


Figure 15- 6: Program flow for measurement with T0 pulse width with rising and falling edge detection (ACC is incremented in interrupt service routine).

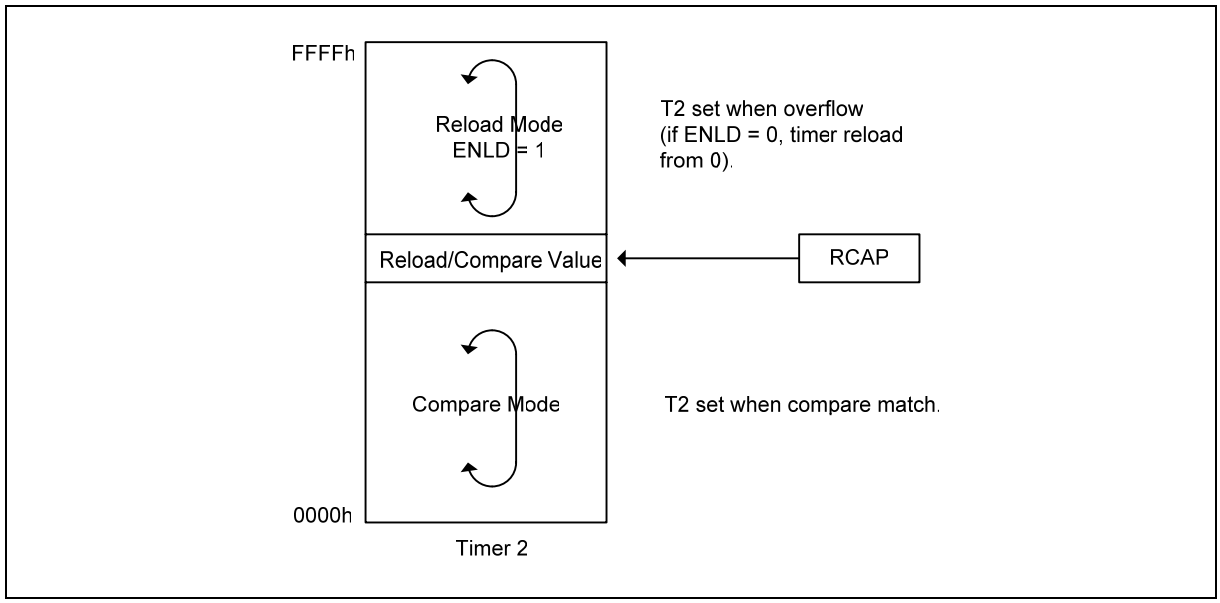


Figure 15- 7: Timer 2 - Compare/Reload Function

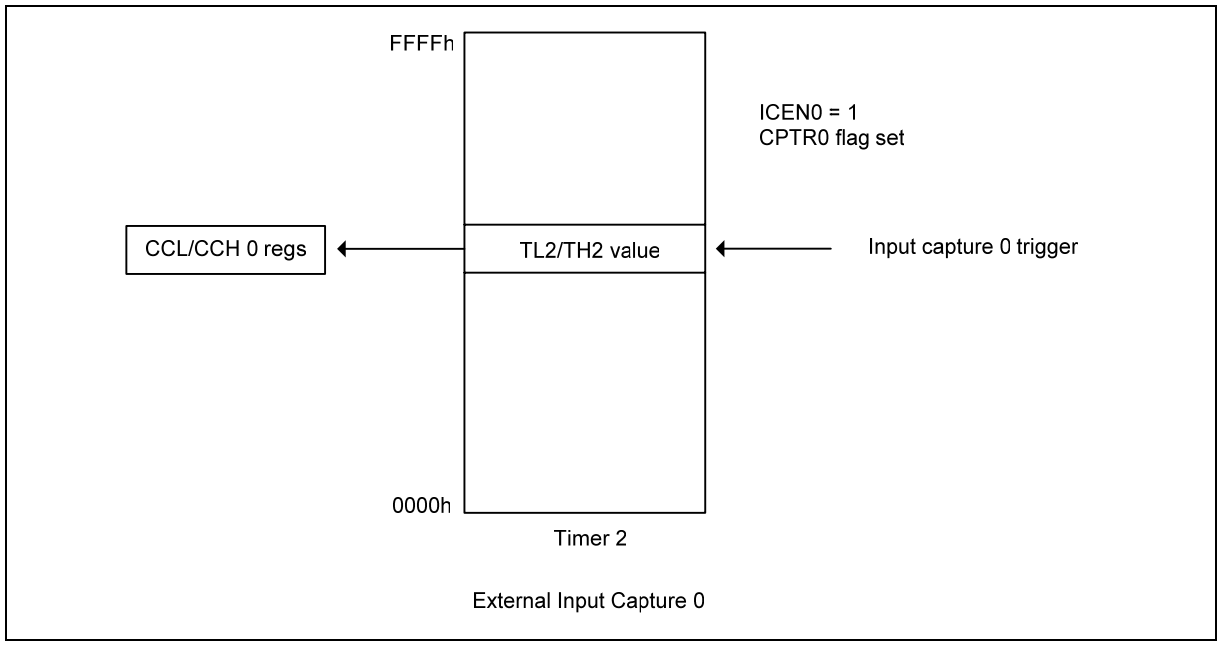


Figure 15- 8: Capture module - Input Capture 0 triggers

15.2 Compare Mode

Timer 2 can be configured for compare mode. The compare mode is enabled by setting the CMP/RL2 bit to 1 in the T2CON register. RCAP2 will serves as a compare register. As Timer 2 counting up, upon matching with RCAP2 value, TF2 will be set (which will generate an interrupt request if enable Timer 2 interrupt ET2 is enabled) and the timer reload from 0 and starts counting again.

15.3 Reload Mode

Timer 2 can be also be configured for reload mode. The reload mode is enabled by clearing the CMP/RL2 bit to 0 in the T2CON register. In this mode, RCAP serves as a reload register. When timer 2 overflows, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers, if ENLD is set. TF2 flag is set, and interrupt request is generated if enable Timer 2 interrupt ET2 is enabled. However, if ENLD = 0, timer 2 will be reload with 0, and count up again.

Alternatively, other reload source is also possible by the input capture pins by configuring the CCLD.1~0 bits. If the ICENx bit is set, then a trigger of external T0, T1 or T2 pin (respectively) will also cause a reload. This action also sets the CPTF0, CPTF1 or CPTF2 flag bit in SFR CAPCON1, respectively.

16. SERIAL PORT (UART)

Serial port in the W79E834 series is a full duplex port. It provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode, W79E834 series generate the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is Transmitted/Received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W79E834 series.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the device. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

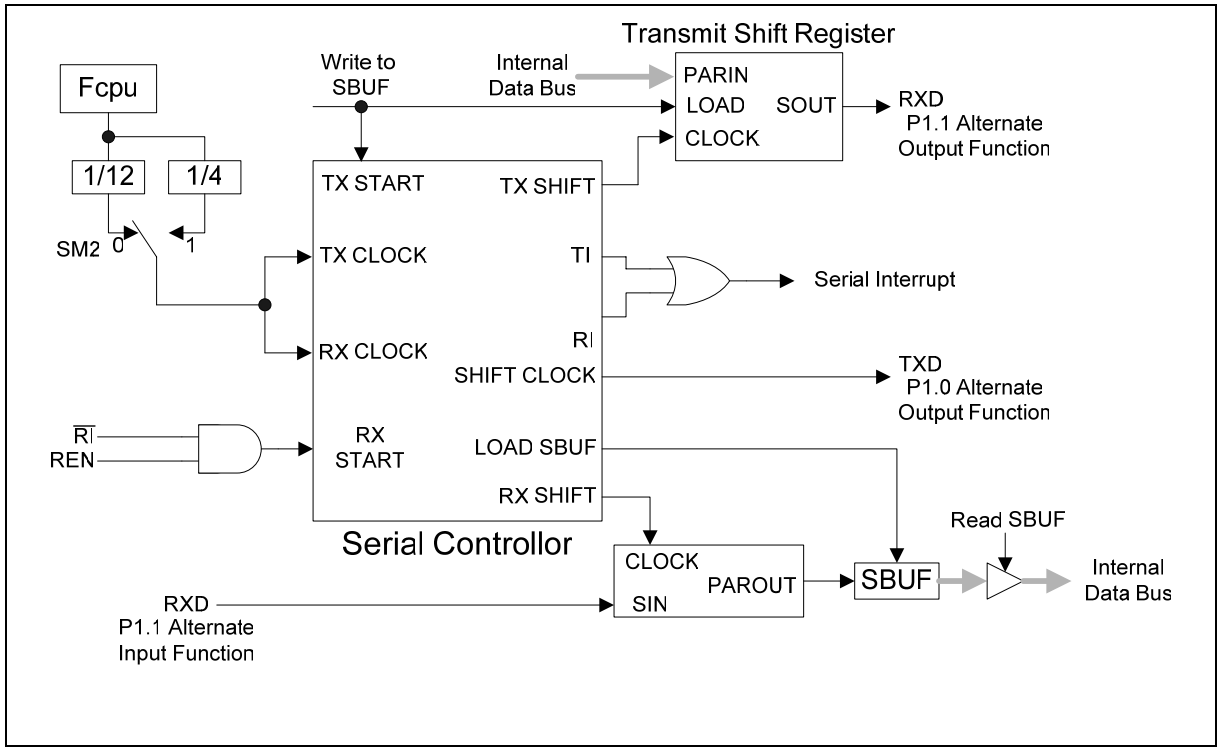


Figure 16- 1: Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On received, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counters after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD

line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

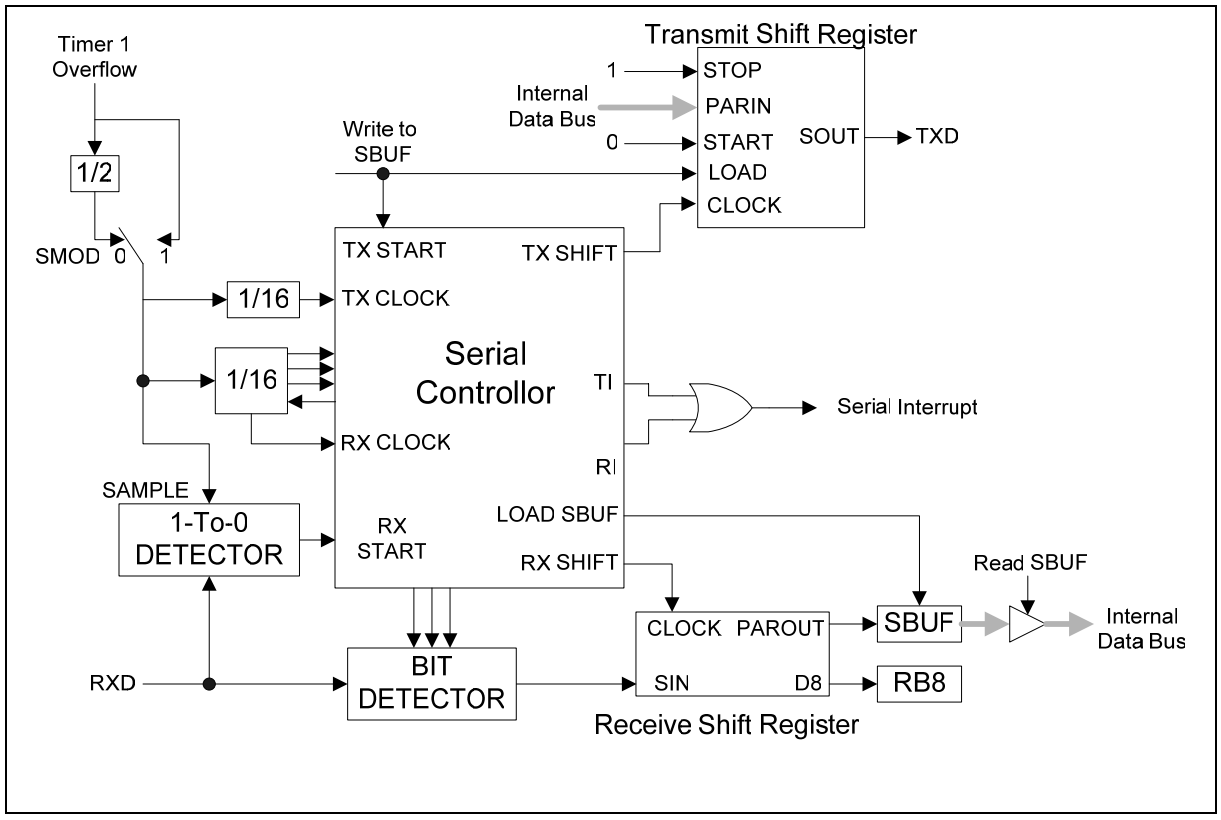


Figure 16- 2: Serial Port Mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counters after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

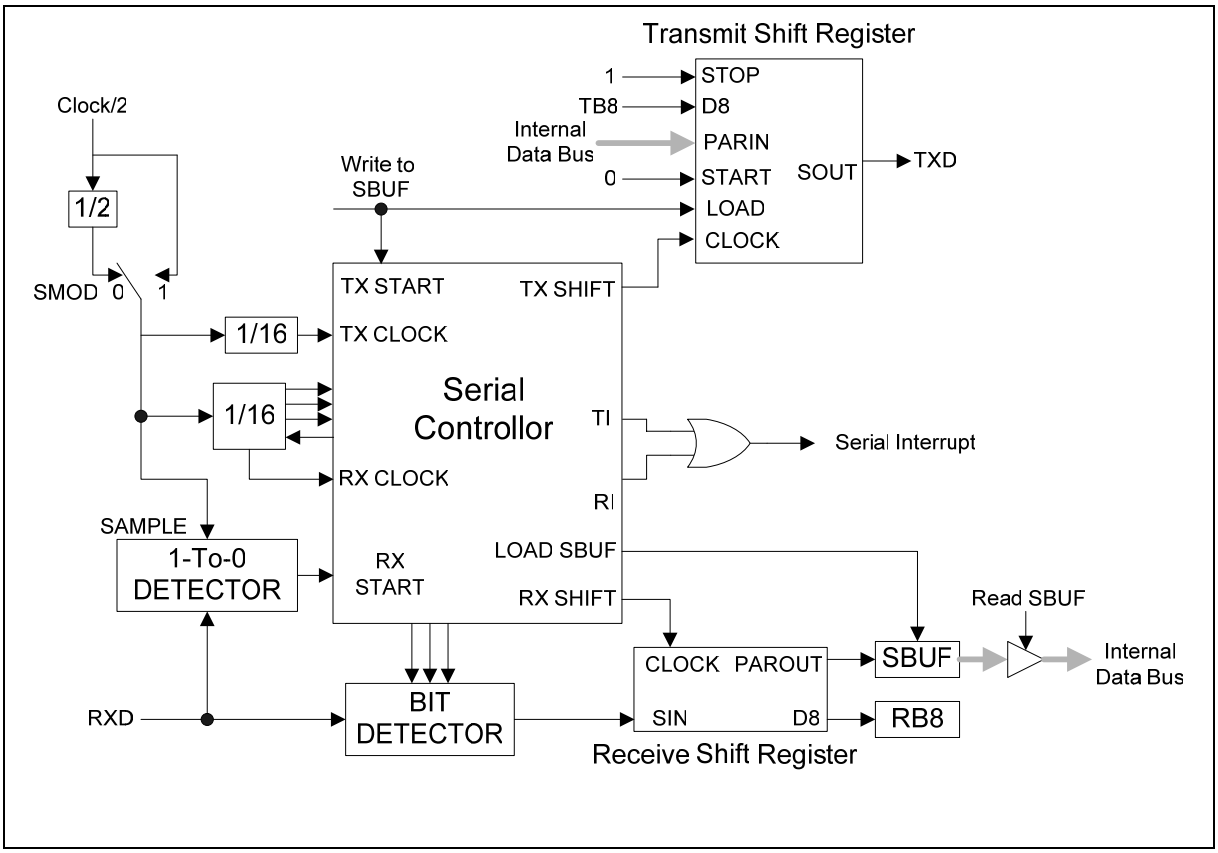


Figure 16- 3: Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

16.4 MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

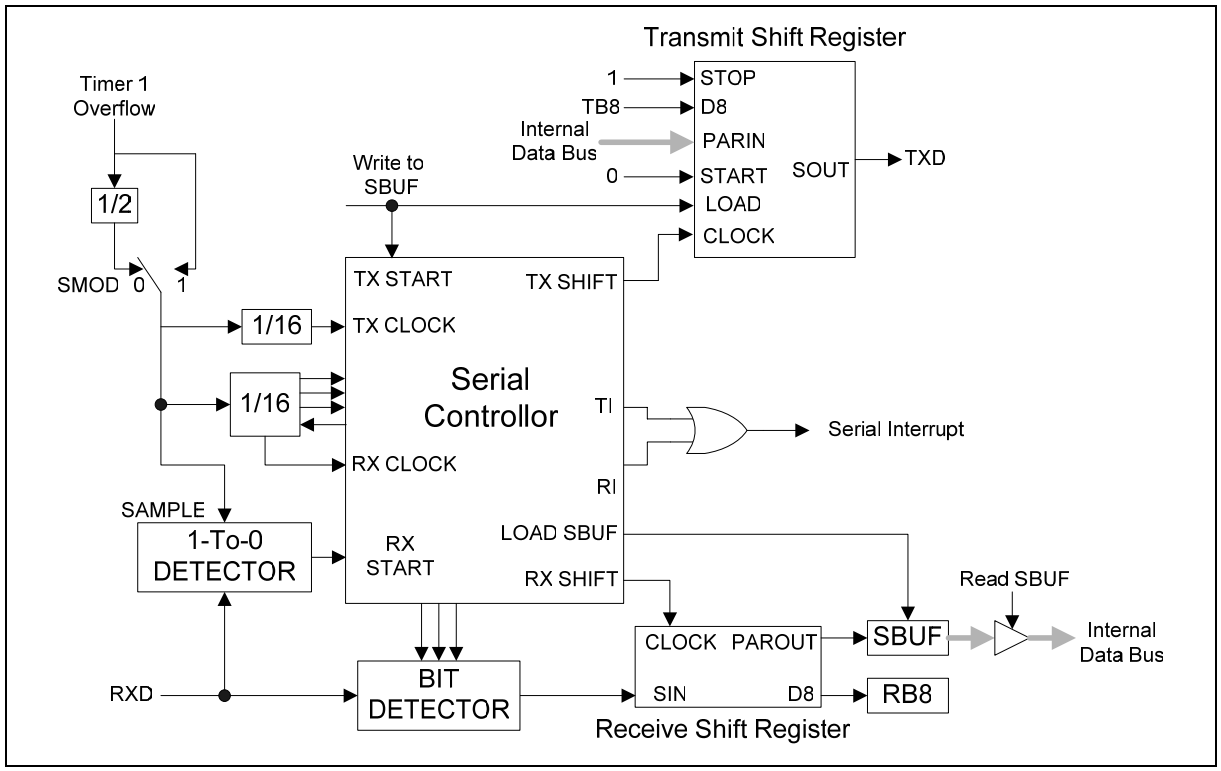


Figure 16- 4: Serial Port Mode 3

SM0	SM1	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1	11 bits	1	1	0, 1

Table 16- 1: Serial Ports Modes

16.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. W79E834 series have the capability to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

16.6 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. The RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR	1010 0100
SADEN	1111 1010
Given:	1010 0x0x

Slave 2:

SADDR	1010 0111
SADEN	1111 1001
Given:	1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares. In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXXb (i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

17. SERIAL PHERIPHERAL INTERFACE (SPI)

17.1 General descriptions

W79E834 series consist of SPI block to support high speed serial communication. It's capable of supporting data transfer rates of 1 Mbit/s, for 16MHz bus frequency. This device's SPI support the following features;

- Master and slave mode.
- Slave select output.
- Programmable serial clock's polarity and phase.
- Receive double buffered data register.
- LSB first enable.
- Write collision detection.
- Transfer complete interrupt.

17.2 Block descriptions

The following figure shows SPI block diagram. It provides an overview of SPI architecture in this device. The main blocks of SPI are SPI register blocks, control logics, baud rate control, and pin control logics;

a. Shift register and read data buffer. It is single buffered in the transmit direction and double buffered in the receive direction. Transmit data cannot be written to the shifter until the previous transfer is complete. When the SPIF set, user will not be able to write to the shift register. User has to clear the SPIF before writing to the shift register. Receive logics consist of parallel read data buffer so the shifter is free to accept a second data, as the first received data will be transferred to the read data buffer.

b. SPI Control block. This provide control functions to configure the device for SPI enable, master or slave, clock phase and polarity, MSB/LSB access first selection, and Slave Select output enable.

c. Baud rate control. This control logics divide CPU clock to 4 different selectable clocks (1/16, 1/64 and 1/128).

SPR1	SPR0	DIVIDER	BAUD RATE
0	0	Reserved	-
0	1	16	1MHz
1	0	64	250kHz
1	1	128	125kHz

Table 17- 1: SPI Baud Rate Selection (based on 16 MHz Bus Clock)

d. SPI registers. There are three SPI registers to support its operations, they are;
   - SPI control registers (SPCR)
   - SPI status registers (SPSR)
   - SPI data register (SPDR)

These registers provide control, status, data storage functions and baud rate selection control. Detail bit descriptions are found at SFR section.

e. Pin control logic. Controls behavior of SPI interface pins.

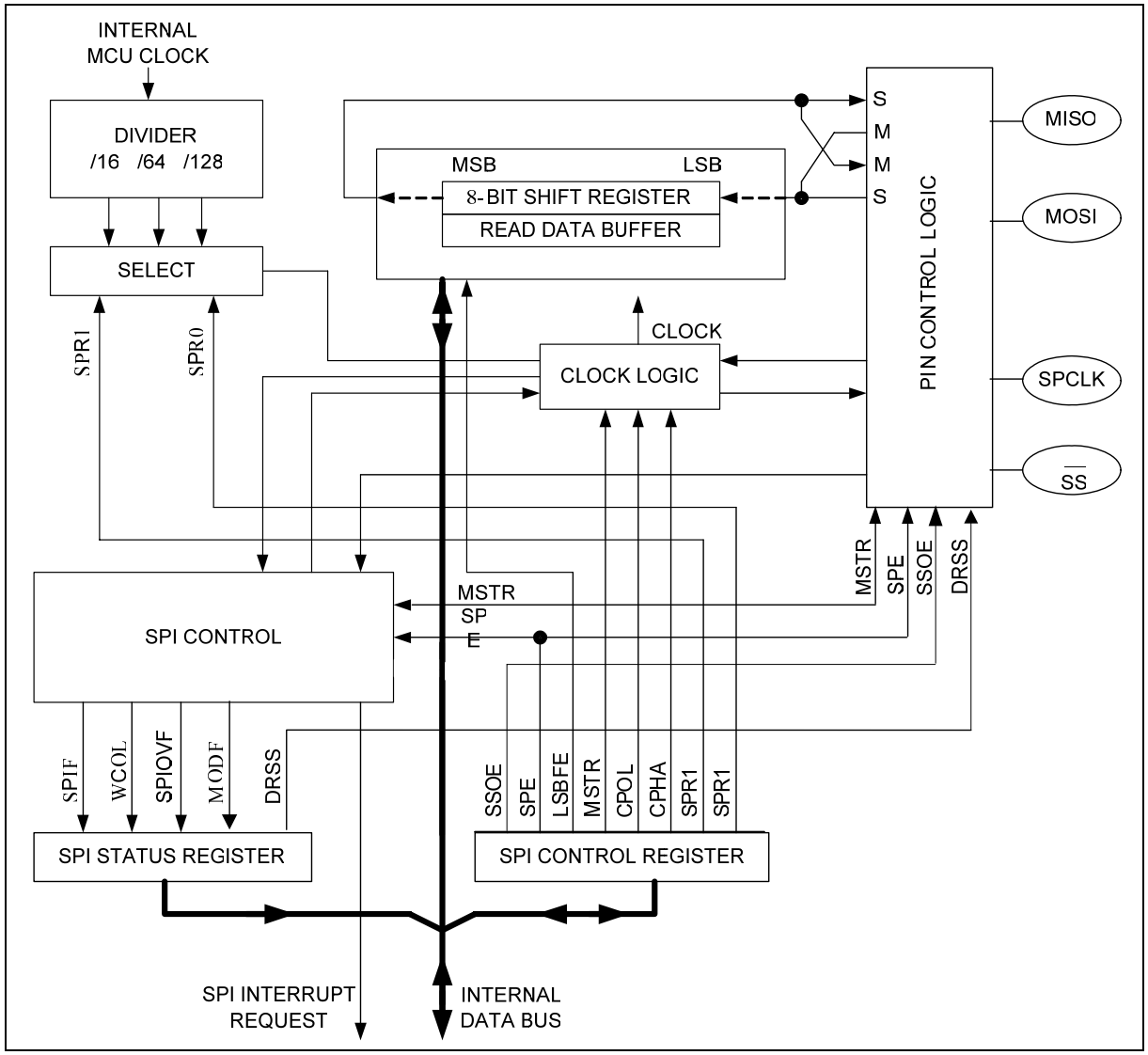


Figure 17- 1: SPI block diagram

17.3 Functional descriptions

17.3.1 Master mode

The device can configure the SPI to operate as a master or as a slave, through MSTR bit. When the MSTR bit is set, master mode is selected, when MSTR bit is cleared, slave mode is selected. During master mode, only master SPI device can initiate transmission. A transmission begins by writing to the master SPDR register. The bytes begin shifting out on MOSI pin under the control of SPCLK. The master places data on MOSI line a half-cycle before SPCLK edge that the slave device uses to latch the data bit. The /SS must stay low before data transactions and stay low for the duration of the transactions.

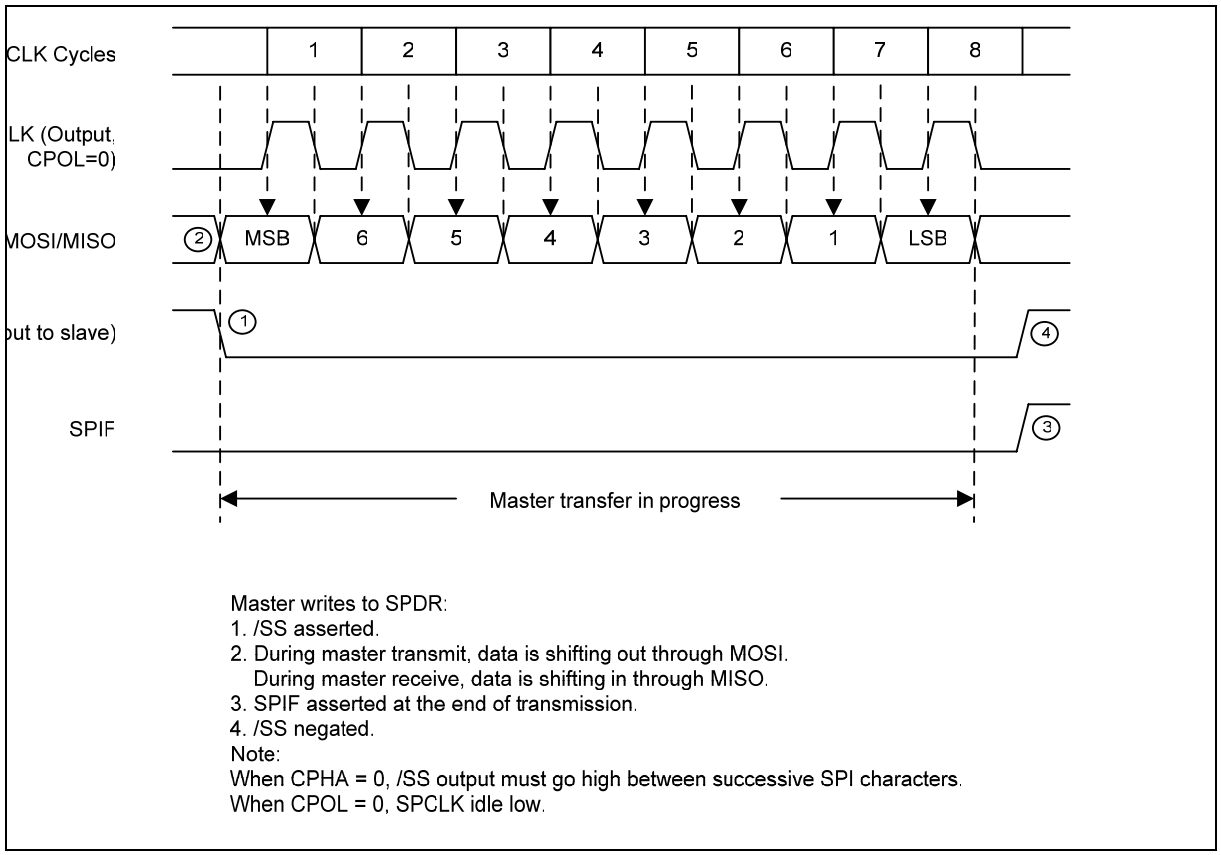


Figure 17- 2: Master Mode Transmission (CPOL = 0, CPHA = 0)

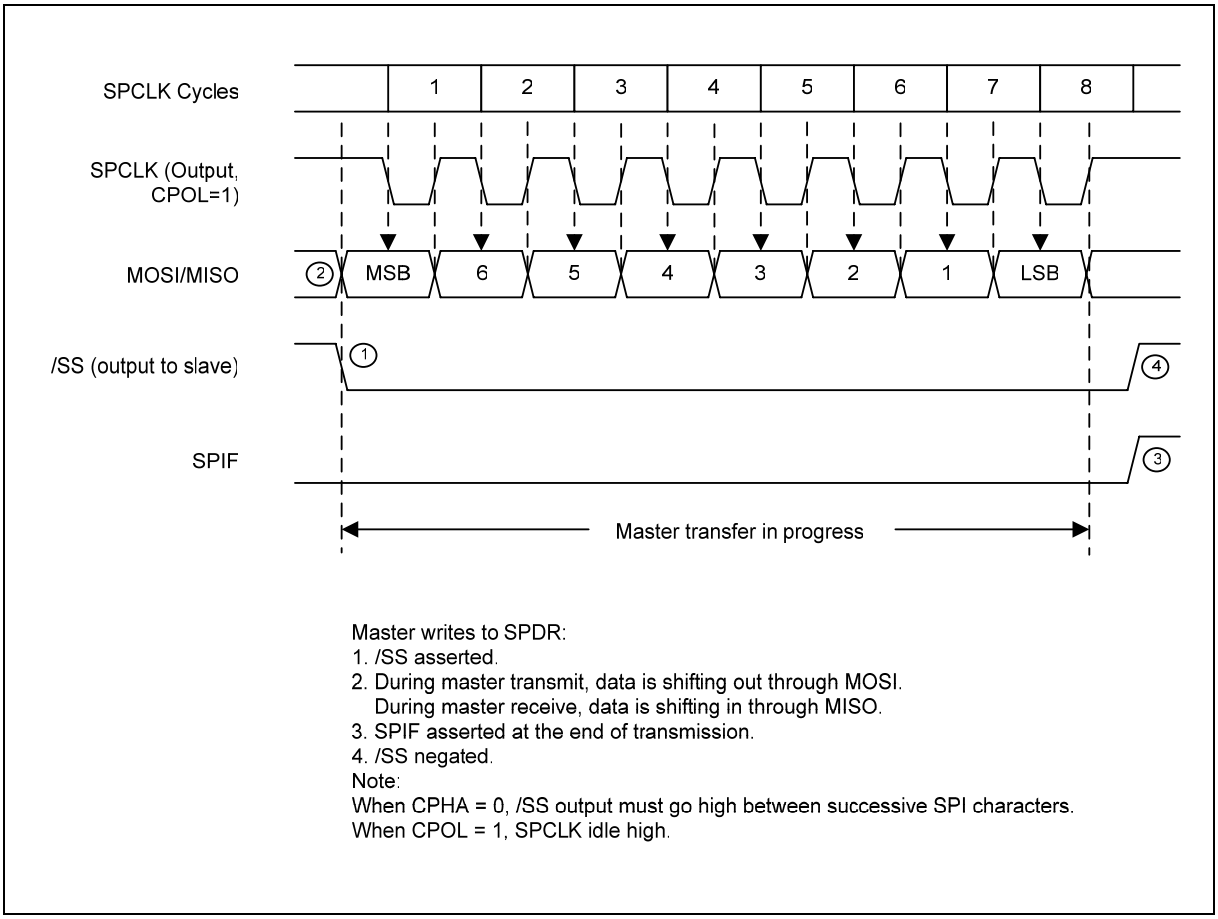
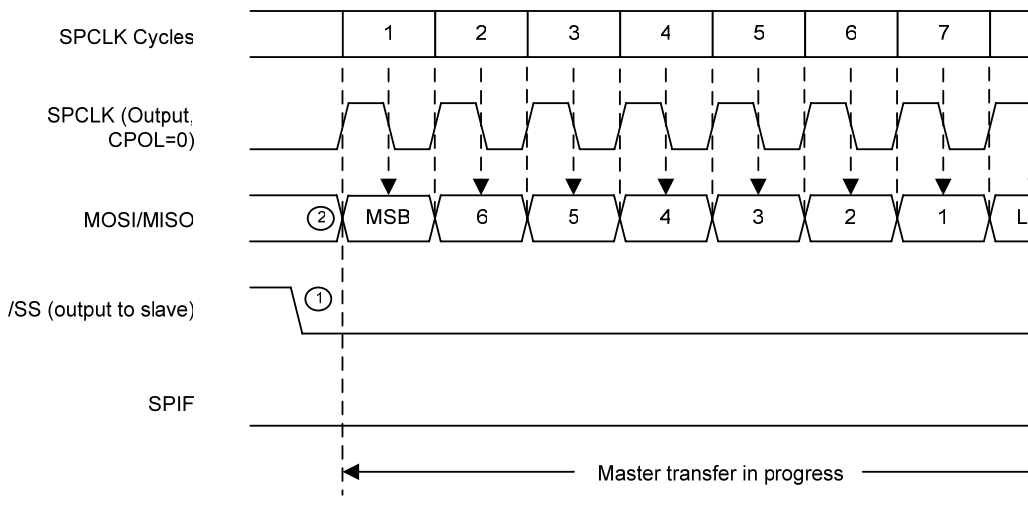


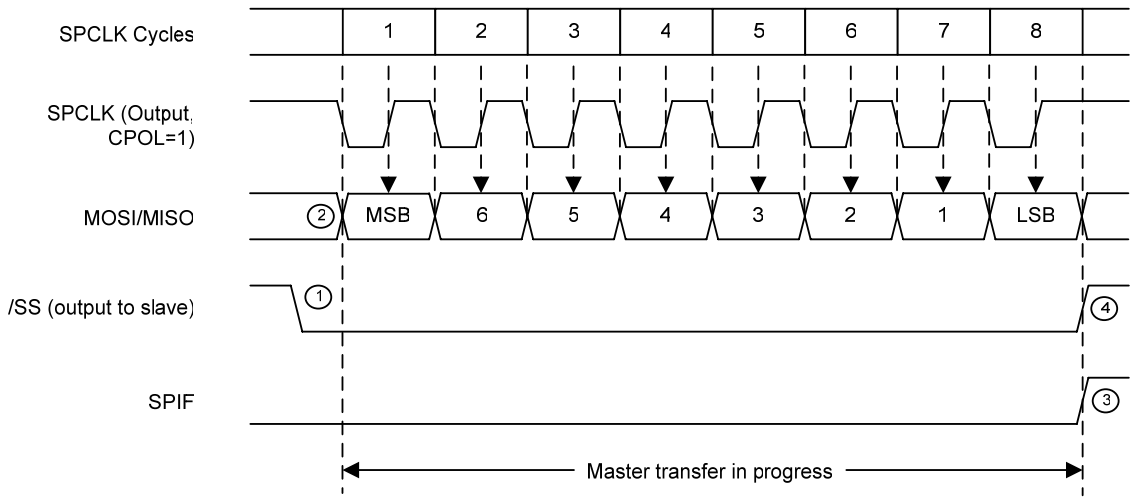
Figure 17- 3: Master Mode Transmission (CPOL = 1, CPHA = 0)



Master writes to SPDR:
1. /SS asserted.
2. During master transmit, data is shifting out through MOSI.
   During master receive, data is shifting in through MISO.
3. SPIF asserted at the end of transmission.
4. /SS negated.

Note:
When CPHA = 1, /SS output can stay low between successive SPI characters.
When CPOL = 0, SPCLK idle low.

Figure 17- 4: Master Mode Transmission (CPOL = 0, CPHA = 1)



Master writes to SPDR:
1. /SS asserted.
2. During master transmit, data is shifting out through MOSI.
   During master receive, data is shifting in through MISO.
3. SPIF asserted at the end of transmission.
4. /SS negated.

Note:
When CPHA = 1, /SS output can stay low between successive SPI characters.
When CPOL = 1, SPCLK idle high.

Figure 17- 5: Master Mode Transmission (CPOL = 1, CPHA = 1)

17.3.2 Slave Mode

When in slave mode, the SPCLK pin becomes input and it will be clock by another master SPI device. The /SS pin also becomes input. Similarly, before data transmissions occurs, and remain low until the transmission completed. If /SS goes high, the SPI is forced into idle state.

Data flows from master to slave on MOSI pin and flows from slave to master on MISO pin. The SPDR is used when transmitting or receiving data on the serial bus. Only a write to this register initiates transmission or reception of a byte, and this only occurs in the master device. At the completion of transferring a byte of data, the SPIF status bit is set in both the master and slave devices. A read of the SPDR is actually a read of a buffer. To prevent an overrun and the loss of the byte that caused the overrun, the first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated.

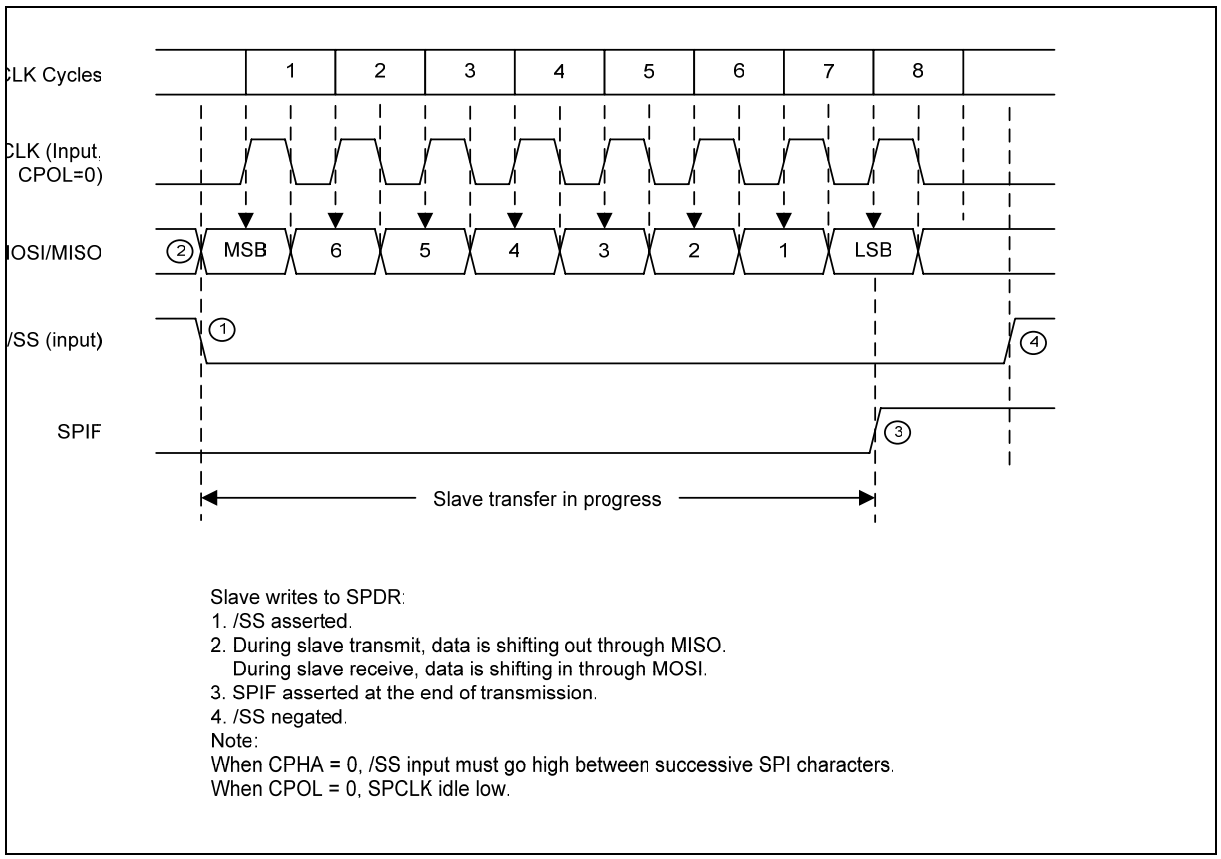
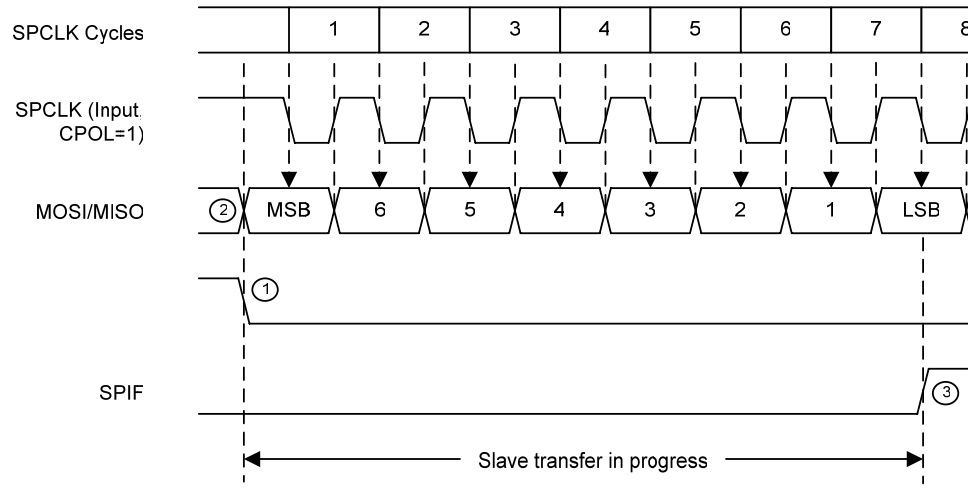


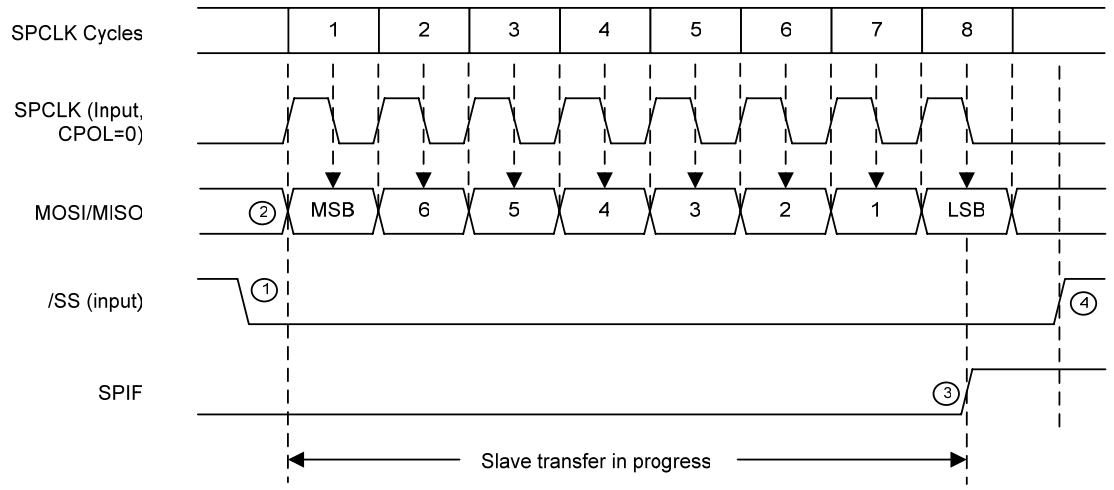
Figure 17- 6: Slave Mode Transmission (CPOL = 0, CPHA = 0)



Slave writes to SPDR:
1. /SS asserted.
2. During slave transmit, data is shifting out through MISO.
   During slave receive, data is shifting in through MOSI.
3. SPIF asserted at the end of transmission.
4. /SS negated.

Note:
When CPHA = 0, /SS input must go high between successive SPI characters.
When CPOL = 1, SPCLK idle high.

Figure 17- 7: Slave Mode Transmission (CPOL = 1, CPHA = 0)



Slave writes to SPDR:
1. /SS asserted.
2. During slave transmit, data is shifting out through MISO.
   During slave receive, data is shifting in through MOSI.
3. SPIF asserted at the end of transmission.
4. /SS negated.

Note:
When CPHA = 1, /SS input can stay low between successive SPI characters.
When CPOL = 0, SPCLK idle low.

Figure 17- 8: Slave Mode Transmission (CPOL = 0, CPHA = 1)

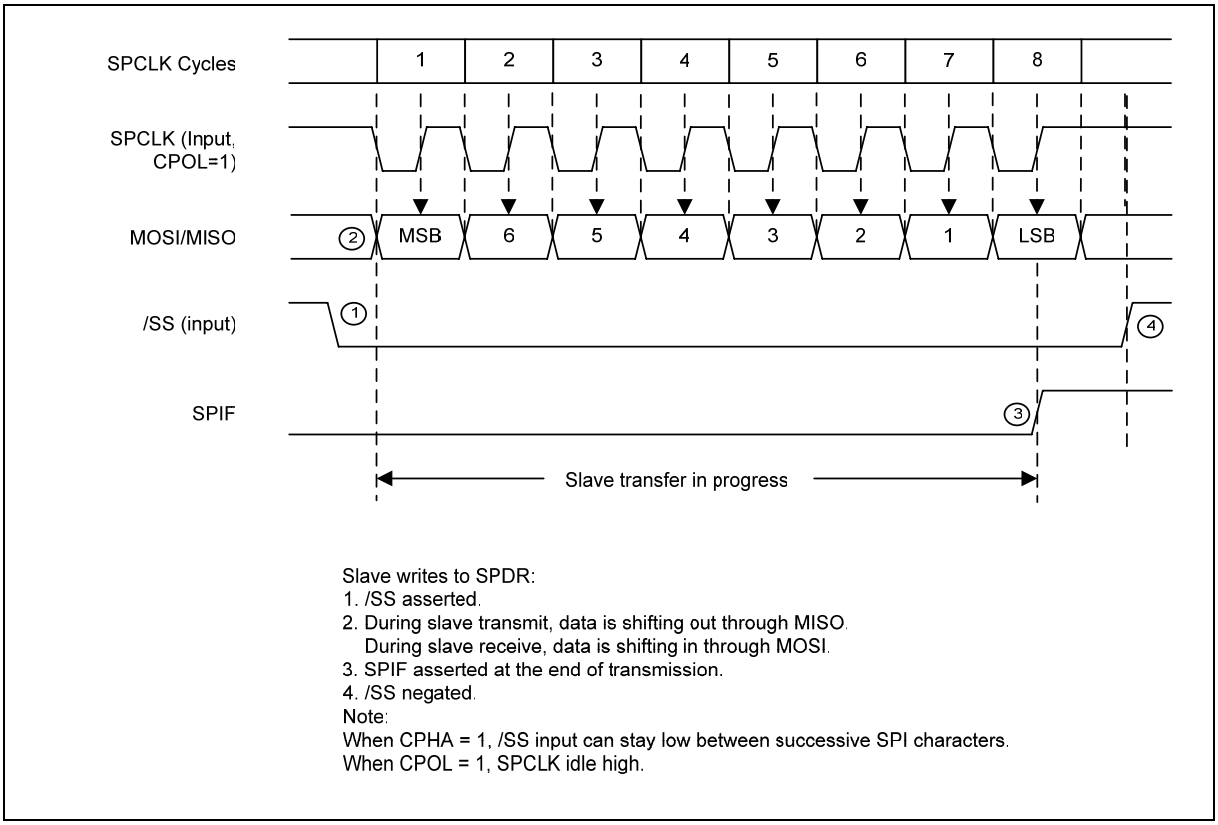


Figure 17- 9: Slave Mode Transmission (CPOL = 1, CPHA = 1)

17.3.3 Slave select

The slave select (/SS) input of a slave device must be externally asserted before a master device can exchange data with the slave device. /SS must be low before data transactions and must stay low for the duration of the transaction. The /SS line of the master must be held high.

The other three lines are dedicated to the SPI whenever the serial peripheral interface is on.

The state of the master and slave CPHA bits affects the operation of /SS. CPHA settings should be identical for master and slave. When CPHA = 0, the shift clock is the OR of /SS with SCK. In this clock phase mode, /SS must go high between successive characters in an SPI message. When CPHA = 1, /SS can be left low between successive SPI characters. In cases where there is only one SPI slave MCU, its /SS line can be tied to VSS as long as only CPHA = 1 clock mode is used.

17.3.4 Slave Select output enable

Available in master mode only, the /SS output is enabled with the SSOE bit in the SPCR register. The /SS output pin is connected to the /SS input pin of the slave device. The /SS output automatically goes low for each transmission when selecting external device and it goes high during each idling state to deselect external devices.

DRSS	SSOE	MASTER MODE	SLAVE MODE
0	0	/SS input (With Mode Fault). See section SPI I/O mode section for detail.	/SS Input (Not affected by SSOE)
0	1	Reserved	/SS Input (Not affected by SSOE)
1	0	/SS General purpose I/O (No Mode Fault)	/SS Input (Not affected by SSOE)
1	1	/SS output (No Mode Fault)	/SS Input (Not affected by SSOE)

Table 17- 2: /SS output

During master mode (with SSOE=DRSS= 0), mode fault will be set if /SS pin is detected low. When mode fault is detected hardware will clear MSTR bit and SPE bit in the meantime it will also generated interrupt request, if ESPI is enabled.

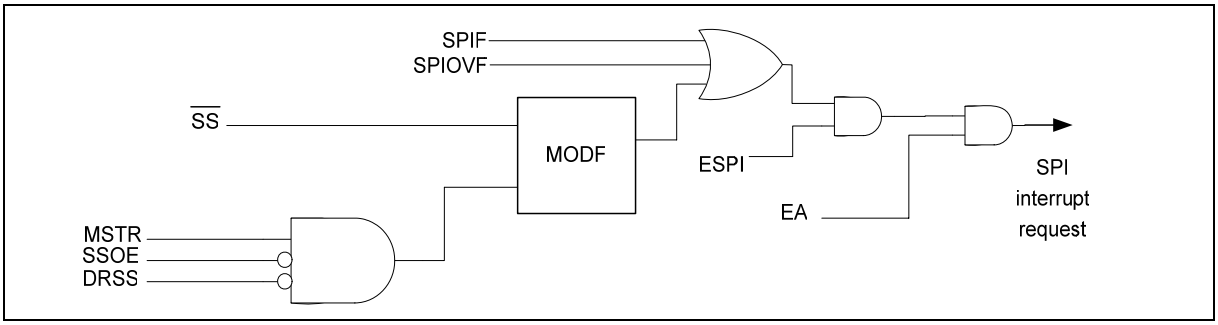


Figure 17- 10: SPI interrupt request

17.3.5 SPI I/O pins mode

When SPI is disabled (SPE = 0) the corresponding I/O is following the setting determined by port mode setting (SFR P2M1 & P2M2). When SPI is enabled (SPE = 1) the SPI pins I/O mode follow the below table. For /SS pin it is always at Quasi-bidirectional mode whether it is configured as master or slave.

	MISO	MOSI	CLK	/SS
Master	Input	Output	Output	**Output*:** DRSS=0,SSOE=0 Input: DRSS=1, SSOE=1
Slave	**Output**** during /SS = Low Else Input mode	Input	Input	Input

Table 17- 3: SPI I/O pins mode

Input = Quasi-bidirectional mode; Output = Push-pull mode

Output[1] = This output mode in /SS is Quasi-bidirectional output mode. Master needs to detect mode fault during master outputs /SS low.

Output[2] = In SLAVE mode, MISO is in output mode only during the time of /SS =Low. Otherwise it must keep in input mode (Quasi-bidirectional).

17.3.6 Programmable serial clock's phase and polarity

The clock polarity SPCR.CPOL control bit selects active high or active low SCK clock, and has no significant effect on the transfer format. The clock phase SPCR.CPHA control bit selects one of two different transfer protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges. Thus, both these bits enable selection of four possible clock formats to be used by SPI system.

The clock phase and polarity should be identical for the master SPI device and the communicating slave device.

When CPHA equals 0, the /SS line must be negated and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while /SS is low, a write collision error results. When CPHA equals 1, the /SS line can remain low between successive transfers.

When CPHA = 0, data is sample on the first edge of SPCLK and when CPHA = 1 data is sample on the second edge of the SPCLK. Prior to changing CPOL setting, SPE must be disabled first.

17.3.7 Receive double buffered data register

This device is single buffered in the transmit direction and double buffered in the receive direction. This means that new data for transmission cannot be written to the shifter until the previous transfer is complete; however, received data is transferred into a parallel read data buffer so the shifter is free to accept a second serial byte. As long as the first byte is read out of the read data buffer before the next byte is ready to be transferred, no overrun condition occurs.

If overrun occur, SPIOVF is set. Second byte serial data cannot be transferred successfully into the data register during overrun condition and the data register will remains the value of the previous byte. The figure below shows the receive data timing waveform when overrun occur.

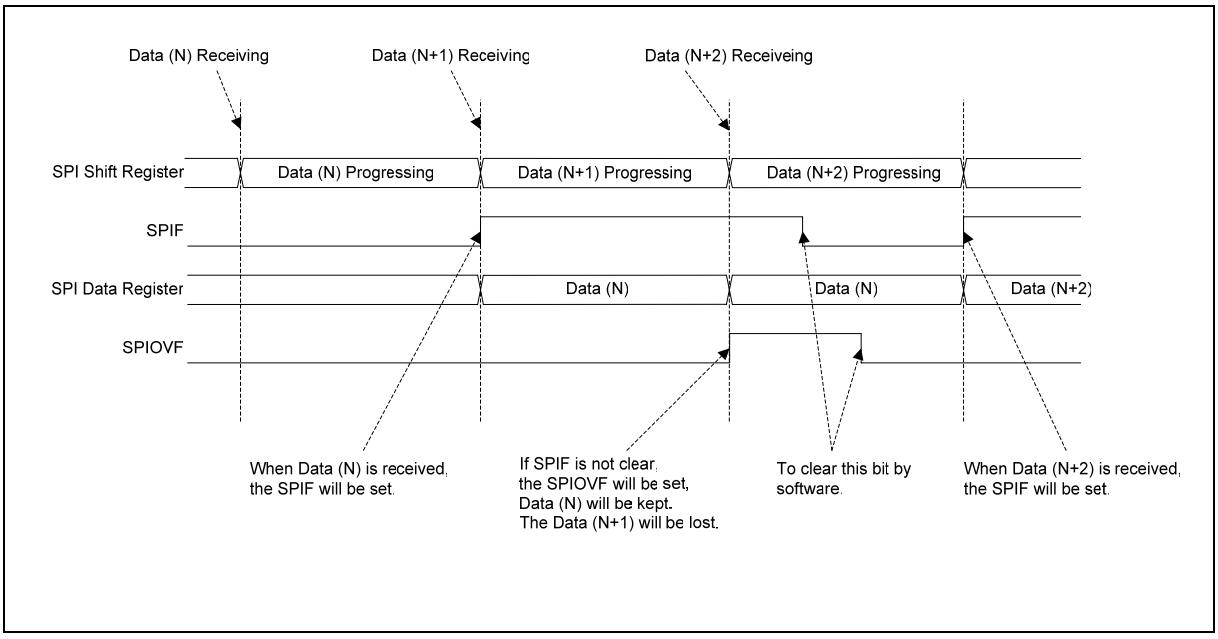


Figure 17- 11: SPI receive data timing waveform

17.3.8 LSB first enable

By default, this device transfer the SPI data most significant bit first. This device provides a control bit SPCR.LSBFE to allow support of transfer of SPI data in least significant bit first.

17.3.9 Write Collision detection

Write collision indicates that an attempt was made to write data to the SPDR while a transfer was in progress. SPDR is not double buffered in the transmit direction, any writes to SPDR cause data to be written directly into the SPI shift register. This write corrupts any transfer in progress, a write collision error is generated (WCOL will be set). The transfer continues undisturbed, and the write data that caused the error is not written to the shifter. A write collision is normally a slave error because a slave has no control over when a master initiates a transfer. A master knows when a transfer is in progress, so there is no reason for a master to generate a write-collision error, although the SPI logic can detect write collisions in both master and slave devices.

WCOL flag is clear by software.

17.3.10 Transfer complete interrupt

This device consists of an interrupt flag at SPSR.SPIF. This flag will be set upon completion of data transfer with external device, or when a new data have been received and copied to SPDR. If interrupt is enable (through ESPI located at EIE.3), the SPI interrupt request will be generated, if global enable is also enabled. SPIF is a software clear interrupt.

17.3.11 Mode Fault

Error arises in a multiple-master system when more than one SPI device simultaneously tries to be a master. This error is called a mode fault.

When the SPI system is configured as a master and the /SS input line goes to active low, a mode fault error has occurred — usually because two devices have attempted to act as master at the same time. In cases where more than one device is concurrently configured as a master, there is a chance of contention between two pin drivers. For push-pull CMOS drivers, this contention can cause permanent damage. The mode fault mechanism attempts to protect the device by disabling the drivers. The MSTR & SPE control bits in the SPCR associated with the SPI are cleared and an interrupt is generated subject to masking by the ESPI control bit.

Other precautions may need to be taken to prevent driver damage. If two devices are made masters at the same time, mode fault does not help protect either one unless one of them selects the other as slave. The amount of damage possible depends on the length of time both devices attempt to act as master.

MODF bit is set automatically by SPI hardware, if the MSTR control bit is set and the slave select input pin becomes 0. This condition is not permitted in normal operation. In the case where /SS is set, it is an output pin rather than being dedicated as the /SS input for the SPI system. In this special case, the mode fault function is inhibited and MODF remains cleared. This flag is cleared by software.

The following figures show the sample hardware connection for multi-master/slave environment, and flow diagram which shows how s/w handles mode fault.

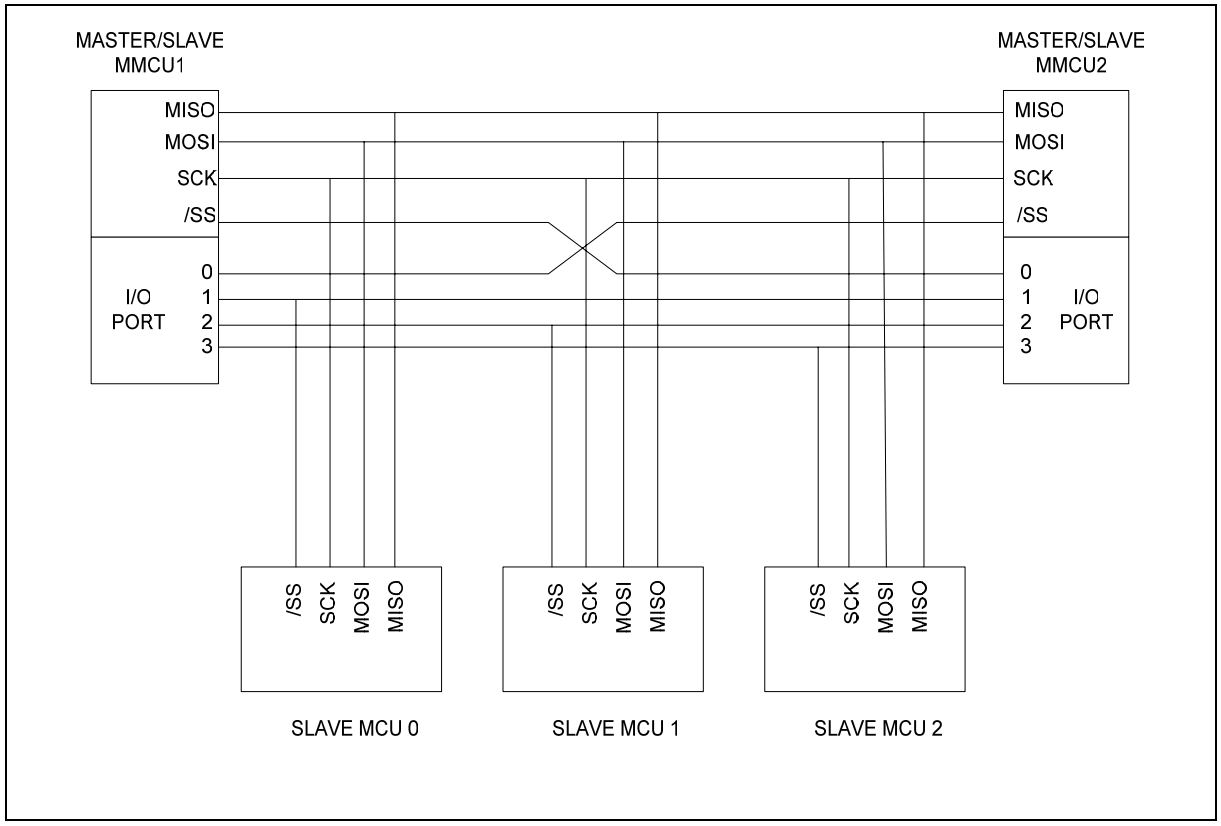


Figure 17- 12: SPI multi-master slave environment

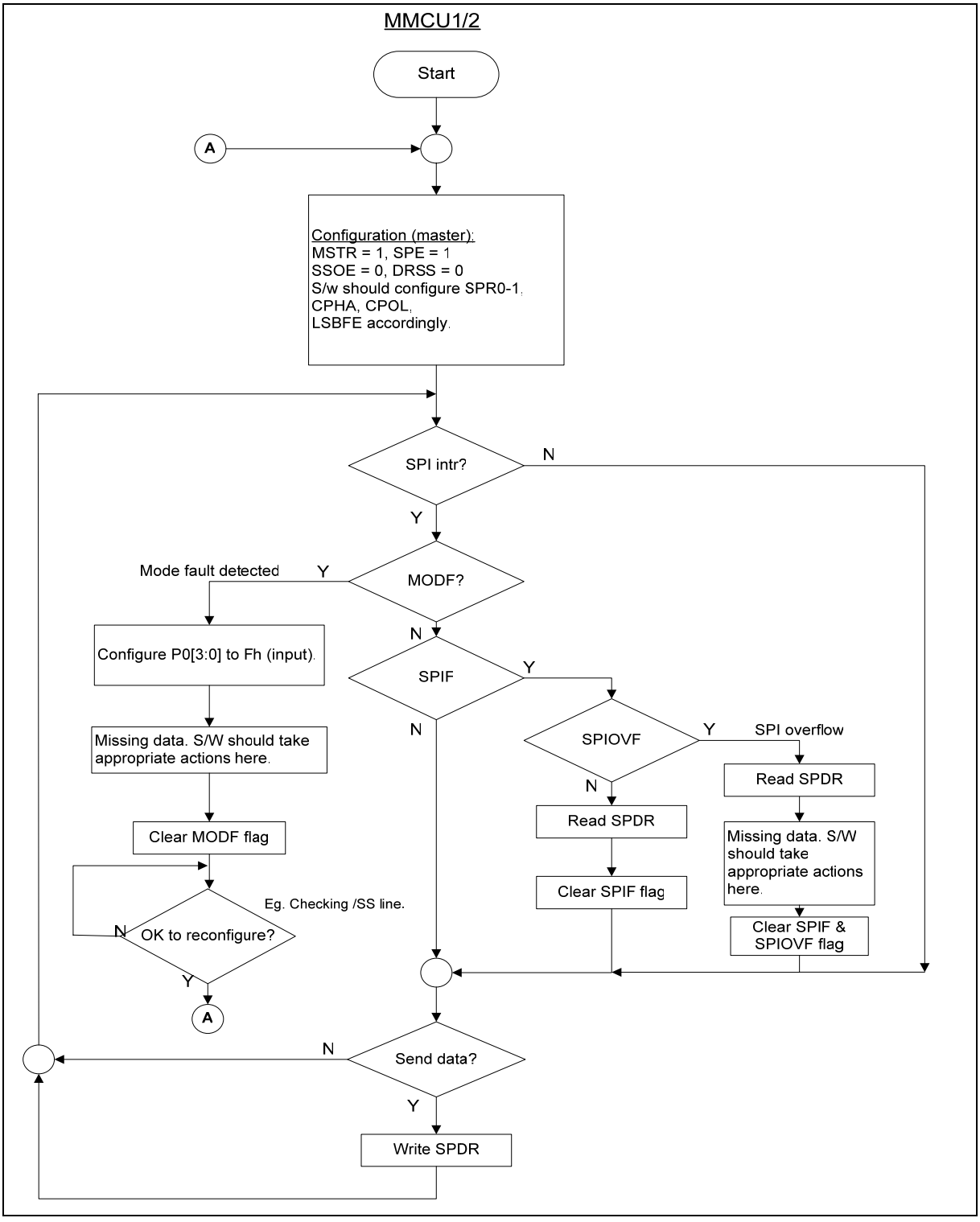


Figure 17- 13: SPI multi-master slave s/w flow diagram

18. TIMED ACCESS PROTECTION

W79E834 series have a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, it has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG     0C7h        ; Define new register TA, located at 0C7h
        MOV     TA, #0AAh
        MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
MOV     TA, #0AAh       ; 3 M/C     Note: M/C = Machine Cycles
MOV     TA, #055h       ; 3 M/C
MOV     WDCON, #00h     ; 3 M/C
```

Example 2: Valid access

```
MOV     TA, #0AAh       ; 3 M/C
MOV     TA, #055h       ; 3 M/C
NOP                     ; 1 M/C
SETB    EWRST           ; 2 M/C
```

Example 3: Valid access

```
MOV     TA, #0Aah               ; 3 M/C
MOV     TA, #055h               ; 3 M/C
ORL     WDCON, #00000010B  ; 3M/C
```

Example 4: Invalid access

```
MOV     TA, #0AAh       ; 3 M/C
MOV     TA, #055h       ; 3 M/C
NOP                     ; 1 M/C
NOP                     ; 1 M/C
CLR     EWT             ; 2 M/C
```

Example 5: Invalid Access

```
MOV     TA, #0AAh       ; 3 M/C
NOP                     ; 1 M/C
MOV     TA, #055h       ; 3 M/C
SETB    EWT             ; 2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles' window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

19. KEYBOARD INTERRUPT (KBI)

W79E834 series are provided with 8 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the device, as shown at figure below. This interrupt may be used to wake up the CPU from Idle or Power Down modes, after chip is in Power Down or Idle Mode.

To support keyboard function is by Port 0. It can allow any or all pins of Port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits of KBI0 ~ KBI7 in the KBI register. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active, and the low pulse must more than 1 machine cycle, an interrupt will be generated if it has been enabled. The KBF bit set by hardware and must be cleared by software. In order to determine which key was pressed, the KBI will allow the interrupt service routine to poll port 0.

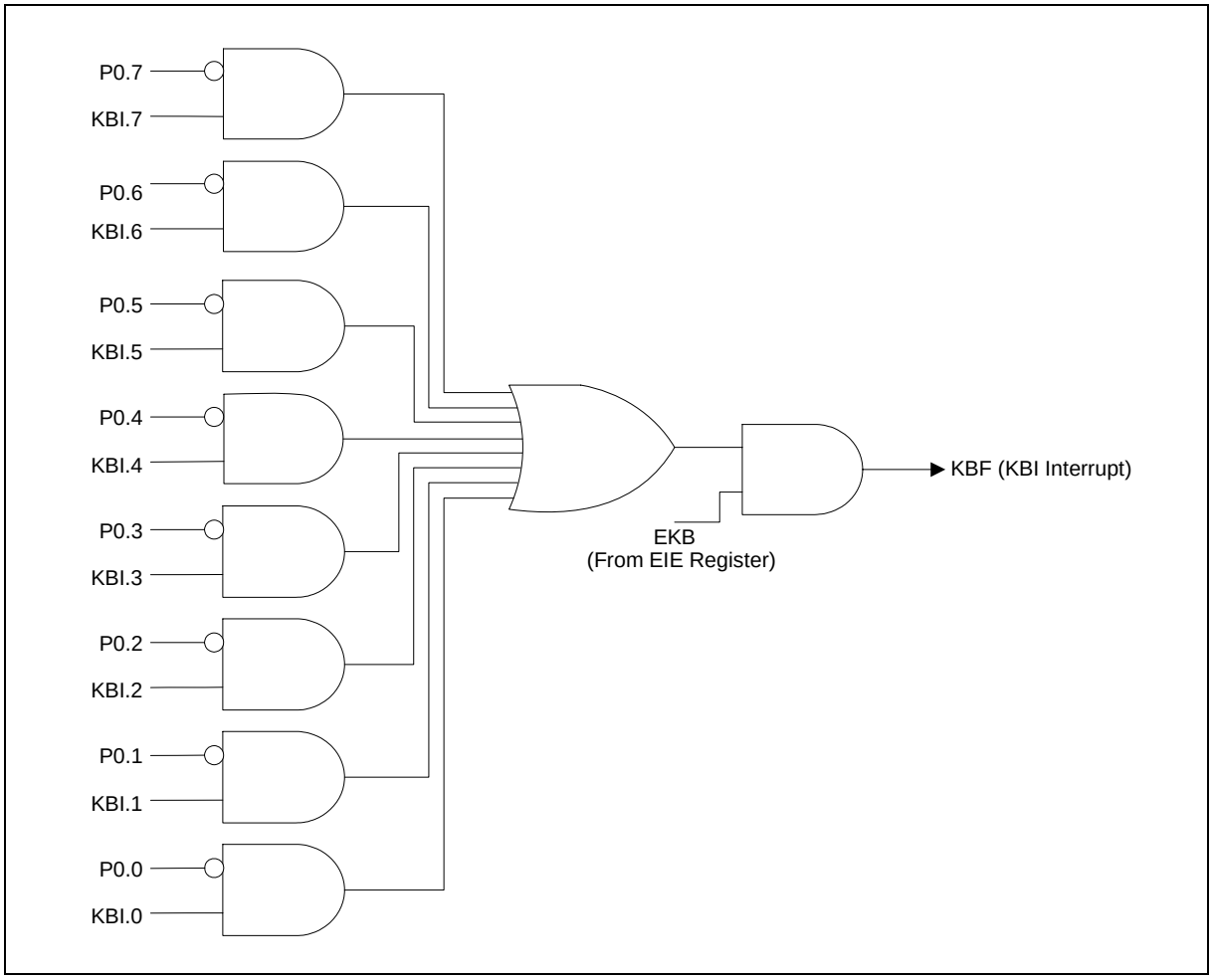


Figure 19- 1: KBI Interrupt

20. I/O PORT CONFIGURATION

W79E834 series have three I/O ports, port 0, port 1, port 2, P3.0 and P3.1. All pins of I/O ports can be configured to one of four types by software except P1.5 is only input pin or set to reset pin. When P1.5 is configured reset pin by RPD=0 in the CONFIG 1 register, the device can support 23 i/o pins by use Crystal. If used on-chip RC oscillator the P1.5 is configured input pin, the device can be supported up to 24 i/o pins. The I/O ports configuration setting as below table.

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance)
1	1	Open Drain

Table 20- 1: I/O port configuration table

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG1 register. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.5 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by T0OE and T1OE on P3M1 register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

Each I/O port of W79E834 series may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P3M1 register; where n is 0, 1 or 2. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The P3.0 (XTAL2) can be configured clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

The default port output configuration for standard W79E834 series I/O ports is the quasi-bidirectional output that is common on the 80C51 and most of its derivatives. This output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes. One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port latch for the pin contains a logic 1. The very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If a pin that has a logic 1 on it is pulled low by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to overpower the weak pull-up and take the voltage on the port pin below its input threshold.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for a brief time, two CPU clocks, in order to pull the port pin high quickly. Then it turns off again. The quasi-bidirectional port configuration is shown as below.

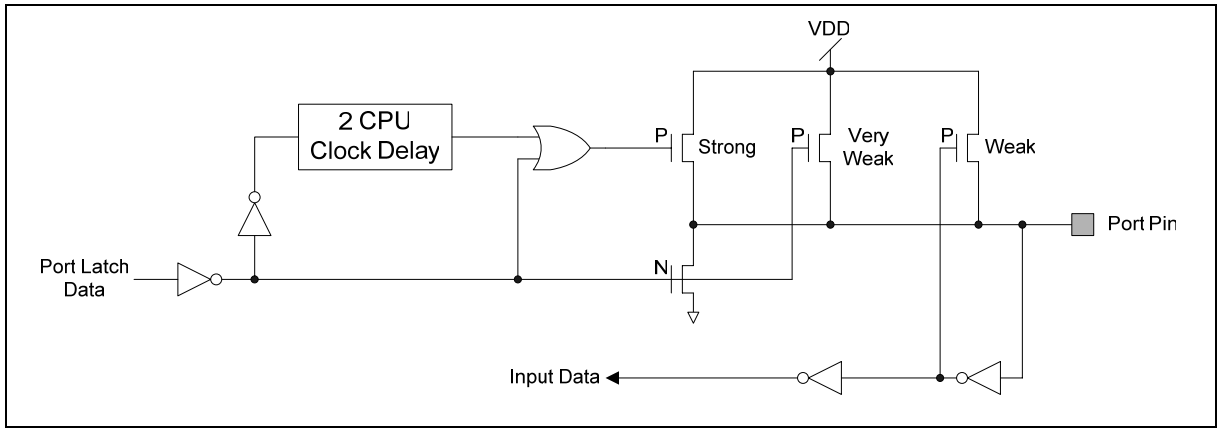


Figure 20- 1: Quasi-Bidirectional Output

20.2 Open Drain Output Configuration

The open drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to VDD. The pull-down for this mode is the same as for the quasi-bidirectional mode. The open drain port configuration is shown as below.

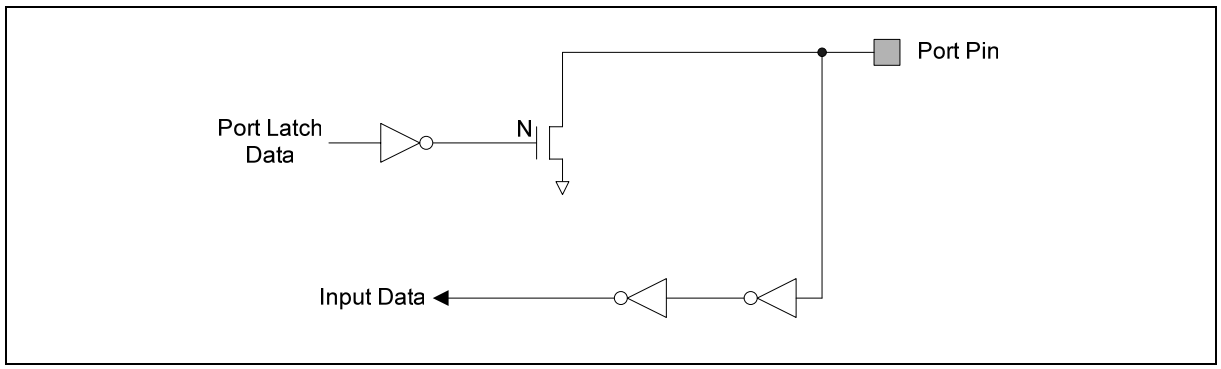


Figure 20- 2: Open Drain Output

20.3 Push-Pull Output Configuration

The push-pull output configuration has the same pull-down structure as both the open drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. The push-pull port configuration is shown below. One port pin that cannot be configured is P1.5. P1.5 may be used as a Schmitt trigger input if the device has been configured for an internal reset and is not using the external reset input function /RST.

The value of port pins at reset is determined by the PRHI bit in the CONFIG1 register. Ports may be configured to reset high or low as needed for the application. When port pins are driven high at reset, they are in quasi-bidirectional mode and therefore do not source large amounts of current. Every output on the device may potentially be used as a 20mA sink LED drive output. However, there is a maximum total output current for all ports which must not be exceeded.

All ports pins of the device have slew rate controlled outputs. This is to limit noise generated by quickly switching output signals. The slew rate is factory set to approximately 10 ns rise and fall times. The unused bits in the P3M1 are used for other purposes. These bits can enable Schmitt trigger inputs on each I/O port, enable toggle outputs from Timer 0 and Timer 1, and enable a clock output if either the internal RC oscillator or external clock input is being used. The last two functions are described in the Timer/Counters and Oscillator sections respectively. Each I/O port of this device may be selected to use TTL level inputs or Schmitt inputs with hysteresis. A single configuration bit determines this selection for the entire port. Port pin P1.5 always has a Schmitt trigger input.

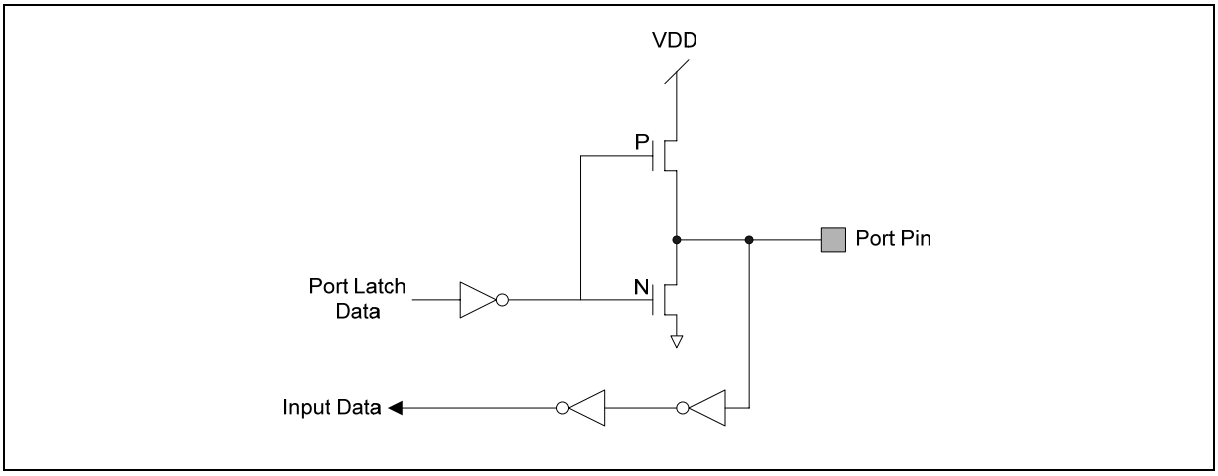


Figure 20- 3: Push-Pull Output

21. OSCILLATOR

W79E834 series provide three oscillator input option. These are configured at CONFIG register (CONFIG1) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 20MHz, and without capacitor or resister.

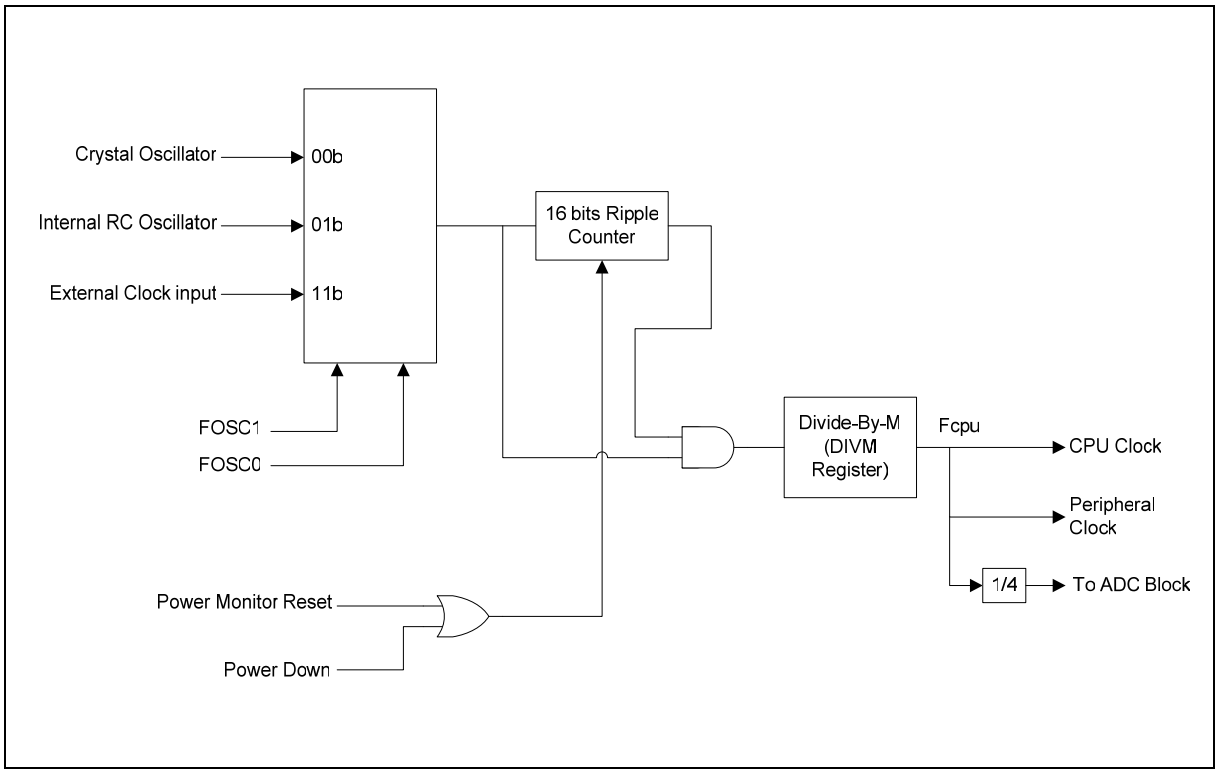


Figure 21- 1: Oscillator

21.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is fixed at 6MHz +/- 25% frequency to support clock source. When FOSC1, FOSC0 = 01b, the On-Chip RC Oscillator is enabled. A clock output on P3.0 (XTAL2) may be enabled when On-Chip RC oscillator is used.

21.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is form 0Hz up to 20MHz. A clock output on P3.0 (XTAL2) may be enabled when External Clock Input is used.

W79E834 series support a clock output function when either the on-chip RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the device. When enabled, via the ENCLK bit in the P3M2 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode, saving additional power. The clock output may also be enabled when the external clock input option is selected.

21.3 CPU Clock Rate select

The CPU clock of W79E834 series may be selected by the DIVM register. If DIVM = 00H, the CPU clock is running at 4 CPU clock per machine cycle, and without any division from source clock (Fosc). When the DIVM register is set to N value, the CPU clock is divided by 2(DVIM+1), so CPU clock frequency division is from 4 to 512. The user may use this feature to set CPU at a lower speed rate for reducing power consumption. This is very similar to the situation when CPU has entered Idle mode. In addition this frequency division function affect all peripheral timings as they are all sourcing from the CPU clock(Fcpu).

22. POWER MONITORING FUNCTION

Power-On Detect and Brownout are two additional power monitoring functions implemented in W79E834 series to prevent incorrect operation during power up and power drop or loss.

22.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

22.2 Brownout Detect

The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. W79E834 series have two brownout voltage levels to select by BOV (CONFIG1.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.

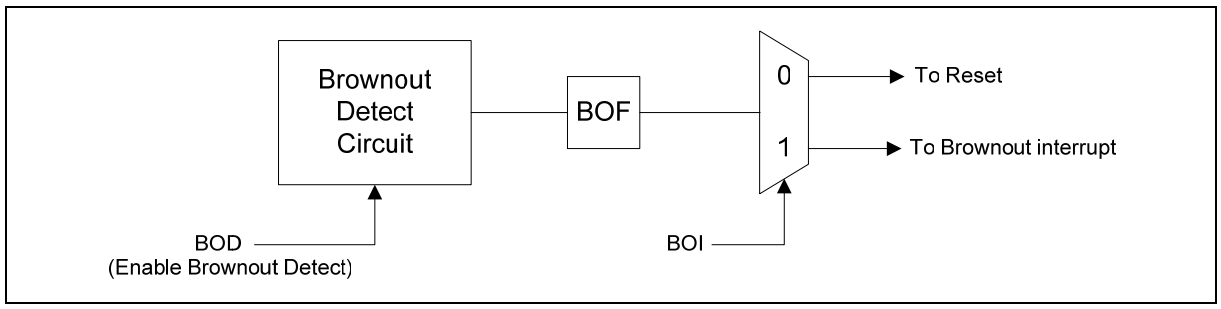


Figure 22- 1: Brownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set that it causes brownout reset or interrupt, and BOF will be cleared by software. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set.

In order to guarantee a correct detection of Brownout, The VDD fall time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.

23. PULSE WIDTH MODULATED OUTPUTS (PWM)

The W79E834 series have four Pulse Width Modulated (PWM) channels, and the PWM outputs are PWM0 (P1.6), PWM1 (P1.7), PWM2 (P0.0) and PWM3 (P2.1). The initial PWM outputs level depend on the CONFIG1.PRHI level set prior to the chip reset. When PRHI is set to high, PWM output will initialize to high after chip reset; if PRHI set to low, PWM output will be initialize to low after chip reset.

The W79E835 series support 10-bits down-counter. The PWM counter operating on clock source F_{CPWM} = F_{OSC}/Pre-scalar. The pre-scalar is controllable through PWMCON3.FP[1:0] bits. When the counter reaches underflow, it will be automatically reloaded from Counter Register (see PWM Block diagram below). The PWM frequency is given by: f_{PWM} = F_{CPWM} / (PWMP+1), where PWMP is 10-bits register of PWMPH.1, PWMPH.0 and PWMPL.7~PWMPL.0.

The Counter Register will be loaded with the PWMP register value when PWMRUN, load and underflow are equal to 1; the load bit will be automatically cleared to zero on the next clock cycle, and at the same time the counter register value will be loaded to the 10-bit down-counter.

The pulse width of each PWM output is determined by the Compare Registers of PWM0L through PWM3L, and PWM0H through PWM3H. When PWM Compare Register is greater than 10-bits counter value, the PWM output is low. Otherwise, the PWM output is high. The PWM output high pulses width is given by:

t_{HI} = (PWMP – PWMn+1).

For alteration of PWMn width, new values need to be programmed to PWMn registers, and Load bit set to 1. Note that the new PWMn width will only take effect after next underflow.

There is an invert bit for each PWMn output. It can be used to invert PWMn output. This device also has an interrupt flag for PWM underflow. When PWM 10-bit down-counter underflow, PWMF flag (PWMCON1.5) will be asserted. PWM interrupt is requested if PWM interrupt is enabled (EIE.5). PWMF can only be cleared by software.

Note :

1. A compare value of all zeroes, 000H, causes the PWM output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remain permanently low. A compare value greater than the counter reloaded value will result in the PWM output being permanently low.
2. When the PWMRUN is cleared, the PWM outputs take on the state prior to the bit being cleared. In general, this state is not known. In order to place the PWM output in a known state when PWMRUN is cleared;
   - Program Compare Registers to either the “always 1” or “always 0” (see note 1).
   - Set Load (and PWMRUN) bits to 1.
   - Wait for PWMF underflow flag or Load bit (=0).
   - Clear PWMRUN.

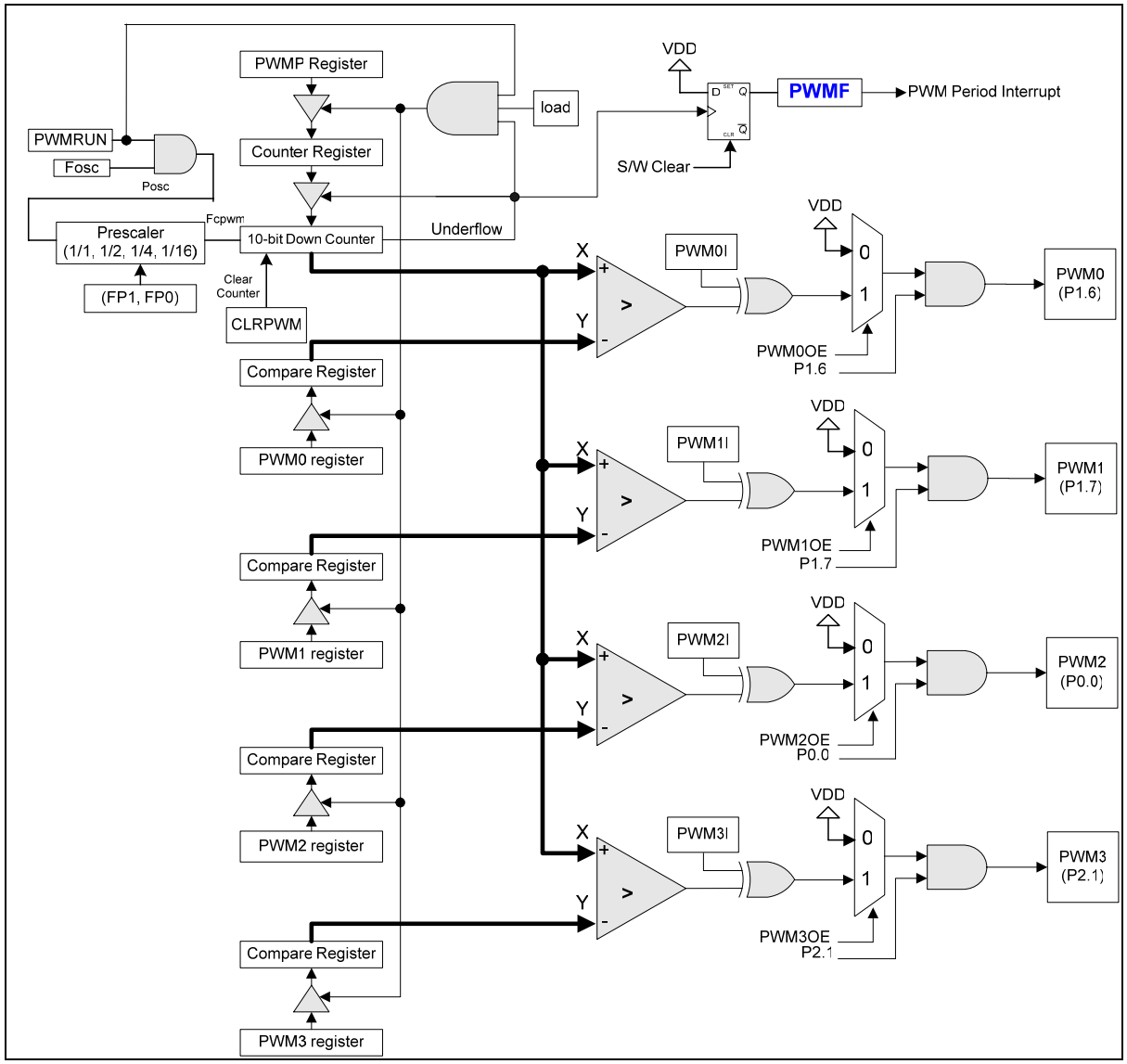


Figure 23- 1: PWM Block Diagram

24. ANALOG-TO-DIGITAL CONVERTER

The ADC contains a DAC which converts the contents of a successive approximation register to a voltage (V_{DAC}) which is compared to the analog input voltage (Vin). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. A conversion is initiated by setting ADCS in the ADCCON register. ADCS can be set by software only or by either hardware or software.

The software only start mode is selected when control bit ADCCON.5 (ADCEX) =0. A conversion is then started by setting control bit ADCCON.3 (ADCS) The hardware or software start mode is selected when ADCCON.5 =1, and a conversion may be started by setting ADCCON.3 as above or by applying a rising edge to external pin STADC. When a conversion is started by applying a rising edge, a low level must be applied to STADC for at least one machine cycle followed by a high level for at least one machine cycle.

The low-to-high transition of STADC is recognized at the end of a machine cycle, and the conversion commences at the beginning of the next cycle. When a conversion is initiated by software, the conversion starts at the beginning of the machine cycle which follows the instruction that sets ADCS. ADCS is actually implemented with tpw flip-flops: a command flip-flop which is affected by set operations, and a status flag which is accessed during read operations.

The next two machine cycles are used to initiate the converter. At the end of the first cycle, the ADCS status flag is set end a value of “1” will be returned if the ADCS flag is read while the conversion is in progress. Sampling of the analog input commences at the end of the second cycle.

During the next eight machine cycles, the voltage at the previously selected pin of one of analog input pin is sampled, and this input voltage should be stable in order to obtain a useful sample. In any event, the input voltage slew rate must be less than 10V/ms in order to prevent an undefined result.

The successive approximation control logic first sets the most significant bit and clears all other bits in the successive approximation register (10 0000 0000b). The output of the DAC (50% full scale) is compared to the input voltage Vin. If the input voltage is greater than V_{DAC}, then the bit remains set; otherwise if is cleared.

The successive approximation control logic now sets the next most significant bit (11 0000 0000b or 01 0000 0000b, depending on the previous result), and the V_{DAC} is compared to Vin again. If the input voltage is greater then V_{DAC}, then the bit remains set; otherwise it is cleared. This process is repeated until all ten bits have been tested, at which stage the result of the conversion is held in the successive approximation register. The conversion takes four machine cycles per bit.

The end of the 10-bit conversion is flagged by control bit ADCCON.4 (ADCI). The upper 8 bits of the result are held in special function register ADCH, and the two remaining bits are held in ADCCON.7 (ADC.1) and ADCCON.6 (ADC.0). The user may ignore the two least significant bits in ADCCON and use the ADC as an 8-bit converter (8 upper bits in ADCH). In any event, the total actual conversion time is 52 machine cycles. ADCI will be set and the ADCS status flag will be reset after the ADCS is set.

Control bits ADCCON.0, ADCCON.1 and ADCCON.2 are used to control an analog multiplexer which selects one of eight analog channels. An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1.

The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode.

When ADCON.5 (ADCEX) is set by external pin to start ADC conversion, after W79E834 series have entered idle mode, P1.4 can start ADC conversion at least 1 machine cycle.

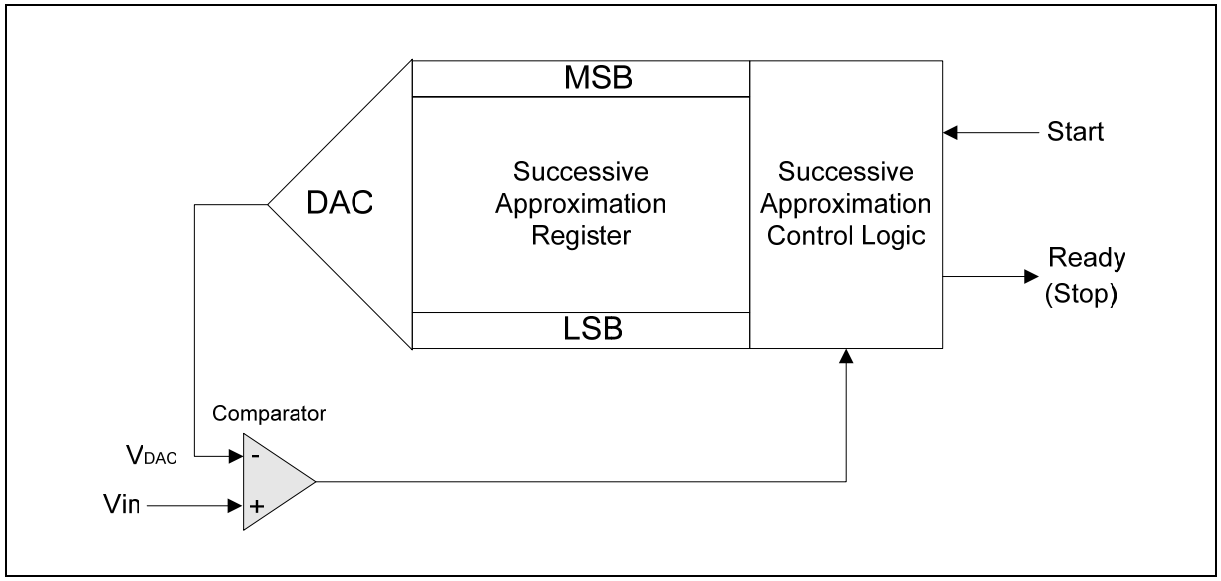


Figure 24- 1: Successive Approximation ADC

24.1 ADC Resolution and Analog Supply:

The ADC circuit has its own supply pins (AVDD and AVSS) and one pins (Vref+) connected to each end of the DAC's resistance-ladder that the AVDD and Vref+ are connected to VDD and AVSS is connected to VSS. The ladder has 1023 equally spaced taps, separated by a resistance of "R". The first tap is located 0.5×R above AVss, and the last tap is located 0.5×R below Vref+. This gives a total ladder resistance of 1024×R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between AVss and [(Vref+) + ½ LSB], the 10-bit result of an A/D conversion will be 0000000000B = 000H. For input voltages between [(Vref+) – 3/2 LSB] and Vref+, the result of a conversion will be 1111111111B = 3FFH. Vref+ and AVSS may be between AV_{DD} + 0.2V and AV_{SS} – 0.2 V. Vref+ should be positive with respect to AVSS, and the input voltage (Vin) should be between Vref+ and AVSS.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{Vin}{Vref+} \quad \text{or Result} = 1024 \times \frac{Vin}{VDD}$$

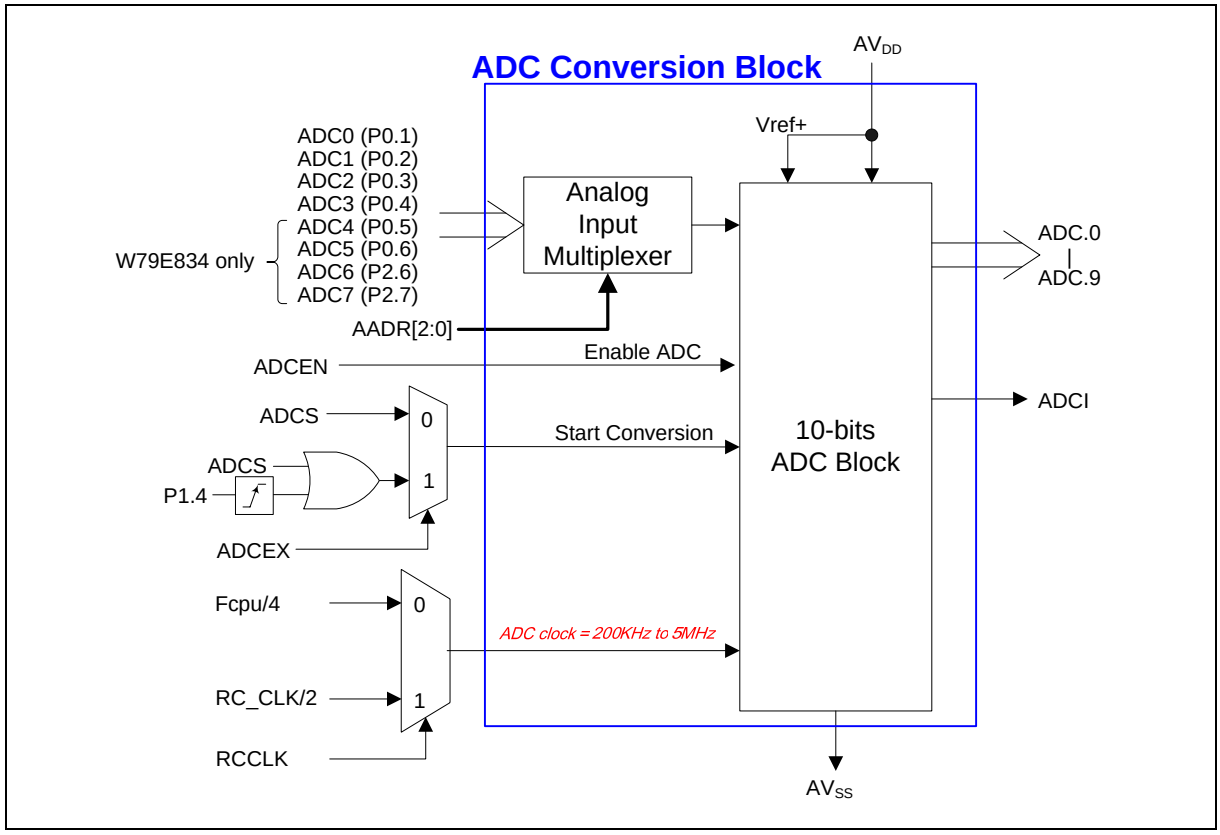


Figure 24- 2: ADC Block Diagram

25. ICP (IN-CIRCUIT PROGRAM) FLASH PROGRAM

The contexts of flash in W79E834 series are empty by default. At the first use, you must program the flash EPROM by external Writer device or by ICP (In-Circuit Program) tool.

In the ICP tool, the user must be taken ICP's program pins before design in system design board which pins in some application circuits are P1.5, P0.4 and P0.5, as shown at figure below. In the ICP program, the P1.5 must set to high voltage (~10.5V), and keeping this voltage to update code, data and/or configure CONFIG bits. After finished, the high voltage of P1.5 will be released. So when use ICP program to suggest the power need power off then power on after ICP program was finished on the system board.

After entry ICP program mode, all pin will be set to quasi-bidirectional mode, and output to level "1".

W79E834 series support programming of Flash EPROM that is 8K/4K/2K bytes AP Flash EPROM. This mode can separate update code or all update at AP Flash EPROM.

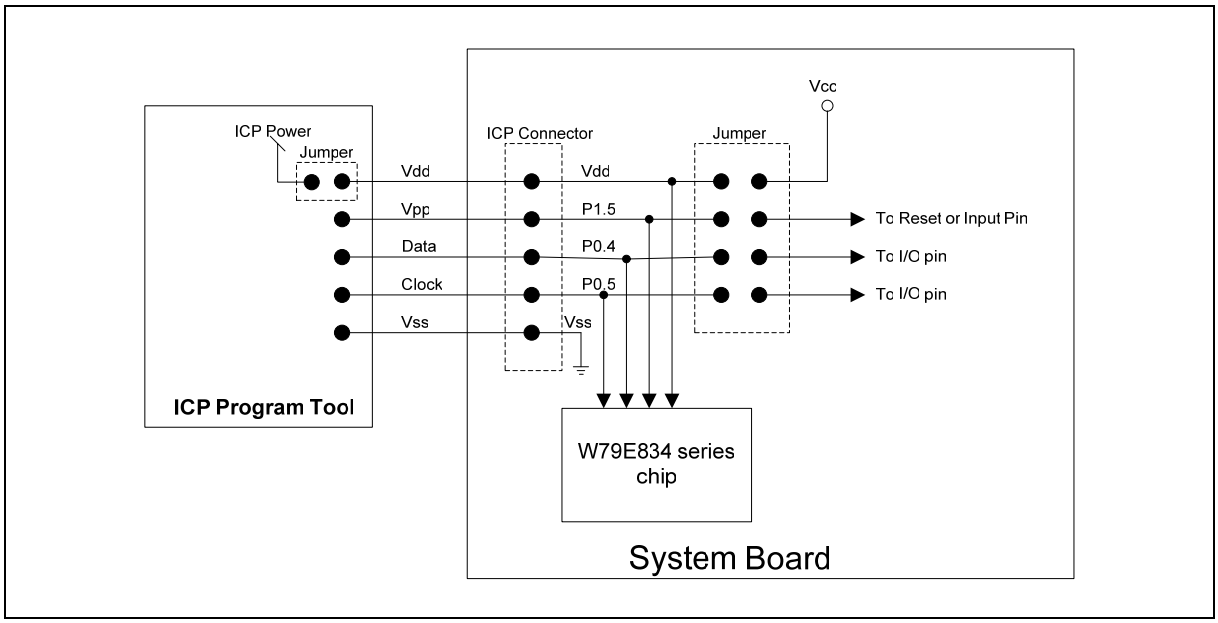


Figure 25- 1: ICP System Board

Note: 1. When using ICP to upgrade code, the P1.5, P0.4 and P0.5 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.
3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.

26. CONFIG BITS

W79E834 series have two CONFIG bits (CONFIG1, CONFIG2) that must be defined at power up and can not be set the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG2) and those operations on it are described below. The data of these bytes may be read by the MOVX instruction at the addresses FB00H~FB01H.

26.1 CONFIG1

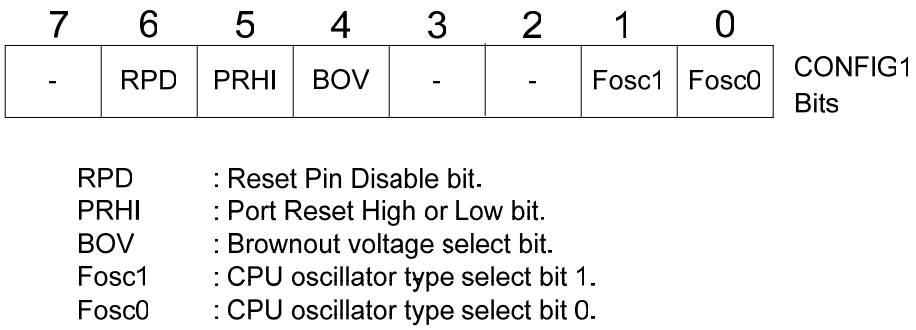


Figure 26- 1: Config1 Register

BIT	NAME	FUNCTION
7	-	Reserved.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.5. 1: Disable Reset function of Pin 1.5, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4	BOV	Brownout Voltage Select bit: 0: Brownout detect voltage is 3.8V. 1: Brownout detect voltage is 2.5V.
3	-	Reserved.
2	-	Reserved.
1	Fosc1	CPU Oscillator Type Select bit 1.
0	Fosc0	CPU Oscillator Type Select bit 0.

Oscillator Configuration bits:

FOSC1	FOSC0	OSC SOURCE
0	0	4MHz ~ 20MHz crystal
0	1	Internal RC Oscillator
1	0	Reserved
1	1	External Oscillator in XTAL1

26.2 CONFIG2

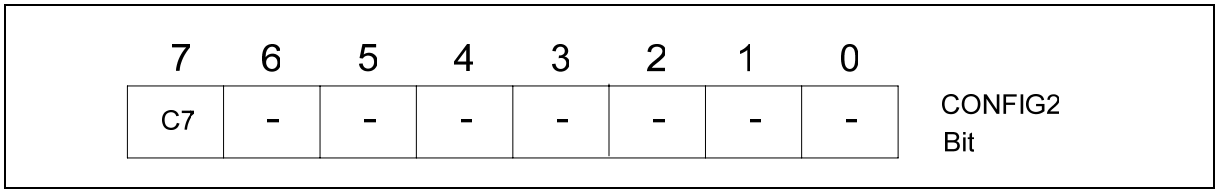


Figure 26- 2: Config2 Register

C7: 8K/4K/2K Flash EPROM Lock bit

This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.

BIT 7	FUNCTION DESCRIPTION
1	The security of 8K/4K/2KB program code is not locked; It can be erased, programmed or read by Writer or ICP Writer.
0	The 8K/4K/2KB program code area is locked; It can't be read by Writer or ICP Writer.

27. ELECTRICAL CHARACTERISTICS

27.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current suck by a I/O pin			25	mA
Maximum Current sourced by a I/O pin			25	mA
Maximum Current suck by total I/O pins			75	mA
Maximum Current sourced by total I/O pins			75	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

27.2 DC Electrical Characteristics

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.7		5.5	V	V_{DD} =4.5V ~ 5.5V @ 20MHz V_{DD} =2.7V ~ 5.5V @ 12MHz
Operating Current	I_{DD1}		18	25	mA	V_{DD} = 5.0V @ 20MHz, No load, /RST = Vss
			6	8	mA	V_{DD} = 3.0V @ 12MHz, No load, /RST = Vss
	I_{DD2}		23	29	mA	V_{DD} = 5.0V @ 16MHz, No load, /RST = V_{DD}, Run NOP
			6.5	9	mA	V_{DD} = 3.0V @ 12MHz, No load, /RST = V_{DD}, Run NOP
Idle Current	I_{IDLE}		11.5	15	mA	V_{DD} = 5.5V, 16 MHz, no load
			5	6.5	mA	V_{DD} = 3.0V, 12 MHz, no load

Continued

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Power Down Current	I_{PWDN}		1	10	µA	V_{DD} = 5.5V, no load @ Disable BOV function
			1	10	µA	V_{DD} = 3.0V, no load @ Disable BOV function
Input Current P0, P1, P2, P3.0, P3.1	I_{IN1}	-50	-	+15	µA	V_{DD} = 5.5V, V_{IN} = 0V<V_{IN}<V_{DD}
Input Current P1.5(/RST pin)[1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2, P3.0, P3.1 (Open Drain)	I_{LK}	-10	-	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3.0, P3.1	I_{TL} [*3]	-500	-	-200	µA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage P0, P1, P2, P3.0, P3.1 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6		V_{DD} = 2.7V
Input High Voltage P0, P1, P2, P3.0, P3.1 (TTL input)	V_{IH1}	2.2	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.8	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	
Positive going threshold (Schmitt input)	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	
Hysteresis voltage	V_{HY}		$0.2V_{DD}$		V	
Source Current P0, P1, P2, P3.0, P3.1 (Quasi-bidirectional and weak pull-up Mode)	I_{SR2}	-150	-210	-360	µA	V_{DD} = 4.5V, V_S = 2.4V
Sink Current P0, P1, P2, P3.0, P3.1 (Quasi-bidirectional and weak pull-up Mode)	I_{SK2}	13	18.5	24	mA	V_{DD} = 4.5V, V_S = 0.45V

Continued

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Output Low Voltage P0, P1, P2, P3.0, P3.1 (PUSH-PULL Mode)	V_{OL1}	-	0.5	0.9	V	V_{DD} = 4.5V, I_{OL} = 20 mA
		-	0.1	0.4	V	V_{DD} = 2.7V, I_{OL} = 3.2 mA
Output High Voltage P0, P1, P2, P3.0, P3.1 (PUSH-PULL Mode)	V_{OH}	2.4	3.4	-	V	V_{DD} = 4.5V, I_{OH} = -16mA
		1.9	2.4	-		V_{DD} = 2.7V, I_{OH} = -3.2mA
Brownout voltage with BOV=1	$V_{BO2.5}$	2.4	-	2.7	V	
Brownout voltage with BOV=0	$V_{BO3.8}$	3.5	-	4	V	

Notes: *1. /RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

*3. Pins of P0, P1, and P2 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

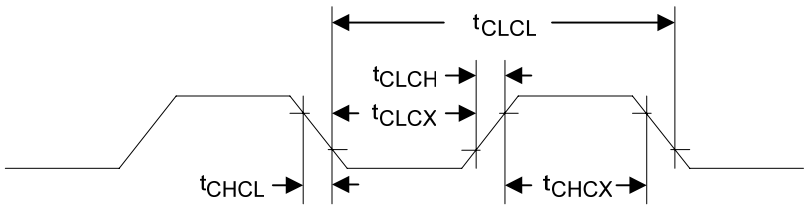
27.3 The ADC Converter DC Electrical Characteristics

(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fosc = 20MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Analog input	AVin	V_{SS}-0.2		V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz	-	5MHz	Hz	ADC block circuit input clock
Conversion time	t_C		$52t_{ADC}$ [1]		us	
Differential non-linearity	DNL	-1	-	+1	LSB	
Integral non-linearity	INL	-2	-	+2	LSB	
Offset error	Ofe	-1	-	+1	LSB	
Gain error	Ge	-1	-	+1	%	
Absolute voltage error	Ae	-3	-	+3	LSB	

Notes: 1. tADC: The period time of ADC input clock.

27.4 AC Electrical Characteristics



Note: Duty cycle is 50%.

27.5 External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12.5	-	-	nS	
Clock Low Time	t_{CLCX}	12.5	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

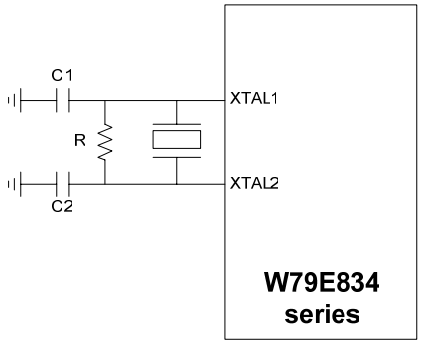
27.6 AC Specification

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	20	MHz

27.7 Typical Application Circuits

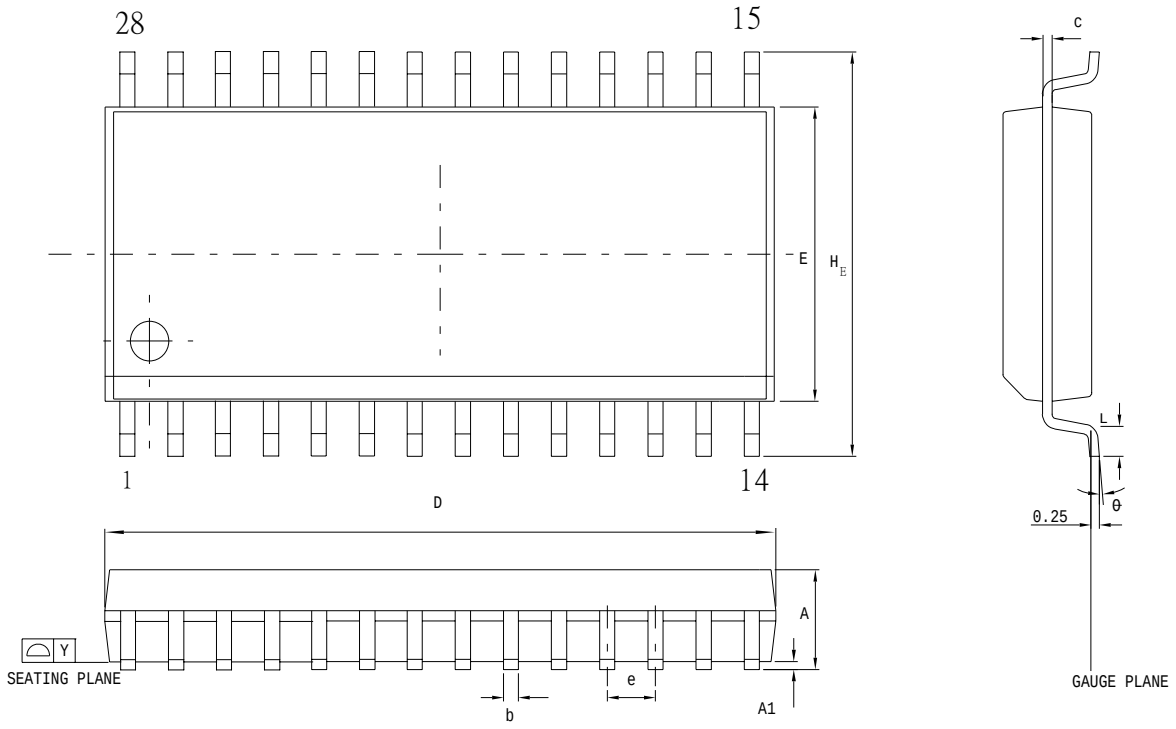
CRYSTAL	C1	C2	R
4MHz ~ 20MHz	without	without	without

The above table shows the reference values for crystal applications.



28. PACKAGE DIMENSIONS

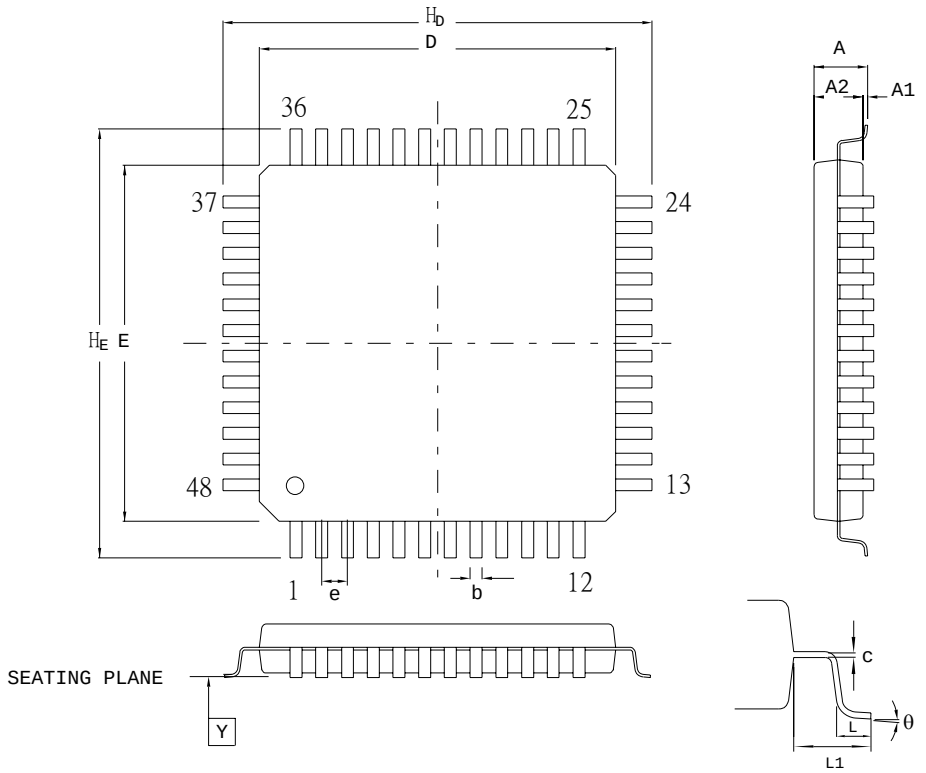
28.1 28L SOP-300mil



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	17.70	18.10	0.697	0.713
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	———	0.10	———	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

28.2 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

29. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 29, 2007	-	Initial Issued
A2	August 9,2007	2	Change “Lead Free (RoHS) SOP 28/24/20: W79E833ASG” to “Lead Free (RoHS) SOP 28: W79E833ASG “
		2	Change “Lead Free (RoHS) SOP 28/24/20: W79E832ASG” to “Lead Free (RoHS) SOP 28: W79E832ASG”
		3	Change “W79E833 PACKAGE:SOP-28/24/20 Pin “ to “W79E833 PACKAGE:SOP-28 Pin”
		3	Change “W79E832 PACKAGE:SOP-28/24/20 Pin” to “W79E832 PACKAGE:SOP-28 Pin”
		5	Change ” W79E833ASG\W79E833ADG\W79E832ASG\ W79E832ADG SOP/DIP 28-PIN” to “W79E833ASG \W79E832ASG SOP 28-PIN “
		2	Remove “Lead Free (RoHS) DIP 28/24/20:W79E833ADG”
		2	Remove “Lead Free (RoHS) DIP 28/24/20:W79E832ADG”
		3	Remove “W79E832AD 2KB 256B 0B 4x10Bit 4x10Bit DIP-28/24/20 Pin”
		3	Remove “W79E833ADG 4KB 256B 0B 4x10Bit 4x10Bit DIP-28/24/20 Pin”
		5	Remove ” W79E833ASG\W79E833ADG\W79E832ASG\ W79E832ADG SOP/DIP 24-PIN”
		5	Remove ”W79E833ASG\W79E833ADG\W79E832ASG\W79E832ADG SOP/DIP 20-PIN”
		130-134	Remove “24L SOP/20L SOP/28L PDIP/24L PDIP/20L PDIP”
A2-2	August 31, 2007	112	Rename H to b.
		45	Updated ADCS bit descriptions.
		33, 82	Added programming note for digital filter.
		44, 81	All WDCON bits except WTRF are TA protected.
		117-118	Revised PWM descriptions.
		88	Updated Timer 2 compare/reload diagram to visio format.

A2-3	September 3, 2007	88	Updated Figure 15-8 to visio format.
A2-4	September 7, 2007	8 All	Updated pin configuration figures to use proper overbar on pin names. Change Logo.
A3	December 27, 2007	24	Revise the content of UART mode select table. (SM0, SM1) is exchanged.
A4	February 21, 2008	63-64 75 114 121 123 128	Add Figure11-1, 11-2 for reset and VDD monitor timing diagram. Revise Figure 14-1 Watchdog Timer diagram Revise Figure 21-1 Oscillator diagram Revise Figure 24-2 ADC Block diagram Remove Config1 bit7 WDTE function Revise Chapter 27.6 oscillator from 16MHz to 20MHz

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