Stellaris® LM3S5951 RevB1 Errata

This document contains known errata at the time of publication for the Stellaris® LM3S5951 microcontroller. The table below summarizes the errata and lists the affected revisions. See the data sheet for more details.

See also the ARM® Cortex™-M3 errata, ARM publication number PR326-PRDC-009450 v2.0.

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Erratum Number	Erratum Title	Revision(s) Affected
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10.2	When in IrDA mode, the UnRx signal requires configuration even if not used	B1
11.1	An interrupt is not generated when using µDMA with the SSI module if the EOT bit is set	B1
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1 JTAG

1.1 JTAG INTEST instruction does not work

Description:

The JTAG INTEST (Boundary Scan) instruction does not properly capture data.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

1.2 The Recover Locked Device sequence does not work

Description:

If software configures any of the JTAG/SWD pins as GPIO or loses the ability to communicate with the debugger, there is a debug sequence that can be used to recover the microcontroller, called the Recover Locked Device sequence. After reconfiguring the JTAG/SWD pins, using the Recover Locked Device sequence does not recover the device.

Workaround:

To get the device unlocked, follow these steps:

1. Power cycle the board and run the debug port unlock procedure in LM Flash Programmer. DO NOT power cycle when LM Flash Programmer tells you to.

2. Go to the Flash Utilities tab in LM Flash Programmer and do a mass erase operation (check "Entire Flash" and then click the Erase button). This erase appears to have failed, but that is ok.

3. Power cycle the board.

4. Go to the Flash Utilities tab in LM Flash Programmer and do another mass erase operation (check "Entire Flash" and then click the Erase button).

Silicon Revision Affected:

B1, C0

Fixed:

Not fixed in Rev C.

2 System Control

2.1 Hard Fault possible when waking from Sleep or Deep-Sleep modes and Cortex-M3 Debug Access Port (DAP) is enabled

Description:

If the Cortex-M3 Debug Access Port (DAP) has been enabled, and the device wakes from a low power sleep or deep-sleep mode, the core may start executing code before all clocks to peripherals have been restored to their run mode configuration. The DAP is usually enabled by software tools accessing the JTAG or SWD interface when debugging or flash programming. If this condition occurs, a Hard Fault is triggered when software accesses a peripheral with an invalid clock.

Workaround:

A software delay loop can be used at the beginning of the interrupt routine that is used to wake up a system from a WFI (Wait For Interrupt) instruction. This stalls the execution of any code that accesses a peripheral register that might cause a fault. This loop can be removed for production software since the DAP is most likely not enabled during normal execution.

Since the DAP is disabled by default (power on reset), the user can also power cycle the device. The DAP will not be enabled unless it is enabled through the JTAG or SWD interface.

Silicon Revision Affected:

B1, C0

Fixed:

Will not be fixed.

2.2 Sleep and Deep-Sleep mode not usable at higher speeds when ISRs reside in Flash memory

Description:

Sleep and Deep-Sleep modes cannot be used when running the processor at 66 or 80 MHz when the ISRs and vector table reside in Flash memory. If Sleep or Deep-Sleep mode is used at those speeds, an invalid PC is sometimes returned for the interrupt vector address when exiting sleep mode.

Workaround:

There are two possible workarounds for this issue:

1. Store the ISRs and vector table in the on-chip SRAM when running the processor at 66 or 80 MHz.
2. Run the processor at 50 MHz.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

2.3 Device Capabilities registers may not accurately reflect available signals

Description:

Some of the Device Capabilities register bits reflect the presence of specific pins on the microcontroller. These bits do not always properly reflect the available signals. Bits affected include **DC3** [31:0], **DC4** [15:14], **DC5** [27:24] and [7:0], and **DC8** [31:0]. Do not rely on the value of these bits in system design.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

2.4 The PIOSC is not trimmed by the factory

Description:

The PIOSC is not trimmed by the factory prior to shipment. This errata item affects any product with date codes prior to 0946.

Workaround:

For parts that have a Hibernation module, the PIOSC can be user calibrated. The PIOSC cannot be calibrated on parts without a Hibernation module.

Silicon Revision Affected:

B1

Fixed:

Fixed for devices with date codes beginning 0946.

3 Hibernation Module

3.1 Hibernation module may have higher current draw than specified in data sheet under certain conditions

Description:

If a battery voltage is applied to the VBAT power pin prior to power being applied to the VDD power pins of the device, the current draw from the VBAT pin is greater than expected. The current may be as high as 1.6 mA instead of the data sheet specified 17 µA. The condition exists until power is applied to the VDD pin. Once the VDD pin has been powered, the VBAT current draw functions as expected. The VDD pin can then be powered up and down as required and the VBAT pin current specification is maintained.

Workaround:

The VBAT pin higher-than-specified current draw condition can be avoided if the microcontroller's VDD power pins are powered on prior to the time a battery voltage is initially applied to the VBAT pin.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.2 Hibernate POR may not reset the Hibernation module until V_{DD} is applied

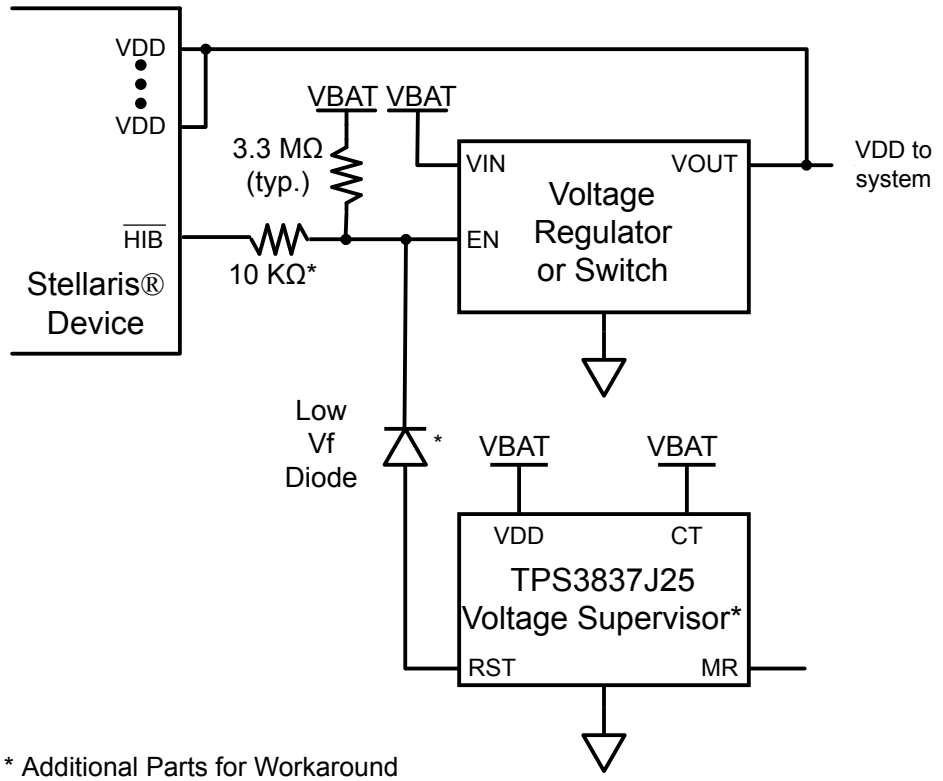
Description:

If V_{DD} is not powered when voltage is first applied to V_{BAT}, the state of the Hibernation module is indeterminate and the $\overline{\text{HIB}}$ signal may be asserted. In this indeterminate state, a lock condition can occur in which the Hibernation module waits for a power-on-reset, but that reset cannot occur until the module deasserts $\overline{\text{HIB}}$. This issue is related to the errata “Hibernation module may have higher current draw than specified in data sheet under certain conditions” on page 5.

Workaround:

The workaround implementation depends on the system-level power supply configuration. For systems that use a battery as the primary power source, an external voltage supervisor (TPS383J25DBV or similar) circuit can be added to force the V_{DD} power supply to start when the battery voltage is first applied (see Figure 1). The voltage supervisor requires only 220 nA and generates a 200-ms positive pulse to turn on the V_{DD} regulator and activate the microcontoller's internal POR circuit.

Figure 1. Workaround Circuit to Ensure Initial Power Up



Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.3 Power consumption increases if V_{DD} is not restored after wake from hibernation

Description:

If a wake event occurs and V_{DD} does not rise to specified levels, then the wake event is held off until V_{DD} is within specified levels. If a large delay occurs between the wake event and VDD reaching specified levels, the V_{BAT} current increases substantially to a typical value of 255 µA until V_{DD} reaches the specified levels, at which point the microcontroller comes out of hibernation and power consumption returns to expected levels.

Workaround:

Ensure that V_{DD} reaches specified levels within 250 µs after the wake event occurs.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.4 ESD protection on the V_{BAT} pin does not meet specifications

Description:

The ESD protection on the V_{BAT} pin fails when tested at 2 kV.

Workaround:

Extra precaution should be taken to protect the part from ESD events. Some applications may require system-level ESD protection on this pin.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.5 Use of the VDD3ON mode to initiate hibernation damages the part

Description:

The VDD3ON mode is enabled by setting the VDD3ON bit in the **Hibernation Control (HIBCTL)** register. Permanent damage can occur to the device if this mode is used.

Workaround:

Do not use the VDD3ON mode to enter hibernation, instead use an external switch or regulator to manage V_{DD} power to the device.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.6 Hibernate module power consumption higher than expected in event wakeup configuration

Description:

With the Hibernation module configured for an external event wakeup, the current consumption of the device is higher than expected. The Hibernation module clock does not shut down properly during the hibernate asynchronous external wake mode resulting in extra current consumption. Some devices properly shut down the clock the first time entering this mode and others do not. When waking from a hibernate event, the Hibernation module clock is always enabled. In subsequent hibernate cycles, the oscillator is not shut down properly and remains active. Hibernate module current consumption averages 21µA with the clock disabled. The current consumption averages 31µA with the Hibernation module clock enabled.

Workaround:

When the Hibernation module clock is not required during hibernation, software can disable it by clearing the CLK32EN bit in the **Hibernation Control (HIBCTL)** register before going into hibernation mode.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.7 The Real-Time Clock gains or loses time going in and out of hibernation when using a crystal

Description:

When using a 4.194304-MHz crystal, the Real-Time clock in the Hibernation module gains or loses a small amount of time (on the order of one second over a 24-hour period when cycling hibernate mode 4 times a minute) when going in and out of hibernation.

Workaround:

Use an external 32.768-kHz oscillator as the source for the Hibernation module clock.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.8 Low-battery detect circuit is powered down during hibernate

Description:

The low-battery detect feature on the V_{BAT} input is only valid when V_{DD} power is present. As a result:

- Because the battery is not electrically loaded when V_{DD} is present, the low-battery detect circuit may not reflect the actual battery status.
- In Hibernate mode, a low-battery condition may prevent wake until the battery is completely depleted.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

3.9 Writes to Hibernation module registers sometimes fail

Description:

Due to the independent clock domain of the Hibernation module, writes may sometimes fail, even though the WRC bit in the **HIBCTL** register is set after the write occurs.

Workaround:

After performing a write to any Hibernation module register or non-volatile memory, read the contents back and verify that they are correct. If they are incorrect, perform the write operation again.

Silicon Revision Affected:

B1, C0

Fixed:

Not fixed in Rev C.

4 Internal Memory

4.1 Cumulative page erases may introduce bit errors in Flash memory

Description:

Cumulative page erases anywhere in the Flash memory array may introduce bit errors. The bit error is not confined to the page being erased or the 4-KB block but could be in any page in the Flash memory. A page erase is used to erase a 1-KB page so it can be rewritten. A mass erase erases the entire Flash memory array (all pages). A bit error means that a bit may change from 0 to 1 or 1 to 0.

Workaround:

There are two possible workarounds for this issue:

1. Minimize total page erases to less than 3000 between mass erases for the lifetime of the product. After each mass erase, an additional 3000 page erase operations are allowed before bit errors may be introduced. At the rate of one page erase per week, this issue would not be seen over at least 17 years.
2. Perform CRC checks on all Flash memory after page erases to increase the chances of detecting the issue. The two CRC functions built into ROM can assist in this.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

4.2 Flash Write Buffer does not function above 50 MHz

Description:

The Flash Write Buffer does not successfully program the Flash memory at speeds above 50 MHz.

Workaround:

Lower the speed of the system clock to 50 MHz or less while programming the Flash memory.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

5 ROM

5.1 Some ROM functions are unsupported

Description:

The following functions are unsupported in ROM:

- CANBitRateSet
- GPIOPinConfigure
- GPIOPinTypeI2S
- I2CSlaveIntClearEx
- I2CSlaveIntDisableEx
- I2CSlaveIntEnableEx
- I2CSlaveIntStatusEx
- I2SIntClear
- I2SIntDisable
- I2SIntEnable
- I2SIntStatus
- I2SMasterClockSelect
- I2SRxConfigSet
- I2SRxDataGet
- I2SRxDataGetNonBlocking
- I2SRxDisable
- I2SRxEnable
- I2SRxFIFOLevelGet
- I2SRxFIFOLimitGet
- I2SRxFIFOLimitSet
- I2STxConfigSet
- I2STxDataPut
- I2STxDataPutNonBlocking
- I2STxDisable
- I2STxEnable
- I2STxFIFOLevelGet
- I2STxFIFOLimitGet
- I2STxFIFOLimitSet
- I2STxRxConfigSet
- I2STxRxDisable
- I2SRxDataGet
- I2STxRxEnable
- SysCtlDelay
- SysCtlI2SMClkSet
- UARTBusy
- UARTFIFODisable

- UARTFIFOEnable
- UARTRxErrorClear
- UARTRxErrorGet
- UARTTxIntModeGet
- UARTTxIntModeSet
- uDMAChannelSelectDefault
- uDMAChannelSelectSecondary
- USBDevEndpointConfigGet
- USBEndpointDataAvail
- USBEndpointDMAChannel
- USBEndpointDMADisable
- USBEndpointDMAEnable
- USBModeGet
- USBOTGHostRequest

Workaround:

Code for these functions is included in the current version of StellarisWare, which can be downloaded from the website at http://www.luminarymicro.com/products/software_updates.html.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

5.2 ROM mapping check for the Boot loader does not function properly

Description:

Before the processor is released from the reset state, the System Control module is supposed to check offset 0x0000.0004 of Flash memory looking for a reset vector that is not 0xFFFF.FFFF. If an initialized reset vector is found, Flash memory is mapped to address 0x0000.0000, otherwise ROM is mapped to address 0x0000.0000. Currently, the System Control module errantly checks offset 0x0000.0008, which is the NMI vector. So, in situations where a valid reset vector (offset 0x0000.0004) has been programmed, but the NMI vector has not been programmed, the ROM is errantly mapped to zero preventing the application that is stored in Flash memory from being executed out of reset.

Workaround:

Ensure that the NMI vector is always programmed.

Silicon Revision Affected:

B1

Fixed:

Not fixed in Rev C.

6 GPIO

6.1 Port B [1:0] pins require external pull-up resistors

Description:

The internal pull-up resistors are not effective for the Port B0 and B1 pins.

Workaround:

External pull-up resistors must be used on these two pins when they are used as GPIOs.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

7 General-Purpose Timer

7.1 The General-Purpose Timer match register does not function correctly in 32-bit mode

Description:

The **GPTM Timer A Match (GPTMTAMATCHR)** register triggers a match interrupt if the lower 16 bits match, regardless of the value of the upper 16 bits.

Workaround:

None.

Silicon Revision Affected:

B1, C0

Fixed:

Not fixed in Rev C.

8 Watchdog Timer 1

8.1 Writes to Watchdog Timer 1 module WDTLOAD register sometimes fail

Description:

Due to the independent clock domain of the Watchdog Timer 1 module, writes to the **Watchdog Load (WDTLOAD)** register may sometimes fail, even though the WRC bit in the **WDTCTL1** register is set after the write occurs.

Workaround:

After performing a write to the **WDTLOAD** register, read the contents back and verify that they are correct. If they are incorrect, perform the write operation again.

Silicon Revision Affected:

B1, C0

Fixed:

Not fixed in Rev C.

9 ADC

9.1 ADC hardware averaging produces erroneous results in differential mode

Description:

The implementation of the ADC averaging circuit does not work correctly when the ADC is sampling in differential mode and the difference between the voltages is approximately 0.0V.

Workaround:

Do not use hardware averaging in differential mode. Instead, use the FIFO to store results and average them in software.

Silicon Revision Affected:

B1, C0

Fixed:

Not fixed in Rev C.

10 UART

10.1 UART Smart Card (ISO 7816) mode does not function

Description:

The UnTX signal does not function correctly as the bit clock in Smart Card mode.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

10.2 When in IrDA mode, the UnRx signal requires configuration even if not used

Description:

When in IrDA mode, the transmitter may not function correctly if the UnRx signal is not used.

Workaround:

When in IrDA mode, if the application does not require the use of the UnRx signal, the GPIO pin that has the UnRx signal as an alternate function must be configured as the UnRx signal and pulled High.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

11 SSI

11.1 An interrupt is not generated when using µDMA with the SSI module if the EOT bit is set

Description:

When using the primary µDMA channels with the SSI module, an interrupt is not generated on transmit µDMA completion if the EOT bit (bit 4 of the **SSICR1** register) is enabled.

Workaround:

Use the alternate µDMA channels for the SSI module.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

12 I2S

12.1 Some bits in the I2SMCLKCFG register do not function

Description:

The top 2 bits of the RXI and TXI bit fields in the **I2SMCLKCFG** register do not function (bits [29:28] of RXI and bits [13:12] of TXI). The RXI and TXI fields contain the 10-bit integer input for the receive and transmit clock generator, respectively. The remaining 8 bits in each field function correctly, so most of the possible integer input choices can be used in system design.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

12.2 I²S SCLK signal is inverted in certain modes

Description:

When the I²S controller is operating as a receiver in SCLK Master mode, the WS signal is latched on the rising edge of SCLK, not the falling edge. In addition, when the controller is operating as a transmitter in SCLK Slave mode, the data is launched on the rising edge of SCLK, not the falling edge.

Workaround:

For the transmitter, there are two possible workarounds for this issue:

1. Ensure that the I2S0TXSCK signal leads the I2S0TXWS signal by at least 4 ns.
2. Configure as I²S mode with DAC in Left-Justified audio format.

For the receiver, ensure that the CODEC is configured as the SCLK master, and the I²S receive module is configured as the SCLK slave.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

13 USB

13.1 USB0ID and USB0VBUS signals are required to be connected regardless of mode

Description:

The DEVMODOTG bit in the **USB General-Purpose Control and Status (USBGPCS)** register does not function correctly.

Workaround:

Connect the USB0VBUS input to VBUS in all modes. In addition, connect the USB0ID pin to ground for Host mode operation and to VDD for Device mode operation using the DEVMOD bit in the **USB General-Purpose Control and Status (USBGPCS)** register.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

13.2 Latch up may occur if power is applied to the VBUS pin but not to VDD

Description:

If power is applied to the VBUS pin but not to VDD, the microcontroller may latch up and or draw excessive current. This condition can occur if the microcontroller is unpowered and is connected as a USB device or OTG B.

Workaround:

Power up the microcontroller before attaching the USB cable. Also, the USB cable must be detached before powering down the microcontroller.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

14 PWM

14.1 PWM generation is incorrect with extreme duty cycles

Description:

If a PWM generator is configured for Count-Up/Down mode, and the **PWM Load (PWMnLOAD)** register is set to a value N, setting the compare to a value of 1 or N-1 results in steady state signals instead of a PWM signal. For example, if the user configures PWM0 as follows:

- PWMENABLE = 0x00000001
  - PWM0 Enabled
- PWM0CTL = 0x00000007
  - Debug mode enabled
  - Count-Up/Down mode
  - Generator enabled
- PWM0LOAD = 0x00000063
  - Load is 99 (decimal), so in Count-Up/Down mode the counter counts from zero to 99 and back down to zero (200 clocks per period)
- PWM0GENA = 0x000000b0
  - Output High when the counter matches comparator A while counting up
  - Output Low when the counter matches comparator A while counting down
- PWM0DBCTL = 0x00000000
  - Dead-band generator is disabled

If the **PWM0 Compare A (PWM0CMPA)** value is set to 0x00000062 (N-1), PWM0 should output a 2-clock-cycle long High pulse. Instead, the PWM0 output is a constant High value.

If the **PWM0CMPA** value is set to 0x00000001, PWM0 should output a 2-clock-cycle long negative (Low) pulse. Instead, the PWM0 output is a constant Low value.

Workaround:

User software must ensure that when using the PWM Count-Up/Down mode, the compare values must never be 1 or the **PWMnLOAD** value minus one (N-1).

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

14.2 Sync of PWM does not trigger "zero" action

Description:

If the **PWM Generator Control (PWM0GENA)** register has the `ActZero` field set to 0x2, then the output is set to 0 when the counter reaches 0, as expected. However, if the counter is cleared by setting the appropriate bit in the **PWM Time Base Sync (PWMSYNC)** register, then the "zero" action is not triggered, and the output is not set to 0.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

14.3 PWM "zero" action occurs when the PWM module is disabled

Description:

The zero pulse may be asserted when the PWM module is disabled.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

14.4 PWM Enable Update register bits do not function

Description:

The ENUPDn bits in the **PWM Enable Update (PWMENUPD)** register do not function. As a result, enabling the PWM modules can't be synchronized.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

15 Electrical Characteristics

15.1 Power-on event may disrupt operation

Description:

Incorrect power sequencing during power up can disrupt operation and potentially cause device failure.

Workaround:

V_{DDC} must be applied approximately 50 µs before V_{DD}. Normally V_{DDC} is controlled by the part's internal LDO voltage regulator. The workaround requires the addition of an external regulator (see Figure 2) to ensure that V_{DDC} sequencing requirements are met (see Figure 3). Recommended regulators include FAN1112SX (SOT223) and FAN2558S12X (SOT23-5).

This fix mitigates the on-chip power issue, but does not solve it completely. During development, the Flash memory should also be reprogrammed (using LMflash or another programming tool) at least once a week.

Figure 2. Configuration of External Regulator

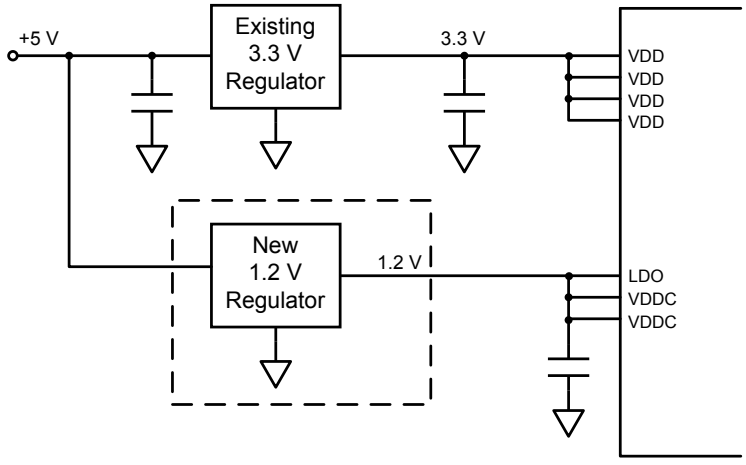
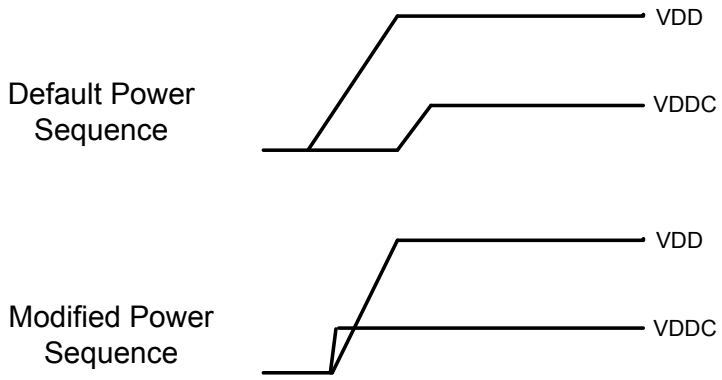


Figure 3. VDDC Sequencing Requirements



Detailed characterization is ongoing. Contact the Applications Support Team for the latest information.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C.

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