



# Stellaris® LM3S1811 Microcontroller


## DATA SHEET

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# Revision History

The revision history table notes changes made between the indicated revisions of the LM3S1811 data sheet.

**Table 1. Revision History**

Date	Revision	Description
May 2009	5285	Started tracking revision history.
June 2009	5779	<ul style="list-style-type: none"> <li>■ In System Control chapter, clarified power-on reset and external reset pin descriptions in "Reset Sources" section.</li> <li>■ Added missing comparator output pin bits to <b>DC3</b> register; reset value changed as well.</li> <li>■ Clarified explanation of nonvolatile register programming in Internal Memory chapter.</li> <li>■ Added explanation of reset value to <b>FMPRE0/1/2/3</b>, <b>FMPPE0/1/2/3</b>, <b>USER_DBG</b>, and <b>USER_REG0</b> registers.</li> <li>■ In Request Type Support table in DMA chapter, corrected general-purpose timer row.</li> <li>■ In General-Purpose Timers chapter, clarified DMA operation.</li> <li>■ Added table "Preliminary Current Consumption" to Characteristics chapter.</li> <li>■ Corrected Nom and Max values in "Hibernation Detailed Current Specifications" table.</li> <li>■ Corrected Nom and Max values in EPI Characteristics table.</li> <li>■ Added "CSn to output invalid" parameter to EPI table "EPI Host-Bus 8 and Host-Bus 16 Interface Characteristics" and figure "Host-Bus 8/16 Mode Read Timing".</li> <li>■ Corrected INL, DNL, OFF and GAIN values in ADC Characteristics table.</li> <li>■ Updated ROM DriverLib appendix with RevC0 functions.</li> <li>■ Updated part ordering numbers.</li> <li>■ Additional minor data sheet clarifications and corrections.</li> </ul>

Table 1. Revision History (*continued*)

Date	Revision	Description
July 2009	5930	<ul style="list-style-type: none"> <li>■ Added "Non-Blocking Read Cycle", "Normal Read Cycle", and "Write Cycle" sections to EPI chapter.</li> <li>■ Corrected values for MAXADC0SPD and MAXADC1SPD bits in <b>DC1</b>, <b>RCGC0</b>, <b>SCGC0</b>, and <b>DCGC0</b> registers.</li> <li>■ Corrected figure "TI Synchronous Serial Frame Format (Single Transfer)".</li> <li>■ Changed HIB pin from type TTL to type OD.</li> <li>■ Made a number of corrections to the Electrical Characteristics chapter: <ul style="list-style-type: none"> <li>– Deleted V<sub>BAT</sub> and V<sub>REFA</sub> parameters from and added footnotes to Recommended DC Operating Conditions table.</li> <li>– Modified Hibernation Module DC Characteristics table.</li> <li>– Deleted Nominal and Maximum Current Specifications section.</li> <li>– Modified EPI SDRAM Characteristics table: <ul style="list-style-type: none"> <li>• Changed t<sub>EPIR</sub> to t<sub>SDRAMR</sub> and deleted values for 2-mA and 4-mA drive.</li> <li>• Changed t<sub>EPIF</sub> to t<sub>SDRAMF</sub> and deleted values for 2-mA and 4-mA drive.</li> </ul> </li> <li>– Changed values for t<sub>COV</sub>, t<sub>COI</sub>, and t<sub>COT</sub> parameters in EPI SDRAM Interface Characteristics table.</li> <li>– Deleted SDRAM Read Command Timing, SDRAM Write Command Timing, SDRAM Write Burst Timing, SDRAM Precharge Command Timing and SDRAM CAS Latency Timing figures and replaced with SDRAM Read Timing and SDRAM Write Timing figures.</li> <li>– Modified Host-Bus 8/16 Mode Write Timing figure.</li> <li>– Modified General-Purpose Mode Read and Write Timing figure.</li> <li>– Modified values for t<sub>DV</sub> and t<sub>DI</sub> parameters, and deleted t<sub>OD</sub> parameter from EPI General-Purpose Interface Characteristics figure.</li> <li>– Major changes to ADC Characteristics tables, including adding additional tables and diagram.</li> </ul> </li> <li>■ Corrected ordering part numbers.</li> <li>■ Additional minor data sheet clarifications and corrections.</li> </ul>



Table 1. Revision History (*continued*)

Date	Revision	Description
October 2009	6419	<ul style="list-style-type: none"> <li>■ Released new 1000, 3000, 5000 and 9000 series Stellaris® devices.</li> <li>■ The IDCODE value was corrected to be 0x4BA0.0477.</li> <li>■ Clarified that the NMISSET bit in the ICSR register in the NVIC is also a source for NMI.</li> <li>■ Clarified the use of the LDO.</li> <li>■ To clarify clock operation, reorganized clocking section, changed the USEFRACT bit to the DIV400 bit and the FRACT bit to the SYSDIV2LSB bit in the RCC2 register, added tables, and rewrote descriptions.</li> <li>■ Corrected bit description of the DSDIVORIDE field in the DSLPCLKCFG register.</li> <li>■ Removed the DSFLASHCFG register at System Control offset 0x14C as it does not function correctly.</li> <li>■ Removed the MAXADC1SPD and MAXADC0SPD fields from the DCGC0 as they have no function in deep-sleep mode.</li> <li>■ Corrected address offsets for the Flash Write Buffer (FWBn) registers.</li> <li>■ Added Flash Control (FCTL) register at Internal memory offset 0x0F8 to help control frequent power cycling when hibernation is not used.</li> <li>■ Changed the name of the EPI channels for clarification: EPI0_TX became EPI0_WFIFO and EPI0_RX became EPI0_NBRFIFO. This change was also made in the DC7 bit descriptions.</li> <li>■ Removed the DMACHIS register at DMA module offset 0x504 as it does not function correctly.</li> <li>■ Corrected alternate channel assignments for the µDMA controller.</li> <li>■ Major improvements to the EPI chapter.</li> <li>■ EPISDRAMCFG2 register was deleted as its function is not needed.</li> <li>■ Clarified PWM source for ADC triggering</li> <li>■ Changed SSI set up and hold times to be expressed in system clocks, not ns.</li> <li>■ Updated Electrical Characteristics chapter with latest data. Changes were made to Hibernation, ADC and EPI content.</li> <li>■ Additional minor data sheet clarifications and corrections.</li> </ul>

## About This Document

This data sheet provides reference information for the LM3S1811 microcontroller, describing the functional blocks of the system-on-chip (SoC) device designed around the ARM® Cortex™-M3 core.

### Audience

This manual is intended for system software developers, hardware designers, and application developers.

### About This Manual

This document is organized into sections that correspond to each major feature.

### Related Documents

The following documents are referenced by the data sheet, and available on the documentation CD or from the Stellaris® web site at [www.luminarymicro.com](http://www.luminarymicro.com):

- *ARM® Cortex™-M3 Technical Reference Manual*
- *ARM® CoreSight Technical Reference Manual*
- *ARM® v7-M Architecture Application Level Reference Manual*
- *Stellaris® Peripheral Driver Library User's Guide*
- *Stellaris® ROM User's Guide*

The following related documents are also referenced:

- *IEEE Standard 1149.1-Test Access Port and Boundary-Scan Architecture*

This documentation list was current as of publication date. Please check the web site for additional documentation, including application notes and white papers.

### Documentation Conventions

This document uses the conventions shown in Table 2 on page 26.

**Table 2. Documentation Conventions**

Notation	Meaning
<b>General Register Notation</b>	
<b>REGISTER</b>	APB registers are indicated in uppercase bold. For example, <b>PBORCTL</b> is the Power-On and Brown-Out Reset Control register. If a register name contains a lowercase n, it represents more than one register. For example, <b>SRCRn</b> represents any (or all) of the three Software Reset Control registers: <b>SRCR0</b> , <b>SRCR1</b> , and <b>SRCR2</b> .
bit	A single bit in a register.
bit field	Two or more consecutive and related bits.
offset 0xnnn	A hexadecimal increment to a register's address, relative to that module's base address as specified in "Memory Map" on page 62.

Table 2. Documentation Conventions (*continued*)

Notation	Meaning
Register <i>N</i>	Registers are numbered consecutively throughout the document to aid in referencing them. The register number has no meaning to software.
reserved	Register bits marked <i>reserved</i> are reserved for future use. In most cases, reserved bits are set to 0; however, user software should not rely on the value of a reserved bit. To provide software compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
yy:xx	The range of register bits inclusive from xx to yy. For example, 31:15 means bits 15 through 31 in that register.
<b>Register Bit/Field Types</b>	This value in the register bit diagram indicates whether software running on the controller can change the value of the bit field.
RC	Software can read this field. The bit or field is cleared by hardware after reading the bit/field.
RO	Software can read this field. Always write the chip reset value.
R/W	Software can read or write this field.
R/W1C	Software can read or write this field. A write of a 0 to a W1C bit does not affect the bit value in the register. A write of a 1 clears the value of the bit in the register; the remaining bits remain unchanged.  This register type is primarily used for clearing interrupt status bits where the read operation provides the interrupt status and the write of the read value clears only the interrupts being reported at the time the register was read.
R/W1S	Software can read or write a 1 to this field. A write of a 0 to a R/W1S bit does not affect the bit value in the register.
W1C	Software can write this field. A write of a 0 to a W1C bit does not affect the bit value in the register. A write of a 1 clears the value of the bit in the register; the remaining bits remain unchanged. A read of the register returns no meaningful data.  This register is typically used to clear the corresponding bit in an interrupt register.
WO	Only a write by software is valid; a read of the register returns no meaningful data.
<b>Register Bit/Field Reset Value</b>	This value in the register bit diagram shows the bit/field value after any reset, unless noted.
0	Bit cleared to 0 on chip reset.
1	Bit set to 1 on chip reset.
-	Nondeterministic.
<b>Pin/Signal Notation</b>	
[ ]	Pin alternate function; a pin defaults to the signal without the brackets.
pin	Refers to the physical connection on the package.
signal	Refers to the electrical signal encoding of a pin.
assert a signal	Change the value of the signal from the logically False state to the logically True state. For active High signals, the asserted signal value is 1 (High); for active Low signals, the asserted signal value is 0 (Low). The active polarity (High or Low) is defined by the signal name (see <i>SIGNAL</i> and <i>SIGNAL</i> below).
deassert a signal	Change the value of the signal from the logically True state to the logically False state.
<i>SIGNAL</i>	Signal names are in uppercase and in the Courier font. An overbar on a signal name indicates that it is active Low. To assert <i>SIGNAL</i> is to drive it Low; to deassert <i>SIGNAL</i> is to drive it High.
<i>SIGNAL</i>	Signal names are in uppercase and in the Courier font. An active High signal has no overbar. To assert <i>SIGNAL</i> is to drive it High; to deassert <i>SIGNAL</i> is to drive it Low.
<b>Numbers</b>	
X	An uppercase X indicates any of several values is allowed, where X can be any legal pattern. For example, a binary value of 0X00 can be either 0100 or 0000, a hex value of 0xX is 0x0 or 0x1, and so on.

**Table 2. Documentation Conventions (continued)**

Notation	Meaning
0x	Hexadecimal numbers have a prefix of 0x. For example, 0x00FF is the hexadecimal number FF.  All other numbers within register tables are assumed to be binary. Within conceptual information, binary numbers are indicated with a b suffix, for example, 1011b, and decimal numbers are written without a prefix or suffix.

# 1 Architectural Overview

Texas Instruments is the industry leader in bringing 32-bit capabilities and the full benefits of ARM® Cortex-M3™-based microcontrollers to the broadest reach of the microcontroller market. For current users of 8- and 16-bit MCUs, Stellaris® with Cortex-M3 offers a direct path to the strongest ecosystem of development tools, software and knowledge in the industry. Designers who migrate to Stellaris® benefit from great tools, small code footprint and outstanding performance. Even more important, designers can enter the ARM ecosystem with full confidence in a compatible roadmap from \$1 to 1 GHz. For users of current 32-bit MCUs, the Stellaris® family offers the industry's first implementation of Cortex-M3 and the Thumb-2 instruction set. With blazingly-fast responsiveness, Thumb-2 technology combines both 16-bit and 32-bit instructions to deliver the best balance of code density and performance. Thumb-2 uses 26 percent less memory than pure 32-bit code to reduce system cost while delivering 25 percent better performance. The Texas Instruments Stellaris® family of microcontrollers—the first ARM® Cortex™-M3 based controllers—brings high-performance 32-bit computing to cost-sensitive embedded microcontroller applications. These pioneering parts deliver customers 32-bit performance at a cost equivalent to legacy 8- and 16-bit devices, all in a package with a small footprint.

The LM3S1811 microcontroller has the following features:

- ARM® Cortex™-M3 Processor Core
  - 50-MHz operation; 60 DMIPS performance
  - ARM Cortex SysTick Timer
  - Nested Vectored Interrupt Controller (NVIC)
- On-Chip Memory
  - 256 KB single-cycle Flash memory
  - 32 KB single-cycle SRAM
  - Internal ROM loaded with StellarisWare® software:
    - Stellaris® Peripheral Driver Library
    - Stellaris® Boot Loader
- External Peripheral Interface (EPI)
  - 8/16/32-bit dedicated parallel bus for external peripherals
  - Supports SDRAM, SRAM/Flash memory, FPGAs, CPLDs
- Advanced Serial Integration
  - Three UARTs with IrDA and ISO 7816 support (one UART with full modem controls)
  - Two I<sup>2</sup>C modules
  - Two Synchronous Serial Interface modules (SSI)

- System Integration
  - Direct Memory Access Controller (DMA)
  - System control and clocks including on-chip precision 16-MHz oscillator
  - Four 32-bit timers (up to eight 16-bit)
  - Eight Capture Compare PWM pins (CCP)
  - Lower-power battery-backed hibernation module
  - Real-Time Clock
  - Two Watchdog Timers
    - One timer runs off the main oscillator
    - One timer runs off the precision internal oscillator
  - Up to 67 GPIOs, depending on configuration
    - Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
    - Independently configurable to 2, 4 or 8 mA drive capability
    - Up to 4 GPIOs can have 18 mA drive capability
- Analog
  - 10-bit Analog-to-Digital Converter (ADC) with eight analog input channels and sample rate of one million samples/second
  - Two analog comparators
  - Eight digital comparators
  - On-chip voltage regulator
- JTAG and ARM Serial Wire Debug (SWD)
- 100-pin LQFP package
- Industrial (-40°C to 85°C) Temperature Range

The Stellaris<sup>®</sup> LM3S1000 microcontrollers are perfect for cost-effective embedded control applications.

The LM3S1811 microcontroller is targeted for industrial applications, including remote monitoring, electronic point-of-sale machines, test and measurement equipment, network appliances and switches, factory automation, HVAC and building control, gaming equipment, motion control, medical instrumentation, and fire and security.

For applications requiring extreme conservation of power, the LM3S1811 microcontroller features a battery-backed Hibernation module to efficiently power down the LM3S1811 to a low-power state during extended periods of inactivity. With a power-up/power-down sequencer, a continuous time counter (RTC), a pair of match registers, an APB interface to the system bus, and dedicated

non-volatile memory, the Hibernation module positions the LM3S1811 microcontroller perfectly for battery applications.

In addition, the LM3S1811 microcontroller offers the advantages of ARM's widely available development tools, System-on-Chip (SoC) infrastructure IP applications, and a large user community. Additionally, the microcontroller uses ARM's Thumb®-compatible Thumb-2 instruction set to reduce memory requirements and, thereby, cost. Finally, the LM3S1811 microcontroller is code-compatible to all members of the extensive Stellaris® family; providing flexibility to fit our customers' precise needs.

Texas Instruments offers a complete solution to get to market quickly, with evaluation and development boards, white papers and application notes, an easy-to-use peripheral driver library, and a strong support, sales, and distributor network. See "Ordering and Contact Information" on page 787 for ordering information for Stellaris® family devices.

## 1.1 Functional Overview

The following sections provide an overview of the features of the LM3S1811 microcontroller. The page number in parentheses indicates where that feature is discussed in detail. Ordering and support information can be found in "Ordering and Contact Information" on page 787.

### 1.1.1 ARM Cortex™-M3

The following sections provide an overview of the ARM Cortex™-M3 processor core and instruction set, the integrated System Timer (SysTick) and the Nested Vectored Interrupt Controller.

#### 1.1.1.1 Processor Core (see page 49)

All members of the Stellaris® product family, including the LM3S1811 microcontroller, are designed around an ARM Cortex™-M3 processor core. The ARM Cortex-M3 processor provides the core for a high-performance, low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- 32-bit ARM® Cortex™-M3 v7M architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- Thumb-2 mixed 16-/32-bit instruction set, delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices; typically in the range of a few kilobytes of memory for microcontroller-class applications
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system and memories
- Hardware division and fast multiplier

- Deterministic, high-performance interrupt handling for time-critical applications
- Memory protection unit (MPU) to provide a privileged mode for protected operating system functionality
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle Flash memory usage
- Ultra-low power consumption with integrated sleep mode
- 50-MHz operation
- 1.25 DMIPS/MHz

“ARM Cortex-M3 Processor Core” on page 49 provides an overview of the ARM core; the core is detailed in the *ARM® Cortex™-M3 Technical Reference Manual*.

#### 1.1.1.2 System Timer (SysTick) (see page 59)

ARM Cortex-M3 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer that fires at a programmable rate (for example, 100 Hz) and invokes a SysTick routine
- A high-speed alarm timer using the system clock
- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter
- A simple counter used to measure time to completion and time used
- An internal clock-source control based on missing/meeting durations. The COUNTFLAG field in the SysTick Control and Status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop

#### 1.1.1.3 Nested Vectored Interrupt Controller (NVIC) (see page 65)

The LM3S1811 controller includes the ARM Nested Vectored Interrupt Controller (NVIC). The NVIC and Cortex-M3 prioritize and handle all exceptions in Handler Mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the Interrupt Service Routine (ISR). The interrupt vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining, meaning that back-to-back interrupts can be performed without the overhead of state saving and restoration. Software can set eight priority levels on 7 exceptions (system handlers) and 37 interrupts.

- Deterministic, fast interrupt processing: always 12 cycles, or just 6 cycles with tail-chaining



- External non-maskable interrupt signal (NMI) available for immediate execution of NMI handler for safety critical applications
- Dynamically reprioritizable interrupts
- Exceptional interrupt handling via hardware implementation of required register manipulations

“Interrupts” on page 65 provides an overview of the NVIC controller and the interrupt map. Exceptions and interrupts are detailed in the *ARM® Cortex™-M3 Technical Reference Manual*.

## 1.1.2 On-Chip Memory

The following sections describe the on-chip memory modules.

### 1.1.2.1 SRAM (see page 198)

The LM3S1811 microcontroller provides 32 KB of single-cycle on-chip SRAM. The internal SRAM of the Stellaris® devices is located at offset 0x2000.0000 of the device memory map.

Because read-modify-write (RMW) operations are very time consuming, ARM has introduced *bit-banding* technology in the new Cortex-M3 processor. With a bit-band-enabled processor, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation.

Data can be transferred to and from the SRAM using the Micro Direct Memory Access Controller (μDMA).

### 1.1.2.2 Flash Memory (see page 198)

The LM3S1811 microcontroller provides 256 KB of single-cycle on-chip Flash memory. The Flash memory is organized as a set of 2-KB blocks that can be individually erased. Erasing a block causes the entire contents of the block to be reset to all 1s. These blocks are paired into a set of 2-KB blocks that can be individually protected. The blocks can be marked as read-only or execute-only, providing different levels of code protection. Read-only blocks cannot be erased or programmed, protecting the contents of those blocks from being modified. Execute-only blocks cannot be erased or programmed, and can only be read by the controller instruction fetch mechanism, protecting the contents of those blocks from being read by either the controller or by a debugger.

### 1.1.2.3 ROM (see page 751)

The LM3S1811 ROM is preprogrammed with the following software and programs:

- Stellaris® Peripheral Driver Library
- Stellaris® Boot Loader

The Stellaris® Peripheral Driver Library is a royalty-free software library for controlling on-chip peripherals with a boot-loader capability. The library performs both peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. In addition, the library is designed to take full advantage of the stellar interrupt performance of the ARM® Cortex™-M3 core. No special pragmas or custom assembly code prologue/epilogue functions are required. For applications that require in-field programmability, the royalty-free Stellaris® Boot Loader can act as an application loader and support in-field firmware updates.

### 1.1.3 External Peripheral Interface (see page 342)

The External Peripheral Interface (EPI) provides access to external devices using a parallel path. Unlike communications peripherals such as SSI, UART, and I<sup>2</sup>C, the EPI is designed to act like a bus to external peripherals and memory.

The EPI has the following features:

- 8/16/32-bit dedicated parallel bus for external peripherals and memory
- Memory interface supports contiguous memory access independent of data bus width, thus enabling code execution directly from SDRAM, SRAM and Flash memory
- Blocking and non-blocking reads
- Separates processor from timing details through use of an internal write FIFO
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Separate channels for read and write
  - Read channel request asserted by programmable levels on the internal non-blocking read FIFO (NBRFIFO)
  - Write channel request asserted by empty on the internal write FIFO (WFIFO)

The EPI supports three primary functional modes: Synchronous Dynamic Random Access Memory (SDRAM) mode, Traditional Host-Bus mode, and General-Purpose mode. The EPI module also provides custom GPIOs; however, unlike regular GPIOs, the EPI module uses a FIFO in the same way as a communication mechanism and is speed-controlled using clocking.

- Synchronous Dynamic Random Access Memory (SDRAM)
  - Supports x16 (single data rate) SDRAM at up to 50 MHz
  - Supports low-cost SDRAMs up to 64 MB (512 megabits)
  - Includes automatic refresh and access to all banks/rows
  - Includes a Sleep/Standby mode to keep contents active with minimal power draw
  - Multiplexed address/data interface for reduced pin count
- Host-bus
  - Traditional x8 and x16 MCU bus interface capabilities
  - Similar device compatibility options as PIC, ATmega, 8051, and others
  - Access to SRAM, NOR Flash memory, and other devices, with up to 1 MB of addressing in unmultiplexed mode and 256 MB in multiplexed mode
  - Support of both muxed and de-muxed address and data
  - Access to a range of devices supporting the non-address FIFO x8 and x16 interface variant, with support for external FIFO (XFIFO) EMPTY and FULL signals

- Speed controlled, with read and write data wait-state counters
- Chip select modes include ALE, CSn, Dual CSn and ALE with dual CSn
- Manual chip-enable (or use extra address pins)
- General Purpose
  - Wide parallel interfaces for fast communications with CPLDs and FPGAs
  - Data widths up to 32-bits
  - Data rates up to 150 MB/second
  - Optional “address” sizes from 4-bits to 16-bits
  - Optional clock output, read/write strobes, framing (with counter-based size), and clock-enable input
- General parallel GPIO
  - 1 to 32 bits, FIFOed with speed control
  - Useful for custom peripherals or for digital data acquisition and actuator controls

#### 1.1.4 Serial Communications Peripherals

The LM3S1811 controller supports both asynchronous and synchronous serial communications with:

- Three UARTs with IrDA and ISO 7816 support (one UART with full modem controls)
- Two I<sup>2</sup>C modules
- Two Synchronous Serial Interface Modules (SSI)

The following sections provide more detail on each of these communications functions.

##### 1.1.4.1 UART (see page 548)

A Universal Asynchronous Receiver/Transmitter (UART) is an integrated circuit used for RS-232C serial communications, containing a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

The LM3S1811 controller includes three fully programmable 16C550-type UARTs. Although the functionality is similar to a 16C550 UART, this UART design is not register compatible. The UART can generate individually masked interrupts from the Rx, Tx, modem status, and error conditions. The module generates a single combined interrupt when any of the interrupts are asserted and are unmasked.

The three UARTs have the following features:

- Programmable baud-rate generator allowing speeds up to 3.125 Mbps for regular speed (divide by 16) and 6.25 Mbps for high speed (divide by 8)
- Separate 16x8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading

- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- False-start bit detection
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation/detection
  - 1 or 2 stop bit generation
- IrDA serial-IR (SIR) encoder/decoder providing
  - Programmable use of IrDA Serial Infrared (SIR) or UART input/output
  - Support of IrDA SIR encoder/decoder functions for data rates up to 115.2 Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41-2.23  $\mu$ s) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power mode bit duration
- Support for communication with ISO 7816 smart cards
- Full modem handshake support (on UART1)
- LIN protocol support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

#### 1.1.4.2 I<sup>2</sup>C (see page 651)

The Inter-Integrated Circuit (I<sup>2</sup>C) bus provides bi-directional data transfer through a two-wire design (a serial data line SDA and a serial clock line SCL). The I<sup>2</sup>C bus interfaces to external I<sup>2</sup>C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on. The I<sup>2</sup>C bus may also be used for system testing and diagnostic purposes in product development and manufacture.

Each device on the I<sup>2</sup>C bus can be designated as either a master or a slave. Each I<sup>2</sup>C module supports both sending and receiving data as either a master or a slave and can operate simultaneously as both a master and a slave. Both the I<sup>2</sup>C master and slave can generate interrupts.

The LM3S1811 controller includes two I<sup>2</sup>C modules with the following features:

- Devices on the I<sup>2</sup>C bus can be designated as either a master or a slave
  - Supports both transmitting and receiving data as either a master or a slave
  - Supports simultaneous master and slave operation
- Four I<sup>2</sup>C modes
  - Master transmit
  - Master receive
  - Slave transmit
  - Slave receive
- Two transmission speeds: Standard (100 Kbps) and Fast (400 Kbps)
- Master and slave interrupt generation
  - Master generates interrupts when a transmit or receive operation completes (or aborts due to an error)
  - Slave generates interrupts when data has been transferred or requested by a master or when a START or STOP condition is detected
- Master with arbitration and clock synchronization, multimaster support, and 7-bit addressing mode

#### 1.1.4.3 SSI (see page 609)

Synchronous Serial Interface (SSI) is a four-wire bi-directional communications interface that converts data between parallel and serial. The SSI module performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data transmitted to a peripheral device. The SSI module can be configured as either a master or slave device. As a slave device, the SSI module can also be configured to disable its output, which allows a master device to be coupled with multiple slave devices. The TX and RX paths are buffered with separate internal FIFOs.

The SSI module also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the SSI module's input clock. Bit rates are generated based on the input clock and the maximum bit rate is determined by the connected peripheral.

The LM3S1811 controller includes two SSI modules with the following features:

- Programmable interface operation for Freescale SPI, MICROWIRE, or Texas Instruments synchronous serial interfaces
- Master or slave operation
- Programmable clock bit rate and prescaler

- Separate transmit and receive FIFOs, each 16 bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loopback test mode for diagnostic/debug testing
- Standard FIFO-based interrupts and End-of-Transmission interrupt
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains 4 entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when FIFO contains 4 entries

### 1.1.5 System Integration

The LM3S1811 controller provides a variety of standard system functions integrated into the device, including:

- Micro Direct Memory Access Controller ( $\mu$ DMA)
- System control and clocks including on-chip precision 16-MHz oscillator
- ARM Cortex SysTick Timer
- Four 32-bit timers (up to eight 16-bit)
- Eight Capture Compare PWM pins (CCP)
- Lower-power battery-backed hibernation module
- Real-Time Clock
- Two Watchdog Timers
- Up to 67 GPIOs, depending on configuration
  - Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
  - Independently configurable to 2, 4 or 8 mA drive capability
  - Up to 4 GPIOs can have 18 mA drive capability

The following sections provide more detail on each of these functions.

#### 1.1.5.1 Direct Memory Access (see page 230)

The LM3S1811 microcontroller includes a Direct Memory Access (DMA) controller, known as micro-DMA ( $\mu$ DMA). The  $\mu$ DMA controller provides a way to offload data transfer tasks from the Cortex-M3 processor, allowing for more efficient use of the processor and the available bus bandwidth. The  $\mu$ DMA controller can perform transfers between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically

perform transfers between peripherals and memory as the peripheral is ready to transfer more data. The  $\mu$ DMA controller provides the following features:

- ARM PrimeCell® 32-channel configurable  $\mu$ DMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of arbitrary transfers initiated from a single request
- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules: GP Timer, UART, ADC, EPI, SSI
  - Alternate channel assignments
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable bus arbitration scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Design optimizations for improved bus access performance between  $\mu$ DMA controller and the processor core
  - $\mu$ DMA controller access is subordinate to core access
  - RAM striping
  - Peripheral bus segmentation
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, half-word, word, or no increment
- Maskable peripheral requests
- Interrupt on transfer completion, with a separate interrupt per channel

#### 1.1.5.2 System Control and Clocks (see page 80)

System control determines the overall operation of the device. It provides information about the device, controls power-saving features, controls the clocking of the device and individual peripherals, and handles reset detection and reporting.

- Device identification information: version, part number, SRAM size, Flash memory size, and so on
- Power control
  - On-chip fixed Low Drop-Out (LDO) voltage regulator
  - Hibernation module handles the power-up/down 3.3 V sequencing and control for the core digital logic and analog circuits
  - Low-power options for microcontroller: Sleep and Deep-sleep modes with clock gating
  - Low-power options for on-chip modules: software controls shutdown of individual peripherals and memory
  - 3.3-V supply brown-out detection and reporting via interrupt or reset
- Multiple clock sources for microcontroller system clock
  - Precision Oscillator (PIOSC): on-chip resource providing a 16 MHz  $\pm 1\%$  frequency at room temperature
    - 16 MHz  $\pm 3\%$  across temperature
    - Can be recalibrated with 7-bit trim resolution
    - Software power down control for low power modes
  - Main Oscillator (MOSC): a frequency-accurate clock source by one of two means: an external single-ended clock source is connected to the OSC0 input pin, or an external crystal is connected across the OSC0 input and OSC1 output pins.
    - External oscillator used with or without on-chip PLL: select supported frequencies from 1 MHz to 16.384 MHz.
    - External crystal: from DC to maximum device speed
  - Internal 30-kHz Oscillator: on chip resource providing a 30 kHz  $\pm 50\%$  frequency, used during power-saving modes
  - Hibernation Module clock source: eliminates need for additional crystal for main clock source
    - 32.768-kHz external oscillator
    - 4.194304-MHz external crystal
- Flexible reset sources
  - Power-on reset (POR)
  - Reset pin assertion
  - Brown-out reset (BOR) detector alerts to system power drops
  - Software reset



- Watchdog timer reset
- MOSC failure

### 1.1.5.3 Four Programmable Timers (see page 410)

Programmable timers can be used to count or time external events that drive the Timer input pins. Each GPTM block provides two 16-bit timers/counters that can be configured to operate independently as timers or event counters, or configured to operate as one 32-bit timer or one 32-bit Real-Time Clock (RTC). Timers can also be used to trigger analog-to-digital (ADC) conversions.

The General-Purpose Timer Module (GPTM) contains four GPTM blocks with the following functional options:

- Count up or down
- 16- or 32-bit programmable one-shot timer
- 16- or 32-bit programmable periodic timer
- 16-bit general-purpose timer with an 8-bit prescaler
- 32-bit Real-Time Clock (RTC) when using an external 32.768-KHz clock as the input
- Eight Capture Compare PWM pins (CCP)
- Daisy chaining of timer modules to allow a single timer to initiate multiple timing events
- ADC event trigger
- User-enabled stalling when the controller asserts CPU Halt flag during debug (excluding RTC mode)
- 16-bit input-edge count- or time-capture modes
- 16-bit PWM mode with software-programmable output inversion of the PWM signal
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine.
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt

### 1.1.5.4 CCP Pins (see page 416)

Capture Compare PWM pins (CCP) can be used by the General-Purpose Timer Module to time/count external events using the CCP pin as an input. Alternatively, the GPTM can generate a simple PWM output on the CCP pin.

The LM3S1811 microcontroller includes eight Capture Compare PWM pins (CCP) that can be programmed to operate in the following modes:

- Capture: The GP Timer is incremented/decremented by programmed events on the CCP input. The GP Timer captures and stores the current timer value when a programmed event occurs.

- Compare: The GP Timer is incremented/decremented by programmed events on the CCP input. The GP Timer compares the current value with a stored value and generates an interrupt when a match occurs.
- PWM: The GP Timer is incremented/decremented by the system clock. A PWM signal is generated based on a match between the counter value and a value stored in a match register and is output on the CCP pin.

#### 1.1.5.5 Hibernation Module (see page 171)

The Hibernation module provides logic to switch power off to the main processor and peripherals and to wake on external or time-based events. The Hibernation module includes power-sequencing logic and has the following features:

- Two mechanisms for power control
  - System power control using discrete external regulator
  - On-chip power control using internal switches under register control
- Dedicated pin for waking using an external signal
- Low-battery detection, signaling, and interrupt generation
- 32-bit real-time counter (RTC)
  - Two 32-bit RTC match registers for timed wake-up and interrupt generation
  - RTC predivider trim for making fine adjustments to the clock rate
- Clock source from a 32.768-kHz external oscillator or a 4.194304-MHz crystal; source can be used for main controller clock
- 64 32-bit words of non-volatile memory to save state during hibernation
- Programmable interrupts for RTC match, external wake, and low battery events

#### 1.1.5.6 Watchdog Timers (see page 453)

A watchdog timer is used to regain control when a system has failed due to a software error or to the failure of an external device to respond in the expected way. The Stellaris<sup>®</sup> Watchdog Timer can generate a nonmaskable interrupt (NMI) or a reset when a time-out value is reached. In addition, the Watchdog Timer is ARM FIRM-compliant and can be configured to generate an interrupt to the controller on its first time-out, and to generate a reset signal on its second time-out. Once the Watchdog Timer has been configured, the lock register can be written to prevent the timer configuration from being inadvertently altered.

The LM3S1811 microcontroller has two Watchdog Timer modules: Watchdog Timer 0 uses the system clock for its timer clock; Watchdog Timer 1 uses the PIOSC as its timer clock. The Stellaris<sup>®</sup> Watchdog Timer module has the following features:

- 32-bit down counter with a programmable load register
- Separate watchdog clock with an enable
- Programmable interrupt generation logic with interrupt masking

- Lock register protection from runaway software
- Reset generation logic with an enable/disable
- User-enabled stalling when the microcontroller asserts the CPU Halt flag during debug

#### 1.1.5.7 Programmable GPIOs (see page 288)

General-purpose input/output (GPIO) pins offer flexibility for a variety of connections. The Stellaris® GPIO module is comprised of nine physical GPIO blocks, each corresponding to an individual GPIO port. The GPIO module is FiRM-compliant (compliant to the ARM Foundation IP for Real-Time Microcontrollers specification) and supports 0-67 programmable input/output pins. The number of GPIOs available depends on the peripherals being used (see “Signal Tables” on page 701 for the signals available to each GPIO pin).

- Up to 67 GPIOs, depending on configuration
- Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
- 5-V-tolerant input/outputs
- Fast toggle capable of a change every two clock cycles
- Two means of port access: either Advanced High-Performance Bus (AHB) with better back-to-back access performance, or the legacy Advanced Peripheral Bus (APB) for backwards-compatibility with existing code
- Programmable control for GPIO interrupts
  - Interrupt generation masking
  - Edge-triggered on rising, falling, or both
  - Level-sensitive on High or Low values
- Bit masking in both read and write operations through address lines
- Can be used to initiate an ADC sample sequence
- Pins configured as digital inputs are Schmitt-triggered
- Programmable control for GPIO pad configuration
  - Weak pull-up or pull-down resistors
  - 2-mA, 4-mA, and 8-mA pad drive for digital communication; up to four pads can be configured with an 18-mA pad drive for high-current applications
  - Slew rate control for the 8-mA drive
  - Open drain enables
  - Digital input enables

#### 1.1.6 Analog

The LM3S1811 controller provides analog functions integrated into the device, including:

- 10-bit Analog-to-Digital Converter (ADC) with eight analog input channels and sample rate of one million samples/second
- Two analog comparators
- Eight digital comparators
- On-chip voltage regulator

The following provides more detail on these analog functions.

#### 1.1.6.1 ADC (see page 478)

An analog-to-digital converter (ADC) is a peripheral that converts a continuous analog voltage to a discrete digital number. The Stellaris<sup>®</sup> ADC module features 10-bit conversion resolution and supports eight input channels plus an internal temperature sensor. Four buffered sample sequencers allow rapid sampling of up to eight analog input sources without controller intervention. Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. A digital comparator function is included that allows the conversion value to be diverted to a comparison unit that provides eight digital comparators.

with the following features:

- Eight analog input channels
- Single-ended and differential-input configurations
- On-chip internal temperature sensor
- Sample rate of one million samples/second
- Flexible, configurable analog-to-digital conversion
- Four programmable sample conversion sequencers from one to eight entries long, with corresponding conversion result FIFOs
- Flexible trigger control
  - Controller (software)
  - Timers
  - Analog Comparators
  - GPIO
- Hardware averaging of up to 64 samples for improved accuracy
- Digital comparison unit providing eight digital comparators
- Converter uses an internal 3-V reference
- Power and ground for the analog circuitry is separate from the digital power and ground
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Dedicated channel for each sample sequencer

- Burst request asserted when interrupt is triggered

### 1.1.6.2 Analog Comparators (see page 688)

An analog comparator is a peripheral that compares two analog voltages and provides a logical output that signals the comparison result. The LM3S1811 microcontroller provides two independent integrated analog comparators that can be configured to drive an output or generate an interrupt or ADC event.

The comparator can provide its output to a device pin, acting as a replacement for an analog comparator on the board, or it can be used to signal the application via interrupts or triggers to the ADC to cause it to start capturing a sample sequence. The interrupt generation and ADC triggering logic is separate. This means, for example, that an interrupt can be generated on a rising edge and the ADC triggered on a falling edge.

The LM3S1811 microcontroller provides two independent integrated analog comparators with the following functions:

- Compare external pin input to external pin input or to internal programmable voltage reference
- Compare a test voltage against any one of the following voltages:
  - An individual external reference voltage
  - A shared single external reference voltage
  - A shared internal reference voltage

### 1.1.7 JTAG and ARM Serial Wire Debug (see page 68)

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The TAP, Instruction Register (IR), and Data Registers (DR) can be used to test the interconnections of assembled printed circuit boards and obtain manufacturing information on the components. The JTAG Port also provides a means of accessing and controlling design-for-test features such as I/O pin observation and control, scan testing, and debugging. Texas Instruments replaces the ARM SW-DP and JTAG-DP with the ARM CoreSight™-compliant Serial Wire JTAG Debug Port (SWJ-DP) interface. The SWJ-DP interface combines the SWD and JTAG debug ports into one module providing all the normal JTAG debug and test functionality plus real-time access to system memory without halting the core or requiring any target resident code. See the *CoreSight™ Design Kit Technical Reference Manual* for details on SWJ-DP. The SWJ-DP interface has the following features:

- IEEE 1149.1-1990 compatible Test Access Port (TAP) controller
- Four-bit Instruction Register (IR) chain for storing JTAG instructions
- IEEE standard instructions: BYPASS, IDCODE, SAMPLE/PRELOAD, EXTEST and INTTEST
- ARM additional instructions: APACC, DPACC and ABORT
- Integrated ARM Serial Wire Debug (SWD)
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints

- Data Watchpoint and Trigger (DWT) unit for implementing watchpoints, trigger resources, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

### 1.1.8 Packaging and Temperature

- Industrial-range 100-pin RoHS-compliant LQFP package

## 1.2 Target Applications

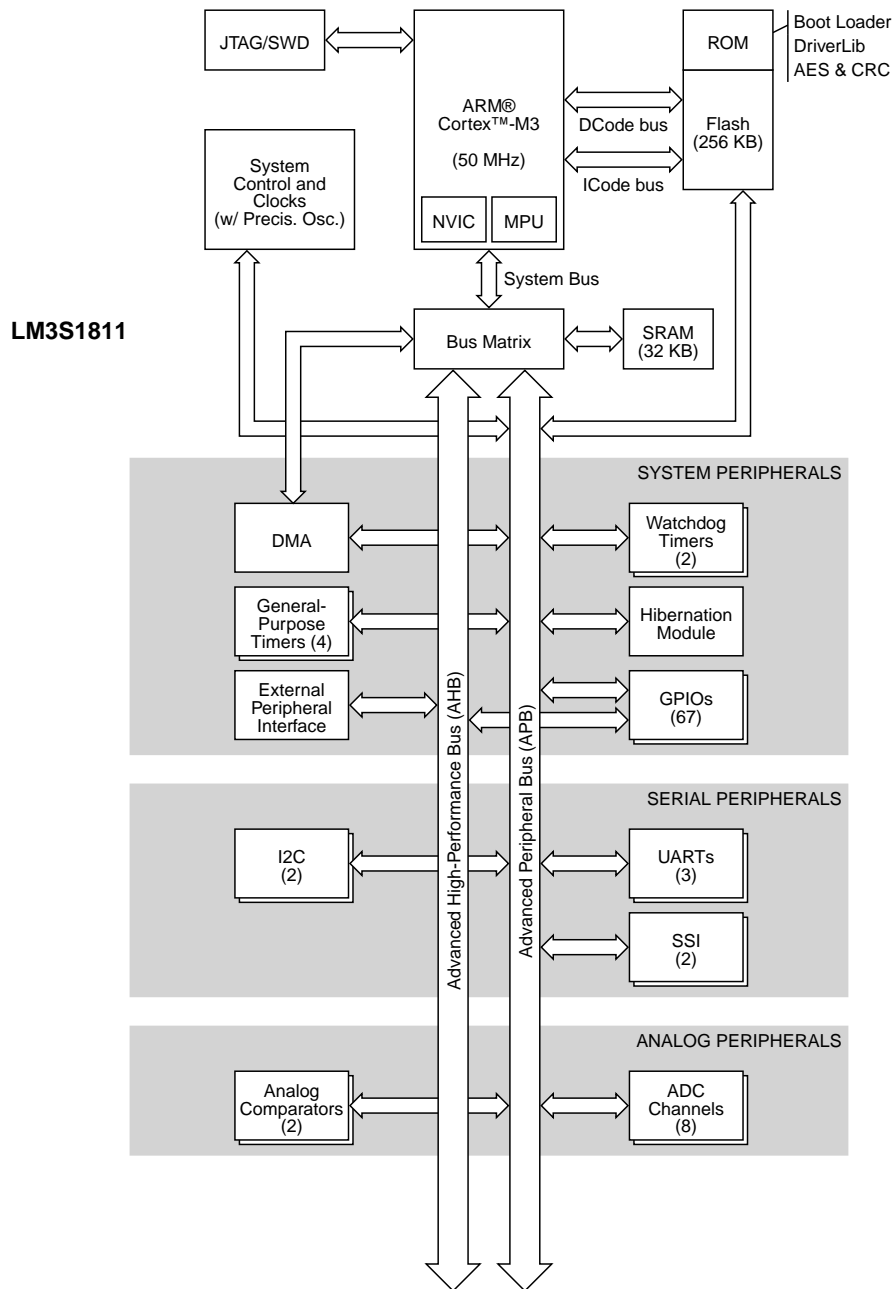
The Stellaris<sup>®</sup> family is positioned for cost-conscious applications requiring significant control processing and connectivity capabilities such as:

- Remote monitoring
- Electronic point-of-sale (POS) machines
- Test and measurement equipment
- Network appliances and switches
- Factory automation
- HVAC and building control
- Gaming equipment
- Motion control
- Medical instrumentation
- Fire and security
- Power and energy
- Transportation

## 1.3 High-Level Block Diagram

Figure 1-1 depicts the features on the Stellaris<sup>®</sup> LM3S1811 microcontroller. Note that there are two on-chip buses that connect the core to the peripherals. The Advanced Peripheral Bus (APB) bus is the legacy bus. The Advanced High-Performance Bus (AHB) bus provides better back-to-back access performance than the APB bus.

Figure 1-1. Stellaris® LM3S1811 Microcontroller High-Level Block Diagram



## 1.4 Additional Features

### 1.4.1 Memory Map (see page 62)

A memory map lists the location of instructions and data in memory. The memory map for the LM3S1811 controller can be found in “Memory Map” on page 62. Register addresses are given as a hexadecimal increment, relative to the module's base address as shown in the memory map. The *ARM® Cortex™-M3 Technical Reference Manual* provides further information on the memory map.

### 1.4.2 Hardware Details

Details on the pins and package can be found in the following sections:

- “Pin Diagram” on page 700
- “Signal Tables” on page 701
- “Operating Characteristics” on page 725
- “Electrical Characteristics” on page 726
- “Package Information” on page 789



## 2 ARM Cortex-M3 Processor Core

The ARM Cortex-M3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts. Features include:

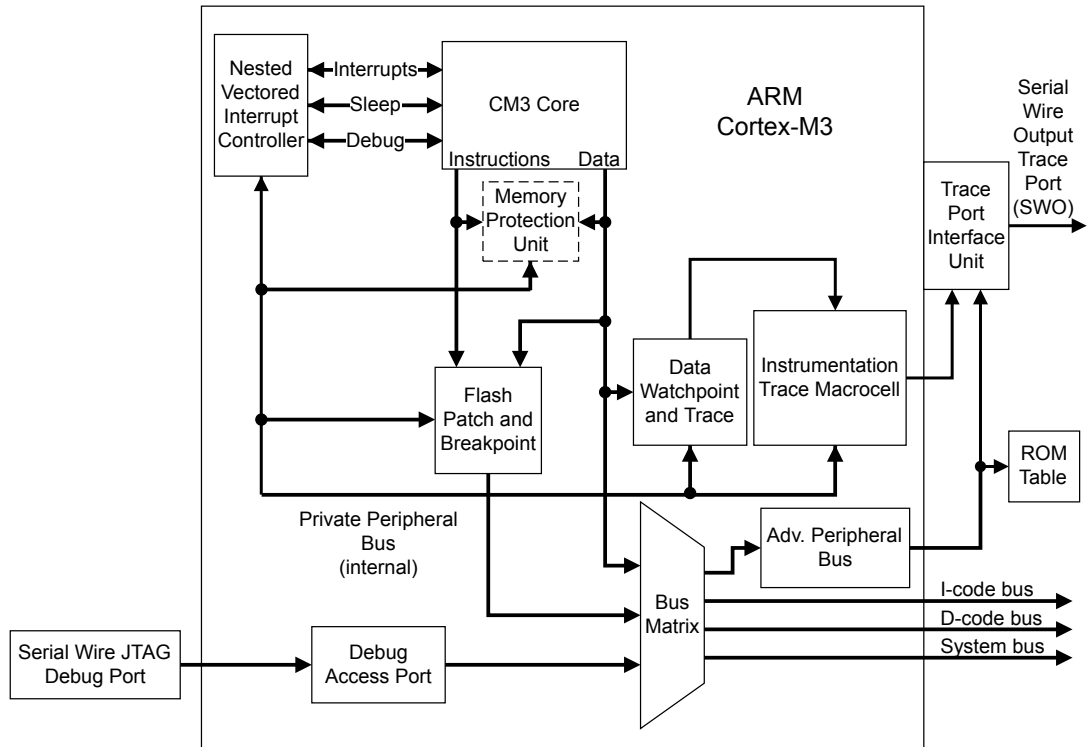
- 32-bit ARM® Cortex™-M3 v7M architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- Thumb-2 mixed 16-/32-bit instruction set, delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices; typically in the range of a few kilobytes of memory for microcontroller-class applications
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system and memories
- Hardware division and fast multiplier
- Deterministic, high-performance interrupt handling for time-critical applications
- Memory protection unit (MPU) to provide a privileged mode for protected operating system functionality
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle Flash memory usage
- Ultra-low power consumption with integrated sleep mode
- 50-MHz operation
- 1.25 DMIPS/MHz

The Stellaris® family of microcontrollers builds on this core to bring high-performance 32-bit computing to cost-sensitive embedded microcontroller applications, such as factory automation and control, industrial control power devices, building and home automation, and stepper motors.

For more information on the ARM Cortex-M3 processor core, see the *ARM® Cortex™-M3 Technical Reference Manual*. For information on SWJ-DP, see the *ARM® CoreSight Technical Reference Manual*.

## 2.1 Block Diagram

Figure 2-1. CPU Block Diagram



## 2.2 Functional Description

**Important:** The *ARM® Cortex™-M3 Technical Reference Manual* describes all the features of an ARM Cortex-M3 in detail. However, these features differ based on the implementation. This section describes the Stellaris® implementation.

Texas Instruments implements the ARM Cortex-M3 core as shown in Figure 2-1 on page 50. The Cortex-M3 uses the entire 16-bit Thumb instruction set and the base Thumb-2 32-bit instruction set. In addition, as noted in the *ARM® Cortex™-M3 Technical Reference Manual*, several Cortex-M3 components are flexible in their implementation: SW/JTAG-DP, ETM, TPIU, the ROM table, the MPU, and the Nested Vectored Interrupt Controller (NVIC). Each of these is addressed in the sections that follow.

### 2.2.1 Programming Model

This section provides a brief overview of the programming model for the Cortex-M3 core. More detailed information can be found in the *ARM® Cortex™-M3 Technical Reference Manual*.

- Privileged access and user access - Code can execute as privileged or unprivileged. Unprivileged execution limits or excludes access to some resources. Privileged execution has access to all resources. Handler mode is always privileged. Thread mode can be privileged or unprivileged.

Thread mode is privileged out of reset, but you can change it to user or unprivileged by setting the CONTROL[0] bit using the MSR instruction. User access prevents:

- Use of some instructions such as CPS to set FAULTMASK and PRIMASK
- Access to most registers in System Control Space (SCS)

When Thread mode has been changed from privileged to user, it cannot change itself back to privileged. Only a Handler can change the privilege of Thread mode. Handler mode is always privileged.

- Register set - The processor has the following 32-bit registers:
  - 13 general-purpose registers, r0-r12
  - Stack point alias of banked registers, SP\_process and SP\_main
  - Link register, r14
  - Program counter, r15
  - One program status register, xPSR.
- Data types - The processor supports the following data types:
  - 32-bit words
  - 16-bit halfwords
  - 8-bit bytes
- Memory formats - The processor views memory as a linear collection of bytes numbered in ascending order from 0. For example, bytes 0-3 hold the first stored word and bytes 4-7 hold the second stored word. The processor accesses code and data in little-endian format, which means that the byte with the lowest address in a word is the least-significant byte of the word. The byte with the highest address in a word is the most significant. The byte at address 0 of the memory system connects to data lines 7-0.
- Instruction set - The Cortex-M3 instruction set contains both 16 and 32-bit instructions. These instructions are summarized in Table 2-1 on page 51 and Table 2-2 on page 53, respectively.

**Table 2-1. 16-Bit Cortex-M3 Instruction Set Summary**

Operation	Assembler
Add register value and C flag to register value	ADC <Rd>, <Rm>
Add immediate 3-bit value to register	ADD <Rd>, <Rn>, #<immed_3>
Add immediate 8-bit value to register	ADD <Rd>, #<immed_8>
Add low register value to low register value	ADD <Rd>, <Rn>, <Rm>
Add high register value to low or high register value	ADD <Rd>, <Rm>
Add 4* (immediate 8-bit value) with PC to register	ADD <Rd>, PC, #<immed_8> * 4
Add 4* (immediate 8-bit value) with SP to register	ADD <Rd>, SP, #<immed_8> * 4
Add 4* (immediate 7-bit value) to SP	ADD SP, #<immed_7> * 4
Bitwise AND register values	AND <Rd>, <Rm>
Arithmetic shift right by immediate number	ASR <Rd>, <Rm>, #<immed_5>

Table 2-1. 16-Bit Cortex-M3 Instruction Set Summary (continued)

Operation	Assembler
Arithmetic shift right by number in register	ASR <Rd>, <Rs>
Branch conditional	B<cond> <target address>
Branch unconditional	B <target_address>
Bit clear	BIC <Rd>, <Rm>
Software breakpoint	BKPT <immed_8>
Branch with link	BL <Rm>
Branch with link and exchange	BLX <Rm>
Branch and exchange	BX <Rm>
Compare not zero and branch	CBNZ <Rn>, <label>
Compare zero and branch	CBZ <Rn>, <label>
Compare negation of register value with another register value	CMN <Rn>, <Rm>
Compare immediate 8-bit value	CMP <Rn>, #<immed_8>
Compare registers	CMP <Rn>, <Rm>
Compare high register to low or high register	CMP <Rn>, <Rm>
Change processor state	CPS <effect>, <iflags>
Copy high or low register value to another high or low register	CPY <Rd> <Rm>
Bitwise exclusive OR register values	EOR <Rd>, <Rm>
Condition the following instruction	IT <cond>
Condition the following two instructions	IT<x> <cond>
Condition the following three instructions	IT<x><y> <cond>
Condition the following four instructions	IT<x><y><z> <cond>
Multiple sequential memory word loads	LDmia <Rn>!, <registers>
Load memory word from base register address + 5-bit immediate offset	LDR <Rd>, [<Rn>, #<immed_5> * 4]
Load memory word from base register address + register offset	LDR <Rd>, [<Rn>, <Rm>]
Load memory word from PC address + 8-bit immediate offset	LDR <Rd>, [PC, #<immed_8> * 4]
Load memory word from SP address + 8-bit immediate offset	LDR, <Rd>, [SP, #<immed_8> * 4]
Load memory byte [7:0] from register address + 5-bit immediate offset	LDRB <Rd>, [<Rn>, #<immed_5>]
Load memory byte [7:0] from register address + register offset	LDRB <Rd>, [<Rn>, <Rm>]
Load memory halfword [15:0] from register address + 5-bit immediate offset	LDRH <Rd>, [<Rn>, #<immed_5> * 2]
Load halfword [15:0] from register address + register offset	LDRH <Rd>, [<Rn>, <Rm>]
Load signed byte [7:0] from register address + register offset	LDRSB <Rd>, [<Rn>, <Rm>]
Load signed halfword [15:0] from register address + register offset	LDRSH <Rd>, [<Rn>, <Rm>]
Logical shift left by immediate number	LSL <Rd>, <Rm>, #<immed_5>
Logical shift left by number in register	LSL <Rd>, <Rs>
Logical shift right by immediate number	LSR <Rd>, <Rm>, #<immed_5>
Logical shift right by number in register	LSR <Rd>, <Rs>
Move immediate 8-bit value to register	MOV <Rd>, #<immed_8>
Move low register value to low register	MOV <Rd>, <Rn>
Move high or low register value to high or low register	MOV <Rd>, <Rm>
Multiply register values	MUL <Rd>, <Rm>
Move complement of register value to register	MVN <Rd>, <Rm>
Negate register value and store in register	NEG <Rd>, <Rm>

Table 2-1. 16-Bit Cortex-M3 Instruction Set Summary (continued)

Operation	Assembler
No operation	NOP <c>
Bitwise logical OR register values	ORR <Rd>, <Rm>
Pop registers from stack	POP <registers>
Pop registers and PC from stack	POP <registers, PC>
Push registers onto stack	PUSH <registers>
Push LR and registers onto stack	PUSH <registers, LR>
Reverse bytes in word and copy to register	REV <Rd>, <Rn>
Reverse bytes in two halfwords and copy to register	REV16 <Rd>, <Rn>
Reverse bytes in low halfword [15:0], sign-extend, and copy to register	REVSH <Rd>, <Rn>
Rotate right by amount in register	ROR <Rd>, <Rs>
Subtract register value and C flag from register value	SBC <Rd>, <Rm>
Send event	SEV <c>
Store multiple register words to sequential memory locations	STMIA <Rn>!, <registers>
Store register word to register address + 5-bit immediate offset	STR <Rd>, [<Rn>, #<immed_5> * 4]
Store register word to register address	STR <Rd>, [<Rn>, <Rm>]
Store register word to SP address + 8-bit immediate offset	STR <Rd>, [SP, #<immed_8> * 4]
Store register byte [7:0] to register address + 5-bit immediate offset	STRB <Rd>, [<Rn>, #<immed_5>]
Store register byte [7:0] to register address	STRB <Rd>, [<Rn>, <Rm>]
Store register halfword [15:0] to register address + 5-bit immediate offset	STRH <Rd>, [<Rn>, #<immed_5> * 2]
Store register halfword [15:0] to register address + register offset	STRH <Rd>, [<Rn>, <Rm>]
Subtract immediate 3-bit value from register	SUB <Rd>, <Rn>, #<immed_3>
Subtract immediate 8-bit value from register value	SUB <Rd>, #<immed_8>
Subtract register values	SUB <Rd>, <Rn>, <Rm>
Subtract 4 (immediate 7-bit value) from SP	SUB SP, #<immed_7> * 4
Operating system service call with 8-bit immediate call code	SVC <immed_8>
Extract byte [7:0] from register, move to register, and sign-extend to 32 bits	SXTB <Rd>, <Rm>
Extract halfword [15:0] from register, move to register, and sign-extend to 32 bits	SXTH <Rd>, <Rm>
Test register value for set bits by ANDing it with another register value	TST <Rn>, <Rm>
Extract byte [7:0] from register, move to register, and zero-extend to 32 bits	UXTB <Rd>, <Rm>#10
Extract halfword [15:0] from register, move to register, and zero-extend to 32 bits	UXTH <Rd>, <Rm>
Wait for event	WFE <c>
Wait for interrupt	WFI <c>

Table 2-2. 32-Bit Cortex-M3 Instruction Set Summary

Operation	Assembler
Add register value, immediate 12-bit value, and C bit	ADC{S}.W <Rd>, <Rn>, #<modify_constant(immed_12>
Add register value, shifted register value, and C bit	ADC{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Add register value and immediate 12-bit value	ADD{S}.W <Rd>, <Rn>, #<modify_constant(immed_12>
Add register value and shifted register value	ADD{S}.W <Rd>, <Rm>{, <shift>}
Add register value and immediate 12-bit value	ADDW.W <Rd>, <Rn>, #<immed_12>
Bitwise AND register value with immediate 12-bit value	AND{S}.W <Rd>, <Rn>, #<modify_constant(immed_12>

Table 2-2. 32-Bit Cortex-M3 Instruction Set Summary (continued)

Operation	Assembler
Bitwise AND register value with shifted register value	AND{S}.W <Rd>, <Rn>, Rm>{, <shift>}
Arithmetic shift right by number in register	ASR{S}.W <Rd>, <Rn>, <Rm>
Conditional branch	B{cond}.W <label>
Clear bit field	BFC.W <Rd>, #<lsb>, #<width>
Insert bit field from one register value into another	BFI.W <Rd>, <Rn>, #<lsb>, #<width>
Bitwise AND register value with complement of immediate 12-bit value	BIC{S}.W <Rd>, <Rn>, #<modify_constant(immed_12)>
Bitwise AND register value with complement of shifted register value	BIC{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Branch with link	BL <label>
Branch with link (immediate)	BL<c> <label>
Unconditional branch	B.W <label>
Clear exclusive clears the local record of the executing processor that an address has had a request for an exclusive access.	CLREX <c>
Return number of leading zeros in register value	CLZ.W <Rd>, <Rn>
Compare register value with two's complement of immediate 12-bit value	CMN.W <Rn>, #<modify_constant(immed_12)>
Compare register value with two's complement of shifted register value	CMN.W <Rn>, <Rm>{, <shift>}
Compare register value with immediate 12-bit value	CMP.W <Rn>, #<modify_constant(immed_12)>
Compare register value with shifted register value	CMP.W <Rn>, <Rm>{, <shift>}
Data memory barrier	DMB <c>
Data synchronization barrier	DSB <c>
Exclusive OR register value with immediate 12-bit value	EOR{S}.W <Rd>, <Rn>, #<modify_constant(immed_12)>
Exclusive OR register value with shifted register value	EOR{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Instruction synchronization barrier	ISB <c>
Load multiple memory registers, increment after or decrement before	LDM{IA DB}.W <Rn>{!}, <registers>
Memory word from base register address + immediate 12-bit offset	LDR.W <Rxf>, [<Rn>, #<offset_12>]
Memory word to PC from register address + immediate 12-bit offset	LDR.W PC, [<Rn>, #<offset_12>]
Memory word to PC from base register address immediate 8-bit offset, postindexed	LDR.W PC, [Rn], #<+/-<offset_8>
Memory word from base register address immediate 8-bit offset, postindexed	LDR.W <Rxf>, [<Rn>], #<+/-<offset_8>
Memory word from base register address immediate 8-bit offset, preindexed	LDR.W <Rxf>, [<Rn>, #<+/-<offset_8>!] LDRT.W <Rxf>, [<Rn>, #<offset_8>]
Memory word to PC from base register address immediate 8-bit offset, preindexed	LDR.W PC, [<Rn>, #<+/-<offset_8>!]
Memory word from register address shifted left by 0, 1, 2, or 3 places	LDR.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Memory word to PC from register address shifted left by 0, 1, 2, or 3 places	LDR.W PC, [<Rn>, <Rm>{, LSL #<shift>}]
Memory word from PC address immediate 12-bit offset	LDR.W <Rxf>, [PC, #<+/-<offset_12>]
Memory word to PC from PC address immediate 12-bit offset	LDR.W PC, [PC, #<+/-<offset_12>]
Memory byte [7:0] from base register address + immediate 12-bit offset	LDRB.W <Rxf>, [<Rn>, #<offset_12>]
Memory byte [7:0] from base register address immediate 8-bit offset, postindexed	LDRB.W <Rxf>. [<Rn>], #<+/-<offset_8>
Memory byte [7:0] from register address shifted left by 0, 1, 2, or 3 places	LDRB.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Memory byte [7:0] from base register address immediate 8-bit offset, preindexed	LDRB.W <Rxf>, [<Rn>, #<+/-<offset_8>!]
Memory byte from PC address immediate 12-bit offset	LDRB.W <Rxf>, [PC, #<+/-<offset_12>]
Memory doubleword from register address 8-bit offset 4, preindexed	LDRD.W <Rxf>, <Rxf2>, [<Rn>, #<+/-<offset_8> * 4]{!}

Table 2-2. 32-Bit Cortex-M3 Instruction Set Summary (continued)

Operation	Assembler
Memory doubleword from register address 8-bit offset 4, postindexed	LDRD.W <Rxf>, <Rxf2>, [<Rn>], #+/-<offset_8> * 4
Load register exclusive calculates an address from a base register value and an immediate offset, loads a word from memory, writes it to a register	LDREX<c> <Rt>,[<Rn>{,<#<imm>}]
Load register exclusive halfword calculates an address from a base register value and an immediate offset, loads a halfword from memory, writes it to a register	LDREXH<c> <Rt>,[<Rn>{,<#<imm>}]
Load register exclusive byte calculates an address from a base register value and an immediate offset, loads a byte from memory, writes it to a register	LDREXB<c> <Rt>,[<Rn>{,<#<imm>}]
Memory halfword [15:0] from base register address + immediate 12-bit offset	LDRH.W <Rxf>, [<Rn>, #<offset_12>]
Memory halfword [15:0] from base register address immediate 8-bit offset, preindexed	LDRH.W <Rxf>, [<Rn>, #<+/-<offset_8>!]
Memory halfword [15:0] from base register address immediate 8-bit offset, postindexed	LDRH.W <Rxf>.[<Rn>], #+/-<offset_8>
Memory halfword [15:0] from register address shifted left by 0, 1, 2, or 3 places	LDRH.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Memory halfword from PC address immediate 12-bit offset	LDRH.W <Rxf>, [PC, #+/-<offset_12>]
Memory signed byte [7:0] from base register address + immediate 12-bit offset	LDRSB.W <Rxf>, [<Rn>, #<offset_12>]
Memory signed byte [7:0] from base register address immediate 8-bit offset, postindexed	LDRSB.W <Rxf>.[<Rn>], #+/-<offset_8>
Memory signed byte [7:0] from base register address immediate 8-bit offset, preindexed	LDRSB.W <Rxf>, [<Rn>, #<+/-<offset_8>!]
Memory signed byte [7:0] from register address shifted left by 0, 1, 2, or 3 places	LDRSB.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Memory signed byte from PC address immediate 12-bit offset	LDRSB.W <Rxf>, [PC, #+/-<offset_12>]
Memory signed halfword [15:0] from base register address + immediate 12-bit offset	LDRSH.W <Rxf>, [<Rn>, #<offset_12>]
Memory signed halfword [15:0] from base register address immediate 8-bit offset, postindexed	LDRSH.W <Rxf>.[<Rn>], #+/-<offset_8>
Memory signed halfword [15:0] from base register address immediate 8-bit offset, preindexed	LDRSH.W <Rxf>, [<Rn>, #<+/-<offset_8>!]
Memory signed halfword [15:0] from register address shifted left by 0, 1, 2, or 3 places	LDRSH.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Memory signed halfword from PC address immediate 12-bit offset	LDRSH.W <Rxf>, [PC, #+/-<offset_12>]
Logical shift left register value by number in register	LSL{S}.W <Rd>, <Rn>, <Rm>
Logical shift right register value by number in register	LSR{S}.W <Rd>, <Rn>, <Rm>
Multiply two signed or unsigned register values and add the low 32 bits to a register value	MLA.W <Rd>, <Rn>, <Rm>, <Racc>
Multiply two signed or unsigned register values and subtract the low 32 bits from a register value	MLS.W <Rd>, <Rn>, <Rm>, <Racc>
Move immediate 12-bit value to register	MOV{S}.W <Rd>, #<modify_constant(immed_12)>
Move shifted register value to register	MOV{S}.W <Rd>, <Rm>{, <shift>}
Move immediate 16-bit value to top halfword [31:16] of register	MOV.T.W <Rd>, #<immed_16>
Move immediate 16-bit value to bottom halfword [15:0] of register and clear top halfword [31:16]	MOV.W.W <Rd>, #<immed_16>
Move to register from status	MRS<c> <Rd>, <psr>
Move to status register	MSR<c> <psr>_<fields>,<Rn>
Multiply two signed or unsigned register values	MUL.W <Rd>, <Rn>, <Rm>
No operation	NOP.W

Table 2-2. 32-Bit Cortex-M3 Instruction Set Summary (continued)

Operation	Assembler
Logical OR NOT register value with immediate 12-bit value	ORN{S}.W <Rd>, <Rn>, #<modify_constant(immed_12)>
Logical OR NOT register value with shifted register value	ORN{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Logical OR register value with immediate 12-bit value	ORR{S}.W <Rd>, <Rn>, #<modify_constant(immed_12)>
Logical OR register value with shifted register value	ORR{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Reverse bit order	RBIT.W <Rd>, <Rm>
Reverse bytes in word	REV.W <Rd>, <Rm>
Reverse bytes in each halfword	REV16.W <Rd>, <Rn>
Reverse bytes in bottom halfword and sign-extend	REVSH.W <Rd>, <Rn>
Rotate right by number in register	ROR{S}.W <Rd>, <Rn>, <Rm>
Rotate right with extend	RRX{S}.W <Rd>, <Rm>
Subtract a register value from an immediate 12-bit value	RSB{S}.W <Rd>, <Rn>, #<modify_constant(immed_12)>
Subtract a register value from a shifted register value	RSB{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Subtract immediate 12-bit value and C bit from register value	SBC{S}.W <Rd>, <Rn>, #<modify_constant(immed_12)>
Subtract shifted register value and C bit from register value	SBC{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Copy selected bits to register and sign-extend	SBFX.W <Rd>, <Rn>, #<lsb>, #<width>
Signed divide	SDIV<c> <Rd>, <Rn>, <Rm>
Send event	SEV<c>
Multiply signed words and add signed-extended value to 2-register value	SMLAL.W <RdLo>, <RdHi>, <Rn>, <Rm>
Multiply two signed register values	SMULL.W <RdLo>, <RdHi>, <Rn>, <Rm>
Signed saturate	SSAT.W <c> <Rd>, #<imm>, <Rn>{, <shift>}
Multiple register words to consecutive memory locations	STM{IA DB}.W <Rn>{!}, <registers>
Register word to register address + immediate 12-bit offset	STR.W <Rxf>, [<Rn>, #<offset_12>]
Register word to register address immediate 8-bit offset, postindexed	STR.W <Rxf>, [<Rn>], #+/-<offset_8>
Register word to register address shifted by 0, 1, 2, or 3 places	STR.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Register word to register address immediate 8-bit offset, preindexed Store, preindexed	STR.W <Rxf>, [<Rn>, #+/-<offset_8>]{!} STRT.W <Rxf>, [<Rn>, #<offset_8>]
Register byte [7:0] to register address immediate 8-bit offset, preindexed	STRB{T}.W <Rxf>, [<Rn>, #+/-<offset_8>]{!}
Register byte [7:0] to register address + immediate 12-bit offset	STRB.W <Rxf>, [<Rn>, #<offset_12>]
Register byte [7:0] to register address immediate 8-bit offset, postindexed	STRB.W <Rxf>, [<Rn>], #+/-<offset_8>
Register byte [7:0] to register address shifted by 0, 1, 2, or 3 places	STRB.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Store doubleword, preindexed	STRD.W <Rxf>, <Rxf2>, [<Rn>, #+/-<offset_8> * 4]{!}
Store doubleword, postindexed	STRD.W <Rxf>, <Rxf2>, [<Rn>, #+/-<offset_8> * 4]
Store register exclusive calculates an address from a base register value and an immediate offset, and stores a word from a register to memory if the executing processor has exclusive access to the memory addressed.	STREX <c> <Rd>, <Rt>, [<Rn>{, #<imm>}]
Store register exclusive byte derives an address from a base register value, and stores a byte from a register to memory if the executing processor has exclusive access to the memory addressed	STREXB <c> <Rd>, <Rt>, [<Rn>]
Store register exclusive halfword derives an address from a base register value, and stores a halfword from a register to memory if the executing processor has exclusive access to the memory addressed.	STREXH <c> <Rd>, <Rt>, [<Rn>]
Register halfword [15:0] to register address + immediate 12-bit offset	STRH.W <Rxf>, [<Rn>, #<offset_12>]
Register halfword [15:0] to register address shifted by 0, 1, 2, or 3 places	STRH.W <Rxf>, [<Rn>, <Rm>{, LSL #<shift>}]
Register halfword [15:0] to register address immediate 8-bit offset, preindexed	STRH{T}.W <Rxf>, [<Rn>, #+/-<offset_8>]{!}



**Table 2-2. 32-Bit Cortex-M3 Instruction Set Summary (continued)**

Operation	Assembler
Register halfword [15:0] to register address immediate 8-bit offset, postindexed	STRH.W <Rxf>, [<Rn>], #+/-<offset_8>
Subtract immediate 12-bit value from register value	SUB{S}.W <Rd>, <Rn>, #<modify_constant(immed_12)>
Subtract shifted register value from register value	SUB{S}.W <Rd>, <Rn>, <Rm>{, <shift>}
Subtract immediate 12-bit value from register value	SUBW.W <Rd>, <Rn>, #<immed_12>
Sign extend byte to 32 bits	SXTB.W <Rd>, <Rm>{, <rotation>}
Sign extend halfword to 32 bits	SXTH.W <Rd>, <Rm>{, <rotation>}
Table branch byte	TBB [<Rn>, <Rm>]
Table branch halfword	TBH [<Rn>, <Rm>, LSL #1]
Exclusive OR register value with immediate 12-bit value	TEQ.W <Rn>, #<modify_constant(immed_12)>
Exclusive OR register value with shifted register value	TEQ.W <Rn>, <Rm>{, <shift>}
Logical AND register value with 12-bit immediate value	TST.W <Rn>, #<modify_constant(immed_12)>
Logical AND register value with shifted register value	TST.W <Rn>, <Rm>{, <shift>}
Copy bit field from register value to register and zero-extend to 32 bits	UBFX.W <Rd>, <Rn>, #<lsb>, #<width>
Unsigned divide	UDIV<c> <Rd>, <Rn>, <Rm>
Multiply two unsigned register values and add to a 2-register value	UMLAL.W <RdLo>, <RdHi>, <Rn>, <Rm>
Multiply two unsigned register values	UMULL.W <RdLo>, <RdHi>, <Rn>, <Rm>
Unsigned saturate	USAT <c> <Rd>, #<imm>, <Rn>{, <shift>}
Copy unsigned byte to register and zero-extend to 32 bits	UXTB.W <Rd>, <Rm>{, <rotation>}
Copy unsigned halfword to register and zero-extend to 32 bits	UXTH.W <Rd>, <Rm>{, <rotation>}
Wait for event	WFE.W
Wait for interrupt	WFI.W

## 2.2.2 Serial Wire and JTAG Debug

Texas Instruments replaces the ARM SW-DP and JTAG-DP with the ARM CoreSight™-compliant Serial Wire JTAG Debug Port (SWJ-DP) interface. As a result, Chapter 12, “Debug Port,” of the *ARM® Cortex™-M3 Technical Reference Manual* does not apply to Stellaris® devices.

The SWJ-DP interface combines the SWD and JTAG debug ports into one module. See the *CoreSight™ Design Kit Technical Reference Manual* for details on SWJ-DP.

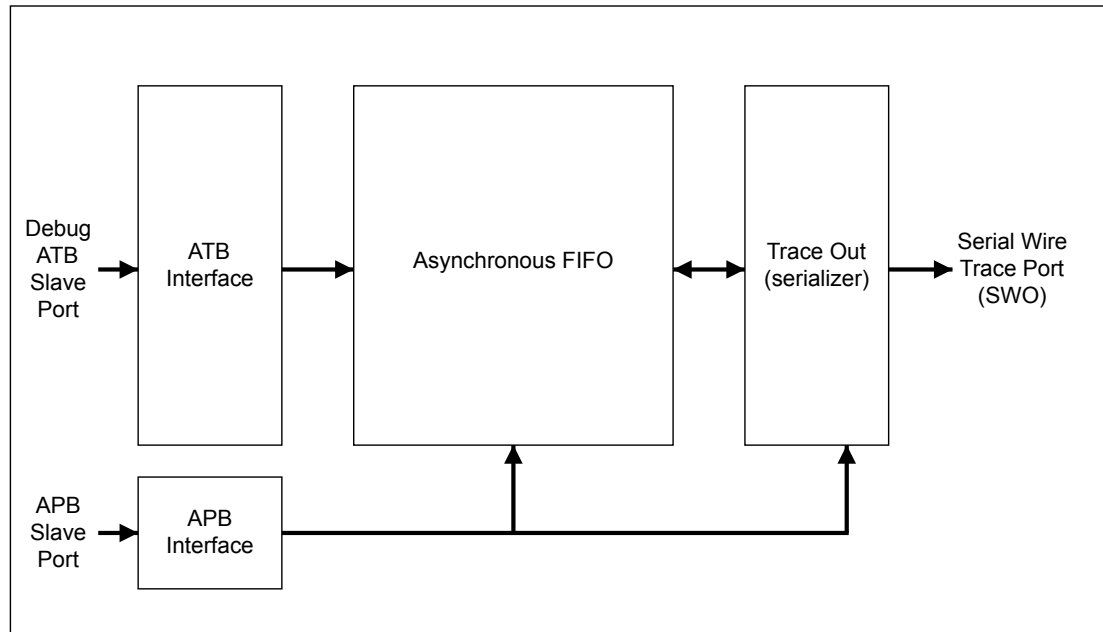
## 2.2.3 Embedded Trace Macrocell (ETM)

ETM is not implemented in the Stellaris® devices. As a result, Chapters 15 and 16 of the *ARM® Cortex™-M3 Technical Reference Manual* can be ignored.

## 2.2.4 Trace Port Interface Unit (TPIU)

The TPIU acts as a bridge between the Cortex-M3 trace data from the ITM, and an off-chip Trace Port Analyzer. Stellaris® devices implement the TPIU as shown in Figure 2-2. This implementation is similar to the non-ETM version described in the *ARM® Cortex™-M3 Technical Reference Manual*, however, SWJ-DP only provides the Serial Wire Viewer (SWV) output format for the TPIU.

Figure 2-2. TPIU Block Diagram



### 2.2.5 ROM Table

The default ROM table is implemented as described in the *ARM® Cortex™-M3 Technical Reference Manual*.

### 2.2.6 Memory Protection Unit (MPU)

The Memory Protection Unit (MPU) is included on the LM3S1811 controller and supports the standard ARMv7 Protected Memory System Architecture (PMSA) model. The MPU provides full support for protection regions, overlapping protection regions, access permissions, and exporting memory attributes to the system.

### 2.2.7 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC):

- Facilitates low-latency exception and interrupt handling
- Controls power management
- Implements system control registers

The NVIC and the processor core interface are closely coupled, which enables low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked (nested) interrupts to enable tail-chaining of interrupts.

You can only fully access the NVIC from privileged mode, but you can pend interrupts in user-mode by enabling the Configuration Control Register (see the *ARM® Cortex™-M3 Technical Reference Manual*). Any other user-mode access causes a bus fault.

All NVIC registers are accessible using byte, halfword, and word unless otherwise stated.

### 2.2.7.1 Interrupts

The *ARM® Cortex™-M3 Technical Reference Manual* describes the maximum number of interrupts and interrupt priorities. The LM3S1811 microcontroller supports 37 interrupts with eight priority levels.

In addition to the peripheral interrupts, the system also provides for a non-maskable interrupt (NMI). The NMI is generally used in safety critical applications where the immediate execution of an interrupt handler is required. The NMI signal is available as an external signal so that it may be generated by external circuitry. The NMI is also used internally as part of the main oscillator verification circuitry. More information on the non-maskable interrupt is located in “Non-Maskable Interrupt” on page 84.

### 2.2.8 System Timer (SysTick)

Cortex-M3 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer which fires at a programmable rate (for example, 100 Hz) and invokes a SysTick routine
- A high-speed alarm timer using the system clock
- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter.
- A simple counter used to measure time to completion and time used
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

#### 2.2.8.1 Functional Description

The timer consists of three registers:

- SysTick Control and Status Register - a control and status counter to configure its clock, enable the counter, enable the SysTick interrupt, and determine counter status
- SysTick Reload Value Register - the reload value for the counter, used to provide the counter's wrap value
- SysTick Current Value Register - the current value of the counter

A fourth register, the SysTick Calibration Value Register, is not implemented in the Stellaris® devices.

When enabled, the timer counts down on each clock from the reload value to zero, reloads (wraps) to the value in the SysTick Reload Value register on the next clock edge, then decrements on subsequent clocks. Clearing the SysTick Reload Value register disables the counter on the next wrap. When the counter reaches zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

Writing to the SysTick Current Value register clears the register and the COUNTFLAG status bit. The write does not trigger the SysTick exception logic. On a read, the current value is the value of the register at the time the register is accessed.

If the core is in debug state (halted), the counter does not decrement. The timer is clocked with respect to a reference clock, which can be either the core clock or an external clock source.

### 2.2.8.2 SysTick Control and Status Register

Use the SysTick Control and Status Register to enable the SysTick features. The reset is 0x0000.0000.

Bit/Field	Name	Type	Reset	Description
31:17	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	COUNTFLAG	R/W	0	Count Flag When set, this bit indicates that the timer has counted to 0 since the last time this register was read. This bit is cleared by a read of the register. If read by the debugger using the DAP, this bit is cleared only if the MasterType bit in the AHB-AP Control Register is clear. Otherwise, the COUNTFLAG bit is not changed by the debugger read.
15:3	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	CLKSOURCE	R/W	0	Clock Source  Value Description 0 External reference clock. (Not implemented for Stellaris® microcontrollers.) 1 Core clock  Because an external reference clock is not supported, this bit must be set in order for SysTick to operate.
1	TICKINT	R/W	0	Tick Interrupt When set, this bit causes an interrupt to be generated to the NVIC when SysTick counts to 0. When clear, interrupt generation is disabled. Software can use the COUNTFLAG to determine if the counter has ever reached 0.
0	ENABLE	R/W	0	Enable When set, this bit enables SysTick to operate in a multi-shot way. That is, the counter loads the Reload value and begins counting down. On reaching 0, the COUNTFLAG bit is set and an interrupt is generated if enabled by TICKINT. The counter then loads the Reload value again and begins counting. When this bit is clear, the counter is disabled.

### 2.2.8.3 SysTick Reload Value Register

The SysTick Reload Value Register specifies the start value to load into the SysTick Current Value Register when the counter reaches 0. The start value can be between 1 and 0x00FF.FFFF. A start value of 0 is possible but has no effect because the SysTick interrupt and COUNTFLAG are activated when counting from 1 to 0.

SysTick can be configured as a multi-shot timer, repeated over and over, firing every N+1 clock pulses, where N is any value from 1 to 0x00FF.FFFF. For example, if a tick interrupt is required every 100 clock pulses, 99 must be written into the RELOAD field.

When configuring SysTick as a single-shot timer, a new value is written on each tick interrupt, and the actual count down value must be written. For example, if a tick is next required after 400 clock pulses, 400 must be written into the RELOAD field.

Bit/Field	Name	Type	Reset	Description
31:24	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
23:0	RELOAD	R/W	-	Reload Value Value to load into the SysTick Current Value Register when the counter reaches 0.

#### 2.2.8.4 SysTick Current Value Register

The SysTick Current Value Register contains the current value of the counter.

Bit/Field	Name	Type	Reset	Description
31:24	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
23:0	CURRENT	W1C	-	Current Value This field contains the current value at the time the register is accessed. No read-modify-write protection is provided, so change with care. This register is write-clear. Writing to it with any value clears the register to 0. Clearing this register also clears the COUNTFLAG bit of the SysTick Control and Status Register.

#### 2.2.8.5 SysTick Calibration Value Register

The SysTick Calibration Value register is not implemented.

### 3 Memory Map

The memory map for the LM3S1811 controller is provided in Table 3-1.

In this manual, register addresses are given as a hexadecimal increment, relative to the module's base address as shown in the memory map. See also Chapter 4, "Memory Map" in the *ARM® Cortex™-M3 Technical Reference Manual*.

Note that within the memory map, all reserved space returns a bus fault when read or written.

**Table 3-1. Memory Map**

Start	End	Description	For details, see page ...
<b>Memory</b>			
0x0000.0000	0x0003.FFFF	On-chip Flash	198
0x0004.0000	0x00FF.FFFF	Reserved	-
0x0100.0000	0x1FFF.FFFF	Reserved for ROM	198
0x2000.0000	0x2000.7FFF	Bit-banded on-chip SRAM	198
0x2000.8000	0x21FF.FFFF	Reserved	-
0x2200.0000	0x220F.FFFF	Bit-band alias of 0x2000.0000 through 0x200F.FFFF	198
0x2210.0000	0x3FFF.FFFF	Reserved	-
<b>FIRM Peripherals</b>			
0x4000.0000	0x4000.0FFF	Watchdog timer 0	456
0x4000.1000	0x4000.1FFF	Watchdog timer 1	456
0x4000.2000	0x4000.3FFF	Reserved	-
0x4000.4000	0x4000.4FFF	GPIO Port A	299
0x4000.5000	0x4000.5FFF	GPIO Port B	299
0x4000.6000	0x4000.6FFF	GPIO Port C	299
0x4000.7000	0x4000.7FFF	GPIO Port D	299
0x4000.8000	0x4000.8FFF	SSI0	623
0x4000.9000	0x4000.9FFF	SSI1	623
0x4000.A000	0x4000.BFFF	Reserved	-
0x4000.C000	0x4000.CFFF	UART0	560
0x4000.D000	0x4000.DFFF	UART1	560
0x4000.E000	0x4000.EFFF	UART2	560
0x4000.F000	0x4001.FFFF	Reserved	-
<b>Peripherals</b>			
0x4002.0000	0x4002.07FF	I <sup>2</sup> C Master 0	666
0x4002.0800	0x4002.0FFF	I <sup>2</sup> C Slave 0	679
0x4002.1000	0x4002.17FF	I <sup>2</sup> C Master 1	666
0x4002.1800	0x4002.1FFF	I <sup>2</sup> C Slave 1	679
0x4002.2000	0x4002.3FFF	Reserved	-
0x4002.4000	0x4002.4FFF	GPIO Port E	299
0x4002.5000	0x4002.5FFF	GPIO Port F	299
0x4002.6000	0x4002.6FFF	GPIO Port G	299
0x4002.7000	0x4002.7FFF	GPIO Port H	299

Table 3-1. Memory Map (continued)

Start	End	Description	For details, see page ...
0x4002.8000	0x4002.FFFF	Reserved	-
0x4003.0000	0x4003.0FFF	Timer 0	424
0x4003.1000	0x4003.1FFF	Timer 1	424
0x4003.2000	0x4003.2FFF	Timer 2	424
0x4003.3000	0x4003.3FFF	Timer 3	424
0x4003.4000	0x4003.7FFF	Reserved	-
0x4003.8000	0x4003.8FFF	ADC0	494
0x4003.9000	0x4003.BFFF	Reserved	-
0x4003.C000	0x4003.CFFF	Analog Comparators	688
0x4003.D000	0x4003.DFFF	GPIO Port J	299
0x4003.E000	0x4005.7FFF	Reserved	-
0x4005.8000	0x4005.8FFF	GPIO Port A (AHB aperture)	299
0x4005.9000	0x4005.9FFF	GPIO Port B (AHB aperture)	299
0x4005.A000	0x4005.AFFF	GPIO Port C (AHB aperture)	299
0x4005.B000	0x4005.BFFF	GPIO Port D (AHB aperture)	299
0x4005.C000	0x4005.CFFF	GPIO Port E (AHB aperture)	299
0x4005.D000	0x4005.DFFF	GPIO Port F (AHB aperture)	299
0x4005.E000	0x4005.EFFF	GPIO Port G (AHB aperture)	299
0x4005.F000	0x4005.FFFF	GPIO Port H (AHB aperture)	299
0x4006.0000	0x4006.0FFF	GPIO Port J (AHB aperture)	299
0x4006.1000	0x400C.FFFF	Reserved	-
0x400D.0000	0x400D.FFFF	EPI0	369
0x400E.0000	0x400F.BFFF	Reserved	-
0x400F.C000	0x400F.CFFF	Hibernation Module	180
0x400F.D000	0x400F.DFFF	Flash memory control	203
0x400F.E000	0x400F.EFFF	System control	95
0x400F.F000	0x400F.FFFF	μDMA	251
0x4010.0000	0x41FF.FFFF	Reserved	-
0x4200.0000	0x43FF.FFFF	Bit-banded alias of 0x4000.0000 through 0x400F.FFFF	-
0x4400.0000	0x5FFF.FFFF	Reserved	-
0x6000.0000	0xCFFF.FFFF	EPI0 mapped peripheral and RAM	-
0xD000.0000	0xDFFF.FFFF	Reserved	-
<b>Private Peripheral Bus</b>			
0xE000.0000	0xE000.0FFF	Instrumentation Trace Macrocell (ITM)	ARM® Cortex™-M3 Technical Reference Manual
0xE000.1000	0xE000.1FFF	Data Watchpoint and Trace (DWT)	ARM® Cortex™-M3 Technical Reference Manual

Table 3-1. Memory Map (continued)

Start	End	Description	For details, see page ...
0xE000.2000	0xE000.2FFF	Flash Patch and Breakpoint (FPB)	ARM® Cortex™-M3 Technical Reference Manual
0xE000.3000	0xE000.DFFF	Reserved	-
0xE000.E000	0xE000.EFFF	Nested Vectored Interrupt Controller (NVIC)	ARM® Cortex™-M3 Technical Reference Manual
0xE000.F000	0xE003.FFFF	Reserved	-
0xE004.0000	0xE004.0FFF	Trace Port Interface Unit (TPIU)	ARM® Cortex™-M3 Technical Reference Manual
0xE004.1000	0xFFFF.FFFF	Reserved	-



## 4 Interrupts

The ARM Cortex-M3 processor and the Nested Vectored Interrupt Controller (NVIC) prioritize and handle all exceptions in Handler Mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the Interrupt Service Routine (ISR). The vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining, which enables back-to-back interrupts to be performed without the overhead of state saving and restoration.

Table 4-1 on page 65 lists all exception types. Software can set eight priority levels on seven of these exceptions (system handlers) as well as on 37 interrupts (listed in Table 4-2 on page 66).

Priorities on the system handlers are set with the NVIC System Handler Priority registers. Interrupts are enabled through the NVIC Interrupt Set Enable register and prioritized with the NVIC Interrupt Priority registers. Priorities can be grouped by splitting priority levels into pre-emption priorities and subpriorities. All of the interrupt registers are described in Chapter 8, “Nested Vectored Interrupt Controller” in the *ARM® Cortex™-M3 Technical Reference Manual*.

Internally, the highest user-programmable priority (0) is treated as fourth priority, after a Reset, Non-Maskable Interrupt (NMI), and a Hard Fault, in that order. Note that 0 is the default priority for all the programmable priorities.

If you assign the same priority level to two or more interrupts, their hardware priority (the lower position number) determines the order in which the processor activates them. For example, if both GPIO Port A and GPIO Port B are priority level 1, then GPIO Port A has higher priority.

---

**Important:** It may take several processor cycles after a write to clear an interrupt source for the NVIC to see the interrupt source de-assert. Thus if the interrupt clear is done as the last action in an interrupt handler, it is possible for the interrupt handler to complete while the NVIC sees the interrupt as still asserted, causing the interrupt handler to be re-entered errantly. This situation can be avoided by either clearing the interrupt source at the beginning of the interrupt handler or by performing a read or write after the write to clear the interrupt source (and flush the write buffer).

---

See Chapter 5, “Exceptions” and Chapter 8, “Nested Vectored Interrupt Controller” in the *ARM® Cortex™-M3 Technical Reference Manual* for more information on exceptions and interrupts.

**Table 4-1. Exception Types**

Exception Type	Vector Number	Priority <sup>a</sup>	Description
-	0	-	Stack top is loaded from the first entry of the vector table on reset.
Reset	1	-3 (highest)	This exception is invoked on power up and warm reset. On the first instruction, Reset drops to the lowest priority (and then is called the base level of activation). This exception is asynchronous.
Non-Maskable Interrupt (NMI)	2	-2	This exception is caused by the assertion of the NMI signal or by using the NVIC Interrupt Control State register and cannot be stopped or preempted by any exception but Reset. This exception is asynchronous.
Hard Fault	3	-1	This exception is caused by all classes of Fault, when the fault cannot activate due to priority or the configurable fault handler has been disabled. This exception is synchronous.
Memory Management	4	programmable	This exception is caused by an MPU mismatch, including access violation and no match. This exception is synchronous.

**Table 4-1. Exception Types (continued)**

Exception Type	Vector Number	Priority <sup>a</sup>	Description
Bus Fault	5	programmable	This exception is caused by a pre-fetch fault, memory access fault, and other address/memory related faults. This exception is synchronous when precise and asynchronous when imprecise.  This fault can be enabled or disabled.
Usage Fault	6	programmable	This exception is caused by a usage fault, such as undefined instruction executed or illegal state transition attempt. This exception is synchronous.
-	7-10	-	Reserved.
SVCcall	11	programmable	This exception is caused by a system service call with an SVC instruction. This exception is synchronous.
Debug Monitor	12	programmable	This exception is caused by the debug monitor (when not halting). This exception is synchronous, but only active when enabled. This exception does not activate if it is a lower priority than the current activation.
-	13	-	Reserved.
PendSV	14	programmable	This exception is caused by a penable request for system service. This exception is asynchronous and only pended by software.
SysTick	15	programmable	This exception is caused by the SysTick timer reaching 0, when it is enabled to generate an interrupt. This exception is asynchronous.
Interrupts	16 and above	programmable	This exception is caused by interrupts asserted from outside the ARM Cortex-M3 core and fed through the NVIC (prioritized). These exceptions are all asynchronous. Table 4-2 on page 66 lists the interrupts on the LM3S1811 controller.

a. 0 is the default priority for all the programmable priorities.

**Table 4-2. Interrupts**

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Description
0-15	-	Processor exceptions
16	0	GPIO Port A
17	1	GPIO Port B
18	2	GPIO Port C
19	3	GPIO Port D
20	4	GPIO Port E
21	5	UART0
22	6	UART1
23	7	SSI0
24	8	I <sup>2</sup> C0
25-29	9-13	Reserved
30	14	ADC0 Sequence 0
31	15	ADC0 Sequence 1
32	16	ADC0 Sequence 2
33	17	ADC0 Sequence 3
34	18	Watchdog Timers 0 and 1
35	19	Timer 0A
36	20	Timer 0B

Table 4-2. Interrupts (continued)

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Description
37	21	Timer 1A
38	22	Timer 1B
39	23	Timer 2A
40	24	Timer 2B
41	25	Analog Comparator 0
42	26	Analog Comparator 1
43	27	Reserved
44	28	System Control
45	29	Flash Memory Control
46	30	GPIO Port F
47	31	GPIO Port G
48	32	GPIO Port H
49	33	UART2
50	34	SSI1
51	35	Timer 3A
52	36	Timer 3B
53	37	I <sup>2</sup> C1
54-58	38-42	Reserved
59	43	Hibernation Module
60-61	44-45	Reserved
62	46	μDMA Software
63	47	μDMA Error
64-68	48-52	Reserved
69	53	EPI
70	54	GPIO Port J
71	55	Reserved

## 5 JTAG Interface

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The TAP, Instruction Register (IR), and Data Registers (DR) can be used to test the interconnections of assembled printed circuit boards and obtain manufacturing information on the components. The JTAG Port also provides a means of accessing and controlling design-for-test features such as I/O pin observation and control, scan testing, and debugging.

The JTAG port is comprised of four pins: TCK, TMS, TDI, and TDO. Data is transmitted serially into the controller on TDI and out of the controller on TDO. The interpretation of this data is dependent on the current state of the TAP controller. For detailed information on the operation of the JTAG port and TAP controller, please refer to the *IEEE Standard 1149.1-Test Access Port and Boundary-Scan Architecture*.

The Stellaris<sup>®</sup> JTAG controller works with the ARM JTAG controller built into the Cortex-M3 core by multiplexing the TDO outputs from both JTAG controllers. ARM JTAG instructions select the ARM TDO output while Stellaris<sup>®</sup> JTAG instructions select the Stellaris<sup>®</sup> TDO output. The multiplexer is controlled by the Stellaris<sup>®</sup> JTAG controller, which has comprehensive programming for the ARM, Stellaris<sup>®</sup>, and unimplemented JTAG instructions.

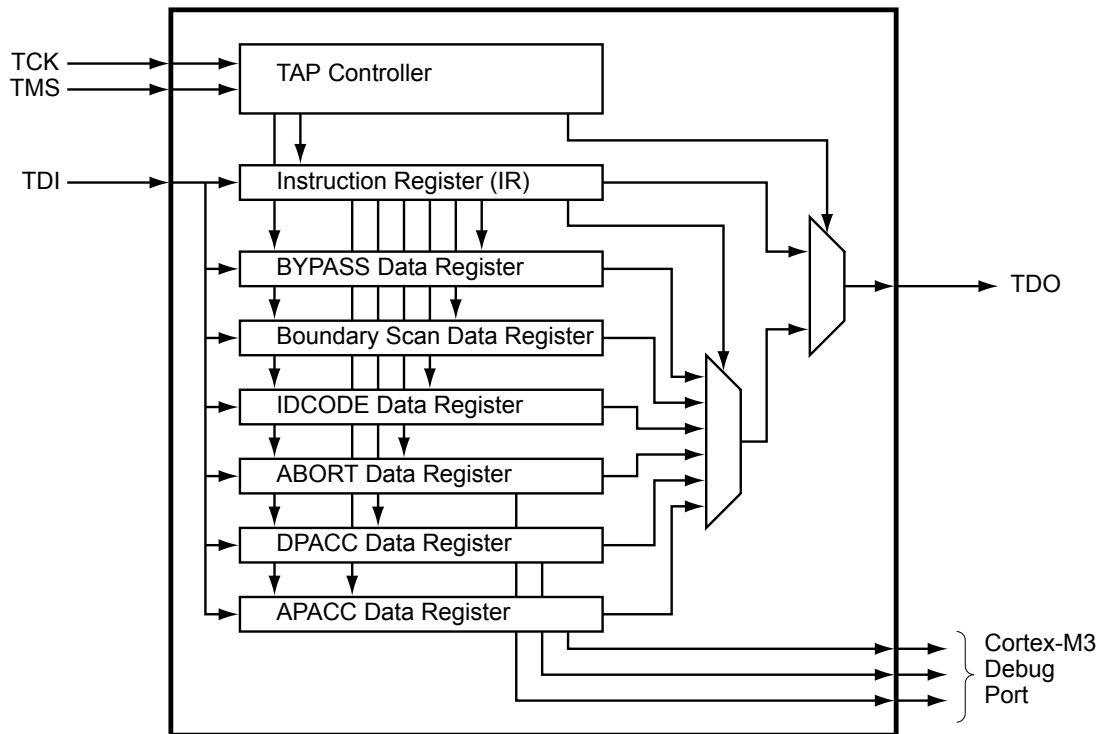
The Stellaris<sup>®</sup> JTAG module has the following features:

- IEEE 1149.1-1990 compatible Test Access Port (TAP) controller
- Four-bit Instruction Register (IR) chain for storing JTAG instructions
- IEEE standard instructions: BYPASS, IDCODE, SAMPLE/PRELOAD, EXTEST and INTTEST
- ARM additional instructions: APACC, DPACC and ABORT
- Integrated ARM Serial Wire Debug (SWD)
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trigger (DWT) unit for implementing watchpoints, trigger resources, and system profiling
  - Instrumentation Trace Macrocell (ITM) for support of printf style debugging
  - Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

See the *ARM<sup>®</sup> Cortex<sup>™</sup>-M3 Technical Reference Manual* for more information on the ARM JTAG controller.

## 5.1 Block Diagram

Figure 5-1. JTAG Module Block Diagram



## 5.2 Signal Description

Table 5-1 on page 69 lists the external signals of the JTAG/SWD controller and describes the function of each. The JTAG/SWD controller signals are alternate functions for some GPIO signals, however note that the reset state of the pins is for the JTAG/SWD function. The JTAG/SWD controller signals are under commit protection and require a special process to be configured as GPIOs, see “Commit Control” on page 294. The column in the table below titled “Pin Mux/Pin Assignment” lists the GPIO pin placement for the JTAG/SWD controller signals. The **AFSEL** bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) is set to choose the JTAG/SWD function. The number in parentheses is the encoding that must be programmed into the **PMC<sub>n</sub>** field in the **GPIO Port Control (GPIOPCTL)** register (page 328) to assign the JTAG/SWD controller signals to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 288.

Table 5-1. Signals for JTAG\_SWO\_SWO

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
SWCLK	80	PC0 (3)	I	TTL	JTAG/SWD CLK.
SWDIO	79	PC1 (3)	I/O	TTL	JTAG TMS and SWDIO.
SWO	77	PC3 (3)	O	TTL	JTAG TDO and SWO.
TCK	80	PC0 (3)	I	TTL	JTAG/SWD CLK.
TDI	78	PC2 (3)	I	TTL	JTAG TDI.
TDO	77	PC3 (3)	O	TTL	JTAG TDO and SWO.

**Table 5-1. Signals for JTAG\_SWD\_SWO (continued)**

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
TMS	79	PC1 (3)	I	TTL	JTAG TMS and SWDIO.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 5.3 Functional Description

A high-level conceptual drawing of the JTAG module is shown in Figure 5-1 on page 69. The JTAG module is composed of the Test Access Port (TAP) controller and serial shift chains with parallel update registers. The TAP controller is a simple state machine controlled by the TCK and TMS inputs. The current state of the TAP controller depends on the sequence of values captured on TMS at the rising edge of TCK. The TAP controller determines when the serial shift chains capture new data, shift data from TDI towards TDO, and update the parallel load registers. The current state of the TAP controller also determines whether the Instruction Register (IR) chain or one of the Data Register (DR) chains is being accessed.

The serial shift chains with parallel load registers are comprised of a single Instruction Register (IR) chain and multiple Data Register (DR) chains. The current instruction loaded in the parallel load register determines which DR chain is captured, shifted, or updated during the sequencing of the TAP controller.

Some instructions, like EXTEST and INTEST, operate on data currently in a DR chain and do not capture, shift, or update any of the chains. Instructions that are not implemented decode to the BYPASS instruction to ensure that the serial path between TDI and TDO is always connected (see Table 5-3 on page 76 for a list of implemented instructions).

See “JTAG and Boundary Scan” on page 731 for JTAG timing diagrams.

**Note:** Of all the possible reset sources, only Power-On reset (POR) and the assertion of the  $\overline{\text{RST}}$  input have any effect on the JTAG module. The pin configurations are reset by both the  $\overline{\text{RST}}$  input and POR, whereas the internal JTAG logic is only reset with POR. See “Reset Sources” on page 81 for more information on reset.

### 5.3.1 JTAG Interface Pins

The JTAG interface consists of four standard pins: TCK, TMS, TDI, and TDO. These pins and their associated state after a power-on reset or reset caused by the  $\overline{\text{RST}}$  input are given in Table 5-2. Detailed information on each pin follows. Refer to “General-Purpose Input/Outputs (GPIOs)” on page 288 for information on how to reprogram the configuration of these pins.

**Table 5-2. JTAG Port Pins State after Power-On Reset or  $\overline{\text{RST}}$  assertion**

Pin Name	Data Direction	Internal Pull-Up	Internal Pull-Down	Drive Strength	Drive Value
TCK	Input	Enabled	Disabled	N/A	N/A
TMS	Input	Enabled	Disabled	N/A	N/A
TDI	Input	Enabled	Disabled	N/A	N/A
TDO	Output	Enabled	Disabled	2-mA driver	High-Z

#### 5.3.1.1 Test Clock Input (TCK)

The TCK pin is the clock for the JTAG module. This clock is provided so the test logic can operate independently of any other system clocks and to ensure that multiple JTAG TAP controllers that are daisy-chained together can synchronously communicate serial test data between components.

During normal operation, TCK is driven by a free-running clock with a nominal 50% duty cycle. When necessary, TCK can be stopped at 0 or 1 for extended periods of time. While TCK is stopped at 0 or 1, the state of the TAP controller does not change and data in the JTAG Instruction and Data Registers is not lost.

By default, the internal pull-up resistor on the TCK pin is enabled after reset, assuring that no clocking occurs if the pin is not driven from an external source. The internal pull-up and pull-down resistors can be turned off to save internal power as long as the TCK pin is constantly being driven by an external source (see page 316 and page 318).

### 5.3.1.2 Test Mode Select (TMS)

The TMS pin selects the next state of the JTAG TAP controller. TMS is sampled on the rising edge of TCK. Depending on the current TAP state and the sampled value of TMS, the next state may be entered. Because the TMS pin is sampled on the rising edge of TCK, the *IEEE Standard 1149.1* expects the value on TMS to change on the falling edge of TCK.

Holding TMS high for five consecutive TCK cycles drives the TAP controller state machine to the Test-Logic-Reset state. When the TAP controller enters the Test-Logic-Reset state, the JTAG module and associated registers are reset to their default values. This procedure should be performed to initialize the JTAG controller. The JTAG Test Access Port state machine can be seen in its entirety in Figure 5-2 on page 72.

By default, the internal pull-up resistor on the TMS pin is enabled after reset. Changes to the pull-up resistor settings on GPIO Port C should ensure that the internal pull-up resistor remains enabled on PC1/TMS; otherwise JTAG communication could be lost (see page 316).

### 5.3.1.3 Test Data Input (TDI)

The TDI pin provides a stream of serial information to the IR chain and the DR chains. TDI is sampled on the rising edge of TCK and, depending on the current TAP state and the current instruction, may present this data to the proper shift register chain. Because the TDI pin is sampled on the rising edge of TCK, the *IEEE Standard 1149.1* expects the value on TDI to change on the falling edge of TCK.

By default, the internal pull-up resistor on the TDI pin is enabled after reset. Changes to the pull-up resistor settings on GPIO Port C should ensure that the internal pull-up resistor remains enabled on PC2/TDI; otherwise JTAG communication could be lost (see page 316).

### 5.3.1.4 Test Data Output (TDO)

The TDO pin provides an output stream of serial information from the IR chain or the DR chains. The value of TDO depends on the current TAP state, the current instruction, and the data in the chain being accessed. In order to save power when the JTAG port is not being used, the TDO pin is placed in an inactive drive state when not actively shifting out data. Because TDO can be connected to the TDI of another controller in a daisy-chain configuration, the *IEEE Standard 1149.1* expects the value on TDO to change on the falling edge of TCK.

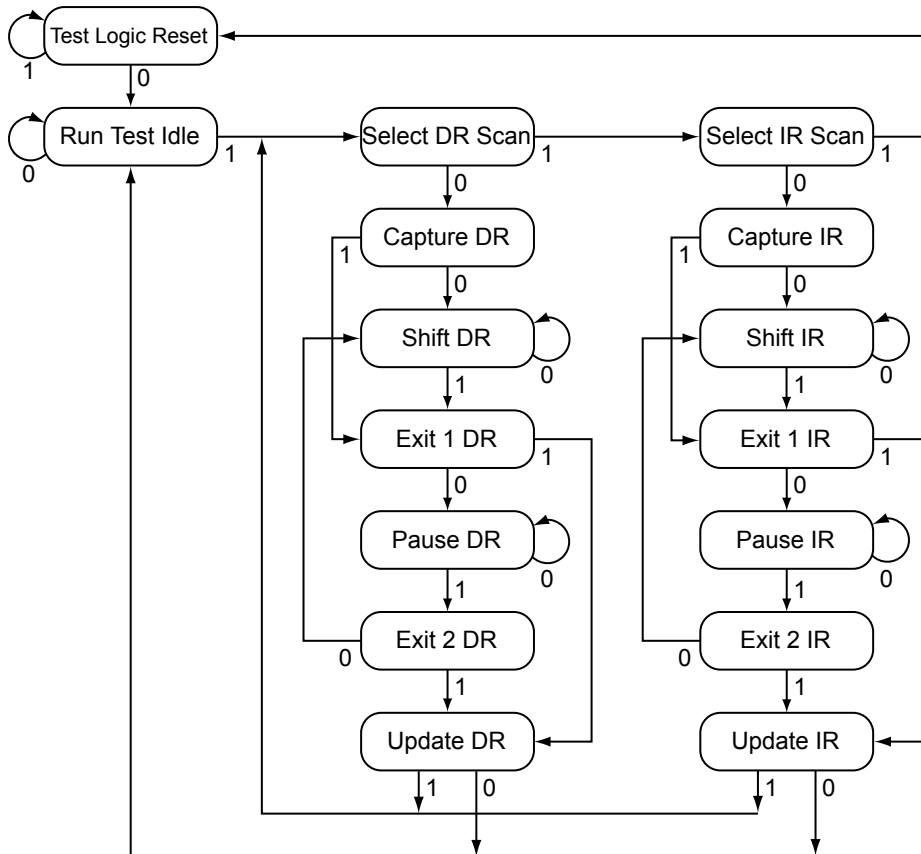
By default, the internal pull-up resistor on the TDO pin is enabled after reset, assuring that the pin remains at a constant logic level when the JTAG port is not being used. The internal pull-up and pull-down resistors can be turned off to save internal power if a High-Z output value is acceptable during certain TAP controller states (see page 316 and page 318).

## 5.3.2 JTAG TAP Controller

The JTAG TAP controller state machine is shown in Figure 5-2. The TAP controller state machine is reset to the Test-Logic-Reset state on the assertion of a Power-On-Reset (POR). In order to reset

the JTAG module after the microcontroller has been powered on, the TMS input must be held HIGH for five TCK clock cycles, resetting the TAP controller and all associated JTAG chains. Asserting the correct sequence on the TMS pin allows the JTAG module to shift in new instructions, shift in data, or idle during extended testing sequences. For detailed information on the function of the TAP controller and the operations that occur in each state, please refer to *IEEE Standard 1149.1*.

**Figure 5-2. Test Access Port State Machine**



### 5.3.3 Shift Registers

The Shift Registers consist of a serial shift register chain and a parallel load register. The serial shift register chain samples specific information during the TAP controller’s CAPTURE states and allows this information to be shifted out on TDO during the TAP controller’s SHIFT states. While the sampled data is being shifted out of the chain on TDO, new data is being shifted into the serial shift register on TDI. This new data is stored in the parallel load register during the TAP controller’s UPDATE states. Each of the shift registers is discussed in detail in “Register Descriptions” on page 75.

### 5.3.4 Operational Considerations

Certain operational parameters must be considered when using the JTAG module. Because the JTAG pins can be programmed to be GPIOs, board configuration and reset conditions on these pins must be considered. In addition, because the JTAG module has integrated ARM Serial Wire Debug, the method for switching between these two operational modes is described below.



### 5.3.4.1 GPIO Functionality

When the microcontroller is reset with either a POR or  $\overline{\text{RST}}$ , the JTAG/SWD port pins default to their JTAG/SWD configurations. The default configuration includes enabling digital functionality ( $\text{DEN}[3:0]$  set in the **Port C GPIO Digital Enable (GPIODEN)** register), enabling the pull-up resistors ( $\text{PUE}[3:0]$  set in the **Port C GPIO Pull-Up Select (GPIOPUR)** register), disabling the pull-down resistors ( $\text{PDE}[3:0]$  cleared in the **Port C GPIO Pull-Down Select (GPIOPDR)** register) and enabling the alternate hardware function ( $\text{AFSEL}[3:0]$  set in the **Port C GPIO Alternate Function Select (GPIOAFSEL)** register) on the JTAG/SWD pins. See page 310, page 316, page 318, and page 321.

It is possible for software to configure these pins as GPIOs after reset by clearing  $\text{AFSEL}[3:0]$  in the **Port C GPIOAFSEL** register. If the user does not require the JTAG/SWD port for debugging or board-level testing, this provides four more GPIOs for use in the design.

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**Caution – It is possible to create a software sequence that prevents the debugger from connecting to the Stellaris® microcontroller. If the program code loaded into flash immediately changes the JTAG pins to their GPIO functionality, the debugger may not have enough time to connect and halt the controller before the JTAG pin functionality switches. As a result, the debugger may be locked out of the part. This issue can be avoided with a software routine that restores JTAG functionality based on an external or software trigger.**

---

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is currently provided for the NMI pin ( $\text{PB7}$ ) and the four JTAG/SWD pins ( $\text{PC}[3:0]$ ). Writes to protected bits of the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 310), **GPIO Pull Up Select (GPIOPUR)** register (see page 316), **GPIO Pull-Down Select (GPIOPDR)** register (see page 318), and **GPIO Digital Enable (GPIODEN)** register (see page 321) are not committed to storage unless the **GPIO Lock (GPIOLOCK)** register (see page 323) has been unlocked and the appropriate bits of the **GPIO Commit (GPIOCR)** register (see page 324) have been set.

### 5.3.4.2 Communication with JTAG/SWD

Because the debug clock and the system clock can be running at different frequencies, care must be taken to maintain reliable communication with the JTAG/SWD interface. In the Capture-DR state, the result of the previous transaction, if any, is returned, together with a 3-bit ACK response. Software should check the ACK response to see if the previous operation has completed before initiating a new transaction. Alternatively, if the system clock is at least 8 times faster than the debug clock ( $\text{TCK}$  or  $\text{SWCLK}$ ), the previous operation has enough time to complete and the ACK bits do not have to be checked.

### 5.3.4.3 Recovering a "Locked" Microcontroller

**Note:** Performing the sequence below restores the nonvolatile registers discussed in “Nonvolatile Register Programming” on page 201 to their factory default values. The mass erase of the Flash memory caused by the sequence below occurs prior to the nonvolatile registers being restored.

If software configures any of the JTAG/SWD pins as GPIO and loses the ability to communicate with the debugger, there is a debug sequence that can be used to recover the microcontroller. Performing a total of ten JTAG-to-SWD and SWD-to-JTAG switch sequences while holding the microcontroller in reset mass erases the Flash memory. The sequence to recover the microcontroller is:

1. Assert and hold the  $\overline{\text{RST}}$  signal.

2. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence on the section called “JTAG-to-SWD Switching” on page 74.
3. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence on the section called “SWD-to-JTAG Switching” on page 75.
4. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
5. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
6. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
7. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
8. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
9. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
10. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
11. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
12. Release the  $\overline{\text{RST}}$  signal.
13. Wait 400 ms.
14. Power-cycle the microcontroller.

#### 5.3.4.4 ARM Serial Wire Debug (SWD)

In order to seamlessly integrate the ARM Serial Wire Debug (SWD) functionality, a serial-wire debugger must be able to connect to the Cortex-M3 core without having to perform, or have any knowledge of, JTAG cycles. This integration is accomplished with a SWD preamble that is issued before the SWD session begins.

The switching preamble used to enable the SWD interface of the SWJ-DP module starts with the TAP controller in the Test-Logic-Reset state. From here, the preamble sequences the TAP controller through the following states: Run Test Idle, Select DR, Select IR, Test Logic Reset, Test Logic Reset, Run Test Idle, Run Test Idle, Select DR, Select IR, Test Logic Reset, Test Logic Reset, Run Test Idle, Run Test Idle, Select DR, Select IR, and Test Logic Reset states.

Stepping through this sequence of the TAP state machine enables the SWD interface and disables the JTAG interface. For more information on this operation and the SWD interface, see the *ARM® Cortex™-M3 Technical Reference Manual* and the *ARM® CoreSight Technical Reference Manual*.

Because this sequence is a valid series of JTAG operations that could be issued, the ARM JTAG TAP controller is not fully compliant to the *IEEE Standard 1149.1*. This instance is the only one where the ARM JTAG TAP controller does not meet full compliance with the specification. Due to the low probability of this sequence occurring during normal operation of the TAP controller, it should not affect normal performance of the JTAG interface.

#### **JTAG-to-SWD Switching**

To switch the operating mode of the Debug Access Port (DAP) from JTAG to SWD mode, the external debug hardware must send the switching preamble to the microcontroller. The 16-bit TMS command for switching to SWD mode is defined as b1110.0111.1001.1110, transmitted LSB first.

This command can also be represented as 0xE79E when transmitted LSB first. The complete switch sequence should consist of the following transactions on the TCK/SWCLK and TMS/SWDIO signals:

1. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that both JTAG and SWD are in their reset/idle states.
2. Send the 16-bit JTAG-to-SWD switch command, 0xE79E, on TMS.
3. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that if SWJ-DP was already in SWD mode, the SWD goes into the line reset state before sending the switch sequence.

### **SWD-to-JTAG Switching**

To switch the operating mode of the Debug Access Port (DAP) from SWD to JTAG mode, the external debug hardware must send a switch command to the microcontroller. The 16-bit TMS command for switching to JTAG mode is defined as b1110.0111.0011.1100, transmitted LSB first. This command can also be represented as 0xE73C when transmitted LSB first. The complete switch sequence should consist of the following transactions on the TCK/SWCLK and TMS/SWDIO signals:

1. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that both JTAG and SWD are in their reset/idle states.
2. Send the 16-bit SWD-to-JTAG switch command, 0xE73C, on TMS.
3. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that if SWJ-DP was already in JTAG mode, the JTAG goes into the Test Logic Reset state before sending the switch sequence.

## **5.4 Initialization and Configuration**

After a Power-On-Reset or an external reset ( $\overline{RST}$ ), the JTAG pins are automatically configured for JTAG communication. No user-defined initialization or configuration is needed. However, if the user application changes these pins to their GPIO function, they must be configured back to their JTAG functionality before JTAG communication can be restored. To return the pins to their JTAG functions, enable the four JTAG pins (PC[3:0]) for their alternate function using the **GPIOAFSEL** register. In addition to enabling the alternate functions, any other changes to the GPIO pad configurations on the four JTAG pins (PC[3:0]) should be returned to their default settings.

## **5.5 Register Descriptions**

The registers in the JTAG TAP Controller or Shift Register chains are not memory mapped and are not accessible through the on-chip Advanced Peripheral Bus (APB). Instead, the registers within the JTAG controller are all accessed serially through the TAP Controller. These registers include the Instruction Register and the six Data Registers.

### **5.5.1 Instruction Register (IR)**

The JTAG TAP Instruction Register (IR) is a four-bit serial scan chain connected between the JTAG TDI and TDO pins with a parallel load register. When the TAP Controller is placed in the correct states, bits can be shifted into the IR. Once these bits have been shifted into the chain and updated, they are interpreted as the current instruction. The decode of the IR bits is shown in Table 5-3. A detailed explanation of each instruction, along with its associated Data Register, follows.

**Table 5-3. JTAG Instruction Register Commands**

IR[3:0]	Instruction	Description
0x0	EXTEST	Drives the values preloaded into the Boundary Scan Chain by the SAMPLE/PRELOAD instruction onto the pads.
0x1	INTEST	Drives the values preloaded into the Boundary Scan Chain by the SAMPLE/PRELOAD instruction into the controller.
0x2	SAMPLE / PRELOAD	Captures the current I/O values and shifts the sampled values out of the Boundary Scan Chain while new preload data is shifted in.
0x8	ABORT	Shifts data into the ARM Debug Port Abort Register.
0xA	DPACC	Shifts data into and out of the ARM DP Access Register.
0xB	APACC	Shifts data into and out of the ARM AC Access Register.
0xE	IDCODE	Loads manufacturing information defined by the <i>IEEE Standard 1149.1</i> into the IDCODE chain and shifts it out.
0xF	BYPASS	Connects TDI to TDO through a single Shift Register chain.
All Others	Reserved	Defaults to the BYPASS instruction to ensure that TDI is always connected to TDO.

**5.5.1.1 EXTEST Instruction**

The EXTEST instruction is not associated with its own Data Register chain. Instead, the EXTEST instruction uses the data that has been preloaded into the Boundary Scan Data Register using the SAMPLE/PRELOAD instruction. When the EXTEST instruction is present in the Instruction Register, the preloaded data in the Boundary Scan Data Register associated with the outputs and output enables are used to drive the GPIO pads rather than the signals coming from the core. With tests that drive known values out of the controller, this instruction can be used to verify connectivity. While the EXTEST instruction is present in the Instruction Register, the Boundary Scan Data Register can be accessed to sample and shift out the current data and load new data into the Boundary Scan Data Register.

**5.5.1.2 INTEST Instruction**

The INTEST instruction is not associated with its own Data Register chain. Instead, the INTEST instruction uses the data that has been preloaded into the Boundary Scan Data Register using the SAMPLE/PRELOAD instruction. When the INTEST instruction is present in the Instruction Register, the preloaded data in the Boundary Scan Data Register associated with the inputs are used to drive the signals going into the core rather than the signals coming from the GPIO pads. With tests that drive known values into the controller, this instruction can be used for testing. It is important to note that although the RST input pin is on the Boundary Scan Data Register chain, it is only observable. While the INTEST instruction is present in the Instruction Register, the Boundary Scan Data Register can be accessed to sample and shift out the current data and load new data into the Boundary Scan Data Register.

**5.5.1.3 SAMPLE/PRELOAD Instruction**

The SAMPLE/PRELOAD instruction connects the Boundary Scan Data Register chain between TDI and TDO. This instruction samples the current state of the pad pins for observation and preloads new test data. Each GPIO pad has an associated input, output, and output enable signal. When the TAP controller enters the Capture DR state during this instruction, the input, output, and output-enable signals to each of the GPIO pads are captured. These samples are serially shifted out on TDO while the TAP controller is in the Shift DR state and can be used for observation or comparison in various tests.

While these samples of the inputs, outputs, and output enables are being shifted out of the Boundary Scan Data Register, new data is being shifted into the Boundary Scan Data Register from TDI. Once the new data has been shifted into the Boundary Scan Data Register, the data is saved in the parallel load registers when the TAP controller enters the Update DR state. This update of the parallel load register preloads data into the Boundary Scan Data Register that is associated with each input, output, and output enable. This preloaded data can be used with the EXTEST and INTEST instructions to drive data into or out of the controller. See “Boundary Scan Data Register” on page 78 for more information.

#### 5.5.1.4 ABORT Instruction

The ABORT instruction connects the associated ABORT Data Register chain between TDI and TDO. This instruction provides read and write access to the ABORT Register of the ARM Debug Access Port (DAP). Shifting the proper data into this Data Register clears various error bits or initiates a DAP abort of a previous request. See the “ABORT Data Register” on page 79 for more information.

#### 5.5.1.5 DPACC Instruction

The DPACC instruction connects the associated DPACC Data Register chain between TDI and TDO. This instruction provides read and write access to the DPACC Register of the ARM Debug Access Port (DAP). Shifting the proper data into this register and reading the data output from this register allows read and write access to the ARM debug and status registers. See “DPACC Data Register” on page 79 for more information.

#### 5.5.1.6 APACC Instruction

The APACC instruction connects the associated APACC Data Register chain between TDI and TDO. This instruction provides read and write access to the APACC Register of the ARM Debug Access Port (DAP). Shifting the proper data into this register and reading the data output from this register allows read and write access to internal components and buses through the Debug Port. See “APACC Data Register” on page 79 for more information.

#### 5.5.1.7 IDCODE Instruction

The IDCODE instruction connects the associated IDCODE Data Register chain between TDI and TDO. This instruction provides information on the manufacturer, part number, and version of the ARM core. This information can be used by testing equipment and debuggers to automatically configure input and output data streams. IDCODE is the default instruction loaded into the JTAG Instruction Register when a Power-On-Reset (POR) is asserted, or the Test-Logic-Reset state is entered. See “IDCODE Data Register” on page 78 for more information.

#### 5.5.1.8 BYPASS Instruction

The BYPASS instruction connects the associated BYPASS Data Register chain between TDI and TDO. This instruction is used to create a minimum length serial path between the TDI and TDO ports. The BYPASS Data Register is a single-bit shift register. This instruction improves test efficiency by allowing components that are not needed for a specific test to be bypassed in the JTAG scan chain by loading them with the BYPASS instruction. See “BYPASS Data Register” on page 78 for more information.

### 5.5.2 Data Registers

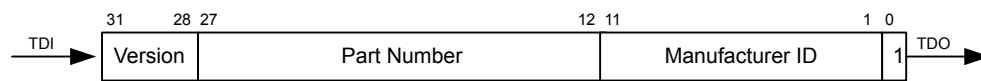
The JTAG module contains six Data Registers. These serial Data Register chains include: IDCODE, BYPASS, Boundary Scan, APACC, DPACC, and ABORT and are discussed in the following sections.

### 5.5.2.1 IDCODE Data Register

The format for the 32-bit IDCODE Data Register defined by the *IEEE Standard 1149.1* is shown in Figure 5-3. The standard requires that every JTAG-compliant microcontroller implement either the IDCODE instruction or the BYPASS instruction as the default instruction. The LSB of the IDCODE Data Register is defined to be a 1 to distinguish it from the BYPASS instruction, which has an LSB of 0. This definition allows auto-configuration test tools to determine which instruction is the default instruction.

The major uses of the JTAG port are for manufacturer testing of component assembly and program development and debug. To facilitate the use of auto-configuration debug tools, the IDCODE instruction outputs a value of 0x4BA0.0477. This value allows the debuggers to automatically configure themselves to work correctly with the Cortex-M3 during debug.

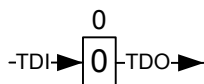
**Figure 5-3. IDCODE Register Format**



### 5.5.2.2 BYPASS Data Register

The format for the 1-bit BYPASS Data Register defined by the *IEEE Standard 1149.1* is shown in Figure 5-4. The standard requires that every JTAG-compliant microcontroller implement either the BYPASS instruction or the IDCODE instruction as the default instruction. The LSB of the BYPASS Data Register is defined to be a 0 to distinguish it from the IDCODE instruction, which has an LSB of 1. This definition allows auto-configuration test tools to determine which instruction is the default instruction.

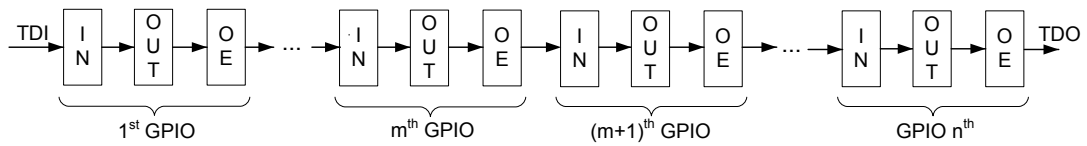
**Figure 5-4. BYPASS Register Format**



### 5.5.2.3 Boundary Scan Data Register

The format of the Boundary Scan Data Register is shown in Figure 5-5. Each GPIO pin, starting with a GPIO pin next to the JTAG port pins, is included in the Boundary Scan Data Register. Each GPIO pin has three associated digital signals that are included in the chain. These signals are input, output, and output enable, and are arranged in that order as shown in the figure.

When the Boundary Scan Data Register is accessed with the SAMPLE/PRELOAD instruction, the input, output, and output enable from each digital pad are sampled and then shifted out of the chain to be verified. The sampling of these values occurs on the rising edge of TCK in the Capture DR state of the TAP controller. While the sampled data is being shifted out of the Boundary Scan chain in the Shift DR state of the TAP controller, new data can be preloaded into the chain for use with the EXTEST and INTEST instructions. The EXTEST instruction forces data out of the controller, and the INTEST instruction forces data into the controller.

**Figure 5-5. Boundary Scan Register Format**

#### 5.5.2.4 APACC Data Register

The format for the 35-bit APACC Data Register defined by ARM is described in the *ARM® Cortex™-M3 Technical Reference Manual*.

#### 5.5.2.5 DPACC Data Register

The format for the 35-bit DPACC Data Register defined by ARM is described in the *ARM® Cortex™-M3 Technical Reference Manual*.

#### 5.5.2.6 ABORT Data Register

The format for the 35-bit ABORT Data Register defined by ARM is described in the *ARM® Cortex™-M3 Technical Reference Manual*.

## 6 System Control

System control configures the overall operation of the device and provides information about the device. Configurable features include reset control, NMI operation, power control, clock control, and low-power modes.

### 6.1 Signal Description

Table 6-1 on page 80 lists the external signals of the System Control module and describes the function of each. The NMI signal is the alternate function for the GPIO PB7 signal and functions as a GPIO after reset. PB7 is under commit protection and requires a special process to be configured as the NMI signal or to subsequently return to the GPIO function, see “Commit Control” on page 294. The column in the table below titled “Pin Mux/Pin Assignment” lists the GPIO pin placement for the NMI signal. The AFSEL bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) should be set to choose the NMI function. The number in parentheses is the encoding that must be programmed into the PMCN field in the **GPIO Port Control (GPIOPCTL)** register (page 328) to assign the NMI signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 288. The remaining signals (with the word “fixed” in the Pin Mux/Pin Assignment column) have a fixed pin assignment and function.

**Table 6-1. Signals for System Control & Clocks**

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
NMI	89	PB7 (4)	I	TTL	Non-maskable interrupt.
OSC0	48	fixed	I	Analog	Main oscillator crystal input or an external clock reference input.
OSC1	49	fixed	O	Analog	Main oscillator crystal output.
RST	64	fixed	I	TTL	System reset input.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

### 6.2 Functional Description

The System Control module provides the following capabilities:

- Device identification, see “Device Identification” on page 80
- Local control, such as reset (see “Reset Control” on page 80), power (see “Power Control” on page 85) and clock control (see “Clock Control” on page 86)
- System control (Run, Sleep, and Deep-Sleep modes), see “System Control” on page 92

#### 6.2.1 Device Identification

Several read-only registers provide software with information on the microcontroller, such as version, part number, SRAM size, Flash memory size, and other features. See the **DID0** (page 96), **DID1** (page 123), **DC0-DC9** (page 125) and **NVMSTAT** (page 142) registers.

#### 6.2.2 Reset Control

This section discusses aspects of hardware functions during reset as well as system software requirements following the reset sequence.



### 6.2.2.1 Reset Sources

The LM3S1811 microcontroller has six sources of reset:

1. Power-on reset (POR) (see page 81).
2. External reset input pin ( $\overline{RST}$ ) assertion (see page 82).
3. Internal brown-out (BOR) detector (see page 83).
4. Software-initiated reset (with the software reset registers) (see page 83).
5. A watchdog timer reset condition violation (see page 84).
6. MOSC failure (see page 85).

Table 6-2 provides a summary of results of the various reset operations.

**Table 6-2. Reset Sources**

Reset Source	Core Reset?	JTAG Reset?	On-Chip Peripherals Reset?
Power-On Reset	Yes	Yes	Yes
$\overline{RST}$	Yes	Pin Config Only	Yes
Brown-Out Reset	Yes	No	Yes
Software Reset	Yes <sup>a</sup>	No	Yes <sup>b</sup>
Watchdog Reset	Yes	No	Yes
MOSC Failure Reset	Yes	No	Yes

a. By using the SYSRESETREQ bit in the ARM Cortex-M3 Application Interrupt and Reset Control register

b. Programmable on a module-by-module basis using the Software Reset Control Registers.

After a reset, the **Reset Cause (RESC)** register is set with the reset cause. The bits in this register are sticky and maintain their state across multiple reset sequences, except when an internal POR is the cause, in which case, all the bits in the **RESC** register are cleared except for the POR indicator. A bit in the **RESC** register can be cleared by writing a 0.

### 6.2.2.2 Power-On Reset (POR)

**Note:** The power-on reset also resets the JTAG controller. An external reset does not.

The internal Power-On Reset (POR) circuit monitors the power supply voltage ( $V_{DD}$ ) and generates a reset signal to all of the internal logic including JTAG when the power supply ramp reaches a threshold value ( $V_{TH}$ ). The microcontroller must be operating within the specified operating parameters when the on-chip power-on reset pulse is complete. The 3.3-V power supply to the microcontroller must reach 3.0 V within 10 msec of  $V_{DD}$  crossing 2.0 V to guarantee proper operation. For applications that require the use of an external reset signal to hold the microcontroller in reset longer than the internal POR, the  $\overline{RST}$  input may be used as discussed in “External  $\overline{RST}$  Pin” on page 82.

The Power-On Reset sequence is as follows:

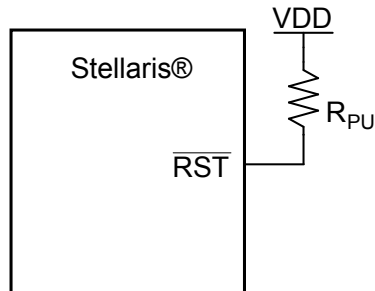
1. The microcontroller waits for internal POR to go inactive.
2. The internal reset is released and the core loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

The internal POR is only active on the initial power-up of the microcontroller. The Power-On Reset timing is shown in Figure 22-5 on page 734.

### 6.2.2.3 External $\overline{\text{RST}}$ Pin

If the application only uses the internal POR circuit, the  $\overline{\text{RST}}$  input must be connected to the power supply ( $V_{\text{DD}}$ ) through an optional pull-up resistor (0 to 10K  $\Omega$ ) as shown in Figure 6-1 on page 82.

**Figure 6-1. Basic  $\overline{\text{RST}}$  Configuration**



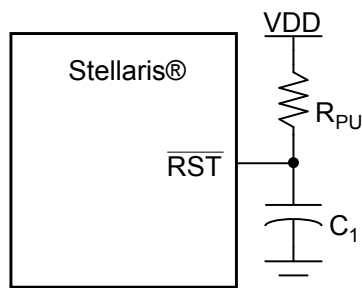
$R_{\text{PU}} = 0$  to 100 k $\Omega$

The external reset pin ( $\overline{\text{RST}}$ ) resets the microcontroller including the core and all the on-chip peripherals except the JTAG TAP controller (see “JTAG Interface” on page 68). The external reset sequence is as follows:

1. The external reset pin ( $\overline{\text{RST}}$ ) is asserted for the duration specified by  $T_{\text{MIN}}$  and then de-asserted (see “Reset” on page 733).
2. The internal reset is released and the core loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

To improve noise immunity and/or to delay reset at power up, the  $\overline{\text{RST}}$  input may be connected to an RC network as shown in Figure 6-2 on page 82.

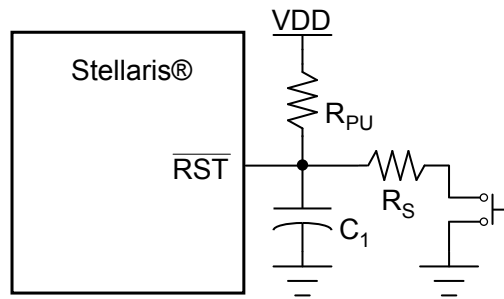
**Figure 6-2. External Circuitry to Extend Power-On Reset**



$R_{\text{PU}} = 1$  k $\Omega$  to 100 k $\Omega$

$C_1 = 1$  nF to 10  $\mu\text{F}$

If the application requires the use of an external reset switch, Figure 6-3 on page 83 shows the proper circuitry to use.

**Figure 6-3. Reset Circuit Controlled by Switch**

Typical  $R_{PU} = 10\text{ k}\Omega$

Typical  $R_S = 470\ \Omega$

$C_1 = 10\text{ nF}$

The  $R_{PU}$  and  $C_1$  components define the power-on delay.

The external reset timing is shown in Figure 22-4 on page 733.

#### 6.2.2.4 Brown-Out Reset (BOR)

The microcontroller provides a brown-out detection circuit that triggers if the power supply ( $V_{DD}$ ) drops below a brown-out threshold voltage ( $V_{BTH}$ ). If a brown-out condition is detected, the system may generate an interrupt or a system reset. Brown-out resets are controlled with the **Power-On and Brown-Out Reset Control (PBORCTL)** register. The  $BORIOR$  bit in the **PBORCTL** register must be set for a brown-out condition to trigger a reset; if  $BORIOR$  is clear, an interrupt is generated. The default condition is to generate an interrupt, so BOR must be enabled. When a Brown-out condition occurs during a Flash PROGRAM or ERASE operation, a full system reset is always triggered without regard to the setting in the **PBORCTL** register.

The result of a brown-out reset is equivalent to that of an assertion of the external  $\overline{RST}$  input, and the reset is held active until the proper  $V_{DD}$  level is restored. The **RESC** register can be examined in the reset interrupt handler to determine if a Brown-Out condition was the cause of the reset, thus allowing software to determine what actions are required to recover.

The internal Brown-Out Reset timing is shown in Figure 22-6 on page 734.

#### 6.2.2.5 Software Reset

Software can reset a specific peripheral or generate a reset to the entire microcontroller.

Peripherals can be individually reset by software via three registers that control reset signals to each on-chip peripheral (see the **SRCRn** registers, page 164). If the bit position corresponding to a peripheral is set and subsequently cleared, the peripheral is reset. The encoding of the reset registers is consistent with the encoding of the clock gating control for peripherals and on-chip functions (see “System Control” on page 92).

The entire microcontroller including the core can be reset by software by setting the **SYSRESETREQ** bit in the Cortex-M3 Application Interrupt and Reset Control register. The software-initiated system reset sequence is as follows:

1. A software microcontroller reset is initiated by setting the **SYSRESETREQ** bit in the ARM Cortex-M3 Application Interrupt and Reset Control register.

2. An internal reset is asserted.
3. The internal reset is deasserted and the microcontroller loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

The software-initiated system reset timing is shown in Figure 22-7 on page 734.

### 6.2.2.6 Watchdog Timer Reset

The Watchdog Timer module's function is to prevent system hangs. The LM3S1811 microcontroller has two Watchdog Timer modules in case one watchdog clock source fails. One watchdog is run off the system clock and the other is run off the Precision Internal Oscillator (PIOSC). Each module operates in the same manner except that because the PIOSC watchdog timer module is in a different clock domain, register accesses must have a time delay between them. The watchdog timer can be configured to generate an interrupt to the microcontroller on its first time-out and to generate a reset on its second time-out.

After the watchdog's first time-out event, the 32-bit watchdog counter is reloaded with the value of the **Watchdog Timer Load (WDTLOAD)** register and resumes counting down from that value. If the timer counts down to zero again before the first time-out interrupt is cleared, and the reset signal has been enabled, the watchdog timer asserts its reset signal to the microcontroller. The watchdog timer reset sequence is as follows:

1. The watchdog timer times out for the second time without being serviced.
2. An internal reset is asserted.
3. The internal reset is released and the microcontroller loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

For more information on the Watchdog Timer module, see "Watchdog Timers" on page 453.

The watchdog reset timing is shown in Figure 22-8 on page 734.

### 6.2.3 Non-Maskable Interrupt

The microcontroller has three sources of non-maskable interrupt (NMI):

- The assertion of the `NMI` signal
- A main oscillator verification error
- The `NMISSET` bit in the **Interrupt Control and Status (ICSR)** register in the Cortex-M3.

Software must check the cause of the interrupt in order to distinguish among the sources.

#### 6.2.3.1 NMI Pin

The alternate function to GPIO port pin B7 is an NMI signal. The alternate function must be enabled in the GPIO for the signal to be used as an interrupt, as described in "General-Purpose Input/Outputs (GPIOs)" on page 288. Note that enabling the NMI alternate function requires the use of the GPIO lock and commit function just like the GPIO port pins associated with JTAG/SWD functionality, see page 324. The active sense of the NMI signal is High; asserting the enabled NMI signal above  $V_{IH}$  initiates the NMI interrupt sequence.

### 6.2.3.2 Main Oscillator Verification Failure

The LM3S1811 microcontroller provides a main oscillator verification circuit that generates an error condition if the oscillator is running too fast or too slow. The main oscillator verification circuit can be programmed to generate a reset event, at which time a Power-on Reset is generated and control is transferred to the NMI handler. The NMI handler is used to address the main oscillator verification failure because the necessary code can be removed from the general reset handler, speeding up reset processing. The detection circuit is enabled by setting the `CVAL` bit in the **Main Oscillator Control (MOSCCTL)** register. The main oscillator verification error is indicated in the main oscillator fail status (`MOSCFAIL`) bit in the **Reset Cause (RESC)** register. The main oscillator verification circuit action is described in more detail in “Main Oscillator Verification Circuit” on page 92.

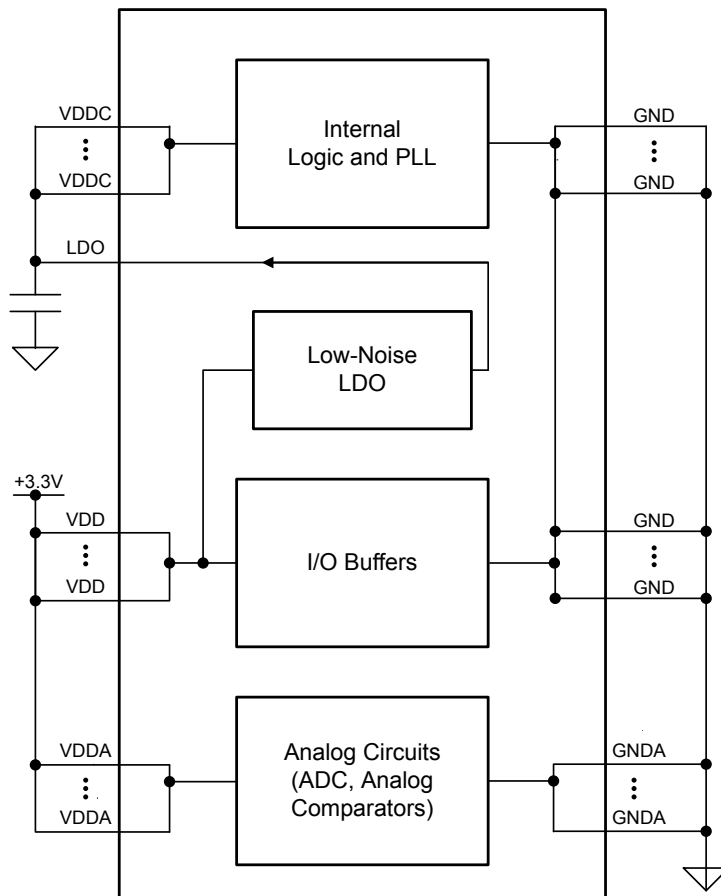
### 6.2.4 Power Control

The Stellaris® microcontroller provides an integrated LDO regulator that is used to provide power to the majority of the microcontroller's internal logic. For power reduction, a non-programmable LDO may be used to scale the microcontroller's 3.3 V input voltage to 1.2V. The voltage output has a minimum voltage of 1.08 V and a maximum of 1.35 V. The LDO delivers up to 60 ma.

Figure 6-4 shows the power architecture.

**Note:** On the printed circuit board, use the `LDO` output as the source of `VDDC` input. In addition, the LDO requires decoupling capacitors. See “On-Chip Low Drop-Out (LDO) Regulator Characteristics” on page 727.

Figure 6-4. Power Architecture



## 6.2.5 Clock Control

System control determines the control of clocks in this part.

### 6.2.5.1 Fundamental Clock Sources

There are multiple clock sources for use in the microcontroller:

- **Precision Internal Oscillator (PIOSC).** The precision internal oscillator is an on-chip clock source that is the clock source the microcontroller uses during and following POR. It does not require the use of any external components and provides a clock that is 16 MHz  $\pm$ 1% at room temperature and  $\pm$ 3% across temperature. The PIOSC allows for a reduced system cost in applications that require an accurate clock source. If the main oscillator is required, software must enable the main oscillator following reset and allow the main oscillator to stabilize before changing the clock reference. If the Hibernation Module clock source is a 32.768-kHz oscillator, the precision internal oscillator can be trimmed by software based on a reference clock for increased accuracy.
- **Main Oscillator (MOSC).** The main oscillator provides a frequency-accurate clock source by one of two means: an external single-ended clock source is connected to the OSC0 input pin, or an external crystal is connected across the OSC0 input and OSC1 output pins. If the PLL is being used, the crystal value must be one of the supported frequencies between 3.579545 MHz through

16.384 MHz (inclusive). If the PLL is not being used, the crystal may be any one of the supported frequencies between 1 MHz and 16.384 MHz. The single-ended clock source range is from DC through the specified speed of the microcontroller. The supported crystals are listed in the `XTAL` bit field in the **RCC** register (see page 107).

- **Internal 30-kHz Oscillator.** The internal 30-kHz oscillator provides an operational frequency of 30 kHz  $\pm$  50%. It is intended for use during Deep-Sleep power-saving modes. This power-savings mode benefits from reduced internal switching and also allows the MOSC and PIOSC to be powered down.
- **Hibernation Module Clock Source.** The Hibernation module can be clocked in one of two ways. The first way is a 4.194304-MHz crystal connected to the `XOSC0` and `XOSC1` pins. This clock signal is divided by 128 internally to produce the 32.768-kHz clock reference. The second way is a 32.768-kHz oscillator connected to the `XOSC0` pin. The clock source for the Hibernation module can be used for the system clock, thus eliminating the need for an additional crystal or oscillator. In addition, a 4.194304-MHz crystal can also be a source for the PLL. The Hibernation module clock source is intended to provide the system with a real-time clock source and may also provide an accurate source of Deep-Sleep or Hibernate mode power savings.

The internal system clock (SysClk), is derived from any of the above sources plus two others: the output of the main internal PLL and the precision internal oscillator divided by four (4 MHz  $\pm$  1%). The frequency of the PLL clock reference must be in the range of 3.579545 MHz to 16.384 MHz (inclusive). Table 6-3 on page 87 shows how the various clock sources can be used in a system.

**Table 6-3. Clock Source Options**

Clock Source	Drive PLL?		Used as SysClk?	
	Yes	ByPass = 0, OSCSRC = 0x1	Yes	ByPass = 1, OSCSRC = 0x1
Precision Internal Oscillator	Yes	ByPass = 0, OSCSRC = 0x1	Yes	ByPass = 1, OSCSRC = 0x1
Precision Internal Oscillator divide by 4 (4 MHz $\pm$ 1%)	No	ByPass = 1	Yes	ByPass = 1, OSCSRC = 0x2
Main Oscillator	Yes	ByPass = 0, OSCSRC = 0x0	Yes	ByPass = 1, OSCSRC = 0x0
Internal 30-kHz Oscillator	No	ByPass = 1	Yes	ByPass = 1, OSCSRC = 0x3
Hibernation Module 4.194304-MHz Crystal	Yes	ByPass = 0, OSCSRC2 = 0x7	Yes	ByPass = 1, OSCSRC2 = 0x6
Hibernation Module 32.768-kHz Oscillator	No	ByPass = 1	Yes	ByPass = 1, OSCSRC2 = 0x7

### 6.2.5.2 Clock Configuration

The **Run-Mode Clock Configuration (RCC)** and **Run-Mode Clock Configuration 2 (RCC2)** registers provide control for the system clock. The **RCC2** register is provided to extend fields that offer additional encodings over the **RCC** register. When used, the **RCC2** register field values are used by the logic over the corresponding field in the **RCC** register. In particular, **RCC2** provides for a larger assortment of clock configuration options. These registers control the following clock functionality:

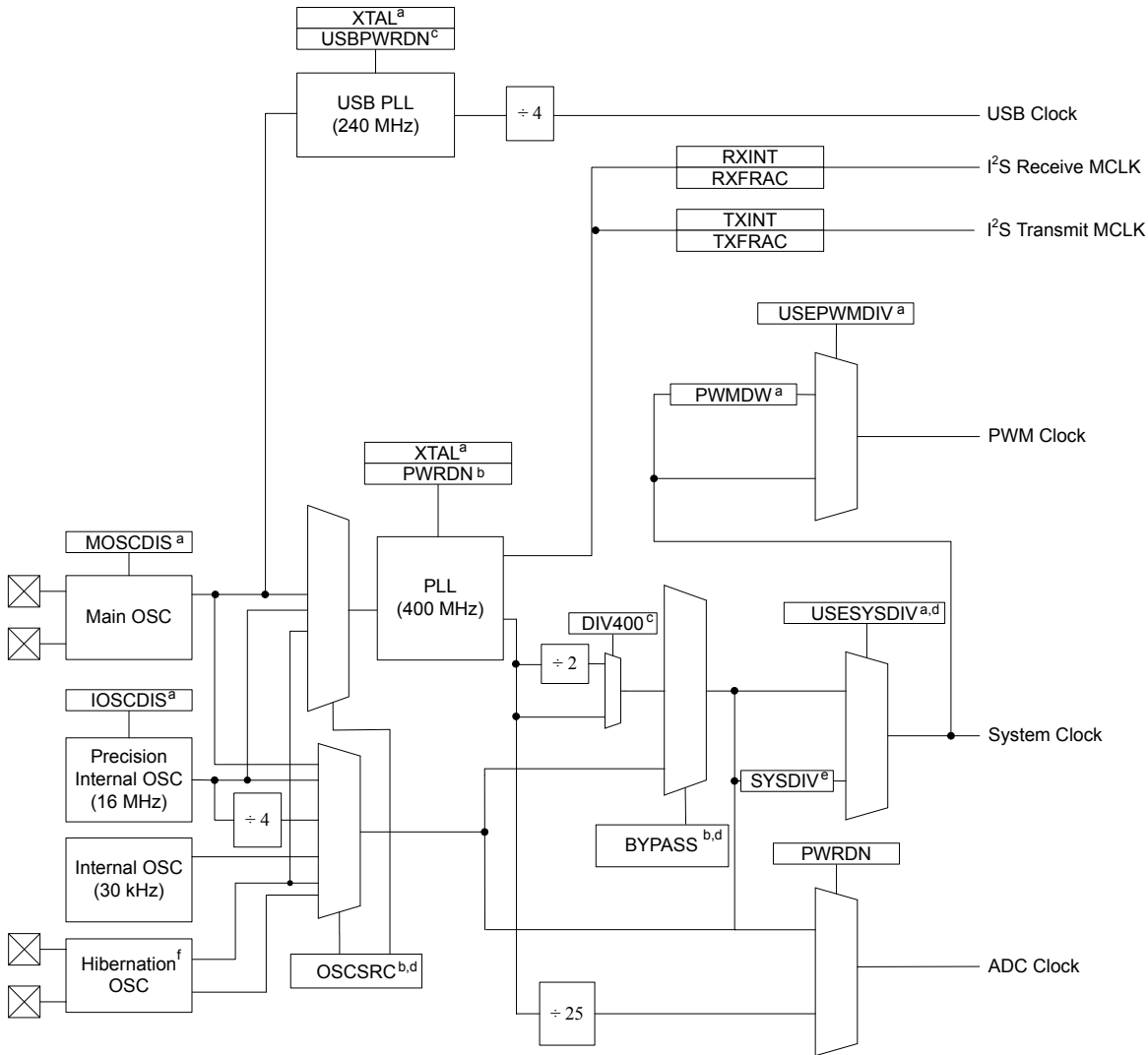
- Source of clocks in sleep and deep-sleep modes
- System clock derived from PLL or other clock source
- Enabling/disabling of oscillators and PLL

- Clock divisors
- Crystal input selection

Figure 6-5 shows the logic for the main clock tree. The peripheral blocks are driven by the system clock signal and can be individually enabled/disabled. The ADC clock signal is automatically divided down to 16 MHz for proper ADC operation.

**Note:** When the ADC module is in operation, the system clock must be at least 16 MHz.

Figure 6-5. Main Clock Tree



- a. Control provided by **RCC** register bit/field.
- b. Control provided by **RCC** register bit/field or **RCC2** register bit/field, if overridden with **RCC2** register bit USERCC2.
- c. Control provided by **RCC2** register bit/field.
- d. Also may be controlled by **DSLCLKCFG** when in deep sleep mode.
- e. Control provided by **RCC** register SYSDIV field, **RCC2** register SYSDIV2 field if overridden with USERCC2 bit, or [SYSDIV2,SYSDIV2LSB] if both USERCC2 and DIV400 bits are set.
- f. Only a 4.194304-Mhz crystal can be used to drive the PLL.

**Note:** The figure above shows all features available on all Stellaris® Tempest-class microcontrollers.



In the **RCC** register, the **SYSDIV** field specifies which divisor is used to generate the system clock from either the PLL output or the oscillator source (depending on how the **BYPASS** bit in this register is configured). When using the PLL, the VCO frequency of 400 MHz is predivided by 2 before the divisor is applied. Table 6-4 shows how the **SYSDIV** encoding affects the system clock frequency, depending on whether the PLL is used (**BYPASS=0**) or another clock source is used (**BYPASS=1**). The divisor is equivalent to the **SYSDIV** encoding plus 1. For a list of possible clock sources, see Table 6-3 on page 87.

**Table 6-4. Possible System Clock Frequencies Using the SYSDIV Field**

SYSDIV	Divisor	Frequency (BYPASS=0)	Frequency (BYPASS=1)	StellarisWare Parameter <sup>a</sup>
0x0	/1	reserved	Clock source frequency	SYSCCTL_SYSDIV_1
0x1	/2	reserved	Clock source frequency/2	SYSCCTL_SYSDIV_2
0x2	/3	reserved	Clock source frequency/3	SYSCCTL_SYSDIV_3
0x3	/4	50 MHz	Clock source frequency/4	SYSCCTL_SYSDIV_4
0x4	/5	40 MHz	Clock source frequency/5	SYSCCTL_SYSDIV_5
0x5	/6	33.33 MHz	Clock source frequency/6	SYSCCTL_SYSDIV_6
0x6	/7	28.57 MHz	Clock source frequency/7	SYSCCTL_SYSDIV_7
0x7	/8	25 MHz	Clock source frequency/8	SYSCCTL_SYSDIV_8
0x8	/9	22.22 MHz	Clock source frequency/9	SYSCCTL_SYSDIV_9
0x9	/10	20 MHz	Clock source frequency/10	SYSCCTL_SYSDIV_10
0xA	/11	18.18 MHz	Clock source frequency/11	SYSCCTL_SYSDIV_11
0xB	/12	16.67 MHz	Clock source frequency/12	SYSCCTL_SYSDIV_12
0xC	/13	15.38 MHz	Clock source frequency/13	SYSCCTL_SYSDIV_13
0xD	/14	14.29 MHz	Clock source frequency/14	SYSCCTL_SYSDIV_14
0xE	/15	13.33 MHz	Clock source frequency/15	SYSCCTL_SYSDIV_15
0xF	/16	12.5 MHz (default)	Clock source frequency/16	SYSCCTL_SYSDIV_16

a. This parameter is used in functions such as `SysCtlClockSet()` in the Stellaris Peripheral Driver Library.

The **SYSDIV2** field in the **RCC2** register is 2 bits wider than the **SYSDIV** field in the **RCC** register so that additional larger divisors up to /64 are possible, allowing a lower system clock frequency for improved Deep Sleep power consumption. When using the PLL, the VCO frequency of 400 MHz is predivided by 2 before the divisor is applied. The divisor is equivalent to the **SYSDIV2** encoding plus 1. Table 6-5 shows how the **SYSDIV2** encoding affects the system clock frequency, depending on whether the PLL is used (**BYPASS2=0**) or another clock source is used (**BYPASS2=1**). For a list of possible clock sources, see Table 6-3 on page 87.

**Table 6-5. Examples of Possible System Clock Frequencies Using the SYSDIV2 Field**

SYSDIV2	Divisor	Frequency (BYPASS2=0)	Frequency (BYPASS2=1)	StellarisWare Parameter <sup>a</sup>
0x00	/1	reserved	Clock source frequency	SYSCCTL_SYSDIV_1
0x01	/2	reserved	Clock source frequency/2	SYSCCTL_SYSDIV_2
0x02	/3	reserved	Clock source frequency/3	SYSCCTL_SYSDIV_3
0x03	/4	50 MHz	Clock source frequency/4	SYSCCTL_SYSDIV_4
...	...	...	...	...
0x09	/10	20 MHz	Clock source frequency/10	SYSCCTL_SYSDIV_10
...	...	...	...	...

**Table 6-5. Examples of Possible System Clock Frequencies Using the SYSDIV2 Field (continued)**

SYSDIV2	Divisor	Frequency (BYPASS2=0)	Frequency (BYPASS2=1)	StellarisWare Parameter <sup>a</sup>
0x3F	/64	3.125 MHz	Clock source frequency/64	SYSTL_SYSDIV_64

a. This parameter is used in functions such as SysCtlClockSet() in the Stellaris Peripheral Driver Library.

To allow for additional frequency choices when using the PLL, the DIV400 bit is provided along with the SYSDIV2LSB bit. When the DIV400 bit is set, bit 22 becomes the LSB for SYSDIV2. In this situation, the divisor is equivalent to the (SYSDIV2 encoding with SYSDIV2LSB appended) plus one. When the DIV400 bit is clear, SYSDIV2LSB is ignored, and the system clock frequency is determined as shown in Table 6-5 on page 89. Care must be taken when using these frequency choices with StellarisWare DriverLib API functions. see Table 6-6.

**Table 6-6. Examples of Possible System Clock Frequencies with DIV400=1**

SYSDIV2	SYSDIV2LSB	Divisor	Frequency (BYPASS2=0) <sup>a</sup>	StellarisWare Parameter <sup>b</sup>
0x00	reserved	/2	reserved	-
0x01	0	/3	reserved	-
	1	/4	reserved	-
0x02	0	/5	reserved	-
	1	/6	reserved	-
0x03	0	/7	reserved	-
	1	/8	50 MHz	SYSTL_SYSDIV_4
0x04	0	/9	44.44 MHz	SYSTL_SYSDIV_4_5
	1	/10	40 MHz	SYSTL_SYSDIV_5
...	...	...	...	...
0x3F	0	/127	3.15 MHz	SYSTL_SYSDIV_63_5
	1	/128	3.125 MHz	SYSTL_SYSDIV_64

a. Note that DIV400 and SYSDIV2LSB are only valid when BYPASS2=0.

b. This parameter is used in functions such as SysCtlClockSet() in the Stellaris Peripheral Driver Library.

### 6.2.5.3 Precision Internal Oscillator Operation (PIOSC)

The microcontroller powers up with the PIOSC running. If another clock source is desired, the PIOSC can be powered down by setting the IOSCDIS bit in the RCC register.

The PIOSC generates a 16 MHz clock with a  $\pm 1\%$  accuracy at room temperatures. Across the extended temperature range, the accuracy is  $\pm 3\%$ . At the factory, the PIOSC is set to 16 MHz at room temperature, however, the frequency can be trimmed for other voltage or temperature conditions using software in one of three ways:

- Default calibration: clear the UTEN bit and set the UPDATE bit in the **Precision Internal Oscillator Calibration (PIOSCCAL)** register.
- User-defined calibration: The user can program the UT value to adjust the PIOSC frequency. As the UT value increases, the generated period increases. To commit a new UT value, first set the UTEN bit, then program the UT field, and then set the UPDATE bit. The adjustment finishes within a few clock periods and is glitch free.

- Automatic calibration using the enable 32.768-kHz oscillator from the Hibernation module: set the `CAL` bit; the results of the calibration are shown in the `RESULT` field in the **Precision Internal Oscillator Statistic (PIOSCSTAT)** register. After calibration is complete, the PIOSC is trimmed using trimmed value returned in the `CT` field.

#### 6.2.5.4 Crystal Configuration for the Main Oscillator (MOSC)

The main oscillator supports the use of a select number of crystals. If the main oscillator is used by the PLL as a reference clock, the supported range of crystals is 3.579545 to 16.384 MHz, otherwise, the range of supported crystals is 1 to 16.384 MHz.

The `XTAL` bit in the **RCC** register (see page 107) describes the available crystal choices and default programming values.

Software configures the **RCC** register `XTAL` field with the crystal number. If the PLL is used in the design, the `XTAL` field value is internally translated to the PLL settings.

#### 6.2.5.5 Main PLL Frequency Configuration

The main PLL is disabled by default during power-on reset and is enabled later by software if required. Software specifies the output divisor to set the system clock frequency and enables the main PLL to drive the output. The PLL operates at 400 MHz, but is divided by two prior to the application of the output divisor. Table 22-9 on page 729 shows the actual PLL frequency and error for a given crystal choice.

To configure the PIOSC to be the clock source for the main PLL, program the `OSCR2` field in the **Run-Mode Clock Configuration 2 (RCC2)** register to be 0x1.

If the main oscillator provides the clock reference to the main PLL, the translation provided by hardware and used to program the PLL is available for software in the **XTAL to PLL Translation (PLLCFG)** register (see page 111). The internal translation provides a translation within  $\pm 1\%$  of the targeted PLL VCO frequency.

To configure the Hibernation module clock source as the PLL input reference, program the `OSCR2` field in the **Run-Mode Clock Configuration 2 (RCC2)** register to be 0x6 for a 4.194304-MHz crystal or 0x7 for an external 32.768-kHz oscillator.

The Crystal Value field (`XTAL`) in the **Run-Mode Clock Configuration (RCC)** register (see page 107) describes the available crystal choices and default programming of the **PLLCFG** register. Any time the `XTAL` field changes, the new settings are translated and the internal PLL settings are updated.

#### 6.2.5.6 PLL Modes

two modes of operation: Normal and Power-Down

- Normal: The PLL multiplies the input clock reference and drives the output.
- Power-Down: Most of the PLL internal circuitry is disabled and the PLL does not drive the output.

The modes are programmed using the **RCC/RCC2** register fields (see page 107 and page 114).

#### 6.2.5.7 PLL Operation

If a PLL configuration is changed, the PLL output frequency is unstable until it reconverges (relocks) to the new setting. The time between the configuration change and relock is  $T_{\text{READY}}$  (see Table 22-8 on page 729). During the relock time, the affected PLL is not usable as a clock reference.

PLL is changed by one of the following:

- Change to the XTAL value in the **RCC** register—writes of the same value do not cause a reload.
- Change in the PLL from Power-Down to Normal mode.

A counter is defined to measure the  $T_{\text{READY}}$  requirement. The counter is clocked by the main oscillator. The range of the main oscillator has been taken into account and the down counter is set to 0x1200 (that is, ~600  $\mu\text{s}$  at an 8.192 MHz external oscillator clock). When the XTAL value is greater than 0x0F, the down counter is set to 0x2400 to maintain the required lock time on higher frequency crystal inputs. Hardware is provided to keep the PLL from being used as a system clock until the  $T_{\text{READY}}$  condition is met after one of the two changes above. It is the user's responsibility to have a stable clock source (like the main oscillator) before the **RCC/RCC2** register is switched to use the PLL.

If the main PLL is enabled and the system clock is switched to use the PLL in one step, the system control hardware continues to clock the microcontroller from the oscillator selected by the **RCC/RCC2** register until the main PLL is stable ( $T_{\text{READY}}$  time met), after which it changes to the PLL. Software can use many methods to ensure that the system is clocked from the main PLL, including periodically polling the `PLLLRIS` bit in the **Raw Interrupt Status (RIS)** register, and enabling the PLL Lock interrupt.

#### 6.2.5.8 Main Oscillator Verification Circuit

The clock control includes circuitry to ensure that the main oscillator is running at the appropriate frequency. The circuit monitors the main oscillator frequency and signals if the frequency is outside of the allowable band of attached crystals.

The detection circuit is enabled using the `CVAL` bit in the **Main Oscillator Control (MOSCCTL)** register. If this circuit is enabled and detects an error, the following sequence is performed by the hardware:

1. The `MOSCFAIL` bit in the **Reset Cause (RESC)** register is set.
2. If the internal oscillator (PIOSC) is disabled, it is enabled.
3. The system clock is switched from the main oscillator to the PIOSC.
4. An internal power-on reset is initiated that lasts for 32 PIOSC periods.
5. Reset is de-asserted and the processor is directed to the NMI handler during the reset sequence.

#### 6.2.6 System Control

For power-savings purposes, the **RCGCn**, **SCGCn**, and **DCGCn** registers control the clock gating logic for each peripheral or block in the system while the microcontroller is in Run, Sleep, and Deep-Sleep mode, respectively. The **DC1**, **DC2** and **DC4** registers act as a write mask for the **RCGCn**, **SCGCn**, and **DCGCn** registers.

There are four levels of operation for the microcontroller defined as:

- **Run Mode.** In Run mode, the microcontroller actively executes code. Run mode provides normal operation of the processor and all of the peripherals that are currently enabled by the **RCGCn** registers. The system clock can be any of the available clock sources including the PLL.
- **Sleep Mode.** In Sleep mode, the clock frequency of the active peripherals is unchanged, but the processor and the memory subsystem are not clocked and therefore no longer execute code. Sleep mode is entered by the Cortex-M3 core executing a WFI (Wait for Interrupt) instruction.

Any properly configured interrupt event in the system brings the processor back into Run mode. See the system control NVIC section of the *ARM® Cortex™-M3 Technical Reference Manual* for more details.

Peripherals are clocked that are enabled in the **SCGCn** register when auto-clock gating is enabled (see the **RCC** register) or the **RCGCn** register when the auto-clock gating is disabled. The system clock has the same source and frequency as that during Run mode.

- **Deep-Sleep Mode.** In Deep-Sleep mode, the clock frequency of the active peripherals may change (depending on the Run mode clock configuration) in addition to the processor clock being stopped. An interrupt returns the microcontroller to Run mode from one of the sleep modes; the sleep modes are entered on request from the code. Deep-Sleep mode is entered by first writing the Deep Sleep Enable bit in the ARM Cortex-M3 NVIC system control register and then executing a WFI instruction. Any properly configured interrupt event in the system brings the processor back into Run mode. See the system control NVIC section of the *ARM® Cortex™-M3 Technical Reference Manual* for more details.

The Cortex-M3 processor core and the memory subsystem are not clocked. Peripherals are clocked that are enabled in the **DCGCn** register when auto-clock gating is enabled (see the **RCC** register) or the **RCGCn** register when auto-clock gating is disabled. The system clock source is specified in the **DSLCLKCFG** register. When the **DSLCLKCFG** register is used, the internal oscillator source is powered up, if necessary, and other clocks are powered down. If the PLL is running at the time of the WFI instruction, hardware powers the PLL down and overrides the **SYSDIV** field of the active **RCC/RCC2** register, to be determined by the **DSDIVORIDE** setting in the **DSLCLKCFG** register, up to /16 or /64 respectively. When the Deep-Sleep exit event occurs, hardware brings the system clock back to the source and frequency it had at the onset of Deep-Sleep mode before enabling the clocks that had been stopped during the Deep-Sleep duration. If the PIOSC or the 4.194304-MHz Hibernation module clock source is used as the PLL reference clock source, it may continue to provide the clock during Deep-Sleep. See page 118.

- **Hibernate Mode.** In this mode, the power supplies are turned off to the main part of the microcontroller and only the Hibernation module's circuitry is active. An external wake event or RTC event is required to bring the microcontroller back to Run mode. The Cortex-M3 processor and peripherals outside of the Hibernation module see a normal "power on" sequence and the processor starts running code. Software can determine if the microcontroller has been restarted from Hibernate mode by inspecting the Hibernation module registers.

## 6.3 Initialization and Configuration

The PLL is configured using direct register writes to the **RCC/RCC2** register. If the **RCC2** register is being used, the **USERCC2** bit must be set and the appropriate **RCC2** bit/field is used. The steps required to successfully change the PLL-based system clock are:

1. Bypass the PLL and system clock divider by setting the **BYPASS** bit and clearing the **USESYS** bit in the **RCC** register, thereby configuring the microcontroller to run off a "raw" clock source and allowing for the new PLL configuration to be validated before switching the system clock to the PLL.
2. Select the crystal value (**XTAL**) and oscillator source (**OSCSRC**), and clear the **PWRDN** bit in **RCC/RCC2**. Setting the **XTAL** field automatically pulls valid PLL configuration data for the appropriate crystal, and clearing the **PWRDN** bit powers and enables the PLL and its output.
3. Select the desired system divider (**SYSDIV**) in **RCC/RCC2** and set the **USESYS** bit in **RCC**. The **SYSDIV** field determines the system frequency for the microcontroller.

4. Wait for the PLL to lock by polling the `PLLLRIS` bit in the **Raw Interrupt Status (RIS)** register.
5. Enable use of the PLL by clearing the `BYPASS` bit in **RCC/RCC2**.

## 6.4 Register Map

Table 6-7 on page 94 lists the System Control registers, grouped by function. The offset listed is a hexadecimal increment to the register's address, relative to the System Control base address of `0x400F.E000`.

**Note:** Spaces in the System Control register space that are not used are reserved for future or internal use. Software should not modify any reserved memory address.

Additional Flash and ROM registers defined in the System Control register space are described in the "Internal Memory" on page 197.

**Table 6-7. System Control Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	DID0	RO	-	Device Identification 0	96
0x004	DID1	RO	-	Device Identification 1	123
0x008	DC0	RO	0x007F.007F	Device Capabilities 0	125
0x010	DC1	RO	-	Device Capabilities 1	126
0x014	DC2	RO	0x430F.5037	Device Capabilities 2	128
0x018	DC3	RO	0xBFFF.0FC0	Device Capabilities 3	130
0x01C	DC4	RO	0x0004.F1FF	Device Capabilities 4	132
0x020	DC5	RO	0x0000.0000	Device Capabilities 5	134
0x024	DC6	RO	0x0000.0000	Device Capabilities 6	135
0x028	DC7	RO	0xFFFF.FFFF	Device Capabilities 7	136
0x02C	DC8	RO	0x0000.00FF	Device Capabilities 8 ADC Channels	140
0x030	PBORCTL	R/W	0x0000.7FFD	Brown-Out Reset Control	98
0x040	SRCR0	R/W	0x00000000	Software Reset Control 0	164
0x044	SRCR1	R/W	0x00000000	Software Reset Control 1	166
0x048	SRCR2	R/W	0x00000000	Software Reset Control 2	169
0x050	RIS	RO	0x0000.0000	Raw Interrupt Status	99
0x054	IMC	R/W	0x0000.0000	Interrupt Mask Control	101
0x058	MISC	R/W1C	0x0000.0000	Masked Interrupt Status and Clear	103
0x05C	RESC	R/W	-	Reset Cause	105
0x060	RCC	R/W	0x0780.3AD1	Run-Mode Clock Configuration	107
0x064	PLLCFG	RO	-	XTAL to PLL Translation	111
0x06C	GPIOHCTL	R/W	0x0000.0000	GPIO High-Performance Bus Control	112

Table 6-7. System Control Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0x070	RCC2	R/W	0x0780.6810	Run-Mode Clock Configuration 2	114
0x07C	MOSCCTL	R/W	0x0000.0000	Main Oscillator Control	117
0x100	RCGC0	R/W	0x00000040	Run Mode Clock Gating Control Register 0	143
0x104	RCGC1	R/W	0x00000000	Run Mode Clock Gating Control Register 1	149
0x108	RCGC2	R/W	0x00000000	Run Mode Clock Gating Control Register 2	158
0x110	SCGC0	R/W	0x00000040	Sleep Mode Clock Gating Control Register 0	145
0x114	SCGC1	R/W	0x00000000	Sleep Mode Clock Gating Control Register 1	152
0x118	SCGC2	R/W	0x00000000	Sleep Mode Clock Gating Control Register 2	160
0x120	DCGC0	R/W	0x00000040	Deep Sleep Mode Clock Gating Control Register 0	147
0x124	DCGC1	R/W	0x00000000	Deep-Sleep Mode Clock Gating Control Register 1	155
0x128	DCGC2	R/W	0x00000000	Deep Sleep Mode Clock Gating Control Register 2	162
0x144	DSLPLCKCFG	R/W	0x0780.0000	Deep Sleep Clock Configuration	118
0x150	PIOSCCAL	R/W	0x0000.0000	Precision Internal Oscillator Calibration	120
0x154	PIOSCSTAT	RO	0x0000.0040	Precision Internal Oscillator Statistics	122
0x190	DC9	RO	0x0000.00FF	Device Capabilities 9 ADC Digital Comparators	141
0x1A0	NVMSTAT	RO	0x0000.0001	Non-Volatile Memory Information	142

## 6.5 Register Descriptions

All addresses given are relative to the System Control base address of 0x400F.E000.

## Register 1: Device Identification 0 (DID0), offset 0x000

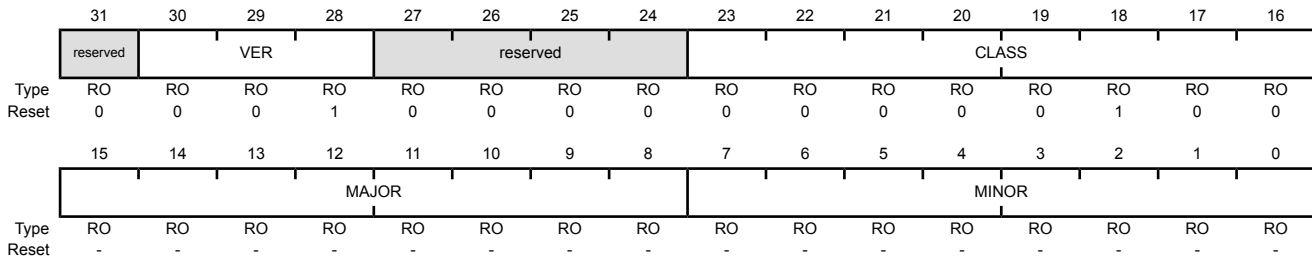
This register identifies the version of the microcontroller.

### Device Identification 0 (DID0)

Base 0x400F.E000

Offset 0x000

Type RO, reset -



Bit/Field	Name	Type	Reset	Description				
31	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.				
30:28	VER	RO	0x1	<p>DID0 Version</p> <p>This field defines the <b>DID0</b> register format version. The version number is numeric. The value of the <code>VER</code> field is encoded as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x1</td> <td>Second version of the <b>DID0</b> register format.</td> </tr> </tbody> </table>	Value	Description	0x1	Second version of the <b>DID0</b> register format.
Value	Description							
0x1	Second version of the <b>DID0</b> register format.							
27:24	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.				
23:16	CLASS	RO	0x04	<p>Device Class</p> <p>The <code>CLASS</code> field value identifies the internal design from which all mask sets are generated for all microcontrollers in a particular product line. The <code>CLASS</code> field value is changed for new product lines, for changes in fab process (for example, a remap or shrink), or any case where the <code>MAJOR</code> or <code>MINOR</code> fields require differentiation from prior microcontrollers. The value of the <code>CLASS</code> field is encoded as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x04</td> <td>Stellaris® Tempest-class microcontrollers</td> </tr> </tbody> </table>	Value	Description	0x04	Stellaris® Tempest-class microcontrollers
Value	Description							
0x04	Stellaris® Tempest-class microcontrollers							



Bit/Field	Name	Type	Reset	Description								
15:8	MAJOR	RO	-	<p>Major Revision</p> <p>This field specifies the major revision number of the microcontroller. The major revision reflects changes to base layers of the design. The major revision number is indicated in the part number as a letter (A for first revision, B for second, and so on). This field is encoded as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Revision A (initial device)</td> </tr> <tr> <td>0x1</td> <td>Revision B (first base layer revision)</td> </tr> <tr> <td>0x2</td> <td>Revision C (second base layer revision)</td> </tr> </tbody> </table> <p>and so on.</p>	Value	Description	0x0	Revision A (initial device)	0x1	Revision B (first base layer revision)	0x2	Revision C (second base layer revision)
Value	Description											
0x0	Revision A (initial device)											
0x1	Revision B (first base layer revision)											
0x2	Revision C (second base layer revision)											
7:0	MINOR	RO	-	<p>Minor Revision</p> <p>This field specifies the minor revision number of the microcontroller. The minor revision reflects changes to the metal layers of the design. The MINOR field value is reset when the MAJOR field is changed. This field is numeric and is encoded as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Initial device, or a major revision update.</td> </tr> <tr> <td>0x1</td> <td>First metal layer change.</td> </tr> <tr> <td>0x2</td> <td>Second metal layer change.</td> </tr> </tbody> </table> <p>and so on.</p>	Value	Description	0x0	Initial device, or a major revision update.	0x1	First metal layer change.	0x2	Second metal layer change.
Value	Description											
0x0	Initial device, or a major revision update.											
0x1	First metal layer change.											
0x2	Second metal layer change.											

## Register 2: Brown-Out Reset Control (PBORCTL), offset 0x030

This register is responsible for controlling reset conditions after initial power-on reset.

### Brown-Out Reset Control (PBORCTL)

Base 0x400F.E000  
 Offset 0x030  
 Type R/W, reset 0x0000.7FFD

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															BORIOR	reserved
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	BORIOR	R/W	0	BOR Interrupt or Reset  Value Description 0 A Brown Out Event causes an interrupt to be generated to the interrupt controller. 1 A Brown Out Event causes a reset of the microcontroller.
0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

### Register 3: Raw Interrupt Status (RIS), offset 0x050

This register indicates the status for system control raw interrupts. An interrupt is sent to the interrupt controller if the corresponding bit in the **Interrupt Mask Control (IMC)** register is set. Writing a 1 to the corresponding bit in the **Masked Interrupt Status and Clear (MISC)** register clears an interrupt status bit.

#### Raw Interrupt Status (RIS)

Base 0x400F.E000

Offset 0x050

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							MOSCPUPRIS	reserved	PLLLRIS	reserved				BORRIS	reserved
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:9	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	MOSCPUPRIS	RO	0	MOSC Power Up Raw Interrupt Status  Value Description 1 Sufficient time has passed for the MOSC to reach the expected frequency. The value for this power-up time is indicated by $T_{MOSC\_SETTLE}$ . 0 Sufficient time has not passed for the MOSC to reach the expected frequency.  This bit is cleared by writing a 1 to the MOSCPUPMIS bit in the <b>MISC</b> register.
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6	PLLLRIS	RO	0	PLL Lock Raw Interrupt Status  Value Description 1 The PLL timer has reached $T_{READY}$ indicating that sufficient time has passed for the PLL to lock. 0 The PLL timer has not reached $T_{READY}$ .  This bit is cleared by writing a 1 to the PLLLMIS bit in the <b>MISC</b> register.
5:2	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
1	BORRIS	RO	0	<p>Brown-Out Reset Raw Interrupt Status</p> <p>Value Description</p> <p>1 A brown-out condition is currently active.</p> <p>0 A brown-out condition is not currently active.</p> <p>Note the <code>BORIOR</code> bit in the <b>PBORCTL</b> register must be cleared to cause an interrupt due to a Brown Out Event.</p> <p>This bit is cleared by writing a 1 to the <code>BORMIS</code> bit in the <b>MISC</b> register.</p>
0	reserved	RO	0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>

## Register 4: Interrupt Mask Control (IMC), offset 0x054

This register contains the mask bits for system control raw interrupts. A raw interrupt, indicated by a bit being set in the **Raw Interrupt Status (RIS)** register, is sent to the interrupt controller if the corresponding bit in this register is set.

### Interrupt Mask Control (IMC)

Base 0x400F.E000  
Offset 0x054  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							MOSCPUPIM	reserved	PLLLIM	reserved				BORIM	reserved
Type	RO	RO	RO	RO	RO	RO	RO	R/W	RO	R/W	RO	RO	RO	RO	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:9	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	MOSCPUPIM	R/W	0	MOSC Power Up Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the MOSCPUPRIS bit in the <b>RIS</b> register is set. 0 The MOSCPUPRIS interrupt is suppressed and not sent to the interrupt controller.
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6	PLLLIM	R/W	0	PLL Lock Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the PLLLRIS bit in the <b>RIS</b> register is set. 0 The PLLLRIS interrupt is suppressed and not sent to the interrupt controller.
5:2	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
1	BORIM	R/W	0	Brown-Out Reset Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the BORRIS bit in the <b>RIS</b> register is set. 0 The BORRIS interrupt is suppressed and not sent to the interrupt controller.
0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 5: Masked Interrupt Status and Clear (MISC), offset 0x058

On a read, this register gives the current masked status value of the corresponding interrupt in the **Raw Interrupt Status (RIS)** register. All of the bits are R/W1C, thus writing a 1 to a bit clears the corresponding raw interrupt bit in the **RIS** register (see page 99).

### Masked Interrupt Status and Clear (MISC)

Base 0x400F.E000

Offset 0x058

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							MOSCPUPMIS	reserved	PLLLMIS	reserved				BORMIS	reserved
Type	RO	RO	RO	RO	RO	RO	RO	R/W1C	RO	R/W1C	RO	RO	RO	RO	R/W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:9	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	MOSCPUPMIS	R/W1C	0	<p>MOSC Power Up Masked Interrupt Status</p> <p><b>Value Description</b></p> <p>1 When read, a 1 indicates that an unmasked interrupt was signaled because sufficient time has passed for the MOSC PLL to lock.</p> <p>Writing a 1 to this bit clears it and also the <code>MOSCPUPRIS</code> bit in the <b>RIS</b> register.</p> <p>0 When read, a 0 indicates that sufficient time has not passed for the MOSC PLL to lock.</p> <p>A write of 0 has no effect on the state of this bit.</p>
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6	PLLLMIS	R/W1C	0	<p>PLL Lock Masked Interrupt Status</p> <p><b>Value Description</b></p> <p>1 When read, a 1 indicates that an unmasked interrupt was signaled because sufficient time has passed for the PLL to lock.</p> <p>Writing a 1 to this bit clears it and also the <code>PLLLRIS</code> bit in the <b>RIS</b> register.</p> <p>0 When read, a 0 indicates that sufficient time has not passed for the PLL to lock.</p> <p>A write of 0 has no effect on the state of this bit.</p>

Bit/Field	Name	Type	Reset	Description
5:2	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	BORMIS	R/W1C	0	BOR Masked Interrupt Status  Value Description 1 When read, a 1 indicates that an unmasked interrupt was signaled because of a brown-out condition.  Writing a 1 to this bit clears it and also the BORRIS bit in the <b>RIS</b> register. 0 When read, a 0 indicates that a brown-out condition has not occurred.  A write of 0 has no effect on the state of this bit.
0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.



## Register 6: Reset Cause (RESC), offset 0x05C

This register is set with the reset cause after reset. The bits in this register are sticky and maintain their state across multiple reset sequences, except when an power-on reset is the cause, in which case, all bits other than POR in the **RESC** register are cleared.

### Reset Cause (RESC)

Base 0x400F.E000

Offset 0x05C

Type R/W, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															MOSCFAIL
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved										WDT1	SW	WDT0	BOR	POR	EXT
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:17	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	MOSCFAIL	R/W	-	MOSC Failure Reset
				Value Description
			1	When read, this bit indicates that the MOSC circuit was enabled for clock validation and failed, generating a reset event.
			0	When read, this bit indicates that a MOSC failure has not generated a reset since the previous power-on reset.
				Writing a 0 to this bit clears it.
15:6	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5	WDT1	R/W	-	Watchdog Timer 1 Reset
				Value Description
			1	When read, this bit indicates that Watchdog Timer 1 timed out and generated a reset.
			0	When read, this bit indicates that Watchdog Timer 1 has not generated a reset since the previous power-on reset.
				Writing a 0 to this bit clears it.

Bit/Field	Name	Type	Reset	Description
4	SW	R/W	-	<p>Software Reset</p> <p>Value Description</p> <p>1 When read, this bit indicates that a software reset has caused a reset event.</p> <p>0 When read, this bit indicates that a software reset has not generated a reset since the previous power-on reset.</p> <p>Writing a 0 to this bit clears it.</p>
3	WDT0	R/W	-	<p>Watchdog Timer 0 Reset</p> <p>Value Description</p> <p>1 When read, this bit indicates that Watchdog Timer 0 timed out and generated a reset.</p> <p>0 When read, this bit indicates that Watchdog Timer 0 has not generated a reset since the previous power-on reset.</p> <p>Writing a 0 to this bit clears it.</p>
2	BOR	R/W	-	<p>Brown-Out Reset</p> <p>Value Description</p> <p>1 When read, this bit indicates that a brown-out reset has caused a reset event.</p> <p>0 When read, this bit indicates that a brown-out reset has not generated a reset since the previous power-on reset.</p> <p>Writing a 0 to this bit clears it.</p>
1	POR	R/W	-	<p>Power-On Reset</p> <p>Value Description</p> <p>1 When read, this bit indicates that a power-on reset has caused a reset event.</p> <p>0 When read, this bit indicates that a power-on reset has not generated a reset.</p> <p>Writing a 0 to this bit clears it.</p>
0	EXT	R/W	-	<p>External Reset</p> <p>Value Description</p> <p>1 When read, this bit indicates that an external reset (<math>\overline{RST}</math> assertion) has caused a reset event.</p> <p>0 When read, this bit indicates that an external reset (<math>\overline{RST}</math> assertion) has not caused a reset event since the previous power-on reset.</p> <p>Writing a 0 to this bit clears it.</p>

## Register 7: Run-Mode Clock Configuration (RCC), offset 0x060

The bits in this register configure the system clock and oscillators.

### Run-Mode Clock Configuration (RCC)

Base 0x400F.E000

Offset 0x060

Type R/W, reset 0x0780.3AD1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved				ACG	SYSDIV				USESYSDIV	reserved					
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		PWRDN	reserved	BYPASS	XTAL				OSCSRC		reserved		IOSCDIS	MOSCDIS	
Type	RO	RO	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Reset	0	0	1	1	1	0	1	0	1	1	0	1	0	0	0	1

Bit/Field	Name	Type	Reset	Description						
31:28	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
27	ACG	R/W	0	<p>Auto Clock Gating</p> <p>This bit specifies whether the system uses the <b>Sleep-Mode Clock Gating Control (SCGCn)</b> registers and <b>Deep-Sleep-Mode Clock Gating Control (DCGCn)</b> registers if the microcontroller enters a Sleep or Deep-Sleep mode (respectively).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>The <b>SCGCn</b> or <b>DCGCn</b> registers are used to control the clocks distributed to the peripherals when the microcontroller is in a sleep mode. The <b>SCGCn</b> and <b>DCGCn</b> registers allow unused peripherals to consume less power when the microcontroller is in a sleep mode.</td> </tr> <tr> <td>0</td> <td>The <b>Run-Mode Clock Gating Control (RCGCn)</b> registers are used when the microcontroller enters a sleep mode.</td> </tr> </tbody> </table> <p>The <b>RCGCn</b> registers are always used to control the clocks in Run mode.</p>	Value	Description	1	The <b>SCGCn</b> or <b>DCGCn</b> registers are used to control the clocks distributed to the peripherals when the microcontroller is in a sleep mode. The <b>SCGCn</b> and <b>DCGCn</b> registers allow unused peripherals to consume less power when the microcontroller is in a sleep mode.	0	The <b>Run-Mode Clock Gating Control (RCGCn)</b> registers are used when the microcontroller enters a sleep mode.
Value	Description									
1	The <b>SCGCn</b> or <b>DCGCn</b> registers are used to control the clocks distributed to the peripherals when the microcontroller is in a sleep mode. The <b>SCGCn</b> and <b>DCGCn</b> registers allow unused peripherals to consume less power when the microcontroller is in a sleep mode.									
0	The <b>Run-Mode Clock Gating Control (RCGCn)</b> registers are used when the microcontroller enters a sleep mode.									
26:23	SYSDIV	R/W	0xF	<p>System Clock Divisor</p> <p>Specifies which divisor is used to generate the system clock from either the PLL output or the oscillator source (depending on how the <b>BYPASS</b> bit in this register is configured). See Table 6-4 on page 89 for bit encodings.</p> <p>If the <b>SYSDIV</b> value is less than <b>MINSYSDIV</b> (see page 126), and the PLL is being used, then the <b>MINSYSDIV</b> value is used as the divisor.</p> <p>If the PLL is not being used, the <b>SYSDIV</b> value can be less than <b>MINSYSDIV</b>.</p>						

Bit/Field	Name	Type	Reset	Description
22	USESYSDIV	R/W	0	<p>Enable System Clock Divider</p> <p>Value Description</p> <p>1 The system clock divider is the source for the system clock. The system clock divider is forced to be used when the PLL is selected as the source.</p> <p>If the <code>USERCC2</code> bit in the <code>RCC2</code> register is set, then the <code>SYSDIV2</code> field in the <code>RCC2</code> register is used as the system clock divider rather than the <code>SYSDIV</code> field in this register.</p> <p>0 The system clock is used undivided.</p>
21:14	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13	PWRDN	R/W	1	<p>PLL Power Down</p> <p>Value Description</p> <p>1 The PLL is powered down. Care must be taken to ensure that another clock source is functioning and that the <code>BYPASS</code> bit is set before setting this bit.</p> <p>0 The PLL is operating normally.</p>
12	reserved	RO	1	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	BYPASS	R/W	1	<p>PLL Bypass</p> <p>Value Description</p> <p>1 The system clock is derived from the OSC source and divided by the divisor specified by <code>SYSDIV</code>.</p> <p>0 The system clock is the PLL output clock divided by the divisor specified by <code>SYSDIV</code>.</p> <p>See Table 6-4 on page 89 for programming guidelines.</p> <p><b>Note:</b> The ADC must be clocked from the PLL or directly from a 16-MHz clock source to operate properly.</p>

Bit/Field	Name	Type	Reset	Description																																																																								
10:6	XTAL	R/W	0x0B	Crystal Value																																																																								
				This field specifies the crystal value attached to the main oscillator. The encoding for this field is provided below. Depending on the crystal used, the PLL frequency may not be exactly 400 MHz, see Table 22-9 on page 729 for more information.																																																																								
				<table border="1"> <thead> <tr> <th>Value</th> <th>Crystal Frequency (MHz) Not Using the PLL</th> <th>Crystal Frequency (MHz) Using the PLL</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>1.000</td> <td>reserved</td> </tr> <tr> <td>0x01</td> <td>1.8432</td> <td>reserved</td> </tr> <tr> <td>0x02</td> <td>2.000</td> <td>reserved</td> </tr> <tr> <td>0x03</td> <td>2.4576</td> <td>reserved</td> </tr> <tr> <td>0x04</td> <td></td> <td>3.579545 MHz</td> </tr> <tr> <td>0x05</td> <td></td> <td>3.6864 MHz</td> </tr> <tr> <td>0x06</td> <td></td> <td>4 MHz</td> </tr> <tr> <td>0x07</td> <td></td> <td>4.096 MHz</td> </tr> <tr> <td>0x08</td> <td></td> <td>4.9152 MHz</td> </tr> <tr> <td>0x09</td> <td></td> <td>5 MHz</td> </tr> <tr> <td>0x0A</td> <td></td> <td>5.12 MHz</td> </tr> <tr> <td>0x0B</td> <td></td> <td>6 MHz (reset value)</td> </tr> <tr> <td>0x0C</td> <td></td> <td>6.144 MHz</td> </tr> <tr> <td>0x0D</td> <td></td> <td>7.3728 MHz</td> </tr> <tr> <td>0x0E</td> <td></td> <td>8 MHz</td> </tr> <tr> <td>0x0F</td> <td></td> <td>8.192 MHz</td> </tr> <tr> <td>0x10</td> <td></td> <td>10.0 MHz</td> </tr> <tr> <td>0x11</td> <td></td> <td>12.0 MHz</td> </tr> <tr> <td>0x12</td> <td></td> <td>12.288 MHz</td> </tr> <tr> <td>0x13</td> <td></td> <td>13.56 MHz</td> </tr> <tr> <td>0x14</td> <td></td> <td>14.31818 MHz</td> </tr> <tr> <td>0x15</td> <td></td> <td>16.0 MHz</td> </tr> <tr> <td>0x16</td> <td></td> <td>16.384 MHz</td> </tr> </tbody> </table>	Value	Crystal Frequency (MHz) Not Using the PLL	Crystal Frequency (MHz) Using the PLL	0x00	1.000	reserved	0x01	1.8432	reserved	0x02	2.000	reserved	0x03	2.4576	reserved	0x04		3.579545 MHz	0x05		3.6864 MHz	0x06		4 MHz	0x07		4.096 MHz	0x08		4.9152 MHz	0x09		5 MHz	0x0A		5.12 MHz	0x0B		6 MHz (reset value)	0x0C		6.144 MHz	0x0D		7.3728 MHz	0x0E		8 MHz	0x0F		8.192 MHz	0x10		10.0 MHz	0x11		12.0 MHz	0x12		12.288 MHz	0x13		13.56 MHz	0x14		14.31818 MHz	0x15		16.0 MHz	0x16		16.384 MHz
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0x0A		5.12 MHz																																																																										
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Bit/Field	Name	Type	Reset	Description										
5:4	OSCSRC	R/W	0x1	<p>Oscillator Source</p> <p>Selects the input source for the OSC. The values are:</p> <table border="0"> <tr> <td>Value</td> <td>Input Source</td> </tr> <tr> <td>0x0</td> <td>MOSC Main oscillator</td> </tr> <tr> <td>0x1</td> <td>PIOSC Precision internal oscillator (default)</td> </tr> <tr> <td>0x2</td> <td>PIOSC/4 Precision internal oscillator / 4</td> </tr> <tr> <td>0x3</td> <td>30 kHz 30-kHz internal oscillator</td> </tr> </table> <p>For additional oscillator sources, see the <b>RCC2</b> register.</p>	Value	Input Source	0x0	MOSC Main oscillator	0x1	PIOSC Precision internal oscillator (default)	0x2	PIOSC/4 Precision internal oscillator / 4	0x3	30 kHz 30-kHz internal oscillator
Value	Input Source													
0x0	MOSC Main oscillator													
0x1	PIOSC Precision internal oscillator (default)													
0x2	PIOSC/4 Precision internal oscillator / 4													
0x3	30 kHz 30-kHz internal oscillator													
3:2	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
1	IOSCDIS	R/W	0	<p>Precision Internal Oscillator Disable</p> <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>1</td> <td>The precision internal oscillator (PIOSC) is disabled.</td> </tr> <tr> <td>0</td> <td>The precision internal oscillator is enabled.</td> </tr> </table>	Value	Description	1	The precision internal oscillator (PIOSC) is disabled.	0	The precision internal oscillator is enabled.				
Value	Description													
1	The precision internal oscillator (PIOSC) is disabled.													
0	The precision internal oscillator is enabled.													
0	MOSCDIS	R/W	1	<p>Main Oscillator Disable</p> <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>1</td> <td>The main oscillator is disabled (default).</td> </tr> <tr> <td>0</td> <td>The main oscillator is enabled.</td> </tr> </table>	Value	Description	1	The main oscillator is disabled (default).	0	The main oscillator is enabled.				
Value	Description													
1	The main oscillator is disabled (default).													
0	The main oscillator is enabled.													

## Register 8: XTAL to PLL Translation (PLLCFG), offset 0x064

This register provides a means of translating external crystal frequencies into the appropriate PLL settings. This register is initialized during the reset sequence and updated anytime that the `XTAL` field changes in the **Run-Mode Clock Configuration (RCC)** register (see page 107).

The PLL frequency is calculated using the **PLLCFG** field values, as follows:

$$\text{PLLFreq} = \text{OSCFreq} * F / (R + 1)$$

### XTAL to PLL Translation (PLLCFG)

Base 0x400F.E000

Offset 0x064

Type RO, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		F										R			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:14	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13:5	F	RO	-	PLL F Value This field specifies the value supplied to the PLL's F input.
4:0	R	RO	-	PLL R Value This field specifies the value supplied to the PLL's R input.

## Register 9: GPIO High-Performance Bus Control (GPIOHBCTL), offset 0x06C

This register controls which internal bus is used to access each GPIO port. When a bit is clear, the corresponding GPIO port is accessed across the legacy Advanced Peripheral Bus (APB) bus and through the APB memory aperture. When a bit is set, the corresponding port is accessed across the Advanced High-Performance Bus (AHB) bus and through the AHB memory aperture. Each GPIO port can be individually configured to use AHB or APB, but may be accessed only through one aperture. The AHB bus provides better back-to-back access performance than the APB bus. The address aperture in the memory map changes for the ports that are enabled for AHB access (see Table 10-6 on page 298).

### GPIO High-Performance Bus Control (GPIOHBCTL)

Base 0x400F.E000

Offset 0x06C

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							PORTJ	PORTH	PORTG	PORTF	PORTE	PORTD	PORTC	PORTB	PORTA
Type	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:9	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	PORTJ	R/W	0	Port J Advanced High-Performance Bus This bit defines the memory aperture for Port J.  Value Description 1 Advanced High-Performance Bus (AHB) 0 Advanced Peripheral Bus (APB). This bus is the legacy bus.
7	PORTH	R/W	0	Port H Advanced High-Performance Bus This bit defines the memory aperture for Port H.  Value Description 1 Advanced High-Performance Bus (AHB) 0 Advanced Peripheral Bus (APB). This bus is the legacy bus.
6	PORTG	R/W	0	Port G Advanced High-Performance Bus This bit defines the memory aperture for Port G.  Value Description 1 Advanced High-Performance Bus (AHB) 0 Advanced Peripheral Bus (APB). This bus is the legacy bus.



Bit/Field	Name	Type	Reset	Description
5	PORTF	R/W	0	<p>Port F Advanced High-Performance Bus</p> <p>This bit defines the memory aperture for Port F.</p> <p>Value Description</p> <p>1 Advanced High-Performance Bus (AHB)</p> <p>0 Advanced Peripheral Bus (APB). This bus is the legacy bus.</p>
4	PORTE	R/W	0	<p>Port E Advanced High-Performance Bus</p> <p>This bit defines the memory aperture for Port E.</p> <p>Value Description</p> <p>1 Advanced High-Performance Bus (AHB)</p> <p>0 Advanced Peripheral Bus (APB). This bus is the legacy bus.</p>
3	PORTD	R/W	0	<p>Port D Advanced High-Performance Bus</p> <p>This bit defines the memory aperture for Port D.</p> <p>Value Description</p> <p>1 Advanced High-Performance Bus (AHB)</p> <p>0 Advanced Peripheral Bus (APB). This bus is the legacy bus.</p>
2	PORTC	R/W	0	<p>Port C Advanced High-Performance Bus</p> <p>This bit defines the memory aperture for Port C.</p> <p>Value Description</p> <p>1 Advanced High-Performance Bus (AHB)</p> <p>0 Advanced Peripheral Bus (APB). This bus is the legacy bus.</p>
1	PORTB	R/W	0	<p>Port B Advanced High-Performance Bus</p> <p>This bit defines the memory aperture for Port B.</p> <p>Value Description</p> <p>1 Advanced High-Performance Bus (AHB)</p> <p>0 Advanced Peripheral Bus (APB). This bus is the legacy bus.</p>
0	PORTA	R/W	0	<p>Port A Advanced High-Performance Bus</p> <p>This bit defines the memory aperture for Port A.</p> <p>Value Description</p> <p>1 Advanced High-Performance Bus (AHB)</p> <p>0 Advanced Peripheral Bus (APB). This bus is the legacy bus.</p>

### Register 10: Run-Mode Clock Configuration 2 (RCC2), offset 0x070

This register overrides the **RCC** equivalent register fields, as shown in Table 6-8, when the `USERCC2` bit is set, allowing the extended capabilities of the **RCC2** register to be used while also providing a means to be backward-compatible to previous parts. Each **RCC2** field that supersedes an **RCC** field is located at the same LSB bit position; however, some **RCC2** fields are larger than the corresponding **RCC** field.

**Table 6-8. RCC2 Fields that Override RCC fields**

RCC2 Field...	Overrides RCC Field
SYSDIV2, bits[28:23]	SYSDIV, bits[26:23]
PWRDN2, bit[13]	PWRDN, bit[13]
BYPASS2, bit[11]	BYPASS, bit[11]
OSCSRC2, bits[6:4]	OSCSRC, bits[5:4]

#### Run-Mode Clock Configuration 2 (RCC2)

Base 0x400F.E000  
 Offset 0x070  
 Type R/W, reset 0x0780.6810

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	USERCC2	DIV400	reserved	SYSDIV2							SYSDIV2LSB	reserved					
Type	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved		PWRDN2	reserved	BYPASS2	reserved				OSCSRC2			reserved				
Type	RO	RO	R/W	RO	R/W	RO	RO	RO	RO	R/W	R/W	R/W	RO	RO	RO	RO	
Reset	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31	USERCC2	R/W	0	Use <b>RCC2</b>
				Value Description 1 The <b>RCC2</b> register fields override the <b>RCC</b> register fields. 0 The <b>RCC</b> register fields are used, and the fields in <b>RCC2</b> are ignored.
30	DIV400	R/W	0	Divide PLL as 400 MHz vs. 200 MHz
				This bit, along with the <code>SYSDIV2LSB</code> bit, allows additional frequency choices.  Value Description 1 Append the <code>SYSDIV2LSB</code> bit to the <code>SYSDIV2</code> field to create a 7 bit divisor using the 400 MHz PLL output, see Table 6-6 on page 90. 0 Use <code>SYSDIV2</code> as is and apply to 200 MHz predivided PLL output. See Table 6-5 on page 89 for programming guidelines.
29	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description						
28:23	SYSDIV2	R/W	0x0F	<p>System Clock Divisor 2</p> <p>Specifies which divisor is used to generate the system clock from either the PLL output or the oscillator source (depending on how the <code>BYPASS2</code> bit is configured). <code>SYSDIV2</code> is used for the divisor when both the <code>USESYSYSDIV</code> bit in the <b>RCC</b> register and the <code>USERCC2</code> bit in this register are set. See Table 6-5 on page 89 for programming guidelines.</p>						
22	SYSDIV2LSB	R/W	0	<p>Additional LSB for <code>SYSDIV2</code></p> <p>When <code>DIV400</code> is set, this bit becomes the LSB of <code>SYSDIV2</code>. If <code>DIV400</code> is clear, this bit is not used. See Table 6-5 on page 89 for programming guidelines.</p> <p>This bit can only be set or cleared when <code>DIV400</code> is set.</p>						
21:14	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
13	PWRDN2	R/W	1	<p>Power-Down PLL 2</p> <table border="0"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>The PLL is powered down.</td> </tr> <tr> <td>0</td> <td>The PLL operates normally.</td> </tr> </tbody> </table>	Value	Description	1	The PLL is powered down.	0	The PLL operates normally.
Value	Description									
1	The PLL is powered down.									
0	The PLL operates normally.									
12	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
11	BYPASS2	R/W	1	<p>PLL Bypass 2</p> <table border="0"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>The system clock is derived from the OSC source and divided by the divisor specified by <code>SYSDIV2</code>.</td> </tr> <tr> <td>0</td> <td>The system clock is the PLL output clock divided by the divisor specified by <code>SYSDIV2</code>.</td> </tr> </tbody> </table> <p>See Table 6-5 on page 89 for programming guidelines.</p> <p><b>Note:</b> The ADC must be clocked from the PLL or directly from a 16-MHz clock source to operate properly.</p>	Value	Description	1	The system clock is derived from the OSC source and divided by the divisor specified by <code>SYSDIV2</code> .	0	The system clock is the PLL output clock divided by the divisor specified by <code>SYSDIV2</code> .
Value	Description									
1	The system clock is derived from the OSC source and divided by the divisor specified by <code>SYSDIV2</code> .									
0	The system clock is the PLL output clock divided by the divisor specified by <code>SYSDIV2</code> .									
10:7	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						

Bit/Field	Name	Type	Reset	Description																
6:4	OSCSRC2	R/W	0x1	<p>Oscillator Source 2</p> <p>Selects the input source for the OSC. The values are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>MOSC Main oscillator</td> </tr> <tr> <td>0x1</td> <td>PIOSC Precision internal oscillator</td> </tr> <tr> <td>0x2</td> <td>PIOSC/4 Precision internal oscillator / 4</td> </tr> <tr> <td>0x3</td> <td>30 kHz 30-kHz internal oscillator</td> </tr> <tr> <td>0x4-0x5</td> <td>Reserved</td> </tr> <tr> <td>0x6</td> <td>4.194304 MHz 4.194304-MHz external oscillator</td> </tr> <tr> <td>0x7</td> <td>32.768 kHz 32.768-kHz external oscillator</td> </tr> </tbody> </table>	Value	Description	0x0	MOSC Main oscillator	0x1	PIOSC Precision internal oscillator	0x2	PIOSC/4 Precision internal oscillator / 4	0x3	30 kHz 30-kHz internal oscillator	0x4-0x5	Reserved	0x6	4.194304 MHz 4.194304-MHz external oscillator	0x7	32.768 kHz 32.768-kHz external oscillator
Value	Description																			
0x0	MOSC Main oscillator																			
0x1	PIOSC Precision internal oscillator																			
0x2	PIOSC/4 Precision internal oscillator / 4																			
0x3	30 kHz 30-kHz internal oscillator																			
0x4-0x5	Reserved																			
0x6	4.194304 MHz 4.194304-MHz external oscillator																			
0x7	32.768 kHz 32.768-kHz external oscillator																			
3:0	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																

## Register 11: Main Oscillator Control (MOSCCTL), offset 0x07C

This register provides the ability to enable the MOSC clock verification circuit. When enabled, this circuit monitors the frequency of the MOSC to verify that the oscillator is operating within specified limits. If the clock goes invalid after being enabled, the microcontroller issues a power-on reset and reboots to the NMI handler.

### Main Oscillator Control (MOSCCTL)

Base 0x400F.E000  
Offset 0x07C  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															CVAL
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	CVAL	R/W	0	Clock Validation for MOSC
				Value Description
				1 The MOSC monitor circuit is enabled.
				0 The MOSC monitor circuit is disabled.

## Register 12: Deep Sleep Clock Configuration (DSLPCCLKCFG), offset 0x144

This register provides configuration information for the hardware control of Deep Sleep Mode.

### Deep Sleep Clock Configuration (DSLPCCLKCFG)

Base 0x400F.E000  
 Offset 0x144  
 Type R/W, reset 0x0780.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved			DSDIVORIDE						reserved						
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						DSOSCSRC					reserved				
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description														
31:29	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.														
28:23	DSDIVORIDE	R/W	0x0F	<p>Divider Field Override</p> <p>If Deep-Sleep mode is enabled when the PLL is running, the PLL is disabled. This 6-bit field contains a system divider field that overrides the <b>SYSDIV</b> field in the <b>RCC</b> register or the <b>SYSDIV2</b> field in the <b>RCC2</b> register during Deep Sleep. This divider is applied to the source selected by the <b>DSOSCSRC</b> field.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>/1</td> </tr> <tr> <td>0x1</td> <td>/2</td> </tr> <tr> <td>0x2</td> <td>/3</td> </tr> <tr> <td>0x3</td> <td>/4</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0x3F</td> <td>/64</td> </tr> </tbody> </table>	Value	Description	0x0	/1	0x1	/2	0x2	/3	0x3	/4	...	...	0x3F	/64
Value	Description																	
0x0	/1																	
0x1	/2																	
0x2	/3																	
0x3	/4																	
...	...																	
0x3F	/64																	
22:7	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.														

Bit/Field	Name	Type	Reset	Description																
6:4	DSOSCSRC	R/W	0x0	<p>Clock Source</p> <p>Specifies the clock source during Deep-Sleep mode.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td> <p>MOSC</p> <p>Use the main oscillator as the source.</p> <p><b>Note:</b> If the PIOSC is being used as the clock reference for the PLL, the PIOSC is the clock source instead of MOSC in Deep-Sleep mode.</p> <p>If the Hibernation module 4.194304-MHz crystal is being used as the clock reference for the PLL, the 4.194304-MHz crystal is the clock source instead of MOSC in Deep-Sleep mode.</p> </td> </tr> <tr> <td>0x1</td> <td> <p>PIOSC</p> <p>Use the precision internal 16-MHz oscillator as the source.</p> <p><b>Note:</b> If the Hibernation module 4.194304-MHz crystal is being used as the clock reference for the PLL, the 4.194304-MHz crystal is the clock source instead of PIOSC in Deep-Sleep mode.</p> </td> </tr> <tr> <td>0x2</td> <td>Reserved</td> </tr> <tr> <td>0x3</td> <td> <p>30 kHz</p> <p>Use the 30-kHz internal oscillator as the source.</p> </td> </tr> <tr> <td>0x4-0x5</td> <td>Reserved</td> </tr> <tr> <td>0x6</td> <td> <p>4.194304 MHz</p> <p>Use the Hibernation module 4.194304-MHz external crystal clock as the source.</p> </td> </tr> <tr> <td>0x7</td> <td> <p>32.768 kHz</p> <p>Use the Hibernation module 32.768-kHz external oscillator as the source.</p> </td> </tr> </tbody> </table>	Value	Description	0x0	<p>MOSC</p> <p>Use the main oscillator as the source.</p> <p><b>Note:</b> If the PIOSC is being used as the clock reference for the PLL, the PIOSC is the clock source instead of MOSC in Deep-Sleep mode.</p> <p>If the Hibernation module 4.194304-MHz crystal is being used as the clock reference for the PLL, the 4.194304-MHz crystal is the clock source instead of MOSC in Deep-Sleep mode.</p>	0x1	<p>PIOSC</p> <p>Use the precision internal 16-MHz oscillator as the source.</p> <p><b>Note:</b> If the Hibernation module 4.194304-MHz crystal is being used as the clock reference for the PLL, the 4.194304-MHz crystal is the clock source instead of PIOSC in Deep-Sleep mode.</p>	0x2	Reserved	0x3	<p>30 kHz</p> <p>Use the 30-kHz internal oscillator as the source.</p>	0x4-0x5	Reserved	0x6	<p>4.194304 MHz</p> <p>Use the Hibernation module 4.194304-MHz external crystal clock as the source.</p>	0x7	<p>32.768 kHz</p> <p>Use the Hibernation module 32.768-kHz external oscillator as the source.</p>
Value	Description																			
0x0	<p>MOSC</p> <p>Use the main oscillator as the source.</p> <p><b>Note:</b> If the PIOSC is being used as the clock reference for the PLL, the PIOSC is the clock source instead of MOSC in Deep-Sleep mode.</p> <p>If the Hibernation module 4.194304-MHz crystal is being used as the clock reference for the PLL, the 4.194304-MHz crystal is the clock source instead of MOSC in Deep-Sleep mode.</p>																			
0x1	<p>PIOSC</p> <p>Use the precision internal 16-MHz oscillator as the source.</p> <p><b>Note:</b> If the Hibernation module 4.194304-MHz crystal is being used as the clock reference for the PLL, the 4.194304-MHz crystal is the clock source instead of PIOSC in Deep-Sleep mode.</p>																			
0x2	Reserved																			
0x3	<p>30 kHz</p> <p>Use the 30-kHz internal oscillator as the source.</p>																			
0x4-0x5	Reserved																			
0x6	<p>4.194304 MHz</p> <p>Use the Hibernation module 4.194304-MHz external crystal clock as the source.</p>																			
0x7	<p>32.768 kHz</p> <p>Use the Hibernation module 32.768-kHz external oscillator as the source.</p>																			
3:0	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																

### Register 13: Precision Internal Oscillator Calibration (PIOSCCAL), offset 0x150

This register provides the ability to update or recalibrate the precision internal oscillator. Note that a 32.768-kHz oscillator must be used as the Hibernation module clock source for the user to be able to calibrate the PIOSC.

#### Precision Internal Oscillator Calibration (PIOSCCAL)

Base 0x400F.E000  
 Offset 0x150  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	UTEN	reserved															
Type	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved						CAL	UPDATE	reserved	UT							
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	UTEN	R/W	0	Use User Trim Value
				Value Description
				1 The trim value in bits[6:0] of this register are used for any update trim operation.
				0 The factory calibration value is used for an update trim operation.
30:10	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9	CAL	R/W	0	Start Calibration
				Value Description
				1 Starts a new calibration of the PIOSC. Results are in the <b>PIOSCSTAT</b> register. The resulting trim value from the operation is active in the PIOSC after the calibration completes. The result overrides any previous update trim operation whether the calibration passes or fails.
				0 No action.
				This bit is auto-cleared when the calibration finishes.
8	UPDATE	R/W	0	Update Trim
				Value Description
				1 Updates the PIOSC trim value with the <b>UT</b> bit or the <b>DT</b> bit in the <b>PIOSCSTAT</b> register. Used with <b>UTEN</b> .
				0 No action.
				This bit is auto-cleared after the update.
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.



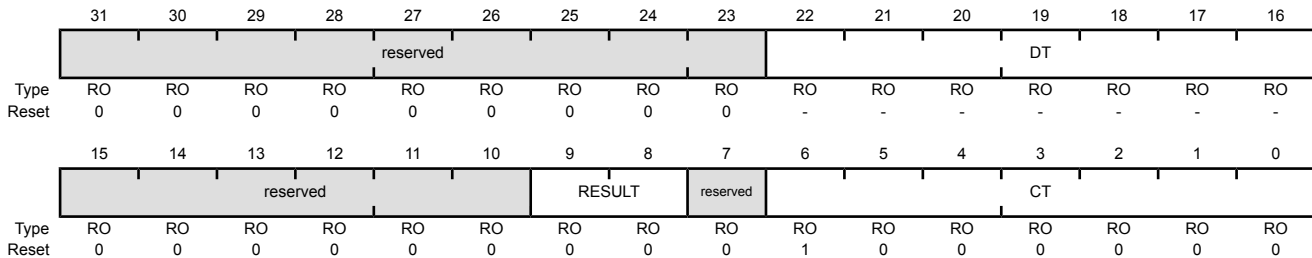
Bit/Field	Name	Type	Reset	Description
6:0	UT	R/W	0x0	User Trim Value User trim value that can be loaded into the PIOSC. Refer to "Main PLL Frequency Configuration" on page 91 for more information on calibrating the PIOSC.

### Register 14: Precision Internal Oscillator Statistics (PIOSCSTAT), offset 0x154

This register provides the user information on the PIOSC calibration. Note that a 32.768-kHz oscillator must be used as the Hibernation module clock source for the user to be able to calibrate the PIOSC.

#### Precision Internal Oscillator Statistics (PIOSCSTAT)

Base 0x400F.E000  
 Offset 0x154  
 Type RO, reset 0x0000.0040



Bit/Field	Name	Type	Reset	Description
31:23	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
22:16	DT	RO	-	Default Trim Value  This field contains the default trim value. This value is loaded into the PIOSC after every full power-up.
15:10	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9:8	RESULT	RO	0	Calibration Result  Value Description 0x0 Calibration has not been attempted. 0x1 The last calibration operation completed to meet 1% accuracy. 0x2 The last calibration operation failed to meet 1% accuracy. 0x3 Reserved
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6:0	CT	RO	0x40	Calibration Trim Value  This field contains the trim value from the last calibration operation. After factory calibration CT and DT are the same.

## Register 15: Device Identification 1 (DID1), offset 0x004

This register identifies the device family, part number, temperature range, and package type.

### Device Identification 1 (DID1)

Base 0x400F.E000

Offset 0x004

Type RO, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VER				FAM				PARTNO							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	0	0	0	0	0	0	0	1	0	1	1	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PINCOUNT			reserved				TEMP			PKG		ROHS	QUAL		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	1	0	0	0	0	0	0	-	-	-	-	-	1	-	-

Bit/Field	Name	Type	Reset	Description				
31:28	VER	RO	0x1	<p>DID1 Version</p> <p>This field defines the <b>DID1</b> register format version. The version number is numeric. The value of the <code>VER</code> field is encoded as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x1</td> <td>Second version of the <b>DID1</b> register format.</td> </tr> </tbody> </table>	Value	Description	0x1	Second version of the <b>DID1</b> register format.
Value	Description							
0x1	Second version of the <b>DID1</b> register format.							
27:24	FAM	RO	0x0	<p>Family</p> <p>This field provides the family identification of the device within the Luminary Micro product portfolio. The value is encoded as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Stellaris family of microcontrollers, that is, all devices with external part numbers starting with LM3S.</td> </tr> </tbody> </table>	Value	Description	0x0	Stellaris family of microcontrollers, that is, all devices with external part numbers starting with LM3S.
Value	Description							
0x0	Stellaris family of microcontrollers, that is, all devices with external part numbers starting with LM3S.							
23:16	PARTNO	RO	0x16	<p>Part Number</p> <p>This field provides the part number of the device within the family. The value is encoded as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x16</td> <td>LM3S1811</td> </tr> </tbody> </table>	Value	Description	0x16	LM3S1811
Value	Description							
0x16	LM3S1811							
15:13	PINCOUNT	RO	0x2	<p>Package Pin Count</p> <p>This field specifies the number of pins on the device package. The value is encoded as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x2</td> <td>100-pin package</td> </tr> </tbody> </table>	Value	Description	0x2	100-pin package
Value	Description							
0x2	100-pin package							

Bit/Field	Name	Type	Reset	Description
12:8	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:5	TEMP	RO	-	Temperature Range  This field specifies the temperature rating of the device. The value is encoded as follows (all other encodings are reserved):  Value Description 0x0 Commercial temperature range (0°C to 70°C) 0x1 Industrial temperature range (-40°C to 85°C) 0x2 Extended temperature range (-40°C to 105°C)
4:3	PKG	RO	-	Package Type  This field specifies the package type. The value is encoded as follows (all other encodings are reserved):  Value Description 0x0 SOIC package 0x1 LQFP package 0x2 BGA package
2	ROHS	RO	1	RoHS-Compliance  This bit specifies whether the device is RoHS-compliant. A 1 indicates the part is RoHS-compliant.
1:0	QUAL	RO	-	Qualification Status  This field specifies the qualification status of the device. The value is encoded as follows (all other encodings are reserved):  Value Description 0x0 Engineering Sample (unqualified) 0x1 Pilot Production (unqualified) 0x2 Fully Qualified

## Register 16: Device Capabilities 0 (DC0), offset 0x008

This register is predefined by the part and can be used to verify features.

### Device Capabilities 0 (DC0)

Base 0x400F.E000

Offset 0x008

Type RO, reset 0x007F.007F

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRAMSZ															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FLASHSZ															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:16	SRAMSZ	RO	0x007F	SRAM Size Indicates the size of the on-chip SRAM memory.  Value    Description 0x007F  32 KB of SRAM
15:0	FLASHSZ	RO	0x007F	Flash Size Indicates the size of the on-chip flash memory.  Value    Description 0x007F  256 KB of Flash

## Register 17: Device Capabilities 1 (DC1), offset 0x010

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, and DCGC0 registers cannot be set.

### Device Capabilities 1 (DC1)

Base 0x400F.E000

Offset 0x010

Type RO, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved			WDT1	reserved												ADC0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	MINSYSDIV				reserved		MAXADCOSPD	MPU	HIB	TEMPSNS	PLL	WDT0	SWO	SWD	JTAG		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		
Reset	-	-	-	-	0	0	1	1	1	1	1	1	1	1	1		

Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	WDT1	RO	1	Watchdog Timer1 Present When set, indicates that watchdog timer 1 is present.
27:17	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	ADC0	RO	1	ADC Module 0 Present When set, indicates that ADC module 0 is present
15:12	MINSYSDIV	RO	-	System Clock Divider Minimum 4-bit divider value for system clock. The reset value is hardware-dependent. See the RCC register for how to change the system clock divisor using the SYSDIV bit.  Value Description 0x1 Divide VCO (400MHZ) by 5 minimum 0x2 Divide VCO (400MHZ) by 2*2 + 2 = 6 minimum 0x3 Specifies a 50-MHz CPU clock with a PLL divider of 4. 0x7 Specifies a 25-MHz clock with a PLL divider of 8. 0x9 Specifies a 20-MHz clock with a PLL divider of 10.
11:10	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
9:8	MAXADC0SPD	RO	0x3	<p>Max ADC0 Speed</p> <p>This field indicates the maximum rate at which the ADC samples data.</p> <p>Value Description</p> <p>0x3 1M samples/second</p>
7	MPU	RO	1	<p>MPU Present</p> <p>When set, indicates that the Cortex-M3 Memory Protection Unit (MPU) module is present. See the ARM Cortex-M3 Technical Reference Manual for details on the MPU.</p>
6	HIB	RO	1	<p>Hibernation Module Present</p> <p>When set, indicates that the Hibernation module is present.</p>
5	TEMPSNS	RO	1	<p>Temp Sensor Present</p> <p>When set, indicates that the on-chip temperature sensor is present.</p>
4	PLL	RO	1	<p>PLL Present</p> <p>When set, indicates that the on-chip Phase Locked Loop (PLL) is present.</p>
3	WDT0	RO	1	<p>Watchdog Timer 0 Present</p> <p>When set, indicates that watchdog timer 0 is present.</p>
2	SWO	RO	1	<p>SWO Trace Port Present</p> <p>When set, indicates that the Serial Wire Output (SWO) trace port is present.</p>
1	SWD	RO	1	<p>SWD Present</p> <p>When set, indicates that the Serial Wire Debugger (SWD) is present.</p>
0	JTAG	RO	1	<p>JTAG Present</p> <p>When set, indicates that the JTAG debugger interface is present.</p>

## Register 18: Device Capabilities 2 (DC2), offset 0x014

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, and DCGC0 registers cannot be set.

### Device Capabilities 2 (DC2)

Base 0x400F.E000

Offset 0x014

Type RO, reset 0x430F.5037

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved	EPI0	reserved				COMP1	COMP0	reserved				TIMER3	TIMER2	TIMER1	TIMER0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	I2C1	reserved	I2C0	reserved						SSI1	SSI0	reserved	UART2	UART1	UART0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	1

Bit/Field	Name	Type	Reset	Description
31	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
30	EPI0	RO	1	EPI Module 0 Present When set, indicates that EPI module 0 is present.
29:26	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
25	COMP1	RO	1	Analog Comparator 1 Present When set, indicates that analog comparator 1 is present.
24	COMP0	RO	1	Analog Comparator 0 Present When set, indicates that analog comparator 0 is present.
23:20	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	TIMER3	RO	1	Timer Module 3 Present When set, indicates that General-Purpose Timer module 3 is present.
18	TIMER2	RO	1	Timer Module 2 Present When set, indicates that General-Purpose Timer module 2 is present.
17	TIMER1	RO	1	Timer Module 1 Present When set, indicates that General-Purpose Timer module 1 is present.
16	TIMER0	RO	1	Timer Module 0 Present When set, indicates that General-Purpose Timer module 0 is present.



Bit/Field	Name	Type	Reset	Description
15	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14	I2C1	RO	1	I2C Module 1 Present When set, indicates that I2C module 1 is present.
13	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	I2C0	RO	1	I2C Module 0 Present When set, indicates that I2C module 0 is present.
11:6	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5	SSI1	RO	1	SSI Module 1 Present When set, indicates that SSI module 1 is present.
4	SSI0	RO	1	SSI Module 0 Present When set, indicates that SSI module 0 is present.
3	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	UART2	RO	1	UART Module 2 Present When set, indicates that UART module 2 is present.
1	UART1	RO	1	UART Module 1 Present When set, indicates that UART module 1 is present.
0	UART0	RO	1	UART Module 0 Present When set, indicates that UART module 0 is present.

## Register 19: Device Capabilities 3 (DC3), offset 0x018

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, and DCGC0 registers cannot be set.

### Device Capabilities 3 (DC3)

Base 0x400F.E000  
 Offset 0x018  
 Type RO, reset 0xBFFF.0FC0

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	32KHZ	reserved	CCP5	CCP4	CCP3	CCP2	CCP1	CCP0	ADC0AIN7	ADC0AIN6	ADC0AIN5	ADC0AIN4	ADC0AIN3	ADC0AIN2	ADC0AIN1	ADC0AIN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved				C1O	C1PLUS	C1MINUS	C0O	C0PLUS	C0MINUS	reserved					
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	32KHZ	RO	1	32KHz Input Clock Available When set, indicates an even CCP pin is present and can be used as a 32-KHz input clock.
30	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
29	CCP5	RO	1	CCP5 Pin Present When set, indicates that Capture/Compare/PWM pin 5 is present.
28	CCP4	RO	1	CCP4 Pin Present When set, indicates that Capture/Compare/PWM pin 4 is present.
27	CCP3	RO	1	CCP3 Pin Present When set, indicates that Capture/Compare/PWM pin 3 is present.
26	CCP2	RO	1	CCP2 Pin Present When set, indicates that Capture/Compare/PWM pin 2 is present.
25	CCP1	RO	1	CCP1 Pin Present When set, indicates that Capture/Compare/PWM pin 1 is present.
24	CCP0	RO	1	CCP0 Pin Present When set, indicates that Capture/Compare/PWM pin 0 is present.
23	ADC0AIN7	RO	1	ADC Module 0 AIN7 Pin Present When set, indicates that ADC module 0 input pin 7 is present.
22	ADC0AIN6	RO	1	ADC Module 0 AIN6 Pin Present When set, indicates that ADC module 0 input pin 6 is present.

Bit/Field	Name	Type	Reset	Description
21	ADC0AIN5	RO	1	ADC Module 0 AIN5 Pin Present When set, indicates that ADC module 0 input pin 5 is present.
20	ADC0AIN4	RO	1	ADC Module 0 AIN4 Pin Present When set, indicates that ADC module 0 input pin 4 is present.
19	ADC0AIN3	RO	1	ADC Module 0 AIN3 Pin Present When set, indicates that ADC module 0 input pin 3 is present.
18	ADC0AIN2	RO	1	ADC Module 0 AIN2 Pin Present When set, indicates that ADC module 0 input pin 2 is present.
17	ADC0AIN1	RO	1	ADC Module 0 AIN1 Pin Present When set, indicates that ADC module 0 input pin 1 is present.
16	ADC0AIN0	RO	1	ADC Module 0 AIN0 Pin Present When set, indicates that ADC module 0 input pin 0 is present.
15:12	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	C1O	RO	1	C1o Pin Present When set, indicates that the analog comparator 1 output pin is present.
10	C1PLUS	RO	1	C1+ Pin Present When set, indicates that the analog comparator 1 (+) input pin is present.
9	C1MINUS	RO	1	C1- Pin Present When set, indicates that the analog comparator 1 (-) input pin is present.
8	C0O	RO	1	C0o Pin Present When set, indicates that the analog comparator 0 output pin is present.
7	C0PLUS	RO	1	C0+ Pin Present When set, indicates that the analog comparator 0 (+) input pin is present.
6	C0MINUS	RO	1	C0- Pin Present When set, indicates that the analog comparator 0 (-) input pin is present.
5:0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 20: Device Capabilities 4 (DC4), offset 0x01C

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, and DCGC0 registers cannot be set.

### Device Capabilities 4 (DC4)

Base 0x400F.E000

Offset 0x01C

Type RO, reset 0x0004.F1FF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved													PICAL	reserved	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCP7	CCP6	UDMA	ROM	reserved			GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GIPOD	GPIOC	GPIOB	GPIOA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:19	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
18	PICAL	RO	1	PIOSC Calibrate When set, indicates that the PIOSC can be calibrated by software.
17:16	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15	CCP7	RO	1	CCP7 Pin Present When set, indicates that Capture/Compare/PWM pin 7 is present.
14	CCP6	RO	1	CCP6 Pin Present When set, indicates that Capture/Compare/PWM pin 6 is present.
13	UDMA	RO	1	Micro-DMA Module Present When set, indicates that the micro-DMA module present.
12	ROM	RO	1	Internal Code ROM Present When set, indicates that internal code ROM is present.
11:9	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	GPIOJ	RO	1	GPIO Port J Present When set, indicates that GPIO Port J is present.
7	GPIOH	RO	1	GPIO Port H Present When set, indicates that GPIO Port H is present.

---

Bit/Field	Name	Type	Reset	Description
6	GPIOG	RO	1	GPIO Port G Present When set, indicates that GPIO Port G is present.
5	GPIOF	RO	1	GPIO Port F Present When set, indicates that GPIO Port F is present.
4	GPIOE	RO	1	GPIO Port E Present When set, indicates that GPIO Port E is present.
3	GPIOD	RO	1	GPIO Port D Present When set, indicates that GPIO Port D is present.
2	GPIOC	RO	1	GPIO Port C Present When set, indicates that GPIO Port C is present.
1	GPIOB	RO	1	GPIO Port B Present When set, indicates that GPIO Port B is present.
0	GPIOA	RO	1	GPIO Port A Present When set, indicates that GPIO Port A is present.

### Register 21: Device Capabilities 5 (DC5), offset 0x020

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, and DCGC0 registers cannot be set.

#### Device Capabilities 5 (DC5)

Base 0x400F.E000  
 Offset 0x020  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 22: Device Capabilities 6 (DC6), offset 0x024

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, and DCGC0 registers cannot be set.

### Device Capabilities 6 (DC6)

Base 0x400F.E000

Offset 0x024

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 23: Device Capabilities 7 (DC7), offset 0x028

This register is predefined by the part and can be used to verify uDMA channel features. A 1 indicates the channel is available on this device; a 0 that the channel is only available on other devices in the family. Most channels have primary and alternate assignments. If the primary function is not available on this microcontroller, the alternate function becomes the primary function. If the alternate function is not available, the primary function is the only option.

### Device Capabilities 7 (DC7)

Base 0x400F.E000  
Offset 0x028  
Type RO, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved	DMACH30	DMACH29	DMACH28	DMACH27	DMACH26	DMACH25	DMACH24	DMACH23	DMACH22	DMACH21	DMACH20	DMACH19	DMACH18	DMACH17	DMACH16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8	DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31	reserved	RO	1	Reserved  Reserved for uDMA channel 31.
30	DMACH30	RO	1	SW  When set, indicates uDMA channel 30 is available for software transfers.
29	DMACH29	RO	1	I2S0_TX / CAN1_TX  When set, indicates uDMA channel 29 is available and connected to the transmit path of I2S module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of CAN module 1 transmit.
28	DMACH28	RO	1	I2S0_RX / CAN1_RX  When set, indicates uDMA channel 28 is available and connected to the receive path of I2S module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of CAN module 1 receive.
27	DMACH27	RO	1	CAN1_TX / ADC1_SS3  When set, indicates uDMA channel 27 is available and connected to the transmit path of CAN module 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of ADC module 1 Sample Sequencer 3.
26	DMACH26	RO	1	CAN1_RX / ADC1_SS2  When set, indicates uDMA channel 26 is available and connected to the receive path of CAN module 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of ADC module 1 Sample Sequencer 2.



Bit/Field	Name	Type	Reset	Description
25	DMACH25	RO	1	SSI1_TX / ADC1_SS1 When set, indicates uDMA channel 25 is available and connected to the transmit path of SSI module 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of ADC module 1 Sample Sequencer 1.
24	DMACH24	RO	1	SSI1_RX / ADC1_SS0 When set, indicates uDMA channel 24 is available and connected to the receive path of SSI module 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of ADC module 1 Sample Sequencer 0.
23	DMACH23	RO	1	UART1_TX / CAN2_TX When set, indicates uDMA channel 23 is available and connected to the transmit path of UART module 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of CAN module 2 transmit.
22	DMACH22	RO	1	UART1_RX / CAN2_RX When set, indicates uDMA channel 22 is available and connected to the receive path of UART module 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of CAN module 2 receive.
21	DMACH21	RO	1	Timer1B / EPI0_WFIFO When set, indicates uDMA channel 21 is available and connected to Timer 1B.
20	DMACH20	RO	1	Timer1A / EPI0_NBRFIFO When set, indicates uDMA channel 20 is available and connected to Timer 1A.
19	DMACH19	RO	1	Timer0B / Timer1B When set, indicates uDMA channel 19 is available and connected to Timer 0B. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 1B.
18	DMACH18	RO	1	Timer0A / Timer1A When set, indicates uDMA channel 18 is available and connected to Timer 0A. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 1A.
17	DMACH17	RO	1	ADC0_SS3 When set, indicates uDMA channel 17 is available and connected to ADC module 0 Sample Sequencer 3.
16	DMACH16	RO	1	ADC0_SS2 When set, indicates uDMA channel 16 is available and connected to ADC module 0 Sample Sequencer 2.

Bit/Field	Name	Type	Reset	Description
15	DMACH15	RO	1	ADC0_SS1 / Timer2B When set, indicates uDMA channel 15 is available and connected to ADC module 0 Sample Sequencer 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 2B.
14	DMACH14	RO	1	ADC0_SS0 / Timer2A When set, indicates uDMA channel 14 is available and connected to ADC module 0 Sample Sequencer 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 2A.
13	DMACH13	RO	1	CAN0_TX / UART2_TX When set, indicates uDMA channel 13 is available and connected to the transmit path of CAN module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of UART module 2 transmit.
12	DMACH12	RO	1	CAN0_RX / UART2_RX When set, indicates uDMA channel 12 is available and connected to the receive path of CAN module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of UART module 2 receive.
11	DMACH11	RO	1	SSI0_TX / SSI1_TX When set, indicates uDMA channel 11 is available and connected to the transmit path of SSI module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of SSI module 1 transmit.
10	DMACH10	RO	1	SSI0_RX / SSI1_RX When set, indicates uDMA channel 10 is available and connected to the receive path of SSI module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of SSI module 1 receive.
9	DMACH9	RO	1	UART0_TX / UART1_TX When set, indicates uDMA channel 9 is available and connected to the transmit path of UART module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of UART module 1 transmit.
8	DMACH8	RO	1	UART0_RX / UART1_RX When set, indicates uDMA channel 8 is available and connected to the receive path of UART module 0. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of UART module 1 receive.
7	DMACH7	RO	1	ETH_TX / Timer2B When set, indicates uDMA channel 7 is available and connected to the transmit path of the Ethernet module. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 2B.

Bit/Field	Name	Type	Reset	Description
6	DMACH6	RO	1	ETH_RX / Timer2A When set, indicates uDMA channel 6 is available and connected to the receive path of the Ethernet module. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 2A.
5	DMACH5	RO	1	USB_EP3_TX / Timer2B When set, indicates uDMA channel 5 is available and connected to the transmit path of USB endpoint 3. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 2B.
4	DMACH4	RO	1	USB_EP3_RX / Timer2A When set, indicates uDMA channel 4 is available and connected to the receive path of USB endpoint 3. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 2A.
3	DMACH3	RO	1	USB_EP2_TX / Timer3B When set, indicates uDMA channel 3 is available and connected to the transmit path of USB endpoint 2. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 3B.
2	DMACH2	RO	1	USB_EP2_RX / Timer3A When set, indicates uDMA channel 2 is available and connected to the receive path of USB endpoint 2. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of Timer 3A.
1	DMACH1	RO	1	USB_EP1_TX / UART2_TX When set, indicates uDMA channel 1 is available and connected to the transmit path of USB endpoint 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of UART module 2 transmit.
0	DMACH0	RO	1	USB_EP1_RX / UART2_RX When set, indicates uDMA channel 0 is available and connected to the receive path of USB endpoint 1. If the corresponding bit in the <b>DMACHALT</b> register is set, the channel is connected instead to the alternate channel assignment of UART module 2 receive.

## Register 24: Device Capabilities 8 ADC Channels (DC8), offset 0x02C

This register is predefined by the part and can be used to verify features.

### Device Capabilities 8 ADC Channels (DC8)

Base 0x400F.E000  
 Offset 0x02C  
 Type RO, reset 0x0000.00FF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								ADC0AIN7	ADC0AIN6	ADC0AIN5	ADC0AIN4	ADC0AIN3	ADC0AIN2	ADC0AIN1	ADC0AIN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	ADC0AIN7	RO	1	ADC Module 0 AIN7 Pin Present When set, indicates that ADC module 0 input pin 7 is present.
6	ADC0AIN6	RO	1	ADC Module 0 AIN6 Pin Present When set, indicates that ADC module 0 input pin 6 is present.
5	ADC0AIN5	RO	1	ADC Module 0 AIN5 Pin Present When set, indicates that ADC module 0 input pin 5 is present.
4	ADC0AIN4	RO	1	ADC Module 0 AIN4 Pin Present When set, indicates that ADC module 0 input pin 4 is present.
3	ADC0AIN3	RO	1	ADC Module 0 AIN3 Pin Present When set, indicates that ADC module 0 input pin 3 is present.
2	ADC0AIN2	RO	1	ADC Module 0 AIN2 Pin Present When set, indicates that ADC module 0 input pin 2 is present.
1	ADC0AIN1	RO	1	ADC Module 0 AIN1 Pin Present When set, indicates that ADC module 0 input pin 1 is present.
0	ADC0AIN0	RO	1	ADC Module 0 AIN0 Pin Present When set, indicates that ADC module 0 input pin 0 is present.

## Register 25: Device Capabilities 9 ADC Digital Comparators (DC9), offset 0x190

This register is predefined by the part and can be used to verify features.

### Device Capabilities 9 ADC Digital Comparators (DC9)

Base 0x400F.E000

Offset 0x190

Type RO, reset 0x0000.00FF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								ADC0DC7	ADC0DC6	ADC0DC5	ADC0DC4	ADC0DC3	ADC0DC2	ADC0DC1	ADC0DC0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	ADC0DC7	RO	1	ADC0 DC7 Present When set, indicates that ADC module 0 Digital Comparator 7 is present.
6	ADC0DC6	RO	1	ADC0 DC6 Present When set, indicates that ADC module 0 Digital Comparator 6 is present.
5	ADC0DC5	RO	1	ADC0 DC5 Present When set, indicates that ADC module 0 Digital Comparator 5 is present.
4	ADC0DC4	RO	1	ADC0 DC4 Present When set, indicates that ADC module 0 Digital Comparator 4 is present.
3	ADC0DC3	RO	1	ADC0 DC3 Present When set, indicates that ADC module 0 Digital Comparator 3 is present.
2	ADC0DC2	RO	1	ADC0 DC2 Present When set, indicates that ADC module 0 Digital Comparator 2 is present.
1	ADC0DC1	RO	1	ADC0 DC1 Present When set, indicates that ADC module 0 Digital Comparator 1 is present.
0	ADC0DC0	RO	1	ADC0 DC0 Present When set, indicates that ADC module 0 Digital Comparator 0 is present.

## Register 26: Non-Volatile Memory Information (NVMSTAT), offset 0x1A0

This register is predefined by the part and can be used to verify features.

### Non-Volatile Memory Information (NVMSTAT)

Base 0x400F.E000

Offset 0x1A0

Type RO, reset 0x0000.0001

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															FWB
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	FWB	RO	1	32 Word Flash Write Buffer Active  When set, indicates that the 32 word Flash memory write buffer feature is active.

## Register 27: Run Mode Clock Gating Control Register 0 (RCGC0), offset 0x100

This register controls the clock gating logic in normal Run mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled (saving power). If the module is unlocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unlocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC0** is the clock configuration register for running operation, **SCGC0** for Sleep operation, and **DCGC0** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Run Mode Clock Gating Control Register 0 (RCGC0)

Base 0x400F.E000

Offset 0x100

Type R/W, reset 0x00000040

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved			WDT1	reserved												ADC0
Type	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved						MAXADC0SPD	reserved	HIB	reserved	WDT0	reserved					
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	R/W	RO	RO	R/W	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	WDT1	R/W	0	WDT1 Clock Gating Control  This bit controls the clock gating for the Watchdog Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
27:17	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	ADC0	R/W	0	ADC0 Clock Gating Control  This bit controls the clock gating for ADC module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
15:10	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description										
9:8	MAXADC0SPD	R/W	0	<p>ADC0 Sample Speed</p> <p>This field sets the rate at which ADC0 samples data. You cannot set the rate higher than the maximum rate. You can set the sample rate by setting the MAXADC0SPD bit as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x3</td> <td>1M samples/second</td> </tr> <tr> <td>0x2</td> <td>500K samples/second</td> </tr> <tr> <td>0x1</td> <td>250K samples/second</td> </tr> <tr> <td>0x0</td> <td>125K samples/second</td> </tr> </tbody> </table>	Value	Description	0x3	1M samples/second	0x2	500K samples/second	0x1	250K samples/second	0x0	125K samples/second
Value	Description													
0x3	1M samples/second													
0x2	500K samples/second													
0x1	250K samples/second													
0x0	125K samples/second													
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
6	HIB	R/W	1	<p>HIB Clock Gating Control</p> <p>This bit controls the clock gating for the Hibernation module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>										
5:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
3	WDT0	R/W	0	<p>WDT0 Clock Gating Control</p> <p>This bit controls the clock gating for the Watchdog Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>										
2:0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										



## Register 28: Sleep Mode Clock Gating Control Register 0 (SCGC0), offset 0x110

This register controls the clock gating logic in Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled (saving power). If the module is unlocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unlocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC0** is the clock configuration register for running operation, **SCGC0** for Sleep operation, and **DCGC0** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Sleep Mode Clock Gating Control Register 0 (SCGC0)

Base 0x400F.E000  
Offset 0x110  
Type R/W, reset 0x00000040

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved			WDT1	reserved							reserved			ADC0	
Type	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						MAXADC0SPD	reserved	HIB	reserved		WDT0	reserved			
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	R/W	RO	RO	R/W	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	WDT1	R/W	0	WDT1 Clock Gating Control  This bit controls the clock gating for Watchdog Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
27:17	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	ADC0	R/W	0	ADC0 Clock Gating Control  This bit controls the clock gating for ADC module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
15:10	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description										
9:8	MAXADC0SPD	R/W	0	<p>ADC0 Sample Speed</p> <p>This field sets the rate at which ADC module 0 samples data. You cannot set the rate higher than the maximum rate. You can set the sample rate by setting the MAXADC0SPD bit as follows (all other encodings are reserved):</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x3</td> <td>1M samples/second</td> </tr> <tr> <td>0x2</td> <td>500K samples/second</td> </tr> <tr> <td>0x1</td> <td>250K samples/second</td> </tr> <tr> <td>0x0</td> <td>125K samples/second</td> </tr> </tbody> </table>	Value	Description	0x3	1M samples/second	0x2	500K samples/second	0x1	250K samples/second	0x0	125K samples/second
Value	Description													
0x3	1M samples/second													
0x2	500K samples/second													
0x1	250K samples/second													
0x0	125K samples/second													
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
6	HIB	R/W	1	<p>HIB Clock Gating Control</p> <p>This bit controls the clock gating for the Hibernation module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>										
5:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
3	WDT0	R/W	0	<p>WDT0 Clock Gating Control</p> <p>This bit controls the clock gating for the Watchdog Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>										
2:0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										

## Register 29: Deep Sleep Mode Clock Gating Control Register 0 (DCGC0), offset 0x120

This register controls the clock gating logic in Deep-Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled (saving power). If the module is unlocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unlocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC0** is the clock configuration register for running operation, **SCGC0** for Sleep operation, and **DCGC0** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Deep Sleep Mode Clock Gating Control Register 0 (DCGC0)

Base 0x400F.E000  
Offset 0x120  
Type R/W, reset 0x00000040

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved			WDT1	reserved							reserved			ADC0	
Type	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved										HIB	reserved		WDT0	reserved	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	RO	RO	R/W	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	WDT1	R/W	0	WDT1 Clock Gating Control  This bit controls the clock gating for the Watchdog Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
27:17	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	ADC0	R/W	0	ADC0 Clock Gating Control  This bit controls the clock gating for ADC module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
15:7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
6	HIB	R/W	1	<b>HIB Clock Gating Control</b>  This bit controls the clock gating for the Hibernation module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
5:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	WDT0	R/W	0	<b>WDT0 Clock Gating Control</b>  This bit controls the clock gating for the Watchdog Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
2:0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 30: Run Mode Clock Gating Control Register 1 (RCGC1), offset 0x104

This register controls the clock gating logic in normal Run mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled (saving power). If the module is unlocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unlocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC1** is the clock configuration register for running operation, **SCGC1** for Sleep operation, and **DCGC1** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Run Mode Clock Gating Control Register 1 (RCGC1)

Base 0x400F.E000

Offset 0x104

Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved	EPI0	reserved				COMP1	COMP0	reserved				TIMER3	TIMER2	TIMER1	TIMER0
Type	RO	R/W	RO	RO	RO	RO	R/W	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	I2C1	reserved	I2C0	reserved						SSI1	SSI0	reserved	UART2	UART1	UART0
Type	RO	R/W	RO	R/W	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
30	EPI0	R/W	0	EPI0 Clock Gating  This bit controls the clock gating for EPI module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
29:26	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
25	COMP1	R/W	0	Analog Comparator 1 Clock Gating  This bit controls the clock gating for analog comparator 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
24	COMP0	R/W	0	Analog Comparator 0 Clock Gating  This bit controls the clock gating for analog comparator 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.

Bit/Field	Name	Type	Reset	Description
23:20	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	TIMER3	R/W	0	Timer 3 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 3. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
18	TIMER2	R/W	0	Timer 2 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 2. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
17	TIMER1	R/W	0	Timer 1 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
16	TIMER0	R/W	0	Timer 0 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
15	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14	I2C1	R/W	0	I2C1 Clock Gating Control  This bit controls the clock gating for I2C module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
13	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	I2C0	R/W	0	I2C0 Clock Gating Control  This bit controls the clock gating for I2C module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
11:6	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
5	SSI1	R/W	0	<p>SSI1 Clock Gating Control</p> <p>This bit controls the clock gating for SSI module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
4	SSI0	R/W	0	<p>SSI0 Clock Gating Control</p> <p>This bit controls the clock gating for SSI module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
3	reserved	RO	0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
2	UART2	R/W	0	<p>UART2 Clock Gating Control</p> <p>This bit controls the clock gating for UART module 2. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
1	UART1	R/W	0	<p>UART1 Clock Gating Control</p> <p>This bit controls the clock gating for UART module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
0	UART0	R/W	0	<p>UART0 Clock Gating Control</p> <p>This bit controls the clock gating for UART module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>

## Register 31: Sleep Mode Clock Gating Control Register 1 (SCGC1), offset 0x114

This register controls the clock gating logic in Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC1** is the clock configuration register for running operation, **SCGC1** for Sleep operation, and **DCGC1** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Sleep Mode Clock Gating Control Register 1 (SCGC1)

Base 0x400F.E000  
Offset 0x114  
Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved	EPI0	reserved			COMP1	COMP0	reserved				TIMER3	TIMER2	TIMER1	TIMER0	
Type	RO	R/W	RO	RO	RO	RO	R/W	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	I2C1	reserved	I2C0	reserved						SSI1	SSI0	reserved	UART2	UART1	UART0
Type	RO	R/W	RO	R/W	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
30	EPI0	R/W	0	EPI0 Clock Gating  This bit controls the clock gating for EPI module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
29:26	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
25	COMP1	R/W	0	Analog Comparator 1 Clock Gating  This bit controls the clock gating for analog comparator 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
24	COMP0	R/W	0	Analog Comparator 0 Clock Gating  This bit controls the clock gating for analog comparator 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.



Bit/Field	Name	Type	Reset	Description
23:20	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	TIMER3	R/W	0	Timer 3 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 3. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
18	TIMER2	R/W	0	Timer 2 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 2. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
17	TIMER1	R/W	0	Timer 1 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
16	TIMER0	R/W	0	Timer 0 Clock Gating Control  This bit controls the clock gating for General-Purpose Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
15	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14	I2C1	R/W	0	I2C1 Clock Gating Control  This bit controls the clock gating for I2C module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
13	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	I2C0	R/W	0	I2C0 Clock Gating Control  This bit controls the clock gating for I2C module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
11:6	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
5	SSI1	R/W	0	<b>SSI1 Clock Gating Control</b>  This bit controls the clock gating for SSI module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
4	SSI0	R/W	0	<b>SSI0 Clock Gating Control</b>  This bit controls the clock gating for SSI module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
3	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	UART2	R/W	0	<b>UART2 Clock Gating Control</b>  This bit controls the clock gating for UART module 2. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
1	UART1	R/W	0	<b>UART1 Clock Gating Control</b>  This bit controls the clock gating for UART module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
0	UART0	R/W	0	<b>UART0 Clock Gating Control</b>  This bit controls the clock gating for UART module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.

## Register 32: Deep-Sleep Mode Clock Gating Control Register 1 (DCGC1), offset 0x124

This register controls the clock gating logic in Deep-Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC1** is the clock configuration register for running operation, **SCGC1** for Sleep operation, and **DCGC1** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Deep-Sleep Mode Clock Gating Control Register 1 (DCGC1)

Base 0x400F.E000

Offset 0x124

Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved	EPI0	reserved				COMP1	COMP0	reserved				TIMER3	TIMER2	TIMER1	TIMER0
Type	RO	R/W	RO	RO	RO	RO	R/W	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	I2C1	reserved	I2C0	reserved						SSI1	SSI0	reserved	UART2	UART1	UART0
Type	RO	R/W	RO	R/W	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
30	EPI0	R/W	0	EPI0 Clock Gating  This bit controls the clock gating for EPI module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
29:26	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
25	COMP1	R/W	0	Analog Comparator 1 Clock Gating  This bit controls the clock gating for analog comparator 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
24	COMP0	R/W	0	Analog Comparator 0 Clock Gating  This bit controls the clock gating for analog comparator 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.

Bit/Field	Name	Type	Reset	Description
23:20	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	TIMER3	R/W	0	<p>Timer 3 Clock Gating Control</p> <p>This bit controls the clock gating for General-Purpose Timer module 3. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</p>
18	TIMER2	R/W	0	<p>Timer 2 Clock Gating Control</p> <p>This bit controls the clock gating for General-Purpose Timer module 2. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</p>
17	TIMER1	R/W	0	<p>Timer 1 Clock Gating Control</p> <p>This bit controls the clock gating for General-Purpose Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</p>
16	TIMER0	R/W	0	<p>Timer 0 Clock Gating Control</p> <p>This bit controls the clock gating for General-Purpose Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</p>
15	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14	I2C1	R/W	0	<p>I2C1 Clock Gating Control</p> <p>This bit controls the clock gating for I2C module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</p>
13	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	I2C0	R/W	0	<p>I2C0 Clock Gating Control</p> <p>This bit controls the clock gating for I2C module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</p>
11:6	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
5	SSI1	R/W	0	<p>SSI1 Clock Gating Control</p> <p>This bit controls the clock gating for SSI module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
4	SSI0	R/W	0	<p>SSI0 Clock Gating Control</p> <p>This bit controls the clock gating for SSI module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
3	reserved	RO	0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
2	UART2	R/W	0	<p>UART2 Clock Gating Control</p> <p>This bit controls the clock gating for UART module 2. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
1	UART1	R/W	0	<p>UART1 Clock Gating Control</p> <p>This bit controls the clock gating for UART module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
0	UART0	R/W	0	<p>UART0 Clock Gating Control</p> <p>This bit controls the clock gating for UART module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>

### Register 33: Run Mode Clock Gating Control Register 2 (RCGC2), offset 0x108

This register controls the clock gating logic in normal Run mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled (saving power). If the module is unlocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unlocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC2** is the clock configuration register for running operation, **SCGC2** for Sleep operation, and **DCGC2** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

#### Run Mode Clock Gating Control Register 2 (RCGC2)

Base 0x400F.E000  
Offset 0x108  
Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		UDMA	reserved				GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
Type	RO	RO	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:14	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13	UDMA	R/W	0	Micro-DMA Clock Gating Control  This bit controls the clock gating for micro-DMA. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
12:9	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	GPIOJ	R/W	0	Port J Clock Gating Control  This bit controls the clock gating for Port J. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.
7	GPIOH	R/W	0	Port H Clock Gating Control  This bit controls the clock gating for Port H. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.

Bit/Field	Name	Type	Reset	Description
6	GPIOG	R/W	0	<p>Port G Clock Gating Control</p> <p>This bit controls the clock gating for Port G. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
5	GPIOF	R/W	0	<p>Port F Clock Gating Control</p> <p>This bit controls the clock gating for Port F. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
4	GPIOE	R/W	0	<p>Port E Clock Gating Control</p> <p>Port E Clock Gating Control. This bit controls the clock gating for Port E. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
3	GPIOD	R/W	0	<p>Port D Clock Gating Control</p> <p>Port D Clock Gating Control. This bit controls the clock gating for Port D. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
2	GPIOC	R/W	0	<p>Port C Clock Gating Control</p> <p>This bit controls the clock gating for Port C. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
1	GPIOB	R/W	0	<p>Port B Clock Gating Control</p> <p>This bit controls the clock gating for Port B. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
0	GPIOA	R/W	0	<p>Port A Clock Gating Control</p> <p>This bit controls the clock gating for Port A. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>

## Register 34: Sleep Mode Clock Gating Control Register 2 (SCGC2), offset 0x118

This register controls the clock gating logic in Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC2** is the clock configuration register for running operation, **SCGC2** for Sleep operation, and **DCGC2** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Sleep Mode Clock Gating Control Register 2 (SCGC2)

Base 0x400F.E000  
Offset 0x118  
Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		UDMA	reserved				GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
Type	RO	RO	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:14	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13	UDMA	R/W	0	Micro-DMA Clock Gating Control  This bit controls the clock gating for micro-DMA. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
12:9	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	GPIOJ	R/W	0	Port J Clock Gating Control  This bit controls the clock gating for Port J. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
7	GPIOH	R/W	0	Port H Clock Gating Control  This bit controls the clock gating for Port H. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.



Bit/Field	Name	Type	Reset	Description
6	GPIOG	R/W	0	<p>Port G Clock Gating Control</p> <p>This bit controls the clock gating for Port G. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
5	GPIOF	R/W	0	<p>Port F Clock Gating Control</p> <p>This bit controls the clock gating for Port F. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
4	GPIOE	R/W	0	<p>Port E Clock Gating Control</p> <p>Port E Clock Gating Control. This bit controls the clock gating for Port E. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
3	GPIOD	R/W	0	<p>Port D Clock Gating Control</p> <p>Port D Clock Gating Control. This bit controls the clock gating for Port D. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
2	GPIOC	R/W	0	<p>Port C Clock Gating Control</p> <p>This bit controls the clock gating for Port C. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
1	GPIOB	R/W	0	<p>Port B Clock Gating Control</p> <p>This bit controls the clock gating for Port B. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
0	GPIOA	R/W	0	<p>Port A Clock Gating Control</p> <p>This bit controls the clock gating for Port A. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>

## Register 35: Deep Sleep Mode Clock Gating Control Register 2 (DCGC2), offset 0x128

This register controls the clock gating logic in Deep-Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC2** is the clock configuration register for running operation, **SCGC2** for Sleep operation, and **DCGC2** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes.

### Deep Sleep Mode Clock Gating Control Register 2 (DCGC2)

Base 0x400F.E000  
Offset 0x128  
Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		UDMA	reserved				GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
Type	RO	RO	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:14	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13	UDMA	R/W	0	Micro-DMA Clock Gating Control  This bit controls the clock gating for micro-DMA. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
12:9	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	GPIOJ	R/W	0	Port J Clock Gating Control  This bit controls the clock gating for Port J. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
7	GPIOH	R/W	0	Port H Clock Gating Control  This bit controls the clock gating for Port H. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.

Bit/Field	Name	Type	Reset	Description
6	GPIOG	R/W	0	<p>Port G Clock Gating Control</p> <p>This bit controls the clock gating for Port G. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
5	GPIOF	R/W	0	<p>Port F Clock Gating Control</p> <p>This bit controls the clock gating for Port F. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
4	GPIOE	R/W	0	<p>Port E Clock Gating Control</p> <p>Port E Clock Gating Control. This bit controls the clock gating for Port E. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
3	GPIOD	R/W	0	<p>Port D Clock Gating Control</p> <p>Port D Clock Gating Control. This bit controls the clock gating for Port D. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
2	GPIOC	R/W	0	<p>Port C Clock Gating Control</p> <p>This bit controls the clock gating for Port C. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
1	GPIOB	R/W	0	<p>Port B Clock Gating Control</p> <p>This bit controls the clock gating for Port B. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>
0	GPIOA	R/W	0	<p>Port A Clock Gating Control</p> <p>This bit controls the clock gating for Port A. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault.</p>

**Register 36: Software Reset Control 0 (SRCR0), offset 0x040**

This register allows individual modules to be reset. Writes to this register are masked by the bits in the **Device Capabilities 1 (DC1)** register.

## Software Reset Control 0 (SRCR0)

Base 0x400F.E000

Offset 0x040

Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved			WDT1	reserved												ADC0
Type	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved											HIB	reserved	WDT0	reserved		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	RO	RO	R/W	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	WDT1	R/W	0	WDT1 Reset Control  When this bit is set, Watchdog Timer module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
27:17	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	ADC0	R/W	0	ADC0 Reset Control  When this bit is set, ADC module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
15:7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6	HIB	R/W	0	HIB Reset Control  When this bit is set, the Hibernation module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
5:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	WDT0	R/W	0	WDT0 Reset Control  When this bit is set, Watchdog Timer module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.

Bit/Field	Name	Type	Reset	Description
2:0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 37: Software Reset Control 1 (SRCR1), offset 0x044

This register allows individual modules to be reset. Writes to this register are masked by the bits in the **Device Capabilities 2 (DC2)** register.

### Software Reset Control 1 (SRCR1)

Base 0x400F.E000

Offset 0x044

Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved	EPI0	reserved				COMP1	COMP0	reserved				TIMER3	TIMER2	TIMER1	TIMER0
Type	RO	R/W	RO	RO	RO	RO	R/W	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	I2C1	reserved	I2C0	reserved				SSI1	SSI0	reserved	UART2	UART1	UART0		
Type	RO	R/W	RO	R/W	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
30	EPI0	R/W	0	EPI0 Reset Control  When this bit is set, EPI module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
29:26	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
25	COMP1	R/W	0	Analog Comp 1 Reset Control  When this bit is set, Analog Comparator module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
24	COMP0	R/W	0	Analog Comp 0 Reset Control  When this bit is set, Analog Comparator module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
23:20	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	TIMER3	R/W	0	Timer 3 Reset Control  Timer 3 Reset Control. When this bit is set, General-Purpose Timer module 3 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
18	TIMER2	R/W	0	Timer 2 Reset Control  When this bit is set, General-Purpose Timer module 2 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.

Bit/Field	Name	Type	Reset	Description
17	TIMER1	R/W	0	<p>Timer 1 Reset Control</p> <p>When this bit is set, General-Purpose Timer module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>
16	TIMER0	R/W	0	<p>Timer 0 Reset Control</p> <p>When this bit is set, General-Purpose Timer module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>
15	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14	I2C1	R/W	0	<p>I2C1 Reset Control</p> <p>When this bit is set, I2C module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>
13	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	I2C0	R/W	0	<p>I2C0 Reset Control</p> <p>When this bit is set, I2C module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>
11:6	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5	SSI1	R/W	0	<p>SSI1 Reset Control</p> <p>When this bit is set, SSI module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>
4	SSI0	R/W	0	<p>SSI0 Reset Control</p> <p>When this bit is set, SSI module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>
3	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	UART2	R/W	0	<p>UART2 Reset Control</p> <p>When this bit is set, UART module 2 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>
1	UART1	R/W	0	<p>UART1 Reset Control</p> <p>When this bit is set, UART module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</p>

Bit/Field	Name	Type	Reset	Description
0	UART0	R/W	0	UART0 Reset Control  When this bit is set, UART module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.



**Register 38: Software Reset Control 2 (SRCR2), offset 0x048**

This register allows individual modules to be reset. Writes to this register are masked by the bits in the **Device Capabilities 4 (DC4)** register.

**Software Reset Control 2 (SRCR2)**

Base 0x400F.E000

Offset 0x048

Type R/W, reset 0x00000000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		UDMA	reserved				GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
Type	RO	RO	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:14	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13	UDMA	R/W	0	Micro-DMA Reset Control  When this bit is set, uDMA module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
12:9	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	GPIOJ	R/W	0	Port J Reset Control  When this bit is set, Port J module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
7	GPIOH	R/W	0	Port H Reset Control  When this bit is set, Port H module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
6	GPIOG	R/W	0	Port G Reset Control  When this bit is set, Port G module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
5	GPIOF	R/W	0	Port F Reset Control  When this bit is set, Port F module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.

Bit/Field	Name	Type	Reset	Description
4	GPIOE	R/W	0	Port E Reset Control  When this bit is set, Port E module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
3	GPIOD	R/W	0	Port D Reset Control  When this bit is set, Port D module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
2	GPIOC	R/W	0	Port C Reset Control  When this bit is set, Port C module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
1	GPIOB	R/W	0	Port B Reset Control  When this bit is set, Port B module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.
0	GPIOA	R/W	0	Port A Reset Control  When this bit is set, Port A module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.

## 7 Hibernation Module

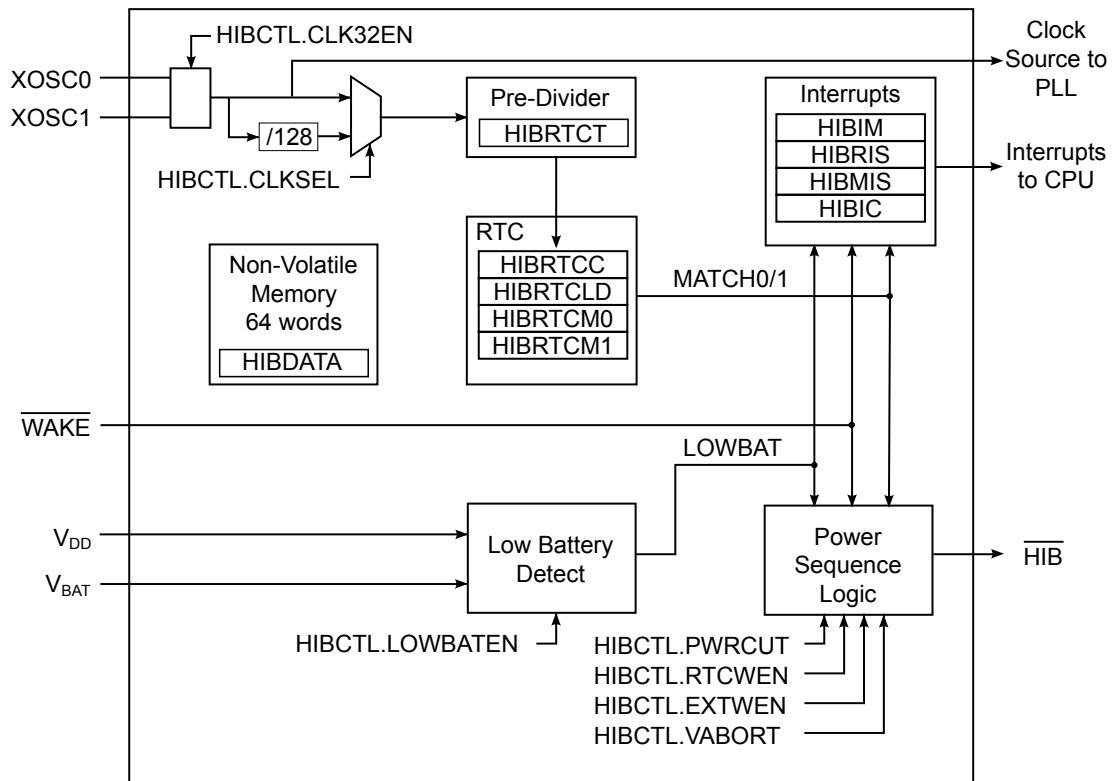
The Hibernation Module manages removal and restoration of power to provide a means for reducing power consumption. When the processor and peripherals are idle, power can be completely removed with only the Hibernation module remaining powered. Power can be restored based on an external signal or at a certain time using the built-in Real-Time Clock (RTC). The Hibernation module can be independently supplied from a battery or an auxiliary power supply.

The Hibernation module has the following features:

- Two mechanisms for power control
  - System power control using discrete external regulator
  - On-chip power control using internal switches under register control
- Dedicated pin for waking using an external signal
- Low-battery detection, signaling, and interrupt generation
- 32-bit real-time counter (RTC)
  - Two 32-bit RTC match registers for timed wake-up and interrupt generation
  - RTC predivider trim for making fine adjustments to the clock rate
- Clock source from a 32.768-kHz external oscillator or a 4.194304-MHz crystal; source can be used for main controller clock
- 64 32-bit words of non-volatile memory to save state during hibernation
- Programmable interrupts for RTC match, external wake, and low battery events

## 7.1 Block Diagram

Figure 7-1. Hibernation Module Block Diagram



## 7.2 Signal Description

Table 7-1 on page 172 lists the external signals of the Hibernation module and describes the function of each. These signals have dedicated functions and are not alternate functions for any GPIO signals.

Table 7-1. Signals for Hibernate

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
HIB	51	fixed	O	OD	An open-drain output that indicates the processor is in Hibernate mode.
VBAT	55	fixed	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
WAKE	50	fixed	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
XOSC0	52	fixed	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 4.194304-MHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC. See the CLKSEL bit in the HIBCTL register.
XOSC1	53	fixed	O	Analog	Hibernation module oscillator crystal output.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 7.3 Functional Description

**Important:** The Hibernate module must have either the RTC function or the External Wake function enabled to ensure proper operation of the microcontroller. See “Initialization” on page 177.

The Hibernation module provides two mechanisms for power control:

- The first mechanism controls the power to the microcontroller with a control signal ( $\overline{\text{HIB}}$ ) that signals an external voltage regulator to turn on or off.
- The second mechanism uses internal switches to control power to the Cortex-M3 as well as to most analog and digital functions while retaining I/O pin power (VDD3ON mode).

The Hibernation module power source is determined dynamically. The supply voltage of the Hibernation module is the larger of the main voltage source ( $V_{\text{DD}}$ ) or the battery/auxilliary voltage source ( $V_{\text{BAT}}$ ). Care must be taken that the voltage amplitude of the 32-kHz oscillator is less than  $V_{\text{BAT}}$ , otherwise, the Hibernation module draws power from the oscillator and not  $V_{\text{BAT}}$ . The Hibernation module also has a separate clock source to maintain a real-time clock (RTC). Once in hibernation, the module signals an external voltage regulator to turn back on the power when an external pin ( $\overline{\text{WAKE}}$ ) is asserted or when the internal RTC reaches a certain value. The Hibernation module can also detect when the battery voltage is low and optionally prevent hibernation when this occurs.

Power-up from a power cut to code execution is defined as the regulator turn-on time (specified at  $t_{\text{HIB\_TO\_VDD}}$  maximum) plus the normal chip POR (see “Hibernation Module” on page 735).

### 7.3.1 Register Access Timing

Because the Hibernation module has an independent clocking domain, certain registers must be written only with a timing gap between accesses. The delay time is  $t_{\text{HIB\_REG\_WRITE}}$ , therefore software must guarantee that this delay is inserted between back-to-back writes to certain Hibernation registers or between a write followed by a read to those same registers. The timing for back-to-back reads from the Hibernation module has no restrictions. Software may make use of the  $\text{WRC}$  bit in the **Hibernation Control (HIBCTL)** register to ensure that the required timing gap has elapsed. This bit is cleared on a write operation and set once the write completes, indicating to software that another write or read may be started safely. Software should poll **HIBCTL** for  $\text{WRC}=1$  prior to accessing any affected register. The following registers are subject to this timing restriction:

- **Hibernation RTC Counter (HIBRTCC)**
- **Hibernation RTC Match 0 (HIBRTCM0)**
- **Hibernation RTC Match 1 (HIBRTCM1)**
- **Hibernation RTC Load (HIBRTCLD)**
- **Hibernation RTC Trim (HIBRTCT)**
- **Hibernation Data (HIBDATA)**

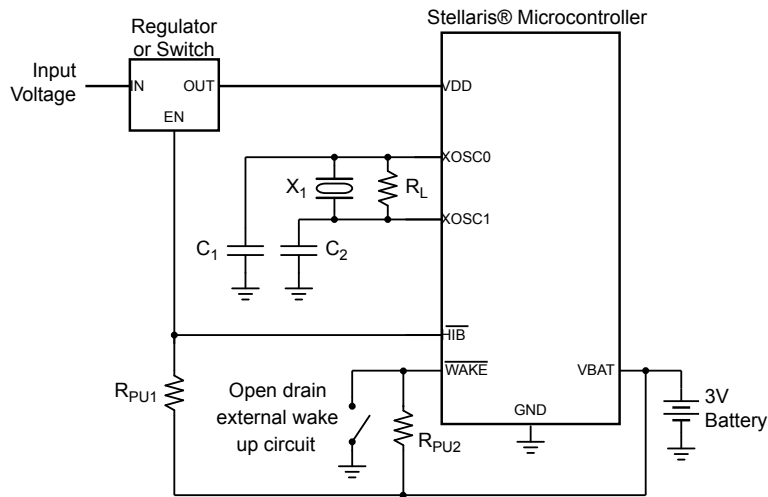
### 7.3.2 Clock Source

The Hibernation module must be clocked by an external source, even if the RTC feature is not used. An external oscillator or crystal can be used for this purpose. To use a crystal, a 4.194304-MHz crystal is connected to the  $\text{xOSC0}$  and  $\text{xOSC1}$  pins. This clock signal is divided by 128 internally to

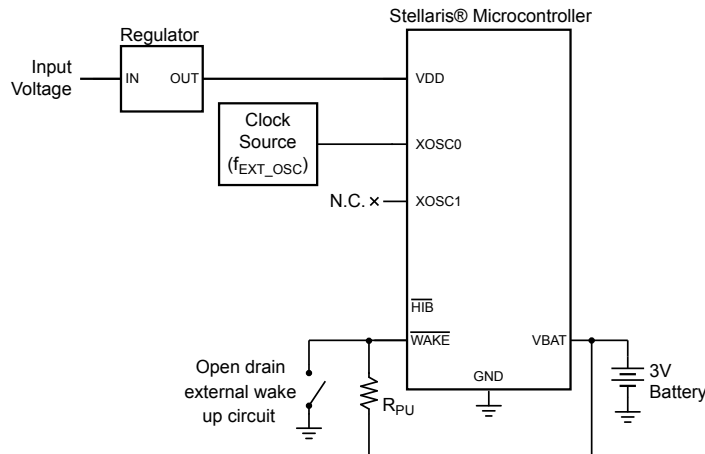
produce the 32.768-kHz clock reference. For an alternate clock source, a 32.768-kHz oscillator can be connected to the XOSC0 pin. Care must be taken that the voltage amplitude of the 32-kHz oscillator is less than  $V_{BAT}$ , otherwise, the Hibernation module draws power from the oscillator and not  $V_{BAT}$  during hibernation. See Figure 7-2 on page 174 and Figure 7-3 on page 175. Note that these diagrams only show the connection to the Hibernation pins and not to the full system. See “Hibernation Module” on page 735 for specific values.

The clock source is enabled by setting the CLK32EN bit of the HIBCTL register. The type of clock source is selected by clearing the CLKSEL bit for a 4.194304-MHz clock source and setting the CLKSEL bit for a 32.768-kHz clock source. If a crystal is used for the clock source, the software must leave a delay of  $t_{XOSC\_SETTLE}$  after writing to the CLK32EN bit and before any other accesses to the Hibernation module registers. The delay allows the crystal to power up and stabilize. If an oscillator is used for the clock source, no delay is needed.

**Figure 7-2. Clock Source Using Crystal**



- Note:**
- X<sub>1</sub> = Crystal frequency is  $f_{XOSC\_XTAL}$ .
  - C<sub>1,2</sub> = Capacitor value derived from crystal vendor load capacitance specifications.
  - R<sub>L</sub> = Load resistor is R<sub>XOSC\_LOAD</sub>.
  - R<sub>PU1</sub> = Pull-up resistor 1 (value and voltage source ( $V_{BAT}$  or Input Voltage) determined by regulator or switch enable input characteristics).
  - R<sub>PU2</sub> = Pull-up resistor 2 is 1 M $\Omega$
- See “Hibernation Module” on page 735 for specific parameter values.

**Figure 7-3. Clock Source Using Dedicated Oscillator and VDD3ON Mode**

**Note:**  $R_{PU}$  = Pull-up resistor is 1 M $\Omega$

If the application does not require the use of the Hibernation module, the XOSC0 and XOSC1 can remain unconnected. In this situation, the Hibernation module registers are not accessible.

### 7.3.3 Battery Management

The Hibernation module can be independently powered by a battery or an auxiliary power source. The module can monitor the voltage level of the battery and detect when the voltage drops below  $V_{LOWBAT}$ . When this happens, an interrupt can be generated. The module can also be configured so that it does not go into Hibernate mode if the battery voltage drops below this threshold. Battery voltage is not measured while in Hibernate mode.

**Important:** System level factors may affect the accuracy of the low battery detect circuit. The designer should consider battery type, discharge characteristics, and a test load during battery voltage measurements.

Note that the Hibernation module draws power from whichever source ( $V_{BAT}$  or  $V_{DD}$ ) has the higher voltage. Therefore, it is important to design the circuit to ensure that  $V_{DD}$  is higher than  $V_{BAT}$  under nominal conditions or else the Hibernation module draws power from the battery even when  $V_{DD}$  is available.

The Hibernation module can be configured to detect a low battery condition by setting the LOWBATEN bit of the HIBCTL register. In this configuration, the LOWBAT bit of the Hibernation Raw Interrupt Status (HIBRIS) register is set when the battery level is low. If the VABORT bit in the HIBCTL register is also set, then the module is prevented from entering Hibernation mode when a low battery is detected. The module can also be configured to generate an interrupt for the low-battery condition (see “Interrupts and Status” on page 177).

### 7.3.4 Real-Time Clock

The Hibernation module includes a 32-bit counter that increments once per second with a proper clock source and configuration (see “Clock Source” on page 173). The 32.768-kHz clock signal is fed into a predivider register that counts down the 32.768-kHz clock ticks to achieve a once per second clock rate for the RTC. The rate can be adjusted to compensate for inaccuracies in the clock source by using the predivider trim register, HIBRTCT. This register has a nominal value of 0x7FFF, and is used for one second out of every 64 seconds to divide the input clock. This configuration

allows the software to make fine corrections to the clock rate by adjusting the predivider trim register up or down from 0x7FFF. The predivider trim should be adjusted up from 0x7FFF in order to slow down the RTC rate and down from 0x7FFF in order to speed up the RTC rate.

The Hibernation module includes two 32-bit match registers that are compared to the value of the RTC counter. The match registers can be used to wake the processor from Hibernation mode or to generate an interrupt to the processor if it is not in hibernation.

The RTC must be enabled with the `RTCEN` bit of the `HIBCTL` register. The value of the RTC can be set at any time by writing to the `HIBRTCLD` register. The predivider trim can be adjusted by reading and writing the `HIBRTCT` register. The predivider uses this register once every 64 seconds to adjust the clock rate. The two match registers can be set by writing to the `HIBRTCM0` and `HIBRTCM1` registers. The RTC can be configured to generate interrupts by using the interrupt registers (see “Interrupts and Status” on page 177).

### 7.3.5 Non-Volatile Memory

The Hibernation module contains 64 32-bit words of memory that are powered from the battery or auxiliary power supply and therefore retained during hibernation. The processor software can save state information in this memory prior to hibernation and recover the state upon waking. The non-volatile memory can be accessed through the `HIBDATA` registers.

### 7.3.6 Power Control Using $\overline{\text{HIB}}$

**Important:** The Hibernation Module requires special system implementation considerations when using  $\overline{\text{HIB}}$  to control power, as it is intended to power-down all other sections of the microcontroller. All system signals and power supplies that connect to the chip must be driven to 0  $V_{\text{DC}}$  or powered down with the same regulator controlled by  $\overline{\text{HIB}}$ . See “Hibernation Module” on page 735 for more details.

The Hibernation module controls power to the microcontroller through the use of the  $\overline{\text{HIB}}$  pin which is intended to be connected to the enable signal of the external regulator(s) providing 3.3 V to the microcontroller and other circuits. When the HIB signal is asserted by the Hibernation module, the external regulator is turned off and no longer powers the microcontroller and any parts of the system that are powered by the regulator. The Hibernation module remains powered from the  $V_{\text{BAT}}$  supply (which could be a battery or an auxiliary power source) until a Wake event. Power to the microcontroller is restored by deasserting the  $\overline{\text{HIB}}$  signal, which causes the external regulator to turn power back on to the chip.

### 7.3.7 Power Control Using VDD3ON Mode

The Hibernation module may also be configured to cut power to all internal modules. In the VDD3ON mode, the regulator should maintain 3.3 V power to the microcontroller during Hibernate. This power control mode is enabled by setting the `VDD3ON` bit in `HIBCTL`.

### 7.3.8 Initiating Hibernate

Hibernation mode is initiated by the microcontroller setting the `HIBREQ` bit of the `HIBCTL` register. Prior to doing this, a wake-up condition must be configured, either from the external  $\overline{\text{WAKE}}$  pin, or by using an RTC match. If a Flash memory write operation is in progress, an interlock feature holds off the transition into Hibernation mode until the write has completed.

The Hibernation module is configured to wake from the external  $\overline{\text{WAKE}}$  pin by setting the `PINWEN` bit of the `HIBCTL` register. It is configured to wake from RTC match by setting the `RTCWEN` bit. Either



one or both of these bits must be set prior to going into hibernation. Note that the WAKE pin uses the Hibernation module's internal power supply as the logic 1 reference.

Upon either external wake-up or RTC match, the Hibernation module delays coming out of hibernation until  $V_{DD}$  is above the minimum specified voltage, see Table 22-2 on page 726.

When the Hibernation module wakes, the microcontroller performs a normal power-on reset. Software can detect that the power-on was due to a wake from hibernation by examining the raw interrupt status register (see “Interrupts and Status” on page 177) and by looking for state data in the non-volatile memory (see “Non-Volatile Memory” on page 176).

### 7.3.9 Interrupts and Status

The Hibernation module can generate interrupts when the following conditions occur:

- Assertion of  $\overline{WAKE}$  pin
- RTC match
- Low battery detected

All of the interrupts are ORed together before being sent to the interrupt controller, so the Hibernation module can only generate a single interrupt request to the controller at any given time. The software interrupt handler can service multiple interrupt events by reading the **Hibernation Masked Interrupt Status (HIBMIS)** register. Software can also read the status of the Hibernation module at any time by reading the **HIBRIS** register which shows all of the pending events. This register can be used at power-on to see if a wake condition is pending, which indicates to the software that a hibernation wake occurred.

The events that can trigger an interrupt are configured by setting the appropriate bits in the **Hibernation Interrupt Mask (HIBIM)** register. Pending interrupts can be cleared by writing the corresponding bit in the **Hibernation Interrupt Clear (HIBIC)** register.

## 7.4 Initialization and Configuration

The Hibernation module has several different configurations. The following sections show the recommended programming sequence for various scenarios. The examples below assume that a 32.768-kHz oscillator is used, and thus always set the **CLKSEL** bit of the **HIBCTL** register. If a 4.194304-MHz crystal is used instead, then the **CLKSEL** bit remains cleared. Because the Hibernation module runs at 32.768 kHz and is asynchronous to the rest of the system, software must allow a delay of  $t_{HIB\_REG\_WRITE}$  after writes to certain registers (see “Register Access Timing” on page 173). The registers that require a delay are listed in a note in “Register Map” on page 180 as well as in each register description.

### 7.4.1 Initialization

The Hibernation module comes out of reset with the system clock enabled to the module, but if the system clock to the module has been disabled, then it must be re-enabled, even if the RTC feature is not used. See page 143.

If a 4.194304-MHz crystal is used, perform the following steps:

1. Write 0x40 to the **HIBCTL** register at offset 0x10 to enable the crystal and select the divide-by-128 input path.

2. Wait for a time of  $t_{\text{HIBOSC\_SETTLE}}$  for the crystal to power up and stabilize before performing any other operations with the Hibernation module.

If a 32.678-kHz oscillator is used, then perform the following steps:

1. Write 0x44 to the **HIBCTL** register at offset 0x10 to enable the oscillator input.
2. No delay is necessary.

The above steps are only necessary when the entire system is initialized for the first time. If the microcontroller has been in hibernation, then the Hibernation module has already been powered up and the above steps are not necessary. The software can detect that the Hibernation module and clock are already powered by examining the **CLK32EN** bit of the **HIBCTL** register.

Table 7-2 on page 178 illustrates how the clocks function with various bit setting both in normal operation and in hibernation.

**Table 7-2. Hibernation Module Clock Operation**

CLK32EN	PINWEN	RTCWEN	CLKSEL	RTCEN	Result Normal Operation	Result Hibernation
0	X	X	X	X	Hibernation module disabled	Hibernation module disabled
1	0	0	0	1	RTC match capability enabled. Module clocked from 4.184304-MHz crystal.	No hibernation
1	0	0	1	1	RTC match capability enabled. Module clocked from 32.768-kHz oscillator.	No hibernation
1	0	1	X	1	Module clocked from selected source	RTC match for wake-up event
1	1	0	X	0	Module clocked from selected source	Clock is powered down during hibernation and powered up again on external wake-up event.
1	1	0	X	1	Module clocked from selected source	Clock is powered up during hibernation for RTC. Wake up on external event.
1	1	1	X	1	Module clocked from selected source	RTC match or external wake-up event, whichever occurs first.

### 7.4.2 RTC Match Functionality (No Hibernation)

Use the following steps to implement the RTC match functionality of the Hibernation module:

1. Write the required RTC match value to one of the **HIBRTCMn** registers at offset 0x004 or 0x008.
2. Write the required RTC load value to the **HIBRTCLD** register at offset 0x00C.
3. Set the required RTC match interrupt mask in the **RTCALT0** and **RTCALT1** bits (bits 1:0) in the **HIBIM** register at offset 0x014.
4. Write 0x0000.0041 to the **HIBCTL** register at offset 0x010 to enable the RTC to begin counting.

### 7.4.3 RTC Match/Wake-Up from Hibernation

Use the following steps to implement the RTC match and wake-up functionality of the Hibernation module:

1. Write the required RTC match value to the **HIBRTCMn** registers at offset 0x004 or 0x008.
2. Write the required RTC load value to the **HIBRTCLD** register at offset 0x00C.
3. Write any data to be retained during power cut to the **HIBDATA** register at offsets 0x030-0x12C.
4. Set the RTC Match Wake-Up and start the hibernation sequence by writing 0x0000.004F to the **HIBCTL** register at offset 0x010.

#### 7.4.4 External Wake-Up from Hibernation

Use the following steps to implement the Hibernation module with the external  $\overline{\text{WAKE}}$  pin as the wake-up source for the microcontroller:

1. Write any data to be retained during power cut to the **HIBDATA** register at offsets 0x030-0x12C.
2. Enable the external wake and start the hibernation sequence by writing 0x0000.0056 to the **HIBCTL** register at offset 0x010.

Note that in this mode, if the RTC is disabled, then the Hibernation clock source is powered down during Hibernation mode and is powered up again on the external wake event to save power during hibernation. If the RTC is enabled before hibernation, it will continue to operate during hibernation.

#### 7.4.5 RTC or External Wake-Up from Hibernation

1. Write the required RTC match value to the **HIBRTCMn** registers at offset 0x004 or 0x008.
2. Write the required RTC load value to the **HIBRTCLD** register at offset 0x00C.
3. Write any data to be retained during power cut to the **HIBDATA** register at offsets 0x030-0x12C.
4. Set the RTC Match/External Wake-Up and start the hibernation sequence by writing 0x0000.005F to the **HIBCTL** register at offset 0x010.

#### 7.4.6 Register Reset

The Hibernation module handles resets according to the following conditions:

- **Cold Reset**  
When the hibernation module has no externally applied voltage and detects a change to either  $V_{DD}$  or  $V_{BAT}$ , it resets all hibernation module registers to the value in Table 7-3 on page 180.
- **Reset During Hibernation Module Disable**  
When the module has either not been enabled or has been disabled by software, the reset is passed through to the Hibernation module circuitry, and the internal state of the module is reset. Non-volatile memory contents are not reset to zero and contents after reset are indeterminate.
- **Reset While Hibernation Module is in Hibernation Mode**  
While in Hibernation mode, or while transitioning from Hibernation mode to run mode (leaving the power cut), the reset generated by the POR circuitry of the microcontroller is suppressed, and the state of the Hibernation module's registers is unaffected.
- **Reset While Hibernation Module is in Normal Mode**

While in normal mode (not hibernating), any reset is suppressed if either the `RTCEN` or the `PINWEN` bit is set in the `HIBCTL` register, and the content/state of the control and data registers is unaffected.

Software must initialize any control or data registers in this condition. Therefore, software is the only mechanism to enable or disable the oscillator and real-time clock operation, or to clear contents of the data memory. The only state that must be cleared by a reset operation while not in Hibernation mode is any state that prevents software from managing the interface.

## 7.5 Register Map

Table 7-3 on page 180 lists the Hibernation registers. All addresses given are relative to the Hibernation Module base address at `0x400F.C000`. Note that the Hibernation module clock must be enabled before the registers can be programmed (see page 143).

**Note:** `HIBRTCC`, `HIBRTCM0`, `HIBRTCM1`, `HIBRTCLD`, `HIBRTCT`, and `HIBDATA` are on the Hibernation module clock domain and have special timing requirements. Software should make use of the `WRC` bit in the `HIBCTL` register to ensure that the required timing gap has elapsed. See “Register Access Timing” on page 173.

**Important:** Reset values apply only to a cold reset. Once configured, the Hibernation module ignores any system reset as long as  $V_{BAT}$  is present.

**Table 7-3. Hibernation Module Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	HIBRTCC	RO	0x0000.0000	Hibernation RTC Counter	181
0x004	HIBRTCM0	R/W	0xFFFF.FFFF	Hibernation RTC Match 0	182
0x008	HIBRTCM1	R/W	0xFFFF.FFFF	Hibernation RTC Match 1	183
0x00C	HIBRTCLD	R/W	0xFFFF.FFFF	Hibernation RTC Load	184
0x010	HIBCTL	R/W	0x8000.0000	Hibernation Control	185
0x014	HIBIM	R/W	0x0000.0000	Hibernation Interrupt Mask	188
0x018	HIBRIS	RO	0x0000.0000	Hibernation Raw Interrupt Status	190
0x01C	HIBMIS	RO	0x0000.0000	Hibernation Masked Interrupt Status	192
0x020	HIBIC	R/W1C	0x0000.0000	Hibernation Interrupt Clear	194
0x024	HIBRTCT	R/W	0x0000.7FFF	Hibernation RTC Trim	195
0x030-0x12C	HIBDATA	R/W	-	Hibernation Data	196

## 7.6 Register Descriptions

The remainder of this section lists and describes the Hibernation module registers, in numerical order by address offset.

## Register 1: Hibernation RTC Counter (HIBRTCC), offset 0x000

This register is the current 32-bit value of the RTC counter.

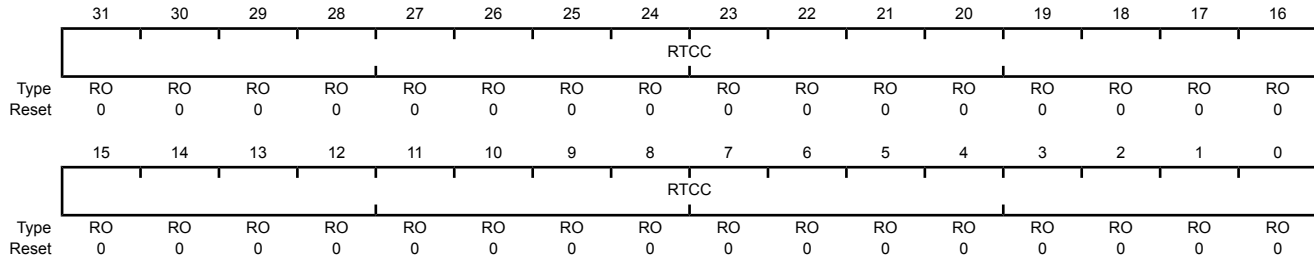
**Note:** **HIBRTCC**, **HIBRTCM0**, **HIBRTCM1**, **HIBRTCLD**, **HIBRTCT**, and **HIBDATA** are on the Hibernation module clock domain and have special timing requirements. Software should make use of the **WRC** bit in the **HIBCTL** register to ensure that the required timing gap has elapsed. See “Register Access Timing” on page 173.

### Hibernation RTC Counter (HIBRTCC)

Base 0x400F.C000

Offset 0x000

Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:0	RTCC	RO	0x0000.0000	RTC Counter

A read returns the 32-bit counter value. This register is read-only. To change the value, use the **HIBRTCLD** register.

## Register 2: Hibernation RTC Match 0 (HIBRTCM0), offset 0x004

This register is the 32-bit match 0 register for the RTC counter.

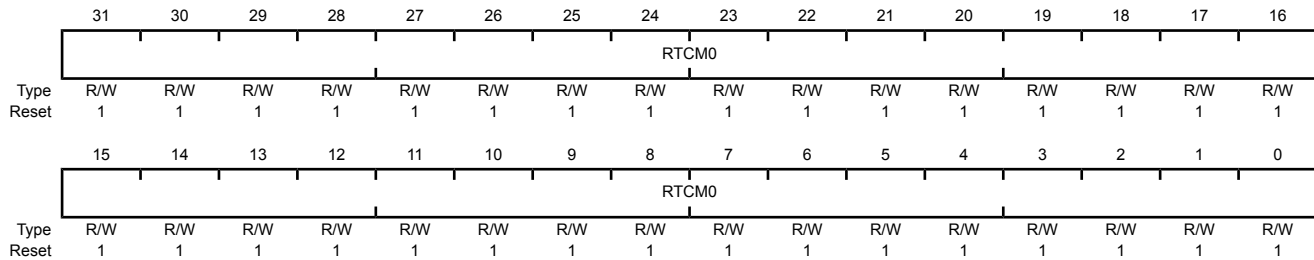
**Note:** **HIBRTCC**, **HIBRTCM0**, **HIBRTCM1**, **HIBRTCLD**, **HIBRTCT**, and **HIBDATA** are on the Hibernation module clock domain and have special timing requirements. Software should make use of the **WRC** bit in the **HIBCTL** register to ensure that the required timing gap has elapsed. See “Register Access Timing” on page 173.

### Hibernation RTC Match 0 (HIBRTCM0)

Base 0x400F.C000

Offset 0x004

Type R/W, reset 0xFFFF.FFFF



Bit/Field	Name	Type	Reset	Description
31:0	RTCM0	R/W	0xFFFF.FFFF	RTC Match 0

A write loads the value into the RTC match register.

A read returns the current match value.

**Register 3: Hibernation RTC Match 1 (HIBRTCM1), offset 0x008**

This register is the 32-bit match 1 register for the RTC counter.

**Note:** **HIBRTCC**, **HIBRTCM0**, **HIBRTCM1**, **HIBRTCLD**, **HIBRTCT**, and **HIBDATA** are on the Hibernation module clock domain and have special timing requirements. Software should make use of the **WRC** bit in the **HIBCTL** register to ensure that the required timing gap has elapsed. See “Register Access Timing” on page 173.

**Hibernation RTC Match 1 (HIBRTCM1)**

Base 0x400F.C000

Offset 0x008

Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RTCM1															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RTCM1															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	RTCM1	R/W	0xFFFF.FFFF	RTC Match 1

A write loads the value into the RTC match register.

A read returns the current match value.

### Register 4: Hibernation RTC Load (HIBRTCLD), offset 0x00C

This register is used to load a 32-bit value loaded into the RTC counter. The load occurs immediately upon this register being written.

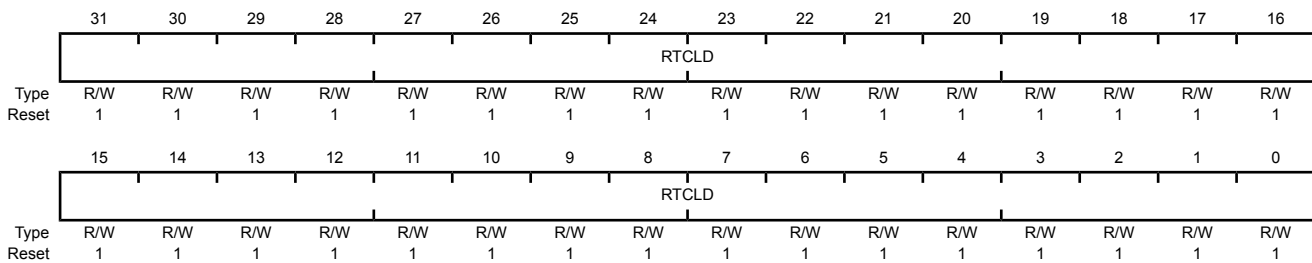
**Note:** **HIBRTCC**, **HIBRTCM0**, **HIBRTCM1**, **HIBRTCLD**, **HIBRTCT**, and **HIBDATA** are on the Hibernation module clock domain and have special timing requirements. Software should make use of the **WRC** bit in the **HIBCTL** register to ensure that the required timing gap has elapsed. See “Register Access Timing” on page 173.

#### Hibernation RTC Load (HIBRTCLD)

Base 0x400F.C000

Offset 0x00C

Type R/W, reset 0xFFFF.FFFF



Bit/Field	Name	Type	Reset	Description
31:0	RTCLD	R/W	0xFFFF.FFFF	RTC Load

A write loads the current value into the RTC counter (RTCC).

A read returns the 32-bit load value.



## Register 5: Hibernation Control (HIBCTL), offset 0x010

This register is the control register for the Hibernation module.

### Hibernation Control (HIBCTL)

Base 0x400F.C000

Offset 0x010

Type R/W, reset 0x8000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRC	reserved														
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							VDD3ON	VABORT	CLK32EN	LOWBATEN	PINWEN	RTCWEN	CLKSEL	HIBREQ	RTCEN
Type	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	WRC	RO	1	<p>Write Complete/Capable</p> <p>Value Description</p> <p>0 The interface is processing a prior write and is busy. Any write operation that is attempted while WRC is 0 results in undetermined behavior.</p> <p>1 The interface is ready to accept a write.</p> <p>Software must poll this bit between write requests and defer writes until WRC=1 to ensure proper operation.</p> <p>This difference may be exploited by software at reset time to detect which method of programming is appropriate: 0 = software delay loops required; 1 = WRC paced available.</p> <p>The bit name WRC means "Write Complete," which is the normal use of the bit (between write accesses). However, because the bit is set out-of-reset, the name can also mean "Write Capable" which simply indicates that the interface may be written to by software.</p>
30:9	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	VDD3ON	R/W	0	<p>VDD Powered</p> <p>Value Description</p> <p>1 The internal switches control the power to the on-chip modules (VDD3ON mode).</p> <p>0 The internal switches are not used. The <math>\overline{\text{HIB}}</math> signal should be used to control an external switch or regulator.</p> <p>Note that regardless of the status of the VDD3ON bit, the <math>\overline{\text{HIB}}</math> signal is asserted during Hibernate mode. Thus, when VDD3ON is set, the <math>\overline{\text{HIB}}</math> signal should not be connected to the 3.3V regulator, and the 3.3V power source should remain connected.</p>

Bit/Field	Name	Type	Reset	Description						
7	VABORT	R/W	0	<p>Power Cut Abort Enable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Power cut is aborted.</td> </tr> <tr> <td>0</td> <td>A power cut occurs during a low-battery alert.</td> </tr> </tbody> </table>	Value	Description	1	Power cut is aborted.	0	A power cut occurs during a low-battery alert.
Value	Description									
1	Power cut is aborted.									
0	A power cut occurs during a low-battery alert.									
6	CLK32EN	R/W	0	<p>Clocking Enable</p> <p>This bit must be enabled to use the Hibernation module.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>The clock source to the Hibernation module is enabled.</td> </tr> <tr> <td>0</td> <td>The clock source to the Hibernation module is disabled.</td> </tr> </tbody> </table> <p>The <b>CLKSEL</b> bit is used to select between the 4.194304-MHz crystal source and the 32.768-kHz oscillator source. If a crystal is used, then software should wait 20 ms after setting this bit to allow the crystal to power up and stabilize.</p>	Value	Description	1	The clock source to the Hibernation module is enabled.	0	The clock source to the Hibernation module is disabled.
Value	Description									
1	The clock source to the Hibernation module is enabled.									
0	The clock source to the Hibernation module is disabled.									
5	LOWBATEN	R/W	0	<p>Low Battery Monitoring Enable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Low battery voltage detection is enabled. If <math>V_{BAT} &lt; V_{LOWBAT}</math>, the <b>LOWBAT</b> bit in the <b>HIBRIS</b> register is set.</td> </tr> <tr> <td>0</td> <td>Low battery monitoring is disabled.</td> </tr> </tbody> </table>	Value	Description	1	Low battery voltage detection is enabled. If $V_{BAT} < V_{LOWBAT}$ , the <b>LOWBAT</b> bit in the <b>HIBRIS</b> register is set.	0	Low battery monitoring is disabled.
Value	Description									
1	Low battery voltage detection is enabled. If $V_{BAT} < V_{LOWBAT}$ , the <b>LOWBAT</b> bit in the <b>HIBRIS</b> register is set.									
0	Low battery monitoring is disabled.									
4	PINWEN	R/W	0	<p>External <math>\overline{WAKE}</math> Pin Enable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>An assertion of the <math>\overline{WAKE}</math> pin takes the microcontroller out of hibernation.</td> </tr> <tr> <td>0</td> <td>The status of the <math>\overline{WAKE}</math> pin has no effect on hibernation.</td> </tr> </tbody> </table>	Value	Description	1	An assertion of the $\overline{WAKE}$ pin takes the microcontroller out of hibernation.	0	The status of the $\overline{WAKE}$ pin has no effect on hibernation.
Value	Description									
1	An assertion of the $\overline{WAKE}$ pin takes the microcontroller out of hibernation.									
0	The status of the $\overline{WAKE}$ pin has no effect on hibernation.									
3	RTCWEN	R/W	0	<p>RTC Wake-up Enable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>An RTC match event (the value the <b>HIBRTCC</b> register matches the value of the <b>HIBRTCM0</b> or <b>HIBRTCM1</b> register) takes the microcontroller out of hibernation.</td> </tr> <tr> <td>0</td> <td>An RTC match event has no effect on hibernation.</td> </tr> </tbody> </table>	Value	Description	1	An RTC match event (the value the <b>HIBRTCC</b> register matches the value of the <b>HIBRTCM0</b> or <b>HIBRTCM1</b> register) takes the microcontroller out of hibernation.	0	An RTC match event has no effect on hibernation.
Value	Description									
1	An RTC match event (the value the <b>HIBRTCC</b> register matches the value of the <b>HIBRTCM0</b> or <b>HIBRTCM1</b> register) takes the microcontroller out of hibernation.									
0	An RTC match event has no effect on hibernation.									
2	CLKSEL	R/W	0	<p>Hibernation Module Clock Select</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Use raw output. Use this value for a 32.768-kHz oscillator.</td> </tr> <tr> <td>0</td> <td>Use Divide-by-128 output. Use this value for a 4.194304-MHz crystal.</td> </tr> </tbody> </table>	Value	Description	1	Use raw output. Use this value for a 32.768-kHz oscillator.	0	Use Divide-by-128 output. Use this value for a 4.194304-MHz crystal.
Value	Description									
1	Use raw output. Use this value for a 32.768-kHz oscillator.									
0	Use Divide-by-128 output. Use this value for a 4.194304-MHz crystal.									

Bit/Field	Name	Type	Reset	Description						
1	HIBREQ	R/W	0	<p>Hibernation Request</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Set this bit to initiate hibernation.</td> </tr> <tr> <td>0</td> <td>No hibernation request.</td> </tr> </tbody> </table> <p>After a wake-up event, this bit is automatically cleared by hardware.</p>	Value	Description	1	Set this bit to initiate hibernation.	0	No hibernation request.
Value	Description									
1	Set this bit to initiate hibernation.									
0	No hibernation request.									
0	RTCEN	R/W	0	<p>RTC Timer Enable</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>The Hibernation module RTC is enabled. The RTC remains active during hibernation.</td> </tr> <tr> <td>0</td> <td>The Hibernation module RTC is disabled. If PINWEN is set, enabling an external wake event, the RTC stops during hibernation to save power.</td> </tr> </tbody> </table>	Value	Description	1	The Hibernation module RTC is enabled. The RTC remains active during hibernation.	0	The Hibernation module RTC is disabled. If PINWEN is set, enabling an external wake event, the RTC stops during hibernation to save power.
Value	Description									
1	The Hibernation module RTC is enabled. The RTC remains active during hibernation.									
0	The Hibernation module RTC is disabled. If PINWEN is set, enabling an external wake event, the RTC stops during hibernation to save power.									

### Register 6: Hibernation Interrupt Mask (HIBIM), offset 0x014

This register is the interrupt mask register for the Hibernation module interrupt sources. Each bit in this register masks the corresponding bit in the **Hibernation Raw Interrupt Status (HIBRIS)** register. If a bit is unmasked, the interrupt is sent to the interrupt controller. If the bit is masked, the interrupt is not sent to the interrupt controller.

#### Hibernation Interrupt Mask (HIBIM)

Base 0x400F.C000  
 Offset 0x014  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												EXTW	LOWBAT	RTCALT1	RTCALT0	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	EXTW	R/W	0	External Wake-Up Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <b>EXTW</b> bit in the <b>HIBRIS</b> register is set. 0 The <b>EXTW</b> interrupt is suppressed and not sent to the interrupt controller.
2	LOWBAT	R/W	0	Low Battery Voltage Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <b>LOWBAT</b> bit in the <b>HIBRIS</b> register is set. 0 The <b>LOWBAT</b> interrupt is suppressed and not sent to the interrupt controller.
1	RTCALT1	R/W	0	RTC Alert 1 Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <b>RTCALT1</b> bit in the <b>HIBRIS</b> register is set. 0 The <b>RTCALT1</b> interrupt is suppressed and not sent to the interrupt controller.

---

Bit/Field	Name	Type	Reset	Description
0	RTCALTO	R/W	0	RTC Alert 0 Interrupt Mask
				Value Description
				1 An interrupt is sent to the interrupt controller when the RTCALTO bit in the <b>HIBRIS</b> register is set.
				0 The RTCALTO interrupt is suppressed and not sent to the interrupt controller.

### Register 7: Hibernation Raw Interrupt Status (HIBRIS), offset 0x018

This register is the raw interrupt status for the Hibernation module interrupt sources. Each bit can be masked by clearing the corresponding bit in the **HIBIM** register. When a bit is masked, the interrupt is not sent to the interrupt controller. Bits in this register are cleared by writing a 1 to the corresponding bit in the **Hibernation Interrupt Clear (HIBIC)** register.

#### Hibernation Raw Interrupt Status (HIBRIS)

Base 0x400F.C000  
 Offset 0x018  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													EXTW	LOWBAT	RTCAL1	RTCAL0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	EXTW	RO	0	External Wake-Up Raw Interrupt Status  Value Description 1 The $\overline{\text{WAKE}}$ pin has been asserted. 0 The $\overline{\text{WAKE}}$ pin has not been asserted.  This bit is cleared by writing a 1 to the <b>EXTW</b> bit in the <b>HIBIC</b> register.
2	LOWBAT	RO	0	Low Battery Voltage Raw Interrupt Status  Value Description 1 The battery voltage dropped below $V_{\text{LOWBAT}}$ . 0 The battery voltage has not dropped below $V_{\text{LOWBAT}}$ .  This bit is cleared by writing a 1 to the <b>LOWBAT</b> bit in the <b>HIBIC</b> register.
1	RTCAL1	RO	0	RTC Alert 1 Raw Interrupt Status  Value Description 1 The value of the <b>HIBRTCC</b> register matches the value in the <b>HIBRTCM1</b> register. 0 No match  This bit is cleared by writing a 1 to the <b>RTCAL1</b> bit in the <b>HIBIC</b> register.

---

Bit/Field	Name	Type	Reset	Description
0	RTCALTO	RO	0	RTC Alert 0 Raw Interrupt Status
				Value Description
			1	The value of the <b>HIBRTCC</b> register matches the value in the <b>HIBRTCM0</b> register.
			0	No match
				This bit is cleared by writing a 1 to the <b>RTCALTO</b> bit in the <b>HIBIC</b> register.

### Register 8: Hibernation Masked Interrupt Status (HIBMIS), offset 0x01C

This register is the masked interrupt status for the Hibernation module interrupt sources. Bits in this register are the AND of the corresponding bits in the **HIBRIS** and **HIBIM** registers. When both corresponding bits are set, the bit in this register is set, and the interrupt is sent to the interrupt controller.

#### Hibernation Masked Interrupt Status (HIBMIS)

Base 0x400F.C000  
 Offset 0x01C  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												EXTW	LOWBAT	RTCALT1	RTCALT0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	EXTW	RO	0	External Wake-Up Masked Interrupt Status  Value Description 1 An unmasked interrupt was signaled due to a <u>WAKE</u> pin assertion. 0 An external wake-up interrupt has not occurred.  This bit is cleared by writing a 1 to the <b>EXTW</b> bit in the <b>HIBIC</b> register.
2	LOWBAT	RO	0	Low Battery Voltage Masked Interrupt Status  Value Description 1 An unmasked interrupt was signaled due to a low battery voltage condition. 0 A low battery voltage interrupt has not occurred.  This bit is cleared by writing a 1 to the <b>LOWBAT</b> bit in the <b>HIBIC</b> register.
1	RTCALT1	RO	0	RTC Alert 1 Masked Interrupt Status  Value Description 1 An unmasked interrupt was signaled due to a low battery voltage condition. 0 A low battery voltage interrupt has not occurred.  When this bit is set, an RTC match 1 interrupt is sent to the interrupt controller.



Bit/Field	Name	Type	Reset	Description
0	RTCALTO	RO	0	RTC Alert 0 Masked Interrupt Status When this bit is set, an RTC match 0 interrupt is sent to the interrupt controller.

### Register 9: Hibernation Interrupt Clear (HIBIC), offset 0x020

This register is the interrupt write-one-to-clear register for the Hibernation module interrupt sources. Writing a 1 to a bit clears the corresponding interrupt in the **HIBRIS** register.

#### Hibernation Interrupt Clear (HIBIC)

Base 0x400F.C000

Offset 0x020

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												EXTW	LOWBAT	RTCALT1	RTCALT0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	EXTW	R/W1C	0	External Wake-Up Masked Interrupt Clear  Writing a 1 to this bit clears the <b>EXTW</b> bit in the <b>HIBRIS</b> and <b>HIBMIS</b> registers.  Reads return an indeterminate value.
2	LOWBAT	R/W1C	0	Low Battery Voltage Masked Interrupt Clear  Writing a 1 to this bit clears the <b>LOWBAT</b> bit in the <b>HIBRIS</b> and <b>HIBMIS</b> registers.  Reads return an indeterminate value.
1	RTCALT1	R/W1C	0	RTC Alert1 Masked Interrupt Clear  Writing a 1 to this bit clears the <b>RTCALT1</b> bit in the <b>HIBRIS</b> and <b>HIBMIS</b> registers.  Reads return an indeterminate value.
0	RTCALT0	R/W1C	0	RTC Alert0 Masked Interrupt Clear  Writing a 1 to this bit clears the <b>RTCALT0</b> bit in the <b>HIBRIS</b> and <b>HIBMIS</b> registers.  Reads return an indeterminate value.

## Register 10: Hibernation RTC Trim (HIBRTCT), offset 0x024

This register contains the value that is used to trim the RTC clock predivider. It represents the computed underflow value that is used during the trim cycle. It is represented as  $0x7FFF \pm N$  clock cycles, where N is the number of clock cycles to add or subtract every 63 seconds.

**Note:** **HIBRTCC**, **HIBRTCM0**, **HIBRTCM1**, **HIBRTCLD**, **HIBRTCT**, and **HIBDATA** are on the Hibernation module clock domain and have special timing requirements. Software should make use of the **WRC** bit in the **HIBCTL** register to ensure that the required timing gap has elapsed. See “Register Access Timing” on page 173.

### Hibernation RTC Trim (HIBRTCT)

Base 0x400F.C000

Offset 0x024

Type R/W, reset 0x0000.7FFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRIM															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	TRIM	R/W	0x7FFF	RTC Trim Value  This value is loaded into the RTC predivider every 64 seconds. It is used to adjust the RTC rate to account for drift and inaccuracy in the clock source. Compensation can be adjusted by software by moving the default value of 0x7FFF up or down. Moving the value up slows down the RTC and moving the value down speeds up the RTC.

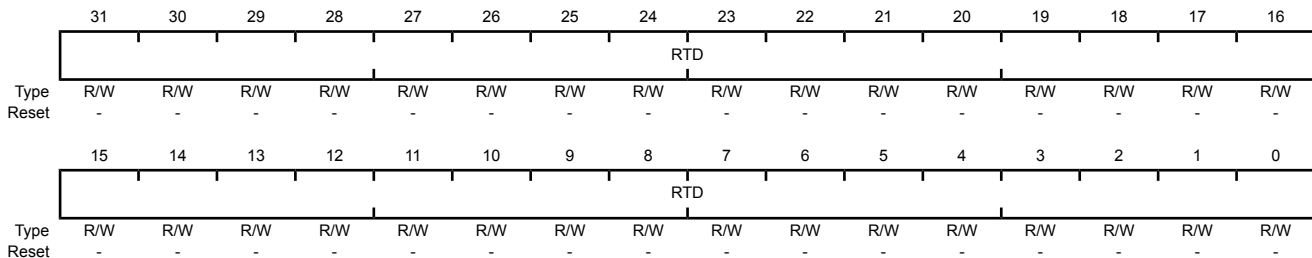
**Register 11: Hibernation Data (HIBDATA), offset 0x030-0x12C**

This address space is implemented as a 64x32-bit memory (256 bytes). It can be loaded by the system processor in order to store any non-volatile state data and does not lose power during a power cut operation.

**Note:** **HIBRTCC**, **HIBRTCM0**, **HIBRTCM1**, **HIBRTCLD**, **HIBRTCT**, and **HIBDATA** are on the Hibernation module clock domain and have special timing requirements. Software should make use of the **WRC** bit in the **HIBCTL** register to ensure that the required timing gap has elapsed. See “Register Access Timing” on page 173.

Hibernation Data (HIBDATA)

Base 0x400F.C000  
 Offset 0x030-0x12C  
 Type R/W, reset -



Bit/Field	Name	Type	Reset	Description
31:0	RTD	R/W	-	Hibernation Module NV Data

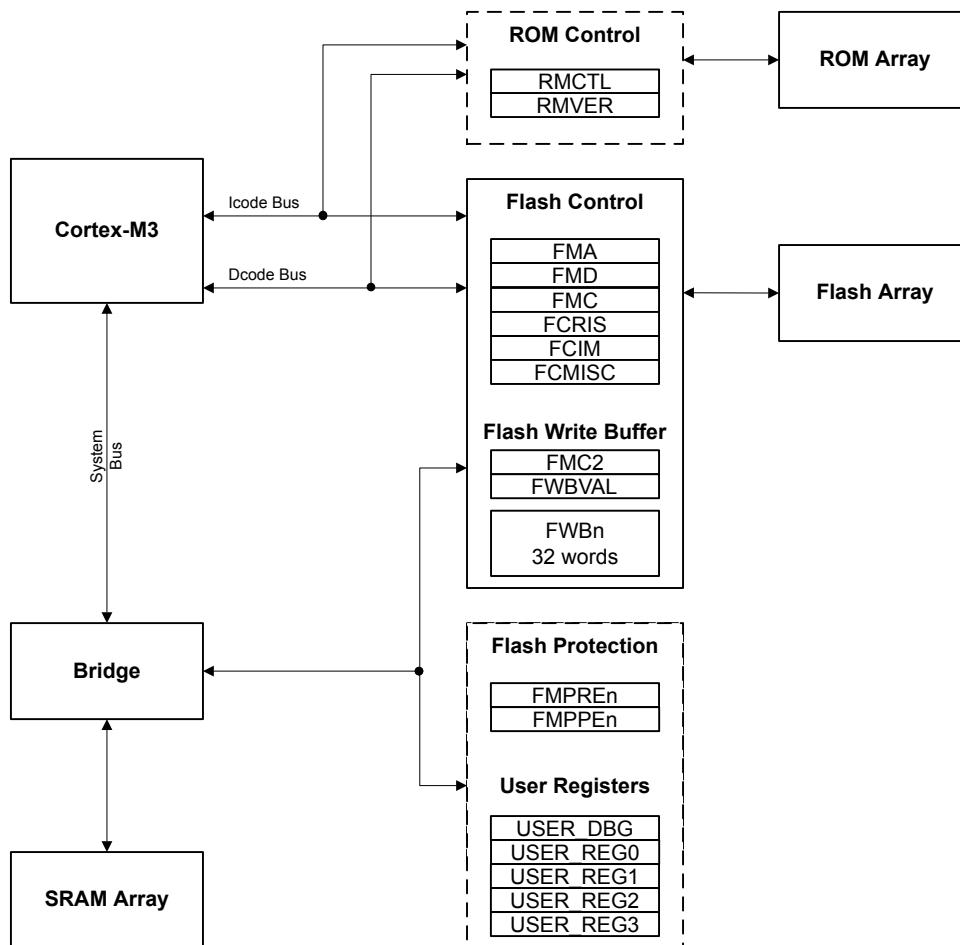
## 8 Internal Memory

The LM3S1811 microcontroller comes with 32 KB of bit-banded SRAM, internal ROM, and 256 KB of Flash memory. The Flash memory controller provides a user-friendly interface, making Flash memory programming a simple task. Flash memory protection can be applied to the Flash memory on a 2-KB block basis.

### 8.1 Block Diagram

Figure 8-1 on page 197 illustrates the internal memory blocks and control logic. The dashed boxes in the figure indicate registers residing in the System Control module.

Figure 8-1. Internal Memory Block Diagram



### 8.2 Functional Description

This section describes the functionality of the SRAM, ROM, and Flash memories.

**Note:** The  $\mu$ DMA controller can transfer data to and from the on-chip SRAM. However, because the Flash memory and ROM are located on a separate internal bus, it is not possible to transfer data from the Flash memory or ROM with the  $\mu$ DMA controller.

## 8.2.1 SRAM

**Note:** The SRAM is implemented using two 32-bit wide SRAM banks (separate SRAM arrays). The banks are partitioned such that one bank contains all even words (the even bank) and the other contains all odd words (the odd bank). A write access that is followed immediately by a read access to the same bank incurs a stall of a single clock cycle. However, a write to one bank followed by a read of the other bank can occur in successive clock cycles without incurring any delay.

The internal SRAM of the Stellaris<sup>®</sup> devices is located at address 0x2000.0000 of the device memory map. To reduce the number of time consuming read-modify-write (RMW) operations, ARM has introduced *bit-banding* technology in the Cortex-M3 processor. With a bit-band-enabled processor, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation. The bit-band base is located at address 0x2200.0000.

The bit-band alias is calculated by using the formula:

$$\text{bit-band alias} = \text{bit-band base} + (\text{byte offset} * 32) + (\text{bit number} * 4)$$

For example, if bit 3 at address 0x2000.1000 is to be modified, the bit-band alias is calculated as:

$$0x2200.0000 + (0x1000 * 32) + (3 * 4) = 0x2202.000C$$

With the alias address calculated, an instruction performing a read/write to address 0x2202.000C allows direct access to only bit 3 of the byte at address 0x2000.1000.

For details about bit-banding, please refer to Chapter 4, “Memory Map” in the *ARM<sup>®</sup> Cortex<sup>™</sup>-M3 Technical Reference Manual*.

## 8.2.2 ROM

The internal ROM of the Stellaris<sup>®</sup> device is located at address 0x0100.0000 of the device memory map. The ROM contains the following components:

- Stellaris<sup>®</sup> Boot Loader and vector table (see “Boot Loader” on page 746)
- Stellaris<sup>®</sup> Peripheral Driver Library (DriverLib) release for product-specific peripherals and interfaces (see “ROM DriverLib Functions” on page 751)

## 8.2.3 Flash Memory

The Flash memory is organized as a set of 1-KB blocks that can be individually erased. An individual 32-bit word can be programmed to change bits from 1 to 0. In addition, a write buffer provides the ability to concurrently program 32 continuous words in Flash memory. Erasing a block causes the entire contents of the block to be reset to all 1s. The 1-KB blocks are paired into sets of 2-KB blocks that can be individually protected. The protection allows blocks to be marked as read-only or execute-only, providing different levels of code protection. Read-only blocks cannot be erased or programmed, protecting the contents of those blocks from being modified. Execute-only blocks cannot be erased or programmed and can only be read by the controller instruction fetch mechanism, protecting the contents of those blocks from being read by either the controller or by a debugger.

---

**Caution – In systems where power might be cycled more frequently than every five minutes, power must be removed from the microcontroller in a controlled manner to ensure proper operation. Software must request permission to power down the part using the USDREQ bit in the Flash Control (FCTL) register and wait to receive an acknowledge from the USDACK bit prior to removing power.**

**Note that this power-down process is not required if the microcontroller enters hibernation mode prior to power being removed.**

---

### 8.2.3.1 Flash Memory Protection

The user is provided two forms of Flash memory protection per 2-KB Flash memory block in four pairs of 32-bit wide registers. The policy for each protection form is controlled by individual bits (per policy per block) in the **FMPPEn** and **FMPREn** registers.

- **Flash Memory Protection Program Enable (FMPPEn)**: If a bit is set, the corresponding block may be programmed (written) or erased. If a bit is cleared, the corresponding block may not be changed.
- **Flash Memory Protection Read Enable (FMPREn)**: If a bit is set, the corresponding block may be executed or read by software or debuggers. If a bit is cleared, the corresponding block may only be executed, and contents of the memory block are prohibited from being accessed as data.

The policies may be combined as shown in Table 8-1 on page 199.

**Table 8-1. Flash Memory Protection Policy Combinations**

FMPPEn	FMPREn	Protection
0	0	Execute-only protection. The block may only be executed and may not be written or erased. This mode is used to protect code.
1	0	The block may be written, erased or executed, but not read. This combination is unlikely to be used.
0	1	Read-only protection. The block may be read or executed but may not be written or erased. This mode is used to lock the block from further modification while allowing any read or execute access.
1	1	No protection. The block may be written, erased, executed or read.

An access that attempts to program or erase a program-protected block is prohibited. An access that attempts to read a read-protected block is prohibited. Such accesses return data of all 0s. A controller interrupt may be optionally generated whenever an attempt is made to improperly access the Flash memory (by setting the **AMASK** bit in the **Flash Controller Interrupt Mask (FCIM)** register) to alert software developers of poorly behaving software during the development and debug phases.

The factory settings for the **FMPREn** and **FMPPEn** registers are a value of 1 for all implemented banks. These settings create a policy of open access and programmability. The register bits may be changed by clearing the specific register bit. The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The changes are committed using the **Flash Memory Control (FMC)** register. Details on programming these bits are discussed in “Nonvolatile Register Programming” on page 201.

## 8.3 Flash Memory Initialization and Configuration

### 8.3.1 Flash Memory Programming

The Stellaris® devices provide a user-friendly interface for Flash memory programming. All erase/program operations are handled via three registers: **Flash Memory Address (FMA)**, **Flash Memory Data (FMD)**, and **Flash Memory Control (FMC)**. Note that if the debug capabilities of the microcontroller have been deactivated, resulting in a "locked" state, a recovery sequence must be performed in order to reactivate the debug module. See “Recovering a "Locked" Microcontroller” on page 73.

**Caution** – The Flash memory is divided into sectors of electrically separated address ranges of 4 KB each, aligned on 4 KB boundaries. Erase/program operations on a 1-KB page have an electrical effect on the other three 1-KB pages within the sector. A specific 1-KB page must be erased after 6 total erase/program cycles occur to the other pages within its 4-KB sector. The following sequence of operations on a 4-KB sector of Flash memory (Page 0..3) provides an example:

- Page 3 is erase and programmed with values.
  - Page 0, Page 1, and Page 2 are erased and then programmed with values. At this point Page 3 has been affected by 3 erase/program cycles.
  - Page 0, Page 1, and Page 2 are again erased and then programmed with values. At this point Page 3 has been affected by 6 erase/program cycles.
  - If the contents of Page 3 must continue to be valid, Page 3 must be erased and reprogrammed before any other page in this sector has another erase or program operation.
- 

### 8.3.1.1 To program a 32-bit word

1. Write source data to the **FMD** register.
  2. Write the target address to the **FMA** register.
  3. Write the Flash memory write key and the **WRITE** bit (a value of 0xA442.0001) to the **FMC** register.
  4. Poll the **FMC** register until the **WRITE** bit is cleared.
- 

**Important:** To ensure proper operation, two writes to the same word must be separated by an **ERASE**. The following two sequences are allowed:

- ERASE -> PROGRAM value -> PROGRAM 0x0000.0000
- ERASE -> PROGRAM value -> ERASE

The following sequence is NOT allowed:

- ERASE -> PROGRAM value -> PROGRAM value
- 

### 8.3.1.2 To perform an erase of a 1-KB page

1. Write the page address to the **FMA** register.
2. Write the Flash memory write key and the **ERASE** bit (a value of 0xA442.0002) to the **FMC** register.
3. Poll the **FMC** register until the **ERASE** bit is cleared.

### 8.3.1.3 To perform a mass erase of the Flash memory

1. Write the Flash memory write key and the **MERASE** bit (a value of 0xA442.0004) to the **FMC** register.



2. Poll the **FMC** register until the `MERASE` bit is cleared.

### 8.3.2 32-Word Flash Memory Write Buffer

A 32-word write buffer provides the capability to perform faster write accesses to the Flash memory by concurrently programming 32 words with a single buffered Flash memory write operation. The buffered Flash memory write operation takes the same amount of time as the single word write operation controlled by bit 0 in the **FMC** register. The data for the buffered write is written to the **Flash Write Buffer (FWBn)** registers.

The registers are 32-word aligned with Flash memory, and therefore the register **FWB0** corresponds with the address in **FMA** where bits [6:0] of **FMA** are all 0. **FWB1** corresponds with the address in **FMA** + 0x4 and so on. Only the **FWBn** registers that have been updated since the previous buffered Flash memory write operation are written. The **Flash Write Buffer Valid (FWBVAL)** register shows which registers have been written since the last buffered Flash memory write operation. This register contains a bit for each of the 32 **FWBn** registers, where bit[n] of **FWBVAL** corresponds to **FWBn**. The **FWBn** register has been updated if the corresponding bit in the **FWBVAL** register is set.

#### 8.3.2.1 To program 32 words with a single buffered Flash memory write operation

1. Write the source data to the **FWBn** registers.
2. Write the target address to the **FMA** register. This must be a 32-word aligned address (that is, bits [6:0] in **FMA** must be 0s).
3. Write the Flash memory write key and the `WRBUF` bit (a value of 0xA442.0001) to the **FMC2** register.
4. Poll the **FMC2** register until the `WRBUF` bit is cleared.

### 8.3.3 Nonvolatile Register Programming

This section discusses how to update registers that are resident within the Flash memory itself. These registers exist in a separate space from the main Flash memory array and are not affected by an `ERASE` or `MASS ERASE` operation. The bits in these registers can be changed from 1 to 0 with a write operation. The register contents are unaffected by any reset condition except power-on reset, which returns the register contents to 0xFFFF.FFFF. By committing the register values using the `COMT` bit in the **FMC** register, the register contents become nonvolatile and are therefore retained following power cycling. Once the register contents are committed, the only way to restore the factory default values is to perform the sequence described in "Recovering a "Locked" Microcontroller" on page 73.

With the exception of the **USER\_DBG** register, the settings in these registers can be tested before committing them to Flash memory. For the **USER\_DBG** register, the data to be written is loaded into the **FMD** register before it is committed. The **FMD** register is read only and does not allow the **USER\_DBG** operation to be tried before committing it to nonvolatile memory.

---

**Important:** The Flash memory resident registers can only have bits changed from 1 to 0 by user programming and can only be committed once. After being committed, these registers can only be restored to their factory default values only by performing the sequence described in "Recovering a "Locked" Microcontroller" on page 73. The mass erase of the main Flash memory array caused by the sequence is performed prior to restoring these registers.

---

In addition, the **USER\_REG0**, **USER\_REG1**, **USER\_REG2**, **USER\_REG3**, and **USER\_DBG** registers each use bit 31 (**NW**) to indicate that they have not been committed and bits in the register may be changed from 1 to 0. Table 8-2 on page 202 provides the **FMA** address required for commitment of each of the registers and the source of the data to be written when the **FMC** register is written with a value of 0xA442.0008. After writing the **COMT** bit, the user may poll the **FMC** register to wait for the commit operation to complete.

**Table 8-2. User-Programmable Flash Memory Resident Registers**

Register to be Committed	FMA Value	Data Source
FMPRE0	0x0000.0000	FMPRE0
FMPRE1	0x0000.0002	FMPRE1
FMPRE2	0x0000.0004	FMPRE2
FMPRE3	0x0000.0006	FMPRE3
FMPPE0	0x0000.0001	FMPPE0
FMPPE1	0x0000.0003	FMPPE1
FMPPE2	0x0000.0005	FMPPE2
FMPPE3	0x0000.0007	FMPPE3
USER_REG0	0x8000.0000	USER_REG0
USER_REG1	0x8000.0001	USER_REG1
USER_REG2	0x8000.0002	USER_REG2
USER_REG3	0x8000.0003	USER_REG3
USER_DBG	0x7510.0000	FMD

## 8.4 Register Map

Table 8-3 on page 202 lists the ROM Controller register and the Flash memory and control registers. The offset listed is a hexadecimal increment to the register's address. The **FMA**, **FMD**, **FMC**, **FCRIS**, **FCIM**, **FCMISC**, **FMC2**, **FWBVAL**, and **FWBn** register offsets are relative to the Flash memory control base address of 0x400F.D000. The ROM and Flash memory protection register offsets are relative to the System Control base address of 0x400F.E000.

**Table 8-3. Flash Register Map**

Offset	Name	Type	Reset	Description	See page
<b>Flash Memory Registers (Flash Control Offset)</b>					
0x000	FMA	R/W	0x0000.0000	Flash Memory Address	204
0x004	FMD	R/W	0x0000.0000	Flash Memory Data	205
0x008	FMC	R/W	0x0000.0000	Flash Memory Control	206
0x00C	FCRIS	RO	0x0000.0000	Flash Controller Raw Interrupt Status	208
0x010	FCIM	R/W	0x0000.0000	Flash Controller Interrupt Mask	209
0x014	FCMISC	R/W1C	0x0000.0000	Flash Controller Masked Interrupt Status and Clear	210
0x020	FMC2	R/W	0x0000.0000	Flash Memory Control 2	211
0x030	FWBVAL	R/W	0x0000.0000	Flash Write Buffer Valid	212
0x0F8	FCTL	R/W	0x0000.0000	Flash Control	214

**Table 8-3. Flash Register Map (continued)**

Offset	Name	Type	Reset	Description	See page
0x100 - 0x17C	FWBn	R/W	0x0000.0000	Flash Write Buffer n	213
<b>Memory Registers (System Control Offset)</b>					
0x0F0	RMCTL	R/W1C	-	ROM Control	215
0x0F4	RMVER	RO	0x0505.0400	ROM Version Register	216
0x130	FMPRE0	R/W	0xFFFF.FFFF	Flash Memory Protection Read Enable 0	217
0x200	FMPRE0	R/W	0xFFFF.FFFF	Flash Memory Protection Read Enable 0	217
0x134	FMPPE0	R/W	0xFFFF.FFFF	Flash Memory Protection Program Enable 0	218
0x400	FMPPE0	R/W	0xFFFF.FFFF	Flash Memory Protection Program Enable 0	218
0x1D0	USER_DBG	R/W	0xFFFF.FFFE	User Debug	219
0x1E0	USER_REG0	R/W	0xFFFF.FFFF	User Register 0	220
0x1E4	USER_REG1	R/W	0xFFFF.FFFF	User Register 1	221
0x1E8	USER_REG2	R/W	0xFFFF.FFFF	User Register 2	222
0x1EC	USER_REG3	R/W	0xFFFF.FFFF	User Register 3	223
0x204	FMPRE1	R/W	0xFFFF.FFFF	Flash Memory Protection Read Enable 1	224
0x208	FMPRE2	R/W	0xFFFF.FFFF	Flash Memory Protection Read Enable 2	225
0x20C	FMPRE3	R/W	0xFFFF.FFFF	Flash Memory Protection Read Enable 3	226
0x404	FMPPE1	R/W	0xFFFF.FFFF	Flash Memory Protection Program Enable 1	227
0x408	FMPPE2	R/W	0xFFFF.FFFF	Flash Memory Protection Program Enable 2	228
0x40C	FMPPE3	R/W	0xFFFF.FFFF	Flash Memory Protection Program Enable 3	229

## 8.5 Flash Memory Register Descriptions (Flash Control Offset)

This section lists and describes the Flash Memory registers, in numerical order by address offset. Registers in this section are relative to the Flash control base address of 0x400F.D000.

## Register 1: Flash Memory Address (FMA), offset 0x000

During a write operation, this register contains a 4-byte-aligned address and specifies where the data is written. During erase operations, this register contains a 1 KB-aligned address and specifies which page is erased. Note that the alignment requirements must be met by software or the results of the operation are unpredictable.

### Flash Memory Address (FMA)

Base 0x400F.D000

Offset 0x000

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved														OFFSET	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OFFSET															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:18	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
17:0	OFFSET	R/W	0x0	Address Offset  Address offset in Flash memory where operation is performed, except for nonvolatile registers (see "Nonvolatile Register Programming" on page 201 for details on values for this field).

## Register 2: Flash Memory Data (FMD), offset 0x004

This register contains the data to be written during the programming cycle or read during the read cycle. Note that the contents of this register are undefined for a read access of an execute-only block. This register is not used during erase cycles.

### Flash Memory Data (FMD)

Base 0x400F.D000

Offset 0x004

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	DATA	R/W	0x0000.0000	Data Value Data value for write operation.

### Register 3: Flash Memory Control (FMC), offset 0x008

When this register is written, the Flash memory controller initiates the appropriate access cycle for the location specified by the **Flash Memory Address (FMA)** register (see page 204). If the access is a write access, the data contained in the **Flash Memory Data (FMD)** register (see page 205) is written to the specified address.

This register must be the final register written and initiates the memory operation. The four control bits in the lower byte of this register are used to initiate memory operations.

Care must be taken not to set multiple control bits as the results of such an operation are unpredictable.

#### Flash Memory Control (FMC)

Base 0x400F.D000  
Offset 0x008  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRKEY															
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												COMT	MERASE	ERASE	WRITE
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description				
31:16	WRKEY	WO	0x0000	Flash Memory Write Key  This field contains a write key, which is used to minimize the incidence of accidental Flash memory writes. The value 0xA442 must be written into this field for a Flash memory write to occur. Writes to the <b>FMC</b> register without this <code>WRKEY</code> value are ignored. A read of this field returns the value 0.				
15:4	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.				
3	COMT	R/W	0	Commit Register Value  This bit is used to commit writes to Flash-memory-resident registers and to monitor the progress of that process.  Value Description <table border="0"> <tr> <td>1</td> <td>Set this bit to commit (write) the register value to a Flash-memory-resident register.  When read, a 1 indicates that the previous commit access is not complete.</td> </tr> <tr> <td>0</td> <td>A write of 0 has no effect on the state of this bit.  When read, a 0 indicates that the previous commit access is complete.</td> </tr> </table> A commit can take up to 50 $\mu$ s.  See "Nonvolatile Register Programming" on page 201 for more information on programming Flash-memory-resident registers.	1	Set this bit to commit (write) the register value to a Flash-memory-resident register.  When read, a 1 indicates that the previous commit access is not complete.	0	A write of 0 has no effect on the state of this bit.  When read, a 0 indicates that the previous commit access is complete.
1	Set this bit to commit (write) the register value to a Flash-memory-resident register.  When read, a 1 indicates that the previous commit access is not complete.							
0	A write of 0 has no effect on the state of this bit.  When read, a 0 indicates that the previous commit access is complete.							

Bit/Field	Name	Type	Reset	Description
2	MERASE	R/W	0	<p>Mass Erase Flash Memory</p> <p>This bit is used to mass erase the Flash main memory and to monitor the progress of that process.</p> <p>Value Description</p> <p>1 Set this bit to erase the Flash main memory.</p> <p>When read, a 1 indicates that the previous mass erase access is not complete.</p> <p>0 A write of 0 has no effect on the state of this bit.</p> <p>When read, a 0 indicates that the previous mass erase access is complete.</p> <p>A mass erase can take up to 250 ms.</p>
1	ERASE	R/W	0	<p>Erase a Page of Flash Memory</p> <p>This bit is used to erase a page of Flash memory and to monitor the progress of that process.</p> <p>Value Description</p> <p>1 Set this bit to erase the Flash memory page specified by the contents of the <b>FMA</b> register.</p> <p>When read, a 1 indicates that the previous page erase access is not complete.</p> <p>0 A write of 0 has no effect on the state of this bit.</p> <p>When read, a 0 indicates that the previous page erase access is complete.</p> <p>A page erase can take up to 25 ms.</p>
0	WRITE	R/W	0	<p>Write a Word into Flash Memory</p> <p>This bit is used to write a word into Flash memory and to monitor the progress of that process.</p> <p>Value Description</p> <p>1 Set this bit to write the data stored in the <b>FMD</b> register into the Flash memory location specified by the contents of the <b>FMA</b> register.</p> <p>When read, a 1 indicates that the write update access is not complete.</p> <p>0 A write of 0 has no effect on the state of this bit.</p> <p>When read, a 0 indicates that the previous write update access is complete.</p> <p>Writing a single word can take up to 50 <math>\mu</math>s.</p>

## Register 4: Flash Controller Raw Interrupt Status (FCRIS), offset 0x00C

This register indicates that the Flash memory controller has an interrupt condition. An interrupt is sent to the interrupt controller only if the corresponding **FCIM** register bit is set.

### Flash Controller Raw Interrupt Status (FCRIS)

Base 0x400F.D000

Offset 0x00C

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved														PRIS	ARIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description				
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.				
1	PRIS	RO	0	<p>Programming Raw Interrupt Status</p> <p>This bit provides status on programming cycles which are write or erase actions generated through the <b>FMC</b> or <b>FMC2</b> register bits (see page 206 and page 211).</p> <p>Value Description</p> <table border="0"> <tr> <td>1</td> <td>The programming cycle has completed.</td> </tr> <tr> <td>0</td> <td>The programming cycle has not completed.</td> </tr> </table> <p>This status is sent to the interrupt controller when the <b>PMASK</b> bit in the <b>FCIM</b> register is set.</p> <p>This bit is cleared by writing a 1 to the <b>PMISC</b> bit in the <b>FCMISC</b> register.</p>	1	The programming cycle has completed.	0	The programming cycle has not completed.
1	The programming cycle has completed.							
0	The programming cycle has not completed.							
0	ARIS	RO	0	<p>Access Raw Interrupt Status</p> <p>This bit indicates if the Flash memory was improperly accessed.</p> <p>Value Description</p> <table border="0"> <tr> <td>1</td> <td>The program tried to access the Flash memory counter to the policy set in the <b>FMPREn</b> and <b>FMPPEn</b> registers.</td> </tr> <tr> <td>0</td> <td>No access has tried to improperly access the Flash memory.</td> </tr> </table> <p>This status is sent to the interrupt controller when the <b>AMASK</b> bit in the <b>FCIM</b> register is set.</p> <p>This bit is cleared by writing a 1 to the <b>AMISC</b> bit in the <b>FCMISC</b> register.</p>	1	The program tried to access the Flash memory counter to the policy set in the <b>FMPREn</b> and <b>FMPPEn</b> registers.	0	No access has tried to improperly access the Flash memory.
1	The program tried to access the Flash memory counter to the policy set in the <b>FMPREn</b> and <b>FMPPEn</b> registers.							
0	No access has tried to improperly access the Flash memory.							



## Register 5: Flash Controller Interrupt Mask (FCIM), offset 0x010

This register controls whether the Flash memory controller generates interrupts to the controller.

### Flash Controller Interrupt Mask (FCIM)

Base 0x400F.D000

Offset 0x010

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved														PMASK	AMASK	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description				
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.				
1	PMASK	R/W	0	<p>Programming Interrupt Mask</p> <p>This bit controls the reporting of the programming raw interrupt status to the interrupt controller.</p> <p>Value Description</p> <table border="0"> <tr> <td>1</td> <td>An interrupt is sent to the interrupt controller when the <code>PRIS</code> bit is set.</td> </tr> <tr> <td>0</td> <td>The <code>PRIS</code> interrupt is suppressed and not sent to the interrupt controller.</td> </tr> </table>	1	An interrupt is sent to the interrupt controller when the <code>PRIS</code> bit is set.	0	The <code>PRIS</code> interrupt is suppressed and not sent to the interrupt controller.
1	An interrupt is sent to the interrupt controller when the <code>PRIS</code> bit is set.							
0	The <code>PRIS</code> interrupt is suppressed and not sent to the interrupt controller.							
0	AMASK	R/W	0	<p>Access Interrupt Mask</p> <p>This bit controls the reporting of the access raw interrupt status to the interrupt controller.</p> <p>Value Description</p> <table border="0"> <tr> <td>1</td> <td>An interrupt is sent to the interrupt controller when the <code>ARIS</code> bit is set.</td> </tr> <tr> <td>0</td> <td>The <code>ARIS</code> interrupt is suppressed and not sent to the interrupt controller.</td> </tr> </table>	1	An interrupt is sent to the interrupt controller when the <code>ARIS</code> bit is set.	0	The <code>ARIS</code> interrupt is suppressed and not sent to the interrupt controller.
1	An interrupt is sent to the interrupt controller when the <code>ARIS</code> bit is set.							
0	The <code>ARIS</code> interrupt is suppressed and not sent to the interrupt controller.							

## Register 6: Flash Controller Masked Interrupt Status and Clear (FCMISC), offset 0x014

This register provides two functions. First, it reports the cause of an interrupt by indicating which interrupt source or sources are signalling the interrupt. Second, it serves as the method to clear the interrupt reporting.

### Flash Controller Masked Interrupt Status and Clear (FCMISC)

Base 0x400F.D000

Offset 0x014

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															PMISC	AMISC
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	PMISC	R/W1C	0	<p>Programming Masked Interrupt Status and Clear</p> <p><b>Value Description</b></p> <p>1 When read, a 1 indicates that an unmasked interrupt was signaled because a programming cycle completed.</p> <p>Writing a 1 to this bit clears <b>PMISC</b> and also the <b>PRIS</b> bit in the <b>FCRIS</b> register (see page 208).</p> <p>0 When read, a 0 indicates that a programming cycle complete interrupt has not occurred.</p> <p>A write of 0 has no effect on the state of this bit.</p>
0	AMISC	R/W1C	0	<p>Access Masked Interrupt Status and Clear</p> <p><b>Value Description</b></p> <p>1 When read, a 1 indicates that an unmasked interrupt was signaled because an improper access to protected Flash memory was attempted.</p> <p>Writing a 1 to this bit clears <b>AMISC</b> and also the <b>ARIS</b> bit in the <b>FCRIS</b> register (see page 208).</p> <p>0 When read, a 0 indicates that no improper accesses have occurred.</p> <p>A write of 0 has no effect on the state of this bit.</p>

## Register 7: Flash Memory Control 2 (FMC2), offset 0x020

When this register is written, the Flash memory controller initiates the appropriate access cycle for the location specified by the **Flash Memory Address (FMA)** register (see page 204). If the access is a write access, the data contained in the **Flash Write Buffer (FWB)** registers is written.

This register must be the final register written as it initiates the memory operation.

### Flash Memory Control 2 (FMC2)

Base 0x400F.D000

Offset 0x020

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRKEY															
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															WRBUF
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	WRKEY	WO	0x0000	Flash Memory Write Key  This field contains a write key, which is used to minimize the incidence of accidental Flash memory writes. The value 0xA442 must be written into this field for a write to occur. Writes to the <b>FMC2</b> register without this <b>WRKEY</b> value are ignored. A read of this field returns the value 0.
15:1	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	WRBUF	R/W	0	Buffered Flash Memory Write

This bit is used to start a buffered write to Flash memory.

#### Value Description

1 Set this bit to write the data stored in the **FWBn** registers to the location specified by the contents of the **FMA** register.

When read, a 1 indicates that the previous buffered Flash memory write access is not complete.

0 A write of 0 has no effect on the state of this bit.

When read, a 0 indicates that the previous buffered Flash memory write access is complete.

A buffered Flash memory write can take up to 4 ms.

## Register 8: Flash Write Buffer Valid (FWBVAL), offset 0x030

This register provides a bitwise status of which **FWB<sub>n</sub>** registers have been written by the processor since the last write of the Flash memory write buffer. The entries with a 1 are written on the next write of the Flash memory write buffer. This register is cleared after the write operation by hardware. A protection violation on the write operation also clears this status.

Software can program the same 32 words to various Flash memory locations by setting the **FWB<sub>[n]</sub>** bits after they are cleared by the write operation. The next write operation then uses the same data as the previous one. In addition, if a **FWB<sub>n</sub>** register change should not be written to Flash memory, software can clear the corresponding **FWB<sub>[n]</sub>** bit to preserve the existing data when the next write operation occurs.

### Flash Write Buffer Valid (FWBVAL)

Base 0x400F.D000

Offset 0x030

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FWB[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FWB[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	FWB[n]	R/W	0x0	Flash Memory Write Buffer

#### Value Description

- |   |  |
|---|--|
| 1 | The corresponding <b>FWB<sub>n</sub></b> register has been updated since the last buffer write operation and is ready to be written to Flash memory. |
| 0 | The corresponding <b>FWB<sub>n</sub></b> register has no new data to be written.   |

Bit 0 corresponds to **FWB<sub>0</sub>**, offset 0x100, and bit 31 corresponds to **FWB<sub>31</sub>**, offset 0x13C.

## Register 9: Flash Write Buffer n (FWBn), offset 0x100 - 0x17C

These 32 registers hold the contents of the data to be written into the Flash memory on a buffered Flash memory write operation. The offset selects one of the 32-bit registers. Only **FWBn** registers that have been updated since the preceding buffered Flash memory write operation are written into the Flash memory, so it is not necessary to write the entire bank of registers in order to write 1 or 2 words. The **FWBn** registers are written into the Flash memory with the **FWB0** register corresponding to the address contained in **FMA**. **FWB1** is written to the address **FMA+0x4** etc. Note that only data bits that are 0 result in the Flash memory being modified. A data bit that is 1 leaves the content of the Flash memory bit at its previous value.

### Flash Write Buffer n (FWBn)

Base 0x400F.D000  
Offset 0x100 - 0x17C  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	DATA	R/W	0x0000.0000	Data Data to be written into the Flash memory.

## Register 10: Flash Control (FCTL), offset 0x0F8

This register is used to ensure that the microcontroller is powered down in a controlled fashion in systems where power is cycled more frequently than once every five minutes. The `USDREQ` bit should be set to indicate that power is going to be turned off. Software should poll the `USDACK` bit to determine when it is acceptable to power down.

Note that this power-down process is not required if the microcontroller enters hibernation mode prior to power being removed.

### Flash Control (FCTL)

Base 0x400F.D000

Offset 0x0F8

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															USDACK	USDREQ
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	USDACK	RO	0	User Shut Down Acknowledge  Value Description 1 The microcontroller can be powered down. 0 The microcontroller cannot yet be powered down.  This bit should be set within 50 ms of setting the <code>USDREQ</code> bit.
0	USDREQ	R/W	0	User Shut Down Request  Value Description 1 Requests permission to power down the microcontroller. 0 No effect.

## 8.6 Memory Register Descriptions (System Control Offset)

The remainder of this section lists and describes the registers that reside in Flash memory, in numerical order by address offset. Registers in this section are relative to the System Control base address of 0x400F.E000.

**Register 11: ROM Control (RMCTL), offset 0x0F0**

This register provides control of the ROM controller state. This register offset is relative to the System Control base address of 0x400F.E000.

**ROM Control (RMCTL)**

Base 0x400F.E000

Offset 0x0F0

Type R/W1C, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															BA
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	BA	R/W1C	-	Boot Alias

Upon reset, the system control module checks address 0x000.0004 to see if it has a valid reset vector. If the data at address 0x0000.0004 is 0xFFFF.FFFF, then it is assumed that the Flash memory has not yet been programmed, and this bit is then set by hardware so that the on-chip ROM appears at address 0x0.

**Value Description**

- |   |  |
|---|--|
| 1 | The microcontroller's ROM appears at address 0x0. This bit is set automatically if the data at address 0x0000.0004 is 0xFFFF.FFFF. |
| 0 | The Flash memory is at address 0x0.  |

This bit is cleared by writing a 1 to this bit position.

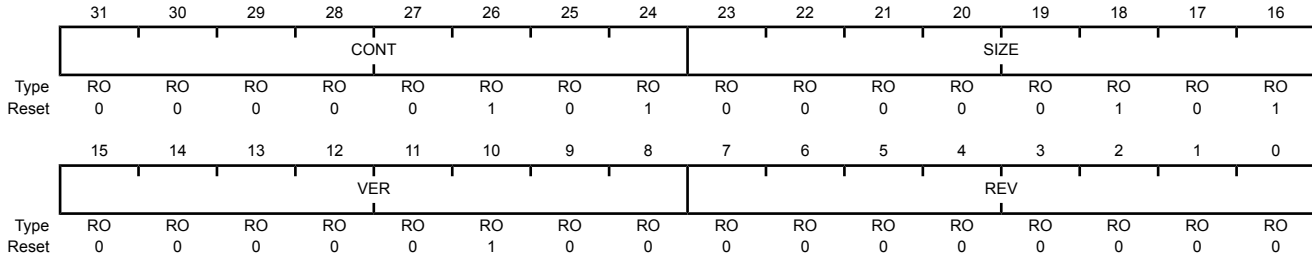
**Register 12: ROM Version Register (RMVER), offset 0x0F4**

**Note:** Offset is relative to System Control base address of 0x400FE000.

A 32-bit read-only register containing the ROM content version information.

ROM Version Register (RMVER)

Base 0x400F.E000  
 Offset 0x0F4  
 Type RO, reset 0x0505.0400



Bit/Field	Name	Type	Reset	Description
31:24	CONT	RO	0x05	ROM Contents  Value Description 0x05 Stellaris Boot Loader & DriverLib with AES
23:16	SIZE	RO	0x00 0x05	ROM Size  This field encodes the size of the ROM.  Value Description 0x00 Stellaris Boot Loader & DriverLib 0x05 Stellaris Boot Loader & DriverLib with AES
15:8	VER	RO	0x104	ROM Version
7:0	REV	RO	0x0	ROM Revision



## Register 13: Flash Memory Protection Read Enable 0 (FMPRE0), offset 0x130 and 0x200

**Note:** This register is aliased for backwards compatibility.

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register stores the read-only protection bits for each 2-KB flash block (**FMPPEn** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPREN** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPREN** and **FMPPEn** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. For additional information, see the "Flash Memory Protection" section.

### Flash Memory Protection Read Enable 0 (FMPRE0)

Base 0x400F.E000  
Offset 0x130 and 0x200  
Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	READ_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	READ_ENABLE	R/W	0xFFFFFFFF	Flash Read Enable  Configures 2-KB flash blocks to be read or executed only. The policies may be combined as shown in the table "Flash Protection Policy Combinations".  Value            Description 0xFFFFFFFF    Bits [31:0] each enable protection on a 2-KB block of Flash memory up to the total of 64 KB.

## Register 14: Flash Memory Protection Program Enable 0 (FMPPE0), offset 0x134 and 0x400

**Note:** This register is aliased for backwards compatibility.

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register stores the execute-only protection bits for each 2-KB flash block (**FMPPE<sub>n</sub>** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPPE<sub>n</sub>** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPPE<sub>n</sub>** and **FMPPE<sub>n</sub>** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. For additional information, see the "Flash Memory Protection" section.

### Flash Memory Protection Program Enable 0 (FMPPE0)

Base 0x400F.E000  
Offset 0x134 and 0x400  
Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	PROG_ENABLE	R/W	0xFFFFFFFF	Flash Programming Enable

Configures 2-KB flash blocks to be execute only. The policies may be combined as shown in the table "Flash Protection Policy Combinations".

Value	Description
0xFFFFFFFF	Bits [31:0] each enable protection on a 2-KB block of Flash memory up to the total of 64 KB.

**Register 15: User Debug (USER\_DBG), offset 0x1D0**

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register provides a write-once mechanism to disable external debugger access to the device in addition to 27 additional bits of user-defined data. The DBG0 bit (bit 0) is set to 0 from the factory and the DBG1 bit (bit 1) is set to 1, which enables external debuggers. Changing the DBG1 bit to 0 disables any external debugger access to the device permanently, starting with the next power-up cycle of the device. The NW bit (bit 31) indicates that the register has not yet been committed and is controlled through hardware to ensure that the register is only committed once. Prior to being committed, bits can only be changed from 1 to 0. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. The only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter.

**User Debug (USER\_DBG)**

Base 0x400F.E000

Offset 0x1D0

Type R/W, reset 0xFFFF.FFFE

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	NW	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	DATA														DBG1	DBG0	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

Bit/Field	Name	Type	Reset	Description
31	NW	R/W	1	User Debug Not Written  When set, this bit indicates that this 32-bit register has not been committed. When clear, this bit specifies that this register has been committed and may not be committed again.
30:2	DATA	R/W	0x1FFFFFFF	User Data  Contains the user data value. This field is initialized to all 1s and can only be committed once.
1	DBG1	R/W	1	Debug Control 1  The DBG1 bit must be 1 and DBG0 must be 0 for debug to be available.
0	DBG0	R/W	0	Debug Control 0  The DBG1 bit must be 1 and DBG0 must be 0 for debug to be available.

### Register 16: User Register 0 (USER\_REG0), offset 0x1E0

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register provides 31 bits of user-defined data that is non-volatile and can only be committed once. Bit 31 indicates that the register is available to be committed and is controlled through hardware to ensure that the register is only committed once. Prior to being committed, bits can only be changed from 1 to 0. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. The write-once characteristics of this register are useful for keeping static information like communication addresses that need to be unique per part and would otherwise require an external EEPROM or other non-volatile device. The only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG section.

#### User Register 0 (USER\_REG0)

Base 0x400F.E000  
 Offset 0x1E0  
 Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NW	DATA														
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31	NW	R/W	1	Not Written  When set, this bit indicates that this 32-bit register has not been committed. When clear, this bit specifies that this register has been committed and may not be committed again.
30:0	DATA	R/W	0x7FFFFFFF	User Data  Contains the user data value. This field is initialized to all 1s and can only be committed once.

**Register 17: User Register 1 (USER\_REG1), offset 0x1E4**

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register provides 31 bits of user-defined data that is non-volatile and can only be written once. Bit 31 indicates that the register is available to be written and is controlled through hardware to ensure that the register is only written once. The write-once characteristics of this register are useful for keeping static information like communication addresses that need to be unique per part and would otherwise require an external EEPROM or other non-volatile device.

**User Register 1 (USER\_REG1)**

Base 0x400F.E000

Offset 0x1E4

Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NW	DATA														
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31	NW	R/W	1	Not Written  When set, this bit indicates that this 32-bit register has not been committed. When clear, this bit specifies that this register has been committed and may not be committed again.
30:0	DATA	R/W	0x7FFFFFFF	User Data  Contains the user data value. This field is initialized to all 1s and can only be committed once.

### Register 18: User Register 2 (USER\_REG2), offset 0x1E8

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register provides 31 bits of user-defined data that is non-volatile and can only be written once. Bit 31 indicates that the register is available to be written and is controlled through hardware to ensure that the register is only written once. The write-once characteristics of this register are useful for keeping static information like communication addresses that need to be unique per part and would otherwise require an external EEPROM or other non-volatile device.

#### User Register 2 (USER\_REG2)

Base 0x400F.E000  
 Offset 0x1E8  
 Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NW	DATA														
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31	NW	R/W	1	Not Written  When set, this bit indicates that this 32-bit register has not been committed. When clear, this bit specifies that this register has been committed and may not be committed again.
30:0	DATA	R/W	0x7FFFFFFF	User Data  Contains the user data value. This field is initialized to all 1s and can only be committed once.

**Register 19: User Register 3 (USER\_REG3), offset 0x1EC**

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register provides 31 bits of user-defined data that is non-volatile and can only be written once. Bit 31 indicates that the register is available to be written and is controlled through hardware to ensure that the register is only written once. The write-once characteristics of this register are useful for keeping static information like communication addresses that need to be unique per part and would otherwise require an external EEPROM or other non-volatile device.

**User Register 3 (USER\_REG3)**

Base 0x400F.E000

Offset 0x1EC

Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NW	DATA														
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31	NW	R/W	1	Not Written  When set, this bit indicates that this 32-bit register has not been committed. When clear, this bit specifies that this register has been committed and may not be committed again.
30:0	DATA	R/W	0x7FFFFFFF	User Data  Contains the user data value. This field is initialized to all 1s and can only be committed once.

**Register 20: Flash Memory Protection Read Enable 1 (FMPRE1), offset 0x204**

**Note:** Offset is relative to System Control base address of 0x400FE000.

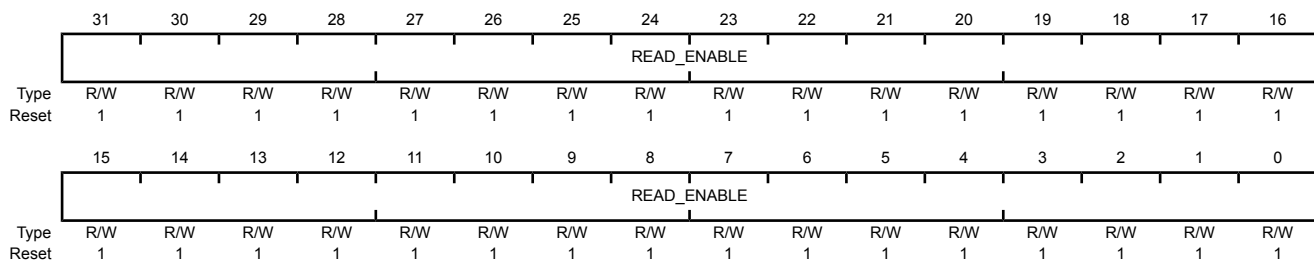
This register stores the read-only protection bits for each 2-KB flash block (**FMPPE<sub>n</sub>** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPRE<sub>n</sub>** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPRE<sub>n</sub>** and **FMPPE<sub>n</sub>** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. If the Flash memory size on the device is less than 64 KB, this register usually reads as zeroes, but software should not rely on these bits to be zero. For additional information, see the "Flash Memory Protection" section.

## Flash Memory Protection Read Enable 1 (FMPRE1)

Base 0x400F.E000

Offset 0x204

Type R/W, reset 0xFFFFFFFF



Bit/Field	Name	Type	Reset	Description
31:0	READ_ENABLE	R/W	0xFFFFFFFF	Flash Read Enable

Configures 2-KB flash blocks to be read or executed only. The policies may be combined as shown in the table "Flash Protection Policy Combinations".

Value	Description
-------	-------------

0xFFFFFFFF	Bits [31:0] each enable protection on a 2-KB block of Flash memory in memory range from 65 to 128 KB.
------------	---



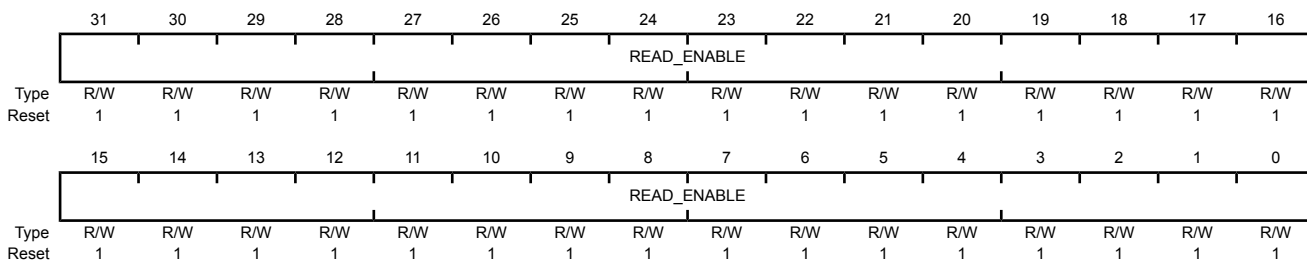
### Register 21: Flash Memory Protection Read Enable 2 (FMPRE2), offset 0x208

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register stores the read-only protection bits for each 2-KB flash block (**FMPPE<sub>n</sub>** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPRE<sub>n</sub>** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPRE<sub>n</sub>** and **FMPPE<sub>n</sub>** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. If the Flash memory size on the device is less than 128 KB, this register usually reads as zeroes, but software should not rely on these bits to be zero. For additional information, see the "Flash Memory Protection" section.

#### Flash Memory Protection Read Enable 2 (FMPRE2)

Base 0x400F.E000  
 Offset 0x208  
 Type R/W, reset 0xFFFF.FFFF



Bit/Field	Name	Type	Reset	Description
31:0	READ_ENABLE	R/W	0xFFFFFFFF	Flash Read Enable  Configures 2-KB flash blocks to be read or executed only. The policies may be combined as shown in the table "Flash Protection Policy Combinations".  Value            Description 0xFFFFFFFF    Bits [31:0] each enable protection on a 2-KB block of Flash memory in the range from 129 to 192 KB.

**Register 22: Flash Memory Protection Read Enable 3 (FMPRE3), offset 0x20C**

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register stores the read-only protection bits for each 2-KB flash block (**FMPPE<sub>n</sub>** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPRE<sub>n</sub>** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPRE<sub>n</sub>** and **FMPPE<sub>n</sub>** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. If the Flash memory size on the device is less than 192 KB, this register usually reads as zeroes, but software should not rely on these bits to be zero. For additional information, see the "Flash Memory Protection" section.

**Flash Memory Protection Read Enable 3 (FMPRE3)**

Base 0x400F.E000

Offset 0x20C

Type R/W, reset 0xFFFFFFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	READ_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	READ_ENABLE	R/W	0xFFFFFFFF	Flash Read Enable

Configures 2-KB flash blocks to be read or executed only. The policies may be combined as shown in the table "Flash Protection Policy Combinations".

Value	Description
-------	-------------

0xFFFFFFFF	Bits [31:0] each enable protection on a 2-KB block of Flash memory in the range from 193 to 256 KB.
------------	---

## Register 23: Flash Memory Protection Program Enable 1 (FMPPE1), offset 0x404

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register stores the execute-only protection bits for each 2-KB flash block (**FMPREN** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPPEn** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPREN** and **FMPPEn** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. If the Flash memory size on the device is less than 64 KB, this register usually reads as zeroes, but software should not rely on these bits to be zero. For additional information, see the "Flash Memory Protection" section.

### Flash Memory Protection Program Enable 1 (FMPPE1)

Base 0x400F.E000

Offset 0x404

Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	PROG_ENABLE	R/W	0xFFFFFFFF	Flash Programming Enable

Value	Description
0xFFFFFFFF	Bits [31:0] each enable protection on a 2-KB block of Flash memory in memory range from 65 to 128 KB.

## Register 24: Flash Memory Protection Program Enable 2 (FMPPE2), offset 0x408

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register stores the execute-only protection bits for each 2-KB flash block (**FMPPE<sub>n</sub>** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPPE<sub>n</sub>** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPPE<sub>n</sub>** and **FMPPE<sub>n</sub>** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. If the Flash memory size on the device is less than 128 KB, this register usually reads as zeroes, but software should not rely on these bits to be zero. For additional information, see the "Flash Memory Protection" section.

### Flash Memory Protection Program Enable 2 (FMPPE2)

Base 0x400F.E000

Offset 0x408

Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	PROG_ENABLE	R/W	0xFFFFFFFF	Flash Programming Enable

Value	Description
0xFFFFFFFF	Bits [31:0] each enable protection on a 2-KB block of Flash memory in the range from 129 to 192 KB.

## Register 25: Flash Memory Protection Program Enable 3 (FMPPE3), offset 0x40C

**Note:** Offset is relative to System Control base address of 0x400FE000.

This register stores the execute-only protection bits for each 2-KB flash block (**FMPPE<sub>n</sub>** stores the execute-only bits). Flash memory up to a total of 64 KB is controlled by this register. Other **FMPPE<sub>n</sub>** registers (if any) provide protection for other 64K blocks. This register is loaded during the power-on reset sequence. The factory settings for the **FMPPE<sub>n</sub>** and **FMPPE<sub>n</sub>** registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is R/W0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the "Recover Locked Device" sequence detailed in the JTAG chapter. If the Flash memory size on the device is less than 192 KB, this register usually reads as zeroes, but software should not rely on these bits to be zero. For additional information, see the "Flash Memory Protection" section.

### Flash Memory Protection Program Enable 3 (FMPPE3)

Base 0x400F.E000

Offset 0x40C

Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PROG_ENABLE															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	PROG_ENABLE	R/W	0xFFFFFFFF	Flash Programming Enable

Value	Description
0xFFFFFFFF	Bits [31:0] each enable protection on a 2-KB block of Flash memory in the range from 193 to 256 KB.

## 9 Micro Direct Memory Access ( $\mu$ DMA)

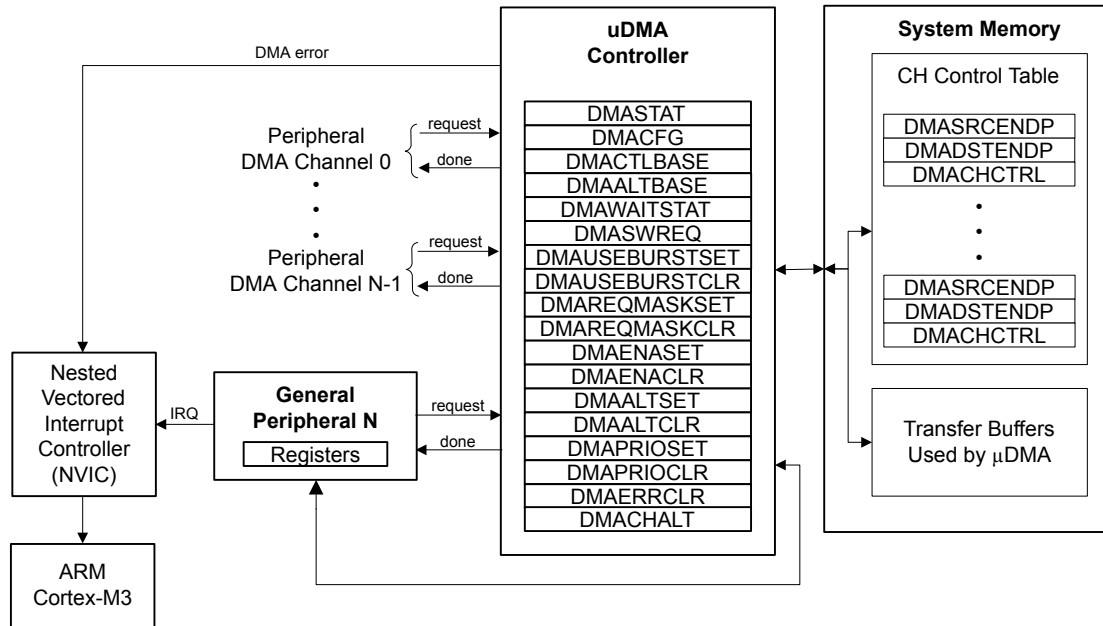
The LM3S1811 microcontroller includes a Direct Memory Access (DMA) controller, known as micro-DMA ( $\mu$ DMA). The  $\mu$ DMA controller provides a way to offload data transfer tasks from the Cortex-M3 processor, allowing for more efficient use of the processor and the available bus bandwidth. The  $\mu$ DMA controller can perform transfers between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. The  $\mu$ DMA controller provides the following features:

- ARM PrimeCell® 32-channel configurable  $\mu$ DMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of arbitrary transfers initiated from a single request
- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules: GP Timer, UART, ADC, EPI, SSI
  - Alternate channel assignments
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable bus arbitration scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Design optimizations for improved bus access performance between  $\mu$ DMA controller and the processor core
  - $\mu$ DMA controller access is subordinate to core access
  - RAM striping
  - Peripheral bus segmentation
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, half-word, word, or no increment
- Maskable peripheral requests

- Interrupt on transfer completion, with a separate interrupt per channel

## 9.1 Block Diagram

Figure 9-1.  $\mu$ DMA Block Diagram



## 9.2 Functional Description

The  $\mu$ DMA controller is a flexible and highly configurable DMA controller designed to work efficiently with the microcontroller's Cortex-M3 processor core. It supports multiple data sizes and address increment schemes, multiple levels of priority among DMA channels, and several transfer modes to allow for sophisticated programmed data transfers. The  $\mu$ DMA controller's usage of the bus is always subordinate to the processor core, so it never holds up a bus transaction by the processor. Because the  $\mu$ DMA controller is only using otherwise-idle bus cycles, the data transfer bandwidth it provides is essentially free, with no impact on the rest of the system. The bus architecture has been optimized to greatly enhance the ability of the processor core and the  $\mu$ DMA controller to efficiently share the on-chip bus, thus improving performance. The optimizations include RAM striping and peripheral bus segmentation, which in many cases allow both the processor core and the  $\mu$ DMA controller to access the bus and perform simultaneous data transfers.

The  $\mu$ DMA controller can transfer data to and from the on-chip SRAM. However, because the Flash memory and ROM are located on a separate internal bus, it is not possible to transfer data from the Flash memory or ROM with the  $\mu$ DMA controller.

Each peripheral function that is supported has a dedicated channel on the  $\mu$ DMA controller that can be configured independently. The  $\mu$ DMA controller implements a unique configuration method using channel control structures that are maintained in system memory by the processor. While simple transfer modes are supported, it is also possible to build up sophisticated "task" lists in memory that allow the  $\mu$ DMA controller to perform arbitrary-sized transfers to and from arbitrary locations as part of a single transfer request. The  $\mu$ DMA controller also supports the use of ping-pong buffering to accommodate constant streaming of data to or from a peripheral.

Each channel also has a configurable arbitration size. The arbitration size is the number of items that are transferred in a burst before the  $\mu$ DMA controller re-arbitrates for channel priority. Using the arbitration size, it is possible to control exactly how many items are transferred to or from a peripheral each time it makes a  $\mu$ DMA service request.

### 9.2.1 Channel Assignments

$\mu$ DMA channels 0-31 are assigned to peripherals according to the following table. The **DMA Channel Alternate Select (DMACHALT)** register (see page 278) can be used to specify the alternate assignment. Most channels have primary and alternate assignments. If the primary function is not available on this microcontroller, the alternate function becomes the primary function. If the alternate function is not available, the primary function is the only option.

**Note:** Channels noted in the table as "Available for software" may be assigned to peripherals in the future. However, they are currently available for software use. Channel 30 is dedicated for software use.

**Table 9-1.  $\mu$ DMA Channel Assignments**

$\mu$ DMA Channel	Peripheral Assigned	Alternate Assignment
0	Available for software	UART2 Receive
1	Available for software	UART2 Transmit
2	Available for software	General-Purpose Timer 3A
3	Available for software	General-Purpose Timer 3B
4	Available for software	General-Purpose Timer 2A
5	Available for software	General-Purpose Timer 2B
6	Available for software	General-Purpose Timer 2A
7	Available for software	General-Purpose Timer 2B
8	UART0 Receive	UART1 Receive
9	UART0 Transmit	UART1 Transmit
10	SSI0 Receive	SSI1 Receive
11	SSI0 Transmit	SSI1 Transmit
12	Available for software	UART2 Receive
13	Available for software	UART2 Transmit
14	ADC0 Sample Sequencer 0	General-Purpose Timer 2A
15	ADC0 Sample Sequencer 1	General-Purpose Timer 2B
16	ADC0 Sample Sequencer 2	Available for software
17	ADC0 Sample Sequencer 3	Available for software
18	General-Purpose Timer 0A	General-Purpose Timer 1A
19	General-Purpose Timer 0B	General-Purpose Timer 1B
20	General-Purpose Timer 1A	EPI0 NBRFIFO
21	General-Purpose Timer 1B	EPI0 WFIFO
22	UART1 Receive	Available for software
23	UART1 Transmit	Available for software
24	SSI1 Receive	Available for software
25	SSI1 Transmit	Available for software
26	Available for software	Available for software
27	Available for software	Available for software



**Table 9-1.  $\mu$ DMA Channel Assignments (continued)**

$\mu$ DMA Channel	Peripheral Assigned	Alternate Assignment
28	Available for software	Available for software
29	Available for software	Available for software
30	Dedicated for software use	
31	Reserved	

### 9.2.2 Priority

The  $\mu$ DMA controller assigns priority to each channel based on the channel number and the priority level bit for the channel. Channel number 0 has the highest priority and as the channel number increases, the priority of a channel decreases. Each channel has a priority level bit to provide two levels of priority: default priority and high priority. If the priority level bit is set, then that channel has higher priority than all other channels at default priority. If multiple channels are set for high priority, then the channel number is used to determine relative priority among all the high priority channels.

The priority bit for a channel can be set using the **DMA Channel Priority Set (DMAPRIOSET)** register and cleared with the **DMA Channel Priority Clear (DMAPRIOCLR)** register.

### 9.2.3 Arbitration Size

When a  $\mu$ DMA channel requests a transfer, the  $\mu$ DMA controller arbitrates among all the channels making a request and services the  $\mu$ DMA channel with the highest priority. Once a transfer begins, it continues for a selectable number of transfers before re-arbitrating among the requesting channels again. The arbitration size can be configured for each channel, ranging from 1 to 1024 item transfers. After the  $\mu$ DMA controller transfers the number of items specified by the arbitration size, it then checks among all the channels making a request and services the channel with the highest priority.

If a lower priority  $\mu$ DMA channel uses a large arbitration size, the latency for higher priority channels is increased because the  $\mu$ DMA controller completes the lower priority burst before checking for higher priority requests. Therefore, lower priority channels should not use a large arbitration size for best response on high priority channels.

The arbitration size can also be thought of as a burst size. It is the maximum number of items that are transferred at any one time in a burst. Here, the term arbitration refers to determination of  $\mu$ DMA channel priority, not arbitration for the bus. When the  $\mu$ DMA controller arbitrates for the bus, the processor always takes priority. Furthermore, the  $\mu$ DMA controller is held off whenever the processor must perform a bus transaction on the same bus, even in the middle of a burst transfer.

### 9.2.4 Request Types

The  $\mu$ DMA controller responds to two types of requests from a peripheral: single or burst. Each peripheral may support either or both types of requests. A single request means that the peripheral is ready to transfer one item, while a burst request means that the peripheral is ready to transfer multiple items.

The  $\mu$ DMA controller responds differently depending on whether the peripheral is making a single request or a burst request. If both are asserted, and the  $\mu$ DMA channel has been set up for a burst transfer, then the burst request takes precedence. See Table 9-2, which shows how each peripheral supports the two request types.

**Table 9-2. Request Type Support**

Peripheral	Single Request Signal	Burst Request Signal
UART TX	TX FIFO Not Full	TX FIFO Level (configurable)

**Table 9-2. Request Type Support (continued)**

Peripheral	Single Request Signal	Burst Request Signal
UART RX	RX FIFO Not Empty	RX FIFO Level (configurable)
SSI TX	TX FIFO Not Full	TX FIFO Level (fixed at 4)
SSI RX	RX FIFO Not Empty	RX FIFO Level (fixed at 4)
ADC	None	Sequencer IE bit
General-Purpose Timer	None	Raw interrupt pulse
EPI WFIFO	None	WFIFO Level (configurable)
EPI NBRFIFO	None	NBRFIFO Level (configurable)

#### 9.2.4.1 Single Request

When a single request is detected, and not a burst request, the  $\mu$ DMA controller transfers one item and then stops to wait for another request.

#### 9.2.4.2 Burst Request

When a burst request is detected, the  $\mu$ DMA controller transfers the number of items that is the lesser of the arbitration size or the number of items remaining in the transfer. Therefore, the arbitration size should be the same as the number of data items that the peripheral can accommodate when making a burst request. For example, the UART generates a burst request based on the FIFO trigger level. In this case, the arbitration size should be set to the amount of data that the FIFO can transfer when the trigger level is reached. A burst transfer runs to completion once it is started, and cannot be interrupted, even by a higher priority channel. Burst transfers complete in a shorter time than the same number of non-burst transfers.

It may be desirable to use only burst transfers and not allow single transfers. For example, perhaps the nature of the data is such that it only makes sense when transferred together as a single unit rather than one piece at a time. The single request can be disabled by using the **DMA Channel Useburst Set (DMAUSEBURSTSET)** register. By setting the bit for a channel in this register, the  $\mu$ DMA controller only responds to burst requests for that channel.

### 9.2.5 Channel Configuration

The  $\mu$ DMA controller uses an area of system memory to store a set of channel control structures in a table. The control table may have one or two entries for each  $\mu$ DMA channel. Each entry in the table structure contains source and destination pointers, transfer size, and transfer mode. The control table can be located anywhere in system memory, but it must be contiguous and aligned on a 1024-byte boundary.

Table 9-3 on page 235 shows the layout in memory of the channel control table. Each channel may have one or two control structures in the control table: a primary control structure and an optional alternate control structure. The table is organized so that all of the primary entries are in the first half of the table, and all the alternate structures are in the second half of the table. The primary entry is used for simple transfer modes where transfers can be reconfigured and restarted after each transfer is complete. In this case, the alternate control structures are not used and therefore only the first half of the table must be allocated in memory; the second half of the control table is not necessary, and that memory can be used for something else. If a more complex transfer mode is used such as ping-pong or scatter-gather, then the alternate control structure is also used and memory space should be allocated for the entire table.

Any unused memory in the control table may be used by the application. This includes the control structures for any channels that are unused by the application as well as the unused control word for each channel.

**Table 9-3. Control Structure Memory Map**

Offset	Channel
0x0	0, Primary
0x10	1, Primary
...	...
0x1F0	31, Primary
0x200	0, Alternate
0x210	1, Alternate
...	...
0x3F0	31, Alternate

Table 9-4 shows an individual control structure entry in the control table. Each entry is aligned on a 16-byte boundary. The entry contains four long words: the source end pointer, the destination end pointer, the control word, and an unused entry. The end pointers point to the ending address of the transfer and are inclusive. If the source or destination is non-incrementing (as for a peripheral register), then the pointer should point to the transfer address.

**Table 9-4. Channel Control Structure**

Offset	Description
0x000	Source End Pointer
0x004	Destination End Pointer
0x008	Control Word
0x00C	Unused

The control word contains the following fields:

- Source and destination data sizes
- Source and destination address increment size
- Number of transfers before bus arbitration
- Total number of items to transfer
- Useburst flag
- Transfer mode

The control word and each field are described in detail in “ $\mu$ DMA Channel Control Structure” on page 252. The  $\mu$ DMA controller updates the transfer size and transfer mode fields as the transfer is performed. At the end of a transfer, the transfer size indicates 0, and the transfer mode indicates "stopped." Because the control word is modified by the  $\mu$ DMA controller, it must be reconfigured before each new transfer. The source and destination end pointers are not modified, so they can be left unchanged if the source or destination addresses remain the same.

Prior to starting a transfer, a  $\mu$ DMA channel must be enabled by setting the appropriate bit in the **DMA Channel Enable Set (DMAENASET)** register. A channel can be disabled by setting the channel bit in the **DMA Channel Enable Clear (DMAENACLR)** register. At the end of a complete  $\mu$ DMA transfer, the controller automatically disables the channel.

## 9.2.6 Transfer Modes

The  $\mu$ DMA controller supports several transfer modes. Two of the modes support simple one-time transfers. Several complex modes support a continuous flow of data.

### 9.2.6.1 Stop Mode

While Stop is not actually a transfer mode, it is a valid value for the mode field of the control word. When the mode field has this value, the  $\mu$ DMA controller does not perform any transfers and disables the channel if it is enabled. At the end of a transfer, the  $\mu$ DMA controller updates the control word to set the mode to Stop.

### 9.2.6.2 Basic Mode

In Basic mode, the  $\mu$ DMA controller performs transfers as long as there are more items to transfer, and a transfer request is present. This mode is used with peripherals that assert a  $\mu$ DMA request signal whenever the peripheral is ready for a data transfer. Basic mode should not be used in any situation where the request is momentary even though the entire transfer should be completed. For example, a software-initiated transfer creates a momentary request, and in Basic mode, only one item is transferred on a software request.

When all of the items have been transferred using Basic mode, the  $\mu$ DMA controller sets the mode for that channel to Stop.

### 9.2.6.3 Auto Mode

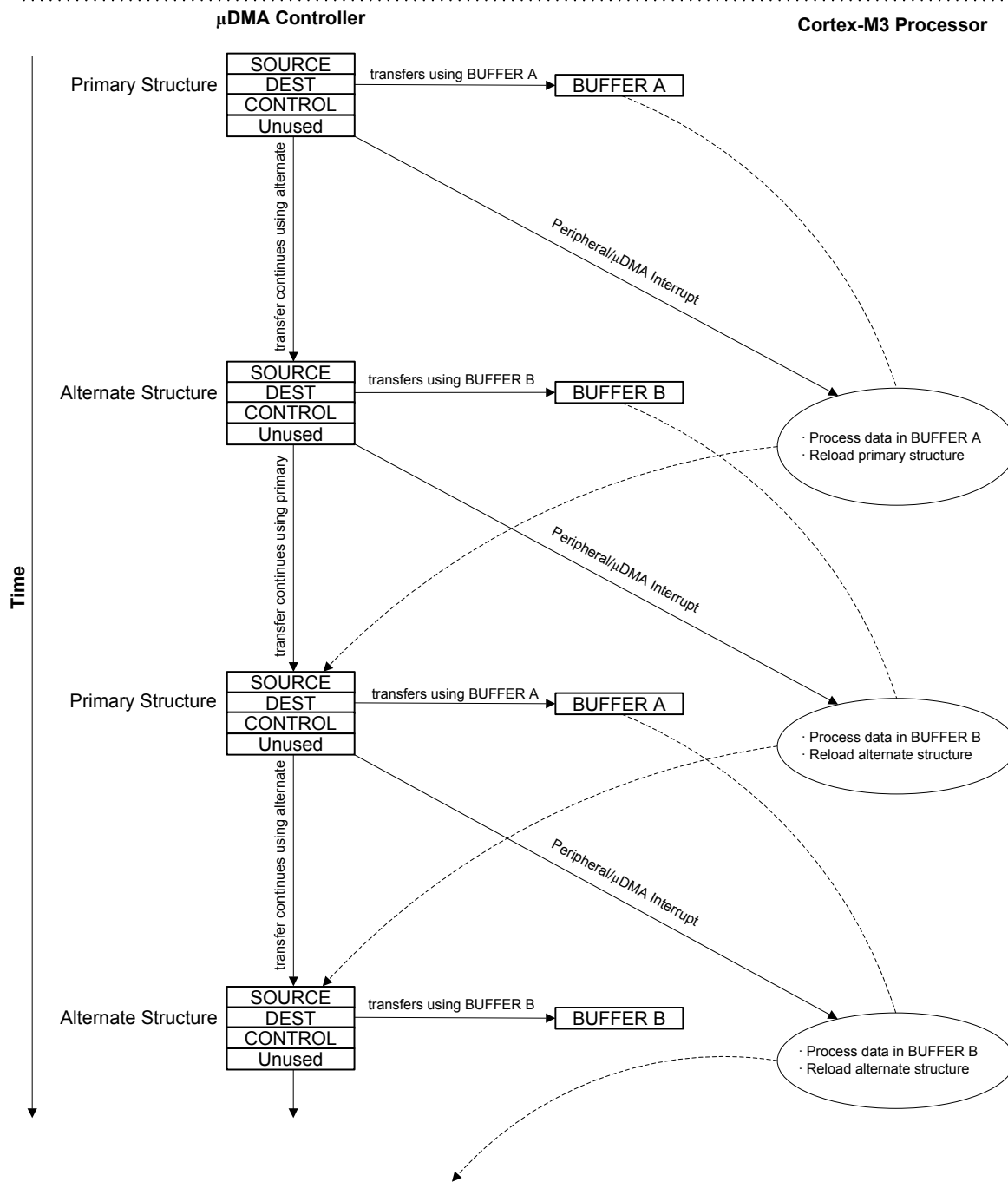
Auto mode is similar to Basic mode, except that once a transfer request is received, the transfer runs to completion, even if the  $\mu$ DMA request is removed. This mode is suitable for software-triggered transfers. Generally, Auto mode is not used with a peripheral.

When all the items have been transferred using Auto mode, the  $\mu$ DMA controller sets the mode for that channel to Stop.

### 9.2.6.4 Ping-Pong

Ping-Pong mode is used to support a continuous data flow to or from a peripheral. To use Ping-Pong mode, both the primary and alternate data structures must be implemented. Both structures are set up by the processor for data transfer between memory and a peripheral. The transfer is started using the primary control structure. When the transfer using the primary control structure is complete, the  $\mu$ DMA controller reads the alternate control structure for that channel to continue the transfer. Each time this happens, an interrupt is generated, and the processor can reload the control structure for the just-completed transfer. Data flow can continue indefinitely this way, using the primary and alternate control structures to switch back and forth between buffers as the data flows to or from the peripheral.

Refer to Figure 9-2 for an example showing operation in Ping-Pong mode.

Figure 9-2. Example of Ping-Pong  $\mu$ DMA Transaction

### 9.2.6.5 Memory Scatter-Gather

Memory Scatter-Gather mode is a complex mode used when data must be transferred to or from varied locations in memory instead of a set of contiguous locations in a memory buffer. For example, a gather  $\mu$ DMA operation could be used to selectively read the payload of several stored packets of a communication protocol and store them together in sequence in a memory buffer.

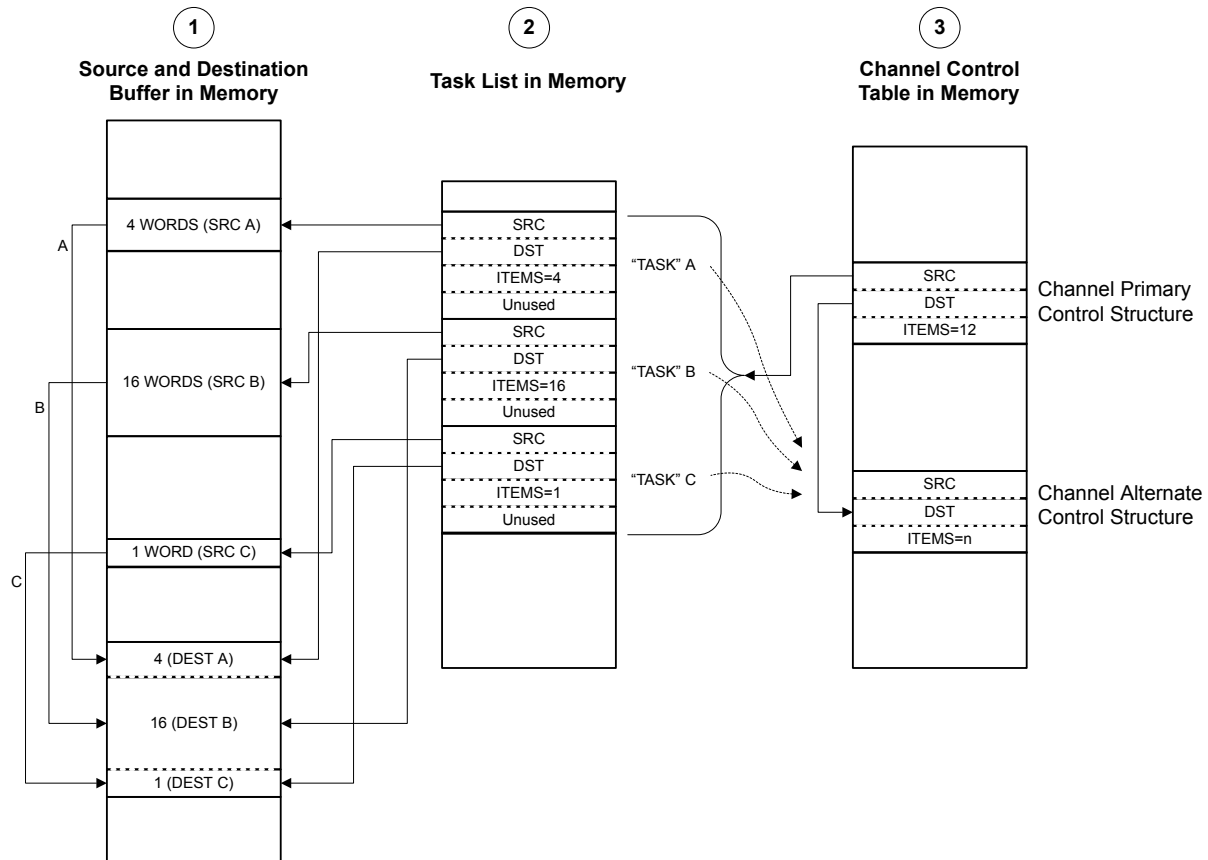
In Memory Scatter-Gather mode, the primary control structure is used to program the alternate control structure from a table in memory. The table is set up by the processor software and contains a list of control structures, each containing the source and destination end pointers, and the control word for a specific transfer. The mode of each control word must be set to Scatter-Gather mode. Each entry in the table is copied in turn to the alternate structure where it is then executed. The  $\mu$ DMA controller alternates between using the primary control structure to copy the next transfer instruction from the list and then executing the new transfer instruction. The end of the list is marked by programming the control word for the last entry to use Basic transfer mode. Once the last transfer is performed using Basic mode, the  $\mu$ DMA controller stops. A completion interrupt is generated only after the last transfer. It is possible to loop the list by having the last entry copy the primary control structure to point back to the beginning of the list (or to a new list). It is also possible to trigger a set of other channels to perform a transfer, either directly, by programming a write to the software trigger for another channel, or indirectly, by causing a peripheral action that results in a  $\mu$ DMA request.

By programming the  $\mu$ DMA controller using this method, a set of arbitrary transfers can be performed based on a single  $\mu$ DMA request.

Refer to Figure 9-3 on page 239 and Figure 9-4 on page 240, which show an example of operation in Memory Scatter-Gather mode. This example shows a *gather* operation, where data in three separate buffers in memory is copied together into one buffer. Figure 9-3 on page 239 shows how the application sets up a  $\mu$ DMA task list in memory that is used by the controller to perform three sets of copy operations from different locations in memory. The primary control structure for the channel that is used for the operation is configured to copy from the task list to the alternate control structure.

Figure 9-4 on page 240 shows the sequence as the  $\mu$ DMA controller performs the three sets of copy operations. First, using the primary control structure, the  $\mu$ DMA controller loads the alternate control structure with task A. It then performs the copy operation specified by task A, copying the data from the source buffer A to the destination buffer. Next, the  $\mu$ DMA controller again uses the primary control structure to load task B into the alternate control structure, and then performs the B operation with the alternate control structure. The process is repeated for task C.

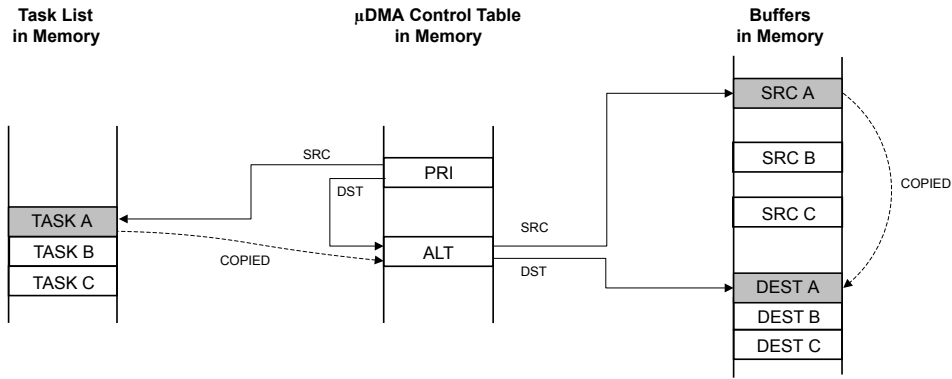
Figure 9-3. Memory Scatter-Gather, Setup and Configuration



## NOTES:

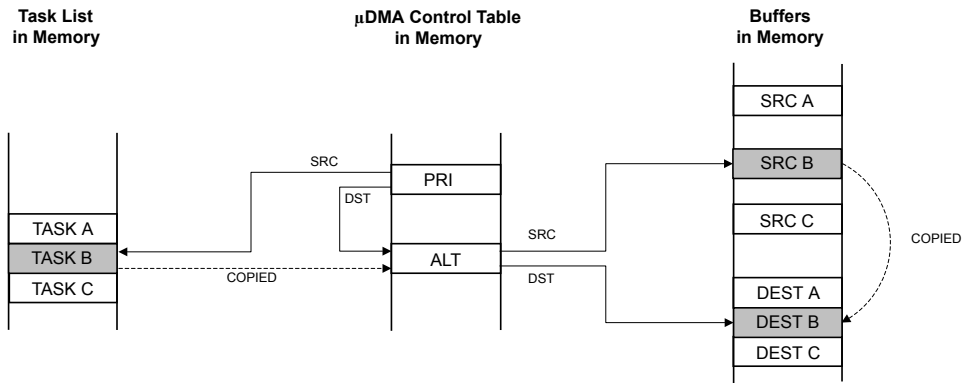
1. Application has a need to copy data items from three separate locations in memory into one combined buffer.
2. Application sets up  $\mu$ DMA "task list" in memory, which contains the pointers and control configuration for three  $\mu$ DMA copy "tasks."
3. Application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where it is executed by the  $\mu$ DMA controller.

Figure 9-4. Memory Scatter-Gather,  $\mu$ DMA Copy Sequence



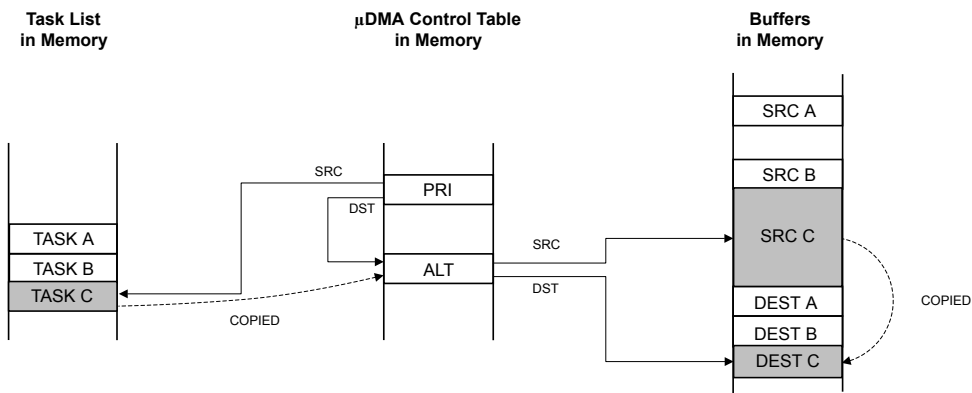
Using the channel's primary control structure, the  $\mu$ DMA controller copies task A configuration to the channel's alternate control structure.

Then, using the channel's alternate control structure, the  $\mu$ DMA controller copies data from the source buffer A to the destination buffer.



Using the channel's primary control structure, the  $\mu$ DMA controller copies task B configuration to the channel's alternate control structure.

Then, using the channel's alternate control structure, the  $\mu$ DMA controller copies data from the source buffer B to the destination buffer.



Using the channel's primary control structure, the  $\mu$ DMA controller copies task C configuration to the channel's alternate control structure.

Then, using the channel's alternate control structure, the  $\mu$ DMA controller copies data from the source buffer C to the destination buffer.



### 9.2.6.6 Peripheral Scatter-Gather

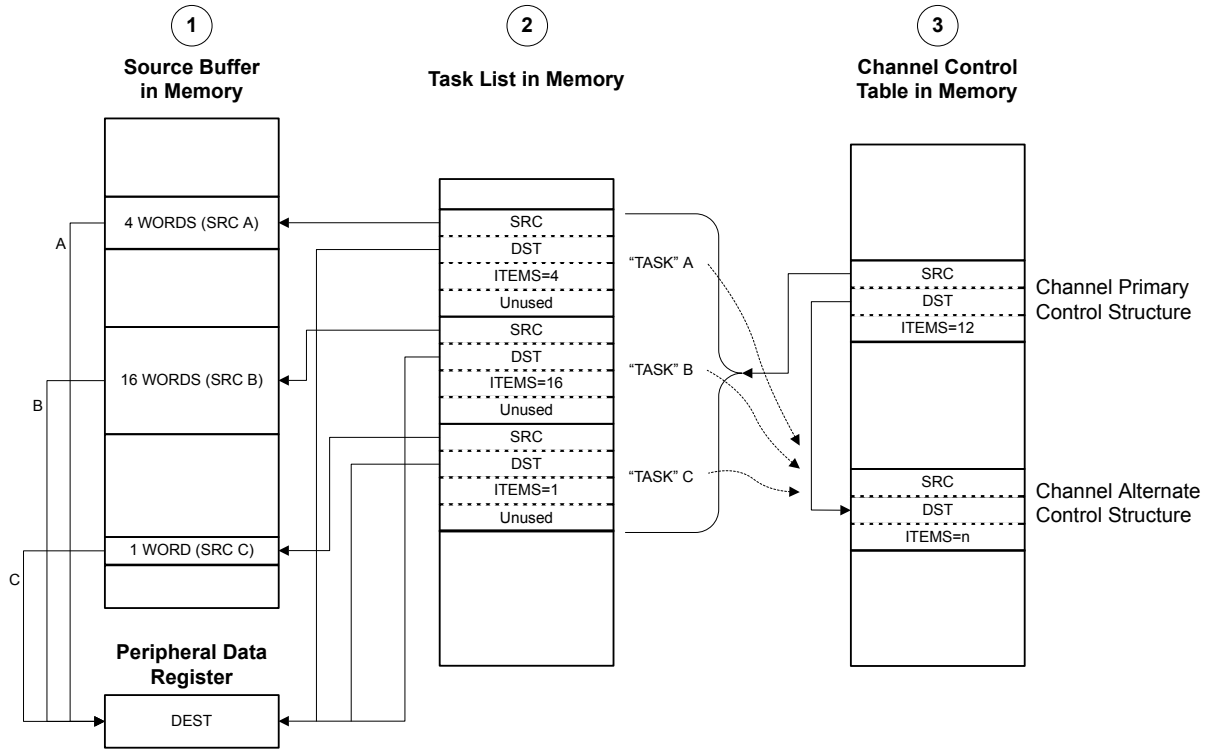
Peripheral Scatter-Gather mode is very similar to Memory Scatter-Gather, except that the transfers are controlled by a peripheral making a  $\mu$ DMA request. Upon detecting a request from the peripheral, the  $\mu$ DMA controller uses the primary control structure to copy one entry from the list to the alternate control structure and then performs the transfer. At the end of this transfer, the next transfer is started only if the peripheral again asserts a  $\mu$ DMA request. The  $\mu$ DMA controller continues to perform transfers from the list only when the peripheral is making a request, until the last transfer is complete. A completion interrupt is generated only after the last transfer.

By using this method, the  $\mu$ DMA controller can transfer data to or from a peripheral from a set of arbitrary locations whenever the peripheral is ready to transfer data.

Refer to Figure 9-5 on page 242 and Figure 9-6 on page 243, which show an example of operation in Peripheral Scatter-Gather mode. This example shows a gather operation, where data from three separate buffers in memory is copied to a single peripheral data register. Figure 9-5 on page 242 shows how the application sets up a  $\mu$ DMA task list in memory that is used by the controller to perform three sets of copy operations from different locations in memory. The primary control structure for the channel that is used for the operation is configured to copy from the task list to the alternate control structure.

Figure 9-6 on page 243 shows the sequence as the  $\mu$ DMA controller performs the three sets of copy operations. First, using the primary control structure, the  $\mu$ DMA controller loads the alternate control structure with task A. It then performs the copy operation specified by task A, copying the data from the source buffer A to the peripheral data register. Next, the  $\mu$ DMA controller again uses the primary control structure to load task B into the alternate control structure, and then performs the B operation with the alternate control structure. The process is repeated for task C.

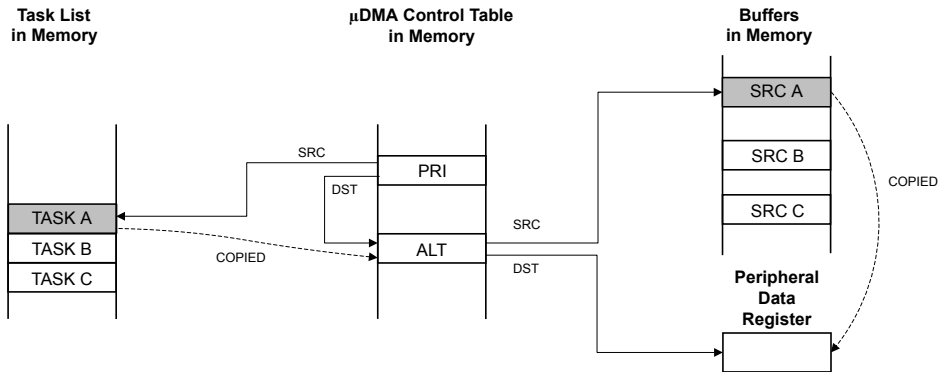
Figure 9-5. Peripheral Scatter-Gather, Setup and Configuration



NOTES:

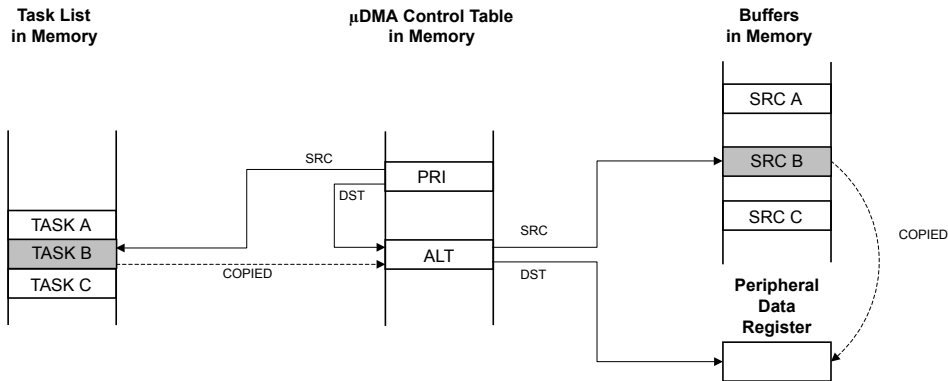
1. Application has a need to copy data items from three separate locations in memory into a peripheral data register.
2. Application sets up  $\mu$ DMA "task list" in memory, which contains the pointers and control configuration for three  $\mu$ DMA copy "tasks."
3. Application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where it is executed by the  $\mu$ DMA controller.

Figure 9-6. Peripheral Scatter-Gather,  $\mu$ DMA Copy Sequence



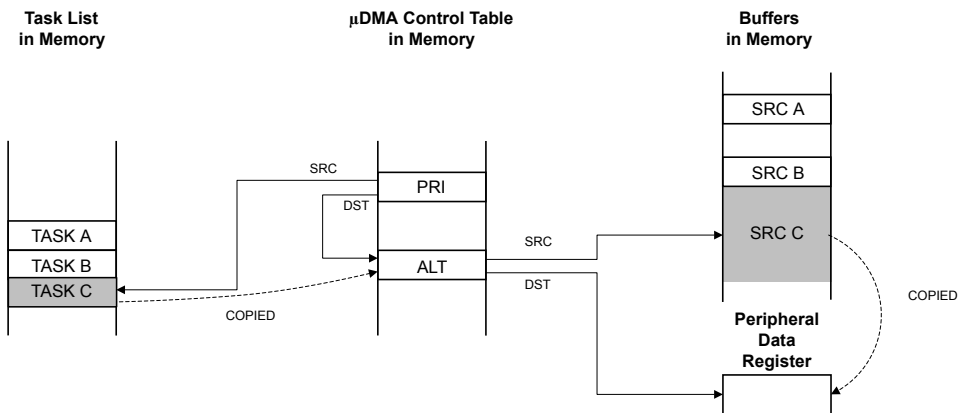
Using the channel's primary control structure, the  $\mu$ DMA controller copies task A configuration to the channel's alternate control structure.

Then, using the channel's alternate control structure, the  $\mu$ DMA controller copies data from the source buffer A to the peripheral data register.



Using the channel's primary control structure, the  $\mu$ DMA controller copies task B configuration to the channel's alternate control structure.

Then, using the channel's alternate control structure, the  $\mu$ DMA controller copies data from the source buffer B to the peripheral data register.



Using the channel's primary control structure, the  $\mu$ DMA controller copies task C configuration to the channel's alternate control structure.

Then, using the channel's alternate control structure, the  $\mu$ DMA controller copies data from the source buffer C to the peripheral data register.

## 9.2.7 Transfer Size and Increment

The  $\mu$ DMA controller supports transfer data sizes of 8, 16, or 32 bits. The source and destination data size must be the same for any given transfer. The source and destination address can be auto-incremented by bytes, half-words, or words, or can be set to no increment. The source and destination address increment values can be set independently, and it is not necessary for the address increment to match the data size as long as the increment is the same or larger than the data size. For example, it is possible to perform a transfer using 8-bit data size, but using an address increment of full words (4 bytes). The data to be transferred must be aligned in memory according to the data size (8, 16, or 32 bits).

Table 9-5 shows the configuration to read from a peripheral that supplies 8-bit data.

**Table 9-5.  $\mu$ DMA Read Example: 8-Bit Peripheral**

Field	Configuration
Source data size	8 bits
Destination data size	8 bits
Source address increment	No increment
Destination address increment	Byte
Source end pointer	Peripheral read FIFO register
Destination end pointer	End of the data buffer in memory

## 9.2.8 Peripheral Interface

Each peripheral that supports  $\mu$ DMA has a single request and/or burst request signal that is asserted when the peripheral is ready to transfer data (see Table 9-2 on page 233). The request signal can be disabled or enabled using the **DMA Channel Request Mask Set (DMAREQMASKSET)** and **DMA Channel Request Mask Clear (DMAREQMASKCLR)** registers. The  $\mu$ DMA request signal is disabled, or masked, when the channel request mask bit is set. When the request is not masked, the  $\mu$ DMA channel is configured correctly and enabled, and the peripheral asserts the request signal, the  $\mu$ DMA controller begins the transfer.

When a  $\mu$ DMA transfer is complete, the  $\mu$ DMA controller generates an interrupt, see “Interrupts and Errors” on page 245 for more information.

For more information on how a specific peripheral interacts with the  $\mu$ DMA controller, refer to the DMA Operation section in the chapter that discusses that peripheral.

## 9.2.9 Software Request

One  $\mu$ DMA channel is dedicated to software-initiated transfers. This channel also has a dedicated interrupt to signal completion of a  $\mu$ DMA transfer. A transfer is initiated by software by first configuring and enabling the transfer, and then issuing a software request using the **DMA Channel Software Request (DMASWREQ)** register. For software-based transfers, the Auto transfer mode should be used.

It is possible to initiate a transfer on any channel using the **DMASWREQ** register. If a request is initiated by software using a peripheral  $\mu$ DMA channel, then the completion interrupt occurs on the interrupt vector for the peripheral instead of the software interrupt vector. Any channel may be used for software requests as long as the corresponding peripheral is not using  $\mu$ DMA for data transfer.

## 9.2.10 Interrupts and Errors

When a  $\mu$ DMA transfer is complete, the  $\mu$ DMA controller generates a completion interrupt on the interrupt vector of the peripheral. Therefore, if  $\mu$ DMA is used to transfer data for a peripheral and interrupts are used, then the interrupt handler for that peripheral must be designed to handle the  $\mu$ DMA transfer completion interrupt. If the transfer uses the software  $\mu$ DMA channel, then the completion interrupt occurs on the dedicated software  $\mu$ DMA interrupt vector (see Table 9-6).

When  $\mu$ DMA is enabled for a peripheral, the  $\mu$ DMA controller stops the normal transfer interrupts for a peripheral from reaching the interrupt controller (the interrupts are still reported in the peripheral's interrupt registers). Thus, when a large amount of data is transferred using  $\mu$ DMA, instead of receiving multiple interrupts from the peripheral as data flows, the interrupt controller receives only one interrupt when the transfer is complete. Unmasked peripheral error interrupts continue to be sent to the interrupt controller.

If the  $\mu$ DMA controller encounters a bus or memory protection error as it attempts to perform a data transfer, it disables the  $\mu$ DMA channel that caused the error and generates an interrupt on the  $\mu$ DMA error interrupt vector. The processor can read the **DMA Bus Error Clear (DMAERRCLR)** register to determine if an error is pending. The `ERRCLR` bit is set if an error occurred. The error can be cleared by writing a 1 to the `ERRCLR` bit.

Table 9-6 shows the dedicated interrupt assignments for the  $\mu$ DMA controller.

**Table 9-6.  $\mu$ DMA Interrupt Assignments**

Interrupt	Assignment
46	$\mu$ DMA Software Channel Transfer
47	$\mu$ DMA Error

## 9.3 Initialization and Configuration

### 9.3.1 Module Initialization

Before the  $\mu$ DMA controller can be used, it must be enabled in the System Control block and in the peripheral. The location of the channel control structure must also be programmed.

The following steps should be performed one time during system initialization:

1. The  $\mu$ DMA peripheral must be enabled in the System Control block. To do this, set the `UDMA` bit of the System Control **RCGC2** register (see page 158).
2. Enable the  $\mu$ DMA controller by setting the `MASTEREN` bit of the **DMA Configuration (DMACFG)** register.
3. Program the location of the channel control table by writing the base address of the table to the **DMA Channel Control Base Pointer (DMACTLBASE)** register. The base address must be aligned on a 1024-byte boundary.

### 9.3.2 Configuring a Memory-to-Memory Transfer

$\mu$ DMA channel 30 is dedicated for software-initiated transfers. However, any channel can be used for software-initiated, memory-to-memory transfer if the associated peripheral is not being used.

#### 9.3.2.1 Configure the Channel Attributes

First, configure the channel attributes:

1. Program bit 30 of the **DMA Channel Priority Set (DMAPRIOSET)** or **DMA Channel Priority Clear (DMAPRIOCLR)** registers to set the channel to High priority or Default priority.
2. Set bit 30 of the **DMA Channel Primary Alternate Clear (DMAALTCLR)** register to select the primary channel control structure for this transfer.
3. Set bit 30 of the **DMA Channel Useburst Clear (DMAUSEBURSTCLR)** register to allow the  $\mu$ DMA controller to respond to single and burst requests.
4. Set bit 30 of the **DMA Channel Request Mask Clear (DMAREQMASKCLR)** register to allow the  $\mu$ DMA controller to recognize requests for this channel.

### 9.3.2.2 Configure the Channel Control Structure

Now the channel control structure must be configured.

This example transfers 256 words from one memory buffer to another. Channel 30 is used for a software transfer, and the control structure for channel 30 is at offset 0x1E0 of the channel control table. The channel control structure for channel 30 is located at the offsets shown in Table 9-7.

**Table 9-7. Channel Control Structure Offsets for Channel 30**

Offset	Description
Control Table Base + 0x1E0	Channel 30 Source End Pointer
Control Table Base + 0x1E4	Channel 30 Destination End Pointer
Control Table Base + 0x1E8	Channel 30 Control Word

#### **Configure the Source and Destination**

The source and destination end pointers must be set to the last address for the transfer (inclusive).

1. Program the source end pointer at offset 0x1E0 to the address of the source buffer + 0x3FC.
2. Program the destination end pointer at offset 0x1E4 to the address of the destination buffer + 0x3FC.

The control word at offset 0x1E8 must be programmed according to Table 9-8.

**Table 9-8. Channel Control Word Configuration for Memory Transfer Example**

Field in DMACHCTL	Bits	Value	Description
DSTINC	31:30	2	32-bit destination address increment
DSTSIZE	29:28	2	32-bit destination data size
SRCINC	27:26	2	32-bit source address increment
SRCSIZE	25:24	2	32-bit source data size
reserved	23:18	0	Reserved
ARBSIZE	17:14	3	Arbitrates after 8 transfers
XFERSIZE	13:4	255	Transfer 256 items
NXTUSEBURST	3	0	N/A for this transfer type
XFERMODE	2:0	2	Use Auto-request transfer mode

### 9.3.2.3 Start the Transfer

Now the channel is configured and is ready to start.

1. Enable the channel by setting bit 30 of the **DMA Channel Enable Set (DMAENASET)** register.
2. Issue a transfer request by setting bit 30 of the **DMA Channel Software Request (DMASWREQ)** register.

The  $\mu$ DMA transfer begins. If the interrupt is enabled, then the processor is notified by interrupt when the transfer is complete. If needed, the status can be checked by reading bit 30 of the **DMAENASET** register. This bit is automatically cleared when the transfer is complete. The status can also be checked by reading the `XFERMODE` field of the channel control word at offset 0x1E8. This field is automatically cleared at the end of the transfer.

### 9.3.3 Configuring a Peripheral for Simple Transmit

This example configures the  $\mu$ DMA controller to transmit a buffer of data to a peripheral. The peripheral has a transmit FIFO with a trigger level of 4. The example peripheral uses  $\mu$ DMA channel 7.

#### 9.3.3.1 Configure the Channel Attributes

First, configure the channel attributes:

1. Configure bit 7 of the **DMA Channel Priority Set (DMAPRIOSET)** or **DMA Channel Priority Clear (DMAPRIOCLR)** registers to set the channel to High priority or Default priority.
2. Set bit 7 of the **DMA Channel Primary Alternate Clear (DMAALTCLR)** register to select the primary channel control structure for this transfer.
3. Set bit 7 of the **DMA Channel Useburst Clear (DMAUSEBURSTCLR)** register to allow the  $\mu$ DMA controller to respond to single and burst requests.
4. Set bit 7 of the **DMA Channel Request Mask Clear (DMAREQMASKCLR)** register to allow the  $\mu$ DMA controller to recognize requests for this channel.

#### 9.3.3.2 Configure the Channel Control Structure

This example transfers 64 bytes from a memory buffer to the peripheral's transmit FIFO register using  $\mu$ DMA channel 7. The control structure for channel 7 is at offset 0x070 of the channel control table. The channel control structure for channel 7 is located at the offsets shown in Table 9-9.

**Table 9-9. Channel Control Structure Offsets for Channel 7**

Offset	Description
Control Table Base + 0x070	Channel 7 Source End Pointer
Control Table Base + 0x074	Channel 7 Destination End Pointer
Control Table Base + 0x078	Channel 7 Control Word

#### **Configure the Source and Destination**

The source and destination end pointers must be set to the last address for the transfer (inclusive). Because the peripheral pointer does not change, it simply points to the peripheral's data register.

1. Program the source end pointer at offset 0x070 to the address of the source buffer + 0x3F.
2. Program the destination end pointer at offset 0x074 to the address of the peripheral's transmit FIFO register.

The control word at offset 0x078 must be programmed according to Table 9-10.

**Table 9-10. Channel Control Word Configuration for Peripheral Transmit Example**

Field in DMACHCTL	Bits	Value	Description
DSTINC	31:30	3	Destination address does not increment
DSTSIZE	29:28	0	8-bit destination data size
SRCINC	27:26	0	8-bit source address increment
SRCSIZE	25:24	0	8-bit source data size
reserved	23:18	0	Reserved
ARBSIZE	17:14	2	Arbitrates after 4 transfers
XFERSIZE	13:4	63	Transfer 64 items
NXTUSEBURST	3	0	N/A for this transfer type
XFERMODE	2:0	1	Use Basic transfer mode

**Note:** In this example, it is not important if the peripheral makes a single request or a burst request. Because the peripheral has a FIFO that triggers at a level of 4, the arbitration size is set to 4. If the peripheral does make a burst request, then 4 bytes are transferred, which is what the FIFO can accommodate. If the peripheral makes a single request (if there is any space in the FIFO), then one byte is transferred at a time. If it is important to the application that transfers only be made in bursts, then the Channel Useburst `SET[7]` bit should be set in the **DMA Channel Useburst Set (DMAUSEBURSTSET)** register.

### 9.3.3.3 Start the Transfer

Now the channel is configured and is ready to start.

1. Enable the channel by setting bit 7 of the **DMA Channel Enable Set (DMAENASET)** register.

The  $\mu$ DMA controller is now configured for transfer on channel 7. The controller makes transfers to the peripheral whenever the peripheral asserts a  $\mu$ DMA request. The transfers continue until the entire buffer of 64 bytes has been transferred. When that happens, the  $\mu$ DMA controller disables the channel and sets the `XFERMODE` field of the channel control word to 0 (Stopped). The status of the transfer can be checked by reading bit 7 of the **DMA Channel Enable Set (DMAENASET)** register. This bit is automatically cleared when the transfer is complete. The status can also be checked by reading the `XFERMODE` field of the channel control word at offset 0x078. This field is automatically cleared at the end of the transfer.

If peripheral interrupts are enabled, then the peripheral interrupt handler receives an interrupt when the entire transfer is complete.

## 9.3.4 Configuring a Peripheral for Ping-Pong Receive

This example configures the  $\mu$ DMA controller to continuously receive 8-bit data from a peripheral into a pair of 64-byte buffers. The peripheral has a receive FIFO with a trigger level of 8. The example peripheral uses  $\mu$ DMA channel 8.

### 9.3.4.1 Configure the Channel Attributes

First, configure the channel attributes:

1. Configure bit 8 of the **DMA Channel Priority Set (DMAPRIOSET)** or **DMA Channel Priority Clear (DMAPRIOCLR)** registers to set the channel to High priority or Default priority.



2. Set bit 8 of the **DMA Channel Primary Alternate Clear (DMAALTCLR)** register to select the primary channel control structure for this transfer.
3. Set bit 8 of the **DMA Channel Useburst Clear (DMAUSEBURSTCLR)** register to allow the  $\mu$ DMA controller to respond to single and burst requests.
4. Set bit 8 of the **DMA Channel Request Mask Clear (DMAREQMASKCLR)** register to allow the  $\mu$ DMA controller to recognize requests for this channel.

#### 9.3.4.2 Configure the Channel Control Structure

This example transfers bytes from the peripheral's receive FIFO register into two memory buffers of 64 bytes each. As data is received, when one buffer is full, the  $\mu$ DMA controller switches to use the other.

To use Ping-Pong buffering, both primary and alternate channel control structures must be used. The primary control structure for channel 8 is at offset 0x080 of the channel control table, and the alternate channel control structure is at offset 0x280. The channel control structures for channel 8 are located at the offsets shown in Table 9-11.

**Table 9-11. Primary and Alternate Channel Control Structure Offsets for Channel 8**

Offset	Description
Control Table Base + 0x080	Channel 8 Primary Source End Pointer
Control Table Base + 0x084	Channel 8 Primary Destination End Pointer
Control Table Base + 0x088	Channel 8 Primary Control Word
Control Table Base + 0x280	Channel 8 Alternate Source End Pointer
Control Table Base + 0x284	Channel 8 Alternate Destination End Pointer
Control Table Base + 0x288	Channel 8 Alternate Control Word

#### **Configure the Source and Destination**

The source and destination end pointers must be set to the last address for the transfer (inclusive). Because the peripheral pointer does not change, it simply points to the peripheral's data register. Both the primary and alternate sets of pointers must be configured.

1. Program the primary source end pointer at offset 0x080 to the address of the peripheral's receive buffer.
2. Program the primary destination end pointer at offset 0x084 to the address of ping-pong buffer A + 0x3F.
3. Program the alternate source end pointer at offset 0x280 to the address of the peripheral's receive buffer.
4. Program the alternate destination end pointer at offset 0x284 to the address of ping-pong buffer B + 0x3F.

The primary control word at offset 0x088 and the alternate control word at offset 0x288 are initially programmed the same way.

1. Program the primary channel control word at offset 0x088 according to Table 9-12.
2. Program the alternate channel control word at offset 0x288 according to Table 9-12.

**Table 9-12. Channel Control Word Configuration for Peripheral Ping-Pong Receive Example**

Field in DMACHCTL	Bits	Value	Description
DSTINC	31:30	0	8-bit destination address increment
DSTSIZE	29:28	0	8-bit destination data size
SRCINC	27:26	3	Source address does not increment
SRCSIZE	25:24	0	8-bit source data size
reserved	23:18	0	Reserved
ARBSIZE	17:14	3	Arbitrates after 8 transfers
XFERSIZE	13:4	63	Transfer 64 items
NXTUSEBURST	3	0	N/A for this transfer type
XFERMODE	2:0	3	Use Ping-Pong transfer mode

**Note:** In this example, it is not important if the peripheral makes a single request or a burst request. Because the peripheral has a FIFO that triggers at a level of 8, the arbitration size is set to 8. If the peripheral does make a burst request, then 8 bytes are transferred, which is what the FIFO can accommodate. If the peripheral makes a single request (if there is any data in the FIFO), then one byte is transferred at a time. If it is important to the application that transfers only be made in bursts, then the Channel Useburst `SET[8]` bit should be set in the **DMA Channel Useburst Set (DMAUSEBURSTSET)** register.

#### 9.3.4.3 Configure the Peripheral Interrupt

An interrupt handler should be configured when using  $\mu$ DMA Ping-Pong mode, it is best to use an interrupt handler. However, the Ping-Pong mode can be configured without interrupts by polling. The interrupt handler is triggered after each buffer is complete.

1. Configure and enable an interrupt handler for the peripheral.

#### 9.3.4.4 Enable the $\mu$ DMA Channel

Now the channel is configured and is ready to start.

1. Enable the channel by setting bit 8 of the **DMA Channel Enable Set (DMAENASET)** register.

#### 9.3.4.5 Process Interrupts

The  $\mu$ DMA controller is now configured and enabled for transfer on channel 8. When the peripheral asserts the  $\mu$ DMA request signal, the  $\mu$ DMA controller makes transfers into buffer A using the primary channel control structure. When the primary transfer to buffer A is complete, it switches to the alternate channel control structure and makes transfers into buffer B. At the same time, the primary channel control word mode field is configured to indicate Stopped, and an interrupt is

When an interrupt is triggered, the interrupt handler must determine which buffer is complete and process the data or set a flag that the data must be processed by non-interrupt buffer processing code. Then the next buffer transfer must be set up.

In the interrupt handler:

1. Read the primary channel control word at offset 0x088 and check the `XFERMODE` field. If the field is 0, this means buffer A is complete. If buffer A is complete, then:
  - a. Process the newly received data in buffer A or signal the buffer processing code that buffer A has data available.

- b. Reprogram the primary channel control word at offset 0x88 according to Table 9-12 on page 250.
2. Read the alternate channel control word at offset 0x288 and check the `XFERMODE` field. If the field is 0, this means buffer B is complete. If buffer B is complete, then:
  - a. Process the newly received data in buffer B or signal the buffer processing code that buffer B has data available.
  - b. Reprogram the alternate channel control word at offset 0x288 according to Table 9-12 on page 250.

### 9.3.5 Configuring Alternate Channels

Alternate peripherals can be assigned to each  $\mu$ DMA channel using the **DMACHALT** register. Each bit represents a  $\mu$ DMA channel. If the bit is set, then the alternate peripheral is used for the channel.

Refer to Table 9-1 on page 232 for alternate channel assignments.

For example, to use SS11 Receive on channel 8 instead of UART0, set bit 8 of the **DMACHALT** register.

## 9.4 Register Map

Table 9-13 on page 251 lists the  $\mu$ DMA channel control structures and registers. The channel control structure shows the layout of one entry in the channel control table. The channel control table is located in system memory, and the location is determined by the application, that is, the base address is n/a (not applicable). In the table below, the offset for the channel control structures is the offset from the entry in the channel control table. See “Channel Configuration” on page 234 and Table 9-3 on page 235 for a description of how the entries in the channel control table are located in memory. The  $\mu$ DMA register addresses are given as a hexadecimal increment, relative to the  $\mu$ DMA base address of 0x400F.F000. Note that the  $\mu$ DMA module clock must be enabled before the registers can be programmed (see page 158).

**Table 9-13.  $\mu$ DMA Register Map**

Offset	Name	Type	Reset	Description	See page
<b><math>\mu</math>DMA Channel Control Structure (Offset from Channel Control Table Base)</b>					
0x000	DMASRCENDP	R/W	-	DMA Channel Source Address End Pointer	253
0x004	DMADSTENDP	R/W	-	DMA Channel Destination Address End Pointer	254
0x008	DMACHCTL	R/W	-	DMA Channel Control Word	255
<b><math>\mu</math>DMA Registers (Offset from <math>\mu</math>DMA Base Address)</b>					
0x000	DMASTAT	RO	0x001F.0000	DMA Status	260
0x004	DMACFG	WO	-	DMA Configuration	262
0x008	DMACTLBASE	R/W	0x0000.0000	DMA Channel Control Base Pointer	263
0x00C	DMAALTBASE	RO	0x0000.0200	DMA Alternate Channel Control Base Pointer	264
0x010	DMAWAITSTAT	RO	0x0000.0000	DMA Channel Wait-on-Request Status	265
0x014	DMASWREQ	WO	-	DMA Channel Software Request	266

Table 9-13.  $\mu$ DMA Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0x018	DMAUSEBURSTSET	R/W	0x0000.0000	DMA Channel Useburst Set	267
0x01C	DMAUSEBURSTCLR	WO	-	DMA Channel Useburst Clear	268
0x020	DMAREQMASKSET	R/W	0x0000.0000	DMA Channel Request Mask Set	269
0x024	DMAREQMASKCLR	WO	-	DMA Channel Request Mask Clear	270
0x028	DMAENASET	R/W	0x0000.0000	DMA Channel Enable Set	271
0x02C	DMAENACL	WO	-	DMA Channel Enable Clear	272
0x030	DMAALTSET	R/W	0x0000.0000	DMA Channel Primary Alternate Set	273
0x034	DMAALTCLR	WO	-	DMA Channel Primary Alternate Clear	274
0x038	DMAPRIOSET	R/W	0x0000.0000	DMA Channel Priority Set	275
0x03C	DMAPRIOCLR	WO	-	DMA Channel Priority Clear	276
0x04C	DMAERRCLR	R/W	0x0000.0000	DMA Bus Error Clear	277
0x500	DMACHALT	R/W	0x0000.0000	DMA Channel Alternate Select	278
0xFD0	DMAPeriphID4	RO	0x0000.0004	DMA Peripheral Identification 4	283
0xFE0	DMAPeriphID0	RO	0x0000.0030	DMA Peripheral Identification 0	279
0xFE4	DMAPeriphID1	RO	0x0000.00B2	DMA Peripheral Identification 1	280
0xFE8	DMAPeriphID2	RO	0x0000.000B	DMA Peripheral Identification 2	281
0xFEC	DMAPeriphID3	RO	0x0000.0000	DMA Peripheral Identification 3	282
0xFF0	DMAPrimeCellID0	RO	0x0000.000D	DMA PrimeCell Identification 0	284
0xFF4	DMAPrimeCellID1	RO	0x0000.00F0	DMA PrimeCell Identification 1	285
0xFF8	DMAPrimeCellID2	RO	0x0000.0005	DMA PrimeCell Identification 2	286
0xFFC	DMAPrimeCellID3	RO	0x0000.00B1	DMA PrimeCell Identification 3	287

## 9.5 $\mu$ DMA Channel Control Structure

The  $\mu$ DMA Channel Control Structure holds the transfer settings for a  $\mu$ DMA channel. Each channel has two control structures, which are located in a table in system memory. Refer to “Channel Configuration” on page 234 for an explanation of the Channel Control Table and the Channel Control Structure.

The channel control structure is one entry in the channel control table. Each channel has a primary and alternate structure. The primary control structures are located at offsets 0x0, 0x10, 0x20 and so on. The alternate control structures are located at offsets 0x200, 0x210, 0x220, and so on.

## Register 1: DMA Channel Source Address End Pointer (DMASRCENDP), offset 0x000

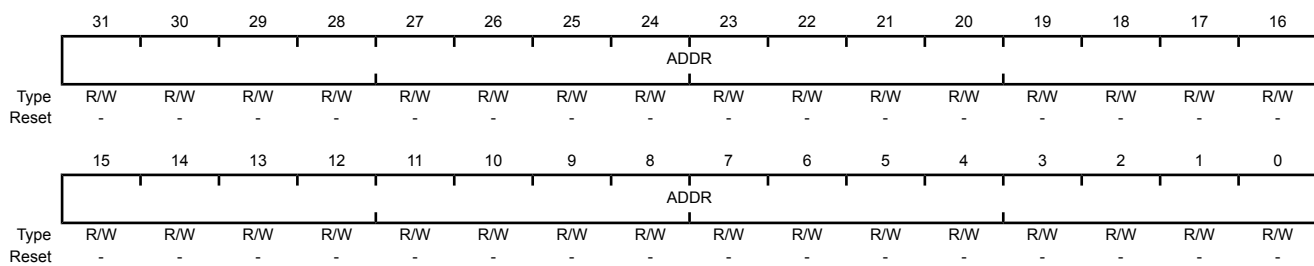
**DMA Channel Source Address End Pointer (DMASRCENDP)** is part of the Channel Control Structure and is used to specify the source address for a  $\mu$ DMA transfer.

The  $\mu$ DMA controller can transfer data to and from the on-chip SRAM. However, because the Flash memory and ROM are located on a separate internal bus, it is not possible to transfer data from the Flash memory or ROM with the  $\mu$ DMA controller.

**Note:** The offset specified is from the base address of the control structure in system memory, not the  $\mu$ DMA module base address.

### DMA Channel Source Address End Pointer (DMASRCENDP)

Base n/a  
Offset 0x000  
Type R/W, reset -



Bit/Field	Name	Type	Reset	Description
31:0	ADDR	R/W	-	Source Address End Pointer  This field points to the last address of the $\mu$ DMA transfer source (inclusive). If the source address is not incrementing (the <b>SRCINC</b> field in the <b>DMACHCTL</b> register is 0x3), then this field points at the source location itself (such as a peripheral data register).

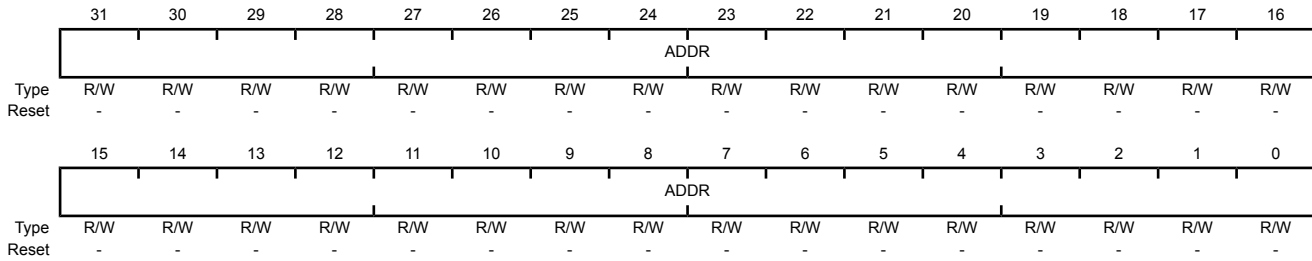
## Register 2: DMA Channel Destination Address End Pointer (DMADSTENDP), offset 0x004

**DMA Channel Destination Address End Pointer (DMADSTENDP)** is part of the Channel Control Structure and is used to specify the destination address for a  $\mu$ DMA transfer.

**Note:** The offset specified is from the base address of the control structure in system memory, not the  $\mu$ DMA module base address.

### DMA Channel Destination Address End Pointer (DMADSTENDP)

Base n/a  
 Offset 0x004  
 Type R/W, reset -



Bit/Field	Name	Type	Reset	Description
31:0	ADDR	R/W	-	Destination Address End Pointer

This field points to the last address of the  $\mu$ DMA transfer destination (inclusive). If the destination address is not incrementing (the `DSTINC` field in the `DMACHCTL` register is 0x3), then this field points at the destination location itself (such as a peripheral data register).

### Register 3: DMA Channel Control Word (DMACHCTL), offset 0x008

**DMA Channel Control Word (DMACHCTL)** is part of the Channel Control Structure and is used to specify parameters of a  $\mu$ DMA transfer.

**Note:** The offset specified is from the base address of the control structure in system memory, not the  $\mu$ DMA module base address.

#### DMA Channel Control Word (DMACHCTL)

Base n/a

Offset 0x008

Type R/W, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSTINC		DSTSIZE		SRCINC		SRCSIZE		reserved				ARBSIZE			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARBSIZE		XFERSIZE										NXTUSEBURST	XFERMODE		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description										
31:30	DSTINC	R/W	-	<p>Destination Address Increment</p> <p>This field configures the destination address increment.</p> <p>The address increment value must be equal or greater than the value of the destination size (DSTSIZE).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Byte Increment by 8-bit locations</td> </tr> <tr> <td>0x1</td> <td>Half-word Increment by 16-bit locations</td> </tr> <tr> <td>0x2</td> <td>Word Increment by 32-bit locations</td> </tr> <tr> <td>0x3</td> <td>No increment Address remains set to the value of the Destination Address End Pointer (DMADSTENDP) for the channel</td> </tr> </tbody> </table>	Value	Description	0x0	Byte Increment by 8-bit locations	0x1	Half-word Increment by 16-bit locations	0x2	Word Increment by 32-bit locations	0x3	No increment Address remains set to the value of the Destination Address End Pointer (DMADSTENDP) for the channel
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Bit/Field	Name	Type	Reset	Description										
29:28	DSTSIZE	R/W	-	<p>Destination Data Size</p> <p>This field configures the destination item data size.</p> <p><b>Note:</b> DSTSIZE must be the same as SRCSIZE.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Byte 8-bit data size</td> </tr> <tr> <td>0x1</td> <td>Half-word 16-bit data size</td> </tr> <tr> <td>0x2</td> <td>Word 32-bit data size</td> </tr> <tr> <td>0x3</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	0x0	Byte 8-bit data size	0x1	Half-word 16-bit data size	0x2	Word 32-bit data size	0x3	Reserved
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0x0	Byte 8-bit data size													
0x1	Half-word 16-bit data size													
0x2	Word 32-bit data size													
0x3	Reserved													
27:26	SRCINC	R/W	-	<p>Source Address Increment</p> <p>This field configures the source address increment.</p> <p>The address increment value must be equal or greater than the value of the source size (SRCSIZE).</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Byte Increment by 8-bit locations</td> </tr> <tr> <td>0x1</td> <td>Half-word Increment by 16-bit locations</td> </tr> <tr> <td>0x2</td> <td>Word Increment by 32-bit locations</td> </tr> <tr> <td>0x3</td> <td>No increment Address remains set to the value of the Source Address End Pointer (DMASRCENDE) for the channel</td> </tr> </tbody> </table>	Value	Description	0x0	Byte Increment by 8-bit locations	0x1	Half-word Increment by 16-bit locations	0x2	Word Increment by 32-bit locations	0x3	No increment Address remains set to the value of the Source Address End Pointer (DMASRCENDE) for the channel
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25:24	SRCSIZE	R/W	-	<p>Source Data Size</p> <p>This field configures the source item data size.</p> <p><b>Note:</b> DSTSIZE must be the same as SRCSIZE.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Byte 8-bit data size.</td> </tr> <tr> <td>0x1</td> <td>Half-word 16-bit data size.</td> </tr> <tr> <td>0x2</td> <td>Word 32-bit data size.</td> </tr> <tr> <td>0x3</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	0x0	Byte 8-bit data size.	0x1	Half-word 16-bit data size.	0x2	Word 32-bit data size.	0x3	Reserved
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0x0	Byte 8-bit data size.													
0x1	Half-word 16-bit data size.													
0x2	Word 32-bit data size.													
0x3	Reserved													



Bit/Field	Name	Type	Reset	Description																										
23:18	reserved	R/W	-	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																										
17:14	ARBSIZE	R/W	-	<p>Arbitration Size</p> <p>This field configures the number of transfers that can occur before the <math>\mu</math>DMA controller re-arbitrates. The possible arbitration rate configurations represent powers of 2 and are shown below.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>1 Transfer</td> </tr> <tr> <td></td> <td>Arbitrates after each <math>\mu</math>DMA transfer</td> </tr> <tr> <td>0x1</td> <td>2 Transfers</td> </tr> <tr> <td>0x2</td> <td>4 Transfers</td> </tr> <tr> <td>0x3</td> <td>8 Transfers</td> </tr> <tr> <td>0x4</td> <td>16 Transfers</td> </tr> <tr> <td>0x5</td> <td>32 Transfers</td> </tr> <tr> <td>0x6</td> <td>64 Transfers</td> </tr> <tr> <td>0x7</td> <td>128 Transfers</td> </tr> <tr> <td>0x8</td> <td>256 Transfers</td> </tr> <tr> <td>0x9</td> <td>512 Transfers</td> </tr> <tr> <td>0xA-0xF</td> <td>1024 Transfers</td> </tr> </tbody> </table> <p>In this configuration, no arbitration occurs during the <math>\mu</math>DMA transfer because the maximum transfer size is 1024.</p>	Value	Description	0x0	1 Transfer		Arbitrates after each $\mu$ DMA transfer	0x1	2 Transfers	0x2	4 Transfers	0x3	8 Transfers	0x4	16 Transfers	0x5	32 Transfers	0x6	64 Transfers	0x7	128 Transfers	0x8	256 Transfers	0x9	512 Transfers	0xA-0xF	1024 Transfers
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0x6	64 Transfers																													
0x7	128 Transfers																													
0x8	256 Transfers																													
0x9	512 Transfers																													
0xA-0xF	1024 Transfers																													
13:4	XFERSIZE	R/W	-	<p>Transfer Size (minus 1)</p> <p>This field configures the total number of items to transfer. The value of this field is 1 less than the number to transfer (value 0 means transfer 1 item). The maximum value for this 10-bit field is 1023 which represents a transfer size of 1024 items.</p> <p>The transfer size is the number of items, not the number of bytes. If the data size is 32 bits, then this value is the number of 32-bit words to transfer.</p> <p>The <math>\mu</math>DMA controller updates this field immediately prior to entering the arbitration process, so it contains the number of outstanding items that is necessary to complete the <math>\mu</math>DMA cycle.</p>																										
3	NXTUSEBURST	R/W	-	<p>Next Useburst</p> <p>This field controls whether the Useburst <math>SET[n]</math> bit is automatically set for the last transfer of a peripheral scatter-gather operation. Normally, for the last transfer, if the number of remaining items to transfer is less than the arbitration size, the <math>\mu</math>DMA controller uses single transfers to complete the transaction. If this bit is set, then the controller uses a burst transfer to complete the last transfer.</p>																										

Bit/Field	Name	Type	Reset	Description																		
2:0	XFERMODE	R/W	-	<p><math>\mu</math>DMA Transfer Mode</p> <p>This field configures the operating mode of the <math>\mu</math>DMA cycle. Refer to “Transfer Modes” on page 236 for a detailed explanation of transfer modes.</p> <p>Because this register is in system RAM, it has no reset value. Therefore, this field should be initialized to 0 before the channel is enabled.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Stop</td> </tr> <tr> <td>0x1</td> <td>Basic</td> </tr> <tr> <td>0x2</td> <td>Auto-Request</td> </tr> <tr> <td>0x3</td> <td>Ping-Pong</td> </tr> <tr> <td>0x4</td> <td>Memory Scatter-Gather</td> </tr> <tr> <td>0x5</td> <td>Alternate Memory Scatter-Gather</td> </tr> <tr> <td>0x6</td> <td>Peripheral Scatter-Gather</td> </tr> <tr> <td>0x7</td> <td>Alternate Peripheral Scatter-Gather</td> </tr> </tbody> </table>	Value	Description	0x0	Stop	0x1	Basic	0x2	Auto-Request	0x3	Ping-Pong	0x4	Memory Scatter-Gather	0x5	Alternate Memory Scatter-Gather	0x6	Peripheral Scatter-Gather	0x7	Alternate Peripheral Scatter-Gather
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0x7	Alternate Peripheral Scatter-Gather																					

**XFERMODE Bit Field Values.**

**Stop**

Channel is stopped or configuration data is invalid. No more transfers can occur.

**Basic**

For each trigger (whether from a peripheral or a software request), the  $\mu$ DMA controller performs the number of transfers specified by the `ARBSIZE` field.

**Auto-Request**

The initial request (software- or peripheral-initiated) is sufficient to complete the entire transfer of `XFERSIZE` items without any further requests.

**Ping-Pong**

This mode uses both the primary and alternate control structures for this channel. When the number of transfers specified by the `XFERSIZE` field have completed for the current control structure (primary or alternate), the  $\mu$ DMA controller switches to the other one. These switches continue until one of the control structures is not set to ping-pong mode. At that point, the  $\mu$ DMA controller stops. An interrupt is generated on completion of the transfers configured by each control structure. See “Ping-Pong” on page 236.

**Memory Scatter-Gather**

When using this mode, the primary control structure for the channel is configured to allow a list of operations (tasks) to be performed. The source address pointer specifies the start of a table of tasks to be copied to the alternate control structure for this channel. The `XFERMODE` field for the alternate control structure should be configured to 0x5 (Alternate memory scatter-gather) to perform the task. When the task completes, the  $\mu$ DMA switches back to the primary channel control structure, which then copies the next task to the alternate control structure. This process continues until the table of tasks is empty. The last task must have an `XFERMODE` value other than 0x5. Note that for continuous operation, the last task can update the primary channel control structure back to the start of the list or to another list. See “Memory Scatter-Gather” on page 237.

**Alternate Memory Scatter-Gather**

This value must be used in the alternate channel control data structure when the  $\mu$ DMA controller operates in Memory Scatter-Gather mode.

**Peripheral Scatter-Gather**

This value must be used in the primary channel control data structure when the  $\mu$ DMA controller operates in Peripheral Scatter-Gather mode. In this mode, the  $\mu$ DMA controller operates exactly the same as in Memory Scatter-Gather mode, except that instead of performing the number of transfers specified by the `XFERSIZE` field in the alternate control structure at one time, the  $\mu$ DMA controller only performs the number of transfers specified by the `ARBSIZE` field per trigger; see Basic mode for details. See “Peripheral Scatter-Gather” on page 241.

**Alternate Peripheral Scatter-Gather**

This value must be used in the alternate channel control data structure when the  $\mu$ DMA controller operates in Peripheral Scatter-Gather mode.

## 9.6 $\mu$ DMA Register Descriptions

The register addresses given are relative to the  $\mu$ DMA base address of 0x400F.F000.

## Register 4: DMA Status (DMASTAT), offset 0x000

The **DMA Status (DMASTAT)** register returns the status of the  $\mu$ DMA controller. You cannot read this register when the  $\mu$ DMA controller is in the reset state.

### DMA Status (DMASTAT)

Base 0x400F.F000

Offset 0x000

Type RO, reset 0x001F.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved											DMACHANS				
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								STATE				reserved			MASTEN
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description																								
31:21	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																								
20:16	DMACHANS	RO	0x1F	Available $\mu$ DMA Channels Minus 1  This field contains a value equal to the number of $\mu$ DMA channels the $\mu$ DMA controller is configured to use, minus one. The value of 0x1F corresponds to 32 $\mu$ DMA channels.																								
15:8	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																								
7:4	STATE	RO	0x0	Control State Machine Status  This field shows the current status of the control state machine. Status can be one of the following.  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>Idle</td></tr> <tr><td>0x1</td><td>Reading channel controller data.</td></tr> <tr><td>0x2</td><td>Reading source end pointer.</td></tr> <tr><td>0x3</td><td>Reading destination end pointer.</td></tr> <tr><td>0x4</td><td>Reading source data.</td></tr> <tr><td>0x5</td><td>Writing destination data.</td></tr> <tr><td>0x6</td><td>Waiting for <math>\mu</math>DMA request to clear.</td></tr> <tr><td>0x7</td><td>Writing channel controller data.</td></tr> <tr><td>0x8</td><td>Stalled</td></tr> <tr><td>0x9</td><td>Done</td></tr> <tr><td>0xA-0xF</td><td>Undefined</td></tr> </tbody> </table>	Value	Description	0x0	Idle	0x1	Reading channel controller data.	0x2	Reading source end pointer.	0x3	Reading destination end pointer.	0x4	Reading source data.	0x5	Writing destination data.	0x6	Waiting for $\mu$ DMA request to clear.	0x7	Writing channel controller data.	0x8	Stalled	0x9	Done	0xA-0xF	Undefined
Value	Description																											
0x0	Idle																											
0x1	Reading channel controller data.																											
0x2	Reading source end pointer.																											
0x3	Reading destination end pointer.																											
0x4	Reading source data.																											
0x5	Writing destination data.																											
0x6	Waiting for $\mu$ DMA request to clear.																											
0x7	Writing channel controller data.																											
0x8	Stalled																											
0x9	Done																											
0xA-0xF	Undefined																											
3:1	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																								

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Bit/Field	Name	Type	Reset	Description
0	MASTEN	RO	0	Master Enable Status
				Value Description
				0 The $\mu$ DMA controller is disabled.
				1 The $\mu$ DMA controller is enabled.

## Register 5: DMA Configuration (DMACFG), offset 0x004

The **DMACFG** register controls the configuration of the  $\mu$ DMA controller.

### DMA Configuration (DMACFG)

Base 0x400F.F000

Offset 0x004

Type WO, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															MASTEN
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:1	reserved	WO	-	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	MASTEN	WO	-	Controller Master Enable
				Value Description
				0 Disables the $\mu$ DMA controller.
				1 Enables $\mu$ DMA controller.

**Register 6: DMA Channel Control Base Pointer (DMACTLBASE), offset 0x008**

The **DMACTLBASE** register must be configured so that the base pointer points to a location in system memory.

The amount of system memory that must be assigned to the  $\mu$ DMA controller depends on the number of  $\mu$ DMA channels used and whether the alternate channel control data structure is used. See “Channel Configuration” on page 234 for details about the Channel Control Table. The base address must be aligned on a 1024-byte boundary. This register cannot be read when the  $\mu$ DMA controller is in the reset state.

**DMA Channel Control Base Pointer (DMACTLBASE)**

Base 0x400F.F000

Offset 0x008

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ADDR															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ADDR						reserved									
Type	R/W	R/W	R/W	R/W	R/W	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

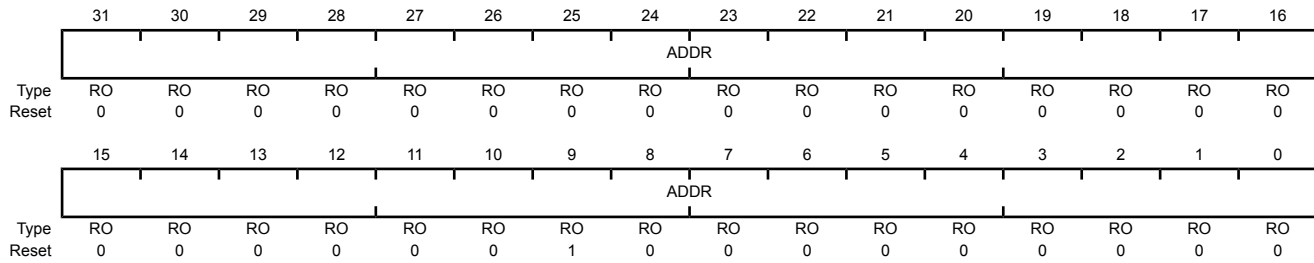
Bit/Field	Name	Type	Reset	Description
31:10	ADDR	R/W	0x0000.00	Channel Control Base Address  This field contains the pointer to the base address of the channel control table. The base address must be 1024-byte aligned.
9:0	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

### Register 7: DMA Alternate Channel Control Base Pointer (DMAALTBASE), offset 0x00C

The **DMAALTBASE** register returns the base address of the alternate channel control data. This register removes the necessity for application software to calculate the base address of the alternate channel control structures. This register cannot be read when the  $\mu$ DMA controller is in the reset state.

#### DMA Alternate Channel Control Base Pointer (DMAALTBASE)

Base 0x400F.F000  
 Offset 0x00C  
 Type RO, reset 0x0000.0200



Bit/Field	Name	Type	Reset	Description
31:0	ADDR	RO	0x0000.0200	Alternate Channel Address Pointer  This field provides the base address of the alternate channel control structures.



## Register 8: DMA Channel Wait-on-Request Status (DMAWAITSTAT), offset 0x010

This read-only register indicates that the  $\mu$ DMA channel is waiting on a request. A peripheral can hold off the  $\mu$ DMA from performing a single request until the peripheral is ready for a burst request to enhance the  $\mu$ DMA performance. The use of this feature is dependent on the design of the peripheral and is not controllable by software in any way. This register cannot be read when the  $\mu$ DMA controller is in the reset state.

### DMA Channel Wait-on-Request Status (DMAWAITSTAT)

Base 0x400F.F000  
Offset 0x010  
Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WAITREQ[n]															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WAITREQ[n]															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
-----------	------	------	-------	-------------

31:0	WAITREQ[n]	RO	0x0000.0000	Channel [n] Wait Status
------	------------	----	-------------	-------------------------

These bits provide the channel wait-on-request status. Bit 0 corresponds to channel 0.

Value Description

- |   |  |
|---|--|
| 1 | The corresponding channel is waiting on a request.     |
| 0 | The corresponding channel is not waiting on a request. |

### Register 9: DMA Channel Software Request (DMASWREQ), offset 0x014

Each bit of the **DMASWREQ** register represents the corresponding  $\mu$ DMA channel. Setting a bit generates a request for the specified  $\mu$ DMA channel.

#### DMA Channel Software Request (DMASWREQ)

Base 0x400F.F000

Offset 0x014

Type WO, reset -



Bit/Field	Name	Type	Reset	Description				
31:0	SWREQ[n]	WO	-	<p>Channel [n] Software Request</p> <p>These bits generate software requests. Bit 0 corresponds to channel 0.</p> <p>Value Description</p> <table border="0"> <tr> <td>1</td> <td>Generate a software request for the corresponding channel.</td> </tr> <tr> <td>0</td> <td>No request generated.</td> </tr> </table> <p>These bits are automatically cleared when the software request has been completed.</p>	1	Generate a software request for the corresponding channel.	0	No request generated.
1	Generate a software request for the corresponding channel.							
0	No request generated.							

**Register 10: DMA Channel Useburst Set (DMAUSEBURSTSET), offset 0x018**

Each bit of the **DMAUSEBURSTSET** register represents the corresponding  $\mu$ DMA channel. Setting a bit disables the channel's single request input from generating requests, configuring the channel to only accept burst requests. Reading the register returns the status of USEBURST.

If the amount of data to transfer is a multiple of the arbitration (burst) size, the corresponding  $SET[n]$  bit is cleared after completing the final transfer. If there are fewer items remaining to transfer than the arbitration (burst) size, the  $\mu$ DMA controller automatically clears the corresponding  $SET[n]$  bit, allowing the remaining items to transfer using single requests. In order to resume transfers using burst requests, the corresponding bit must be set again. A bit should not be set if the corresponding peripheral does not support the burst request model.

Refer to “Request Types” on page 233 for more details about request types.

**DMA Channel Useburst Set (DMAUSEBURSTSET)**

Base 0x400F.F000  
Offset 0x018  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	SET[n]	R/W	0x0000.0000	Channel [n] Useburst Set

Value	Description
0	$\mu$ DMA channel [n] responds to single or burst requests.
1	$\mu$ DMA channel [n] responds only to burst requests.

Bit 0 corresponds to channel 0. This bit is automatically cleared as described above. A bit can also be manually cleared by setting the corresponding  $CLR[n]$  bit in the **DMAUSEBURSTCLR** register.

### Register 11: DMA Channel Useburst Clear (DMAUSEBURSTCLR), offset 0x01C

Each bit of the **DMAUSEBURSTCLR** register represents the corresponding  $\mu$ DMA channel. Setting a bit clears the corresponding **SET[n]** bit in the **DMAUSEBURSTSET** register.

#### DMA Channel Useburst Clear (DMAUSEBURSTCLR)

Base 0x400F.F000

Offset 0x01C

Type WO, reset -



Bit/Field	Name	Type	Reset	Description
31:0	CLR[n]	WO	-	Channel [n] Useburst Clear

Value Description

0 No effect.

1 Setting a bit clears the corresponding **SET[n]** bit in the **DMAUSEBURSTSET** register meaning that  $\mu$ DMA channel [n] responds to single and burst requests.

## Register 12: DMA Channel Request Mask Set (DMAREQMASKSET), offset 0x020

Each bit of the **DMAREQMASKSET** register represents the corresponding  $\mu$ DMA channel. Setting a bit disables  $\mu$ DMA requests for the channel. Reading the register returns the request mask status. When a  $\mu$ DMA channel's request is masked, that means the peripheral can no longer request  $\mu$ DMA transfers. The channel can then be used for software-initiated transfers.

### DMA Channel Request Mask Set (DMAREQMASKSET)

Base 0x400F.F000  
Offset 0x020  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	SET[n]	R/W	0x0000.0000	Channel [n] Request Mask Set

#### Value Description

Value	Description
0	The peripheral associated with channel [n] is enabled to request $\mu$ DMA transfers.
1	The peripheral associated with channel [n] is not able to request $\mu$ DMA transfers. Channel [n] may be used for software-initiated transfers.

Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding `CLR[n]` bit in the **DMAREQMASKCLR** register.

### Register 13: DMA Channel Request Mask Clear (DMAREQMASKCLR), offset 0x024

Each bit of the **DMAREQMASKCLR** register represents the corresponding  $\mu$ DMA channel. Setting a bit clears the corresponding **SET[n]** bit in the **DMAREQMASKSET** register.

#### DMA Channel Request Mask Clear (DMAREQMASKCLR)

Base 0x400F.F000

Offset 0x024

Type WO, reset -



Bit/Field	Name	Type	Reset	Description
31:0	CLR[n]	WO	-	Channel [n] Request Mask Clear

**Value Description**

- 0 No effect.
- 1 Setting a bit clears the corresponding **SET[n]** bit in the **DMAREQMASKSET** register meaning that the peripheral associated with channel [n] is enabled to request  $\mu$ DMA transfers.

## Register 14: DMA Channel Enable Set (DMAENASET), offset 0x028

Each bit of the **DMAENASET** register represents the corresponding  $\mu$ DMA channel. Setting a bit enables the corresponding  $\mu$ DMA channel. Reading the register returns the enable status of the channels. If a channel is enabled but the request mask is set (**DMAREQMASKSET**), then the channel can be used for software-initiated transfers.

### DMA Channel Enable Set (DMAENASET)

Base 0x400F.F000  
Offset 0x028  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	SET[n]	R/W	0x0000.0000	Channel [n] Enable Set

Value	Description
0	$\mu$ DMA Channel [n] is disabled.
1	$\mu$ DMA Channel [n] is enabled.

Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding **CLR[n]** bit in the **DMAENACLR** register.

### Register 15: DMA Channel Enable Clear (DMAENACLRL), offset 0x02C

Each bit of the **DMAENACLRL** register represents the corresponding  $\mu$ DMA channel. Setting a bit clears the corresponding **SET[n]** bit in the **DMAENASET** register.

#### DMA Channel Enable Clear (DMAENACLRL)

Base 0x400F.F000

Offset 0x02C

Type WO, reset -



Bit/Field	Name	Type	Reset	Description
31:0	CLR[n]	WO	-	Clear Channel [n] Enable Clear

Value	Description
0	No effect.
1	Setting a bit clears the corresponding <b>SET[n]</b> bit in the <b>DMAENASET</b> register meaning that channel [n] is disabled for $\mu$ DMA transfers.

**Note:** The controller disables a channel when it completes the  $\mu$ DMA cycle.



## Register 16: DMA Channel Primary Alternate Set (DMAALTSET), offset 0x030

Each bit of the **DMAALTSET** register represents the corresponding  $\mu$ DMA channel. Setting a bit configures the  $\mu$ DMA channel to use the alternate control data structure. Reading the register returns the status of which control data structure is in use for the corresponding  $\mu$ DMA channel.

### DMA Channel Primary Alternate Set (DMAALTSET)

Base 0x400F.F000  
Offset 0x030  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	SET[n]	R/W	0x0000.0000	Channel [n] Alternate Set

#### Value Description

- |   |   |
|---|---|
| 0 | $\mu$ DMA channel [n] is using the primary control structure.   |
| 1 | $\mu$ DMA channel [n] is using the alternate control structure. |

Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding CLR[n] bit in the **DMAALTCLR** register.

**Note:** For Ping-Pong and Scatter-Gather cycle types, the  $\mu$ DMA controller automatically sets these bits to select the alternate channel control data structure.

## Register 17: DMA Channel Primary Alternate Clear (DMAALTCLR), offset 0x034

Each bit of the **DMAALTCLR** register represents the corresponding  $\mu$ DMA channel. Setting a bit clears the corresponding **SET[n]** bit in the **DMAALTSET** register.

### DMA Channel Primary Alternate Clear (DMAALTCLR)

Base 0x400F.F000

Offset 0x034

Type WO, reset -



Bit/Field	Name	Type	Reset	Description
31:0	CLR[n]	WO	-	Channel [n] Alternate Clear

Value	Description
0	No effect.
1	Setting a bit clears the corresponding <b>SET[n]</b> bit in the <b>DMAALTSET</b> register meaning that channel [n] is using the primary control structure.

**Note:** For Ping-Pong and Scatter-Gather cycle types, the  $\mu$ DMA controller automatically sets these bits to select the alternate channel control data structure.

## Register 18: DMA Channel Priority Set (DMAPRIOSET), offset 0x038

Each bit of the **DMAPRIOSET** register represents the corresponding  $\mu$ DMA channel. Setting a bit configures the  $\mu$ DMA channel to have a high priority level. Reading the register returns the status of the channel priority mask.

### DMA Channel Priority Set (DMAPRIOSET)

Base 0x400F.F000  
Offset 0x038  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SET[n]															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:0	SET[n]	R/W	0x0000.0000	Channel [n] Priority Set

#### Value Description

- 0  $\mu$ DMA channel [n] is using the default priority level.
- 1  $\mu$ DMA channel [n] is using a high priority level.

Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding CLR[n] bit in the **DMAPRIOCLR** register.

### Register 19: DMA Channel Priority Clear (DMAPRIOCLR), offset 0x03C

Each bit of the **DMAPRIOCLR** register represents the corresponding  $\mu$ DMA channel. Setting a bit clears the corresponding **SET[n]** bit in the **DMAPRIOSET** register.

#### DMA Channel Priority Clear (DMAPRIOCLR)

Base 0x400F.F000

Offset 0x03C

Type WO, reset -



Bit/Field	Name	Type	Reset	Description
31:0	CLR[n]	WO	-	Channel [n] Priority Clear
				Value Description
				0 No effect.
				1 Setting a bit clears the corresponding <b>SET[n]</b> bit in the <b>DMAPRIOSET</b> register meaning that channel [n] is using the default priority level.

**Register 20: DMA Bus Error Clear (DMAERRCLR), offset 0x04C**

The **DMAERRCLR** register is used to read and clear the  $\mu$ DMA bus error status. The error status is set if the  $\mu$ DMA controller encountered a bus error while performing a transfer. If a bus error occurs on a channel, that channel is automatically disabled by the  $\mu$ DMA controller. The other channels are unaffected.

**DMA Bus Error Clear (DMAERRCLR)**

Base 0x400F.F000  
Offset 0x04C  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															ERRCLR
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

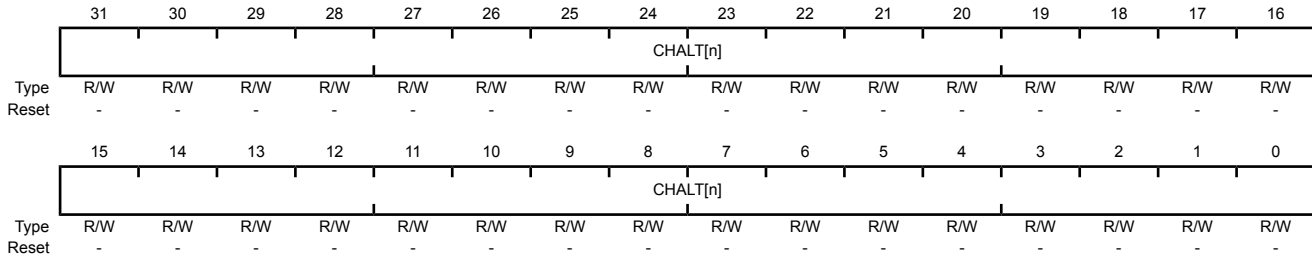
Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	ERRCLR	R/W1C	0	$\mu$ DMA Bus Error Status
				Value Description
				0 No bus error is pending.
				1 A bus error is pending.
				This bit is cleared by writing a 1 to it.

## Register 21: DMA Channel Alternate Select (DMACHALT), offset 0x500

Each bit of the **DMACHALT** register represents the corresponding  $\mu$ DMA channel. Setting a bit selects the alternate channel assignment as specified in Table 9-1 on page 232.

### DMA Channel Alternate Select (DMACHALT)

Base 0x400F.F000  
 Offset 0x500  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:0	CHALT[n]	R/W	-	Channel [n] Alternate Assignment Select
				Value Description
				0 Use the primary channel assignment.
				1 Use the alternate channel assignment.

**Register 22: DMA Peripheral Identification 0 (DMAPeriphID0), offset 0xFE0**

The **DMAPeriphIDn** registers are hard-coded, and the fields within the registers determine the reset values.

**DMA Peripheral Identification 0 (DMAPeriphID0)**

Base 0x400F.F000

Offset 0xFE0

Type RO, reset 0x0000.0030

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID0							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID0	RO	0x30	$\mu$ DMA Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.

### Register 23: DMA Peripheral Identification 1 (DMAPeriphID1), offset 0xFE4

The DMAPeriphIDn registers are hard-coded, and the fields within the registers determine the reset values.

#### DMA Peripheral Identification 1 (DMAPeriphID1)

Base 0x400F.F000  
 Offset 0xFE4  
 Type RO, reset 0x0000.00B2

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID1							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID1	RO	0xB2	$\mu$ DMA Peripheral ID Register [15:8] Can be used by software to identify the presence of this peripheral.



## Register 24: DMA Peripheral Identification 2 (DMAPeriphID2), offset 0xFE8

The **DMAPeriphIDn** registers are hard-coded, and the fields within the registers determine the reset values.

### DMA Peripheral Identification 2 (DMAPeriphID2)

Base 0x400F.F000

Offset 0xFE8

Type RO, reset 0x0000.000B

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID2							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID2	RO	0x0B	<p>μDMA Peripheral ID Register [23:16]</p> <p>Can be used by software to identify the presence of this peripheral.</p>

## Register 25: DMA Peripheral Identification 3 (DMAPeriphID3), offset 0xFEC

The **DMAPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

### DMA Peripheral Identification 3 (DMAPeriphID3)

Base 0x400F.F000

Offset 0xFEC

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID3	RO	0x00	$\mu$ DMA Peripheral ID Register [31:24] Can be used by software to identify the presence of this peripheral.

**Register 26: DMA Peripheral Identification 4 (DMAPeriphID4), offset 0xFD0**

The **DMAPeriphIDn** registers are hard-coded, and the fields within the registers determine the reset values.

**DMA Peripheral Identification 4 (DMAPeriphID4)**

Base 0x400F.F000

Offset 0xFD0

Type RO, reset 0x0000.0004

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID4							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID4	RO	0x04	$\mu$ DMA Peripheral ID Register Can be used by software to identify the presence of this peripheral.

### Register 27: DMA PrimeCell Identification 0 (DMAPCellID0), offset 0xFF0

The **DMAPCellIDn** registers are hard-coded, and the fields within the registers determine the reset values.

#### DMA PrimeCell Identification 0 (DMAPCellID0)

Base 0x400F.F000  
 Offset 0xFF0  
 Type RO, reset 0x0000.000D

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID0							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID0	RO	0x0D	$\mu$ DMA PrimeCell ID Register [7:0] Provides software a standard cross-peripheral identification system.

**Register 28: DMA PrimeCell Identification 1 (DMAPCellID1), offset 0xFF4**

The **DMAPCellIDn** registers are hard-coded, and the fields within the registers determine the reset values.

## DMA PrimeCell Identification 1 (DMAPCellID1)

Base 0x400F.F000

Offset 0xFF4

Type RO, reset 0x0000.00F0

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID1							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID1	RO	0xF0	$\mu$ DMA PrimeCell ID Register [15:8] Provides software a standard cross-peripheral identification system.

### Register 29: DMA PrimeCell Identification 2 (DMAPCellID2), offset 0xFF8

The **DMAPCellIDn** registers are hard-coded, and the fields within the registers determine the reset values.

#### DMA PrimeCell Identification 2 (DMAPCellID2)

Base 0x400F.F000  
 Offset 0xFF8  
 Type RO, reset 0x0000.0005



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID2	RO	0x05	$\mu$ DMA PrimeCell ID Register [23:16] Provides software a standard cross-peripheral identification system.

## Register 30: DMA PrimeCell Identification 3 (DMAPCellID3), offset 0xFFC

The **DMA PrimeCell IDn** registers are hard-coded, and the fields within the registers determine the reset values.

### DMA PrimeCell Identification 3 (DMAPCellID3)

Base 0x400F.F000

Offset 0xFFC

Type RO, reset 0x0000.00B1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID3	RO	0xB1	<p>μDMA PrimeCell ID Register [31:24]</p> <p>Provides software a standard cross-peripheral identification system.</p>

## 10 General-Purpose Input/Outputs (GPIOs)

The GPIO module is composed of nine physical GPIO blocks, each corresponding to an individual GPIO port (Port A, Port B, Port C, Port D, Port E, Port F, Port G, Port H, Port J). The GPIO module supports up to 67 programmable input/output pins, depending on the peripherals being used.

The GPIO module has the following features:

- Up to 67 GPIOs, depending on configuration
- Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
- 5-V-tolerant input/outputs
- Fast toggle capable of a change every two clock cycles
- Two means of port access: either Advanced High-Performance Bus (AHB) with better back-to-back access performance, or the legacy Advanced Peripheral Bus (APB) for backwards-compatibility with existing code
- Programmable control for GPIO interrupts
  - Interrupt generation masking
  - Edge-triggered on rising, falling, or both
  - Level-sensitive on High or Low values
- Bit masking in both read and write operations through address lines
- Can be used to initiate an ADC sample sequence
- Pins configured as digital inputs are Schmitt-triggered
- Programmable control for GPIO pad configuration
  - Weak pull-up or pull-down resistors
  - 2-mA, 4-mA, and 8-mA pad drive for digital communication; up to four pads can be configured with an 18-mA pad drive for high-current applications
  - Slew rate control for the 8-mA drive
  - Open drain enables
  - Digital input enables

### 10.1 Signal Description

GPIO signals have alternate hardware functions. Table 10-2 on page 289 lists the GPIO pins and their analog and digital alternate functions. The  $A_{INx}$  analog signals are not 5-V tolerant and go through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding  $DEN$  bit in the **GPIO Digital Enable (GPIODEN)** register and setting the corresponding  $AMSEL$  bit in the **GPIO Analog Mode Select (GPIOAMSEL)** register. Other analog signals are 5-V tolerant and are connected directly to their circuitry ( $C0-$ ,  $C0+$ ,  $C1-$ ,  $C1+$ ). These



signals are configured by clearing the DEN bit in the **GPIO Digital Enable (GPIODEN)** register. The digital alternate hardware functions are enabled by setting the appropriate bit in the **GPIO Alternate Function Select (GPIOAFSEL)** and **GPIODEN** registers and configuring the PMC<sub>x</sub> bit field in the **GPIO Port Control (GPIOPCTL)** register to the numeric encoding shown in the table below. Table entries that are shaded gray are the default values for the corresponding GPIO pin.

**Important:** All GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL=0**, **GPIODEN=0**, **GPIOPDR=0**, **GPIOPUR=0**, and **GPIOPCTL=0**) with the exception of the pins shown in the table below. A Power-On-Reset ( $\overline{\text{POR}}$ ) or asserting  $\overline{\text{RST}}$  puts the pins back to their default state.

**Table 10-1. GPIO Pins With Non-Zero Reset Values**

GPIO Pins	Default State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOPCTL
PA[1:0]	UART0	1	1	0	0	0x1
PA[5:2]	SSI0	1	1	0	0	0x1
PB[3:2]	I <sup>2</sup> C0	1	1	0	0	0x1
PC[3:0]	JTAG/SWD	1	1	0	1	0x3

**Table 10-2. GPIO Pins and Alternate Functions**

IO	Pin	Analog Function	Digital Function (GPIOPCTL PMC <sub>x</sub> Bit Field Encoding) <sup>a</sup>											
			1	2	3	4	5	6	7	8	9	10	11	
PA0	26	-	U0Rx	-	-	-	-	-	-	-	I2C1SCL	U1Rx	-	-
PA1	27	-	U0Tx	-	-	-	-	-	-	-	I2C1SDA	U1Tx	-	-
PA2	28	-	SSI0Clk	-	-	-	-	-	-	-	-	-	-	-
PA3	29	-	SSI0Fss	-	-	-	-	-	-	-	-	-	-	-
PA4	30	-	SSI0Rx	-	-	-	-	-	-	-	-	-	-	-
PA5	31	-	SSI0Tx	-	-	-	-	-	-	-	-	-	-	-
PA6	34	-	I2C1SCL	CCP1	-	-	-	-	-	-	-	U1CTS	-	-
PA7	35	-	I2C1SDA	CCP4	-	-	-	-	CCP3	-	-	U1DCD	-	-
PB0	66	-	CCP0	-	-	-	U1Rx	-	-	-	-	-	-	-
PB1	67	-	CCP2	-	-	CCP1	U1Tx	-	-	-	-	-	-	-
PB2	72	-	I2C0SCL	-	-	CCP3	CCP0	-	-	-	-	-	-	-
PB3	65	-	I2C0SDA	-	-	-	-	-	-	-	-	-	-	-
PB4	92	C0-	-	-	-	U2Rx	-	-	U1Rx	EPI0S23	-	-	-	-
PB5	91	C1-	C0o	CCP5	CCP6	CCP0	-	CCP2	U1Tx	EPI0S22	-	-	-	-
PB6	90	VREFA C0+	CCP1	CCP7	C0o	-	-	CCP5	-	-	-	-	-	-
PB7	89	-	-	-	-	NMI	-	-	-	-	-	-	-	-
PC0	80	-	-	-	TCK SWCLK	-	-	-	-	-	-	-	-	-
PC1	79	-	-	-	TMS SWDIO	-	-	-	-	-	-	-	-	-
PC2	78	-	-	-	TDI	-	-	-	-	-	-	-	-	-
PC3	77	-	-	-	TDO SWO	-	-	-	-	-	-	-	-	-
PC4	25	-	CCP5	-	-	-	CCP2	CCP4	-	EPI0S2	CCP1	-	-	-

Table 10-2. GPIO Pins and Alternate Functions (continued)

IO	Pin	Analog Function	Digital Function (GPIOCTL PMCx Bit Field Encoding) <sup>a</sup>										
			1	2	3	4	5	6	7	8	9	10	11
PC5	24	C1+	CCP1	C1o	C0o	-	CCP3	-	-	EPIOS3	-	-	-
PC6	23	-	CCP3	-	-	-	U1Rx	CCP0	-	EPIOS4	-	-	-
PC7	22	-	CCP4	-	-	CCP0	U1Tx	-	C1o	EPIOS5	-	-	-
PD0	10	-	-	-	-	U2Rx	U1Rx	CCP6	-	-	U1CTS	-	-
PD1	11	-	-	-	-	U2Tx	U1Tx	CCP7	-	-	U1DCD	CCP2	-
PD2	12	-	U1Rx	CCP6	-	CCP5	-	-	-	EPIOS20	-	-	-
PD3	13	-	U1Tx	CCP7	-	CCP0	-	-	-	EPIOS21	-	-	-
PD4	97	AIN7	CCP0	CCP3	-	-	-	-	-	-	U1RI	EPIOS19	-
PD5	98	AIN6	CCP2	CCP4	-	-	-	-	-	-	U2Rx	EPIOS28	-
PD6	99	AIN5	-	-	-	-	-	-	-	-	U2Tx	EPIOS29	-
PD7	100	AIN4	-	C0o	CCP1	-	-	-	-	-	U1DTR	EPIOS30	-
PE0	74	-	-	SSI1Clk	CCP3	-	-	-	-	EPIOS8	-	-	-
PE1	75	-	-	SSI1Fss	-	CCP2	CCP6	-	-	EPIOS9	-	-	-
PE2	95	-	CCP4	SSI1Rx	-	-	CCP2	-	-	EPIOS24	-	-	-
PE3	96	-	CCP1	SSI1Tx	-	-	CCP7	-	-	EPIOS25	-	-	-
PE4	6	AIN3	CCP3	-	-	-	U2Tx	CCP2	-	-	-	-	-
PE5	5	AIN2	CCP5	-	-	-	-	-	-	-	-	-	-
PE6	2	AIN1	-	C1o	-	-	-	-	-	-	U1CTS	-	-
PE7	1	AIN0	-	-	-	-	-	-	-	-	U1DCD	-	-
PF0	47	-	-	-	-	-	-	-	-	-	U1DSR	-	-
PF1	61	-	-	-	-	-	-	-	-	-	U1RTS	CCP3	-
PF2	60	-	-	-	-	-	-	-	-	-	SSI1Clk	-	-
PF3	59	-	-	-	-	-	-	-	-	-	SSI1Fss	-	-
PF4	58	-	CCP0	C0o	-	-	-	-	-	EPIOS12	SSI1Rx	-	-
PF5	46	-	CCP2	C1o	-	-	-	-	-	EPIOS15	SSI1Tx	-	-
PF6	43	-	CCP1	-	-	-	-	-	-	-	-	U1RTS	-
PF7	42	-	CCP4	-	-	-	-	-	-	EPIOS12	-	-	-
PG0	19	-	U2Rx	-	I2C1SCL	-	-	-	-	EPIOS13	-	-	-
PG1	18	-	U2Tx	-	I2C1SDA	-	-	-	-	EPIOS14	-	-	-
PG2	17	-	-	-	-	-	-	-	-	-	-	-	-
PG3	16	-	-	-	-	-	-	-	-	-	-	-	-
PG4	41	-	CCP3	-	-	-	-	-	-	EPIOS15	-	U1RI	-
PG5	40	-	CCP5	-	-	-	-	-	-	-	-	U1DTR	-
PG6	37	-	-	-	-	-	-	-	-	-	-	U1RI	-
PG7	36	-	-	-	-	-	-	-	-	CCP5	EPIOS31	-	-
PH0	86	-	CCP6	-	-	-	-	-	-	EPIOS6	-	-	-
PH1	85	-	CCP7	-	-	-	-	-	-	EPIOS7	-	-	-
PH2	84	-	-	C1o	-	-	-	-	-	EPIOS1	-	-	-
PH3	83	-	-	-	-	-	-	-	-	EPIOS0	-	-	-
PH4	76	-	-	-	-	-	-	-	-	EPIOS10	-	-	SSI1Clk

Table 10-2. GPIO Pins and Alternate Functions (continued)

IO	Pin	Analog Function	Digital Function (GPIOCTL PMCx Bit Field Encoding) <sup>a</sup>											
			1	2	3	4	5	6	7	8	9	10	11	
PH5	63	-	-	-	-	-	-	-	-	-	EPI0S11	-	-	SSI1Fss
PH6	62	-	-	-	-	-	-	-	-	-	EPI0S26	-	-	SSI1Rx
PH7	15	-	-	-	-	-	-	-	-	-	EPI0S27	-	-	SSI1Tx
PJ0	14	-	-	-	-	-	-	-	-	-	EPI0S16	-	-	I2C1SCL
PJ1	87	-	-	-	-	-	-	-	-	-	EPI0S17	-	-	I2C1SDA
PJ2	39	-	-	-	-	-	-	-	-	-	EPI0S18	CCP0	-	-

a. The digital signals that are shaded gray are the power-on default values for the corresponding GPIO pin.

## 10.2 Functional Description

Each GPIO port is a separate hardware instantiation of the same physical block (see Figure 10-1 on page 291 and Figure 10-2 on page 292). The LM3S1811 microcontroller contains nine ports and thus nine of these physical GPIO blocks. Note that not all pins may be implemented on every block. Some GPIO pins can function as I/O signals for the on-chip peripheral modules. For information on which GPIO pins are used for alternate hardware functions, refer to Table 20-5 on page 722.

Figure 10-1. Digital I/O Pads

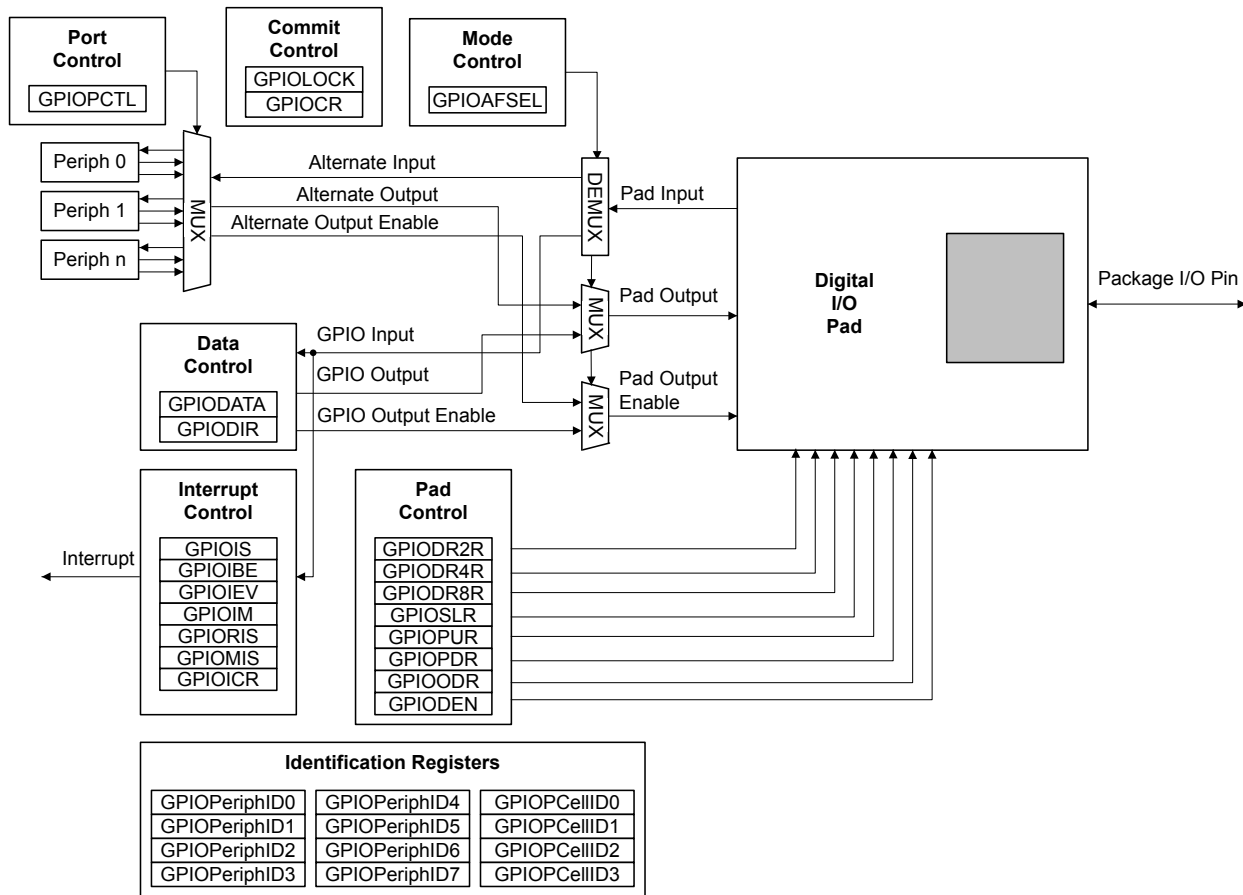
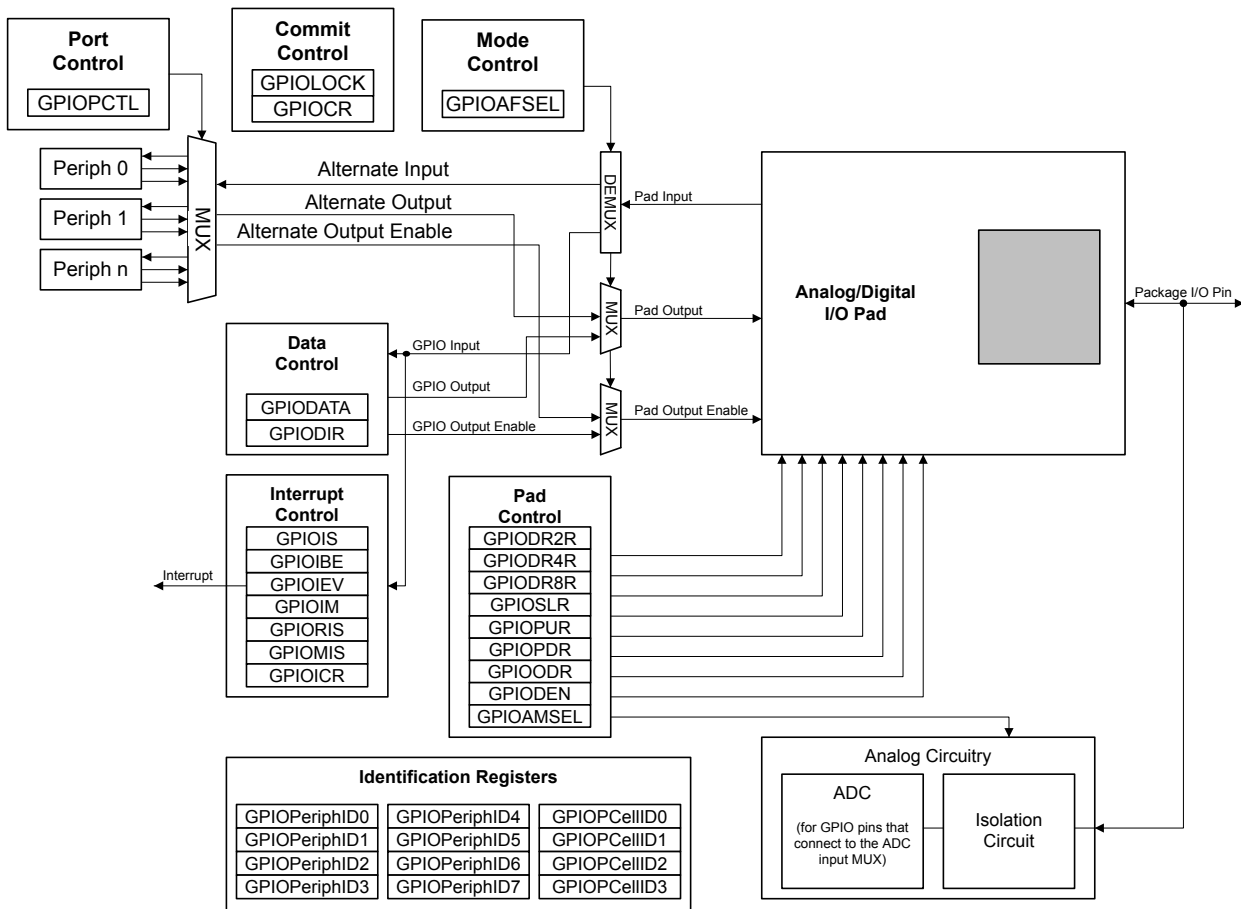


Figure 10-2. Analog/Digital I/O Pads



### 10.2.1 Data Control

The data control registers allow software to configure the operational modes of the GPIOs. The data direction register configures the GPIO as an input or an output while the data register either captures incoming data or drives it out to the pads.

**Caution – It is possible to create a software sequence that prevents the debugger from connecting to the Stellaris® microcontroller. If the program code loaded into flash immediately changes the JTAG pins to their GPIO functionality, the debugger may not have enough time to connect and halt the controller before the JTAG pin functionality switches. As a result, the debugger may be locked out of the part. This issue can be avoided with a software routine that restores JTAG functionality based on an external or software trigger.**

#### 10.2.1.1 Data Direction Operation

The **GPIO Direction (GPIODIR)** register (see page 301) is used to configure each individual pin as an input or output. When the data direction bit is cleared, the GPIO is configured as an input, and the corresponding data register bit captures and stores the value on the GPIO port. When the data direction bit is set, the GPIO is configured as an output, and the corresponding data register bit is driven out on the GPIO port.

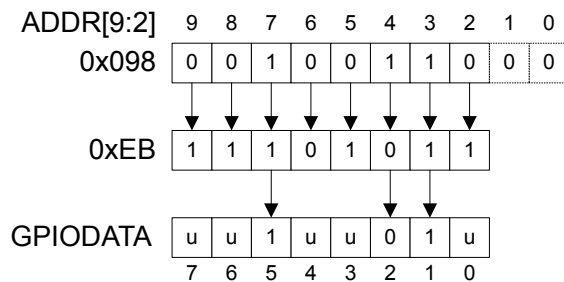
### 10.2.1.2 Data Register Operation

To aid in the efficiency of software, the GPIO ports allow for the modification of individual bits in the **GPIO Data (GPIODATA)** register (see page 300) by using bits [9:2] of the address bus as a mask. In this manner, software drivers can modify individual GPIO pins in a single instruction without affecting the state of the other pins. This method is more efficient than the conventional method of performing a read-modify-write operation to set or clear an individual GPIO pin. To implement this feature, the **GPIODATA** register covers 256 locations in the memory map.

During a write, if the address bit associated with that data bit is set, the value of the **GPIODATA** register is altered. If the address bit is cleared, the data bit is left unchanged.

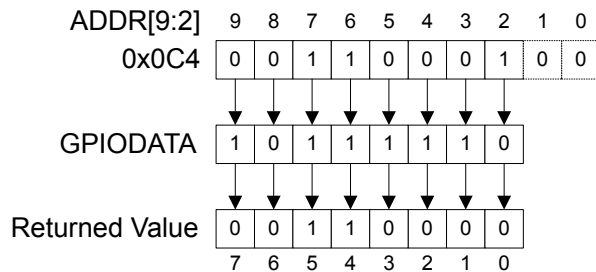
For example, writing a value of 0xEB to the address GPIODATA + 0x098 has the results shown in Figure 10-3, where u indicates that data is unchanged by the write.

**Figure 10-3. GPIODATA Write Example**



During a read, if the address bit associated with the data bit is set, the value is read. If the address bit associated with the data bit is cleared, the data bit is read as a zero, regardless of its actual value. For example, reading address GPIODATA + 0x0C4 yields as shown in Figure 10-4.

**Figure 10-4. GPIODATA Read Example**



## 10.2.2 Interrupt Control

The interrupt capabilities of each GPIO port are controlled by a set of seven registers. These registers are used to select the source of the interrupt, its polarity, and the edge properties. When one or more GPIO inputs cause an interrupt, a single interrupt output is sent to the interrupt controller for the entire GPIO port. For edge-triggered interrupts, software must clear the interrupt to enable any further interrupts. For a level-sensitive interrupt, the external source must hold the level constant for the interrupt to be recognized by the controller.

Three registers define the edge or sense that causes interrupts:

- **GPIO Interrupt Sense (GPIOIS)** register (see page 302)

- **GPIO Interrupt Both Edges (GPIOIBE)** register (see page 303)
- **GPIO Interrupt Event (GPIOIEV)** register (see page 304)

Interrupts are enabled/disabled via the **GPIO Interrupt Mask (GPIOIM)** register (see page 305).

When an interrupt condition occurs, the state of the interrupt signal can be viewed in two locations: the **GPIO Raw Interrupt Status (GPIORIS)** and **GPIO Masked Interrupt Status (GPIOMIS)** registers (see page 306 and page 307). As the name implies, the **GPIOMIS** register only shows interrupt conditions that are allowed to be passed to the interrupt controller. The **GPIORIS** register indicates that a GPIO pin meets the conditions for an interrupt, but has not necessarily been sent to the interrupt controller.

In addition to providing GPIO functionality,  $PB4$  can also be used as an external trigger for the ADC. If  $PB4$  is configured as a non-masked interrupt pin (the appropriate bit of **GPIOIM** is set), an interrupt for Port B is generated, and an external trigger signal is sent to the ADC. If the **ADC Event Multiplexer Select (ADCEMUX)** register is configured to use the external trigger, an ADC conversion is initiated. See page 505.

If no other Port B pins are being used to generate interrupts, the ARM Integrated Nested Vectored Interrupt Controller (NVIC) Interrupt Set Enable (SETENA) register can disable the Port B interrupts, and the ADC interrupt can be used to read back the converted data. Otherwise, the Port B interrupt handler must ignore and clear interrupts on  $PB4$  and wait for the ADC interrupt, or the ADC interrupt must be disabled in the SETENA register and the Port B interrupt handler must poll the ADC registers until the conversion is completed. See the *ARM® Cortex™-M3 Technical Reference Manual* for more information.

Interrupts are cleared by writing a 1 to the appropriate bit of the **GPIO Interrupt Clear (GPIOICR)** register (see page 309).

When programming the interrupt control registers (**GPIOIS**, **GPIOIBE**, or **GPIOIEV**), the interrupts should be masked (**GPIOIM** cleared). Writing any value to an interrupt control register can generate a spurious interrupt if the corresponding bits are enabled.

### 10.2.3 Mode Control

The GPIO pins can be controlled by either software or hardware. Software control is the default for most signals and corresponds to the GPIO mode, where the **GPIO DATA** register is used to read or write the corresponding pins. When hardware control is enabled via the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 310), the pin state is controlled by its alternate function (that is, the peripheral).

Further pin muxing options are provided through the **GPIO Port Control (GPIOCTL)** register which selects one of several peripheral functions for each GPIO. For information on the configuration options, refer to Table 20-5 on page 722.

**Note:** If any pin is to be used as an ADC input, the appropriate bit in the **GPIOAMSEL** register must be set to disable the analog isolation circuit.

### 10.2.4 Commit Control

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is currently provided for the **NMI** pin ( $PB7$ ) and the four **JTAG/SWD** pins ( $PC[3:0]$ ). Writes to protected bits of the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 310), **GPIO Pull Up Select (GPIOPUR)** register (see page 316), **GPIO Pull-Down Select (GPIOPDR)** register (see page 318), and **GPIO Digital Enable (GPIODEN)** register (see page 321) are not committed to storage unless the **GPIO Lock (GPIOLOCK)** register

(see page 323) has been unlocked and the appropriate bits of the **GPIO Commit (GPIOCR)** register (see page 324) have been set.

### 10.2.5 Pad Control

The pad control registers allow software to configure the GPIO pads based on the application requirements. The pad control registers include the **GPIO DR2R**, **GPIO DR4R**, **GPIO DR8R**, **GPIO ODR**, **GPIO PUR**, **GPIO PDR**, **GPIO SLR**, and **GPIO DEN** registers. These registers control drive strength, open-drain configuration, pull-up and pull-down resistors, slew-rate control and digital input enable for each GPIO.

For special high-current applications, the GPIO output buffers may be used with the following restrictions. With the GPIO pins configured as 8-mA output drivers, a total of four GPIO outputs may be used to sink current loads up to 18 mA each. At 18-mA sink current loading, the  $V_{OL}$  value is specified as 1.2 V. The high-current GPIO package pins must be selected such that there are only a maximum of two per side of the physical package with the total number of high-current GPIO outputs not exceeding four for the entire package.

### 10.2.6 Identification

The identification registers configured at reset allow software to detect and identify the module as a GPIO block. The identification registers include the **GPIO PeriphID0-GPIO PeriphID7** registers as well as the **GPIO CellID0-GPIO CellID3** registers.

## 10.3 Initialization and Configuration

The GPIO modules may be accessed via two different memory apertures. The legacy aperture, the Advanced Peripheral Bus (APB), is backwards-compatible with previous Stellaris® parts. The other aperture, the Advanced High-Performance Bus (AHB), offers the same register map but provides better back-to-back access performance than the APB bus. These apertures are mutually exclusive. The aperture enabled for a given GPIO port is controlled by the appropriate bit in the **GPIOHBCTL** register (see page 112).

To use the pins in a particular GPIO port, the clock for the port must be enabled by setting the appropriate GPIO Port bit field ( $GPIO_n$ ) in the **RCGC2** register (see page 158).

On reset, all GPIO pins are configured out of reset to be undriven (tristate): **GPIOAFSEL=0**, **GPIO DEN=0**, **GPIO PDR=0**, and **GPIO PUR=0**, except for the pins shown in Table 10-1 on page 289. Table 10-3 on page 295 shows all possible configurations of the GPIO pads and the control register settings required to achieve them. Table 10-4 on page 296 shows how a rising edge interrupt is configured for pin 2 of a GPIO port.

**Table 10-3. GPIO Pad Configuration Examples**

Configuration	GPIO Register Bit Value <sup>a</sup>									
	AFSEL	DIR	ODR	DEN	PUR	PDR	DR2R	DR4R	DR8R	SLR
Digital Input (GPIO)	0	0	0	1	?	?	X	X	X	X
Digital Output (GPIO)	0	1	0	1	?	?	?	?	?	?
Open Drain Output (GPIO)	0	1	1	1	X	X	?	?	?	?
Open Drain Input/Output (I <sup>2</sup> C)	1	X	1	1	X	X	?	?	?	?
Digital Input (Timer CCP)	1	X	0	1	?	?	X	X	X	X

Table 10-3. GPIO Pad Configuration Examples (continued)

Configuration	GPIO Register Bit Value <sup>a</sup>									
	AFSEL	DIR	ODR	DEN	PUR	PDR	DR2R	DR4R	DR8R	SLR
Digital Output (Timer PWM)	1	X	0	1	?	?	?	?	?	?
Digital Input/Output (SSI)	1	X	0	1	?	?	?	?	?	?
Digital Input/Output (UART)	1	X	0	1	?	?	?	?	?	?
Analog Input (Comparator)	0	0	0	0	0	0	X	X	X	X
Digital Output (Comparator)	1	X	0	1	?	?	?	?	?	?

a. X=Ignored (don't care bit)

?=Can be either 0 or 1, depending on the configuration

Table 10-4. GPIO Interrupt Configuration Example

Register	Desired Interrupt Event Trigger	Pin 2 Bit Value <sup>a</sup>							
		7	6	5	4	3	2	1	0
GPIOIS	0=edge 1=level	X	X	X	X	X	0	X	X
GPIOIBE	0=single edge 1=both edges	X	X	X	X	X	0	X	X
GPIOIEV	0=Low level, or falling edge 1=High level, or rising edge	X	X	X	X	X	1	X	X
GPIOIM	0=masked 1=not masked	0	0	0	0	0	1	0	0

a. X=Ignored (don't care bit)

## 10.4 Register Map

Table 10-6 on page 298 lists the GPIO registers. Each GPIO port can be accessed through one of two bus apertures. The legacy aperture, the Advanced Peripheral Bus (APB), is backwards-compatible with previous Stellaris<sup>®</sup> parts. The other aperture, the Advanced High-Performance Bus (AHB), offers the same register map but provides better back-to-back access performance than the APB bus.

**Important:** The GPIO registers in this chapter are duplicated in each GPIO block; however, depending on the block, all eight bits may not be connected to a GPIO pad. In those cases, writing to unconnected bits has no effect, and reading unconnected bits returns no meaningful data.



The offset listed is a hexadecimal increment to the register's address, relative to that GPIO port's base address:

- GPIO Port A (APB): 0x4000.4000
- GPIO Port A (AHB): 0x4005.8000
- GPIO Port B (APB): 0x4000.5000
- GPIO Port B (AHB): 0x4005.9000
- GPIO Port C (APB): 0x4000.6000
- GPIO Port C (AHB): 0x4005.A000
- GPIO Port D (APB): 0x4000.7000
- GPIO Port D (AHB): 0x4005.B000
- GPIO Port E (APB): 0x4002.4000
- GPIO Port E (AHB): 0x4005.C000
- GPIO Port F (APB): 0x4002.5000
- GPIO Port F (AHB): 0x4005.D000
- GPIO Port G (APB): 0x4002.6000
- GPIO Port G (AHB): 0x4005.E000
- GPIO Port H (APB): 0x4002.7000
- GPIO Port H (AHB): 0x4005.F000
- GPIO Port J (APB): 0x4003.D000
- GPIO Port J (AHB): 0x4006.0000

Note that each GPIO module clock must be enabled before the registers can be programmed (see page 158).

**Important:** All GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL=0**, **GPIODEN=0**, **GPIOPDR=0**, **GPIOPUR=0**, and **GPIOCTL=0**) with the exception of the pins shown in the table below. A Power-On-Reset ( $\overline{POR}$ ) or asserting  $\overline{RST}$  puts the pins back to their default state.

**Table 10-5. GPIO Pins With Non-Zero Reset Values**

GPIO Pins	Default State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOCTL
PA[1:0]	UART0	1	1	0	0	0x1
PA[5:2]	SSI0	1	1	0	0	0x1
PB[3:2]	I <sup>2</sup> C0	1	1	0	0	0x1
PC[3:0]	JTAG/SWD	1	1	0	1	0x3

**Note:** The default register type for the **GPIOCR** register is RO for all GPIO pins with the exception of the **NMI** pin and the four JTAG/SWD pins (**PB7** and **PC[3:0]**). These five pins are currently the only GPIOs that are protected by the **GPIOCR** register. Because of this, the register type for GPIO Port B7 and GPIO Port C[3:0] is R/W.

The default reset value for the **GPIOCR** register is 0x0000.00FF for all GPIO pins, with the exception of the **NMI** pin and the four JTAG/SWD pins (**PB7** and **PC[3:0]**). To ensure that the JTAG port is not accidentally programmed as a GPIO, these four pins default to non-committable. To ensure that the **NMI** pin is not accidentally programmed as the non-maskable interrupt pin, it defaults to non-committable. Because of this, the default reset value of **GPIOCR** for GPIO Port B is 0x0000.007F while the default reset value of **GPIOCR** for Port C is 0x0000.00F0.

**Table 10-6. GPIO Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	GPIODATA	R/W	0x0000.0000	GPIO Data	300
0x400	GPIODIR	R/W	0x0000.0000	GPIO Direction	301
0x404	GPIOIS	R/W	0x0000.0000	GPIO Interrupt Sense	302
0x408	GPIOIBE	R/W	0x0000.0000	GPIO Interrupt Both Edges	303
0x40C	GPIOIEV	R/W	0x0000.0000	GPIO Interrupt Event	304
0x410	GPIOIM	R/W	0x0000.0000	GPIO Interrupt Mask	305
0x414	GPIORIS	RO	0x0000.0000	GPIO Raw Interrupt Status	306
0x418	GIOMIS	RO	0x0000.0000	GPIO Masked Interrupt Status	307
0x41C	GPIOICR	W1C	0x0000.0000	GPIO Interrupt Clear	309
0x420	GPIOAFSEL	R/W	-	GPIO Alternate Function Select	310
0x500	GPIODR2R	R/W	0x0000.00FF	GPIO 2-mA Drive Select	312
0x504	GPIODR4R	R/W	0x0000.0000	GPIO 4-mA Drive Select	313
0x508	GPIODR8R	R/W	0x0000.0000	GPIO 8-mA Drive Select	314
0x50C	GPIOODR	R/W	0x0000.0000	GPIO Open Drain Select	315
0x510	GIOPUR	R/W	-	GPIO Pull-Up Select	316
0x514	GIOPDR	R/W	0x0000.0000	GPIO Pull-Down Select	318
0x518	GPIOSLR	R/W	0x0000.0000	GPIO Slew Rate Control Select	320
0x51C	GPIODEN	R/W	-	GPIO Digital Enable	321
0x520	GPIOLOCK	R/W	0x0000.0001	GPIO Lock	323
0x524	GPIOCR	-	-	GPIO Commit	324
0x528	GPIOAMSEL	R/W	0x0000.0000	GPIO Analog Mode Select	326
0x52C	GIOPCTL	R/W	-	GPIO Port Control	328
0xFD0	GPIOPeriphID4	RO	0x0000.0000	GPIO Peripheral Identification 4	330
0xFD4	GPIOPeriphID5	RO	0x0000.0000	GPIO Peripheral Identification 5	331
0xFD8	GPIOPeriphID6	RO	0x0000.0000	GPIO Peripheral Identification 6	332
0xFDC	GPIOPeriphID7	RO	0x0000.0000	GPIO Peripheral Identification 7	333
0xFE0	GPIOPeriphID0	RO	0x0000.0061	GPIO Peripheral Identification 0	334
0xFE4	GPIOPeriphID1	RO	0x0000.0000	GPIO Peripheral Identification 1	335
0xFE8	GPIOPeriphID2	RO	0x0000.0018	GPIO Peripheral Identification 2	336
0xFEC	GPIOPeriphID3	RO	0x0000.0001	GPIO Peripheral Identification 3	337
0xFF0	GPIOPCellID0	RO	0x0000.000D	GPIO PrimeCell Identification 0	338
0xFF4	GPIOPCellID1	RO	0x0000.00F0	GPIO PrimeCell Identification 1	339

**Table 10-6. GPIO Register Map (continued)**

Offset	Name	Type	Reset	Description	See page
0xFF8	GPIOCellID2	RO	0x0000.0005	GPIO PrimeCell Identification 2	340
0xFFC	GPIOCellID3	RO	0x0000.00B1	GPIO PrimeCell Identification 3	341

## 10.5 Register Descriptions

The remainder of this section lists and describes the GPIO registers, in numerical order by address offset.

### Register 1: GPIO Data (GPIODATA), offset 0x000

The **GPIODATA** register is the data register. In software control mode, values written in the **GPIODATA** register are transferred onto the GPIO port pins if the respective pins have been configured as outputs through the **GPIO Direction (GPIODIR)** register (see page 301).

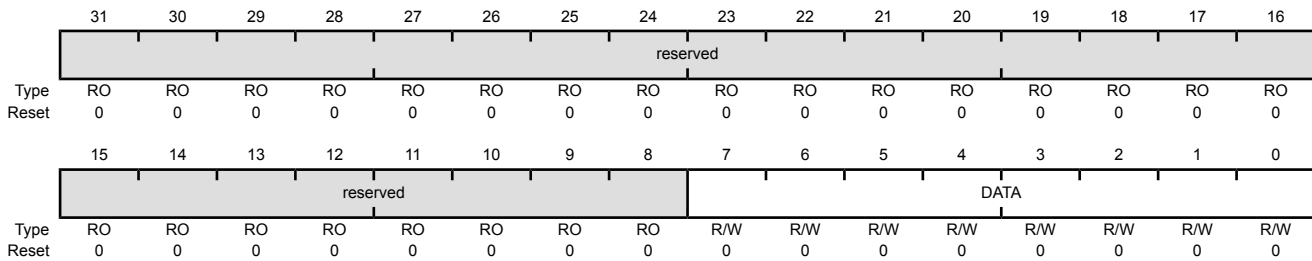
In order to write to **GPIODATA**, the corresponding bits in the mask, resulting from the address bus bits [9:2], must be set. Otherwise, the bit values remain unchanged by the write.

Similarly, the values read from this register are determined for each bit by the mask bit derived from the address used to access the data register, bits [9:2]. Bits that are set in the address mask cause the corresponding bits in **GPIODATA** to be read, and bits that are clear in the address mask cause the corresponding bits in **GPIODATA** to be read as 0, regardless of their value.

A read from **GPIODATA** returns the last bit value written if the respective pins are configured as outputs, or it returns the value on the corresponding input pin when these are configured as inputs. All bits are cleared by a reset.

#### GPIO Data (GPIODATA)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x000  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DATA	R/W	0x00	GPIO Data

This register is virtually mapped to 256 locations in the address space. To facilitate the reading and writing of data to these registers by independent drivers, the data read from and written to the registers are masked by the eight address lines [9:2]. Reads from this register return its current state. Writes to this register only affect bits that are not masked by ADDR[9:2] and are configured as outputs. See “Data Register Operation” on page 293 for examples of reads and writes.

## Register 2: GPIO Direction (GPIODIR), offset 0x400

The **GPIODIR** register is the data direction register. Setting a bit in the **GPIODIR** register configures the corresponding pin to be an output, while clearing a bit configures the corresponding pin to be an input. All bits are cleared by a reset, meaning all GPIO pins are inputs by default.

### GPIO Direction (GPIODIR)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x400  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DIR							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

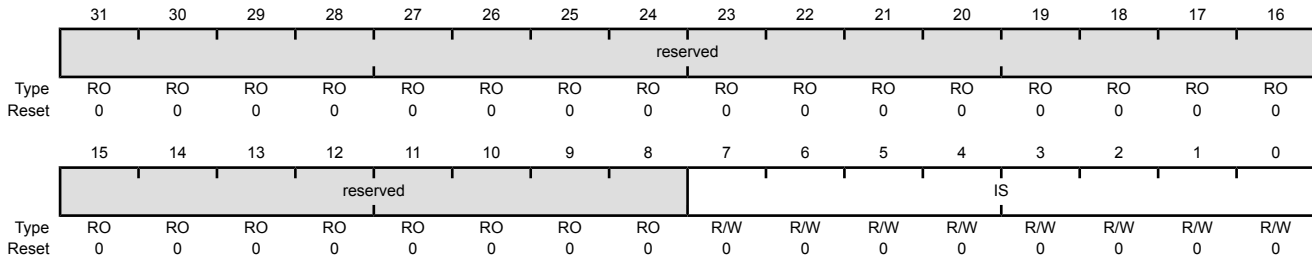
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DIR	R/W	0x00	GPIO Data Direction
				Value Description
				0 Corresponding pin is an input.
				1 Corresponding pins is an output.

### Register 3: GPIO Interrupt Sense (GPIOIS), offset 0x404

The **GPIOIS** register is the interrupt sense register. Setting a bit in the **GPIOIS** register configures the corresponding pin to detect levels, while clearing a bit configures the corresponding pin to detect edges. All bits are cleared by a reset.

#### GPIO Interrupt Sense (GPIOIS)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x404  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description	
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.	
7:0	IS	R/W	0x00	GPIO Interrupt Sense	
Value Description					
	0	The edge on the corresponding pin is detected (edge-sensitive).			
	1	The level on the corresponding pin is detected (level-sensitive).			

## Register 4: GPIO Interrupt Both Edges (GPIOIBE), offset 0x408

The **GPIOIBE** register allows both edges to cause interrupts. When the corresponding bit in the **GPIO Interrupt Sense (GPIOIS)** register (see page 302) is set to detect edges, setting a bit in the **GPIOIBE** register configures the corresponding pin to detect both rising and falling edges, regardless of the corresponding bit in the **GPIO Interrupt Event (GPIOIEV)** register (see page 304). Clearing a bit configures the pin to be controlled by the **GPIOIEV** register. All bits are cleared by a reset.

### GPIO Interrupt Both Edges (GPIOIBE)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x408

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								IBE							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

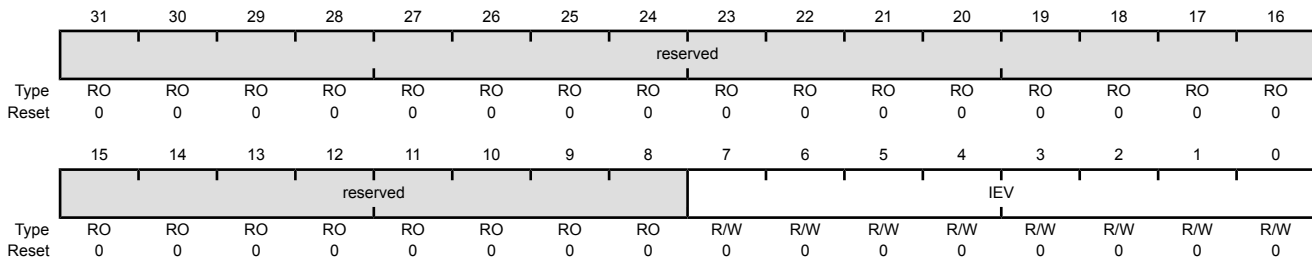
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	IBE	R/W	0x00	GPIO Interrupt Both Edges
				Value Description
				0 Interrupt generation is controlled by the <b>GPIO Interrupt Event (GPIOIEV)</b> register (see page 304).
				1 Both edges on the corresponding pin trigger an interrupt.

### Register 5: GPIO Interrupt Event (GPIOIEV), offset 0x40C

The **GPIOIEV** register is the interrupt event register. Setting a bit in the **GPIOIEV** register configures the corresponding pin to detect rising edges or high levels, depending on the corresponding bit value in the **GPIO Interrupt Sense (GPIOIS)** register (see page 302). Clearing a bit configures the pin to detect falling edges or low levels, depending on the corresponding bit value in the **GPIOIS** register. All bits are cleared by a reset.

#### GPIO Interrupt Event (GPIOIEV)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x40C  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	IEV	R/W	0x00	GPIO Interrupt Event
				Value Description
				0 A falling edge or a Low level on the corresponding pin triggers an interrupt.
				1 A rising edge or a High level on the corresponding pin triggers an interrupt.



## Register 6: GPIO Interrupt Mask (GPIOIM), offset 0x410

The **GPIOIM** register is the interrupt mask register. Setting a bit in the **GPIOIM** register allows interrupts that are generated by the corresponding pin to be sent to the interrupt controller on the combined interrupt signal. Clearing a bit prevents an interrupt on the corresponding pin from being sent to the interrupt controller. All bits are cleared by a reset.

### GPIO Interrupt Mask (GPIOIM)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x410  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								IME							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	IME	R/W	0x00	GPIO Interrupt Mask Enable

#### Value Description

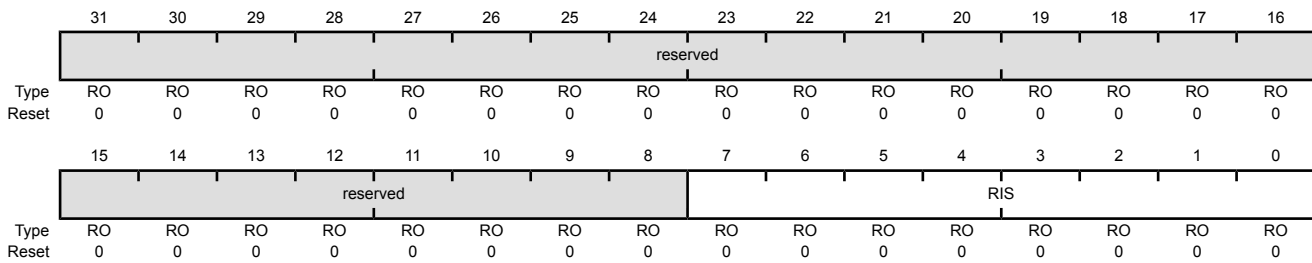
Value	Description
0	The interrupt from the corresponding pin is masked.
1	The interrupt from the corresponding pin is sent to the interrupt controller.

### Register 7: GPIO Raw Interrupt Status (GPIORIS), offset 0x414

The **GPIORIS** register is the raw interrupt status register. A bit in this register is set when an interrupt condition occurs on the corresponding GPIO pin. If the corresponding bit in the **GPIO Interrupt Mask (GPIOIM)** register (see page 305) is set, the interrupt is sent to the interrupt controller. Bits read as zero indicate that corresponding input pins have not initiated an interrupt. A bit in this register can be cleared by writing a 1 to the corresponding bit in the **GPIO Interrupt Clear (GPIOICR)** register.

#### GPIO Raw Interrupt Status (GPIORIS)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x414  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	RIS	RO	0x00	GPIO Interrupt Raw Status
				Value Description
				1 An interrupt condition has occurred on the corresponding pin.
				0 An interrupt condition has not occurred on the corresponding pin.
				A bit is cleared by writing a 1 to the corresponding bit in the <b>GPIOICR</b> register.

## Register 8: GPIO Masked Interrupt Status (GPIOMIS), offset 0x418

The **GPIOMIS** register is the masked interrupt status register. If a bit is set in this register, the corresponding interrupt has triggered an interrupt to the interrupt controller. If a bit is clear, either no interrupt has been generated, or the interrupt is masked.

In addition to providing GPIO functionality, **PB4** can also be used as an external trigger for the ADC. If **PB4** is configured as a non-masked interrupt pin (the appropriate bit of **GPIOIM** is set), an interrupt for Port B is generated, and an external trigger signal is sent to the ADC. If the **ADC Event Multiplexer Select (ADCEMUX)** register is configured to use the external trigger, an ADC conversion is initiated. See page 505.

If no other Port B pins are being used to generate interrupts, the ARM Integrated Nested Vectored Interrupt Controller (NVIC) Interrupt Set Enable (SETNA) register can disable the Port B interrupts, and the ADC interrupt can be used to read back the converted data. Otherwise, the Port B interrupt handler must ignore and clear interrupts on PB4 and wait for the ADC interrupt, or the ADC interrupt must be disabled in the SETNA register and the Port B interrupt handler must poll the ADC registers until the conversion is completed. See the *ARM® Cortex™-M3 Technical Reference Manual* for more information.

**GPIOMIS** is the state of the interrupt after masking.

### GPIO Masked Interrupt Status (GPIOMIS)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x418  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								MIS							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
7:0	MIS	RO	0x00	GPIO Masked Interrupt Status
				Value Description
				1 An interrupt condition on the corresponding pin has triggered an interrupt to the interrupt controller.
				0 An interrupt condition on the corresponding pin is masked or has not occurred.
				A bit is cleared by writing a 1 to the corresponding bit in the <b>GPIOICR</b> register.

## Register 9: GPIO Interrupt Clear (GPIOICR), offset 0x41C

The **GPIOICR** register is the interrupt clear register. Writing a 1 to a bit in this register clears the corresponding interrupt bit in the **GPIOIRIS** and **GPIOMIS** registers. Writing a 0 has no effect.

### GPIO Interrupt Clear (GPIOICR)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x41C  
 Type W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								IC							
Type	RO	RO	RO	RO	RO	RO	RO	RO	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	IC	W1C	0x00	GPIO Interrupt Clear
				Value Description
				1 The corresponding interrupt is cleared.
				0 The corresponding interrupt is unaffected.

**Register 10: GPIO Alternate Function Select (GPIOAFSEL), offset 0x420**

The **GPIOAFSEL** register is the mode control select register. If a bit is clear, the pin is used as a GPIO and is controlled by the GPIO registers. Setting a bit in this register configures the corresponding GPIO line to be controlled by an associated peripheral. Several possible peripheral functions are multiplexed on each GPIO. The **GPIO Port Control (GPIOCTL)** register is used to select one of the possible functions. Table 20-5 on page 722 details which functions are muxed on each GPIO pin. The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in the table below.

**Important:** All GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL**=0, **GPIODEN**=0, **GPIOPDR**=0, **GPIOPUR**=0, and **GPIOCTL**=0) with the exception of the pins shown in the table below. A Power-On-Reset ( $\overline{POR}$ ) or asserting  $\overline{RST}$  puts the pins back to their default state.

**Table 10-7. GPIO Pins With Non-Zero Reset Values**

GPIO Pins	Default State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOCTL
PA[1:0]	UART0	1	1	0	0	0x1
PA[5:2]	SSI0	1	1	0	0	0x1
PB[3:2]	I <sup>2</sup> C0	1	1	0	0	0x1
PC[3:0]	JTAG/SWD	1	1	0	1	0x3

**Caution – It is possible to create a software sequence that prevents the debugger from connecting to the Stellaris<sup>®</sup> microcontroller. If the program code loaded into flash immediately changes the JTAG pins to their GPIO functionality, the debugger may not have enough time to connect and halt the controller before the JTAG pin functionality switches. As a result, the debugger may be locked out of the part. This issue can be avoided with a software routine that restores JTAG functionality based on an external or software trigger.**

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is currently provided for the  $\overline{NMI}$  pin ( $\overline{PB7}$ ) and the four JTAG/SWD pins ( $\overline{PC[3:0]}$ ). Writes to protected bits of the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 310), **GPIO Pull Up Select (GPIOPUR)** register (see page 316), **GPIO Pull-Down Select (GPIOPDR)** register (see page 318), and **GPIO Digital Enable (GPIODEN)** register (see page 321) are not committed to storage unless the **GPIO Lock (GPIOLOCK)** register (see page 323) has been unlocked and the appropriate bits of the **GPIO Commit (GPIOCR)** register (see page 324) have been set.

When using the I<sup>2</sup>C module, in addition to setting the **GPIOAFSEL** register bits for the I<sup>2</sup>C clock and data pins, the pins should be set to open drain using the **GPIO Open Drain Select (GPIOODR)** register (see examples in “Initialization and Configuration” on page 295).

GPIO Alternate Function Select (GPIOAFSEL)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000

Offset 0x420  
 Type R/W, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								AFSEL							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	AFSEL	R/W	-	GPIO Alternate Function Select

Value Description

- 0 The associated pin functions as a GPIO and is controlled by the GPIO registers.
- 1 The associated pin functions as a peripheral signal and is controlled by the alternate hardware function.

The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in Table 10-1 on page 289.

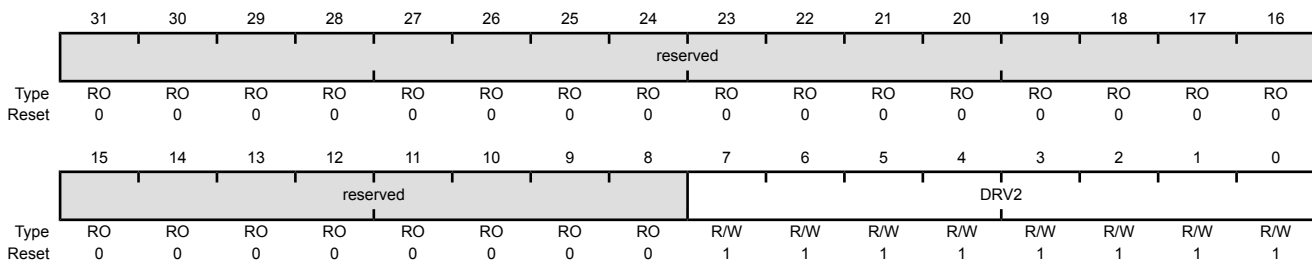
### Register 11: GPIO 2-mA Drive Select (GPIODR2R), offset 0x500

The **GPIODR2R** register is the 2-mA drive control register. Each GPIO signal in the port can be individually configured without affecting the other pads. When setting the **DRV2** bit for a GPIO signal, the corresponding **DRV4** bit in the **GPIODR4R** register and **DRV8** bit in the **GPIODR8R** register are automatically cleared by hardware. By default, all GPIO pins have 2-mA drive.

#### GPIO 2-mA Drive Select (GPIODR2R)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x500

Type R/W, reset 0x0000.00FF



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DRV2	R/W	0xFF	Output Pad 2-mA Drive Enable

Value	Description
1	The corresponding GPIO pin has 2-mA drive.
0	The drive for the corresponding GPIO pin is controlled by the <b>GPIODR4R</b> or <b>GPIODR8R</b> register.

Setting a bit in either the **GPIODR4** register or the **GPIODR8** register clears the corresponding 2-mA enable bit. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.



## Register 12: GPIO 4-mA Drive Select (GPIODR4R), offset 0x504

The **GPIODR4R** register is the 4-mA drive control register. Each GPIO signal in the port can be individually configured without affecting the other pads. When setting the **DRV4** bit for a GPIO signal, the corresponding **DRV2** bit in the **GPIODR2R** register and **DRV8** bit in the **GPIODR8R** register are automatically cleared by hardware.

### GPIO 4-mA Drive Select (GPIODR4R)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x504

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DRV4							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DRV4	R/W	0x00	Output Pad 4-mA Drive Enable

#### Value Description

Value	Description
1	The corresponding GPIO pin has 4-mA drive.
0	The drive for the corresponding GPIO pin is controlled by the <b>GPIODR2R</b> or <b>GPIODR8R</b> register.

Setting a bit in either the **GPIODR2** register or the **GPIODR8** register clears the corresponding 4-mA enable bit. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.

### Register 13: GPIO 8-mA Drive Select (GPIODR8R), offset 0x508

The **GPIODR8R** register is the 8-mA drive control register. Each GPIO signal in the port can be individually configured without affecting the other pads. When setting the **DRV8** bit for a GPIO signal, the corresponding **DRV2** bit in the **GPIODR2R** register and **DRV4** bit in the **GPIODR4R** register are automatically cleared by hardware. The 8-mA setting is also used for high-current operation.

**Note:** There is no configuration difference between 8-mA and high-current operation. The additional current capacity results from a shift in the  $V_{OH}/V_{OL}$  levels. See “Recommended DC Operating Conditions” on page 726 for further information.

#### GPIO 8-mA Drive Select (GPIODR8R)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x508  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DRV8							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DRV8	R/W	0x00	Output Pad 8-mA Drive Enable

Value	Description
1	The corresponding GPIO pin has 8-mA drive.
0	The drive for the corresponding GPIO pin is controlled by the <b>GPIODR2R</b> or <b>GPIODR4R</b> register.

Setting a bit in either the **GPIODR2** register or the **GPIODR4** register clears the corresponding 8-mA enable bit. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.

## Register 14: GPIO Open Drain Select (GPIOODR), offset 0x50C

The **GPIOODR** register is the open drain control register. Setting a bit in this register enables the open-drain configuration of the corresponding GPIO pad. When open-drain mode is enabled, the corresponding bit should also be set in the **GPIO Digital Input Enable (GPIODEN)** register (see page 321). Corresponding bits in the drive strength and slew rate control registers (**GPIODR2R**, **GPIODR4R**, **GPIODR8R**, and **GPIOSLR**) can be set to achieve the desired rise and fall times. The GPIO acts as an open-drain input if the corresponding bit in the **GPIODIR** register is cleared. If open drain is selected while the GPIO is configured as an input, the GPIO will remain an input and the open-drain selection has no effect until the GPIO is changed to an output.

When using the I<sup>2</sup>C module, in addition to configuring the pin to open drain, the **GPIO Alternate Function Select (GPIOAFSEL)** register bits for the I<sup>2</sup>C clock and data pins should be set (see examples in “Initialization and Configuration” on page 295).

### GPIO Open Drain Select (GPIOODR)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x50C  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								ODE							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	ODE	R/W	0x00	Output Pad Open Drain Enable

#### Value Description

1	The corresponding pin is configured as open drain.
0	The corresponding pin is not configured as open drain.

**Register 15: GPIO Pull-Up Select (GPIOPUR), offset 0x510**

The **GPIOPUR** register is the pull-up control register. When a bit is set, a weak pull-up resistor on the corresponding GPIO signal is enabled. Setting a bit in **GPIOPUR** automatically clears the corresponding bit in the **GPIO Pull-Down Select (GPIOPDR)** register (see page 318). Write access to this register is protected with the **GPIOCR** register. Bits in **GPIOCR** that are cleared prevent writes to the equivalent bit in this register.

**Important:** All GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL**=0, **GPIODEN**=0, **GPIOPDR**=0, **GPIOPUR**=0, and **GPIOCTL**=0) with the exception of the pins shown in the table below. A Power-On-Reset (**POR**) or asserting **RST** puts the pins back to their default state.

**Table 10-8. GPIO Pins With Non-Zero Reset Values**

GPIO Pins	Default State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOCTL
PA[1:0]	UART0	1	1	0	0	0x1
PA[5:2]	SSI0	1	1	0	0	0x1
PB[3:2]	I <sup>2</sup> C0	1	1	0	0	0x1
PC[3:0]	JTAG/SWD	1	1	0	1	0x3

**Note:** The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is currently provided for the **NMI** pin (**PB7**) and the four **JTAG/SWD** pins (**PC[3:0]**). Writes to protected bits of the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 310), **GPIO Pull Up Select (GPIOPUR)** register (see page 316), **GPIO Pull-Down Select (GPIOPDR)** register (see page 318), and **GPIO Digital Enable (GPIODEN)** register (see page 321) are not committed to storage unless the **GPIO Lock (GPIOLOCK)** register (see page 323) has been unlocked and the appropriate bits of the **GPIO Commit (GPIOCR)** register (see page 324) have been set.

GPIO Pull-Up Select (GPIOPUR)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000

Offset 0x510  
 Type R/W, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PUE							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PUE	R/W	-	Pad Weak Pull-Up Enable

Value	Description
1	The corresponding pin has a weak pull-up resistor.
0	The corresponding pin is not affected.

Setting a bit in the **GPIOPDR** register clears the corresponding bit in the **GPIOPUR** register. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.

The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in Table 10-1 on page 289.

### Register 16: GPIO Pull-Down Select (GPIOPDR), offset 0x514

The **GPIOPDR** register is the pull-down control register. When a bit is set, a weak pull-down resistor on the corresponding GPIO signal is enabled. Setting a bit in **GPIOPDR** automatically clears the corresponding bit in the **GPIO Pull-Up Select (GPIOPUR)** register (see page 316).

**Important:** All GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL=0**, **GPIODEN=0**, **GPIOPDR=0**, **GPIOPUR=0**, and **GPIOCTL=0**) with the exception of the pins shown in the table below. A Power-On-Reset (**POR**) or asserting **RST** puts the pins back to their default state.

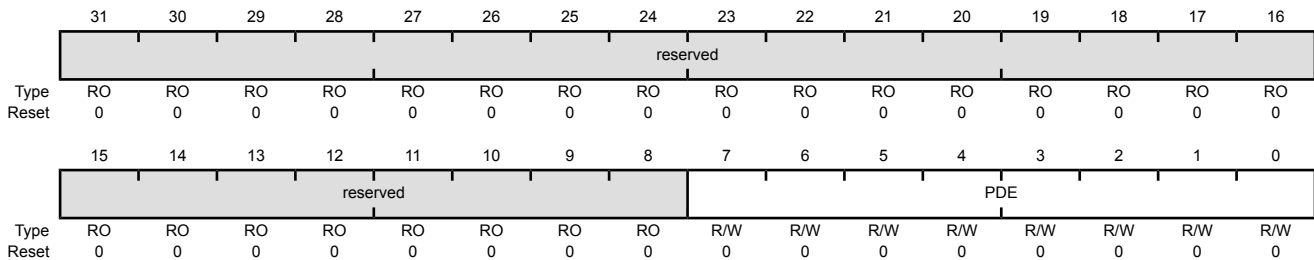
**Table 10-9. GPIO Pins With Non-Zero Reset Values**

GPIO Pins	Default State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOCTL
PA[1:0]	UART0	1	1	0	0	0x1
PA[5:2]	SSI0	1	1	0	0	0x1
PB[3:2]	I <sup>2</sup> C0	1	1	0	0	0x1
PC[3:0]	JTAG/SWD	1	1	0	1	0x3

**Note:** The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is currently provided for the **NMI** pin (**PB7**) and the four **JTAG/SWD** pins (**PC[3:0]**). Writes to protected bits of the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 310), **GPIO Pull Up Select (GPIOPUR)** register (see page 316), **GPIO Pull-Down Select (GPIOPDR)** register (see page 318), and **GPIO Digital Enable (GPIODEN)** register (see page 321) are not committed to storage unless the **GPIO Lock (GPIOLOCK)** register (see page 323) has been unlocked and the appropriate bits of the **GPIO Commit (GPIOCR)** register (see page 324) have been set.

#### GPIO Pull-Down Select (GPIOPDR)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x514  
 Type R/W, reset 0x0000.0000



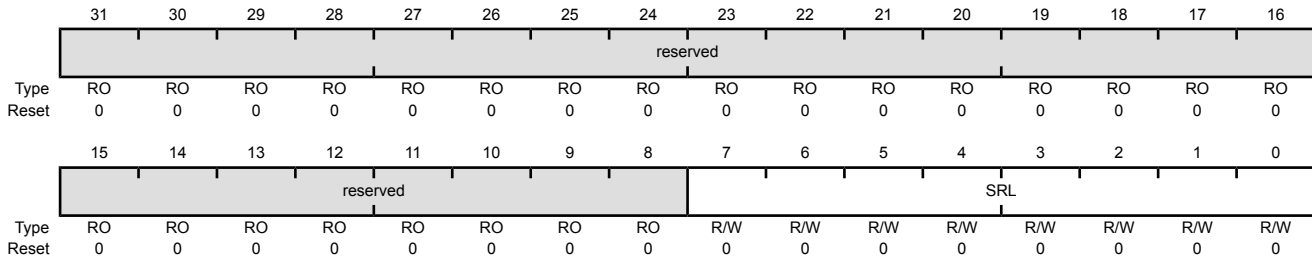
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PDE	R/W	0x00	Pad Weak Pull-Down Enable
				<p>Value Description</p> <p>1 The corresponding pin has a weak pull-down resistor.</p> <p>0 The corresponding pin is not affected.</p> <p>Setting a bit in the <b>GPIOPUR</b> register clears the corresponding bit in the <b>GPIOPDR</b> register. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.</p>

### Register 17: GPIO Slew Rate Control Select (GPIOSLR), offset 0x518

The **GPIOSLR** register is the slew rate control register. Slew rate control is only available when using the 8-mA drive strength option via the **GPIO 8-mA Drive Select (GPIODR8R)** register (see page 314).

#### GPIO Slew Rate Control Select (GPIOSLR)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x518  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description	
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.	
7:0	SRL	R/W	0x00	Slew Rate Limit Enable (8-mA drive only)	
Value Description					
	1	Slew rate control is enabled for the corresponding pin.			
	0	Slew rate control is disabled for the corresponding pin.			



## Register 18: GPIO Digital Enable (GPIODEN), offset 0x51C

**Note:** Pins configured as digital inputs are Schmitt-triggered.

The **GPIODEN** register is the digital enable register. By default, all GPIO signals except those listed below are configured out of reset to be undriven (tristate). Their digital function is disabled; they do not drive a logic value on the pin and they do not allow the pin voltage into the GPIO receiver. To use the pin as a digital input or output (either GPIO or alternate function), the corresponding **GPIODEN** bit must be set.

**Important:** All GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL**=0, **GPIODEN**=0, **GPIOPDR**=0, **GPIOPUR**=0, and **GPIOPCTL**=0) with the exception of the pins shown in the table below. A Power-On-Reset ( $\overline{POR}$ ) or asserting  $\overline{RST}$  puts the pins back to their default state.

**Table 10-10. GPIO Pins With Non-Zero Reset Values**

GPIO Pins	Default State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOPCTL
PA[1:0]	UART0	1	1	0	0	0x1
PA[5:2]	SSI0	1	1	0	0	0x1
PB[3:2]	I <sup>2</sup> C0	1	1	0	0	0x1
PC[3:0]	JTAG/SWD	1	1	0	1	0x3

**Note:** The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is currently provided for the **NMI** pin (**PB7**) and the four JTAG/SWD pins (**PC[3:0]**). Writes to protected bits of the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 310), **GPIO Pull Up Select (GPIOPUR)** register (see page 316), **GPIO Pull-Down Select (GPIOPDR)** register (see page 318), and **GPIO Digital Enable (GPIODEN)** register (see page 321) are not committed to storage unless the **GPIO Lock (GPIOLOCK)** register (see page 323) has been unlocked and the appropriate bits of the **GPIO Commit (GPIOCR)** register (see page 324) have been set.

GPIO Digital Enable (GPIODEN)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000

Offset 0x51C  
 Type R/W, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DEN							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DEN	R/W	-	Digital Enable

Value	Description
0	The digital functions for the corresponding pin are disabled.
1	The digital functions for the corresponding pin are enabled.

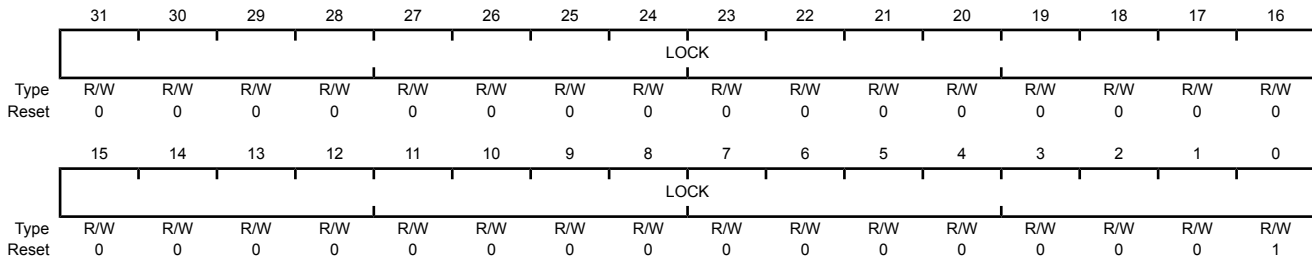
The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in Table 10-1 on page 289.

### Register 19: GPIO Lock (GPIOLOCK), offset 0x520

The **GPIOLOCK** register enables write access to the **GPIOCR** register (see page 324). Writing 0x4C4F.434B to the **GPIOLOCK** register unlocks the **GPIOCR** register. Writing any other value to the **GPIOLOCK** register re-enables the locked state. Reading the **GPIOLOCK** register returns the lock status rather than the 32-bit value that was previously written. Therefore, when write accesses are disabled, or locked, reading the **GPIOLOCK** register returns 0x0000.0001. When write accesses are enabled, or unlocked, reading the **GPIOLOCK** register returns 0x0000.0000.

#### GPIO Lock (GPIOLOCK)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x520  
 Type R/W, reset 0x0000.0001



Bit/Field	Name	Type	Reset	Description
31:0	LOCK	R/W	0x0000.0001	GPIO Lock

A write of the value 0x4C4F.434B unlocks the **GPIO Commit (GPIOCR)** register for write access. A write of any other value or a write to the **GPIOCR** register reapplies the lock, preventing any register updates.

A read of this register returns the following values:

Value	Description
0x0000.0001	The <b>GPIOCR</b> register is locked and may not be modified.
0x0000.0000	The <b>GPIOCR</b> register is unlocked and may be modified.

### Register 20: GPIO Commit (GPIOCR), offset 0x524

The **GPIOCR** register is the commit register. The value of the **GPIOCR** register determines which bits of the **GPIOAFSEL**, **GPIOPUR**, **GPIOPDR**, and **GPIONEN** registers are committed when a write to these registers is performed. If a bit in the **GPIOCR** register is cleared, the data being written to the corresponding bit in the **GPIOAFSEL**, **GPIOPUR**, **GPIOPDR**, or **GPIONEN** registers cannot be committed and retains its previous value. If a bit in the **GPIOCR** register is set, the data being written to the corresponding bit of the **GPIOAFSEL**, **GPIOPUR**, **GPIOPDR**, or **GPIONEN** registers is committed to the register and reflects the new value.

The contents of the **GPIOCR** register can only be modified if the status in the **GPIOLOCK** register is unlocked. Writes to the **GPIOCR** register are ignored if the status in the **GPIOLOCK** register is locked.

**Important:** This register is designed to prevent accidental programming of the registers that control connectivity to the NMI and JTAG/SWD debug hardware. By initializing the bits of the **GPIOCR** register to 0 for **PB7** and **PC[3:0]**, the NMI and JTAG/SWD debug port can only be converted to GPIOs through a deliberate set of writes to the **GPIOLOCK**, **GPIOCR**, and the corresponding registers.

Because this protection is currently only implemented on the NMI and JTAG/SWD pins on **PB7** and **PC[3:0]**, all of the other bits in the **GPIOCR** registers cannot be written with 0x0. These bits are hardwired to 0x1, ensuring that it is always possible to commit new values to the **GPIOAFSEL**, **GPIOPUR**, **GPIOPDR**, or **GPIONEN** register bits of these other pins.

#### GPIO Commit (GPIOCR)

- GPIO Port A (APB) base: 0x4000.4000
- GPIO Port A (AHB) base: 0x4005.8000
- GPIO Port B (APB) base: 0x4000.5000
- GPIO Port B (AHB) base: 0x4005.9000
- GPIO Port C (APB) base: 0x4000.6000
- GPIO Port C (AHB) base: 0x4005.A000
- GPIO Port D (APB) base: 0x4000.7000
- GPIO Port D (AHB) base: 0x4005.B000
- GPIO Port E (APB) base: 0x4002.4000
- GPIO Port E (AHB) base: 0x4005.C000
- GPIO Port F (APB) base: 0x4002.5000
- GPIO Port F (AHB) base: 0x4005.D000
- GPIO Port G (APB) base: 0x4002.6000
- GPIO Port G (AHB) base: 0x4005.E000
- GPIO Port H (APB) base: 0x4002.7000
- GPIO Port H (AHB) base: 0x4005.F000
- GPIO Port J (APB) base: 0x4003.D000
- GPIO Port J (AHB) base: 0x4006.0000

Offset 0x524  
Type -, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CR							
Type	RO	RO	RO	RO	RO	RO	RO	RO	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CR	-	-	GPIO Commit
				Value Description
				1 The corresponding <b>GPIOAFSEL</b> , <b>GPIOPUR</b> , <b>GPIOPDR</b> , or <b>GIODEN</b> bits can be written.
				0 The corresponding <b>GPIOAFSEL</b> , <b>GPIOPUR</b> , <b>GPIOPDR</b> , or <b>GIODEN</b> bits cannot be written.
				<b>Note:</b> The default register type for the <b>GPIOCR</b> register is RO for all GPIO pins with the exception of the <b>NMI</b> pin and the four JTAG/SWD pins ( <b>PB7</b> and <b>PC[3:0]</b> ). These five pins are currently the only GPIOs that are protected by the <b>GPIOCR</b> register. Because of this, the register type for GPIO Port B7 and GPIO Port C[3:0] is R/W.
				The default reset value for the <b>GPIOCR</b> register is 0x0000.00FF for all GPIO pins, with the exception of the <b>NMI</b> pin and the four JTAG/SWD pins ( <b>PB7</b> and <b>PC[3:0]</b> ). To ensure that the JTAG port is not accidentally programmed as a GPIO, these four pins default to non-committable. To ensure that the <b>NMI</b> pin is not accidentally programmed as the non-maskable interrupt pin, it defaults to non-committable. Because of this, the default reset value of <b>GPIOCR</b> for GPIO Port B is 0x0000.007F while the default reset value of <b>GPIOCR</b> for Port C is 0x0000.00F0.

## Register 21: GPIO Analog Mode Select (GPIOAMSEL), offset 0x528

**Important:** This register is only valid for ports D and E; the corresponding base addresses for the remaining ports are not valid.

If any pin is to be used as an ADC input, the appropriate bit in **GPIOAMSEL** must be set to disable the analog isolation circuit.

The **GPIOAMSEL** register controls isolation circuits to the analog side of a unified I/O pad. Because the GPIOs may be driven by a 5-V source and affect analog operation, analog circuitry requires isolation from the pins when they are not used in their analog function.

Each bit of this register controls the isolation circuitry for the corresponding GPIO signal. For information on which GPIO pins can be used for ADC functions, refer to Table 20-5 on page 722.

### GPIO Analog Mode Select (GPIOAMSEL)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0x528  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								GPIOAMSEL				reserved			
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
7:4	GPIOAMSEL	R/W	0x0	<p>GPIO Analog Mode Select</p> <p>Value Description</p> <p>1 The analog function of the pin is enabled, the isolation is disabled, and the pin is capable of analog functions.</p> <p>0 The analog function of the pin is disabled, the isolation is enabled, and the pin is capable of digital functions as specified by the other GPIO configuration registers.</p> <p><b>Note:</b> This register and bits are only valid for GPIO signals that share analog function through a unified I/O pad.</p> <p>The reset state of this register is 0 for all signals.</p>
3:0	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

### Register 22: GPIO Port Control (GPIOCTL), offset 0x52C

The **GPIOCTL** register is used in conjunction with the **GPIOAFSEL** register and selects the specific peripheral signal for each GPIO pin when using the alternate function mode. Most bits in the **GPIOAFSEL** register are cleared on reset, therefore most GPIO pins are configured as GPIOs by default. When a bit is set in the **GPIOAFSEL** register, the corresponding GPIO signal is controlled by an associated peripheral. The **GPIOCTL** register selects one out of a set of peripheral functions for each GPIO, providing additional flexibility in signal definition. For information on the defined encodings for the bit fields in this register, refer to Table 20-5 on page 722. The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in the table below.

**Important:** All GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL=0**, **GIODEN=0**, **GPIOPDR=0**, **GPIOPUR=0**, and **GPIOCTL=0**) with the exception of the pins shown in the table below. A Power-On-Reset ( $\overline{POR}$ ) or asserting  $\overline{RST}$  puts the pins back to their default state.

**Table 10-11. GPIO Pins With Non-Zero Reset Values**

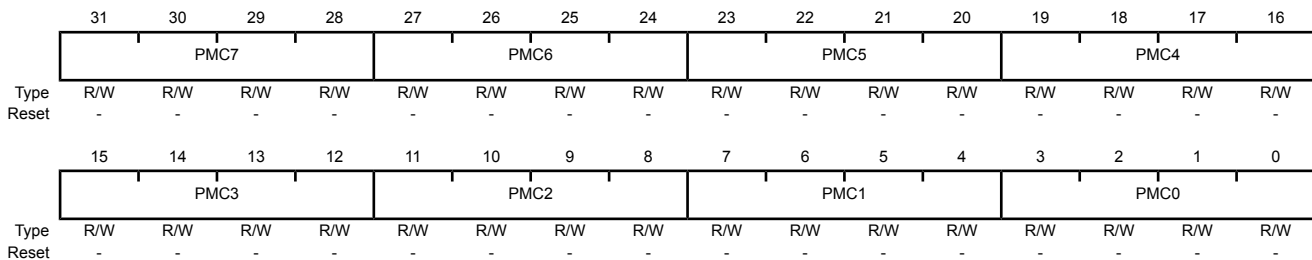
GPIO Pins	Default State	GPIOAFSEL	GIODEN	GPIOPDR	GPIOPUR	GPIOCTL
PA[1:0]	UART0	1	1	0	0	0x1
PA[5:2]	SSI0	1	1	0	0	0x1
PB[3:2]	I <sup>2</sup> C0	1	1	0	0	0x1
PC[3:0]	JTAG/SWD	1	1	0	1	0x3

#### GPIO Port Control (GPIOCTL)

- GPIO Port A (APB) base: 0x4000.4000
- GPIO Port A (AHB) base: 0x4005.8000
- GPIO Port B (APB) base: 0x4000.5000
- GPIO Port B (AHB) base: 0x4005.9000
- GPIO Port C (APB) base: 0x4000.6000
- GPIO Port C (AHB) base: 0x4005.A000
- GPIO Port D (APB) base: 0x4000.7000
- GPIO Port D (AHB) base: 0x4005.B000
- GPIO Port E (APB) base: 0x4002.4000
- GPIO Port E (AHB) base: 0x4005.C000
- GPIO Port F (APB) base: 0x4002.5000
- GPIO Port F (AHB) base: 0x4005.D000
- GPIO Port G (APB) base: 0x4002.6000
- GPIO Port G (AHB) base: 0x4005.E000
- GPIO Port H (APB) base: 0x4002.7000
- GPIO Port H (AHB) base: 0x4005.F000
- GPIO Port J (APB) base: 0x4003.D000
- GPIO Port J (AHB) base: 0x4006.0000

Offset 0x52C

Type R/W, reset -





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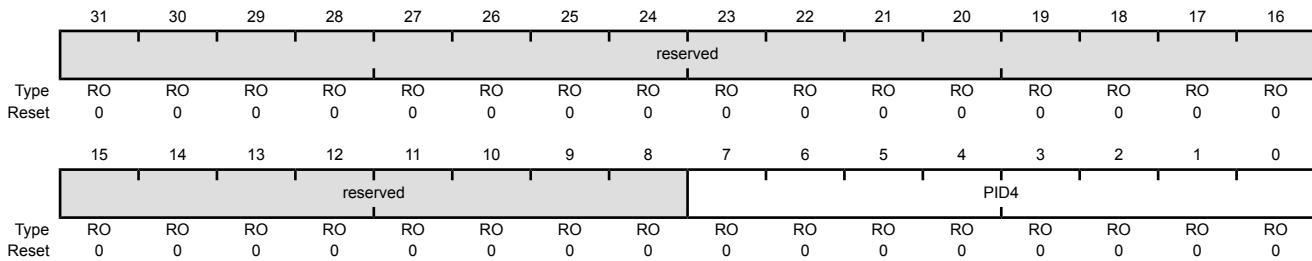
Bit/Field	Name	Type	Reset	Description
31:28	PMC7	R/W	-	Port Mux Control 7 This field controls the configuration for GPIO pin 7.
27:24	PMC6	R/W	-	Port Mux Control 6 This field controls the configuration for GPIO pin 6.
23:20	PMC5	R/W	-	Port Mux Control 5 This field controls the configuration for GPIO pin 5.
19:16	PMC4	R/W	-	Port Mux Control 4 This field controls the configuration for GPIO pin 4.
15:12	PMC3	R/W	-	Port Mux Control 3 This field controls the configuration for GPIO pin 3.
11:8	PMC2	R/W	-	Port Mux Control 2 This field controls the configuration for GPIO pin 2.
7:4	PMC1	R/W	-	Port Mux Control 1 This field controls the configuration for GPIO pin 1.
3:0	PMC0	R/W	-	Port Mux Control 0 This field controls the configuration for GPIO pin 0.

**Register 23: GPIO Peripheral Identification 4 (GPIOPeriphID4), offset 0xFD0**

The **GPIOPeriphID4**, **GPIOPeriphID5**, **GPIOPeriphID6**, and **GPIOPeriphID7** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

GPIO Peripheral Identification 4 (GPIOPeriphID4)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFD0  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID4	RO	0x00	GPIO Peripheral ID Register [7:0]

**Register 24: GPIO Peripheral Identification 5 (GPIOPeriphID5), offset 0xFD4**

The **GPIOPeriphID4**, **GPIOPeriphID5**, **GPIOPeriphID6**, and **GPIOPeriphID7** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

**GPIO Peripheral Identification 5 (GPIOPeriphID5)**

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFD4

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID5							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

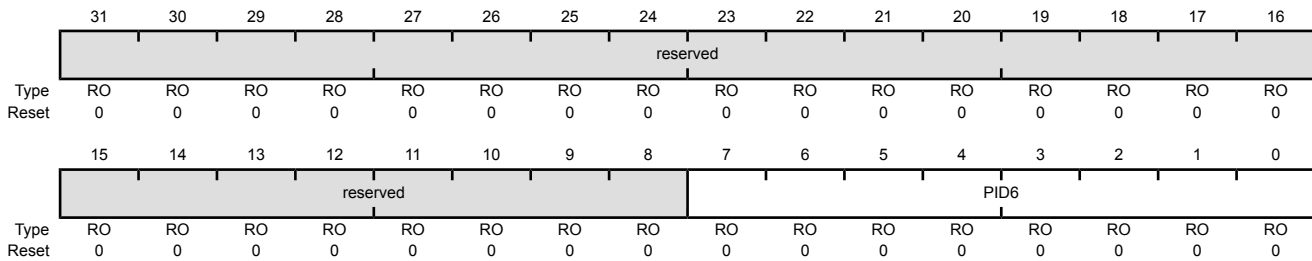
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID5	RO	0x00	GPIO Peripheral ID Register [15:8]

### Register 25: GPIO Peripheral Identification 6 (GPIOPeriphID6), offset 0xFD8

The **GPIOPeriphID4**, **GPIOPeriphID5**, **GPIOPeriphID6**, and **GPIOPeriphID7** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

#### GPIO Peripheral Identification 6 (GPIOPeriphID6)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFD8  
 Type RO, reset 0x0000.0000



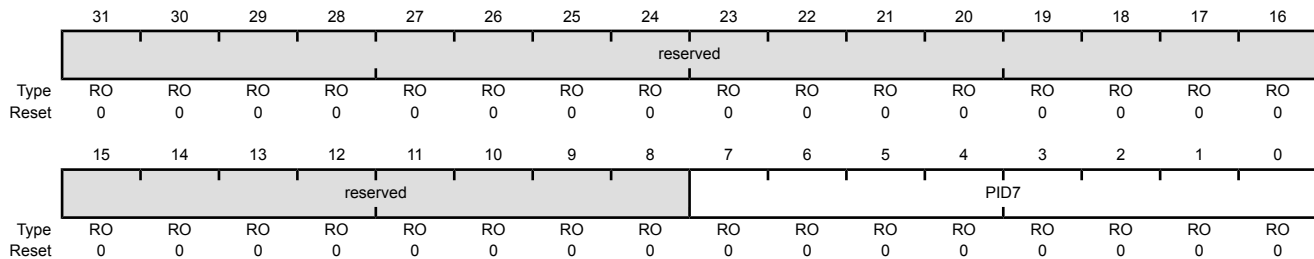
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID6	RO	0x00	GPIO Peripheral ID Register [23:16]

**Register 26: GPIO Peripheral Identification 7 (GPIOPeriphID7), offset 0xFDC**

The **GPIOPeriphID4**, **GPIOPeriphID5**, **GPIOPeriphID6**, and **GPIOPeriphID7** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

## GPIO Peripheral Identification 7 (GPIOPeriphID7)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFDC  
 Type RO, reset 0x0000.0000



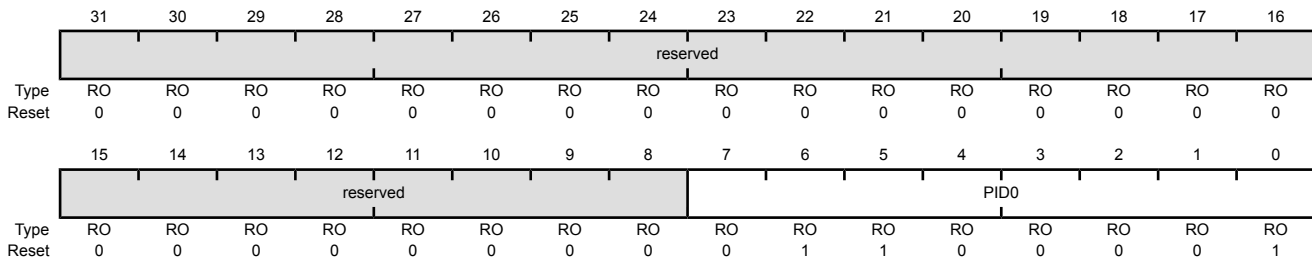
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID7	RO	0x00	GPIO Peripheral ID Register [31:24]

### Register 27: GPIO Peripheral Identification 0 (GPIOPeriphID0), offset 0xFE0

The **GPIOPeriphID0**, **GPIOPeriphID1**, **GPIOPeriphID2**, and **GPIOPeriphID3** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

#### GPIO Peripheral Identification 0 (GPIOPeriphID0)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFE0  
 Type RO, reset 0x0000.0061



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID0	RO	0x61	GPIO Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.

**Register 28: GPIO Peripheral Identification 1 (GPIOPeriphID1), offset 0xFE4**

The **GPIOPeriphID0**, **GPIOPeriphID1**, **GPIOPeriphID2**, and **GPIOPeriphID3** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

**GPIO Peripheral Identification 1 (GPIOPeriphID1)**

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFE4

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID1							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

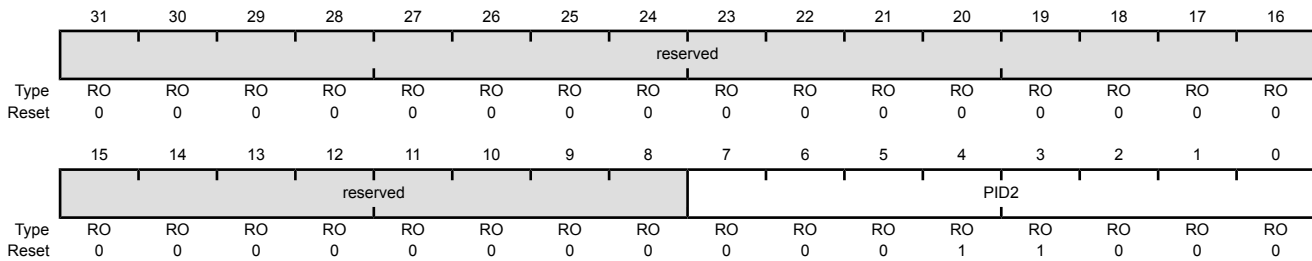
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID1	RO	0x00	GPIO Peripheral ID Register [15:8] Can be used by software to identify the presence of this peripheral.

### Register 29: GPIO Peripheral Identification 2 (GPIOPeriphID2), offset 0xFE8

The **GPIOPeriphID0**, **GPIOPeriphID1**, **GPIOPeriphID2**, and **GPIOPeriphID3** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

#### GPIO Peripheral Identification 2 (GPIOPeriphID2)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFE8  
 Type RO, reset 0x0000.0018



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID2	RO	0x18	GPIO Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.



**Register 30: GPIO Peripheral Identification 3 (GPIOPeriphID3), offset 0xFEC**

The **GPIOPeriphID0**, **GPIOPeriphID1**, **GPIOPeriphID2**, and **GPIOPeriphID3** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

**GPIO Peripheral Identification 3 (GPIOPeriphID3)**

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFEC

Type RO, reset 0x0000.0001

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

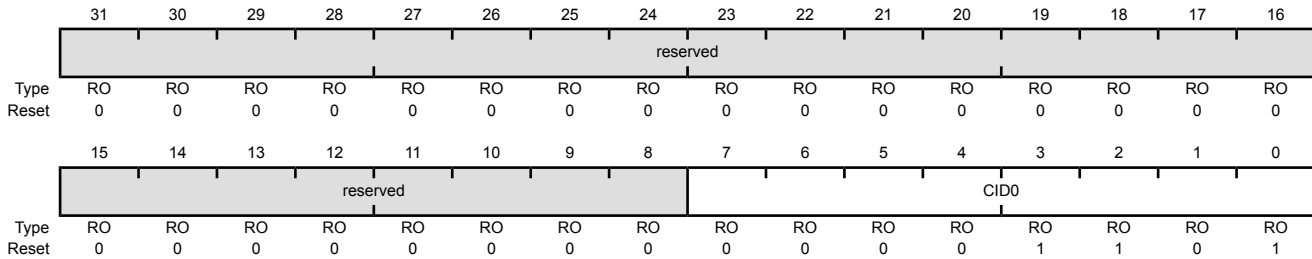
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID3	RO	0x01	GPIO Peripheral ID Register [31:24] Can be used by software to identify the presence of this peripheral.

### Register 31: GPIO PrimeCell Identification 0 (GPIOCellID0), offset 0xFF0

The **GPIOCellID0**, **GPIOCellID1**, **GPIOCellID2**, and **GPIOCellID3** registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

#### GPIO PrimeCell Identification 0 (GPIOCellID0)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFF0  
 Type RO, reset 0x0000.000D



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID0	RO	0x0D	GPIO PrimeCell ID Register [7:0] Provides software a standard cross-peripheral identification system.

**Register 32: GPIO PrimeCell Identification 1 (GPIOCellID1), offset 0xFF4**

The **GPIOCellID0**, **GPIOCellID1**, **GPIOCellID2**, and **GPIOCellID3** registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

## GPIO PrimeCell Identification 1 (GPIOCellID1)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFF4  
 Type RO, reset 0x0000.00F0

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID1							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

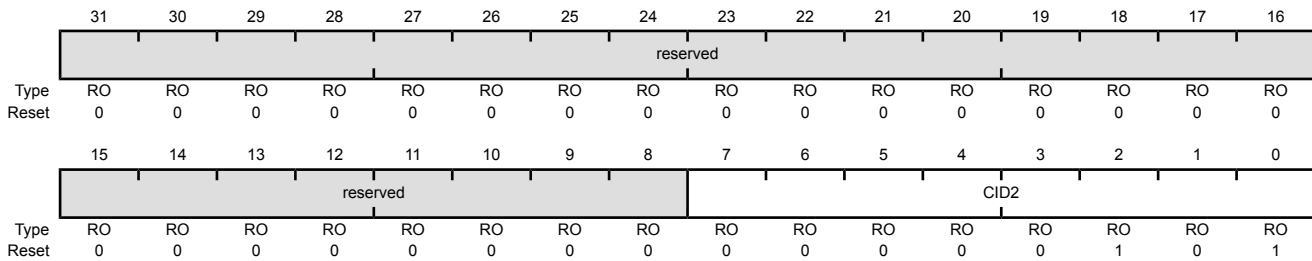
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID1	RO	0xF0	GPIO PrimeCell ID Register [15:8] Provides software a standard cross-peripheral identification system.

### Register 33: GPIO PrimeCell Identification 2 (GPIOCellID2), offset 0xFF8

The **GPIOCellID0**, **GPIOCellID1**, **GPIOCellID2**, and **GPIOCellID3** registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

#### GPIO PrimeCell Identification 2 (GPIOCellID2)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFF8  
 Type RO, reset 0x0000.0005



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID2	RO	0x05	GPIO PrimeCell ID Register [23:16] Provides software a standard cross-peripheral identification system.

## Register 34: GPIO PrimeCell Identification 3 (GPIOCellID3), offset 0xFFC

The **GPIOCellID0**, **GPIOCellID1**, **GPIOCellID2**, and **GPIOCellID3** registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

### GPIO PrimeCell Identification 3 (GPIOCellID3)

GPIO Port A (APB) base: 0x4000.4000  
 GPIO Port A (AHB) base: 0x4005.8000  
 GPIO Port B (APB) base: 0x4000.5000  
 GPIO Port B (AHB) base: 0x4005.9000  
 GPIO Port C (APB) base: 0x4000.6000  
 GPIO Port C (AHB) base: 0x4005.A000  
 GPIO Port D (APB) base: 0x4000.7000  
 GPIO Port D (AHB) base: 0x4005.B000  
 GPIO Port E (APB) base: 0x4002.4000  
 GPIO Port E (AHB) base: 0x4005.C000  
 GPIO Port F (APB) base: 0x4002.5000  
 GPIO Port F (AHB) base: 0x4005.D000  
 GPIO Port G (APB) base: 0x4002.6000  
 GPIO Port G (AHB) base: 0x4005.E000  
 GPIO Port H (APB) base: 0x4002.7000  
 GPIO Port H (AHB) base: 0x4005.F000  
 GPIO Port J (APB) base: 0x4003.D000  
 GPIO Port J (AHB) base: 0x4006.0000  
 Offset 0xFFC  
 Type RO, reset 0x0000.00B1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID3	RO	0xB1	GPIO PrimeCell ID Register [31:24] Provides software a standard cross-peripheral identification system.

## 11 External Peripheral Interface (EPI)

The External Peripheral Interface is a high-speed parallel bus for external peripherals or memory. It has several modes of operation to interface gluelessly to many types of external devices. The External Peripheral Interface is similar to a standard microprocessor address/data bus, except that it must typically be connected to just one type of external device. Enhanced capabilities include  $\mu$ DMA support, clocking control and support for external FIFO buffers.

The EPI has the following features:

- 8/16/32-bit dedicated parallel bus for external peripherals and memory
- Memory interface supports contiguous memory access independent of data bus width, thus enabling code execution directly from SDRAM, SRAM and Flash memory
- Blocking and non-blocking reads
- Separates processor from timing details through use of an internal write FIFO
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Separate channels for read and write
  - Read channel request asserted by programmable levels on the internal non-blocking read FIFO (NBRFIFO)
  - Write channel request asserted by empty on the internal write FIFO (WFIFO)

The EPI supports three primary functional modes: Synchronous Dynamic Random Access Memory (SDRAM) mode, Traditional Host-Bus mode, and General-Purpose mode. The EPI module also provides custom GPIOs; however, unlike regular GPIOs, the EPI module uses a FIFO in the same way as a communication mechanism and is speed-controlled using clocking.

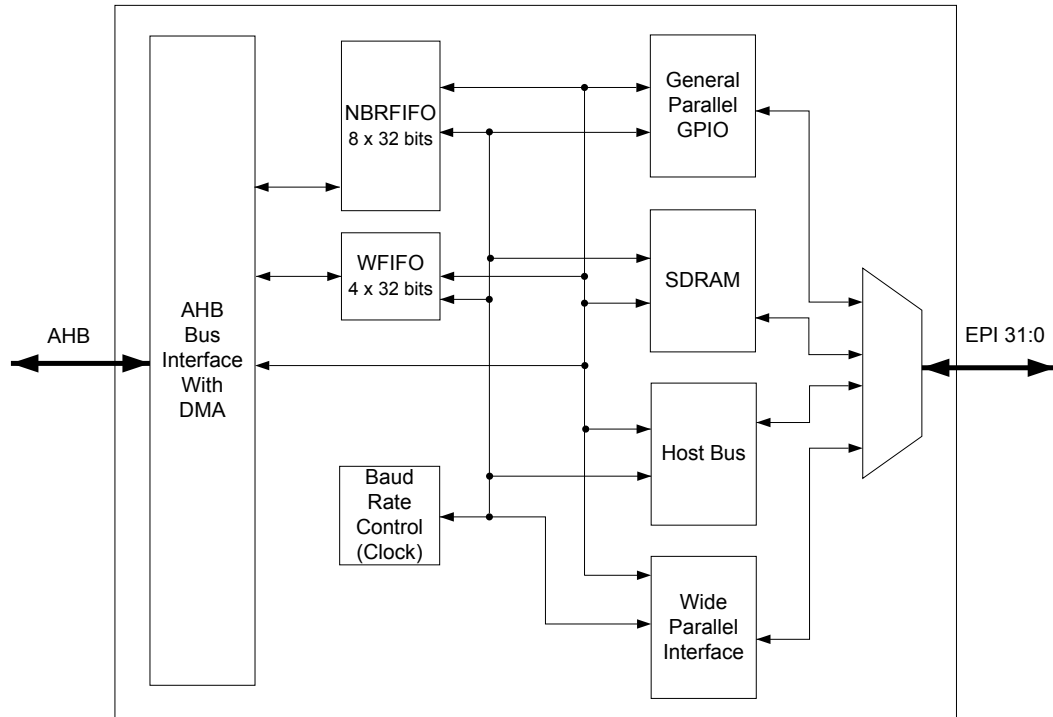
- Synchronous Dynamic Random Access Memory (SDRAM)
  - Supports x16 (single data rate) SDRAM at up to 50 MHz
  - Supports low-cost SDRAMs up to 64 MB (512 megabits)
  - Includes automatic refresh and access to all banks/rows
  - Includes a Sleep/Standby mode to keep contents active with minimal power draw
  - Multiplexed address/data interface for reduced pin count
- Host-bus
  - Traditional x8 and x16 MCU bus interface capabilities
  - Similar device compatibility options as PIC, ATmega, 8051, and others
  - Access to SRAM, NOR Flash memory, and other devices, with up to 1 MB of addressing in unmultiplexed mode and 256 MB in multiplexed mode
  - Support of both muxed and de-muxed address and data

- Access to a range of devices supporting the non-address FIFO x8 and x16 interface variant, with support for external FIFO (XFIFO) EMPTY and FULL signals
- Speed controlled, with read and write data wait-state counters
- Chip select modes include ALE, CSn, Dual CSn and ALE with dual CSn
- Manual chip-enable (or use extra address pins)
- General Purpose
  - Wide parallel interfaces for fast communications with CPLDs and FPGAs
  - Data widths up to 32-bits
  - Data rates up to 150 MB/second
  - Optional “address” sizes from 4-bits to 16-bits
  - Optional clock output, read/write strobes, framing (with counter-based size), and clock-enable input
- General parallel GPIO
  - 1 to 32 bits, FIFOed with speed control
  - Useful for custom peripherals or for digital data acquisition and actuator controls

## 11.1 EPI Block Diagram

Figure 11-1 on page 344 provides a block diagram of a Stellaris® EPI module.

Figure 11-1. EPI Block Diagram



## 11.2 Signal Description

Table 11-1 on page 344 lists the external signals of the EPI controller and describes the function of each. The EPI controller signals are alternate functions for GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the GPIO pin placement for the EPI signals. The **AFSEL** bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) should be set to choose the EPI controller function. The number in parentheses is the encoding that must be programmed into the **PMC<sub>n</sub>** field in the **GPIO Port Control (GPIOPCTL)** register (page 328) to assign the EPI signals to the specified GPIO port pins. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 288.

Table 11-1. Signals for External Peripheral Interface

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
EPI0S0	83	PH3 (8)	I/O	TTL	EPI module 0 signal 0.
EPI0S1	84	PH2 (8)	I/O	TTL	EPI module 0 signal 1.
EPI0S2	25	PC4 (8)	I/O	TTL	EPI module 0 signal 2.
EPI0S3	24	PC5 (8)	I/O	TTL	EPI module 0 signal 3.
EPI0S4	23	PC6 (8)	I/O	TTL	EPI module 0 signal 4.
EPI0S5	22	PC7 (8)	I/O	TTL	EPI module 0 signal 5.
EPI0S6	86	PH0 (8)	I/O	TTL	EPI module 0 signal 6.
EPI0S7	85	PH1 (8)	I/O	TTL	EPI module 0 signal 7.
EPI0S8	74	PE0 (8)	I/O	TTL	EPI module 0 signal 8.
EPI0S9	75	PE1 (8)	I/O	TTL	EPI module 0 signal 9.
EPI0S10	76	PH4 (8)	I/O	TTL	EPI module 0 signal 10.



Table 11-1. Signals for External Peripheral Interface (*continued*)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
EPI0S11	63	PH5 (8)	I/O	TTL	EPI module 0 signal 11.
EPI0S12	42 58	PF7 (8) PF4 (8)	I/O	TTL	EPI module 0 signal 12.
EPI0S13	19	PG0 (8)	I/O	TTL	EPI module 0 signal 13.
EPI0S14	18	PG1 (8)	I/O	TTL	EPI module 0 signal 14.
EPI0S15	41 46	PG4 (8) PF5 (8)	I/O	TTL	EPI module 0 signal 15.
EPI0S16	14	PJ0 (8)	I/O	TTL	EPI module 0 signal 16.
EPI0S17	87	PJ1 (8)	I/O	TTL	EPI module 0 signal 17.
EPI0S18	39	PJ2 (8)	I/O	TTL	EPI module 0 signal 18.
EPI0S19	97	PD4 (10)	I/O	TTL	EPI module 0 signal 19.
EPI0S20	12	PD2 (8)	I/O	TTL	EPI module 0 signal 20.
EPI0S21	13	PD3 (8)	I/O	TTL	EPI module 0 signal 21.
EPI0S22	91	PB5 (8)	I/O	TTL	EPI module 0 signal 22.
EPI0S23	92	PB4 (8)	I/O	TTL	EPI module 0 signal 23.
EPI0S24	95	PE2 (8)	I/O	TTL	EPI module 0 signal 24.
EPI0S25	96	PE3 (8)	I/O	TTL	EPI module 0 signal 25.
EPI0S26	62	PH6 (8)	I/O	TTL	EPI module 0 signal 26.
EPI0S27	15	PH7 (8)	I/O	TTL	EPI module 0 signal 27.
EPI0S28	98	PD5 (10)	I/O	TTL	EPI module 0 signal 28.
EPI0S29	99	PD6 (10)	I/O	TTL	EPI module 0 signal 29.
EPI0S30	100	PD7 (10)	I/O	TTL	EPI module 0 signal 30.
EPI0S31	36	PG7 (9)	I/O	TTL	EPI module 0 signal 31.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 11.3 Functional Description

The EPI controller provides a glueless, programmable interface to a variety of common external peripherals such as SDRAM, Host Bus x8 and x16 devices, RAM, Flash memory, CPLDs and FPGAs. In addition, the EPI controller provides custom GPIO that can use a FIFO with speed control by using either the internal write FIFO (WFIFO) or the non-blocking read FIFO (NBRFIFO). The WFIFO can hold 4 words of data that are written to the external interface at the rate controlled by the **EPI Main Baud Rate (EPIBAUD)** register. The NBRFIFO can hold 8 words of data and samples at the rate controlled by the **EPIBAUD** register. The EPI controller provides predictable operation and thus has an advantage over regular GPIO which has more variable timing due to on-chip bus arbitration and delays across bus bridges. Blocking reads stall the CPU until the transaction completes. Non-blocking reads are performed in the background and allow the processor to continue operation. In addition, write data can also be stored in the WFIFO to allow multiple writes with no stalls.

Main read and write operations can be performed in subsets of the range 0x6000.0000 to 0xCFFF.FFFF. A read from an address mapped location uses the offset and size to control the address and size of the external operation. When performing a multi-value load, the read is done as a burst (when available) to maximize performance. A write to an address mapped location uses the offset and size to control the address and size of the external operation. When performing a multi-value store, the write is done as a burst (when available) to maximize performance.

### 11.3.1 Non-Blocking Reads

The EPI Controller supports a special kind of read called a non-blocking read, also referred to as a posted read. Where a normal read stalls the processor or  $\mu$ DMA until the data is returned, a non-blocking read is performed in the background.

A non-blocking read is configured by writing the start address into a **EPIRADDR $n$**  register, the size per transaction into a **EPIRSIZEn** register, and then the count of operations into a **EPIRPSTD $n$**  register. After each read is completed, the result is written into the NBRFIFO and the **EPIRADDR $n$**  register is incremented by the size (1, 2, or 4).

If the NBRFIFO is filled, then the reads pause until space is made available. The NBRFIFO can be configured to interrupt the processor or trigger the  $\mu$ DMA based on fullness using the **EPIFIFOLVL** register. By using the trigger/interrupt method, the  $\mu$ DMA (or processor) can keep space available in the NBRFIFO and allow the reads to continue unimpeded.

When performing non-blocking reads, the SDRAM controller issues two additional read transactions after the burst request is terminated. The data for these additional transfers is discarded. This situation is transparent to the user other than the additional EPI bus activity and can safely be ignored.

Two non-blocking read register sets are available to allow sequencing and ping-pong use. When one completes, the other then activates. So, for example, if 20 words are to be read from 0x100 and 10 words from 0x200, the **EPIRPSTD0** register can be set up with the read from 0x100 (with a count of 20), and the **EPIRPSTD1** register can be set up with the read from 0x200 (with a count of 10). When **EPIRPSTD0** finishes (count goes to 0), the **EPIRPSTD1** register then starts its operation. The NBRFIFO has then passed 30 values. When used with the  $\mu$ DMA, it may transfer 30 values (simple sequence), or the primary/alternate model may be used to handle the first 20 in one way and the second 10 in another. It is also possible to reload the **EPIRPSTD0** register when it is finished (and the **EPIRPSTD1** register is active); thereby, keeping the interface constantly busy.

To cancel a non-blocking read, the **EPIRPSTD $n$**  register is cleared. Care must be taken, however if the register set was active to drain away any values read into the NBRFIFO and ensure that any read in progress is allowed to complete.

To ensure that the cancel is complete, the following algorithm is used (using the **EPIRPSTD0** register for example):

```
EPIRPSTD0 = 0;
while ((EPISTAT & 0x11) == 0x10)
; // we are active and busy
// if here, then other one is active or interface no longer busy
cnt = (EPIRADDR0 – original_address) / EPIRSIZE0; // count of values read
cnt -= values_read_so_far;
// cnt is now number left in FIFO
while (cnt-->0)
value = EPIREADFIFO; // drain
```

The above algorithm can be optimized in code; however, the important point is to wait for the cancel to complete because the external interface could have been in the process of reading a value when the cancel came in, and it must be allowed to complete.

### 11.3.2 DMA Operation

The  $\mu$ DMA can be used to efficiently transfer data from and to the NBRFIFO and the WFIFO. The  $\mu$ DMA has one channel for write and one for read. The write channel copies values to the WFIFO when the WFIFO is at the level specified by the **EPI FIFO Level Selects (EPIFIFOLVL)** register. The non-blocking read channel copies values from the NBRFIFO when the NBRFIFO is at the level specified by the **EPIFIFOLVL** register. For non-blocking reads, the start address, the size per transaction, and the count of elements must be programmed in the  $\mu$ DMA. Note that both non-blocking read register sets can be used, and they fill the NBRFIFO such that one runs to completion, then the next one starts (they do not interleave).

For blocking reads, the  $\mu$ DMA software channel (or another unused channel) is used for memory-to-memory transfers (or memory to peripheral, where some other peripheral is used). In this situation, the  $\mu$ DMA stalls until the read is complete and is not able to service another channel until the read is done. As a result, the arbitration size should normally be programmed to one access at a time. The  $\mu$ DMA controller can also transfer from and to the NBRFIFO and the WFIFO using the  $\mu$ DMA software channel in memory mode, however, the  $\mu$ DMA is stalled once the NBRFIFO is empty or the WFIFO is full. Note that when the  $\mu$ DMA controller is stalled, the core continues operation. See “Micro Direct Memory Access ( $\mu$ DMA)” on page 230 for more information on configuring the  $\mu$ DMA.

## 11.4 Initialization and Configuration

To enable and initialize the EPI controller, the following steps are necessary:

1. Enable the EPI module using the **RCGC1** register. See page 149.
2. Enable the clock to the appropriate GPIO module via the **RCGC2** register. See page 158. To find out which GPIO port to enable, refer to Table 11-1 on page 344.
3. Set the GPIO **AFSEL** bits for the appropriate pins. See page 310. To determine which GPIOs to configure, see Table 20-4 on page 717.
4. Configure the GPIO current level and/or slew rate as specified for the mode selected. See page 312 and page 320.
5. Configure the **PMC<sub>n</sub>** fields in the **GPIOPCTL** register to assign the EPI signals to the appropriate pins. See page 328 and Table 20-5 on page 722.
6. Select the mode for the EPI block to SDRAM, HB8, HB16, or general parallel use, using the **MODE** field in the **EPI Configuration (EPICFG)** register. Set the mode-specific details (if needed) using the appropriate mode configuration **EPI xxx Configuration (EPIxxxCFG)** and **EPI xxx Configuration 2 (EPIxxxCFG2)** registers. Set the **EPI Main Baud Rate (EPIBAUD)** register if the baud rate must be slower than the system clock rate.
7. Configure the address mapping using the **EPI Address Map (EPIADDRMAP)** register. The selected start address and range is dependent on the type of external device and maximum address (as appropriate). For example, for a 512-megabit SDRAM, program the **ERADR** field to 0x1 for address 0x6000.0000 or 0x2 for address 0x8000.0000; and program the **ERSZ** field to 0x3 for 256 MB. If using General-Purpose mode and no address at all, program the **EPADR** field to 0x1 for address 0xA000.0000 or 0x2 for address 0xC000.0000; and program the **EPSZ** field to 0x0 for 256 bytes.

8. To read or write directly, use the mapped address area (configured with the **EPIADDRMAP** register). Up to 4 or 5 writes can be performed at once without blocking. Each read is blocked until the value is retrieved.
9. To perform a non-blocking read, see “Non-Blocking Reads” on page 346.

The following sub-sections describe the initialization and configuration for each of the modes of operation. Care must be taken to initialize everything properly to ensure correct operation. Control of the GPIO states is also important, as changes may cause the external device to interpret pin states as actions or commands (see “Register Descriptions” on page 299). Normally, a pull-up or pull-down is needed on the board to at least control the chip-select or chip-enable as the Stellaris® GPIOs come out of reset in tri-state.

### 11.4.1 SDRAM Mode

When activating the SDRAM mode, it is important to consider a few points:

1. Generally, it takes over 100  $\mu$ s from when the mode is activated to when the first operation is allowed. The SDRAM controller begins the SDRAM initialization sequence as soon as the mode is selected and enabled via the **EPICFG** register. It is important that the GPIOs are properly configured before the SDRAM mode is enabled, as the EPI controller is relying on the GPIO block's ability to drive the pins immediately. As part of the initialization sequence, the LOAD MODE REGISTER command is automatically sent to the SDRAM with a value of 0x27, which sets a CAS latency of 2 and a full page burst length.
2. The **INITSEQ** bit in the **EPI Status (EPISTAT)** register can be checked to determine when the initialization sequence is complete.
3. When using a frequency range and/or refresh value other than the default value, it is important to configure the **FREQ** and **RFSH** fields in the **EPI SDRAM Configuration (EPISDRAMCFG)** register shortly after activating the mode. After the 100- $\mu$ s startup time, the EPI block must be configured properly to keep the SDRAM contents stable.
4. The **SLEEP** bit in the **EPISDRAMCFG** register may be configured to put the SDRAM into a low-power self-refreshing state. It is important to note that the SDRAM mode must not be disabled once enabled, or else the SDRAM is no longer clocked and the contents are lost.

The **SIZE** field of the **EPISDRAMCFG** register must be configured correctly based on the amount of SDRAM in the system.

The **FREQ** field must be configured according to the value that represents the range being used. Based on the range selected, the number of external clocks used between certain operations (for example, **PRECHARGE** or **ACTIVATE**) is determined. If a higher frequency is given than is used, then the only downside is that the peripheral is slower (uses more cycles for these delays). If a lower frequency is given, incorrect operation occurs.

See “External Peripheral Interface (EPI)” on page 736 for timing details for the SDRAM mode.

#### 11.4.1.1 External Signal Connections

The Table 11-2 on page 349 table defines how EPI module signals should be connected to SDRAMs. The table applies when using a x16 SDRAM up to 512 megabits. Note that the EPI signals must use 8-mA drive when interfacing to SDRAM, see page 314. Any unused EPI controller signals can be used as GPIOs or another alternate function.

Table 11-2. EPI SDRAM Signal Connections

EPI Signal	SDRAM Signal <sup>a</sup>	
EPI0S0	A0	D0
EPI0S1	A1	D1
EPI0S2	A2	D2
EPI0S3	A3	D3
EPI0S4	A4	D4
EPI0S5	A5	D5
EPI0S6	A6	D6
EPI0S7	A7	D7
EPI0S8	A8	D8
EPI0S9	A9	D9
EPI0S10	A10	D10
EPI0S11	A11	D11
EPI0S12	A12 <sup>b</sup>	D12
EPI0S13	BA0	D13
EPI0S14	BA1	D14
EPI0S15	D15	
EPI0S16	DQML	
EPI0S17	DQMH	
EPI0S18	CASn	
EPI0S19	RASn	
EPI0S20-EPI0S27	not used	
EPI0S28	WEn	
EPI0S29	CSn	
EPI0S30	CKE	
EPI0S31	CLK	

a. If 2 signals are listed, connect the EPI signal to both pins.

b. Only for 256/512 megabit SDRAMs

#### 11.4.1.2 Refresh Configuration

The refresh count is based on the external clock speed and the number of rows per bank as well as the refresh period. The `RFSH` field represents how many external clock cycles remain before an AUTO-REFRESH is required. The normal formula is:

$$RFSH = (t_{Refresh\_us} / number\_rows) / ext\_clock\_period$$

A refresh period is normally 64 ms, or 64000  $\mu$ s. The number of rows is normally 4096 or 8192. The `ext_clock_period` is a value expressed in  $\mu$ sec and is derived by dividing 1000 by the clock speed expressed in MHz. So, 50 MHz is  $1000/50=20$  ns, or 0.02  $\mu$ s. A typical SDRAM is 4096 rows per bank if the system clock is running at 50 MHz with an **EPIBAUD** register value of 0:

$$RFSH = (64000/4096) / 0.02 = 15.625 \mu s / 0.02 \mu s = 781.25$$

The default value in the `RFSH` field is 750 decimal or 0x2EE to allow for a margin of safety and providing 15  $\mu$ s per refresh. It is important to note that this number should always be smaller or equal to what is required by the above equation. For example, if running the external clock at 25 MHz (40 ns per clock period), 390 is the highest number that may be used. Note that the external

clock may be 25 MHz when the system clock is 25 MHz or when the system clock is 50 MHz and configuring the `COUNT0` field in the **EPIBAUD** register to 1 (divide by 2).

If a number larger than allowed is used, the SDRAM is not refreshed often enough, and data is lost.

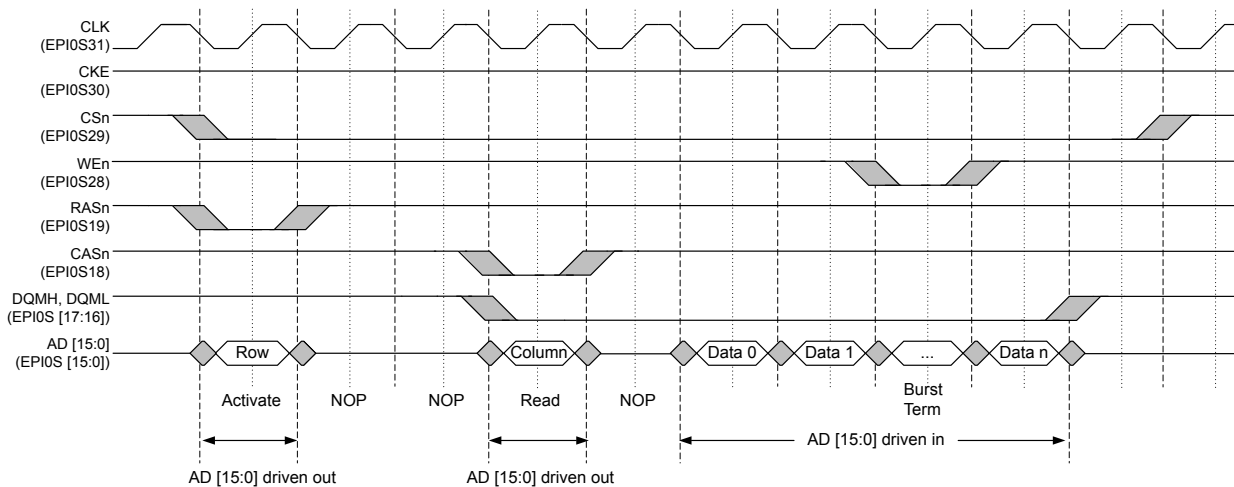
### 11.4.1.3 Bus Interface Speed

The EPI Controller SDRAM interface can operate up to 50 MHz. The `COUNT0` field in the **EPIBAUD** register configures the speed of the EPI clock. For system clock (SysClk) speeds up to 50 MHz, the `COUNT0` field can be 0x0000, and the SDRAM interface can run at the same speed as SysClk. However, if SysClk is running at higher speeds, the bus interface can run only as fast as half speed, and the `COUNT0` field must be configured to at least 0x0001.

### 11.4.1.4 Non-Blocking Read Cycle

Figure 11-2 on page 350 shows a non-blocking read cycle of  $n$  halfwords;  $n$  can be any number greater than or equal to 1. The cycle begins with the Activate command and the row address on the `EPIOS[15:0]` signals. With the programmed CAS latency of 2, the Read command with the column address on the `EPIOS[15:0]` signals follows after 2 clock cycles. Following one more NOP cycle, data is read in on the `EPIOS[15:0]` signals on every rising clock edge. The Burst Terminate command is issued during the cycle when the next-to-last halfword is read in. The `DQMH` and `DQML` signals are deasserted after the last halfword of data is received; the `CSn` signal deasserts on the following clock cycle, signaling the end of the read cycle. At least one clock period of inactivity separates any two SDRAM cycles.

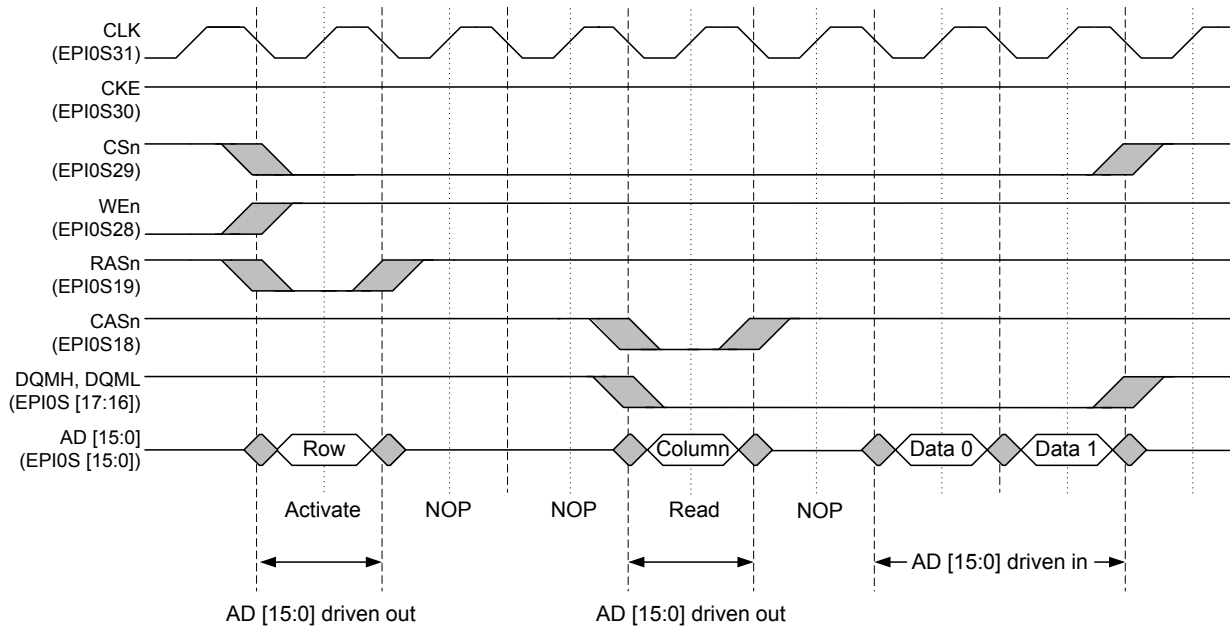
Figure 11-2. SDRAM Non-Blocking Read Cycle



### 11.4.1.5 Normal Read Cycle

Figure 11-3 on page 351 shows a normal read cycle of  $n$  halfwords;  $n$  can be 1 or 2. The cycle begins with the Activate command and the row address on the `EPIOS[15:0]` signals. With the programmed CAS latency of 2, the Read command with the column address on the `EPIOS[15:0]` signals follows after 2 clock cycles. Following one more NOP cycle, data is read in on the `EPIOS[15:0]` signals on every rising clock edge. The `DQMH`, `DQML`, and `CSn` signals are deasserted after the last halfword of data is received, signaling the end of the cycle. At least one clock period of inactivity separates any two SDRAM cycles.

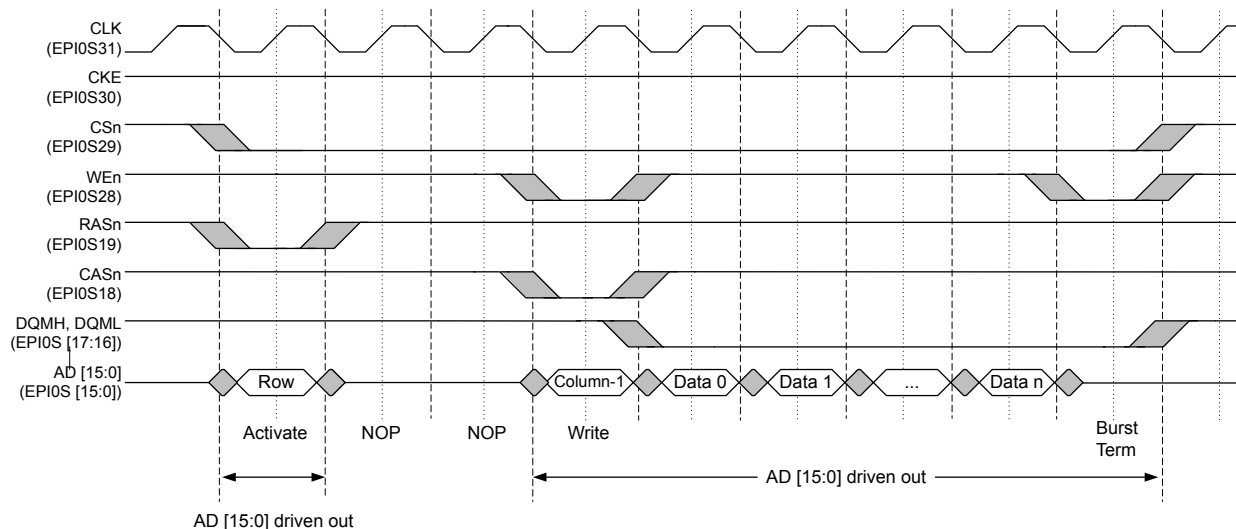
Figure 11-3. SDRAM Normal Read Cycle



#### 11.4.1.6 Write Cycle

Figure 11-4 on page 352 shows a write cycle of  $n$  halfwords;  $n$  can be any number greater than or equal to 1. The cycle begins with the Activate command and the row address on the  $EPIOS[15:0]$  signals. With the programmed CAS latency of 2, the Write command with the column address on the  $EPIOS[15:0]$  signals follows after 2 clock cycles. When writing to SDRAMs, the Write command is presented with the first halfword of data. Because the address lines and the data lines are multiplexed, the column address is modified to be (programmed address -1). During the Write command, the DQMH and DQML signals are high, so no data is written to the SDRAM. On the next clock, the DQMH and DQML signals are asserted, and the data associated with the programmed address is written. The Burst Terminate command occurs during the clock cycle following the write of the last halfword of data. The WEn, DQMH, DQML, and CSn signals are deasserted after the last halfword of data is received, signaling the end of the access. At least one clock period of inactivity separates any two SDRAM cycles.

Figure 11-4. SDRAM Write Cycle



## 11.4.2 Host Bus Mode

Host Bus supports the traditional 8-bit and 16-bit interfaces popularized by the 8051 devices and SRAM devices. This interface is asynchronous and uses strobe pins to control activity.

### 11.4.2.1 Control Pins

The main three strobes are ALE (Address latch enable), WRn (write), and RDn (sometimes called OEn, used for read). Note that the timings are designed for older logic and so are hold-time vs. setup-time specific. To ensure proper operation on this bus, the EPI block uses two system clocks per transition to allow significant skewing of control vs. data signals. So, for example, ALE rises one EPI clock before ADDR/DATA is asserted. Likewise, ALE falls (latch point) one EPI clock before DATA changes or tri-states. The same approach is used for the WRn and RDn/OEn strobes. The polarity of the read and write strobes can be active high or active low by clearing or setting the RDHIGH and WRHIGH bits in the **EPI Host-Bus n Configuration 2 (EPIHBnCFG2)** register.

The ALE can be changed to CSn through the **EPIHBnCFG2** register. The ALE is best used for Host-Bus muxed mode in which EPI address and data pins are shared. All Host-Bus accesses have an address phase followed by a data phase. The ALE indicates to an external latch to capture the address then hold it until the data phase. CSn is best used for Host-Bus unmuxed mode in which EPI address and data pins are separate. The CSn indicates when the address and data phases of a read or write access is occurring. Both the ALE and the CSn modes can be enhanced to access two external devices using settings in the **EPIHBnCFG2** register. Wait states can be added to the data phase of the access using the WRWS and RDWS bits in the **EPIHBnCFG2** register.

For FIFO mode, the ALE is not used, and two input holds are optionally supported to gate input and output to what the XFIFO can handle.

Host-Bus 8 and Host-Bus 16 modes are very configurable. The user has the ability to connect 1 or 2 external devices to the EPI signals as well as control whether byte select signals are provided in HB16 mode. These capabilities depend on the configuration of the MODE field in the **EPIHBnCFG** register, the CSCFG field in the **EPIHBnCFG2** register, and the BSEL bit in the **EPIHB16CFG** register. When BSEL=1, byte select signals are provided, so byte-sized data can be read and written at any address, however these signals reduce the available address width by 2 pins. When BSEL=0, byte reads and writes at odd addresses only act on the even byte, and byte writes at even addresses



write invalid values into the odd byte. As a result, accesses should be made as half-words (16-bits) or words (32-bits). In C/C++, programmers should use only short int and long int for accesses. Table 11-3 on page 353 shows the capabilities of the HB8 and HB16 modes as well as the available address bits with the possible combinations of these bits.

Although the `EPIOS31` signal can be configured for the EPI clock signal in Host-Bus mode, it is not required and should be configured as a GPIO to reduce EMI in the system.

**Table 11-3. Capabilities of Host Bus 8 and Host Bus 16 Modes**

Host Bus Type	MODE	CSCFG	Max # of External Devices	BSEL	Byte Access	Available Address
HB8	0x0	0x0, 0x1	1	N/A	Always	28 bits
HB8	0x0	0x2	2	N/A	Always	27 bits
HB8	0x0	0x3	2	N/A	Always	26 bits
HB8	0x1	0x0, 0x1	1	N/A	Always	20 bits
HB8	0x1	0x2	2	N/A	Always	19 bits
HB8	0x1	0x3	2	N/A	Always	18 bits
HB8	0x3	0x1	1	N/A	Always	none
HB8	0x3	0x3	2	N/A	Always	none
HB16	0x0	0x0, 0x1	1	0	No	28 bits
HB16	0x0	0x0, 0x1	1	1	Yes	26 bits
HB16	0x0	0x2	2	0	No	27 bits
HB16	0x0	0x2	2	1	Yes	25 bits
HB16	0x0	0x3	2	0	No	26 bits
HB16	0x0	0x3	2	1	Yes	24 bits
HB16	0x1	0x0, 0x1	1	0	No	12 bits
HB16	0x1	0x0, 0x1	1	1	Yes	10 bits
HB16	0x1	0x2	2	0	No	11 bits
HB16	0x1	0x2	2	1	Yes	9 bits
HB16	0x1	0x3	2	0	No	10 bits
HB16	0x1	0x3	2	1	Yes	8 bits
HB16	0x3	0x1	1	0	No	none
HB16	0x3	0x1	1	1	Yes	none
HB16	0x3	0x3	2	0	No	none
HB16	0x3	0x3	2	1	Yes	none

Table 11-4 on page 353 shows how the `EPI[31:0]` signals function while in Host-Bus 8 mode. Notice that the signal configuration changes based on the address/data mode selected by the `MODE` field in the `EPIHB8CFG2` register and on the chip select configuration selected by the `CSCFG` field in the same register. Any unused EPI controller signals can be used as GPIOs or another alternate function.

**Table 11-4. EPI Host-Bus 8 Signal Connections**

EPI Signal	CSCFG	HB8 Signal (MODE =ADMUX)	HB8 Signal (MODE =ADNOMUX (SRAM))	HB8 Signal (MODE =XFIFO)
EPIOS0	X <sup>a</sup>	AD0	D0	D0

Table 11-4. EPI Host-Bus 8 Signal Connections (continued)

EPI Signal	CSCFG	HB8 Signal (MODE =ADMUX)	HB8 Signal (MODE =ADNOMUX (SRAM))	HB8 Signal (MODE =XFIFO)
EPI0S1	X	AD1	D1	D1
EPI0S2	X	AD2	D2	D2
EPI0S3	X	AD3	D3	D3
EPI0S4	X	AD4	D4	D4
EPI0S5	X	AD5	D5	D5
EPI0S6	X	AD6	D6	D6
EPI0S7	X	AD7	D7	D7
EPI0S8	X	A8	A0	-
EPI0S9	X	A9	A1	-
EPI0S10	X	A10	A2	-
EPI0S11	X	A11	A3	-
EPI0S12	X	A12	A4	-
EPI0S13	X	A13	A5	-
EPI0S14	X	A14	A6	-
EPI0S15	X	A15	A7	-
EPI0S16	X	A16	A8	-
EPI0S17	X	A17	A9	-
EPI0S18	X	A18	A10	-
EPI0S19	X	A19	A11	-
EPI0S20	X	A20	A12	-
EPI0S21	X	A21	A13	-
EPI0S22	X	A22	A14	-
EPI0S23	X	A23	A15	-
EPI0S24	X	A24	A16	-
EPI0S25	0x0	A25 <sup>b</sup>	A17	-
	0x1			-
	0x2			CS1n
	0x3			-
EPI0S26	0x0	A26	A18	FEMPTY
	0x1			
	0x2			
	0x3	CS0n	CS0n	
EPI0S27	0x0	A27	A19	FFULL
	0x1			
	0x2	CSn1	CSn1	
	0x3			
EPI0S28	X	RDn/OEn	RDn/OEn	RDn
EPI0S29	X	WRn	WRn	WRn

**Table 11-4. EPI Host-Bus 8 Signal Connections (continued)**

EPI Signal	CSCFG	HB8 Signal (MODE =ADMUX)	HB8 Signal (MODE =ADNOMUX (SRAM))	HB8 Signal (MODE =XFIFO)
EPI0S30	0x0	ALE	ALE	-
	0x1	CSn	CSn	CSn
	0x2	CS0n	CS0n	CS0n
	0x3	ALE	ALE	-
EPI0S31	X	Clock <sup>c</sup>	Clock <sup>c</sup>	Clock <sup>c</sup>

a. "X" indicates the state of this field is a don't care.

b. When an entry straddles several row, the signal configuration is the same for all rows.

c. EPI0S31 should be configured as a GPIO. Clock function may not be supported in future revisions.

Table 11-5 on page 355 shows how the EPI[31:0] signals function while in Host-Bus 16 mode. Notice that the signal configuration changes based on the address/data mode selected by the MODE field in the EPIHB16CFG2 register, on the chip select configuration selected by the CSCFG field in the same register, and on whether byte selects are used as configured by the BSEL bit in the EPIHB16CFG register. Any unused EPI controller signals can be used as GPIOs or another alternate function.

**Table 11-5. EPI Host-Bus 16 Signal Connections**

EPI Signal	CSCFG	BSEL	HB16 Signal (MODE =ADMUX)	HB16 Signal (MODE =ADNOMUX (SRAM))	HB16 Signal (MODE =XFIFO)
EPI0S0	X <sup>a</sup>	X	AD0	D0	D0
EPI0S1	X	X	AD1	D1	D1
EPI0S2	X	X	AD2	D2	D2
EPI0S3	X	X	AD3	D3	D3
EPI0S4	X	X	AD4	D4	D4
EPI0S5	X	X	AD5	D5	D5
EPI0S6	X	X	AD6	D6	D6
EPI0S7	X	X	AD7	D7	D7
EPI0S8	X	X	AD8	D8	D8
EPI0S9	X	X	AD9	D9	D9
EPI0S10	X	X	AD10	D10	D10
EPI0S11	X	X	AD11	D11	D11
EPI0S12	X	X	AD12	D12	D12
EPI0S13	X	X	AD13	D13	D13
EPI0S14	X	X	AD14	D14	D14
EPI0S15	X	X	AD15	D15	D15
EPI0S16	X	X	A16	A0 <sup>b</sup>	-
EPI0S17	X	X	A17	A1	-
EPI0S18	X	X	A18	A2	-
EPI0S19	X	X	A19	A3	-
EPI0S20	X	X	A20	A4	-
EPI0S21	X	X	A21	A5	-
EPI0S22	X	X	A22	A6	-

Table 11-5. EPI Host-Bus 16 Signal Connections (continued)

EPI Signal	CSCFG	BSEL	HB16 Signal (MODE =ADMUX)	HB16 Signal (MODE =ADNOMUX (SRAM))	HB16 Signal (MODE =XFIFO)		
EPI0S23	X <sup>c</sup>	0	A23	A7	-		
		1			BSEL0n		
EPI0S24	0x0	0	A24	A8	-		
		1			BSEL1n		
	0x1	0			-		
		1			BSEL1n		
	0x2	0			-		
		1			BSEL1n		
	0x3	0			-		
		1			BSEL0n	BSEL0n	BSEL1n
EPI0S25	0x0	X	A25	A9	-		
			0x2	0	A25	A9	CS1n
	1	BSEL0n		BSEL0n			
	0x3	0	A25	A9	--		
			1	BSEL1n		BSEL1n	
	EPI0S26	0x0	0	A26	A10	FEMPTY	
1			BSEL0n	BSEL0n			
0x1		0	A26	A10			
		1	BSEL0n	BSEL0n			
0x2		0	A26	A10			
		1	BSEL1n	BSEL1n			
0x3		X	CS0n	CS0n			
EPI0S27	0x0	0	A27	A11	FFULL		
		1	BSEL1n	BSEL1n			
	0x1	0	A27	A11			
		1	BSEL1n	BSEL1n			
	0x2	X	CS1n	CS1n			
						0x3	X
	EPI0S28	X	X	RDn/OEn			
	EPI0S29	X	X	WRn		WRn	WRn
EPI0S30	0x0	X	ALE	ALE	-		
	0x1	X	CSn	CSn	CSn		
	0x2	X	CS0n	CS0n	CS0n		
	0x3	X	ALE	ALE	-		
EPI0S31	X	X	Clock <sup>d</sup>	Clock <sup>d</sup>	Clock <sup>d</sup>		

a. "X" indicates the state of this field is a don't care.

b. In this mode, half-word accesses are used. AO is the LSB of the address and is equivalent to the system A1 address.

c. When an entry straddles several row, the signal configuration is the same for all rows.

d. EPI0S31 should be configured as a GPIO. Clock function may not be supported in future revisions.

### 11.4.2.2 Speed of Transactions

The `COUNT0` field in the **EPIBAUD** register must be configured to set the main transaction rate based on what the slave device can support (including wiring considerations). The main control transitions are normally  $\frac{1}{2}$  the baud rate (`COUNT0 = 1`) because the EPI block forces data vs. control to change on alternating clocks. When using dual chip-selects, each chip select can access the bus using differing baud rates by setting the `CSBAUD` bit in the **EPIHBnCFG2** register. In this case, the `COUNT0` field controls the `CS0n` transactions, and the `COUNT1` field controls the `CS1n` transactions.

Additionally, the Host-Bus mode provides read and write wait states for the data portion to support different classes of device. These wait states stretch the data period (hold the rising edge of data strobe) and may be used in all four sub-modes. The wait states are set using the `WRWS` and `RDWS` bits in the **EPI Host-Bus n Configuration (EPIHBnCFG)** register.

### 11.4.2.3 Sub-Modes of Host Bus 8/16

The EPI controller supports four variants of the Host-Bus model using 8 or 16 bits of data in all four cases. The four sub-modes are selected using the `MODE` bits in the **EPIHBnCFG** register, and are:

1. Address and data are muxed. This scheme is used by many 8051 devices, some Microchip PIC parts, and some ATmega parts. When used for standard SRAMs, a latch must be used between the microcontroller and the SRAM. This sub-mode is provided for compatibility with existing devices that support data transfers without a latch (for example, LCD controllers or CPLDs). In general, the de-muxed sub-mode should normally be used. The ALE configuration should be used in this mode, as all Host-Bus accesses have an address phase followed by a data phase. The ALE indicates to an external latch to capture the address then hold until the data phase. The ALE configuration is controlled by configuring the `CSCFG` field to be `0x0` in the **EPIHBnCFG2** register. The ALE can be enhanced to access two external devices with the addition of two separate `CSn` signals. By configuring the `CSCFG` field in the to be `0x3` in the **EPIHBnCFG2** register, `EPI0S30` functions as ALE, `EPI0S27` functions as `CS1n`, and `EPI0S26` functions as `CS0n`. The `CSn` is best used for Host-Bus unmuxed mode which EPI address and data pins are separate. The `CSn` indicates when the address and data phases of a read or write access are occurring.
2. Address and data are separate with 8 or 16 bits of data and up to 20 bits of address (1 MB). This scheme is used by more modern 8051 devices, as well as some PIC and ATmega parts. This mode is generally used with real SRAMs, many EEPROMs, and many NOR Flash memory devices. Note that there is no hardware command write support for Flash memory devices; this mode should only be used for Flash memory devices programmed at manufacturing time. If a Flash memory device must be written and does not support a direct programming model, the command mechanism must be performed in software. The `CSn` configuration should be used in this mode. The `CSn` signal indicates when the address and data phases of a read or write access is occurring. The `CSn` configuration is controlled by configuring the `CSCFG` field to be `0x1` in the **EPIHBnCFG2** register. The `CSn` configuration can be enhanced to access two external devices via separate `CSn`. By configuring the `CSCFG` field to be `0x2`, `EPI0S30` functions as `CS0n` and `EPI0S27` functions as `CS1n`.
3. SRAM fast mode where address and data are separate. This sub-mode is used for real SRAMs which can be read more quickly by only changing the address (and not using `RDn/OEn` strobing). In this sub-mode, reads are performed by keeping the read mode selected (output enable is asserted) and then changing the address pins. The data pins are changed by the SRAM after the address pins change. For example, to read data from address `0x100` and then `0x101`, the EPI controller asserts the output-enable signal and then configures the address pins to `0x100`; the EPI controller then captures what is on the data pins and increments `A0` to 1 (so the address

is now 0x101); the EPI controller then captures what is on the data pins. Note that this mode consumes higher power because the SRAM must continuously drive the data pins. This mode is not practical in HB16 mode for normal SRAMs because there are generally not enough address bits available.

4. FIFO mode uses 8 or 16 bits of data, removes ALE and address pins and optionally adds external XFIFO FULL/EMPTY flag inputs. This scheme is used by many devices, such as radios, communication devices (including USB2 devices), and some FPGA configurations (FIFO through block RAM). This sub-mode provides the data side of the normal Host-Bus interface, but is paced by the FIFO control signals. It is important to consider that the XFIFO FULL/EMPTY control signals may stall the interface and could have an impact on blocking read latency from the processor or  $\mu$ DMA.

The `WORD` bit in the **EPIHBnCFG2** register can be set to use memory more efficiently. By default, the EPI controller uses data bits [7:0] for Host-Bus 8 accesses or bits [15:0] for Host-Bus 16 accesses. When the `WORD` bit is set, the EPI controller can automatically route bytes of data onto the correct byte lanes such that data can be stored in bits [31:8] (HB8) or [31:16] (HB16). In addition, for the three modes above (1, 2, 4) that the Host-Bus 16 mode supports, byte select signals can be optionally implemented by setting the `BSEL` bit in the **EPIHB16CFG** register.

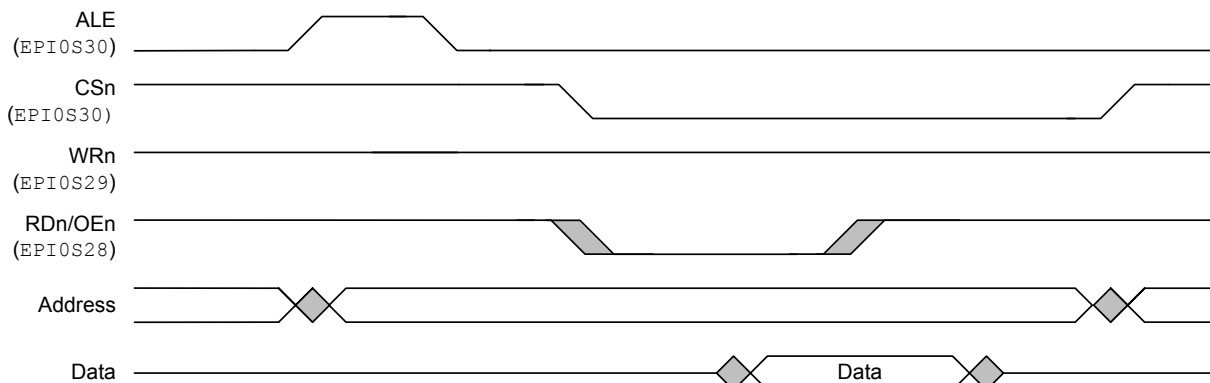
See “External Peripheral Interface (EPI)” on page 736 for timing details for the Host-Bus mode.

#### 11.4.2.4 Bus Operation

Bus operation is the same in Host-Bus 8 and Host-Bus 16 modes and is asynchronous. Timing diagrams show both ALE and CSn operation, but only one signal or the other is used in all modes except for ALE with dual chip selects mode (`CSCFG` field is 0x3 in the **EPIHBnCFG2** register). Address and data on write cycles are held after the CSn signal is deasserted. The optional HB16 byte select signals have the same timing as the address signals. If wait states are required in the bus access, they can be inserted during the data phase of the access using the `WRWS` and `RDWS` bits in the **EPIHBnCFG2** register. Each wait state adds 2 EPI clock cycles to the duration of the `WRn` or `RDn` strobe.

Figure 11-5 on page 358 shows a basic Host-Bus read cycle. Figure 11-6 on page 359 shows a basic Host-Bus write cycle. Both of these figures show address and data signals in the non-multiplexed mode (`MODE` field is 0x1 in the **EPIHBnCFG** register).

**Figure 11-5. Host-Bus Read Cycle, MODE = 0x1, WRHIGH = 1, RDHIGH = 1**



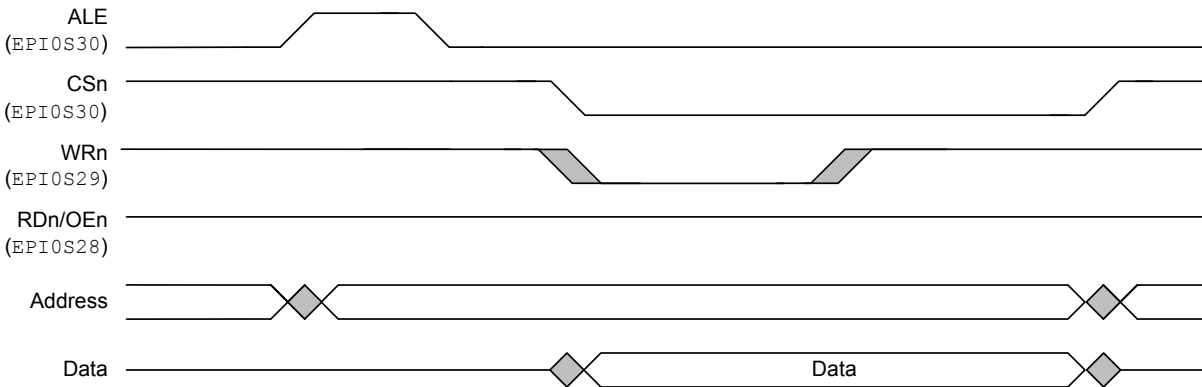
**Figure 11-6. Host-Bus Write Cycle, MODE = 0x1, WRHIGH = 1, RDHIGH = 1**

Figure 11-7 on page 359 shows a write cycle with the address and data signals multiplexed (MODE field is 0x0 in the **EPIHBnCFG** register). A read cycle would look similar, with the RDn strobe being asserted along with CSn and data being latched on the rising edge of RDn.

**Figure 11-7. Host-Bus Write Cycle with Multiplexed Address and Data, MODE = 0x0, WRHIGH = 1, RDHIGH = 1**

FIFO mode accesses are the same as normal read and write accesses, except that the ALE signal and address pins are not present. Two input signals can be used to indicate when the XFIFO is full or empty to gate transactions and avoid overruns and underruns. The FFULL and FEMPTY signals are synchronized and must be recognized as asserted by the microcontroller for 2 system clocks before they affect transaction status. The MAXWAIT field in the **EPIHBnCFG** register defines the maximum number of EPI clocks to wait while the FEMPTY or FFULL signal is holding off a transaction. Figure 11-8 on page 360 shows how the FEMPTY signal should respond to a write and read from the XFIFO. Figure 11-9 on page 360 shows how the FEMPTY and FFULL signals should respond to 2 writes and 1 read from an external FIFO that contains two entries.

Figure 11-8. Write Followed by Read to External FIFO

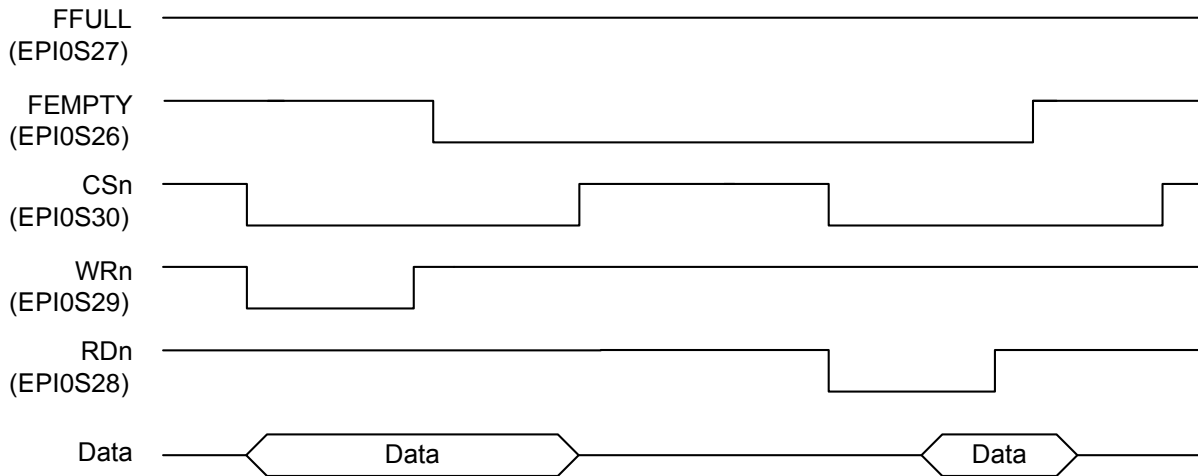
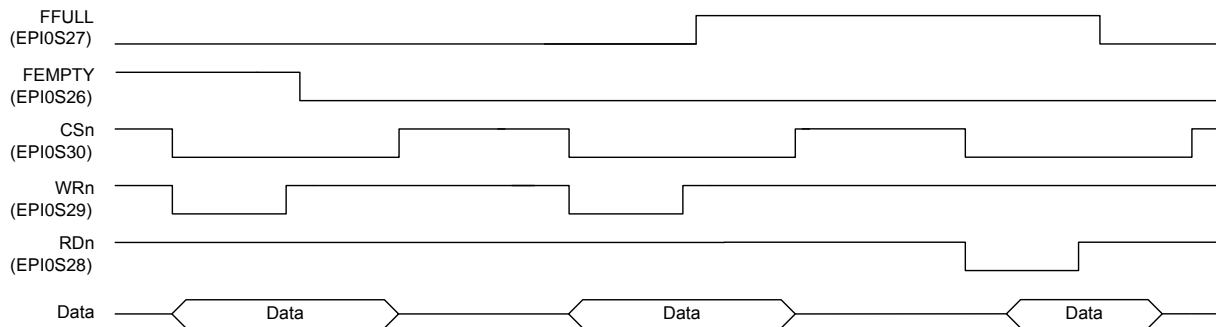


Figure 11-9. Two-Entry FIFO



### 11.4.3 General-Purpose Mode

The **General-Purpose Mode Configuration (EPIGPCFG)** register is used to configure the control, data, and address pins, if used. Any unused EPI controller signals can be used as GPIOs or another alternate function. The general-purpose configuration can be used for custom interfaces with FPGAs, CPLDs, and digital data acquisition and actuator control.

**Important:** The **RD2CYC** bit in the **EPIGPCFG** register must be set at all times in General-Purpose mode to ensure proper operation.

General-Purpose mode is designed for three general types of use:

- Extremely high-speed clocked interfaces to FPGAs and CPLDs. Three sizes of data and optional address are supported. Framing and clock-enable functions permit more optimized interfaces.
- General parallel GPIO. From 1 to 32 pins may be written or read, with the speed precisely controlled by the **EPIBAUD** register baud rate (when used with the **WFIFO** and/or the **NBRFIFO**) or by the rate of accesses from software or  $\mu$ DMA. Examples of this type of use include:
  - Reading 20 sensors at fixed time periods by configuring 20 pins to be inputs, configuring the **COUNT0** field in the **EPIBAUD** register to some divider, and then using non-blocking reads.



- Implementing a very wide ganged PWM/PCM with fixed frequency for driving actuators, LEDs, etc.
- Implementing SDIO 4-bit mode where commands are driven or captured on 6 pins with fixed timing, fed by the  $\mu$ DMA.
- General custom interfaces of any speed.

The configuration allows for choice of an output clock (free-running or gated), a framing signal (with frame size), a ready input (to stretch transactions), a read and write strobe, an address (of varying sizes), and data (of varying sizes). Additionally, provisions are made for separating data and address phases.

The interface has the following optional features:

- Use of the EPI clock output is controlled by the `CLKPIN` bit in the **EPIGPCFG** register. Unlocked uses include general-purpose I/O and asynchronous interfaces (optionally using RD and WR strobes). Clocked interfaces allow for higher speeds and are much easier to connect to FPGAs and CPLDs (which usually include input clocks).
- EPI clock, if used, may be free running or gated depending on the `CLKGATE` bit in the **EPIGPCFG** register. A free-running EPI clock requires another method for determining when data is live, such as the frame pin or RD/WR strobes. A gated clock approach uses a setup-time model in which the EPI clock controls when transactions are starting and stopping. The gated clock is held high until a new transaction is started and goes high at the end of the cycle where RD/WR/FRAME and address (and data if write) are emitted.
- Use of the ready input (iRDY) from the external device is controlled by the `RDYEN` bit in the **EPIGPCFG** register. The iRDY signal uses `EPIOS27` and may only be used with a free-running clock. iRDY gates transactions, no matter what state they are in. When iRDY is deasserted, the transaction is held off from completing.
- Use of the frame output (FRAME) is controlled by the `FRMPIN` bit in the **EPIGPCFG** register. The frame pin may be used whether the clock is output or not, and whether the clock is free running or not. It may also be used along with the iRDY signal. The frame may be a pulse (one clock) or may be 50/50 split across the frame size (controlled by the `FRM50` bit in the **EPIGPCFG** register). The frame count (the size of the frame as specified by the `FRMCNT` field in the **EPIGPCFG** register) may be between 1 and 15 clocks for pulsed and between 2 and 30 clocks for 50/50. The frame pin counts transactions and not clocks; a transaction is any clock where the RD or WR strobe is high (if used). So, if the `FRMCNT` bit is set, then the frame pin pulses every other transaction; if 2-cycle reads and writes are used, it pulses every other address phase. `FRM50` must be used with this in mind as it may hold state for many clocks waiting for the next transaction.
- Use of the RD and WR outputs is controlled by the `RW` bit in the **EPIGPCFG** register. For interfaces where the direction is known (in advance, related to frame size, or other means), these strobes are not needed. For most other interfaces, RD and WR are used so the external peripheral knows what transaction is taking place, and if any transaction is taking place.
- Separation of address/request and data phases may be used on writes using the `WR2CYC` bit in the **EPIGPCFG** register. This configuration allows the external peripheral extra time to act. Address and data phases must be separated on reads, and the `RD2CYC` bit in the **EPIGPCFG** register must be set. When configured to use an address as specified by the `ASIZE` field in the **EPIGPCFG** register, the address is emitted on the with the RD strobe (first cycle) and data is

expected to be returned on the next cycle (when RD is not asserted). If no address is used, then RD is asserted on the first cycle and data is captured on the second cycle (when RD is not asserted), allowing more setup time for data.

For writes, the output may be in one or two cycles. In the two-cycle case, the address (if any) is emitted on the first cycle with the WR strobe and the data is emitted on the second cycle (with WR not asserted). Although split address and write data phases are not normally needed for logic reasons, it may be useful to make read and write timings match. If 2-cycle reads or writes are used, the RW bit is automatically set.

- Address may be emitted (controlled by the ASIZE field in the **EPIGPCFG** register). The address may be up to 4 bits (16 possible values), up to 12 bits (4096 possible values), or up to 20 bits (1 M possible values). Size of address limits size of data, for example, 4 bits of address support up to 24 bits data. Address comes from the bottom address bits (the bits on the EPI signals that are immediately following the data bits) used for the transaction by the processor or  $\mu$ DMA. The address signals may be used by the external peripheral as an address, code (command), or for other unrelated uses (such as a chip enable).
- Data may be 8 bits, 16 bits, 24 bits, or 32 bits (controlled by the DSIZE field in the **EPIGPCFG** register). 32-bit data cannot be used with address or EPI clock or any other signal. 24-bit data can only be used with 4-bit address or no address. 32-bit data requires that either the WR2CYC bit or the RD2CYC bit in the **EPIGPCFG** register is set.
- Memory can be used more efficiently by using the Word Access Mode. By default, the EPI controller uses data bits [7:0] when the DSIZE field in the **EPIGPCFG** register is 0x0; data bits [15:0] when the DSIZE field is 0x1; data bits [23:0] when the DSIZE field is 0x2; and data bits [31:0] when the DSIZE field is 0x3. When the WORD bit in the **EPIGPCFG2** register is set, the EPI controller automatically routes bytes of data onto the correct byte lanes such that data can be stored in bits [31:8] for DSIZE=0x0 and bits [31:16] for DSIZE=0x1.
- When using the EPI controller as a GPIO interface, writes are FIFOed (up to 4 can be held at any time), and up to 32 pins are changed using the **EPIBAUD** clock rate specified by COUNT0. As a result, output pin control can be very precisely controlled as a function of time. By contrast, when writing to normal GPIOs, writes can only occur 8-bits at a time and take up to two clock cycles to complete. In addition, the write itself may be further delayed by the bus due to draining of a previous write. With both GPIO and the EPI controller, reads may be performed directly, in which case the current pin states are read back. With the EPI controller, the non-blocking interface may also be used to perform reads based on a fixed time rule via the **EPIBAUD** clock rate.

Table 11-6 on page 362 shows how the EPIOS[31:0] signals function while in General-Purpose mode. Notice that the address connections vary depending on the data-width restrictions of the external peripheral.

**Table 11-6. EPI General Purpose Signal Connections**

EPI Signal	General-Purpose Signal (D8, A20)	General- Purpose Signal (D16, A12)	General- Purpose Signal (D24, A4)	General- Purpose Signal (D32)
EPIOS0	D0	D0	D0	D0
EPIOS1	D1	D1	D1	D1
EPIOS2	D2	D2	D2	D2
EPIOS3	D3	D3	D3	D3
EPIOS4	D4	D4	D4	D4
EPIOS5	D5	D5	D5	D5

Table 11-6. EPI General Purpose Signal Connections (*continued*)

EPI Signal	General-Purpose Signal (D8, A20)	General- Purpose Signal (D16, A12)	General- Purpose Signal (D24, A4)	General- Purpose Signal (D32)
EPI0S6	D6	D6	D6	D6
EPI0S7	D7	D7	D7	D7
EPI0S8	A0	D8	D8	D8
EPI0S9	A1	D9	D9	D9
EPI0S10	A2	D10	D10	D10
EPI0S11	A3	D11	D11	D11
EPI0S12	A4	D12	D12	D12
EPI0S13	A5	D13	D13	D13
EPI0S14	A6	D14	D14	D14
EPI0S15	A7	D15	D15	D15
EPI0S16	A8	A0 <sup>a</sup>	D16	D16
EPI0S17	A9	A1	D17	D17
EPI0S18	A10	A2	D18	D18
EPI0S19	A11	A3	D19	D19
EPI0S20	A12	A4	D20	D20
EPI0S21	A13	A5	D21	D21
EPI0S22	A14	A6	D22	D22
EPI0S23	A15	A7	D23	D23
EPI0S24	A16	A8	A0 <sup>b</sup>	D24
EPI0S25	A17	A9	A1	D25
EPI0S26	A18	A10	A2	D26
EPI0S27	A19/iRDY <sup>c</sup>	A11/iRDY <sup>c</sup>	A3/iRDY <sup>c</sup>	D27
EPI0S28	WR	WR	WR	D28
EPI0S29	RD	RD	RD	D29
EPI0S30	Frame	Frame	Frame	D30
EPI0S31	Clock	Clock	Clock	D31

a. In this mode, half-word accesses are used. A0 is the LSB of the address and is equivalent to the system A1 address.

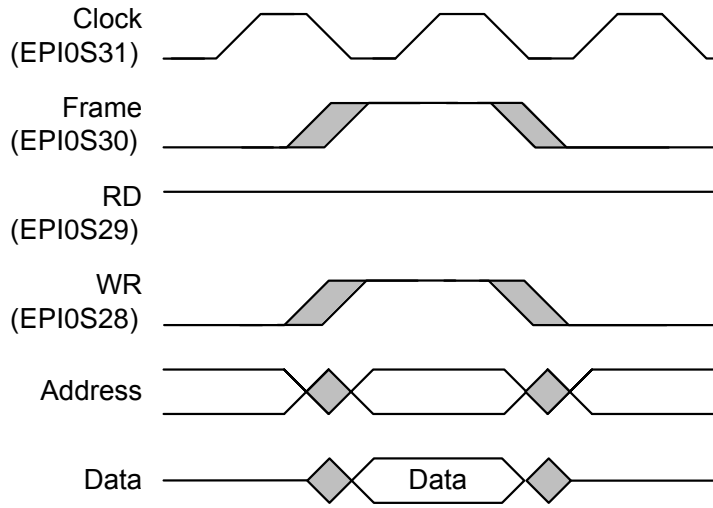
b. In this mode, word accesses are used. A0 is the LSB of the address and is equivalent to the system A2 address.

c. This signal is iRDY if the `RDYEN` bit in the `EPIGPCFG` register is set.

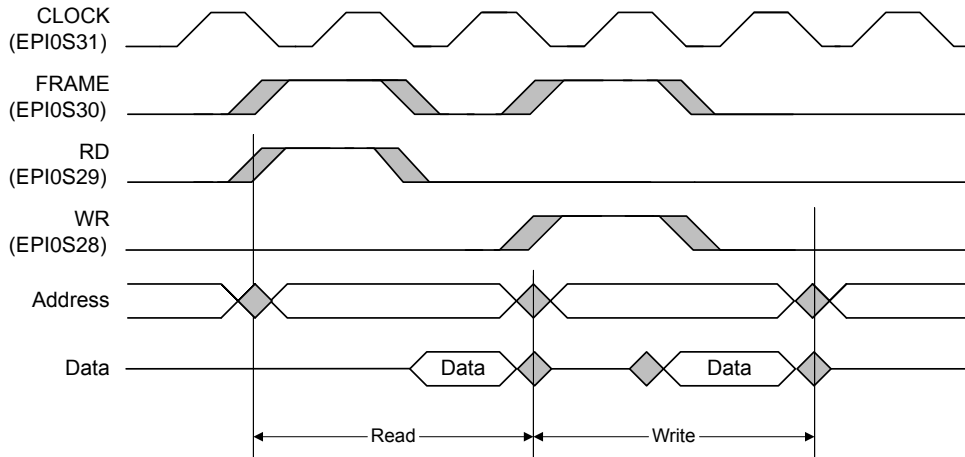
### 11.4.3.1 Bus Operation

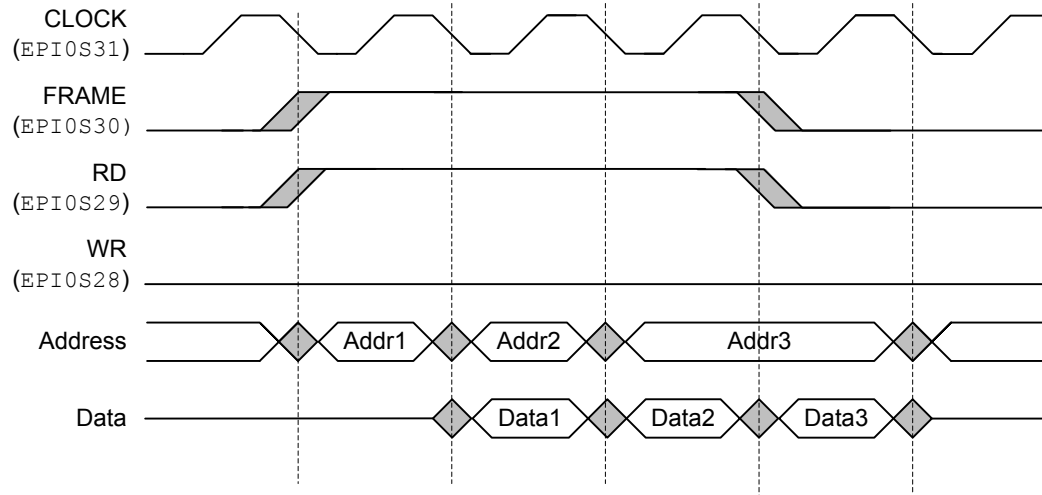
A basic access is 1 EPI clock for write cycles and 2 EPI clocks for read cycles. An additional EPI clock can be inserted into a write cycle by setting the `WR2CYC` bit in the `EPIGPCFG` register. Note that the `RD2CYC` bit must always be set in the `EPIGPCFG` register. If the iRDY signal is deasserted, further transactions are held off until the iRDY signal is asserted again.

**Figure 11-10. Single-Cycle Write Access, FRM50=0, FRMCNT=0, WRCYC=0**

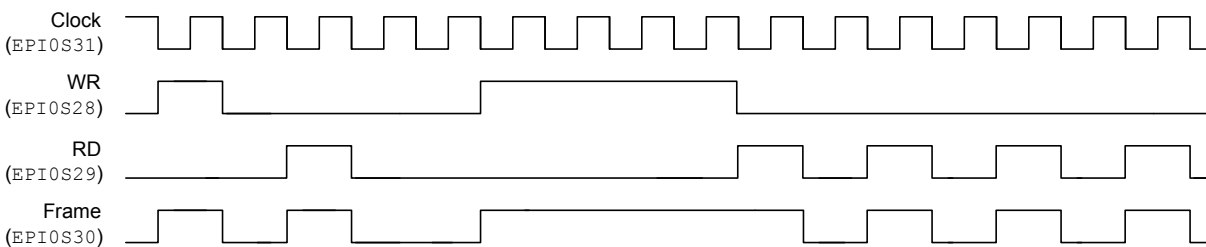


**Figure 11-11. Two-Cycle Read, Write Accesses, FRM50=0, FRMCNT=0, RDCYC=1, WRCYC=1**

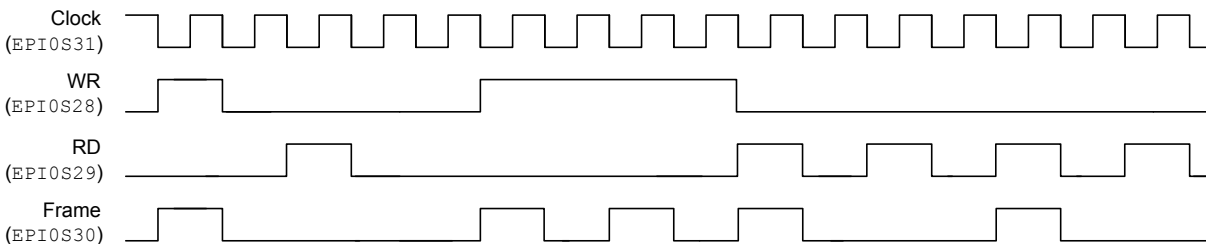


**Figure 11-12. Read Accesses, FRM50=0, FRMCNT=0, RDCYC=1****FRAME Signal Operation**

The operation of the FRAME signal is controlled by the FRMCNT and FRM50 bits. When FRM50 is clear, the FRAME signal is high whenever the WR or RD strobe is high. When FRMCNT is clear, the FRAME signal is simply the logical OR of the WR and RD strobes so the FRAME signal is high during every read or write access, see Figure 11-13 on page 365.

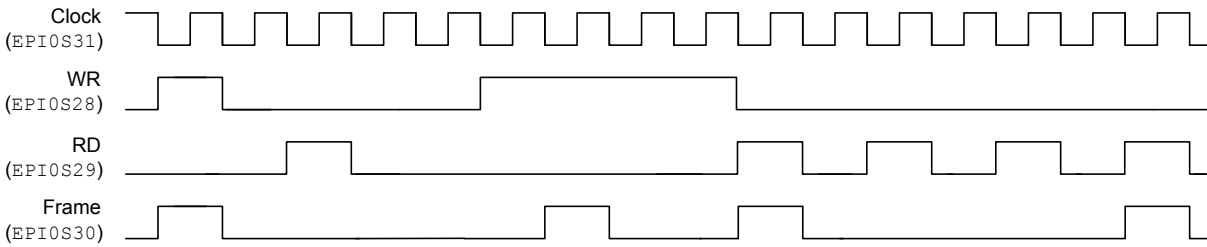
**Figure 11-13. FRAME Signal Operation, FRM50=0 and FRMCNT=0**

If the FRMCNT field is 0x1, then the FRAME signal pulses high during every other read or write access, see Figure 11-14 on page 365.

**Figure 11-14. FRAME Signal Operation, FRM50=0 and FRMCNT=1**

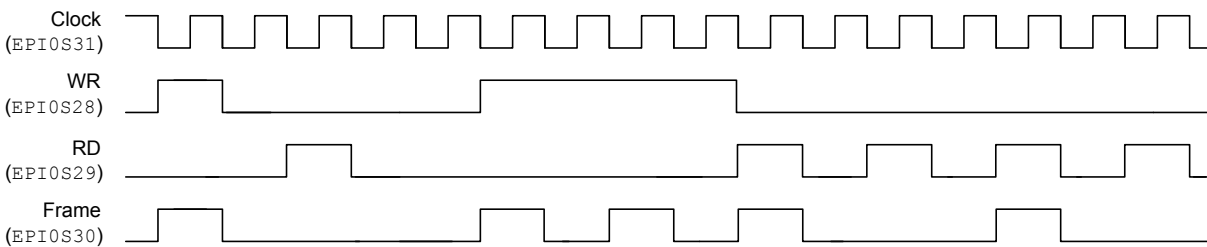
If the FRMCNT field is 0x2 and FRM50 is clear, then the FRAME signal pulses high during every third access, and so on for every value of FRMCNT, see Figure 11-15 on page 366.

**Figure 11-15. FRAME Signal Operation, FRM50=0 and FRMCNT=2**



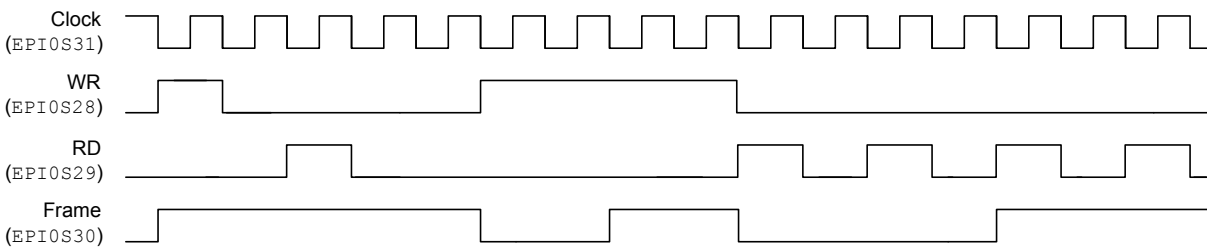
When  $FRM50$  is set, the FRAME signal transitions on the rising edge of either the WR or RD strobes. When  $FRMCNT=0$ , the FRAME signal transitions on the rising edge of WR or RD for every access, see Figure 11-16 on page 366.

**Figure 11-16. FRAME Signal Operation, FRM50=1 and FRMCNT=0**



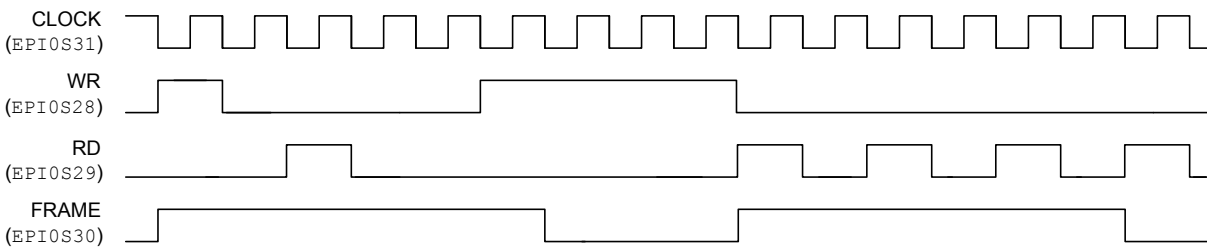
When  $FRMCNT=1$ , the FRAME signal transitions on the rising edge of the WR or RD strobes for every other access, see Figure 11-17 on page 366.

**Figure 11-17. FRAME Signal Operation, FRM50=1 and FRMCNT=1**



When  $FRMCNT=2$ , the FRAME signal transitions the rising edge of the WR or RD strobes for every third access, and so on for every value of  $FRMCNT$ , see Figure 11-18 on page 366.

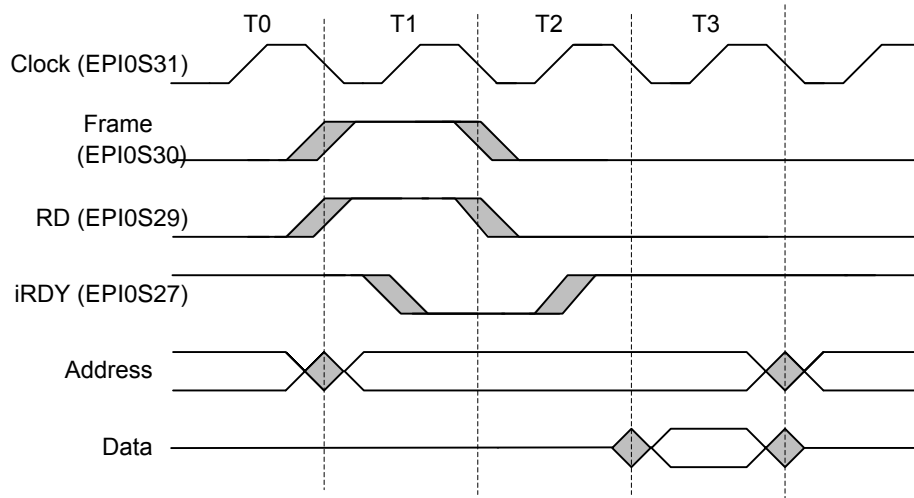
**Figure 11-18. FRAME Signal Operation, FRM50=1 and FRMCNT=2**



### iRDY Signal Operation

The ready input (iRDY) from the external device is enabled by the `RDYEN` bit in the `EPIGPCFG` register. iRDY is input on `EPIOS27` and may only be used with a free-running clock (`CLKGATE` is clear). iRDY is sampled on the falling edge of the EPI clock and gates transactions, no matter what state they are in. Figure 11-19 on page 367 shows the iRDY signal being recognized as deasserted on the falling edge of T1. The `FRAME`, `RD`, Address, Data signals behave as they would during a normal transaction in T1. T2 is the frozen state, and signals are held in this state until iRDY is recognized as asserted again. At the falling edge of T2, when iRDY is asserted again, the cycle continues and completes in T3.

**Figure 11-19. iRDY Signal Operation, `FRM50=0`, `FRMCNT=0`, and `RD2CYC=1`**



### EPI Clock Operation

If the `CLKGATE` bit in the `EPIGPCFG` register is clear, the EPI clock always toggles when General-purpose mode is enabled. If `CLKGATE` is set, the clock is output only when a transaction is occurring, otherwise the clock is held high. If the `WR2CYC` bit is clear, the EPI clock begins toggling 1 cycle before the `WR` strobe goes high. If the `WR2CYC` bit is set, the EPI clock begins toggling when the `WR` strobe goes high. The clock stops toggling after the first rising edge after the `WR` strobe is deasserted. The `RD` strobe operates in the same manner as the `WR` strobe when the `WR2CYC` bit is set, as the `RD2CYC` bit must always be set. See Figure 11-20 on page 367 and Figure 11-21 on page 368.

**Figure 11-20. EPI Clock Operation, `CLKGATE=1`, `WR2CYC=0`**

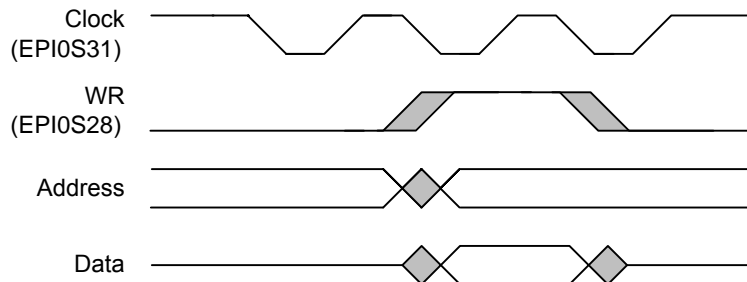
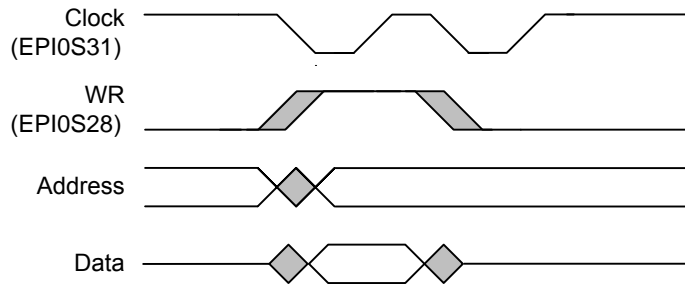


Figure 11-21. EPI Clock Operation, CLKGATE=1, WR2CYC=1



## 11.5 Register Map

Table 11-7 on page 368 lists the EPI registers. The offset listed is a hexadecimal increment to the register's address, relative to the base address of 0x400D.0000. Note that the EPI controller clock must be enabled before the registers can be programmed (see page 149).

**Note:** A back-to-back write followed by a read of the same register reads the value that written by the first write access, not the value from the second write access. (This situation only occurs when the processor core attempts this action, the  $\mu$ DMA does not do this.). To read back what was just written, another instruction must be generated between the write and read. Read-write does not have this issue, so use of read-write for clear of error interrupt cause is not affected.

Table 11-7. External Peripheral Interface (EPI) Register Map

Offset	Name	Type	Reset	Description	See page
0x000	EPICFG	R/W	0x0000.0000	EPI Configuration	370
0x004	EPIBAUD	R/W	0x0000.0000	EPI Main Baud Rate	371
0x010	EPISDRAMCFG	R/W	0x42EE.0000	EPI SDRAM Configuration	373
0x010	EPIHB8CFG	R/W	0x0000.FF00	EPI Host-Bus 8 Configuration	375
0x010	EPIHB16CFG	R/W	0x0000.FF00	EPI Host-Bus 16 Configuration	378
0x010	EPIGPCFG	R/W	0x0000.FF00	EPI General-Purpose Configuration	382
0x014	EPIHB8CFG2	R/W	0x0000.0000	EPI Host-Bus 8 Configuration 2	386
0x014	EPIHB16CFG2	R/W	0x0000.0000	EPI Host-Bus 16 Configuration 2	388
0x014	EPIGPCFG2	R/W	0x0000.0000	EPI General-Purpose Configuration 2	390
0x01C	EPIADDRMAP	R/W	0x0000.0000	EPI Address Map	391
0x020	EPIRSIZE0	R/W	0x0000.0003	EPI Read Size 0	393
0x024	EPIRADDR0	R/W	0x0000.0000	EPI Read Address 0	394
0x028	EPIRPSTD0	R/W	0x0000.0000	EPI Non-Blocking Read Data 0	395
0x030	EPIRSIZE1	R/W	0x0000.0003	EPI Read Size 1	393
0x034	EPIRADDR1	R/W	0x0000.0000	EPI Read Address 1	394
0x038	EPIRPSTD1	R/W	0x0000.0000	EPI Non-Blocking Read Data 1	395



Table 11-7. External Peripheral Interface (EPI) Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0x060	EPISTAT	RO	0x0000.0000	EPI Status	397
0x06C	EPIRFIFOCNT	RO	-	EPI Read FIFO Count	399
0x070	EPIREADFIFO	RO	-	EPI Read FIFO	400
0x074	EPIREADFIFO1	RO	-	EPI Read FIFO Alias 1	400
0x078	EPIREADFIFO2	RO	-	EPI Read FIFO Alias 2	400
0x07C	EPIREADFIFO3	RO	-	EPI Read FIFO Alias 3	400
0x080	EPIREADFIFO4	RO	-	EPI Read FIFO Alias 4	400
0x084	EPIREADFIFO5	RO	-	EPI Read FIFO Alias 5	400
0x088	EPIREADFIFO6	RO	-	EPI Read FIFO Alias 6	400
0x08C	EPIREADFIFO7	RO	-	EPI Read FIFO Alias 7	400
0x200	EPIFIFOLVL	R/W	0x0000.0033	EPI FIFO Level Selects	401
0x204	EPIWFIFOCNT	RO	0x0000.0000	EPI Write FIFO Count	403
0x210	EPIIM	R/W	0x0000.0000	EPI Interrupt Mask	404
0x214	EPIRIS	RO	0x0000.0000	EPI Raw Interrupt Status	405
0x218	EPIMIS	RO	0x0000.0000	EPI Masked Interrupt Status	407
0x21C	EPIEISC	R/W1C	0x0000.0000	EPI Error Interrupt Status and Clear	408

## 11.6 Register Descriptions

This section lists and describes the EPI registers, in numerical order by address offset.

## Register 1: EPI Configuration (EPICFG), offset 0x000

**Important:** The `MODE` field determines which configuration register is accessed for offsets 0x010 and 0x014. Any write to the `EPICFG` register resets the register contents at offsets 0x010 and 0x014.

The configuration register is used to enable the block, select a mode, and select the basic pin use (based on the mode). Note that attempting to program an undefined `MODE` field clears the `BLKEN` bit and disables the EPI controller.

### EPI Configuration (EPICFG)

Base 0x400D.0000  
 Offset 0x000  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												BLKEN	MODE			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description																				
31:5	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																				
4	BLKEN	R/W	0	Block Enable																				
				<table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>1</td> <td>The EPI controller is enabled.</td> </tr> <tr> <td>0</td> <td>The EPI controller is disabled.</td> </tr> </table>	Value	Description	1	The EPI controller is enabled.	0	The EPI controller is disabled.														
Value	Description																							
1	The EPI controller is enabled.																							
0	The EPI controller is disabled.																							
3:0	MODE	R/W	0x0	Mode Select																				
				<table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>0x0</td> <td>General Purpose</td> </tr> <tr> <td></td> <td>General-Purpose mode. Control, address, and data pins are configured using the <code>EPIGPCFG</code> and <code>EPIGPCFG2</code> registers.</td> </tr> <tr> <td>0x1</td> <td>SDRAM</td> </tr> <tr> <td></td> <td>Supports SDR SDRAM. Control, address, and data pins are configured using the <code>EPISDRAMCFG</code> register.</td> </tr> <tr> <td>0x2</td> <td>8-Bit Host-Bus (HB8)</td> </tr> <tr> <td></td> <td>Host-bus 8-bit interface (also known as the MCU interface). Control, address, and data pins are configured using the <code>EPIHB8CFG</code> and <code>EPIHB8CFG2</code> registers.</td> </tr> <tr> <td>0x3</td> <td>16-Bit Host-Bus (HB16)</td> </tr> <tr> <td></td> <td>Host-bus 16-bit interface (standard SRAM). Control, address, and data pins are configured using the <code>EPIHB16CFG</code> and <code>EPIHB16CFG2</code> registers.</td> </tr> <tr> <td>0x3-0xF</td> <td>Reserved</td> </tr> </table>	Value	Description	0x0	General Purpose		General-Purpose mode. Control, address, and data pins are configured using the <code>EPIGPCFG</code> and <code>EPIGPCFG2</code> registers.	0x1	SDRAM		Supports SDR SDRAM. Control, address, and data pins are configured using the <code>EPISDRAMCFG</code> register.	0x2	8-Bit Host-Bus (HB8)		Host-bus 8-bit interface (also known as the MCU interface). Control, address, and data pins are configured using the <code>EPIHB8CFG</code> and <code>EPIHB8CFG2</code> registers.	0x3	16-Bit Host-Bus (HB16)		Host-bus 16-bit interface (standard SRAM). Control, address, and data pins are configured using the <code>EPIHB16CFG</code> and <code>EPIHB16CFG2</code> registers.	0x3-0xF	Reserved
Value	Description																							
0x0	General Purpose																							
	General-Purpose mode. Control, address, and data pins are configured using the <code>EPIGPCFG</code> and <code>EPIGPCFG2</code> registers.																							
0x1	SDRAM																							
	Supports SDR SDRAM. Control, address, and data pins are configured using the <code>EPISDRAMCFG</code> register.																							
0x2	8-Bit Host-Bus (HB8)																							
	Host-bus 8-bit interface (also known as the MCU interface). Control, address, and data pins are configured using the <code>EPIHB8CFG</code> and <code>EPIHB8CFG2</code> registers.																							
0x3	16-Bit Host-Bus (HB16)																							
	Host-bus 16-bit interface (standard SRAM). Control, address, and data pins are configured using the <code>EPIHB16CFG</code> and <code>EPIHB16CFG2</code> registers.																							
0x3-0xF	Reserved																							

## Register 2: EPI Main Baud Rate (EPIBAUD), offset 0x004

The system clock is used internally to the EPI Controller. The baud rate counter can be used to divide the system clock down to control the speed on the external interface. If the mode selected emits an external EPI clock, this register defines the EPI clock emitted. If the mode selected does not use an EPI clock, this register controls the speed of changes on the external interface. Care must be taken to program this register properly so that the speed of the external bus corresponds to the speed of the external peripheral and puts acceptable current load on the pins. `COUNT0` is the bit field used in all modes except in HB8 and HB16 modes with dual chip selects when different baud rates are selected, see page 386. If different baud rates are used, `COUNT0` is associated with the address range specified by `CS0` and `COUNT1` is associated with the address range specified by `CS1`.

The `COUNTn` field is not a straight divider or count. The EPI Clock on `EPI0S31` is related to the `COUNTn` field and the system clock as follows:

If `COUNTn = 0`,

$$EPIClockFreq = SystemClockFreq$$

otherwise:

$$EPIClockFreq = \frac{SystemClockFreq}{\left(\left\lfloor \frac{COUNTn}{2} \right\rfloor + 1\right) \times 2}$$

So, for example, a `COUNTn` of 0x0001 results in a clock rate of  $\frac{1}{2}$ (system clock); a `COUNTn` of 0x0002 or 0x0003 results in a clock rate of  $\frac{1}{4}$ (system clock).

### EPI Main Baud Rate (EPIBAUD)

Base 0x400D.0000  
Offset 0x004  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	COUNT1															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COUNT0															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	COUNT1	RO	0x0000	Baud Rate Counter 1  This bit field is only valid when the <code>CSCFG</code> field is 0x2 or 0x3 and the <code>CSBAUD</code> bit is set in the <code>EPIHBnCFG2</code> register.  This bit field contains a counter used to divide the system clock by the count. The maximum frequency for the external EPI clock is 50 MHz.  A count of 0 means the system clock is used as is.

Bit/Field	Name	Type	Reset	Description
15:0	COUNT0	R/W	0x0000	Baud Rate Counter 0  This bit field contains a counter used to divide the system clock by the count. The maximum frequency for the external EPI clock is 50 MHz.  A count of 0 means the system clock is used as is.

### Register 3: EPI SDRAM Configuration (EPISDRAMCFG), offset 0x010

**Important:** The `MODE` field in the `EPICFG` register determines which configuration register is accessed for offsets 0x010 and 0x014.

To access `EPISDRAMCFG`, the `MODE` field must be 0x1.

The SDRAM Configuration register is used to specify several parameters for the SDRAM controller. Note that this register is reset when the `MODE` field in the `EPICFG` register is changed. If another mode is selected and the SDRAM mode is selected again, the values must be reinitialized.

The SDRAM interface designed to interface to x16 SDR SDRAMs of 64 MHz or higher, with the address and data pins overlapped (wire ORed on the board). See Table 11-2 on page 349 for pin assignments.

#### EPI SDRAM Configuration (EPISDRAMCFG)

Base 0x400D.0000

Offset 0x010

Type R/W, reset 0x42EE.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FREQ		reserved			RFSH										
Type	R/W	R/W	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	1	0	1	1	1	0	1	1	1	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						SLEEP	reserved							SIZE	
Type	RO	RO	RO	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description										
31:30	FREQ	R/W	0x1	<p>Frequency Range</p> <p>This field configures the frequency range of the system clock. This field must be configured correctly to ensure proper operation. This field does not affect the refresh counting, which is configured separately using the <code>RFSH</code> field (and is based on system clock rate and number of rows per bank). The ranges are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0 - 15 MHz</td> </tr> <tr> <td>0x1</td> <td>15 - 30 MHz</td> </tr> <tr> <td>0x2</td> <td>30 - 50 MHz</td> </tr> <tr> <td>0x3</td> <td>50 - 100 MHz</td> </tr> </tbody> </table>	Value	Description	0x0	0 - 15 MHz	0x1	15 - 30 MHz	0x2	30 - 50 MHz	0x3	50 - 100 MHz
Value	Description													
0x0	0 - 15 MHz													
0x1	15 - 30 MHz													
0x2	30 - 50 MHz													
0x3	50 - 100 MHz													
29:27	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
26:16	RFSH	R/W	0x2EE	<p>Refresh Counter</p> <p>This field contains the refresh counter in system clocks. The reset value of 0x2EE provides a refresh period of 64 ms when using a 50 MHz clock.</p>										
15:10	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										

Bit/Field	Name	Type	Reset	Description
9	SLEEP	R/W	0	Sleep Mode  Value Description 1 The SDRAM is put into low power state, but is self-refreshed. 0 No effect.
8:2	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1:0	SIZE	R/W	0x0	Size of SDRAM  The value of this field affects address pins and behavior.  Value Description 0x0 64 megabits (8MB) 0x1 128 megabits (16MB) 0x2 256 megabits (32MB) 0x3 512 megabits (64MB)

## Register 4: EPI Host-Bus 8 Configuration (EPIHB8CFG), offset 0x010

**Important:** The `MODE` field in the `EPICFG` register determines which configuration register is accessed for offsets 0x010 and 0x014.

To access `EPIHB8CFG`, the `MODE` field must be 0x2.

The Host Bus 8 Configuration register is activated when the HB8 mode is selected. The HB8 mode supports muxed address/data (overlay of lower 8 address and all 8 data pins), separated address/data, and address-less FIFO mode. Note that this register is reset when the `MODE` field in the `EPICFG` register is changed. If another mode is selected and the HB8 mode is selected again, the values must be reinitialized.

This mode is intended to support SRAMs, Flash memory (read), FIFOs, CPLDs/FPGAs, and devices with an MCU/HostBus slave or 8-bit FIFO interface support.

Refer to Table 11-4 on page 353 for information on signal configuration controlled by this register and the `EPIHB8CFG2` register.

If less address pins are required, the corresponding `AFSEL` bit (page 310) should not be enabled so the EPI controller does not drive those pins, and they are available as standard GPIOs.

There is no direct chip enable (CE) model. Instead, CE can be handled in one of three ways:

1. Manually control via GPIOs.
2. Associate one or more upper address pins to CE. Because CE is normally CEn, lower addresses are not used. For example, if pins `EPIOS27` and `EPIOS26` are used for Device 1 and 0 respectively, then address 0x6800.0000 accesses Device 0 (Device 1 has its CEn high), and 0x6400.0000 accesses Device 1 (Device 0 has its CEn high). The pull-up behavior on the corresponding GPIOs must be properly configured to ensure that the pins are disabled when the interface is not in use.
3. With certain SRAMs, the ALE can be used as CEn because the address remains stable after the ALE strobe. The subsequent WRn or RDn signals write or read when ALE is low thus providing CEn functionality.

### EPI Host-Bus 8 Configuration (EPIHB8CFG)

Base 0x400D.0000

Offset 0x010

Type R/W, reset 0x0000.FF00

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved								XFFEN	XFEEN	WRHIGH	RDHIGH	reserved			
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MAXWAIT								WRWS		RDWS		reserved		MODE	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:24	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
23	XFFEN	R/W	0	External FIFO FULL Enable  Value Description 1 An external FIFO full signal can be used to control write cycles. If this bit is set and the FFULL full signal is high, XFIFO writes are stalled. 0 No effect.
22	XFEEN	R/W	0	External FIFO EMPTY Enable  Value Description 1 An external FIFO empty signal can be used to control read cycles. If this bit is set and the FEMPTY signal is high, XFIFO reads are stalled. 0 No effect.
21	WRHIGH	R/W	0	WRITE Strobe Polarity  Value Description 1 The WRITE strobe is WRn (active low). 0 The WRITE strobe is WR (active high).
20	RDHIGH	R/W	0	READ Strobe Polarity  Value Description 1 The READ strobe is RDn (active low). 0 The READ strobe is RD (active high).
19:16	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:8	MAXWAIT	R/W	0xFF	Maximum Wait  This field defines the maximum number of external clocks to wait while an external FIFO ready signal is holding off a transaction (FFULL and FEMPTY).  When this field is clear, the transaction is held off forever.



Bit/Field	Name	Type	Reset	Description
7:6	WRWS	R/W	0x0	<p>Write Wait States</p> <p>This field adds wait states to the data phase (the address phase is not affected). The effect is to delay the rising edge of WRn (or the falling edge of WR). Each wait state adds 2 EPI clock cycles to the access time.</p> <p>Value Description</p> <p>0x0 No wait states.</p> <p>0x1 1 wait state.</p> <p>0x2 2 wait states.</p> <p>0x3 3 wait states.</p> <p>This field is used in conjunction with the <b>EPIBAUD</b> register.</p>
5:4	RDWS	R/W	0x0	<p>Read Wait States</p> <p>This field adds wait states to the data phase (the address phase is not affected). The effect is to delay the rising edge of RDn/Oen (or the falling edge of RD). Each wait state adds 2 EPI clock cycles to the access time.</p> <p>Value Description</p> <p>0x0 No wait states.</p> <p>0x1 1 wait state.</p> <p>0x2 2 wait states.</p> <p>0x3 3 wait states.</p> <p>This field is used in conjunction with the <b>EPIBAUD</b> register.</p>
3:2	reserved	RO	0x0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
1:0	MODE	R/W	0x0	<p>Host Bus Sub-Mode</p> <p>This field determines which of four Host Bus 8 sub-modes to use. Sub-mode use is determined by the connected external peripheral. See Table 11-4 on page 353 for information on how this bit field affects the operation of the EPI signals.</p> <p>Value Description</p> <p>0x0 ADMUX – AD[7:0] Data and Address are muxed.</p> <p>0x1 ADNONMUX – D[7:0] Data and address are separate.</p> <p>0x2 SRAM This mode is the same as ADNONMUX, but uses address switch for multiple reads instead of OEn strobing.</p> <p>0x3 XFIFO – D[7:0] This mode adds XFIFO controls with sense of XFIFO full and XFIFO empty. This mode uses no address or ALE.</p>

## Register 5: EPI Host-Bus 16 Configuration (EPIHB16CFG), offset 0x010

**Important:** The `MODE` field in the `EPICFG` register determines which configuration register is accessed for offsets 0x010 and 0x014.

To access `EPIHB16CFG`, the `MODE` field must be 0x3.

The Host Bus 16 sub-configuration register is activated when the HB16 mode is selected. The HB16 mode supports muxed address/data (overlay of lower 16 address and all 16 data pins), separated address/data, and address-less FIFO mode. Note that this register is reset when the `MODE` field in the `EPICFG` register is changed. If another mode is selected and the HB16 mode is selected again, the values must be reinitialized.

This mode is intended to support SRAMs, Flash memory (read), FIFOs, and CPLDs/FPGAs, and devices with an MCU/HostBus slave or 16-bit FIFO interface support.

Refer to Table 11-5 on page 355 for information on signal configuration controlled by this register and the `EPIHB16CFG2` register.

If less address pins are required, the corresponding `AFSEL` bit (page 310) should not be enabled so the EPI controller does not drive those pins, and they are available as standard GPIOs.

There is no direct chip enable (CE) model. Instead, CE can be handled in one of three ways:

1. Manually control via GPIOs.
2. Associate one or more upper address pins to CE. Because CE is normally CEn, lower addresses are not used. For example, if pins `EPI0S27` and `EPI0S26` are used for Device 1 and 0 respectively, then address 0x6800.0000 accesses Device 0 (Device 1 has its CEn high), and 0x6400.0000 accesses Device 1 (Device 0 has its CEn high). The pull-up behavior on the corresponding GPIOs must be properly configured to ensure that the pins are disabled when the interface is not in use.
3. With certain SRAMs, the ALE can be used as CEn because the address remains stable after the ALE strobe. The subsequent `WRn` or `RDn` signals write or read when ALE is low thus providing CEn functionality.

### EPI Host-Bus 16 Configuration (EPIHB16CFG)

Base 0x400D.0000  
 Offset 0x010  
 Type R/W, reset 0x0000.FF00

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved								XFFEN	XFEEN	WRHIGH	RDHIGH	reserved			
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MAXWAIT								WRWS		RDWS		reserved	BSEL	MODE	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:24	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
23	XFFEN	R/W	0	External FIFO FULL Enable  Value Description 1 An external FIFO full signal can be used to control write cycles. If this bit is set and the FFULL signal is high, XFIFO writes are stalled. 0 No effect.
22	XFEEN	R/W	0	External FIFO EMPTY Enable  Value Description 1 An external FIFO empty signal can be used to control read cycles. If this bit is set and the FEMPTY signal is high, XFIFO reads are stalled. 0 No effect.
21	WRHIGH	R/W	0	WRITE Strobe Polarity  Value Description 1 The WRITE strobe is WRn (active low). 0 The WRITE strobe is WR (active high).
20	RDHIGH	R/W	0	READ Strobe Polarity  Value Description 1 The READ strobe is RDn (active low). 0 The READ strobe is RD (active high).
19:16	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:8	MAXWAIT	R/W	0xFF	Maximum Wait  This field defines the maximum number of external clocks to wait while an external FIFO ready signal is holding off a transaction (FFULL and FEMPTY).  When this field is clear, the transaction is held off forever.

Bit/Field	Name	Type	Reset	Description
7:6	WRWS	R/W	0x0	<p>Write Wait States</p> <p>This field adds wait states to the data phase (the address phase is not affected). The effect is to delay the rising edge of WRn (or the falling edge of WR). Each wait state adds 2 EPI clock cycles to the access time.</p> <p>Value Description</p> <p>0x0 No wait states.</p> <p>0x1 1 wait state.</p> <p>0x2 2 wait states.</p> <p>0x3 3 wait states.</p> <p>This field is used in conjunction with the <b>EPIBAUD</b> register.</p>
5:4	RDWS	R/W	0x0	<p>Read Wait States</p> <p>This field adds wait states to the data phase (the address phase is not affected). The effect is to delay the rising edge of RDn/Oen (or the falling edge of RD). Each wait state adds 2 EPI clock cycles to the access time.</p> <p>Value Description</p> <p>0x0 No wait states.</p> <p>0x1 1 wait state.</p> <p>0x2 2 wait states.</p> <p>0x3 3 wait states.</p> <p>This field is used in conjunction with the <b>EPIBAUD</b> register.</p>
3	reserved	RO	0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
2	BSEL	R/W	0	<p>Byte Select Configuration</p> <p>This bit enables byte select operation.</p> <p>Value Description</p> <p>0 No Byte Selects</p> <p>Data is read and written as 16 bits.</p> <p>1 Enable Byte Selects</p> <p>Two EPI signals function as byte select signals to allow 8-bit transfers. See Table 11-5 on page 355 for details on which EPI signals are used.</p>

Bit/Field	Name	Type	Reset	Description
1:0	MODE	R/W	0x0	<p>Host Bus Sub-Mode</p> <p>This field determines which of three Host Bus 16 sub-modes to use. Sub-mode use is determined by the connected external peripheral. See Table 11-5 on page 355 for information on how this bit field affects the operation of the EPI signals.</p> <p>Value Description</p> <p>0x0 ADMUX – AD[15:0] Data and Address are muxed.</p> <p>0x1 ADNONMUX – D[15:0] Data and address are separate. This mode is not practical in HB16 mode for normal peripherals because there are generally not enough address bits available.</p> <p>0x2 SRAM This mode is the same as ADNONMUX, but uses address switch for multiple reads instead of OEn strobing. This mode is not practical in HB16 mode for normal SRAMs because there are generally not enough address bits available.</p> <p>0x3 XFIFO – D[15:0] This mode adds XFIFO controls with sense of XFIFO full and XFIFO empty. This mode uses no address or ALE.</p>

## Register 6: EPI General-Purpose Configuration (EPIGPCFG), offset 0x010

**Important:** The `MODE` field in the `EPICFG` register determines which configuration register is accessed for offsets 0x010 and 0x014.

To access `EPIGPCFG`, the `MODE` field must be 0x0.

The `RD2CYC` bit must be set at all times in General-Purpose mode to ensure proper operation.

The General-Purpose configuration register is used to configure the control, data, and address pins. This mode can be used for custom interfaces with FPGAs, CPLDs, and for digital data acquisition and actuator control. Note that this register is reset when the `MODE` field in the `EPICFG` register is changed. If another mode is selected and the General-purpose mode is selected again, the register the values must be reinitialized.

This mode is designed for 3 general types of use:

- Extremely high-speed clocked interfaces to FPGAs and CPLDs, with 3 sizes of data and optional address. Framing and clock-enable permit more optimized interfaces.
- General parallel GPIO. From 1 to 32 pins may be written or read, with the speed precisely controlled by the baud rate in the `EPIBAUD` register (when used with the `NBRFIFO` and/or the `WFIFO`) or by rate of accesses from software or  $\mu$ DMA.
- General custom interfaces of any speed.

The configuration allows for choice of an output clock (free running or gated), a framing signal (with frame size), a ready input (to stretch transactions), read and write strobes, address of varying sizes, and data of varying sizes. Additionally, provisions are made for splitting address and data phases on the external interface.

### EPI General-Purpose Configuration (EPIGPCFG)

Base 0x400D.0000  
 Offset 0x010  
 Type R/W, reset 0x0000.FF00

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CLKPIN	CLKGATE	reserved	RDYEN	FRMPIN	FRM50	FRMCNT			RW	reserved	WR2CYC	RD2CYC	reserved		
Type	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	R/W	R/W	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MAXWAIT							reserved		ASIZE		reserved		DSIZE		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W	RO	RO	R/W	R/W
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
-----------	------	------	-------	-------------

31	CLKPIN	R/W	0	Clock Pin
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Value	Description
1	<code>EPIOS31</code> functions as the EPI clock output.
0	No clock output.

The EPI clock is generated from the `COUNT0` field in the `EPIBAUD` register (as is the system clock which is divided down from it).

Bit/Field	Name	Type	Reset	Description
30	CLKGATE	R/W	0	<p>Clock Gated</p> <p>Value Description</p> <p>1 The EPI clock is output only when there is data to write or read (current transaction); otherwise the EPI clock is held low.</p> <p>0 The EPI clock is free running.</p> <p>Note that <code>EPIOS27</code> is an <code>iRDY</code> signal if <code>RDYEN</code> is set. <code>CLKGATE</code> is ignored if <code>CLKPIN</code> is 0 or if the <code>COUNT0</code> field in the <b>EPIBAUD</b> register is cleared.</p>
29	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	RDYEN	R/W	0	<p>Ready Enable</p> <p>Value Description</p> <p>1 The external peripheral drives an <code>iRDY</code> signal into pin <code>EPIOS27</code>.</p> <p>0 The external peripheral does not drive an <code>iRDY</code> signal and is assumed to be ready always.</p> <p>The ready enable signal may only be used with a free-running EPI clock (<code>CLKGATE=0</code>).</p> <p>The external <code>iRDY</code> signal is sampled on the falling edge of the EPI clock. Setup and hold times must be met to ensure registration on the next falling EPI clock edge.</p> <p>This bit is ignored if <code>CLKPIN</code> is 0 or <code>CLKGATE</code> is 1.</p>
27	FRMPIN	R/W	0	<p>Framing Pin</p> <p>Value Description</p> <p>1 A framing signal is output on <code>EPIOS30</code>.</p> <p>0 No framing signal is output.</p> <p>Framing has no impact on data itself, but forms a context for the external peripheral. When used with a free-running EPI clock, the <code>FRAME</code> signal forms the valid signal. When used with a gated EPI clock, it is usually used to form a frame size.</p>
26	FRM50	R/W	0	<p>50/50 Frame</p> <p>Value Description</p> <p>1 The <code>FRAME</code> signal is output as 50/50 duty cycle using count (see <code>FRMCNT</code>).</p> <p>0 The <code>FRAME</code> signal is output as a single pulse, and then held low for the count.</p> <p>This bit is ignored if <code>FRMPIN</code> is 0.</p>

Bit/Field	Name	Type	Reset	Description
25:22	FRMCNT	R/W	0x0	<p>Frame Count</p> <p>This field specifies the size of the frame in EPI clocks. The frame counter is used to determine the frame size. The count is FRMCNT+1. So, a FRMCNT of 0 forms a pure transaction valid signal (held high during transactions, low otherwise).</p> <p>A FRMCNT of 0 with FRM50 set inverts the FRAME signal on each transaction. A FRMCNT of 1 means the FRAME signal is inverted every other transaction; a value of 15 means every sixteenth transaction.</p> <p>If FRM50 is set, the frame is held high for FRMCNT+1 transactions, then held low for that many transactions, and so on.</p> <p>If FRM50 is clear, the frame is pulsed high for one EPI clock and then low for FRMCNT EPI clocks.</p> <p>This field is ignored if FRMPIN is 0.</p>
21	RW	R/W	0	<p>Read and Write</p> <p>Value Description</p> <p>1 RD and WR strobes are asserted on EPI0S29 and EPI0S28. RD is asserted high on the rising edge of the EPI clock when a read is being performed. WR is asserted high on the rising edge of the EPI clock when a write is being performed</p> <p>0 RD and WR strobes are not output.</p> <p>This bit is forced to 1 when RD2CYC and/or WR2CYC is 1.</p>
20	reserved	RO	0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
19	WR2CYC	R/W	0	<p>2-Cycle Writes</p> <p>Value Description</p> <p>1 Writes are two EPI clock cycles long, with address on one EPI clock cycle (with the WR strobe asserted) and data written on the following EPI clock cycle (with WR strobe de-asserted). The next address (if any) is in the cycle following.</p> <p>0 Data is output on the same EPI clock cycle as the address.</p> <p>When this bit is set, then the RW bit is forced to be set.</p>
18	RD2CYC	R/W	0	<p>2-Cycle Reads</p> <p>Value Description</p> <p>1 Reads are two EPI clock cycles, with address on one EPI clock cycle (with the RD strobe asserted) and data captured on the following EPI clock cycle (with the RD strobe de-asserted). The next address (if any) is in the cycle following.</p> <p>0 Data is captured on the EPI clock cycle with READ strobe asserted.</p> <p>When this bit is set, then the RW bit is forced to be set.</p> <p><b>Caution – This bit must be set at all times in General-Purpose mode to ensure proper operation.</b></p>



Bit/Field	Name	Type	Reset	Description										
17:16	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
15:8	MAXWAIT	R/W	0xFF	<p>Maximum Wait</p> <p>This field defines the maximum number of EPI clocks to wait while the iRDY signal (see RDYEN) is holding off a transaction. If this field is 0, the transaction is held forever. If the maximum wait of 255 clocks (MAXWAIT=0xFF) is exceeded, an error interrupt occurs and the transaction is aborted/ignored.</p>										
7:6	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
5:4	ASIZE	R/W	0x0	<p>Address Bus Size</p> <p>This field defines the size of the address bus. The address can be up to 4-bits wide with a 24-bit data bus, up to 12-bits wide with a 16-bit data bus, and up to 20-bits wide with an 8-bit data bus. If the full address bus is not used, use the least significant address bits. Any unused address bits can be used as GPIOs by clearing the AFSEL bit for the corresponding GPIOs. Also, if RDYEN is 1, then the address sizes are 1 smaller (3, 11, 19).</p> <p>The values are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>No address</td> </tr> <tr> <td>0x1</td> <td>Up to 4 bits wide.</td> </tr> <tr> <td>0x2</td> <td>Up to 12 bits wide. This size cannot be used with 24-bit data.</td> </tr> <tr> <td>0x3</td> <td>Up to 20 bits wide. This size cannot be used with data sizes other than 8.</td> </tr> </tbody> </table>	Value	Description	0x0	No address	0x1	Up to 4 bits wide.	0x2	Up to 12 bits wide. This size cannot be used with 24-bit data.	0x3	Up to 20 bits wide. This size cannot be used with data sizes other than 8.
Value	Description													
0x0	No address													
0x1	Up to 4 bits wide.													
0x2	Up to 12 bits wide. This size cannot be used with 24-bit data.													
0x3	Up to 20 bits wide. This size cannot be used with data sizes other than 8.													
3:2	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
1:0	DSIZE	R/W	0x0	<p>Size of Data Bus</p> <p>This field defines the size of the data bus (starting at EPIOS0). Subsets of these numbers can be created by clearing the AFSEL bit for the corresponding GPIOs. Note that size 32 may not be used with clock, frame, address, or other control.</p> <p>The values are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>8 Bits Wide (EPIOS0 to EPIOS7)</td> </tr> <tr> <td>0x1</td> <td>16 Bits Wide (EPIOS0 to EPIOS15)</td> </tr> <tr> <td>0x2</td> <td>24 Bits Wide (EPIOS0 to EPIOS23)</td> </tr> <tr> <td>0x3</td> <td>32 Bits Wide (EPIOS0 to EPIOS31)</td> </tr> </tbody> </table> <p>This size may not be used with an EPI clock. This value is normally used for acquisition input and actuator control as well as other general-purpose uses that require 32 bits per direction.</p>	Value	Description	0x0	8 Bits Wide (EPIOS0 to EPIOS7)	0x1	16 Bits Wide (EPIOS0 to EPIOS15)	0x2	24 Bits Wide (EPIOS0 to EPIOS23)	0x3	32 Bits Wide (EPIOS0 to EPIOS31)
Value	Description													
0x0	8 Bits Wide (EPIOS0 to EPIOS7)													
0x1	16 Bits Wide (EPIOS0 to EPIOS15)													
0x2	24 Bits Wide (EPIOS0 to EPIOS23)													
0x3	32 Bits Wide (EPIOS0 to EPIOS31)													

## Register 7: EPI Host-Bus 8 Configuration 2 (EPIHB8CFG2), offset 0x014

**Important:** The `MODE` field in the `EPICFG` register determines which configuration register is accessed for offsets 0x010 and 0x014.

To access `EPIHB8CFG2`, the `MODE` field must be 0x2.

This register is used to configure operation while in Host-Bus 8 mode. Note that this register is reset when the `MODE` field in the `EPICFG` register is changed. If another mode is selected and the Host-Bus 8 mode is selected again, the values must be reinitialized.

### EPI Host-Bus 8 Configuration 2 (EPIHB8CFG2)

Base 0x400D.0000

Offset 0x014

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WORD	reserved				CSBAUD	CSCFG			reserved						
Type	R/W	RO	RO	RO	RO	R/W	R/W	R/W	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description										
31	WORD	R/W	0	<p>Word Access Mode</p> <p>By default, the EPI controller uses data bits [7:0] for Host-Bus 8 accesses. When using Word Access mode, the EPI controller can automatically route bytes of data onto the correct byte lanes such that data can be stored in bits [31:8].</p> <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>0</td> <td>Word Access mode is disabled.</td> </tr> <tr> <td>1</td> <td>Word Access mode is enabled.</td> </tr> </table>	Value	Description	0	Word Access mode is disabled.	1	Word Access mode is enabled.				
Value	Description													
0	Word Access mode is disabled.													
1	Word Access mode is enabled.													
30:27	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
26	CSBAUD	R/W	0	<p>Chip Select Baud Rate</p> <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>0</td> <td>Same Baud Rate</td> </tr> <tr> <td colspan="2">Both CS0n and CS1n use the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register.</td> </tr> <tr> <td>1</td> <td>Different Baud Rates</td> </tr> <tr> <td colspan="2">CS0n uses the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register. CSn1 uses the baud rate defined by the <code>COUNT1</code> field in the <code>EPIBAUD</code> register.</td> </tr> </table>	Value	Description	0	Same Baud Rate	Both CS0n and CS1n use the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register.		1	Different Baud Rates	CS0n uses the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register. CSn1 uses the baud rate defined by the <code>COUNT1</code> field in the <code>EPIBAUD</code> register.	
Value	Description													
0	Same Baud Rate													
Both CS0n and CS1n use the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register.														
1	Different Baud Rates													
CS0n uses the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register. CSn1 uses the baud rate defined by the <code>COUNT1</code> field in the <code>EPIBAUD</code> register.														

Bit/Field	Name	Type	Reset	Description
25:24	CSCFG	R/W	0x0	<p>Chip Select Configuration</p> <p>Value Description</p> <p>0x0 ALE Configuration</p> <p>EPIOS30 is used as an address latch (ALE). When using this mode, the address and data should be muxed (HB8MODE field in the <b>EPIHB8CFG</b> register should be configured to 0x0). If needed, the address can be latched by external logic.</p> <p>0x1 CSn Configuration</p> <p>EPIOS30 is used as a Chip Select (CSn). When using this mode, the address and data should not be muxed (HB8MODE field in the <b>EPIHB8CFG</b> register should be configured to 0x1). In this mode, the WR signal (EPIOS29) and the RD signal (EPIOS28) are used to latch the address when CSn is low.</p> <p>0x2 Dual CSn Configuration</p> <p>EPIOS30 is used as CS0n and EPIOS27 is used as CS1n. Whether CS0n or CS1n is asserted is determined by the most significant address bit for a respective external address map. This configuration can be used for a RAM bank split between 2 devices as well as when using both an external RAM and an external peripheral.</p> <p>0x3 ALE with Dual CSn Configuration</p> <p>EPIOS30 is used as address latch (ALE), EPIOS27 is used as CS0n, and EPIOS26 is used as CS1n. Whether CS0n or CS1n is asserted is determined by the most significant address bit for a respective external address map.</p>
23:0	reserved	RO	0x00.0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 8: EPI Host-Bus 16 Configuration 2 (EPIHB16CFG2), offset 0x014

**Important:** The `MODE` field in the `EPICFG` register determines which configuration register is accessed for offsets 0x010 and 0x014.

To access `EPIHB16CFG2`, the `MODE` field must be 0x3.

This register is used to configure operation while in Host-Bus 16 mode. Note that this register is reset when the `MODE` field in the `EPICFG` register is changed. If another mode is selected and the Host-Bus 16 mode is selected again, the values must be reinitialized.

### EPI Host-Bus 16 Configuration 2 (EPIHB16CFG2)

Base 0x400D.0000  
 Offset 0x014  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WORD	reserved				CSBAUD	CSCFG			reserved						
Type	R/W	RO	RO	RO	RO	R/W	R/W	R/W	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	WORD	R/W	0	Word Access Mode  By default, the EPI controller uses data bits [15:0] for Host-Bus 16 accesses. When using Word Access mode, the EPI controller can automatically route bytes of data onto the correct byte lanes such that data can be stored in bits [31:16].  Value Description 0 Word Access mode is disabled. 1 Word Access mode is enabled.
30:27	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
26	CSBAUD	R/W	0	Chip Select Baud Rate  Value Description 0 Same Baud Rate Both CS0n and CS1n use the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register. 1 Different Baud Rates CS0n uses the baud rate for the external bus that is defined by the <code>COUNT0</code> field in the <code>EPIBAUD</code> register. CSn1 uses the baud rate defined by the <code>COUNT1</code> field in the <code>EPIBAUD</code> register.

Bit/Field	Name	Type	Reset	Description
25:24	CSCFG	R/W	0x0	<p>Chip Select Configuration</p> <p>This field controls the chip select options, including an ALE format and a chip select format.</p> <p>Value Description</p> <p>0x0 ALE Configuration</p> <p>EPIOS30 is used as an address latch (ALE). When using this mode, the address and data should be muxed (HB16MODE field in the EPIHB16CFG register should be configured to 0x0). If needed, the address can be latched by external logic.</p> <p>0x1 CSn Configuration</p> <p>EPIOS30 is used as a Chip Select (CSn). When using this mode, the address and data should not be muxed (HB16MODE field in the EPIHB16CFG register should be configured to 0x1). In this mode, the WR signal (EPIOS29) and the RD signal (EPIOS28) are used to latch the address when CSn is low.</p> <p>0x2 Dual CSn Configuration</p> <p>EPIOS30 is used as CS0n and EPIOS27 is used as CS1n. Whether CS0n or CS1n is asserted is determined by the most significant address bit for a respective external address map. This configuration can be used for a RAM bank split between 2 devices as well as when using both an external RAM and an external peripheral.</p> <p>0x3 ALE with Dual CSn Configuration</p> <p>EPIOS30 is used as address latch (ALE), EPIOS27 is used as CS0n, and EPIOS26 is used as CS1n. Whether CS0n or CS1n is asserted is determined by the most significant address bit for a respective external address map.</p>
23:0	reserved	RO	0x00.0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

## Register 9: EPI General-Purpose Configuration 2 (EPIGPCFG2), offset 0x014

**Important:** The `MODE` field in the `EPICFG` register determines which configuration register is accessed for offsets 0x010 and 0x014.

To access `EPIGPCFG2`, the `MODE` field must be 0x0.

This register is used to configure operation while in General-Purpose mode. Note that this register is reset when the `MODE` field in the `EPICFG` register is changed. If another mode is selected and the General-Purpose mode is selected again, the values must be reinitialized.

### EPI General-Purpose Configuration 2 (EPIGPCFG2)

Base 0x400D.0000  
 Offset 0x014  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WORD	reserved														
Type	R/W	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description						
31	WORD	R/W	0x0	<p>Word Access Mode</p> <p>By default, the EPI controller uses data bits [7:0] when the <code>DSIZE</code> field in the <code>EPIGPCFG</code> register is 0x0; data bits [15:0] when the <code>DSIZE</code> field is 0x1; data bits [23:0] when the <code>DSIZE</code> field is 0x2; and data bits [31:0] when the <code>DSIZE</code> field is 0x3.</p> <p>When using Word Access mode, the EPI controller can automatically route bytes of data onto the correct byte lanes such that data can be stored in bits [31:8] for <code>DSIZE</code>=0x0 and bits [31:16] for <code>DSIZE</code>=0x1. For <code>DSIZE</code>=0x2 or 0x3, this bit must be clear.</p> <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>0</td> <td>Word Access mode is disabled.</td> </tr> <tr> <td>1</td> <td>Word Access mode is enabled.</td> </tr> </table>	Value	Description	0	Word Access mode is disabled.	1	Word Access mode is enabled.
Value	Description									
0	Word Access mode is disabled.									
1	Word Access mode is enabled.									
30:0	reserved	RO	0x000.0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						

## Register 10: EPI Address Map (EPIADDRMAP), offset 0x01C

This register enables address mapping. The EPI controller can directly address memory and peripherals. In addition, the EPI controller supports address mapping to allow indirect accesses in the External RAM and External Peripheral areas.

If the external device is a peripheral, including a FIFO or a directly addressable device, the `EPSZ` and `EPADR` bit fields should be configured for the address space. If the external device is SDRAM, SRAM, NOR or NAND Flash memory, the `ERADR` and `ERSZ` bit fields should be configured for the address space.

If one of the Dual-Chip-Select modes is selected (`CSCFG=0x2` or `0x3` in the `EPIHBnCFG2` register), both chip selects can share the peripheral or the memory space, or one chip select can use the peripheral space and the other can use the memory space. If the `EPADR` field is not `0x0` and the `ERADR` field is `0x0`, then the address specified by `EPADR` is used for both chip selects, with `CS0n` being asserted when the MSB of the address range is 0 and `CS1n` being asserted when the MSB of the address range is 1. If the `ERADR` field is not `0x0` and the `EPADR` field is `0x0`, then the address specified by `ERADR` is used for both chip selects, with the MSB performing the same delineation. If both the `EPADR` and the `ERADR` are not `0x0`, then `CS0n` is asserted for the address range defined by `EPADR` and `CS1n` is asserted for the address range defined by `ERADR`.

### EPI Address Map (EPIADDRMAP)

Base 0x400D.0000  
Offset 0x01C  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								EPSZ		EPADR		ERSZ		ERADR	
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:6	EPSZ	R/W	0x0	External Peripheral Size  This field selects the size of the external peripheral. If the size of the external peripheral is larger, a bus fault occurs. If the size of the external peripheral is smaller, it wraps (upper address bits unused):  Value Description 0x0 256 bytes; lower address range: 0x00 to 0xFF 0x1 64 KB; lower address range: 0x0000 to 0xFFFF 0x2 16 MB; lower address range: 0x00.0000 to 0xFF.FFFF 0x3 256 MB; lower address range: 0x000.0000 to 0xFFF.FFFF

Bit/Field	Name	Type	Reset	Description
5:4	EPADR	R/W	0x0	External Peripheral Address This field selects address mapping for the external peripheral area:  Value Description 0x0 Not mapped 0x1 At 0xA000.0000 0x2 At 0xC000.0000 0x3 reserved
3:2	ERSZ	R/W	0x0	External RAM Size This field selects the size of mapped RAM. If the size of the external memory is larger, a bus fault occurs. If the size of the external memory is smaller, it wraps (upper address bits unused):  Value Description 0x0 256 bytes; lower address range: 0x00 to 0xFF 0x1 64 KB; lower address range: 0x0000 to 0xFFFF 0x2 16 MB; lower address range: 0x00.0000 to 0xFF.FFFF 0x3 256 MB; lower address range: 0x000.0000 to 0xFFF.FFFF
1:0	ERADR	R/W	0x0	External RAM Address Selects address mapping for external RAM area:  Value Description 0x0 Not mapped 0x1 At 0x6000.0000 0x2 At 0x8000.0000 0x3 reserved



**Register 11: EPI Read Size 0 (EPIRSIZE0), offset 0x020****Register 12: EPI Read Size 1 (EPIRSIZE1), offset 0x030**

This register selects the size of transactions when performing non-blocking reads with the **EPIRPSTDn** registers. This size affects how the external address is incremented.

The **SIZE** field must match the external data width as configured in the **EPIHBnCFG** or **EPIGPCFG** register.

SDRAM mode uses a 16-bit data interface. If **SIZE** is 0x1, data is returned on the least significant bits (D[7:0]), and the remaining bits D[31:8] are all zeros, therefore the data on bits D[15:8] is lost. If **SIZE** is 0x2, data is returned on the least significant bits (D[15:0]), and the remaining bits D[31:16] are all zeros.

Note that changing this register while a read is active has an unpredictable effect.

**EPI Read Size 0 (EPIRSIZE0)**

Base 0x400D.0000

Offset 0x020

Type R/W, reset 0x0000.0003

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved														SIZE	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1:0	SIZE	R/W	0x3	Current Size
	Value	Description		
	0x0	reserved		
	0x1	Byte (8 bits)		
	0x2	Half-word (16 bits)		
	0x3	Word (32 bits)		

**Register 13: EPI Read Address 0 (EPIRADDR0), offset 0x024**

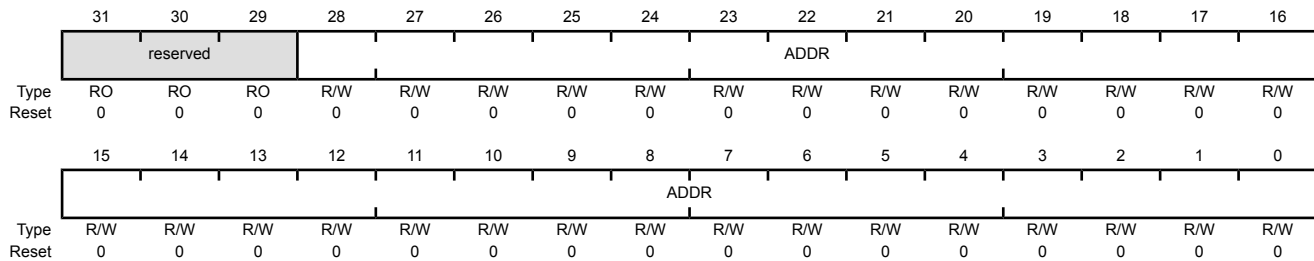
**Register 14: EPI Read Address 1 (EPIRADDR1), offset 0x034**

This register holds the current address value. When performing non-blocking reads via the **EPIRSTDn** registers, this register's value forms the address (when used by the mode). That is, when an **EPIRSTDn** register is written with a non-0 value, this register is used as the first address. After each read, it is incremented by the size specified by the corresponding **EPIRSIZEn** register. Thus at the end of a read, this register contains the next address for the next read. For example, if the last read was 0x20, and the size is word, then the register contains 0x24. When a non-blocking read is cancelled, this register contains the next address that would have been read had it not been cancelled. For example, if reading by bytes and 0x103 had been read but not 0x104, this register contains 0x104. In this manner, the system can determine the number of values in the NBRFIFO to drain.

Note that changing this register while a read is active has an unpredictable effect due to race condition.

EPI Read Address 0 (EPIRADDR0)

Base 0x400D.0000  
 Offset 0x024  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28:0	ADDR	R/W	0x000.0000	Current Address Next address to read.

**Register 15: EPI Non-Blocking Read Data 0 (EPIRPSTD0), offset 0x028****Register 16: EPI Non-Blocking Read Data 1 (EPIRPSTD1), offset 0x038**

This register sets up a non-blocking read via the external interface. A non-blocking read is started by writing to this register with the count (other than 0). Clearing this register terminates an active non-blocking read as well as cancelling any that are pending. This register should always be cleared before writing a value other than 0; failure to do so can cause improper operation.

The first address is based on the corresponding **EPIADDRn** register. The address register is incremented by the size specified by the **EPIRSIZEn** register after each read. If the size is less than a word, only the least significant bits of data are filled into the NBRFIFO; the most significant bits are cleared.

Note that all three registers may be written using one STM instruction, such as with a structure copy in C/C++.

The data may be read from the **EPIREADFIFO** register after the read cycle is completed. The interrupt mechanism is normally used to trigger the FIFO reads via ISR or  $\mu$ DMA.

If the countdown has not reached 0 and the NBRFIFO is full, the external interface waits until a NBRFIFO entry becomes available to continue.

Note: if a blocking read or write is performed through the address mapped area (at 0x6000.0000 through 0xCFFF.FFFF), any current non-blocking read is paused (at the next safe boundary), and the blocking request is inserted. After completion of any blocking reads or writes, the non-blocking reads continue from where they were paused.

The other way to read data is via the address mapped locations (see the **EPIADDRMAP** register), but this method is blocking (core or  $\mu$ DMA waits until result is returned).

To cancel a non-blocking read, clear this register. To make sure that all values read are drained from the NBRFIFO, the **EPISTAT** register must be consulted to be certain that bits **NBRBUSY** and **ACTIVE** are cleared. One of these registers should not be cleared until either the other **EPIRPSTDn** register becomes active or the external interface is not busy. At that point, the corresponding **EPIADDRn** register indicates how many values were read.

**EPI Non-Blocking Read Data 0 (EPIRPSTD0)**

Base 0x400D.0000

Offset 0x028

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved			POSTCNT												
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:13	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
12:0	POSTCNT	R/W	0x000	<p>Post Count</p> <p>A write of a non-zero value starts a read operation for that count. Note that it is the software's responsibility to handle address wraparound.</p> <p>Reading this register provides the current count.</p> <p>A write of 0 cancels a non-blocking read (whether active now or pending).</p> <p>Prior to writing a non-zero value, this register must first be cleared.</p>

## Register 17: EPI Status (EPISTAT), offset 0x060

This register indicates which non-blocking read register is currently active; it also indicates whether the external interface is busy performing a write or non-blocking read (it cannot be performing a blocking read, as the bus would be blocked and as a result, this register could not be accessed).

This register is useful for determining which non-blocking read register is active when both are loaded with values and when implementing sequencing or sharing.

This register is also useful when canceling non-blocking reads, as it shows how many values were read by the canceled side.

### EPI Status (EPISTAT)

Base 0x400D.0000

Offset 0x060

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						CELOW	XFFULL	XFEMPTY	INITSEQ	WBUSY	NBRBUSY	reserved			ACTIVE
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:10	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9	CELOW	RO	0	<p>Clock Enable Low</p> <p>This bit provides information on the clock status when in general-purpose mode and the RDYEN bit is set.</p> <p>Value Description</p> <p>1 The external device is gating the clock (iRDY is low). Attempts to read or write in this situation are stalled until the clock is enabled or the counter times out as specified by the MAXWAIT field.</p> <p>0 The external device is not gating the clock.</p>
8	XFFULL	RO	0	<p>External FIFO Full</p> <p>This bit provides information on the XFIFO when in the FIFO sub-mode of the Host Bus n mode with the XFFEN bit set in the EPIHBnCFG register. The EPIOS26 signal reflects the status of this bit.</p> <p>Value Description</p> <p>1 The XFIFO is signaling as full (the FIFO full signal is high). Attempts to write in this case are stalled until the XFIFO full signal goes low or the counter times out as specified by the MAXWAIT field.</p> <p>0 The external device is not gating the clock.</p>

Bit/Field	Name	Type	Reset	Description
7	XFEMPTY	RO	0	<p>External FIFO Empty</p> <p>This bit provides information on the XFIFO when in the FIFO sub-mode of the Host Bus n mode with the <i>XFEEEN</i> bit set in the <b>EPIHBnCFG</b> register. The <i>EPIOS27</i> signal reflects the status of this bit.</p> <p>Value Description</p> <p>1 The XFIFO is signaling as empty (the FIFO empty signal is high). Attempts to read in this case are stalled until the XFIFO empty signal goes low or the counter times out as specified by the <i>MAXWAIT</i> field.</p> <p>0 The external device is not gating the clock.</p>
6	INITSEQ	RO	0	<p>Initialization Sequence</p> <p>Value Description</p> <p>1 The SDRAM interface is running through the wakeup period (greater than 100 <math>\mu</math>s). If an attempt is made to read or write the SDRAM during this period, the access is held off until the wakeup period is complete.</p> <p>0 The SDRAM interface is not in the wakeup period.</p>
5	WBUSY	RO	0	<p>Write Busy</p> <p>Value Description</p> <p>1 The external interface is performing a write.</p> <p>0 The external interface is not performing a write.</p>
4	NBRBUSY	RO	0	<p>Non-Blocking Read Busy</p> <p>Value Description</p> <p>1 The external interface is performing a non-blocking read, or if the non-blocking read is paused due to a write.</p> <p>0 The external interface is not performing a non-blocking read.</p>
3:1	reserved	RO	0x0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
0	ACTIVE	RO	0	<p>Register Active</p> <p>Value Description</p> <p>1 The <b>EPIRPSTD1</b> register is active.</p> <p>0 If <i>NBRBUSY</i> is set, the <b>EPIRPSTD0</b> register is active. If the <i>NBRBUSY</i> bit is clear, then neither <b>EPIRPSTDx</b> register is active.</p>

## Register 18: EPI Read FIFO Count (EPIRFIFOCNT), offset 0x06C

This register returns the number of values in the NBRFIFO (the data in the NBRFIFO can be read via the **EPIREADFIFO** register). A race is possible, but that only means that more values may come in after this register has been read.

### EPI Read FIFO Count (EPIRFIFOCNT)

Base 0x400D.0000

Offset 0x06C

Type RO, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													COUNT		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-	-

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	COUNT	RO	-	FIFO Count Number of filled entries in the NBRFIFO.

**Register 19: EPI Read FIFO (EPIREADFIFO), offset 0x070**

**Register 20: EPI Read FIFO Alias 1 (EPIREADFIFO1), offset 0x074**

**Register 21: EPI Read FIFO Alias 2 (EPIREADFIFO2), offset 0x078**

**Register 22: EPI Read FIFO Alias 3 (EPIREADFIFO3), offset 0x07C**

**Register 23: EPI Read FIFO Alias 4 (EPIREADFIFO4), offset 0x080**

**Register 24: EPI Read FIFO Alias 5 (EPIREADFIFO5), offset 0x084**

**Register 25: EPI Read FIFO Alias 6 (EPIREADFIFO6), offset 0x088**

**Register 26: EPI Read FIFO Alias 7 (EPIREADFIFO7), offset 0x08C**

**Important:** Use caution when reading this register. Performing a read may change bit status.

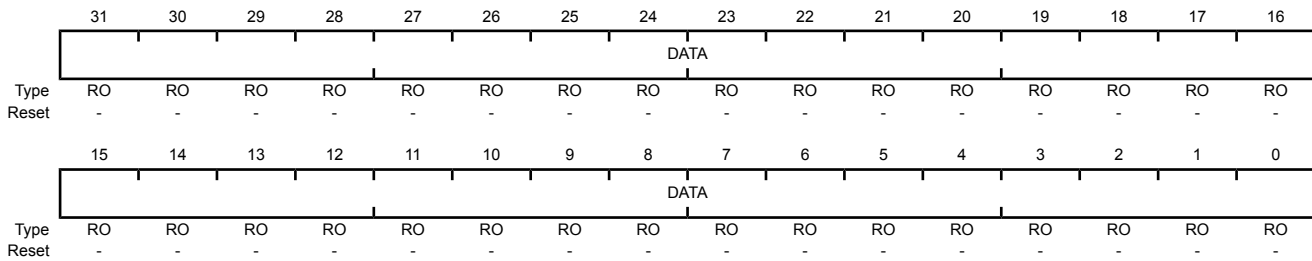
This register returns the contents of the NBRFIFO or 0 if the NBRFIFO is empty. Each read returns the data that is at the top of the NBRFIFO, and then empties that value from the NBRFIFO. The alias registers can be used with the LDMIA instruction for more efficient operation (for up to 8 registers). See *ARM® Cortex™-M3 Technical Reference Manual* for more information on the LDMIA instruction.

EPI Read FIFO (EPIREADFIFO)

Base 0x400D.0000

Offset 0x070

Type RO, reset -



Bit/Field	Name	Type	Reset	Description
31:0	DATA	RO	-	Reads Data

This field contains the data that is at the top of the NBRFIFO. After being read, the NBRFIFO entry is removed.



## Register 27: EPI FIFO Level Selects (EPIFIFOLVL), offset 0x200

This register allows selection of the FIFO levels which trigger an interrupt to the interrupt controller or, more efficiently, a DMA request to the  $\mu$ DMA. The NBRFIFO select triggers on fullness such that it triggers on match or above (more full). The WFIFO triggers on emptiness such that it triggers on match or below (less entries).

It should be noted that the FIFO triggers are not identical to other such FIFOs in Stellaris® peripherals. In particular, empty and full triggers are provided to avoid wait states when using blocking operations.

The settings in this register are only meaningful if the  $\mu$ DMA is active or the interrupt is enabled.

Additionally, this register allows protection against writes stalling and notification of performing blocking reads which stall for extra time due to preceding writes. The two functions behave in a non-orthogonal way because read and write are not orthogonal.

The write error bit configures the system such that an attempted write to an already full WFIFO abandons the write and signals an error interrupt to prevent accidental latencies due to stalling writes.

The read error bit configures the system such that after a read has been stalled due to any preceding writes in the WFIFO, the error interrupt is generated. Note that the excess stall is not prevented, but an interrupt is generated after the fact to notify that it has happened.

### EPI FIFO Level Selects (EPIFIFOLVL)

Base 0x400D.0000  
Offset 0x200  
Type R/W, reset 0x0000.0033

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved														WFERR	RSERR
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved										WRFIFO		reserved	RDFIFO		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1

Bit/Field	Name	Type	Reset	Description
31:18	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

17	WFERR	R/W	0	Write Full Error
----	-------	-----	---	------------------

#### Value Description

- |   |   |
|---|---|
| 1 | This bit enables the Write Full error interrupt (WTFULL in the <b>EPIIC</b> register) to be generated when a write is attempted and the WFIFO is full. The write stalls until a WFIFO entry becomes available.  |
| 0 | The Write Full error interrupt is disabled. Writes are stalled when the WFIFO is full until a space becomes available but an error is not generated. Note that the Cortex-M3 write buffer may hide that stall if no other memory transactions are attempted during that time. |

Bit/Field	Name	Type	Reset	Description
16	RSERR	R/W	0	<p>Read Stall Error</p> <p>Value Description</p> <p>1 This bit enables the Read Stalled error interrupt (<code>RSTALL</code> in the <b>EPIIC</b> register) to be generated when a read is attempted and the WFIFO is not empty. The read is still stalled during the time the WFIFO drains, but this error notifies the application that this excess delay has occurred.</p> <p>0 The Read Stalled error interrupt is disabled. Reads behave as normal and are stalled until any preceding writes have completed and the read has returned a result.</p> <p>Note that the configuration of this bit has no effect on non-blocking reads.</p>
15:7	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6:4	WRFIFO	R/W	0x3	<p>Write FIFO</p> <p>This field configures the trigger point for the WFIFO.</p> <p>Value Description</p> <p>0x0 Trigger when there are 1 to 4 spaces available in the WFIFO.</p> <p>0x1 reserved</p> <p>0x2 Trigger when there are 1 to 3 spaces available in the WFIFO.</p> <p>0x3 Trigger when there are 1 to 2 spaces available in the WFIFO.</p> <p>0x4 Trigger when there is 1 space available in the WFIFO.</p> <p>0x5-0x7 reserved</p>
3	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	RDFIFO	R/W	0x3	<p>Read FIFO</p> <p>This field configures the trigger point for the NBRFIFO.</p> <p>Value Description</p> <p>0x0 reserved</p> <p>0x1 Trigger when there are 1 or more entries in the NBRFIFO.</p> <p>0x2 Trigger when there are 2 or more entries in the NBRFIFO.</p> <p>0x3 Trigger when there are 4 or more entries in the NBRFIFO.</p> <p>0x4 Trigger when there are 6 or more entries in the NBRFIFO.</p> <p>0x5 Trigger when there are 7 or more entries in the NBRFIFO.</p> <p>0x6 Trigger when there are 8 entries in the NBRFIFO.</p> <p>0x7 reserved</p>

**Register 28: EPI Write FIFO Count (EPIWFIFOCNT), offset 0x204**

This register contains the number of slots currently available in the WFIFO. This register may be used for polled writes to avoid stalling and for blocking reads to avoid excess stalling (due to undrained writes). An example use for writes may be:

```
for (idx = 0; idx < cnt; idx++) {
while (EPIWFIFOCNT == 0) ;
*ext_ram = *mydata++;
}
```

The above code ensures that writes to the address mapped location do not occur unless the WFIFO has room. Although polling makes the code wait (spinning in the loop), it does not prevent interrupts being serviced due to bus stalling.

**EPI Write FIFO Count (EPIWFIFOCNT)**

Base 0x400D.0000

Offset 0x204

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													WTAV		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	WTAV	RO	0x0	Available Write Transactions The number of write transactions available in the WFIFO. When clear, a write is stalled waiting for a slot to become free (from a preceding write completing).

### Register 29: EPI Interrupt Mask (EPIIM), offset 0x210

This register is the interrupt mask set or clear register. For each interrupt source (read, write, and error), a mask value of 1 allows the interrupt source to trigger an interrupt to the interrupt controller; a mask value of 0 prevents the interrupt source from triggering an interrupt.

Note that interrupt masking has no effect on  $\mu$ DMA, which operates off the raw source of the read and write interrupts.

#### EPI Interrupt Mask (EPIIM)

Base 0x400D.0000  
 Offset 0x210  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													WRIM	RDIM	ERRIM	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	WRIM	R/W	0	Write Interrupt Mask  Value Description 1 WRRIS in the <b>EPIRIS</b> register is not masked and can trigger an interrupt to the interrupt controller. 0 WRRIS in the <b>EPIRIS</b> register is masked and does not cause an interrupt.
1	RDIM	R/W	0	Read Interrupt Mask  Value Description 1 RDRIS in the <b>EPIRIS</b> register is not masked and can trigger an interrupt to the interrupt controller. 0 RDRIS in the <b>EPIRIS</b> register is masked and does not cause an interrupt.
0	ERRIM	R/W	0	Error Interrupt Mask  Value Description 1 ERRIS in the <b>EPIRIS</b> register is not masked and can trigger an interrupt to the interrupt controller. 0 ERRIS in the <b>EPIRIS</b> register is masked and does not cause an interrupt.

## Register 30: EPI Raw Interrupt Status (EPIRIS), offset 0x214

This register is the raw interrupt status register. On a read, it gives the current state of each interrupt source. A write has no effect.

Note that raw status for read and write is set or cleared based on FIFO fullness as controlled by **EPIFIFOLVL**.

Raw status for error is held until the error is cleared by writing to the **EPIIC** register.

### EPI Raw Interrupt Status (EPIRIS)

Base 0x400D.0000

Offset 0x214

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													WRRIS	RDRIS	ERRIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	WRRIS	RO	0	Write Raw Interrupt Status  Value Description 1 The number of available entries in the WFIFO is within the range specified by the trigger level (the <code>WRFIFO</code> field in the <b>EPIFIFOLVL</b> register). 0 The number of available entries in the WFIFO is above the range specified by the trigger level.  This bit is cleared when the level in the WFIFO is above the trigger point programmed by the <code>WRFIFO</code> field.
1	RDRIS	RO	0	Read Raw Interrupt Status  Value Description 1 The number of valid entries in the NBRFIFO is within the range specified by the trigger level (the <code>RDFIFO</code> field in the <b>EPIFIFOLVL</b> register). 0 The number of valid entries in the NBRFIFO is below the range specified by the trigger level.  This bit is cleared when the level in the NBRFIFO is below the trigger point programmed by the <code>RDFIFO</code> field.

Bit/Field	Name	Type	Reset	Description				
0	ERRRIS	RO	0	<p>Error Raw Interrupt Status</p> <p>The error interrupt occurs in the following situations:</p> <ul style="list-style-type: none"> <li>■ <b>WFIFO Full.</b> For a full WFIFO to generate an error interrupt, the <code>WFERR</code> bit in the <b>EPIFIFOLVL</b> register must be set.</li> <li>■ <b>Read Stalled.</b> For a stalled read to generate an error interrupt, the <code>RSERR</code> bit in the <b>EPIFIFOLVL</b> register must be set.</li> <li>■ <b>Timeout.</b> If the <code>MAXWAIT</code> field in the <b>EPIGPCFG</b> register is configured to a value other than 0, a timeout error occurs when <code>iRDY</code> or <code>XFIFO</code> not-ready signals hold a transaction for more than the count in the <code>MAXWAIT</code> field.</li> </ul> <p>Value Description</p> <table border="0"> <tr> <td>1</td> <td>A WFIFO Full, a Read Stalled, or a Timeout error has occurred.</td> </tr> <tr> <td>0</td> <td>An error has not occurred.</td> </tr> </table> <p>To determine which error occurred, read the status of the <b>EPI Error Interrupt Status and Clear (EPIEISC)</b> register. This bit is cleared by writing a 1 to the bit in the <b>EPIEISC</b> register that caused the interrupt.</p>	1	A WFIFO Full, a Read Stalled, or a Timeout error has occurred.	0	An error has not occurred.
1	A WFIFO Full, a Read Stalled, or a Timeout error has occurred.							
0	An error has not occurred.							

## Register 31: EPI Masked Interrupt Status (EPIMIS), offset 0x218

This register is the masked interrupt status register. On read, it gives the current state of each interrupt source (read, write, and error) after being masked via the **EPIIM** register. A write has no effect.

The values returned are the ANDing of the **EPIIM** and **EPIRIS** registers. If a bit is set in this register, the interrupt is sent to the interrupt controller.

### EPI Masked Interrupt Status (EPIMIS)

Base 0x400D.0000

Offset 0x218

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													WRMIS	RDMIS	ERRMIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description						
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
2	WRMIS	RO	0	Write Masked Interrupt Status  <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>1</td> <td>The number of available entries in the WFIFO is within the range specified by the trigger level (the <b>WRFIFO</b> field in the <b>EPIFIFOLVL</b> register) and the <b>WRIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.</td> </tr> <tr> <td>0</td> <td>The number of available entries in the WFIFO is above the range specified by the trigger level or the interrupt is masked.</td> </tr> </table>	Value	Description	1	The number of available entries in the WFIFO is within the range specified by the trigger level (the <b>WRFIFO</b> field in the <b>EPIFIFOLVL</b> register) and the <b>WRIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.	0	The number of available entries in the WFIFO is above the range specified by the trigger level or the interrupt is masked.
Value	Description									
1	The number of available entries in the WFIFO is within the range specified by the trigger level (the <b>WRFIFO</b> field in the <b>EPIFIFOLVL</b> register) and the <b>WRIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.									
0	The number of available entries in the WFIFO is above the range specified by the trigger level or the interrupt is masked.									
1	RDMIS	RO	0	Read Masked Interrupt Status  <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>1</td> <td>The number of valid entries in the NBRFIFO is within the range specified by the trigger level (the <b>RDFIFO</b> field in the <b>EPIFIFOLVL</b> register) and the <b>RDIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.</td> </tr> <tr> <td>0</td> <td>The number of valid entries in the NBRFIFO is below the range specified by the trigger level or the interrupt is masked.</td> </tr> </table>	Value	Description	1	The number of valid entries in the NBRFIFO is within the range specified by the trigger level (the <b>RDFIFO</b> field in the <b>EPIFIFOLVL</b> register) and the <b>RDIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.	0	The number of valid entries in the NBRFIFO is below the range specified by the trigger level or the interrupt is masked.
Value	Description									
1	The number of valid entries in the NBRFIFO is within the range specified by the trigger level (the <b>RDFIFO</b> field in the <b>EPIFIFOLVL</b> register) and the <b>RDIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.									
0	The number of valid entries in the NBRFIFO is below the range specified by the trigger level or the interrupt is masked.									
0	ERRMIS	RO	0	Error Masked Interrupt Status  <table border="0"> <tr> <td>Value</td> <td>Description</td> </tr> <tr> <td>1</td> <td>A WFIFO Full, a Read Stalled, or a Timeout error has occurred and the <b>ERIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.</td> </tr> <tr> <td>0</td> <td>An error has not occurred or the interrupt is masked.</td> </tr> </table>	Value	Description	1	A WFIFO Full, a Read Stalled, or a Timeout error has occurred and the <b>ERIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.	0	An error has not occurred or the interrupt is masked.
Value	Description									
1	A WFIFO Full, a Read Stalled, or a Timeout error has occurred and the <b>ERIM</b> bit in the <b>EPIIM</b> register is set, triggering an interrupt to the interrupt controller.									
0	An error has not occurred or the interrupt is masked.									

### Register 32: EPI Error Interrupt Status and Clear (EPIEISC), offset 0x21C

This register is used to clear a pending error interrupt. If any of these bits are set, the `ERRRIS` bit in the `EPIRIS` register is set, and an EPI controller error is sent to the interrupt controller if the `ERIM` bit in the `EPIIM` register is set. Clearing any defined bit has no effect; setting a bit clears the error source and the raw error returns to 0. Note that writing to this register and reading back immediately (pipelined by the processor) returns the old register contents. One cycle is needed between write and read.

#### EPI Error Interrupt Status and Clear (EPIEISC)

Base 0x400D.0000  
 Offset 0x21C  
 Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													WTFULL	RSTALL	TOUT	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	WTFULL	R/W1C	0	Write FIFO Full Error  Value Description 1 The <code>WFERR</code> bit is enabled and a write is stalled due to the WFIFO being full. 0 The <code>WFERR</code> bit is not enabled or no writes are stalled.  Writing a 1 to this bit clears it and the <code>WFERR</code> bit in the <code>EPIFIFOLVL</code> register.
1	RSTALL	R/W1C	0	Read Stalled Error  Value Description 1 The <code>RSERR</code> bit is enabled and a pending read is stalled due to writes in the WFIFO. 0 The <code>RSERR</code> bit is not enabled or no pending reads are stalled.  Writing a 1 to this bit clears it and the <code>RSERR</code> bit in the <code>EPIFIFOLVL</code> register.



---

Bit/Field	Name	Type	Reset	Description
0	TOUT	R/W1C	0	<p>Timeout Error</p> <p>This bit is the timeout error source. The timeout error occurs when the iRDY or XFIFO not-ready signals hold a transaction for more than the count in the MAXWAIT field (when not 0).</p> <p>Value Description</p> <p>1 A timeout error has occurred.</p> <p>0 No timeout error has occurred.</p> <p>Writing a 1 to bit this clears it.</p>

## 12 General-Purpose Timers

Programmable timers can be used to count or time external events that drive the Timer input pins. The Stellaris® General-Purpose Timer Module (GPTM) contains four GPTM blocks (Timer 0, Timer 1, Timer 2, and Timer 3). Each GPTM block provides two 16-bit timers/counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or configured to operate as one 32-bit timer or one 32-bit Real-Time Clock (RTC). Timers can also be used to trigger  $\mu$ DMA transfers.

In addition, timers can be used to trigger analog-to-digital conversions (ADC). The ADC trigger signals from all of the general-purpose timers are ORed together before reaching the ADC module, so only one timer should be used to trigger ADC events.

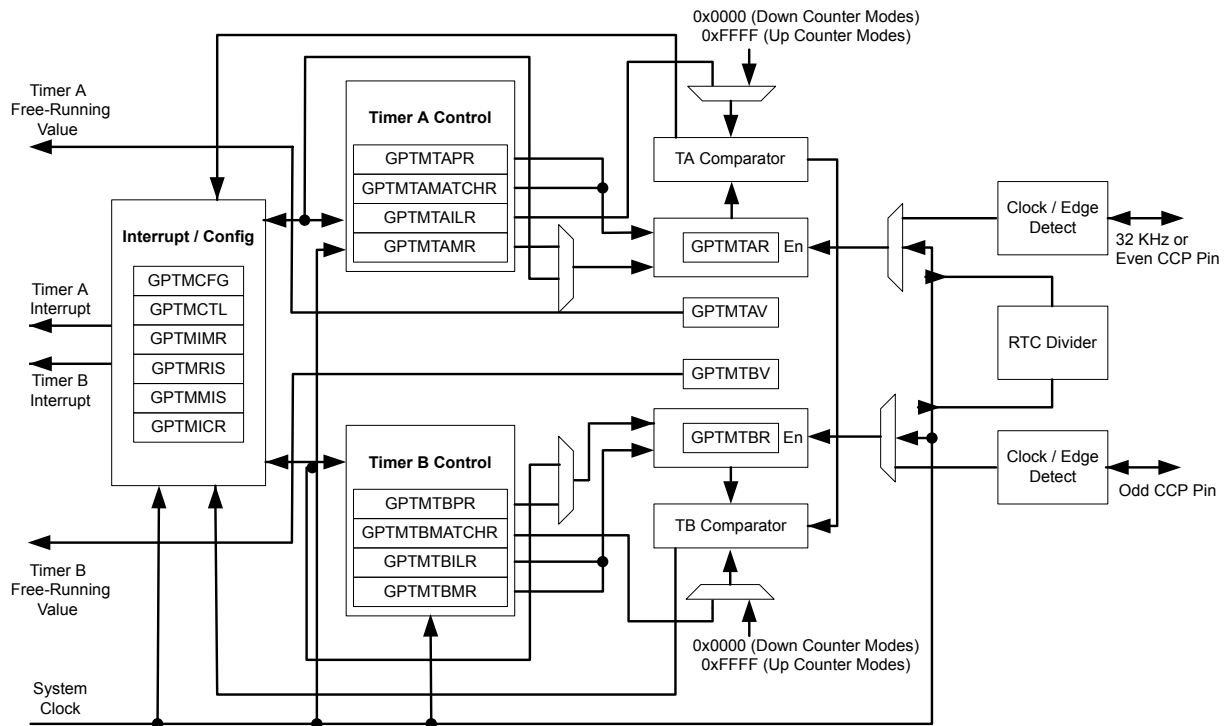
The GPT Module is one timing resource available on the Stellaris® microcontrollers. Other timer resources include the System Timer (SysTick) (see “System Timer (SysTick)” on page 59).

The General-Purpose Timer Module (GPTM) contains four GPTM blocks with the following functional options:

- Count up or down
- 16- or 32-bit programmable one-shot timer
- 16- or 32-bit programmable periodic timer
- 16-bit general-purpose timer with an 8-bit prescaler
- 32-bit Real-Time Clock (RTC) when using an external 32.768-KHz clock as the input
- Eight Capture Compare PWM pins (CCP)
- Daisy chaining of timer modules to allow a single timer to initiate multiple timing events
- ADC event trigger
- User-enabled stalling when the controller asserts CPU Halt flag during debug (excluding RTC mode)
- 16-bit input-edge count- or time-capture modes
- 16-bit PWM mode with software-programmable output inversion of the PWM signal
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine.
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt

## 12.1 Block Diagram

Figure 12-1. GPTM Module Block Diagram



**Note:** In Figure 12-1 on page 411, the specific Capture Compare PWM (CCP) pins available depend on the Stellaris® device. See Table 12-1 on page 411 for the available CCP pins and their timer assignments

Table 12-1. Available CCP Pins

Timer	16-Bit Up/Down Counter	Even CCP Pin	Odd CCP Pin
Timer 0	Timer A	CCP0	-
	Timer B	-	CCP1
Timer 1	Timer A	CCP2	-
	Timer B	-	CCP3
Timer 2	Timer A	CCP4	-
	Timer B	-	CCP5
Timer 3	Timer A	CCP6	-
	Timer B	-	CCP7

## 12.2 Signal Description

Table 12-2 on page 412 lists the external signals of the GP Timer module and describes the function of each. The GP Timer signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for these GP Timer signals. The `AFSEL` bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) should be set to choose the GP Timer function.

The number in parentheses is the encoding that must be programmed into the  $PMC_n$  field in the **GPIO Port Control (GPIOCTL)** register (page 328) to assign the GP Timer signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 288.

**Table 12-2. Signals for General-Purpose Timers**

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
CCP0	13	PD3 (4)	I/O	TTL	Capture/Compare/PWM 0.
	22	PC7 (4)			
	23	PC6 (6)			
	39	PJ2 (9)			
	58	PF4 (1)			
	66	PB0 (1)			
	72	PB2 (5)			
	91	PB5 (4)			
	97	PD4 (1)			
CCP1	24	PC5 (1)	I/O	TTL	Capture/Compare/PWM 1.
	25	PC4 (9)			
	34	PA6 (2)			
	43	PF6 (1)			
	67	PB1 (4)			
	90	PB6 (1)			
	96	PE3 (1)			
		100			
CCP2	6	PE4 (6)	I/O	TTL	Capture/Compare/PWM 2.
	11	PD1 (10)			
	25	PC4 (5)			
	46	PF5 (1)			
	67	PB1 (1)			
	75	PE1 (4)			
	91	PB5 (6)			
		95			
	98	PD5 (1)			
CCP3	6	PE4 (1)	I/O	TTL	Capture/Compare/PWM 3.
	23	PC6 (1)			
	24	PC5 (5)			
	35	PA7 (7)			
	41	PG4 (1)			
	61	PF1 (10)			
	72	PB2 (4)			
		74			
	97	PD4 (2)			
CCP4	22	PC7 (1)	I/O	TTL	Capture/Compare/PWM 4.
	25	PC4 (6)			
	35	PA7 (2)			
	42	PF7 (1)			
	95	PE2 (1)			
		98			
CCP5	5	PE5 (1)	I/O	TTL	Capture/Compare/PWM 5.
	12	PD2 (4)			
	25	PC4 (1)			
	36	PG7 (8)			
	40	PG5 (1)			
	90	PB6 (6)			
		91			

Table 12-2. Signals for General-Purpose Timers (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
CCP6	10	PD0 (6)	I/O	TTL	Capture/Compare/PWM 6.
	12	PD2 (2)			
	75	PE1 (5)			
	86	PH0 (1)			
	91	PB5 (3)			
CCP7	11	PD1 (6)	I/O	TTL	Capture/Compare/PWM 7.
	13	PD3 (2)			
	85	PH1 (1)			
	90	PB6 (2)			
	96	PE3 (5)			

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 12.3 Functional Description

The main components of each GPTM block are two free-running 16-bit up/down counters (referred to as Timer A and Timer B), two 16-bit match registers, 2 16-bit shadow registers, and two 16-bit load/initialization registers and their associated control functions. The exact functionality of each GPTM is controlled by software and configured through the register interface.

Software configures the GPTM using the **GPTM Configuration (GPTMCFG)** register (see page 425), the **GPTM Timer A Mode (GPTMTAMR)** register (see page 426), and the **GPTM Timer B Mode (GPTMTBMR)** register (see page 428). When in one of the 32-bit modes, the timer can only act as a 32-bit timer. However, when configured in 16-bit mode, the GPTM can have its two 16-bit timers configured in any combination of the 16-bit modes.

### 12.3.1 GPTM Reset Conditions

After reset has been applied to the GPTM module, the module is in an inactive state, and all control registers are cleared and in their default states. Counters Timer A and Timer B are initialized to 0xFFFF, along with their corresponding load registers: the **GPTM Timer A Interval Load (GPTMTAILR)** register (see page 443) and the **GPTM Timer B Interval Load (GPTMTBILR)** register (see page 444) and shadow registers: the **GPTM Timer A Value (GPTMTAV)** register (see page 451) and the **GPTM Timer B Value (GPTMTBV)** register (see page 452). The prescale counters are initialized to 0x00: the **GPTM Timer A Prescale (GPTMTAPR)** register (see page 447) and the **GPTM Timer B Prescale (GPTMTBPR)** register (see page 448).

### 12.3.2 32-Bit Timer Operating Modes

This section describes the three GPTM 32-bit timer modes (One-Shot, Periodic, and RTC) and their configurations.

The GPTM is placed into 32-bit mode by writing a 0x0 (One-Shot/Periodic 32-bit timer mode) or a 0x1 (RTC mode) to the **GPTMCFG** bit field in the **GPTM Configuration (GPTMCFG)** register. In both configurations, certain GPTM registers are concatenated to form pseudo 32-bit registers. These registers include:

- **GPTM Timer A Interval Load (GPTMTAILR)** register [15:0], see page 443
- **GPTM Timer B Interval Load (GPTMTBILR)** register [15:0], see page 444
- **GPTM Timer A (GPTMTAR)** register [15:0], see page 449
- **GPTM Timer B (GPTMTBR)** register [15:0], see page 450

- **GPTM Timer A Value (GPTMTAV)** register [15:0], see page 451
- **GPTM Timer B Value (GPTMTBV)** register [15:0], see page 452

In the 32-bit modes, the GPTM translates a 32-bit write access to **GPTMTAILR** into a write access to both **GPTMTAILR** and **GPTMTBILR**. The resulting word ordering for such a write operation is:

```
GPTMTBILR[15:0]:GPTMTAILR[15:0]
```

Likewise, a 32-bit read access to **GPTMTAR** returns the value:

```
GPTMTBR[15:0]:GPTMTAR[15:0]
```

A 32-bit read access to **GPTMTAV** returns the value:

```
GPTMTBV[15:0]:GPTMTAV[15:0]
```

### 12.3.2.1 32-Bit One-Shot/Periodic Timer Mode

In 32-bit one-shot and periodic timer modes, the concatenated versions of the Timer A and Timer B registers are configured as a 32-bit up or down counter. The selection of one-shot or periodic mode is determined by the value written to the **TAMR** field of the **GPTM Timer A Mode (GPTMTAMR)** register (see page 426); there is no need to write to the **GPTM Timer B Mode (GPTMTBMR)** register.

When software sets the **TAEN** bit in the **GPTM Control (GPTMCTL)** register (see page 430), the timer begins counting up or down from its preloaded value. Alternatively, if the **TnWOT** bit is set in the **GPTMTnMR** register, once the **TnEN** bit is set, the timer waits for a trigger to begin counting (see “Wait-for-Trigger Mode” on page 419).

Once the time-out event (0x0000.0000 when counting down, 0xFFFF.FFFF when counting up) is reached, the timer reloads its start value from the concatenated **GPTMTAILR** on the next cycle. If configured to be a one-shot timer, the timer stops counting and clears the **TAEN** bit in the **GPTMCTL** register. If configured as a periodic timer, it continues counting. If the **TnSNAPS** bit in the **GPTMTnMR** register is set, the actual free-running value of the timer at the time-out event is loaded into the **GPTMTAR** register. In this manner, software can determine the time elapsed from the interrupt assertion to the ISR entry.

In addition to reloading the count value, the GPTM generates interrupts and triggers when it reaches the time-out event. The GPTM sets the **TATORIS** bit in the **GPTM Raw Interrupt Status (GPTMRIS)** register (see page 435), and holds it until it is cleared by writing the **GPTM Interrupt Clear (GPTMICR)** register (see page 441). If the time-out interrupt is enabled in the **GPTM Interrupt Mask (GPTIMR)** register (see page 433), the GPTM also sets the **TATOMIS** bit in the **GPTM Masked Interrupt Status (GPTMMIS)** register (see page 438). By setting the **TAMIE** bit in the **GPTMTAMR** register, an interrupt can also be generated when the Timer A value equals the value loaded into the **GPTM Timer A Match (GPTMTAMATCH)** register. This interrupt has the same status, masking, and clearing functions as the time-out interrupt. The ADC trigger is enabled by setting the **TAOTE** bit in **GPTMCTL**. The  $\mu$ DMA trigger is enabled by configuring and enabling the appropriate  $\mu$ DMA channel. See “Channel Configuration” on page 234.

If software reloads the **GPTMTAILR** register while the counter is running, the counter loads the new value on the next clock cycle and continues counting from the new value.

If the **TASTALL** bit in the **GPTMCTL** register is set, the timer freezes counting until the bit is cleared.

### 12.3.2.2 32-Bit Real-Time Clock Timer Mode

In Real-Time Clock (RTC) mode, the concatenated versions of the Timer A and Timer B registers are configured as a 32-bit up-counter. When RTC mode is selected for the first time after reset, the counter is loaded with a value of 0x0000.0001. All subsequent load values must be written to the **GPTM Timer A Interval Load (GPTMTAILR)** register (see page 443).

The input clock on the CCP0, CCP2, or CCP4 signal is required to be 32.768 KHz in RTC mode. The clock signal is then divided down to a 1-Hz rate and is passed along to the input of the 32-bit counter.

When software writes the TAEN bit in the **GPTMCTL** register, the counter starts counting up from its preloaded value of 0x0000.0001. When the current count value matches the preloaded value in the **GPTMTAMATCHR** register, the GPTM asserts the RTCRIS bit in **GPTMRIS** and continues counting until either a hardware reset, or it is disabled by software (clearing the TAEN bit). If the RTC interrupt is enabled in **GPTIMR**, the GPTM also sets the RTCMIS bit in **GPTMISR** and generates a controller interrupt. The status flags are cleared by writing the RTCCINT bit in **GPTMICR**.

In addition to generating interrupts, a  $\mu$ DMA trigger can be generated. The  $\mu$ DMA trigger is enabled by configuring and enabling the appropriate  $\mu$ DMA channel. See “Channel Configuration” on page 234.

If the TASTALL and/or TBSTALL bits in the **GPTMCTL** register are set, the timer does not freeze if the RTCEN bit is set in **GPTMCTL**.

### 12.3.3 16-Bit Timer Operating Modes

The GPTM is placed into global 16-bit mode by writing a value of 0x4 to the **GPTM Configuration (GPTMCFG)** register (see page 425). This section describes each of the GPTM 16-bit modes of operation. Timer A and Timer B have identical modes, so a single description is given using an *n* to reference both.

#### 12.3.3.1 16-Bit One-Shot/Periodic Timer Mode

In 16-bit one-shot and periodic timer modes, the timer is configured as a 16-bit up or down-counter with an optional 8-bit prescaler that effectively extends the counting range of the timer to 24 bits. The selection of one-shot or periodic mode is determined by the value written to the TnMR field of the **GPTMTnMR** register. The optional prescaler is loaded into the **GPTM Timer n Prescale (GPTMTnPR)** register.

When software sets the TnEN bit in the **GPTMCTL** register, the timer begins counting up or down from its preloaded value. Alternatively, if the TnWOT bit is set in the **GPTMTnMR** register, once the TnEN bit is set, the timer waits for a trigger to begin counting (see “Wait-for-Trigger Mode” on page 419).

Once the time-out event (0x0000 when counting down, 0xFFFF when counting up) is reached, the timer reloads its start value from **GPTMTnILR** and **GPTMTnPR** on the next cycle. If configured to be a one-shot timer, the timer stops counting and clears the TnEN bit in the **GPTMCTL** register. If configured as a periodic timer, it continues counting. If the TnSNAPS bit in the **GPTMTnMR** register is set, the actual free-running value of the timer at the time-out event is loaded into the **GPTMTAR** register. In this manner, software can determine the time elapsed from the interrupt assertion to the ISR entry.

In addition to reloading the count value, the timer generates interrupts and triggers when it reaches the time-out event. The GPTM sets the TnTORIS bit in the **GPTMRIS** register, and holds it until it is cleared by writing the **GPTMICR** register. If the time-out interrupt is enabled in **GPTIMR**, the GPTM also sets the TnTOMIS bit in **GPTMISR** and generates a controller interrupt. By setting the TnMIE bit in the **GPTMTnMR** register, an interrupt can also be generated when the timer value equals the value loaded into the **GPTM Timer n Match (GPTMTnMATCH)** register. This interrupt

has the same status, masking, and clearing functions as the time-out interrupt. The ADC trigger is enabled by setting the **TnOTE** bit in the **GPTMCTL** register. The  $\mu$ DMA trigger is enabled by configuring and enabling the appropriate  $\mu$ DMA channel. See “Channel Configuration” on page 234.

If software reloads the **GPTMTAILR** register while the counter is running, the counter loads the new value on the next clock cycle and continues counting from the new value.

If the **TnSTALL** bit in the **GPTMCTL** register is set, the timer freezes counting until the bit is cleared.

The following example shows a variety of configurations for a 16-bit free-running timer while using the prescaler. All values assume a 50-MHz clock with  $T_c=20$  ns (clock period).

**Table 12-3. 16-Bit Timer With Prescaler Configurations**

Prescale	#Clock ( $T_c$ ) <sup>a</sup>	Max Time	Units
00000000	1	1.3107	mS
00000001	2	2.6214	mS
00000010	3	3.9321	mS
-----	--	--	--
11111100	254	332.9229	mS
11111110	255	334.2336	mS
11111111	256	335.5443	mS

a.  $T_c$  is the clock period.

### 12.3.3.2 16-Bit Input Edge-Count Mode

**Note:** For rising-edge detection, the input signal must be High for at least two system clock periods following the rising edge. Similarly, for falling-edge detection, the input signal must be Low for at least two system clock periods following the falling edge. Based on this criteria, the maximum input frequency for edge detection is 1/4 of the system frequency.

In Edge-Count mode, the timer is configured as a 16-bit down-counter with an optional 8-bit prescaler that effectively extends the counting range of the timer to 24 bits. In this mode, the timer is capable of capturing three types of events: rising edge, falling edge, or both. To place the timer in Edge-Count mode, the **TnCMR** bit of the **GPTMTnMR** register must be cleared. The type of edge that the timer counts is determined by the **TnEVENT** fields of the **GPTMCTL** register. During initialization, the **GPTM Timer n Match (GPTMTnMATCHR)** register is configured so that the difference between the value in the **GPTMTnILR** register and the **GPTMTnMATCHR** register equals the number of edge events that must be counted. The optional prescaler is loaded into the **GPTM Timer n Prescale (GPTMTnPR)** register.

When software writes the **TnEN** bit in the **GPTM Control (GPTMCTL)** register, the timer is enabled for event capture. Each input event on the **CCP** pin decrements the counter by 1 until the event count matches **GPTMTnMATCHR**. When the counts match, the GPTM asserts the **CnMRIS** bit in the **GPTMRIS** register (and the **CnMMIS** bit, if the interrupt is not masked).

In addition to generating interrupts, a  $\mu$ DMA trigger can be generated. The  $\mu$ DMA trigger is enabled by configuring and enabling the appropriate  $\mu$ DMA channel. See “Channel Configuration” on page 234.

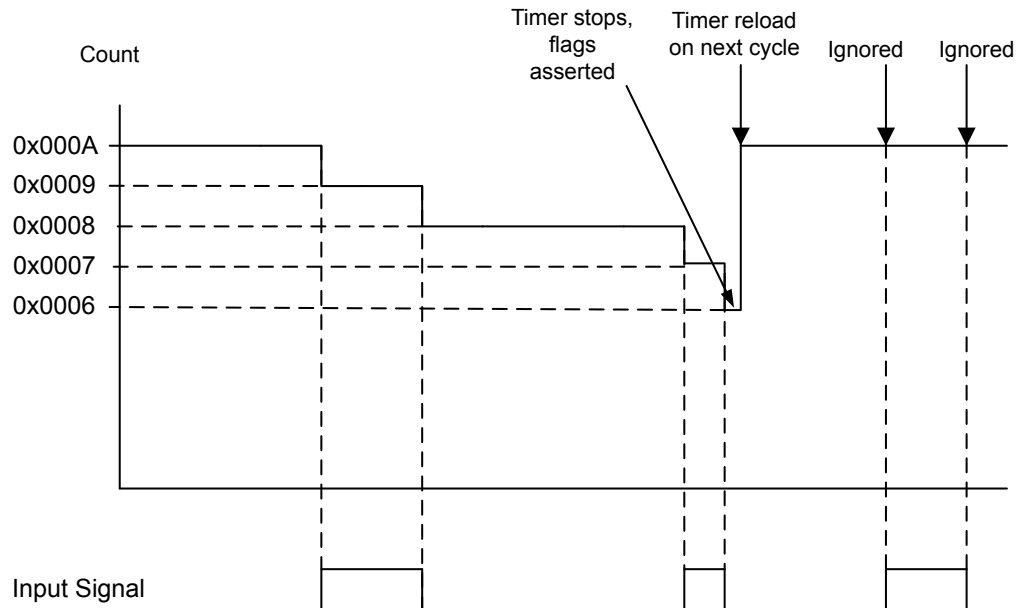
The counter is then reloaded using the value in **GPTMTnILR**, and stopped because the GPTM automatically clears the **TnEN** bit in the **GPTMCTL** register. Once the event count has been reached, all further events are ignored until **TnEN** is re-enabled by software. The **GPTMTnV** contains the free-running timer value and can be read to determine the time that elapsed between the interrupt assertion and the entry into the ISR.



Figure 12-2 on page 417 shows how Input Edge-Count mode works. In this case, the timer start value is set to **GPTMnILR** = 0x000A and the match value is set to **GPTMnMATCHR** = 0x0006 so that four edge events are counted. The counter is configured to detect both edges of the input signal.

Note that the last two edges are not counted since the timer automatically clears the **TnEN** bit after the current count matches the value in the **GPTMnMR** register.

**Figure 12-2. 16-Bit Input Edge-Count Mode Example**



### 12.3.3.3 16-Bit Input Edge-Time Mode

**Note:** For rising-edge detection, the input signal must be High for at least two system clock periods following the rising edge. Similarly, for falling edge detection, the input signal must be Low for at least two system clock periods following the falling edge. Based on this criteria, the maximum input frequency for edge detection is 1/4 of the system frequency.

In Edge-Time mode, the timer is configured as a 16-bit free-running down-counter with an optional 8-bit prescaler that effectively extends the counting range of the timer to 24 bits. In this mode, the timer is initialized to the value loaded in the **GPTMTnILR** register (or 0xFFFF at reset). This mode allows for event capture of either rising or falling edges, but not both. The timer is placed into Edge-Time mode by setting the **TnCMR** bit in the **GPTMTnMR** register, and the type of event that the timer captures is determined by the **TnEVENT** fields of the **GPTMCnTL** register. The optional prescaler is loaded into the **GPTM Timer n Prescale (GPTMTnPR)** register.

When software writes the **TnEN** bit in the **GPTMCTL** register, the timer is enabled for event capture. When the selected input event is detected, the current **Tn** counter value is captured in the **GPTMTnR** register and is available to be read by the microcontroller. The GPTM then asserts the **CnERIS** bit (and the **CnEMIS** bit, if the interrupt is not masked). The **GPTMTnV** is the free-running value of the timer and can be read to determine the time that elapsed between the interrupt assertion and the entry into the ISR.

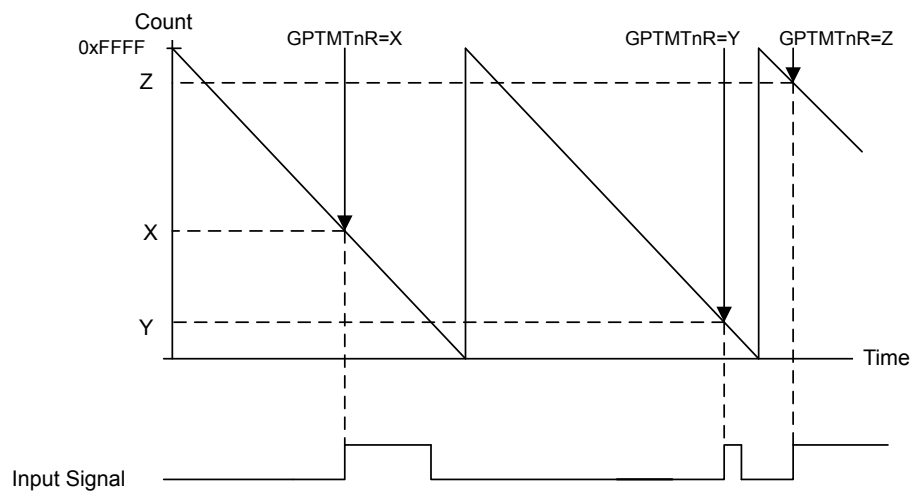
In addition to generating interrupts, a  $\mu$ DMA trigger can be generated. The  $\mu$ DMA trigger is enabled by configuring and enabling the appropriate  $\mu$ DMA channel. See “Channel Configuration” on page 234.

After an event has been captured, the timer does not stop counting. It continues to count until the  $TnEN$  bit is cleared. When the timer reaches the 0x0000 state, it is reloaded with the value from the **GPTMnILR** register.

Figure 12-3 on page 418 shows how input edge timing mode works. In the diagram, it is assumed that the start value of the timer is the default value of 0xFFFF, and the timer is configured to capture rising edge events.

Each time a rising edge event is detected, the current count value is loaded into the **GPTMTnR** register, and is held there until another rising edge is detected (at which point the new count value is loaded into **GPTMTnR**).

**Figure 12-3. 16-Bit Input Edge-Time Mode Example**



#### 12.3.3.4 16-Bit PWM Mode

**Note:** The prescaler is not available in 16-Bit PWM mode.

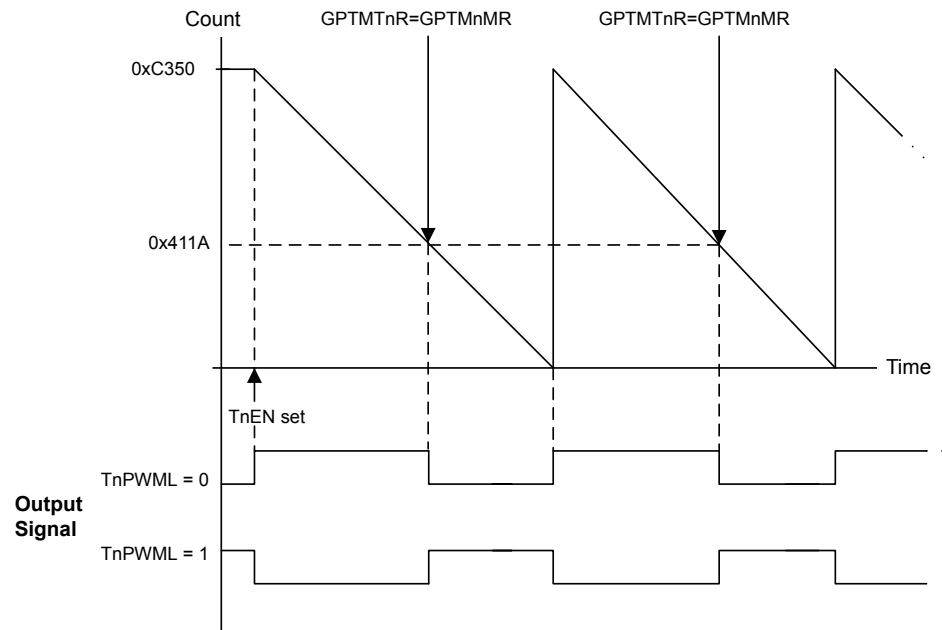
The GPTM supports a simple PWM generation mode. In PWM mode, the timer is configured as a down-counter with a start value (and thus period) defined by **GPTMTnILR**. PWM mode is enabled with the **GPTMTnMR** register by setting the  $TnAMS$  bit to 0x1, the  $TnCMR$  bit to 0x0, and the  $TnMR$  field to 0x2.

When software writes the  $TnEN$  bit in the **GPTMCTL** register, the counter begins counting down until it reaches the 0x0000 state. On the next counter cycle, the counter reloads its start value from **GPTMTnILR** and continues counting until disabled by software clearing the  $TnEN$  bit in the **GPTMCTL** register. No interrupts or status bits are asserted in PWM mode.

The output PWM signal asserts when the counter is at the value of the **GPTMTnILR** register (its start state), and is deasserted when the counter value equals the value in the **GPTM Timer n Match Register (GPTMnMATCHR)**. Software has the capability of inverting the output PWM signal by setting the  $TnPWML$  bit in the **GPTMCTL** register.

Figure 12-4 on page 419 shows how to generate an output PWM with a 1-ms period and a 66% duty cycle assuming a 50-MHz input clock and  $TnPWML = 0$  (duty cycle would be 33% for the  $TnPWML = 1$  configuration). For this example, the start value is **GPTMnILR**=0xC350 and the match value is **GPTMnMR**=0x411A.

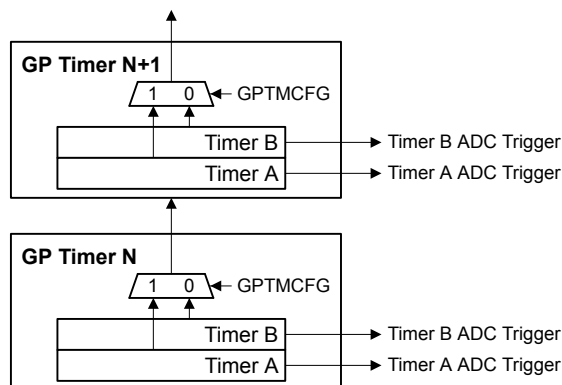
Figure 12-4. 16-Bit PWM Mode Example



### 12.3.3.5 Wait-for-Trigger Mode

The Wait-for-Trigger mode allows daisy chaining of the timer modules such that once configured, a single timer can initiate multiple timing events using the Timer triggers. Wait-for-Trigger mode is enabled by setting the  $T_{nWOT}$  bit in the **GPTMTnMR** register. When the  $T_{nWOT}$  bit is set, Timer N+1 does not begin counting until the timer in the previous position in the daisy chain (Timer N) reaches its time-out event. The daisy chain is configured such that GPTM1 always follows GPTM0, GPTM2 follows GPTM1, and so on. If Timer A is in 32-bit mode (controlled by the  $GPTMCFG$  bit in the **GPTMCFG** register), it triggers Timer A in the next module. If Timer A is in 16-bit mode, it triggers Timer B in the same module, and Timer B triggers Timer A in the next module. Care must be taken that the  $T_{AWOT}$  bit is never set in GPTM0. Figure 12-5 on page 419 shows how the  $GPTMCFG$  bit affects the daisy chain. This function is valid for both one-shot and periodic modes.

Figure 12-5. Timer Daisy Chain



### 12.3.4 DMA Operation

The timers each have a dedicated  $\mu$ DMA channel and can provide a request signal to the  $\mu$ DMA controller. The request is a burst type and occurs whenever a timer raw interrupt condition occurs. The arbitration size of the  $\mu$ DMA transfer should be set to the amount of data that should be transferred whenever a timer event occurs.

For example, to transfer 256 items, 8 items at a time every 10 ms, configure a timer to generate a periodic timeout at 10 ms. Configure the  $\mu$ DMA transfer for a total of 256 items, with a burst size of 8 items. Each time the timer times out, the  $\mu$ DMA controller transfers 8 items, until all 256 items have been transferred.

No other special steps are needed to enable Timers for  $\mu$ DMA operation. Refer to “Micro Direct Memory Access ( $\mu$ DMA)” on page 230 for more details about programming the  $\mu$ DMA controller.

## 12.4 Initialization and Configuration

To use the general-purpose timers, the peripheral clock must be enabled by setting the `TIMER0`, `TIMER1`, `TIMER2`, and `TIMER3` bits in the **RCGC1** register (see page 149). If using any CCP pins, the clock to the appropriate GPIO module must be enabled via the **RCGC2** register in the System Control module (see page 158). To find out which GPIO port to enable, refer to Table 20-4 on page 717. Configure the `PMCn` fields in the **GPIOPCTL** register to assign the CCP signals to the appropriate pins (see page 328 and Table 20-5 on page 722).

This section shows module initialization and configuration examples for each of the supported timer modes.

### 12.4.1 32-Bit One-Shot/Periodic Timer Mode

The GPTM is configured for 32-bit One-Shot and Periodic modes by the following sequence:

1. Ensure the timer is disabled (the `TAEN` bit in the **GPTMCTL** register is cleared) before making any changes.
2. Write the **GPTM Configuration Register (GPTMCFG)** with a value of `0x0000.0000`.
3. Configure the `TAMR` field in the **GPTM Timer A Mode Register (GPTMTAMR)**:
  - a. Write a value of `0x1` for One-Shot mode.
  - b. Write a value of `0x2` for Periodic mode.
4. Optionally configure the `TASNAPS`, `TAWOT`, `TAMTE`, and `TACDIR` bits in the **GPTMTAMR** register to select whether to capture the value of the free-running timer at time-out, use an external trigger to start counting, configure an additional trigger or interrupt, and count up or down.
5. Load the start value into the **GPTM Timer A Interval Load Register (GPTMTAILR)**.
6. If interrupts are required, set the appropriate bits in the **GPTM Interrupt Mask Register (GPTMIMR)**.
7. Set the `TAEN` bit in the **GPTMCTL** register to enable the timer and start counting.
8. Poll the **GPTMRIS** register or wait for the interrupt to be generated (if enabled). In both cases, the status flags are cleared by writing a 1 to the appropriate bit of the **GPTM Interrupt Clear Register (GPTMICR)**.

If the `TAMIE` bit in the **GPTMTAMR** register is set, the `RTCRES` bit in the **GPTMRIS** register is set, and the timer continues counting. In One-Shot mode, the timer stops counting after the time-out event. To re-enable the timer, repeat the sequence. A timer configured in Periodic mode reloads the timer and continues counting after the time-out event.

## 12.4.2 32-Bit Real-Time Clock (RTC) Mode

To use the RTC mode, the timer must have a 32.768-KHz input signal on the `CCP0`, `CCP2`, or `CCP4` signal. To enable the RTC feature, follow these steps:

1. Ensure the timer is disabled (the `TAEN` bit is cleared) before making any changes.
2. Write the **GPTM Configuration Register (GPTMCFG)** with a value of `0x0000.0001`.
3. Write the match value to the **GPTM Timer A Match Register (GPTMTAMATCHR)**.
4. Set/clear the `RTCEN` bit in the **GPTM Control Register (GPTMCTL)** as needed.
5. If interrupts are required, set the `RTCIM` bit in the **GPTM Interrupt Mask Register (GPTMIMR)**.
6. Set the `TAEN` bit in the **GPTMCTL** register to enable the timer and start counting.

When the timer count equals the value in the **GPTMTAMATCHR** register, the counter is re-loaded with `0x0000.0000` and begins counting. If an interrupt is enabled, it does not have to be cleared.

## 12.4.3 16-Bit One-Shot/Periodic Timer Mode

A timer is configured for 16-bit One-Shot and Periodic modes by the following sequence:

1. Ensure the timer is disabled (the `TnEN` bit is cleared) before making any changes.
2. Write the **GPTM Configuration Register (GPTMCFG)** with a value of `0x0000.0004`.
3. Set the `TnMR` field in the **GPTM Timer Mode (GPTMTnMR)** register:
  - a. Write a value of `0x1` for One-Shot mode.
  - b. Write a value of `0x2` for Periodic mode.
4. Optionally configure the `TnSNAPS`, `TnWOT`, `TnMTE` and `TnCDIR` bits in the **GPTMTnMR** register to select whether to capture the value of the free-running timer at time-out, use an external trigger to start counting, configure an additional trigger or interrupt, and count up or down.
5. If a prescaler is to be used, write the prescale value to the **GPTM Timer n Prescale Register (GPTMTnPR)**.
6. Load the start value into the **GPTM Timer Interval Load Register (GPTMTnILR)**.
7. If interrupts are required, set the appropriate bit in the **GPTM Interrupt Mask Register (GPTMIMR)**.
8. Set the `TnEN` bit in the **GPTM Control Register (GPTMCTL)** to enable the timer and start counting.

9. Poll the **GPTMRIS** register or wait for the interrupt to be generated (if enabled). In both cases, the status flags are cleared by writing a 1 to the appropriate bit of the **GPTM Interrupt Clear Register (GPTMICR)**.

If the  $TnMIE$  bit in the **GPTMTnMR** register is set, the  $RTCRES$  bit in the **GPTMRIS** register is set, and the timer continues counting. In One-Shot mode, the timer stops counting after the time-out event. To re-enable the timer, repeat the sequence. A timer configured in Periodic mode reloads the timer and continues counting after the time-out event.

#### 12.4.4 16-Bit Input Edge-Count Mode

A timer is configured to Input Edge-Count mode by the following sequence:

1. Ensure the timer is disabled (the  $TnEN$  bit is cleared) before making any changes.
2. Write the **GPTM Configuration (GPTMCFG)** register with a value of 0x0000.0004.
3. In the **GPTM Timer Mode (GPTMTnMR)** register, write the  $TnCMR$  field to 0x0 and the  $TnMR$  field to 0x3.
4. Configure the type of event(s) that the timer captures by writing the  $TnEVENT$  field of the **GPTM Control (GPTMCTL)** register.
5. If a prescaler is to be used, write the prescale value to the **GPTM Timer n Prescale Register (GPTMTnPR)**.
6. Load the timer start value into the **GPTM Timer n Interval Load (GPTMTnILR)** register.
7. Load the event count into the **GPTM Timer n Match (GPTMTnMATCHR)** register.
8. If interrupts are required, set the  $CnMIM$  bit in the **GPTM Interrupt Mask (GPTMIMR)** register.
9. Set the  $TnEN$  bit in the **GPTMCTL** register to enable the timer and begin waiting for edge events.
10. Poll the  $CnMRIS$  bit in the **GPTMRIS** register or wait for the interrupt to be generated (if enabled). In both cases, the status flags are cleared by writing a 1 to the  $CnMCINT$  bit of the **GPTM Interrupt Clear (GPTMICR)** register.

In Input Edge-Count Mode, the timer stops after the programmed number of edge events has been detected. To re-enable the timer, ensure that the  $TnEN$  bit is cleared and repeat step 4 on page 422 through step 9 on page 422.

#### 12.4.5 16-Bit Input Edge Timing Mode

A timer is configured to Input Edge Timing mode by the following sequence:

1. Ensure the timer is disabled (the  $TnEN$  bit is cleared) before making any changes.
2. Write the **GPTM Configuration (GPTMCFG)** register with a value of 0x0000.0004.
3. In the **GPTM Timer Mode (GPTMTnMR)** register, write the  $TnCMR$  field to 0x1 and the  $TnMR$  field to 0x3.
4. Configure the type of event that the timer captures by writing the  $TnEVENT$  field of the **GPTM Control (GPTMCTL)** register.

5. If a prescaler is to be used, write the prescale value to the **GPTM Timer n Prescale Register (GPTMTnPR)**.
6. Load the timer start value into the **GPTM Timer n Interval Load (GPTMTnILR)** register.
7. If interrupts are required, set the **CnEIM** bit in the **GPTM Interrupt Mask (GPTMIMR)** register.
8. Set the **TnEN** bit in the **GPTM Control (GPTMCTL)** register to enable the timer and start counting.
9. Poll the **CnERIS** bit in the **GPTMRIS** register or wait for the interrupt to be generated (if enabled). In both cases, the status flags are cleared by writing a 1 to the **CnECINT** bit of the **GPTM Interrupt Clear (GPTMICR)** register. The time at which the event happened can be obtained by reading the **GPTM Timer n (GPTMTnR)** register.

In Input Edge Timing mode, the timer continues running after an edge event has been detected, but the timer interval can be changed at any time by writing the **GPTMTnILR** register. The change takes effect at the next cycle after the write.

### 12.4.6 16-Bit PWM Mode

A timer is configured to PWM mode using the following sequence:

1. Ensure the timer is disabled (the **TnEN** bit is cleared) before making any changes.
2. Write the **GPTM Configuration (GPTMCFG)** register with a value of 0x0000.0004.
3. In the **GPTM Timer Mode (GPTMTnMR)** register, set the **TnAMS** bit to 0x1, the **TnCMR** bit to 0x0, and the **TnMR** field to 0x2.
4. Configure the output state of the PWM signal (whether or not it is inverted) in the **TnEVENT** field of the **GPTM Control (GPTMCTL)** register.
5. Load the timer start value into the **GPTM Timer n Interval Load (GPTMTnILR)** register.
6. Load the **GPTM Timer n Match (GPTMTnMATCHR)** register with the match value.
7. Set the **TnEN** bit in the **GPTM Control (GPTMCTL)** register to enable the timer and begin generation of the output PWM signal.

In PWM Timing mode, the timer continues running after the PWM signal has been generated. The PWM period can be adjusted at any time by writing the **GPTMTnILR** register, and the change takes effect at the next cycle after the write.

## 12.5 Register Map

Table 12-4 on page 424 lists the GPTM registers. The offset listed is a hexadecimal increment to the register's address, relative to that timer's base address:

- Timer0: 0x4003.0000
- Timer1: 0x4003.1000
- Timer2: 0x4003.2000
- Timer3: 0x4003.3000

Note that the GP Timer module clock must be enabled before the registers can be programmed (see page 149).

Table 12-4. Timers Register Map

Offset	Name	Type	Reset	Description	See page
0x000	GPTMCFG	R/W	0x0000.0000	GPTM Configuration	425
0x004	GPTMTAMR	R/W	0x0000.0000	GPTM Timer A Mode	426
0x008	GPTMTBMR	R/W	0x0000.0000	GPTM Timer B Mode	428
0x00C	GPTMCTL	R/W	0x0000.0000	GPTM Control	430
0x018	GPTMIMR	R/W	0x0000.0000	GPTM Interrupt Mask	433
0x01C	GPTMRIS	RO	0x0000.0000	GPTM Raw Interrupt Status	435
0x020	GPTMMIS	RO	0x0000.0000	GPTM Masked Interrupt Status	438
0x024	GPTMICR	W1C	0x0000.0000	GPTM Interrupt Clear	441
0x028	GPTMTAILR	R/W	0xFFFF.FFFF	GPTM Timer A Interval Load	443
0x02C	GPTMTBILR	R/W	0x0000.FFFF	GPTM Timer B Interval Load	444
0x030	GPTMTAMATCHR	R/W	0xFFFF.FFFF	GPTM Timer A Match	445
0x034	GPTMTBMATCHR	R/W	0x0000.FFFF	GPTM Timer B Match	446
0x038	GPTMTAPR	R/W	0x0000.0000	GPTM Timer A Prescale	447
0x03C	GPTMTBPR	R/W	0x0000.0000	GPTM Timer B Prescale	448
0x048	GPTMTAR	RO	0xFFFF.FFFF	GPTM Timer A	449
0x04C	GPTMTBR	RO	0x0000.FFFF	GPTM Timer B	450
0x050	GPTMTAV	RO	0xFFFF.FFFF	GPTM Timer A Value	451
0x054	GPTMTBV	RO	0x0000.FFFF	GPTM Timer B Value	452

## 12.6 Register Descriptions

The remainder of this section lists and describes the GPTM registers, in numerical order by address offset.



## Register 1: GPTM Configuration (GPTMCFG), offset 0x000

This register configures the global operation of the GPTM module. The value written to this register determines whether the GPTM is in 32- or 16-bit mode.

### GPTM Configuration (GPTMCFG)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x000  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													GPTMCFG			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	GPTMCFG	R/W	0x0	GPTM Configuration

The GPTMCFG values are defined as follows:

Value	Description
0x0	32-bit timer configuration.
0x1	32-bit real-time clock (RTC) counter configuration.
0x2	Reserved
0x3	Reserved
0x4	16-bit timer configuration. The function is controlled by bits 1:0 of <b>GPTMTAMR</b> and <b>GPTMTBMR</b> .

## Register 2: GPTM Timer A Mode (GPTMTAMR), offset 0x004

This register configures the GPTM based on the configuration selected in the **GPTMCFG** register. When in 16-bit PWM mode, set the **TAAMS** bit, clear the **TACMR** bit, and configure the **TAMR** field to 0x2.

In 16-bit timer configuration, **TAMR** controls the 16-bit timer modes for Timer A. In 32-bit timer configuration, this register controls the mode, and the contents of **GPTMTBMR** are ignored.

### GPTM Timer A Mode (GPTMTAMR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x004  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								TASNAPS	TAWOT	TAMIE	TACDIR	TAAMS	TACMR	TAMR	
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	TASNAPS	R/W	0	GPTM Timer A Snap-Shot Mode  Value Description 0 Snap-shot mode is disabled. 1 If Timer A is configured in the periodic mode, the actual free-running value of Timer A is loaded at the time-out event into the <b>GPTM Timer A (GPTMTAR)</b> register.
6	TAWOT	R/W	0	GPTM Timer A Wait-on-Trigger  Value Description 0 Timer A begins counting as soon as it is enabled. 1 If Timer A is enabled ( <b>TAEN</b> is set in the <b>GPTMCTL</b> register), Timer A does not begin counting until it receives a trigger from the timer in the previous position in the daisy chain, see Figure 12-5 on page 419. This function is valid for both one-shot and periodic modes.

This bit must be clear for GP Timer Module 0, Timer A.

Bit/Field	Name	Type	Reset	Description
5	TAMIE	R/W	0	<p>GPTM Timer A Match Interrupt Enable</p> <p>Value Description</p> <p>0 The match interrupt is disabled.</p> <p>1 An interrupt is generated when the match value in the <b>GPTMTAMATCHR</b> register is reached in the one-shot and periodic modes.</p>
4	TACDIR	R/W	0	<p>GPTM Timer A Count Direction</p> <p>Value Description</p> <p>0 The timer counts down.</p> <p>1 When in one-shot or periodic mode, the timer counts up. When counting up, the timer starts from a value of 0x0000.</p>
3	TAAMS	R/W	0	<p>GPTM Timer A Alternate Mode Select</p> <p>The <b>TAAMS</b> values are defined as follows:</p> <p>Value Description</p> <p>0 Capture mode is enabled.</p> <p>1 PWM mode is enabled.</p> <p><b>Note:</b> To enable PWM mode, you must also clear the <b>TACMR</b> bit and configure the <b>TAMR</b> field to 0x2.</p>
2	TACMR	R/W	0	<p>GPTM Timer A Capture Mode</p> <p>The <b>TACMR</b> values are defined as follows:</p> <p>Value Description</p> <p>0 Edge-Count mode</p> <p>1 Edge-Time mode</p>
1:0	TAMR	R/W	0x0	<p>GPTM Timer A Mode</p> <p>The <b>TAMR</b> values are defined as follows:</p> <p>Value Description</p> <p>0x0 Reserved</p> <p>0x1 One-Shot Timer mode</p> <p>0x2 Periodic Timer mode</p> <p>0x3 Capture mode</p> <p>The Timer mode is based on the timer configuration defined by bits 2:0 in the <b>GPTMCFG</b> register (16-or 32-bit).</p>

### Register 3: GPTM Timer B Mode (GPTMTBMR), offset 0x008

This register configures the GPTM based on the configuration selected in the **GPTMCFG** register. When in 16-bit PWM mode, set the **TBAMS** bit, clear the **TBCMR** bit, and configure the **TBMR** field to 0x2.

In 16-bit timer configuration, these bits control the 16-bit timer modes for Timer B. In 32-bit timer configuration, this register's contents are ignored, and **GPTMTAMR** is used.

#### GPTM Timer B Mode (GPTMTBMR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x008  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								TBSNAPS	TBWOT	TBMIE	TBCDIR	TBAMS	TBCMR	TBMR	
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	TBSNAPS	R/W	0	GPTM Timer B Snap-Shot Mode  Value Description 0 Snap-shot mode is disabled. 1 If Timer B is configured in the periodic mode, the actual free-running value of Timer B is loaded at the time-out event into the <b>GPTM Timer B (GPTMTBR)</b> register.
6	TBWOT	R/W	0	GPTM Timer B Wait-on-Trigger  Value Description 0 Timer B begins counting as soon as it is enabled. 1 If Timer B is enabled ( <b>TBEN</b> is set in the <b>GPTMCTL</b> register), Timer B does not begin counting until it receives an it receives a trigger from the timer in the previous position in the daisy chain. See Figure 12-5 on page 419. This function is valid for both one-shot and periodic modes.

Bit/Field	Name	Type	Reset	Description
5	TBMIE	R/W	0	<p>GPTM Timer B Match Interrupt Enable</p> <p>Value Description</p> <p>0 The match interrupt is disabled.</p> <p>1 An interrupt is generated when the match value in the <b>GPTMTBMATCHR</b> register is reached in the one-shot and periodic modes.</p>
4	TBCDIR	R/W	0	<p>GPTM Timer B Count Direction</p> <p>Value Description</p> <p>0 The timer counts down.</p> <p>1 When in one-shot or periodic mode, the timer counts up. When counting up, the timer starts from a value of 0x0000.</p>
3	TBAMS	R/W	0	<p>GPTM Timer B Alternate Mode Select</p> <p>The <b>TBAMS</b> values are defined as follows:</p> <p>Value Description</p> <p>0 Capture mode is enabled.</p> <p>1 PWM mode is enabled.</p> <p><b>Note:</b> To enable PWM mode, you must also clear the <b>TBCMR</b> bit and set the <b>TBMR</b> field to 0x2.</p>
2	TBCMR	R/W	0	<p>GPTM Timer B Capture Mode</p> <p>The <b>TBCMR</b> values are defined as follows:</p> <p>Value Description</p> <p>0 Edge-Count mode</p> <p>1 Edge-Time mode</p>
1:0	TBMR	R/W	0x0	<p>GPTM Timer B Mode</p> <p>The <b>TBMR</b> values are defined as follows:</p> <p>Value Description</p> <p>0x0 Reserved</p> <p>0x1 One-Shot Timer mode</p> <p>0x2 Periodic Timer mode</p> <p>0x3 Capture mode</p> <p>The timer mode is based on the timer configuration defined by bits 2:0 in the <b>GPTMCFG</b> register.</p>

### Register 4: GPTM Control (GPTMCTL), offset 0x00C

This register is used alongside the **GPTMCFG** and **GMTMTnMR** registers to fine-tune the timer configuration, and to enable other features such as timer stall and the output trigger. The output trigger can be used to initiate transfers on the ADC module.

#### GPTM Control (GPTMCTL)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x00C  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	TBPWML	TBOTE	reserved	TBEVENT	TBSTALL	TBEN	reserved	TAPWML	TAOTE	RTCEN	TAEVENT	TASTALL	TAEN		
Type	RO	R/W	R/W	RO	R/W	R/W	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:15	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14	TBPWML	R/W	0	GPTM Timer B PWM Output Level  The TBPWML values are defined as follows:  Value Description 0 Output is unaffected. 1 Output is inverted.
13	TBOTE	R/W	0	GPTM Timer B Output Trigger Enable  The TBOTE values are defined as follows:  Value Description 0 The output Timer B ADC trigger is disabled. 1 The output Timer B ADC trigger is enabled.  In addition, the ADC must be enabled and the timer selected as a trigger source with the EMn bit in the <b>ADCEMUX</b> register (see page 505).
12	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description										
11:10	TBEVENT	R/W	0x0	<p>GPTM Timer B Event Mode</p> <p>The TBEVENT values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Positive edge</td> </tr> <tr> <td>0x1</td> <td>Negative edge</td> </tr> <tr> <td>0x2</td> <td>Reserved</td> </tr> <tr> <td>0x3</td> <td>Both edges</td> </tr> </tbody> </table>	Value	Description	0x0	Positive edge	0x1	Negative edge	0x2	Reserved	0x3	Both edges
Value	Description													
0x0	Positive edge													
0x1	Negative edge													
0x2	Reserved													
0x3	Both edges													
9	TBSTALL	R/W	0	<p>GPTM Timer B Stall Enable</p> <p>The TBSTALL values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Timer B stalling is disabled.</td> </tr> <tr> <td>1</td> <td>Timer B stalling is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Timer B stalling is disabled.	1	Timer B stalling is enabled.				
Value	Description													
0	Timer B stalling is disabled.													
1	Timer B stalling is enabled.													
8	TBEN	R/W	0	<p>GPTM Timer B Enable</p> <p>The TBEN values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Timer B is disabled.</td> </tr> <tr> <td>1</td> <td>Timer B is enabled and begins counting or the capture logic is enabled based on the <b>GPTMCFG</b> register.</td> </tr> </tbody> </table>	Value	Description	0	Timer B is disabled.	1	Timer B is enabled and begins counting or the capture logic is enabled based on the <b>GPTMCFG</b> register.				
Value	Description													
0	Timer B is disabled.													
1	Timer B is enabled and begins counting or the capture logic is enabled based on the <b>GPTMCFG</b> register.													
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
6	TAPWML	R/W	0	<p>GPTM Timer A PWM Output Level</p> <p>The TAPWML values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Output is unaffected.</td> </tr> <tr> <td>1</td> <td>Output is inverted.</td> </tr> </tbody> </table>	Value	Description	0	Output is unaffected.	1	Output is inverted.				
Value	Description													
0	Output is unaffected.													
1	Output is inverted.													
5	TAOTE	R/W	0	<p>GPTM Timer A Output Trigger Enable</p> <p>The TAOTE values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The output Timer A ADC trigger is disabled.</td> </tr> <tr> <td>1</td> <td>The output Timer A ADC trigger is enabled.</td> </tr> </tbody> </table> <p>In addition, the ADC must be enabled and the timer selected as a trigger source with the EM<sub>n</sub> bit in the <b>ADCEMUX</b> register (see page 505).</p>	Value	Description	0	The output Timer A ADC trigger is disabled.	1	The output Timer A ADC trigger is enabled.				
Value	Description													
0	The output Timer A ADC trigger is disabled.													
1	The output Timer A ADC trigger is enabled.													

Bit/Field	Name	Type	Reset	Description										
4	RTCEN	R/W	0	<p>GPTM RTC Enable</p> <p>The <code>RTCEN</code> values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>RTC counting is disabled.</td> </tr> <tr> <td>1</td> <td>RTC counting is enabled.</td> </tr> </tbody> </table>	Value	Description	0	RTC counting is disabled.	1	RTC counting is enabled.				
Value	Description													
0	RTC counting is disabled.													
1	RTC counting is enabled.													
3:2	TAEVENT	R/W	0x0	<p>GPTM Timer A Event Mode</p> <p>The <code>TAEVENT</code> values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Positive edge</td> </tr> <tr> <td>0x1</td> <td>Negative edge</td> </tr> <tr> <td>0x2</td> <td>Reserved</td> </tr> <tr> <td>0x3</td> <td>Both edges</td> </tr> </tbody> </table>	Value	Description	0x0	Positive edge	0x1	Negative edge	0x2	Reserved	0x3	Both edges
Value	Description													
0x0	Positive edge													
0x1	Negative edge													
0x2	Reserved													
0x3	Both edges													
1	TASTALL	R/W	0	<p>GPTM Timer A Stall Enable</p> <p>The <code>TASTALL</code> values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Timer A stalling is disabled.</td> </tr> <tr> <td>1</td> <td>Timer A stalling is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Timer A stalling is disabled.	1	Timer A stalling is enabled.				
Value	Description													
0	Timer A stalling is disabled.													
1	Timer A stalling is enabled.													
0	TAEN	R/W	0	<p>GPTM Timer A Enable</p> <p>The <code>TAEN</code> values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Timer A is disabled.</td> </tr> <tr> <td>1</td> <td>Timer A is enabled and begins counting or the capture logic is enabled based on the <code>GPTMCFG</code> register.</td> </tr> </tbody> </table>	Value	Description	0	Timer A is disabled.	1	Timer A is enabled and begins counting or the capture logic is enabled based on the <code>GPTMCFG</code> register.				
Value	Description													
0	Timer A is disabled.													
1	Timer A is enabled and begins counting or the capture logic is enabled based on the <code>GPTMCFG</code> register.													



## Register 5: GPTM Interrupt Mask (GPTMIMR), offset 0x018

This register allows software to enable/disable GPTM controller-level interrupts. Setting a bit enables the corresponding interrupt, while clearing a bit disables it.

### GPTM Interrupt Mask (GPTMIMR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x018  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved				TBMIM	CBEIM	CBMIM	TBTOIM	reserved				TAMIM	RTCIM	CAEIM	CAMIM	TATOIM
Type	RO	RO	RO	RO	R/W	R/W	R/W	R/W	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description						
31:12	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
11	TBMIM	R/W	0	GPTM Timer B Mode Match Interrupt Mask The TBMIM values are defined as follows: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									
10	CBEIM	R/W	0	GPTM Capture B Event Interrupt Mask The CBEIM values are defined as follows: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									
9	CBMIM	R/W	0	GPTM Capture B Match Interrupt Mask The CBMIM values are defined as follows: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									

Bit/Field	Name	Type	Reset	Description						
8	TBTOIM	R/W	0	<p>GPTM Timer B Time-Out Interrupt Mask</p> <p>The TBTOIM values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
4	TAMIM	R/W	0	<p>GPTM Timer A Mode Match Interrupt Mask</p> <p>The TAMIM values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									
3	RTCIM	R/W	0	<p>GPTM RTC Interrupt Mask</p> <p>The RTCIM values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									
2	CAEIM	R/W	0	<p>GPTM Capture A Event Interrupt Mask</p> <p>The CAEIM values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									
1	CAMIM	R/W	0	<p>GPTM Capture A Match Interrupt Mask</p> <p>The CAMIM values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									
0	TATOIM	R/W	0	<p>GPTM Timer A Time-Out Interrupt Mask</p> <p>The TATOIM values are defined as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Interrupt is disabled.</td> </tr> <tr> <td>1</td> <td>Interrupt is enabled.</td> </tr> </tbody> </table>	Value	Description	0	Interrupt is disabled.	1	Interrupt is enabled.
Value	Description									
0	Interrupt is disabled.									
1	Interrupt is enabled.									

## Register 6: GPTM Raw Interrupt Status (GPTMRIS), offset 0x01C

This register shows the state of the GPTM's internal interrupt signal. These bits are set whether or not the interrupt is masked in the **GPTMIMR** register. Each bit can be cleared by writing a 1 to its corresponding bit in **GPTMICR**.

### GPTM Raw Interrupt Status (GPTMRIS)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x01C  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved				TBMRIS	CBERIS	CBMRIS	TBTORIS	reserved				TAMRIS	RTCRIS	CAERIS	CAMRIS	TATORIS
Type	RO	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	R/W	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:12	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	TBMRIS	R/W	0	GPTM Timer B Mode Match Raw Interrupt  Value Description 1 The <b>TBMIE</b> bit is set in the <b>GPTMTBMR</b> register, and the match value in the <b>GPTMTBMATCHR</b> register has been reached when in the one-shot and periodic modes. 0 The match value has not been reached.  This bit is cleared by writing a 1 to the <b>TBMCINT</b> bit in the <b>GPTMICR</b> register.
10	CBERIS	RO	0	GPTM Capture B Event Raw Interrupt  Value Description 1 The Capture B event has occurred. 0 The Capture B event has not occurred.  This bit is cleared by writing a 1 to the <b>CBECINT</b> bit in the <b>GPTMICR</b> register.
9	CBMRIS	RO	0	GPTM Capture B Match Raw Interrupt  Value Description 1 The Capture B match has occurred. 0 The Capture B match has not occurred.  This bit is cleared by writing a 1 to the <b>CBMCINT</b> bit in the <b>GPTMICR</b> register.

Bit/Field	Name	Type	Reset	Description
8	TBTORIS	RO	0	<p>GPTM Timer B Time-Out Raw Interrupt</p> <p>Value Description</p> <p>1 Timer B has timed out.</p> <p>0 Timer B has not timed out.</p> <p>This bit is cleared by writing a 1 to the <code>TBTOCINT</code> bit in the <b>GPTMICR</b> register.</p>
7:5	reserved	RO	0x0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
4	TAMRIS	R/W	0	<p>GPTM Timer A Mode Match Raw Interrupt</p> <p>Value Description</p> <p>1 The <code>TAMIE</code> bit is set in the <b>GPTMTAMR</b> register, and the match value in the <b>GPTMTAMATCHR</b> register has been reached when in the one-shot and periodic modes.</p> <p>0 The match value has not been reached.</p> <p>This bit is cleared by writing a 1 to the <code>TAMCINT</code> bit in the <b>GPTMICR</b> register.</p>
3	RTCRIS	RO	0	<p>GPTM RTC Raw Interrupt</p> <p>Value Description</p> <p>1 The RTC event has occurred.</p> <p>0 The RTC event has not occurred.</p> <p>This bit is cleared by writing a 1 to the <code>RTCCINT</code> bit in the <b>GPTMICR</b> register.</p>
2	CAERIS	RO	0	<p>GPTM Capture A Event Raw Interrupt</p> <p>Value Description</p> <p>1 The Capture A event has occurred.</p> <p>0 The Capture A event has not occurred.</p> <p>This bit is cleared by writing a 1 to the <code>CAECINT</code> bit in the <b>GPTMICR</b> register.</p>
1	CAMRIS	RO	0	<p>GPTM Capture A Match Raw Interrupt</p> <p>Value Description</p> <p>1 The Capture A match has occurred.</p> <p>0 The Capture A match has not occurred.</p> <p>This bit is cleared by writing a 1 to the <code>CAMCINT</code> bit in the <b>GPTMICR</b> register.</p>

---

Bit/Field	Name	Type	Reset	Description
0	TATORIS	RO	0	GPTM Timer A Time-Out Raw Interrupt
				Value Description
				1 Timer A has timed out.
				0 Timer A has not timed out.
				This bit is cleared by writing a 1 to the TATOCINT bit in the <b>GPTMICR</b> register.

### Register 7: GPTM Masked Interrupt Status (GPTMMIS), offset 0x020

This register show the state of the GPTM's controller-level interrupt. If an interrupt is unmasked in **GPTMIMR**, and there is an event that causes the interrupt to be asserted, the corresponding bit is set in this register. All bits are cleared by writing a 1 to the corresponding bit in **GPTMICR**.

#### GPTM Masked Interrupt Status (GPTMMIS)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x020  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved				TBMMIS	CBEMIS	CBMMIS	TBTOMIS	reserved				TAMMIS	RTCMIS	CAEMIS	CAMMIS	TATOMIS
Type	RO	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	R/W	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:12	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	TBMMIS	R/W	0	GPTM Timer B Mode Match Masked Interrupt  Value Description 1 An unmasked Timer B Mode Match interrupt has occurred. 0 A Timer B Mode Match interrupt has not occurred or is masked.  This bit is cleared by writing a 1 to the <b>TBMCINT</b> bit in the <b>GPTMICR</b> register.
10	CBEMIS	RO	0	GPTM Capture B Event Masked Interrupt  Value Description 1 An unmasked Capture B event interrupt has occurred. 0 A Capture B event interrupt has not occurred or is masked.  This bit is cleared by writing a 1 to the <b>CBECINT</b> bit in the <b>GPTMICR</b> register.

Bit/Field	Name	Type	Reset	Description
9	CBMMIS	RO	0	<p>GPTM Capture B Match Masked Interrupt</p> <p>Value Description</p> <p>1 An unmasked Capture B Match interrupt has occurred.</p> <p>0 A Capture B Mode Match interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>CBMCINT</code> bit in the <b>GPTMICR</b> register.</p>
8	TBTOMIS	RO	0	<p>GPTM Timer B Time-Out Masked Interrupt</p> <p>Value Description</p> <p>1 An unmasked Timer B Time-Out interrupt has occurred.</p> <p>0 A Timer B Time-Out interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>TBTOCINT</code> bit in the <b>GPTMICR</b> register.</p>
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	TAMMIS	R/W	0	<p>GPTM Timer A Mode Match Masked Interrupt</p> <p>Value Description</p> <p>1 An unmasked Timer A Mode Match interrupt has occurred.</p> <p>0 A Timer A Mode Match interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>TAMCINT</code> bit in the <b>GPTMICR</b> register.</p>
3	RTCMIS	RO	0	<p>GPTM RTC Masked Interrupt</p> <p>Value Description</p> <p>1 An unmasked RTC event interrupt has occurred.</p> <p>0 An RTC event interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>RTCCINT</code> bit in the <b>GPTMICR</b> register.</p>
2	CAEMIS	RO	0	<p>GPTM Capture A Event Masked Interrupt</p> <p>Value Description</p> <p>1 An unmasked Capture A event interrupt has occurred.</p> <p>0 A Capture A event interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>CAECINT</code> bit in the <b>GPTMICR</b> register.</p>

Bit/Field	Name	Type	Reset	Description
1	CAMMIS	RO	0	<p>GPTM Capture A Match Masked Interrupt</p> <p>Value Description</p> <p>1 An unmasked Capture A Match interrupt has occurred.</p> <p>0 A Capture A Mode Match interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the CAMCINT bit in the <b>GPTMICR</b> register.</p>
0	TATOMIS	RO	0	<p>GPTM Timer A Time-Out Masked Interrupt</p> <p>Value Description</p> <p>1 An unmasked Timer A Time-Out interrupt has occurred.</p> <p>0 A Timer A Time-Out interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the TATOCINT bit in the <b>GPTMICR</b> register.</p>



## Register 8: GPTM Interrupt Clear (GPTMICR), offset 0x024

This register is used to clear the status bits in the **GPTMRIS** and **GPTMMIS** registers. Writing a 1 to a bit clears the corresponding bit in the **GPTMRIS** and **GPTMMIS** registers.

### GPTM Interrupt Clear (GPTMICR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x024  
 Type W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved				TBMCINT	CBECINT	CBMCINT	TBTOCINT	reserved			TAMCINT	RTCCINT	CAECINT	CAMCINT	TATOCINT
Type	RO	RO	RO	RO	W1C	W1C	W1C	W1C	RO	RO	RO	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:12	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	TBMCINT	W1C	0	GPTM Timer B Mode Match Interrupt Clear  Writing a 1 to this bit clears the <b>TBMRIS</b> bit in the <b>GPTMRIS</b> register and the <b>TBMMIS</b> bit in the <b>GPTMMIS</b> register.
10	CBECINT	W1C	0	GPTM Capture B Event Interrupt Clear  Writing a 1 to this bit clears the <b>CBERIS</b> bit in the <b>GPTMRIS</b> register and the <b>CBEMIS</b> bit in the <b>GPTMMIS</b> register.
9	CBMCINT	W1C	0	GPTM Capture B Match Interrupt Clear  Writing a 1 to this bit clears the <b>CBMRIS</b> bit in the <b>GPTMRIS</b> register and the <b>CBMMIS</b> bit in the <b>GPTMMIS</b> register.
8	TBTOCINT	W1C	0	GPTM Timer B Time-Out Interrupt Clear  Writing a 1 to this bit clears the <b>TBTORIS</b> bit in the <b>GPTMRIS</b> register and the <b>TBTOMIS</b> bit in the <b>GPTMMIS</b> register.
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	TAMCINT	W1C	0	GPTM Timer A Mode Match Interrupt Clear  Writing a 1 to this bit clears the <b>TAMRIS</b> bit in the <b>GPTMRIS</b> register and the <b>TAMMIS</b> bit in the <b>GPTMMIS</b> register.
3	RTCCINT	W1C	0	GPTM RTC Interrupt Clear  Writing a 1 to this bit clears the <b>RTCRIS</b> bit in the <b>GPTMRIS</b> register and the <b>RTCMIS</b> bit in the <b>GPTMMIS</b> register.

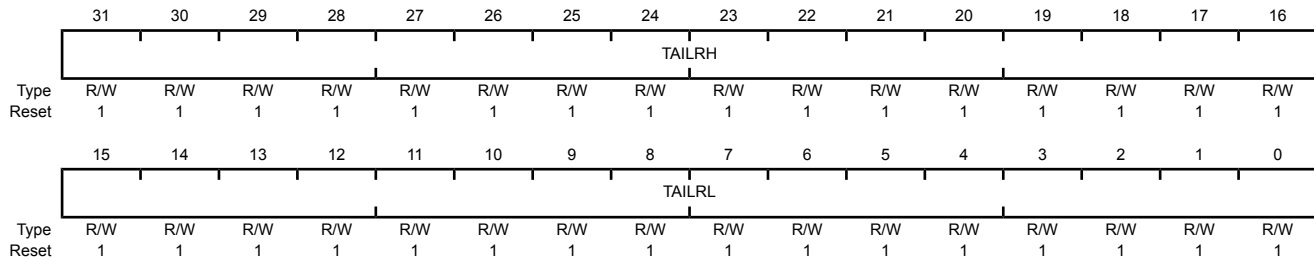
Bit/Field	Name	Type	Reset	Description
2	CAECINT	W1C	0	GPTM Capture A Event Interrupt Clear Writing a 1 to this bit clears the CAERIS bit in the <b>GPTMRIS</b> register and the CAEMIS bit in the <b>GPTMMIS</b> register.
1	CAMCINT	W1C	0	GPTM Capture A Match Interrupt Clear Writing a 1 to this bit clears the CAMRIS bit in the <b>GPTMRIS</b> register and the CAMMIS bit in the <b>GPTMMIS</b> register.
0	TATOCINT	W1C	0	GPTM Timer A Time-Out Raw Interrupt Writing a 1 to this bit clears the TATORIS bit in the <b>GPTMRIS</b> register and the TATOMIS bit in the <b>GPTMMIS</b> register.

## Register 9: GPTM Timer A Interval Load (GPTMTAILR), offset 0x028

This register is used to load the starting count value into the timer. When GPTM is configured to one of the 32-bit modes, **GPTMTAILR** appears as a 32-bit register (the upper 16-bits correspond to the contents of the **GPTM Timer B Interval Load (GPTMTBILR)** register). In 16-bit mode, the upper 16 bits of this register read as 0s and have no effect on the state of **GPTMTBILR**.

### GPTM Timer A Interval Load (GPTMTAILR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x028  
 Type R/W, reset 0xFFFF.FFFF



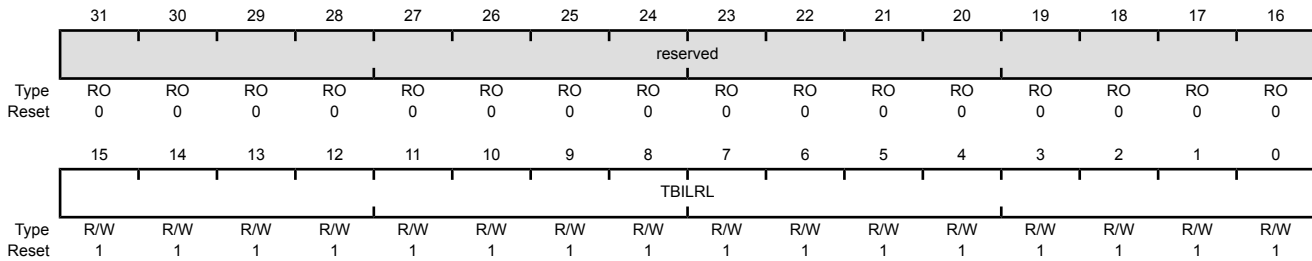
Bit/Field	Name	Type	Reset	Description
31:16	TAILRH	R/W	0xFFFF	GPTM Timer A Interval Load Register High  When configured for 32-bit mode via the <b>GPTMCFG</b> register, the <b>GPTM Timer B Interval Load (GPTMTBILR)</b> register loads this value on a write. A read returns the current value of <b>GPTMTBILR</b> .  In 16-bit mode, this field reads as 0 and does not have an effect on the state of <b>GPTMTBILR</b> .
15:0	TAILRL	R/W	0xFFFF	GPTM Timer A Interval Load Register Low  For both 16- and 32-bit modes, writing this field loads the counter for Timer A. A read returns the current value of <b>GPTMTAILR</b> .

### Register 10: GPTM Timer B Interval Load (GPTMTBILR), offset 0x02C

This register is used to load the starting count value into Timer B. When the GPTM is configured to a 32-bit mode, **GPTMTBILR** returns the current value of Timer B and ignores writes.

#### GPTM Timer B Interval Load (GPTMTBILR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x02C  
 Type R/W, reset 0x0000.FFFF



Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	TBILRL	R/W	0xFFFF	GPTM Timer B Interval Load Register

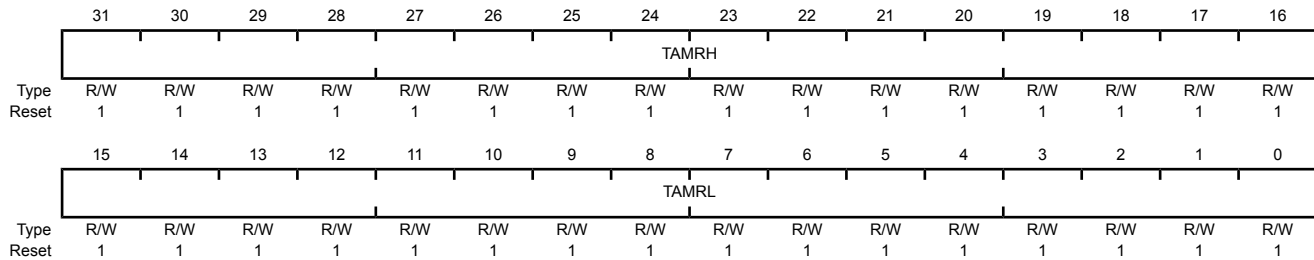
When the GPTM is not configured as a 32-bit timer, a write to this field updates **GPTMTBILR**. In 32-bit mode, writes are ignored, and reads return the current value of **GPTMTBILR**.

## Register 11: GPTM Timer A Match (GPTMTAMATCHR), offset 0x030

This register is loaded with a match value. Interrupts can be generated when the timer value is equal to the value in this register in one-shot or periodic mode. In 16-bit Edge-Count mode, this register along with **GPTMTAILR**, determines how many edge events are counted. The total number of edge events counted is equal to the value in **GPTMTAILR** minus this value.

### GPTM Timer A Match (GPTMTAMATCHR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x030  
 Type R/W, reset 0xFFFF.FFFF



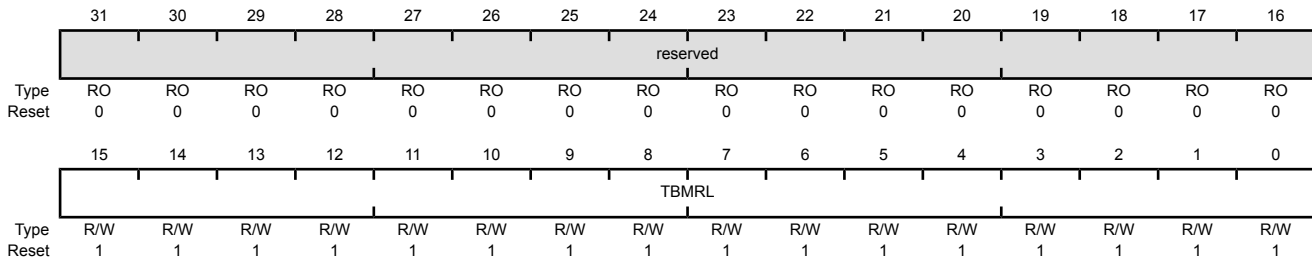
Bit/Field	Name	Type	Reset	Description
31:16	TAMRH	R/W	0xFFFF	<p>GPTM Timer A Match Register High</p> <p>When the timer is configured for 32-bit mode via the <b>GPTMCFG</b> register, this value is compared to the upper half of <b>GPTMTAR</b> to determine match events.</p> <p>In 16-bit mode, this field reads as 0 and does not have an effect on the state of <b>GPTMTBMATCHR</b>.</p>
15:0	TAMRL	R/W	0xFFFF	<p>GPTM Timer A Match Register Low</p> <p>When the timer is configured for 32-bit mode via the <b>GPTMCFG</b> register, this value is compared to the lower half of <b>GPTMTAR</b>, to determine match events.</p> <p>When the timer is configured for 16-bit mode via the <b>GPTMCFG</b> register, this value is compared to <b>GPTMTAR</b> to determine match events.</p> <p>When configured for 16-bit Edge-Count mode, this value along with <b>GPTMTAILR</b>, determines how many edge events are counted. The total number of edge events counted is equal to the value in <b>GPTMTAILR</b> minus this value.</p> <p>When configured for PWM mode, this value along with <b>GPTMTAILR</b>, determines the duty cycle of the output PWM signal.</p>

### Register 12: GPTM Timer B Match (GPTMTBMATCHR), offset 0x034

This register is loaded with a match value. Interrupts can be generated when the timer value is equal to the value in this register in one-shot or periodic mode. In 16-bit Edge-Count mode, this register along with **GPTMTAILR**, determines how many edge events are counted. The total number of edge events counted is equal to the value in **GPTMTAILR** minus this value.

#### GPTM Timer B Match (GPTMTBMATCHR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x034  
 Type R/W, reset 0x0000.FFFF



Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	TBMRL	R/W	0xFFFF	GPTM Timer B Match Register Low  When the timer is configured for 16-bit mode via the <b>GPTMCFG</b> register, this value is compared to <b>GPTMTBR</b> to determine match events.  When configured for 16-bit Edge-Count mode, this value along with <b>GPTMTBILR</b> , determines how many edge events are counted. The total number of edge events counted is equal to the value in <b>GPTMTBILR</b> minus this value.  When configured for PWM mode, this value along with <b>GPTMTBILR</b> , determines the duty cycle of the output PWM signal.

**Register 13: GPTM Timer A Prescale (GPTMTAPR), offset 0x038**

This register allows software to extend the range of the 16-bit timers.

**GPTM Timer A Prescale (GPTMTAPR)**

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x038  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								TAPSR							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	TAPSR	R/W	0x00	GPTM Timer A Prescale

The register loads this value on a write. A read returns the current value of the register.

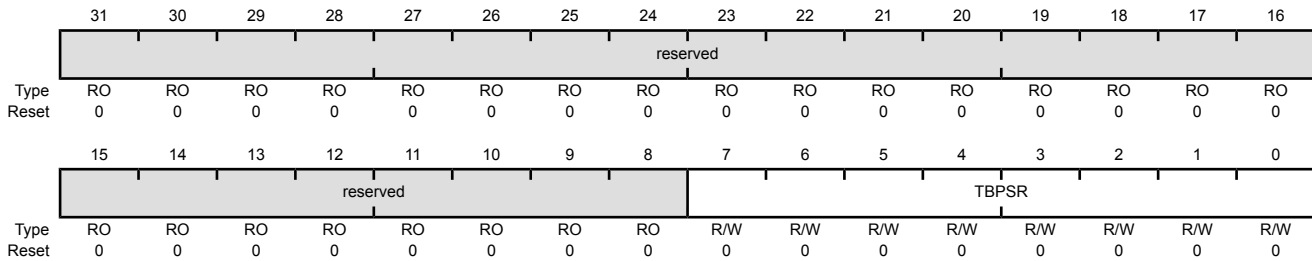
Refer to Table 12-3 on page 416 for more details and an example.

### Register 14: GPTM Timer B Prescale (GPTMTBPR), offset 0x03C

This register allows software to extend the range of the 16-bit timers.

#### GPTM Timer B Prescale (GPTMTBPR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x03C  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	TBPSR	R/W	0x00	GPTM Timer B Prescale

The register loads this value on a write. A read returns the current value of this register.

Refer to Table 12-3 on page 416 for more details and an example.

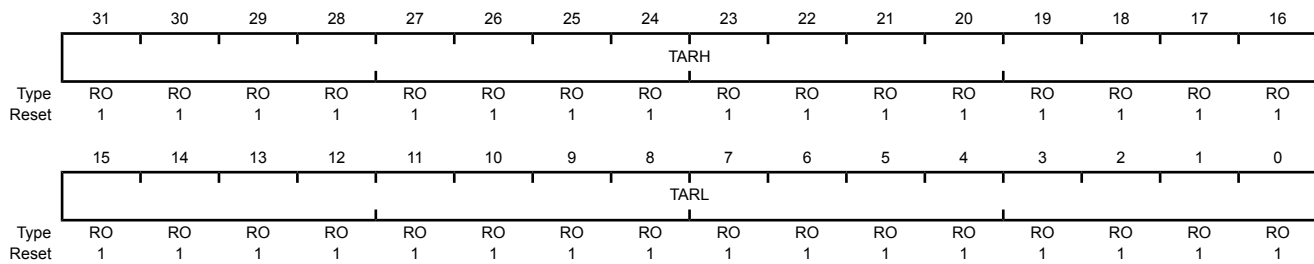


**Register 15: GPTM Timer A (GPTMTAR), offset 0x048**

This register shows the current value of the Timer A counter in all cases except for Input Edge-Count mode. When in this mode, this register contains the time at which the last edge event took place.

**GPTM Timer A (GPTMTAR)**

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x048  
 Type RO, reset 0xFFFF.FFFF



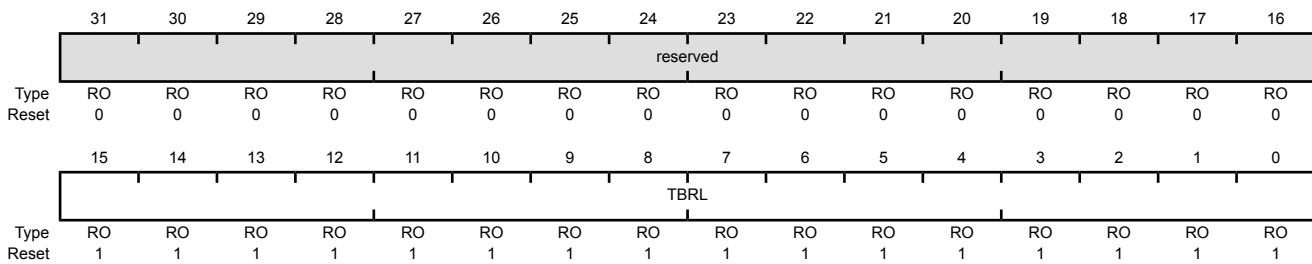
Bit/Field	Name	Type	Reset	Description
31:16	TARH	RO	0xFFFF	GPTM Timer A Register High  If the <b>GPTMCFG</b> is in a 32-bit mode, Timer B value is read. If the <b>GPTMCFG</b> is in a 16-bit mode, this is read as zero.
15:0	TARL	RO	0xFFFF	GPTM Timer A Register Low  A read returns the current value of the <b>GPTM Timer A Count Register</b> , except in Input Edge-Count mode, when it returns the timestamp from the last edge event.

### Register 16: GPTM Timer B (GPTMTBR), offset 0x04C

This register shows the current value of the Timer B counter in all cases except for Input Edge-Count mode. When in this mode, this register contains the time at which the last edge event took place.

#### GPTM Timer B (GPTMTBR)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x04C  
 Type RO, reset 0x0000.FFFF



Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	TBRL	RO	0xFFFF	GPTM Timer B

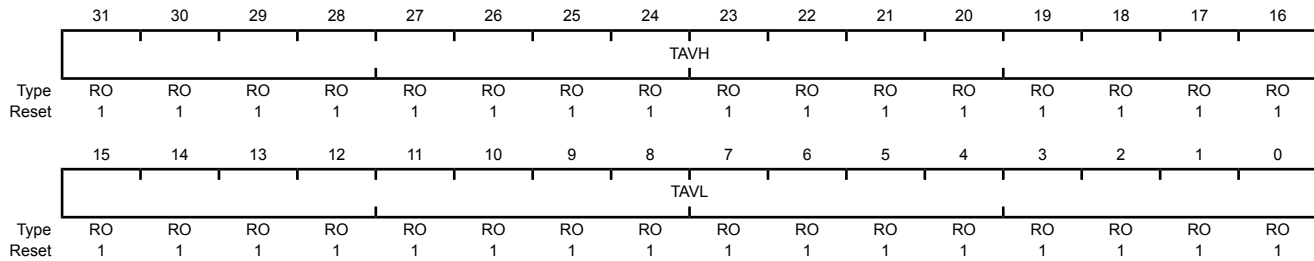
A read returns the current value of the **GPTM Timer B Count Register**, except in Input Edge-Count mode, when it returns the timestamp from the last edge event.

**Register 17: GPTM Timer A Value (GPTMTAV), offset 0x050**

This register shows the current, free-running value of Timer A in all modes. Software can use this value to determine the time elapsed between an interrupt and the ISR entry.

**GPTM Timer A Value (GPTMTAV)**

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x050  
 Type RO, reset 0xFFFF.FFFF



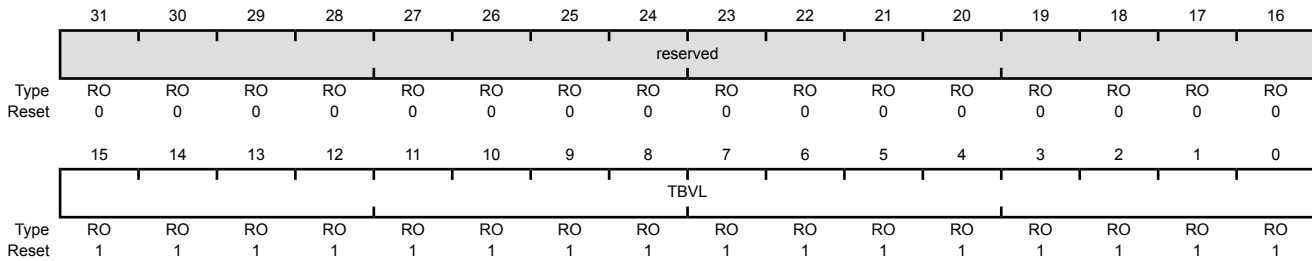
Bit/Field	Name	Type	Reset	Description
31:16	TAVH	RO	0xFFFF	GPTM Timer A Value High  If the <b>GPTMCFG</b> is configured for 32-bit mode, the Timer B value is read. If the <b>GPTMCFG</b> is configured for 16-bit mode, this is read as zero.
15:0	TAVL	RO	0xFFFF	GPTM Timer A Register Low  A read returns the current value of Timer A.

### Register 18: GPTM Timer B Value (GPTMTBV), offset 0x054

This register shows the current, free-running value of Timer B in all modes. Software can use this value to determine the time elapsed between an interrupt and the ISR entry.

#### GPTM Timer B Value (GPTMTBV)

Timer0 base: 0x4003.0000  
 Timer1 base: 0x4003.1000  
 Timer2 base: 0x4003.2000  
 Timer3 base: 0x4003.3000  
 Offset 0x054  
 Type RO, reset 0x0000.FFFF



Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	TBVL	RO	0xFFFF	GPTM Timer B Register A read returns the current value of Timer B.

## 13 Watchdog Timers

A watchdog timer can generate a nonmaskable interrupt (NMI) or a reset when a time-out value is reached. The watchdog timer is used to regain control when a system has failed due to a software error or due to the failure of an external device to respond in the expected way. The LM3S1811 microcontroller has two Watchdog Timer Modules, one module is clocked by the system clock (Watchdog Timer 0) and the other is clocked by the PIOSC (Watchdog Timer 1). The two modules are identical except that WDT1 is in a different clock domain, and therefore requires synchronizers. As a result, WDT1 has a bit defined in the **Watchdog Timer Control (WDTCTL)** register to indicate when a write to a WDT1 register is complete. Software can use this bit to ensure that the previous access has completed before starting the next access.

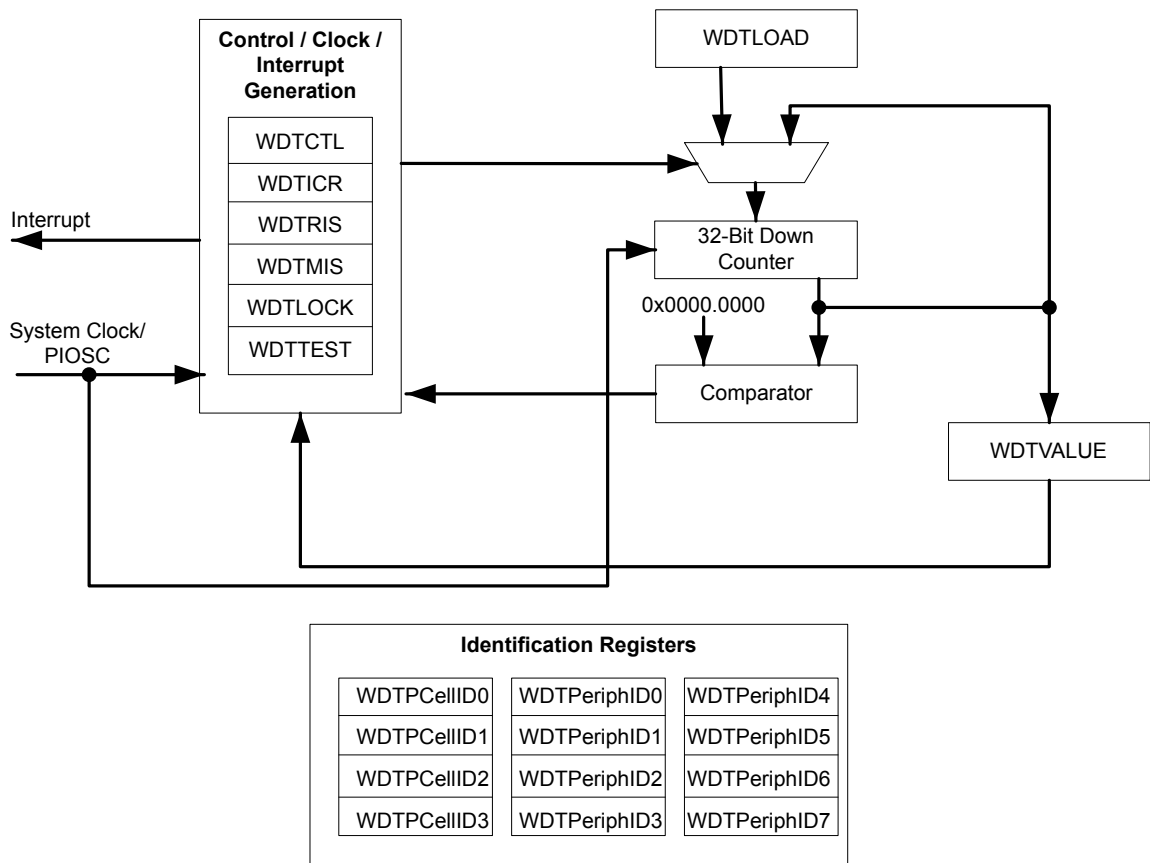
The Stellaris® LM3S1811 controller has two Watchdog Timer modules with the following features:

- 32-bit down counter with a programmable load register
- Separate watchdog clock with an enable
- Programmable interrupt generation logic with interrupt masking
- Lock register protection from runaway software
- Reset generation logic with an enable/disable
- User-enabled stalling when the microcontroller asserts the CPU Halt flag during debug

The Watchdog Timer can be configured to generate an interrupt to the controller on its first time-out, and to generate a reset signal on its second time-out. Once the Watchdog Timer has been configured, the lock register can be written to prevent the timer configuration from being inadvertently altered.

## 13.1 Block Diagram

Figure 13-1. WDT Module Block Diagram



## 13.2 Functional Description

The Watchdog Timer module generates the first time-out signal when the 32-bit counter reaches the zero state after being enabled; enabling the counter also enables the watchdog timer interrupt. After the first time-out event, the 32-bit counter is re-loaded with the value of the **Watchdog Timer Load (WDTLOAD)** register, and the timer resumes counting down from that value. Once the Watchdog Timer has been configured, the **Watchdog Timer Lock (WDTLOCK)** register is written, which prevents the timer configuration from being inadvertently altered by software.

If the timer counts down to its zero state again before the first time-out interrupt is cleared, and the reset signal has been enabled by setting the `RESEN` bit in the **WDTCTL** register, the Watchdog timer asserts its reset signal to the system. If the interrupt is cleared before the 32-bit counter reaches its second time-out, the 32-bit counter is loaded with the value in the **WDTLOAD** register, and counting resumes from that value.

If **WDTLOAD** is written with a new value while the Watchdog Timer counter is counting, then the counter is loaded with the new value and continues counting.

Writing to **WDTLOAD** does not clear an active interrupt. An interrupt must be specifically cleared by writing to the **Watchdog Interrupt Clear (WDTICR)** register.

The Watchdog module interrupt and reset generation can be enabled or disabled as required. When the interrupt is re-enabled, the 32-bit counter is preloaded with the load register value and not its last state.

### 13.2.1 Register Access Timing

Because the Watchdog Timer 1 module has an independent clocking domain, its registers must be written with a timing gap between accesses. Software must guarantee that this delay is inserted between back-to-back writes to WDT1 registers or between a write followed by a read to the registers. The timing for back-to-back reads from the WDT1 module has no restrictions. The **WRC** bit in the **Watchdog Control (WDTCTL)** register for WDT1 indicates that the required timing gap has elapsed. This bit is cleared on a write operation and set once the write completes, indicating to software that another write or read may be started safely. Software should poll **WDTCTL** for **WRC=1** prior to accessing another register. Note that WDT0 does not have this restriction as it runs off the system clock.

## 13.3 Initialization and Configuration

To use the WDT, its peripheral clock must be enabled by setting the **WDT** bit in the **RCGC0** register, see page 143.

The Watchdog Timer is configured using the following sequence:

1. Load the **WDTLOAD** register with the desired timer load value.
2. If WDT1, wait for the **WRC** bit in the **WDTCTL** register to be set.
3. If the Watchdog is configured to trigger system resets, set the **RESEN** bit in the **WDTCTL** register.
4. If WDT1, wait for the **WRC** bit in the **WDTCTL** register to be set.
5. Set the **INTEN** bit in the **WDTCTL** register to enable the Watchdog and lock the control register.

If software requires that all of the watchdog registers are locked, the Watchdog Timer module can be fully locked by writing any value to the **WDTLOCK** register. To unlock the Watchdog Timer, write a value of 0x1ACC.E551.

## 13.4 Register Map

Table 13-1 on page 456 lists the Watchdog registers. The offset listed is a hexadecimal increment to the register's address, relative to the Watchdog Timer base address:

- WDT0: 0x4000.0000
- WDT1: 0x4000.1000

Note that the Watchdog Timer module clock must be enabled before the registers can be programmed (see page 143).

**Table 13-1. Watchdog Timers Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	WDTLOAD	R/W	0xFFFF.FFFF	Watchdog Load	457
0x004	WDTVALUE	RO	0xFFFF.FFFF	Watchdog Value	458
0x008	WDTCTL	R/W	0x0000.0000 (WDT0) 0x8000.0000 (WDT1)	Watchdog Control	459
0x00C	WDTICR	WO	-	Watchdog Interrupt Clear	461
0x010	WDTRIS	RO	0x0000.0000	Watchdog Raw Interrupt Status	462
0x014	WDTMIS	RO	0x0000.0000	Watchdog Masked Interrupt Status	463
0x418	WDTTEST	R/W	0x0000.0000	Watchdog Test	464
0xC00	WDTLOCK	R/W	0x0000.0000	Watchdog Lock	465
0xFD0	WDTPeriphID4	RO	0x0000.0000	Watchdog Peripheral Identification 4	466
0xFD4	WDTPeriphID5	RO	0x0000.0000	Watchdog Peripheral Identification 5	467
0xFD8	WDTPeriphID6	RO	0x0000.0000	Watchdog Peripheral Identification 6	468
0xFDC	WDTPeriphID7	RO	0x0000.0000	Watchdog Peripheral Identification 7	469
0xFE0	WDTPeriphID0	RO	0x0000.0005	Watchdog Peripheral Identification 0	470
0xFE4	WDTPeriphID1	RO	0x0000.0018	Watchdog Peripheral Identification 1	471
0xFE8	WDTPeriphID2	RO	0x0000.0018	Watchdog Peripheral Identification 2	472
0xFEC	WDTPeriphID3	RO	0x0000.0001	Watchdog Peripheral Identification 3	473
0xFF0	WDTPrimeCellID0	RO	0x0000.000D	Watchdog PrimeCell Identification 0	474
0xFF4	WDTPrimeCellID1	RO	0x0000.00F0	Watchdog PrimeCell Identification 1	475
0xFF8	WDTPrimeCellID2	RO	0x0000.0006	Watchdog PrimeCell Identification 2	476
0xFFC	WDTPrimeCellID3	RO	0x0000.00B1	Watchdog PrimeCell Identification 3	477

## 13.5 Register Descriptions

The remainder of this section lists and describes the WDT registers, in numerical order by address offset.



## Register 1: Watchdog Load (WDTLOAD), offset 0x000

This register is the 32-bit interval value used by the 32-bit counter. When this register is written, the value is immediately loaded and the counter restarts counting down from the new value. If the **WDTLOAD** register is loaded with 0x0000.0000, an interrupt is immediately generated.

### Watchdog Load (WDTLOAD)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0x000

Type R/W, reset 0xFFFF.FFFF

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WDTLOAD															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WDTLOAD															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit/Field	Name	Type	Reset	Description
31:0	WDTLOAD	R/W	0xFFFF.FFFF	Watchdog Load Value

## Register 2: Watchdog Value (WDTVALUE), offset 0x004

This register contains the current count value of the timer.

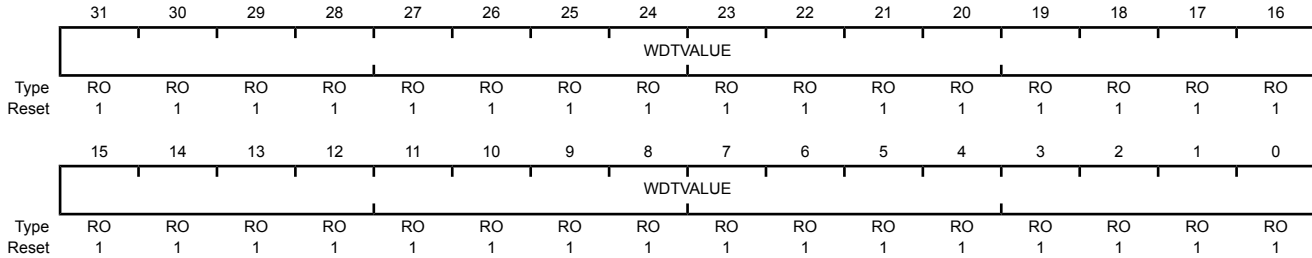
### Watchdog Value (WDTVALUE)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0x004

Type RO, reset 0xFFFF.FFFF



Bit/Field	Name	Type	Reset	Description
31:0	WDTVALUE	RO	0xFFFF.FFFF	Watchdog Value Current value of the 32-bit down counter.

### Register 3: Watchdog Control (WDTCTL), offset 0x008

This register is the watchdog control register. The watchdog timer can be configured to generate a reset signal (on second time-out) or an interrupt on time-out.

When the watchdog interrupt has been enabled, all subsequent writes to the control register are ignored. The only mechanism that can re-enable writes is a hardware reset.

**Important:** Because the Watchdog Timer 1 module has an independent clocking domain, its registers must be written with a timing gap between accesses. Software must guarantee that this delay is inserted between back-to-back writes to WDT1 registers or between a write followed by a read to the registers. The timing for back-to-back reads from the WDT1 module has no restrictions. The `WRC` bit in the **Watchdog Control (WDTCTL)** register for WDT1 indicates that the required timing gap has elapsed. This bit is cleared on a write operation and set once the write completes, indicating to software that another write or read may be started safely. Software should poll **WDTCTL** for `WRC=1` prior to accessing another register. Note that WDT0 does not have this restriction as it runs off the system clock and therefore does not have a `WRC` bit.

#### Watchdog Control (WDTCTL)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0x008

Type R/W, reset 0x0000.0000 (WDT0) and 0x8000.0000 (WDT1)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	WRC	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved														RESEN	INTEN	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
-----------	------	------	-------	-------------

31	WRC	RO	1	Write Complete
----	-----	----	---	----------------

The `WRC` values are defined as follows:

Value	Description
-------	-------------

0	A write access to one of the WDT1 registers is in progress.
---	---

1	A write access is not in progress, and WDT1 registers can be read or written.
---	---

**Note:** This bit is reserved for WDT0 and has a reset value of 0.

30:2	reserved	RO	0x000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
------	----------	----	-----------	---

Bit/Field	Name	Type	Reset	Description
1	RESEN	R/W	0	Watchdog Reset Enable The RESEN values are defined as follows:  Value Description 0 Disabled. 1 Enable the Watchdog module reset output.
0	INTEN	R/W	0	Watchdog Interrupt Enable The INTEN values are defined as follows:  Value Description 0 Interrupt event disabled (once this bit is set, it can only be cleared by a hardware reset). 1 Interrupt event enabled. Once enabled, all writes are ignored.

## Register 4: Watchdog Interrupt Clear (WDTICR), offset 0x00C

This register is the interrupt clear register. A write of any value to this register clears the Watchdog interrupt and reloads the 32-bit counter from the **WDTLOAD** register. Value for a read or reset is indeterminate.

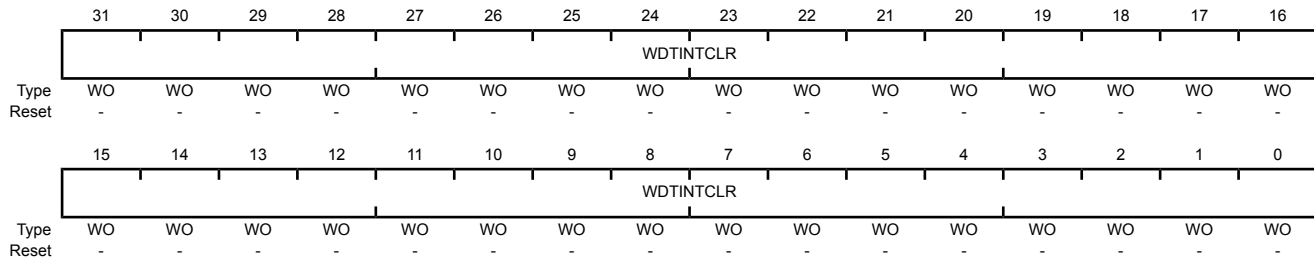
### Watchdog Interrupt Clear (WDTICR)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0x00C

Type WO, reset -



Bit/Field	Name	Type	Reset	Description
31:0	WDTINTCLR	WO	-	Watchdog Interrupt Clear

### Register 5: Watchdog Raw Interrupt Status (WDTRIS), offset 0x010

This register is the raw interrupt status register. Watchdog interrupt events can be monitored via this register if the controller interrupt is masked.

#### Watchdog Raw Interrupt Status (WDTRIS)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0x010  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															WDTRIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	WDTRIS	RO	0	Watchdog Raw Interrupt Status
				Value Description
				1 A watchdog time-out event has occurred.
				0 The watchdog has not timed out.

**Register 6: Watchdog Masked Interrupt Status (WDTMIS), offset 0x014**

This register is the masked interrupt status register. The value of this register is the logical AND of the raw interrupt bit and the Watchdog interrupt enable bit.

**Watchdog Masked Interrupt Status (WDTMIS)**

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0x014

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															WDTMIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	WDTMIS	RO	0	Watchdog Masked Interrupt Status
				Value Description
				1 A watchdog time-out event has been signalled to the interrupt controller.
				0 The watchdog has not timed out or the watchdog timer interrupt is masked.

### Register 7: Watchdog Test (WDTTEST), offset 0x418

This register provides user-enabled stalling when the microcontroller asserts the CPU halt flag during debug.

#### Watchdog Test (WDTTEST)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0x418  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							STALL	reserved							
Type	RO	RO	RO	RO	RO	RO	RO	R/W	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:9	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	STALL	R/W	0	Watchdog Stall Enable  Value Description 1 If the microcontroller is stopped with a debugger, the watchdog timer stops counting. Once the microcontroller is restarted, the watchdog timer resumes counting. 0 The watchdog timer continues counting if the microcontroller is stopped with a debugger.
7:0	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

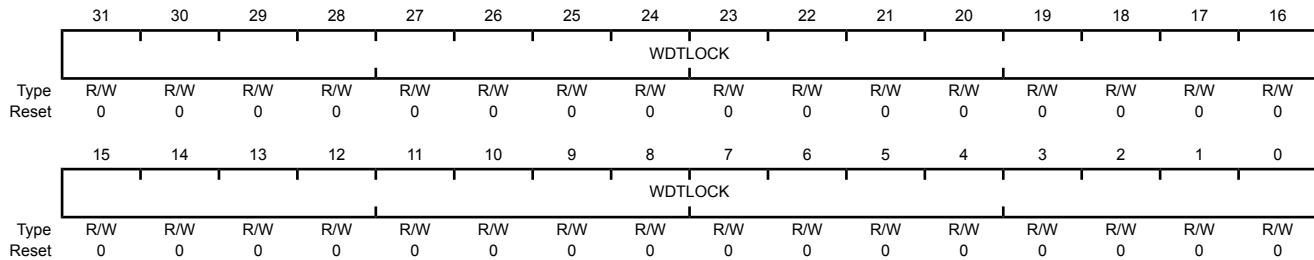


## Register 8: Watchdog Lock (WDTLOCK), offset 0xC00

Writing 0x1ACC.E551 to the **WDTLOCK** register enables write access to all other registers. Writing any other value to the **WDTLOCK** register re-enables the locked state for register writes to all the other registers. Reading the **WDTLOCK** register returns the lock status rather than the 32-bit value written. Therefore, when write accesses are disabled, reading the **WDTLOCK** register returns 0x0000.0001 (when locked; otherwise, the returned value is 0x0000.0000 (unlocked)).

### Watchdog Lock (WDTLOCK)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0xC00  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:0	WDTLOCK	R/W	0x0000.0000	Watchdog Lock

A write of the value 0x1ACC.E551 unlocks the watchdog registers for write access. A write of any other value reapplies the lock, preventing any register updates.

A read of this register returns the following values:

Value	Description
0x0000.0001	Locked
0x0000.0000	Unlocked

### Register 9: Watchdog Peripheral Identification 4 (WDTPeriphID4), offset 0xFD0

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

#### Watchdog Peripheral Identification 4 (WDTPeriphID4)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0xFD0  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID4							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID4	RO	0x00	WDT Peripheral ID Register [7:0]

## Register 10: Watchdog Peripheral Identification 5 (WDTPeriphID5), offset 0xFD4

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### Watchdog Peripheral Identification 5 (WDTPeriphID5)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0xFD4

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID5							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

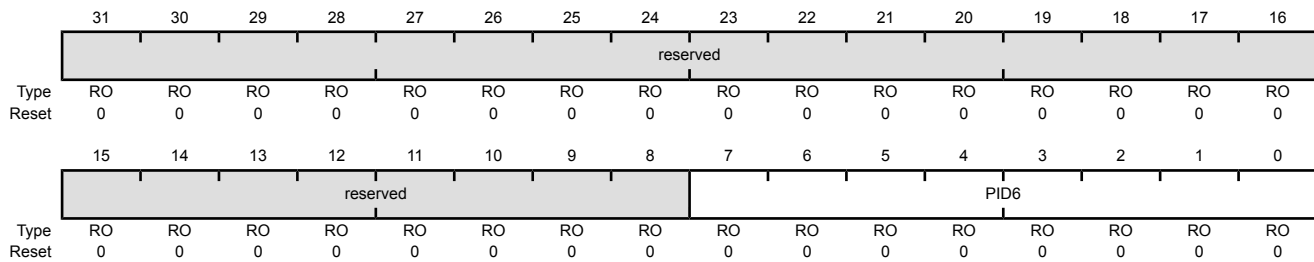
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID5	RO	0x00	WDT Peripheral ID Register [15:8]

## Register 11: Watchdog Peripheral Identification 6 (WDTPeriphID6), offset 0xFD8

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### Watchdog Peripheral Identification 6 (WDTPeriphID6)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0xFD8  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID6	RO	0x00	WDT Peripheral ID Register [23:16]

## Register 12: Watchdog Peripheral Identification 7 (WDTPeriphID7), offset 0xFDC

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### Watchdog Peripheral Identification 7 (WDTPeriphID7)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0xFDC

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID7							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID7	RO	0x00	WDT Peripheral ID Register [31:24]

### Register 13: Watchdog Peripheral Identification 0 (WDTPeriphID0), offset 0xFE0

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

#### Watchdog Peripheral Identification 0 (WDTPeriphID0)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0xFE0  
 Type RO, reset 0x0000.0005

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID0							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID0	RO	0x05	Watchdog Peripheral ID Register [7:0]

## Register 14: Watchdog Peripheral Identification 1 (WDTPeriphID1), offset 0xFE4

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### Watchdog Peripheral Identification 1 (WDTPeriphID1)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0xFE4

Type RO, reset 0x0000.0018

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID1							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID1	RO	0x18	Watchdog Peripheral ID Register [15:8]

## Register 15: Watchdog Peripheral Identification 2 (WDTPeriphID2), offset 0xFE8

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### Watchdog Peripheral Identification 2 (WDTPeriphID2)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0xFE8  
 Type RO, reset 0x0000.0018

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID2							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID2	RO	0x18	Watchdog Peripheral ID Register [23:16]



## Register 16: Watchdog Peripheral Identification 3 (WDTPeriphID3), offset 0xFEC

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### Watchdog Peripheral Identification 3 (WDTPeriphID3)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0xFEC

Type RO, reset 0x0000.0001

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID3	RO	0x01	Watchdog Peripheral ID Register [31:24]

### Register 17: Watchdog PrimeCell Identification 0 (WDTPCellID0), offset 0xFF0

The **WDTPCellIDn** registers are hard-coded and the fields within the register determine the reset value.

#### Watchdog PrimeCell Identification 0 (WDTPCellID0)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0xFF0  
 Type RO, reset 0x0000.000D

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved								CID0								
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID0	RO	0x0D	Watchdog PrimeCell ID Register [7:0]

**Register 18: Watchdog PrimeCell Identification 1 (WDTPCellID1), offset 0xFF4**

The **WDTPCellIDn** registers are hard-coded and the fields within the register determine the reset value.

## Watchdog PrimeCell Identification 1 (WDTPCellID1)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0xFF4

Type RO, reset 0x0000.00F0

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID1							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID1	RO	0xF0	Watchdog PrimeCell ID Register [15:8]

### Register 19: Watchdog PrimeCell Identification 2 (WDTPCellID2), offset 0xFF8

The **WDTPCellIDn** registers are hard-coded and the fields within the register determine the reset value.

#### Watchdog PrimeCell Identification 2 (WDTPCellID2)

WDT0 base: 0x4000.0000  
 WDT1 base: 0x4000.1000  
 Offset 0xFF8  
 Type RO, reset 0x0000.0006

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID2							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID2	RO	0x06	Watchdog PrimeCell ID Register [23:16]

**Register 20: Watchdog PrimeCell Identification 3 (WDTPCellID3), offset 0xFFC**

The **WDTPCellIDn** registers are hard-coded and the fields within the register determine the reset value.

## Watchdog PrimeCell Identification 3 (WDTPCellID3)

WDT0 base: 0x4000.0000

WDT1 base: 0x4000.1000

Offset 0xFFC

Type RO, reset 0x0000.00B1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID3	RO	0xB1	Watchdog PrimeCell ID Register [31:24]

## 14 Analog-to-Digital Converter (ADC)

An analog-to-digital converter (ADC) is a peripheral that converts a continuous analog voltage to a discrete digital number.

The Stellaris<sup>®</sup> ADC module features 10-bit conversion resolution and supports eight input channels, plus an internal temperature sensor. The ADC module contains four programmable sequencers allowing the sampling of multiple analog input sources without controller intervention. Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. A digital comparator function is included which allows the conversion value to be diverted to a digital comparator module. The digital comparator module provides eight digital comparators. The comparator module measures the ADC conversion value against two user-defined values to determine the operational range of the signal.

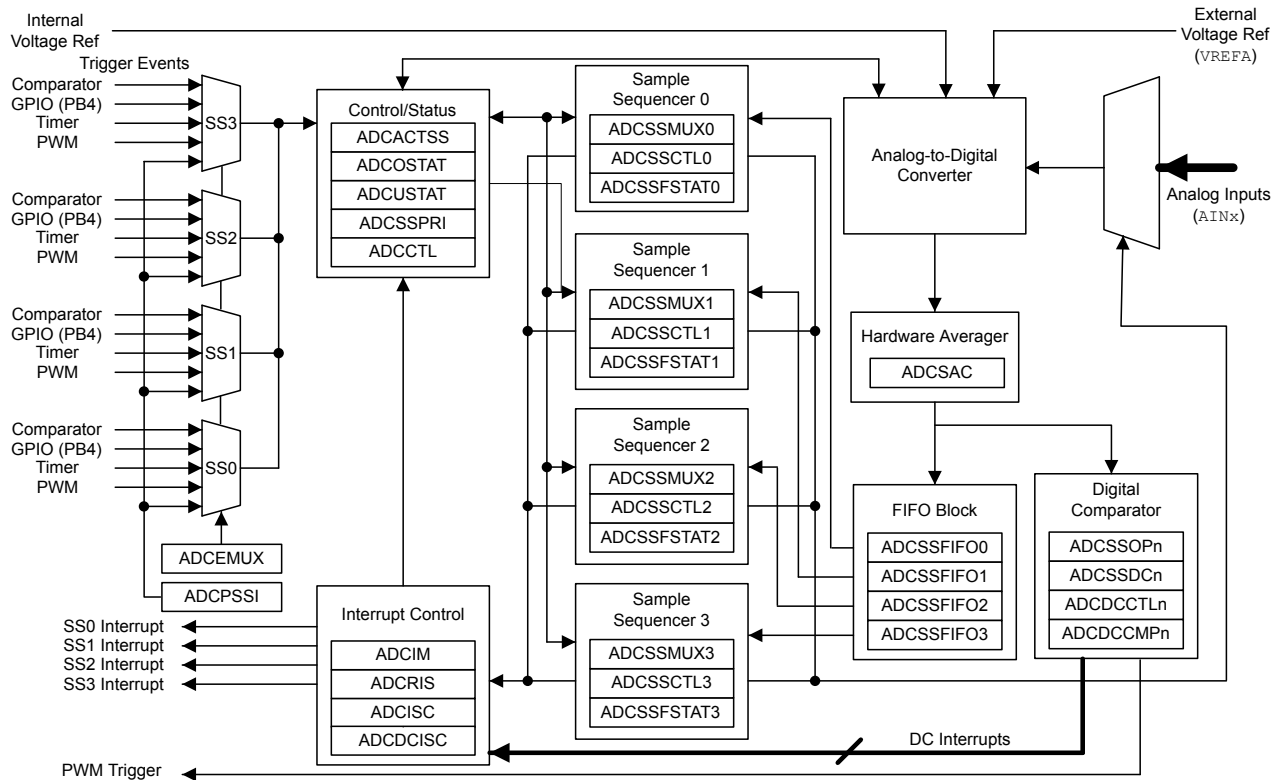
The Stellaris<sup>®</sup> LM3S1811 microcontroller provides one ADC module with the following features:

- Eight analog input channels
- Single-ended and differential-input configurations
- On-chip internal temperature sensor
- Sample rate of one million samples/second
- Flexible, configurable analog-to-digital conversion
- Four programmable sample conversion sequencers from one to eight entries long, with corresponding conversion result FIFOs
- Flexible trigger control
  - Controller (software)
  - Timers
  - Analog Comparators
  - GPIO
- Hardware averaging of up to 64 samples for improved accuracy
- Digital comparison unit providing eight digital comparators
- Converter uses an internal 3-V reference
- Power and ground for the analog circuitry is separate from the digital power and ground
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Dedicated channel for each sample sequencer
  - Burst request asserted when interrupt is triggered

## 14.1 Block Diagram

Figure 14-1 on page 479 provides details on the internal configuration of the ADC controls and data registers.

Figure 14-1. ADC Module Block Diagram



## 14.2 Signal Description

Table 14-1 on page 479 lists the external signals of the ADC module and describes the function of each. The ADC signals are analog functions for some GPIO signals. The column in the table below titled "Pin Mux/Pin Assignment" lists the GPIO pin placement for the ADC signals. Note that when a pin is used as an ADC input, the appropriate bit in the **GPIO Analog Mode Select (GPIOAMSEL)** register must be set to disable the analog isolation circuit, and the appropriate bit in the **GPIO Digital Enable (GPIODEN)** register must be clear to disable digital function. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 288.

Table 14-1. Signals for ADC

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
AIN0	1	PE7	I	Analog	Analog-to-digital converter input 0.
AIN1	2	PE6	I	Analog	Analog-to-digital converter input 1.
AIN2	5	PE5	I	Analog	Analog-to-digital converter input 2.
AIN3	6	PE4	I	Analog	Analog-to-digital converter input 3.
AIN4	100	PD7	I	Analog	Analog-to-digital converter input 4.
AIN5	99	PD6	I	Analog	Analog-to-digital converter input 5.

Table 14-1. Signals for ADC (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
AIN6	98	PD5	I	Analog	Analog-to-digital converter input 6.
AIN7	97	PD4	I	Analog	Analog-to-digital converter input 7.
VREFA	90	PB6	I	Analog	This input provides a reference voltage used to specify the input voltage at which the ADC converts to a maximum value. In other words, the voltage that is applied to VREFA is the voltage with which an AIN <sub>n</sub> signal is converted to 1023. The VREFA input is limited to the range specified in Table 22-2 on page 726.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 14.3 Functional Description

The Stellaris<sup>®</sup> ADC collects sample data by using a programmable sequence-based approach instead of the traditional single or double-sampling approaches found on many ADC modules. Each *sample sequence* is a fully programmed series of consecutive (back-to-back) samples, allowing the ADC to collect data from multiple input sources without having to be re-configured or serviced by the processor. The programming of each sample in the sample sequence includes parameters such as the input source and mode (differential versus single-ended input), interrupt generation on sample completion, and the indicator for the last sample in the sequence. The  $\mu$ DMA can be used to more efficiently move data from the sample sequencers without CPU intervention.

### 14.3.1 Sample Sequencers

The sampling control and data capture is handled by the sample sequencers. All of the sequencers are identical in implementation except for the number of samples that can be captured and the depth of the FIFO. Table 14-2 on page 480 shows the maximum number of samples that each sequencer can capture and its corresponding FIFO depth. In this implementation, each FIFO entry is a 32-bit word, with the lower 10 bits containing the conversion result.

Table 14-2. Samples and FIFO Depth of Sequencers

Sequencer	Number of Samples	Depth of FIFO
SS3	1	1
SS2	4	4
SS1	4	4
SS0	8	8

For a given sample sequence, each sample is defined by two 4-bit nibbles in the **ADC Sample Sequence Input Multiplexer Select (ADCSSMUX<sub>n</sub>)** and **ADC Sample Sequence Control (ADCSSCTL<sub>n</sub>)** registers, where "n" corresponds to the sequence number. The **ADCSSMUX<sub>n</sub>** nibbles select the input pin, while the **ADCSSCTL<sub>n</sub>** nibbles contain the sample control bits corresponding to parameters such as temperature sensor selection, interrupt enable, end of sequence, and differential input mode. Sample sequencers are enabled by setting the respective **ASEN<sub>n</sub>** bit in the **ADC Active Sample Sequencer (ADCACTSS)** register and should be configured before being enabled. Sampling is then initiated by setting the **SS<sub>n</sub>** bit in the **ADC Processor Sample Sequence Initiate (ADCPSSI)** register.

When configuring a sample sequence, multiple uses of the same input pin within the same sequence is allowed. In the **ADCSSCTL<sub>n</sub>** register, the **IE<sub>n</sub>** bits can be set for any combination of samples,



allowing interrupts to be generated after every sample in the sequence if necessary. Also, the `END` bit can be set at any point within a sample sequence. For example, if Sequencer 0 is used, the `END` bit can be set in the nibble associated with the fifth sample, allowing Sequencer 0 to complete execution of the sample sequence after the fifth sample.

After a sample sequence completes execution, the result data can be retrieved from the **ADC Sample Sequence Result FIFO (ADCSSFIFO<sub>n</sub>)** registers. The FIFOs are simple circular buffers that read a single address to "pop" result data. For software debug purposes, the positions of the FIFO head and tail pointers are visible in the **ADC Sample Sequence FIFO Status (ADCSSFSTAT<sub>n</sub>)** registers along with `FULL` and `EMPTY` status flags. Overflow and underflow conditions are monitored using the **ADCOSTAT** and **ADCUSTAT** registers.

### 14.3.2 Module Control

Outside of the sample sequencers, the remainder of the control logic is responsible for tasks such as:

- Interrupt generation
- Sequence prioritization
- Trigger configuration
- Comparator configuration

Most of the ADC control logic runs at the ADC clock rate of 14-18 MHz. The internal ADC divider is configured for 16-MHz operation automatically by hardware when the system `XTAL` is selected.

#### 14.3.2.1 Interrupts

The register configurations of the sample sequencers and digital comparators dictate which events generate raw interrupts, but do not have control over whether the interrupt is actually sent to the interrupt controller. The ADC module's interrupt signals are controlled by the state of the `MASK` bits in the **ADC Interrupt Mask (ADCIM)** register. Interrupt status can be viewed at two locations: the **ADC Raw Interrupt Status (ADCRIS)** register, which shows the raw status of the various interrupt signals; and the **ADC Interrupt Status and Clear (ADCISC)** register, which shows active interrupts that are enabled by the **ADCIM** register. Sequencer interrupts are cleared by writing a 1 to the corresponding `IN` bit in **ADCISC**. Digital comparator interrupts are cleared by writing a 1 to the **ADC Digital Comparator Interrupt Status and Clear (ADCDCISC)** register.

#### 14.3.2.2 DMA Operation

The ADC module provides a request signal to the  $\mu$ DMA controller for each sample sequencer. Each sample sequencer has a dedicated  $\mu$ DMA channel. The request signal is a burst type and is asserted whenever an interrupt is enabled in a sample sequence (`IE` bit in the **ADCSSCTL<sub>n</sub>** register is set). Single requests are not supported.

The arbitration size of the  $\mu$ DMA transfer must be a power of 2, and the associated `IE` bits in the **ADDCSCTL<sub>n</sub>** register must be set. For example, if the  $\mu$ DMA channel of SS0 has an arbitration size of four, the `IE3` bit (4th sample) and the `IE7` bit (8th sample) must be set. Thus the  $\mu$ DMA request occurs every time 4 samples have been acquired. No other special steps are needed to enable the ADC module for  $\mu$ DMA operation.

Refer to the "Micro Direct Memory Access ( $\mu$ DMA)" on page 230 for more details about programming the  $\mu$ DMA controller.

### 14.3.2.3 Prioritization

When sampling events (triggers) happen concurrently, they are prioritized for processing by the values in the **ADC Sample Sequencer Priority (ADCSSPRI)** register. Valid priority values are in the range of 0-3, with 0 being the highest priority and 3 being the lowest. Multiple active sample sequencer units with the same priority do not provide consistent results, so software must ensure that all active sample sequencer units have a unique priority value.

### 14.3.2.4 Sampling Events

Sample triggering for each sample sequencer is defined in the **ADC Event Multiplexer Select (ADCEMUX)** register. Trigger sources include processor (default), analog comparators, an external signal on GPIO  $PB4$ , a GP Timer, and continuous sampling. Software can initiate sampling by setting the  $SS_x$  bits in the **ADC Processor Sample Sequence Initiate (ADCPSSI)** register.

Care must be taken when using the continuous sampling trigger. If a sequencer's priority is too high, it is possible to starve other lower priority sequencers.

## 14.3.3 Hardware Sample Averaging Circuit

Higher precision results can be generated using the hardware averaging circuit, however, the improved results are at the cost of throughput. Up to 64 samples can be accumulated and averaged to form a single data entry in the sequencer FIFO. Throughput is decreased proportionally to the number of samples in the averaging calculation. For example, if the averaging circuit is configured to average 16 samples, the throughput is decreased by a factor of 16.

By default the averaging circuit is off, and all data from the converter passes through to the sequencer FIFO. The averaging hardware is controlled by the **ADC Sample Averaging Control (ADCSAC)** register (see page 513). A single averaging circuit has been implemented, thus all input channels receive the same amount of averaging whether they are single-ended or differential.

## 14.3.4 Analog-to-Digital Converter

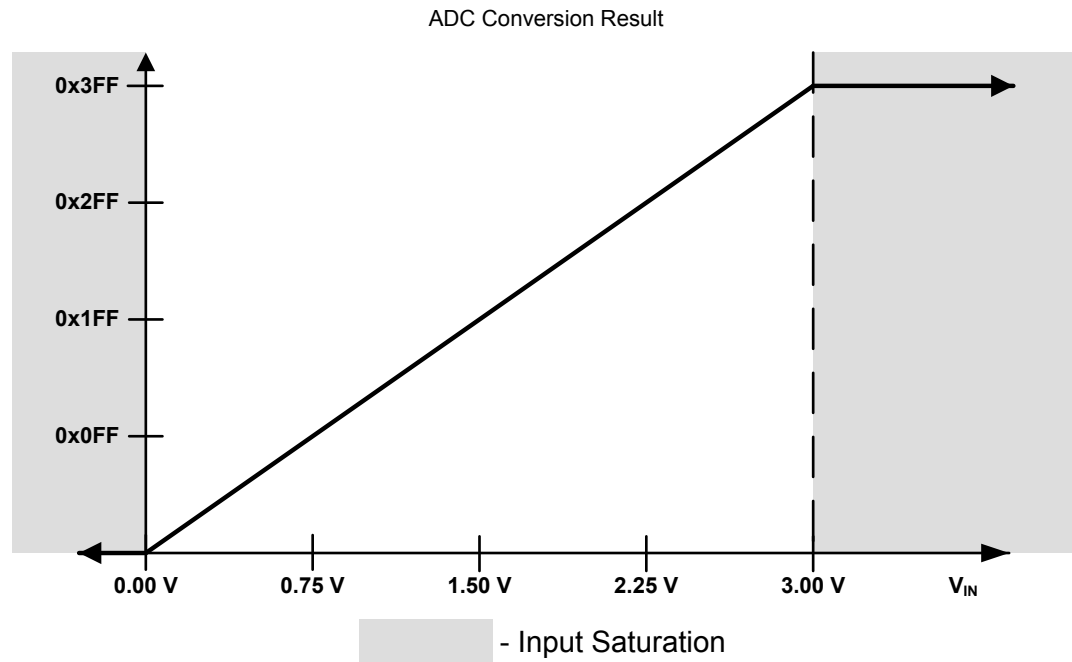
The Analog-to-Digital Converter (ADC) module uses a Successive Approximation Register (SAR) architecture to deliver a 10-bit, low-power, high-precision conversion value. The successive-approximation algorithm uses a current mode D/A converter to achieve lower settling time, resulting in higher conversion speeds for the A/D converter. In addition, built-in sample-and-hold circuitry with offset-calibration circuitry improves conversion accuracy. The ADC must be run from the PLL or a 14- to 18-MHz clock source.

The ADC operates from the 3.3-V analog and 1.2-V digital power supply. Integrated shutdown modes are available to reduce power consumption when ADC conversions are not required. The analog inputs are connected to the ADC through custom pads and specially balanced input paths to minimize the distortion on the inputs. Detailed information on the ADC power supplies and analog inputs can be found in "Analog-to-Digital Converter" on page 741.

### 14.3.4.1 Internal Voltage Reference

The band-gap circuitry generates an internal 3.0 V reference that is used by the ADC to produce a conversion value from the selected analog input. The range of this conversion value is from 0x000 to 0x3FF. In single-ended-input mode, the 0x000 value corresponds to an analog input voltage of 0.0 V; the 0x3FF value corresponds to an analog input voltage of 3.0 V. This configuration results in a resolution of approximately 2.9 mV per ADC code. While the analog input pads can handle voltages beyond this range, the ADC conversions saturate in under-voltage and over-voltage cases. Figure 14-2 on page 483 shows the ADC conversion function of the analog inputs.

Figure 14-2. Internal Voltage Conversion Result



### 14.3.5 Differential Sampling

In addition to traditional single-ended sampling, the ADC module supports differential sampling of two analog input channels. To enable differential sampling, software must set the  $D_n$  bit in the **ADCSSCTL0n** register in a step's configuration nibble.

When a sequence step is configured for differential sampling, the input pair to sample must be configured in the **ADCSSMUXn** register. Differential pair 0 samples analog inputs 0 and 1; differential pair 1 samples analog inputs 2 and 3; and so on (see Table 14-3 on page 483). The ADC does not support other differential pairings such as analog input 0 with analog input 3.

**Table 14-3. Differential Sampling Pairs**

Differential Pair	Analog Inputs
0	0 and 1
1	2 and 3
2	4 and 5
3	6 and 7

The voltage sampled in differential mode is the difference between the odd and even channels:

$\Delta V$  (differential voltage) =  $V_{IN\_EVEN}$  (even channels) –  $V_{IN\_ODD}$  (odd channels), therefore:

- If  $\Delta V = 0$ , then the conversion result = 0x1FF
- If  $\Delta V > 0$ , then the conversion result > 0x1FF (range is 0x1FF–0x3FF)
- If  $\Delta V < 0$ , then the conversion result < 0x1FF (range is 0–0x1FF)

The differential pairs assign polarities to the analog inputs: the even-numbered input is always positive, and the odd-numbered input is always negative. In order for a valid conversion result to appear, the negative input must be in the range of  $\pm 1.5$  V of the positive input. If an analog input is greater than 3 V or less than 0 V (the valid range for analog inputs), the input voltage is clipped, meaning it appears as either 3 V or 0 V, respectively, to the ADC.

Figure 14-3 on page 484 shows an example of the negative input centered at 1.5 V. In this configuration, the differential range spans from -1.5 V to 1.5 V. Figure 14-4 on page 485 shows an example where the negative input is centered at -0.75 V, meaning inputs on the positive input saturate past a differential voltage of -0.75 V since the input voltage is less than 0 V. Figure 14-5 on page 485 shows an example of the negative input centered at 2.25 V, where inputs on the positive channel saturate past a differential voltage of 0.75 V since the input voltage would be greater than 3 V.

**Figure 14-3. Differential Sampling Range,  $V_{IN\_ODD} = 1.5$  V**

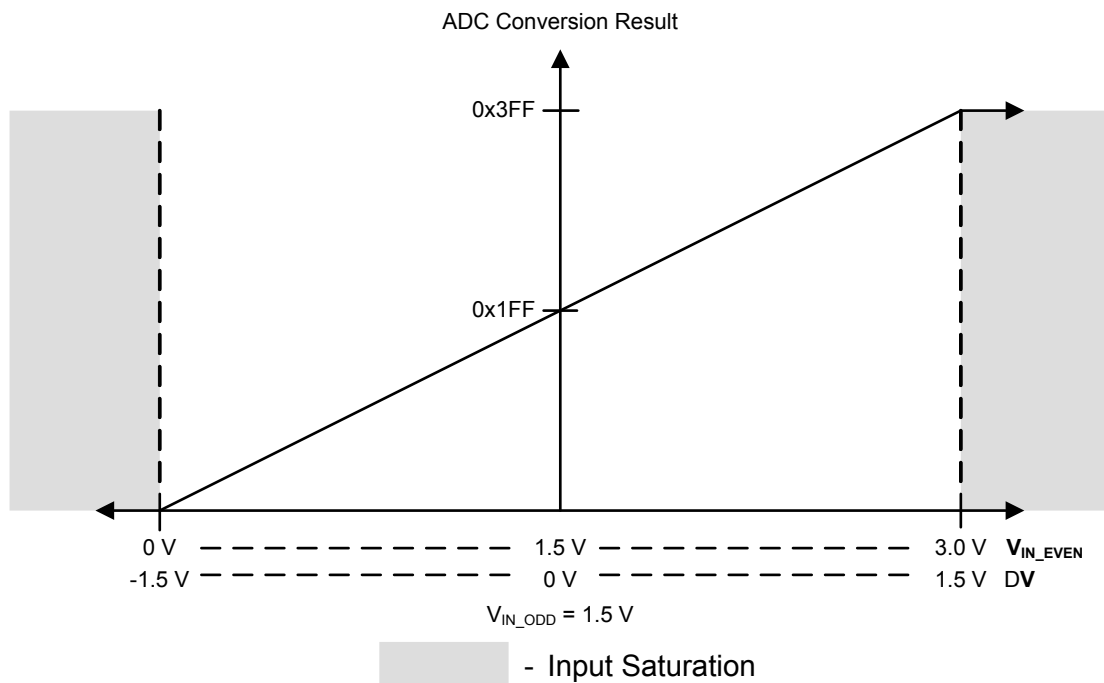


Figure 14-4. Differential Sampling Range,  $V_{IN\_ODD} = 0.75\text{ V}$

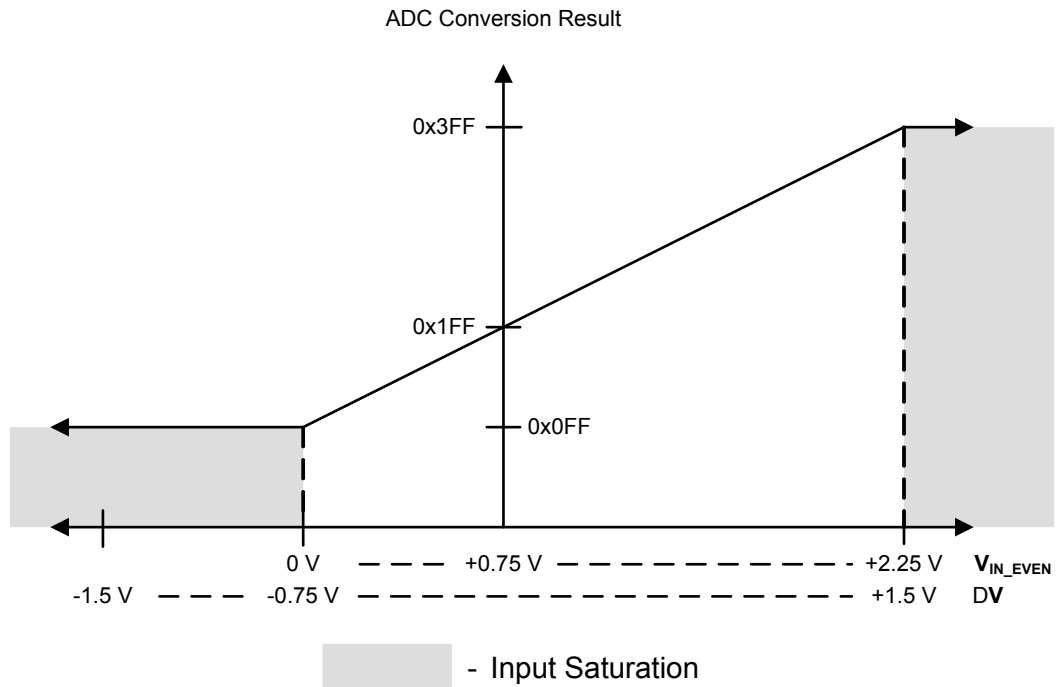
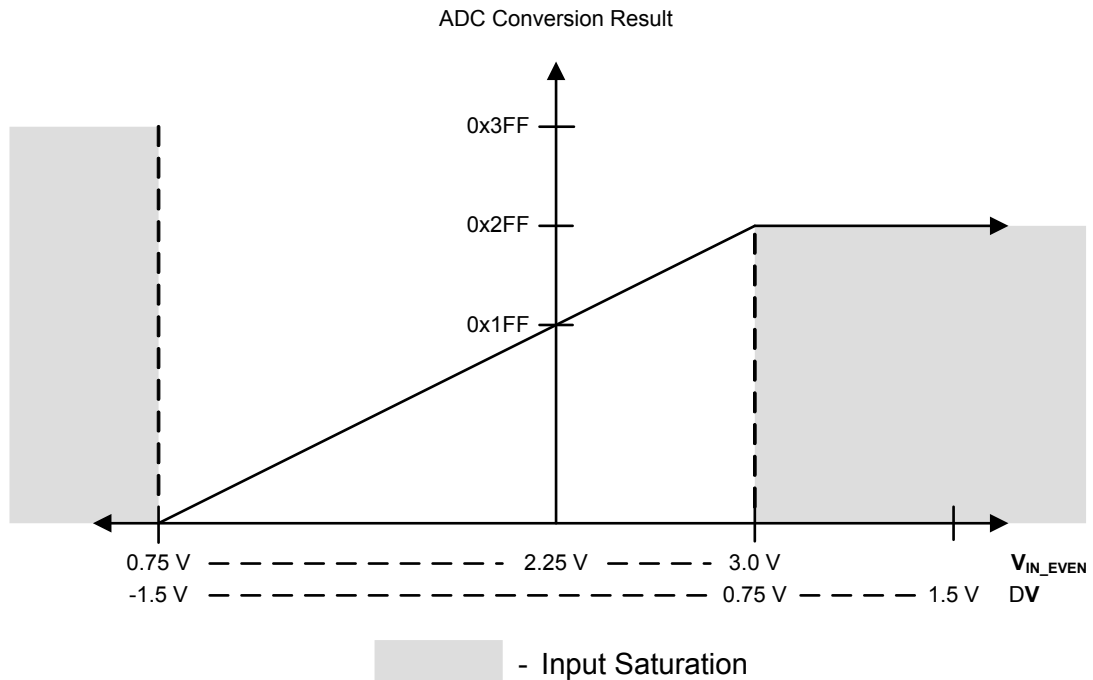


Figure 14-5. Differential Sampling Range,  $V_{IN\_ODD} = 2.25\text{ V}$



### 14.3.6 Internal Temperature Sensor

The temperature sensor serves two primary purposes: 1) to notify the system that internal temperature is too high or low for reliable operation and 2) to provide temperature measurements for calibration of the Hibernate module RTC trim value.

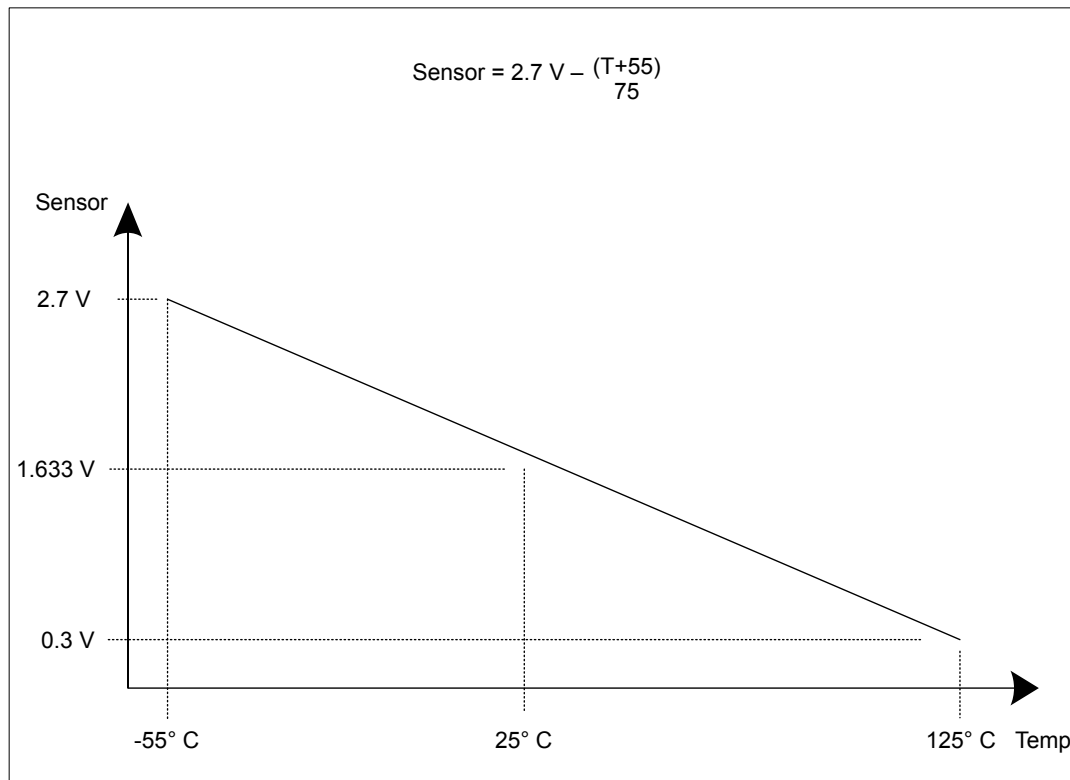
The temperature sensor does not have a separate enable, because it also contains the bandgap reference and must always be enabled. The reference is supplied to other analog modules; not just the ADC. In addition, the temperature sensor has a second power-down input in the 3.3 V domain which provides control by the Hibernation module.

The internal temperature sensor provides an analog temperature reading as well as a reference voltage. The voltage at the output terminal *SENSO* is given by the following equation:

$$SENSO = 2.7 - ((T + 55) / 75)$$

This relation is shown in Figure 14-6 on page 486.

**Figure 14-6. Internal Temperature Sensor Characteristic**



The temperature reading from the temperature sensor can also be given as a function of the ADC value. The following formula calculates temperature (in °C) based on the ADC reading:

$$Temperature = 147.5 - ((225 \times ADC) / 1023)$$

### 14.3.7 Digital Comparator Unit

An ADC is commonly used to sample an external signal and to monitor its value to ensure that it remains in a given range. To automate this monitoring procedure and reduce the amount of processor overhead that is required, eight digital comparators are provided. Conversions from the ADC that are sent to the digital comparators are compared against the user programmable limits in the **ADC**

**Digital Comparator Range (ADCDCMPn)** registers. If the observed signal moves out of the acceptable range, a processor interrupt can be generated. The digital comparators four operational modes (Once, Always, Hysteresis Once, Hysteresis Always) can be applied to three separate regions (low band, mid band, high band) as defined by the user.

#### 14.3.7.1 Output Functions

ADC conversions can either be stored in the ADC Sample Sequence FIFOs or compared using the digital comparator resources as defined by the  $S_nDCOP$  bits in the **ADC Sample Sequence n Operation (ADCSSOPn)** register. These selected ADC conversions are used by their respective digital comparator to monitor the external signal. Each comparator has two possible output functions: processor interrupts and triggers.

Each function has its own state machine to track the monitored signal. Even though the interrupt and trigger functions can be enabled individually or both at the same time, the same conversion data is used by each function to determine if the right conditions have been met to assert the associated output.

##### **Interrupts**

The digital comparator interrupt function is enabled by setting the  $CIE$  bit in the **ADC Digital Comparator Control (ADCDCCTLn)** register. This bit enables the interrupt function state machine to start monitoring the incoming ADC conversions. When the appropriate set of conditions is met, and the  $DCONSS_x$  bit is set in the **ADCIM** register, an interrupt is sent to the interrupt controller.

##### **Triggers**

The digital comparator trigger function is enabled by setting the  $CTE$  bit in the **ADCDCCTLn** register. This bit enables the trigger function state machine to start monitoring the incoming ADC conversions. When the appropriate set of conditions is met, the corresponding digital comparator trigger to the PWM module is asserted.

#### 14.3.7.2 Operational Modes

Four operational modes are provided to support a broad range of applications and multiple possible signaling requirements: Always, Once, Hysteresis Always, and Hysteresis Once. The operational mode is selected using the  $CIM$  or  $CTM$  field in the **ADCDCCTLn** register.

##### **Always Mode**

In the Always operational mode, the associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria. The result is a string of assertions on the interrupt or trigger while the conversions are within the appropriate range.

##### **Once Mode**

In the Once operational mode, the associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria, and the previous ADC conversion value did not. The result is a single assertion of the interrupt or trigger when the conversions are within the appropriate range.

##### **Hysteresis-Always Mode**

The Hysteresis-Always operational mode can only be used in conjunction with the low-band or high-band regions because the mid-band region must be crossed and the opposite region entered to clear the hysteresis condition. In the Hysteresis-Always mode, the associated interrupt or trigger is asserted in the following cases: 1) the ADC conversion value meets its comparison criteria or 2)

a previous ADC conversion value has met the comparison criteria, and the hysteresis condition has not been cleared by entering the opposite region. The result is a string of assertions on the interrupt or trigger that continue until the opposite region is entered.

#### **Hysteresis-Once Mode**

The Hysteresis-Once operational mode can only be used in conjunction with the low-band or high-band regions because the mid-band region must be crossed and the opposite region entered to clear the hysteresis condition. In the Hysteresis-Once mode, the associated interrupt or trigger is asserted only when the ADC conversion value meets its comparison criteria, the hysteresis condition is clear, and the previous ADC conversion did not meet the comparison criteria. The result is a single assertion on the interrupt or trigger.

### **14.3.7.3 Function Ranges**

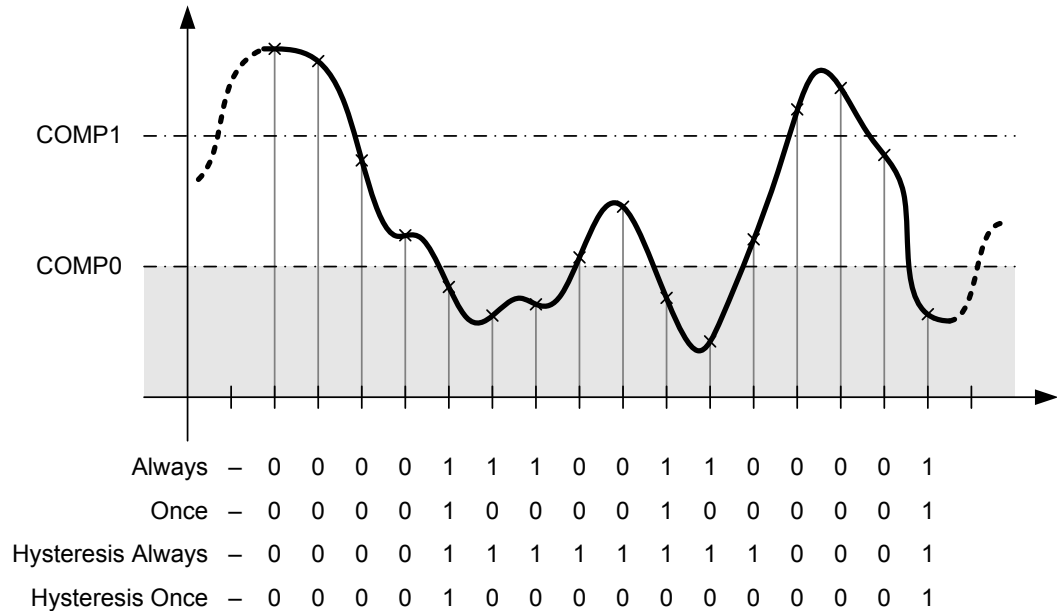
The two comparison values, `COMP0` and `COMP1`, in the **ADC Digital Comparator Range (ADCDCMPn)** register effectively break the conversion area into three distinct regions. These regions are referred to as the low-band (less than or equal to `COMP0`), mid-band (greater than `COMP0` but less than or equal to `COMP1`), and high-band (greater than `COMP1`) regions. `COMP0` and `COMP1` may be programmed to the same value, effectively creating two regions, but `COMP1` must always be greater than or equal to the value of `COMP0`. A `COMP1` value that is less than `COMP0` generates unpredictable results.

#### **Low-Band Operation**

To operate in the low-band region, either the `CIC` field or the `CTC` field in the **ADCDCCTLn** register must be programmed to `0x0`. This setting causes interrupts or triggers to be generated in the low-band region as defined by the programmed operational mode. An example of the state of the interrupt/trigger signal in the low-band region for each of the operational modes is shown in Figure 14-7 on page 489. Note that a "0" in a column following the operational mode name (Always, Once, Hysteresis Always, and Hysteresis Once) indicates that the interrupt or trigger signal is de-asserted and a "1" indicates that the signal is asserted.



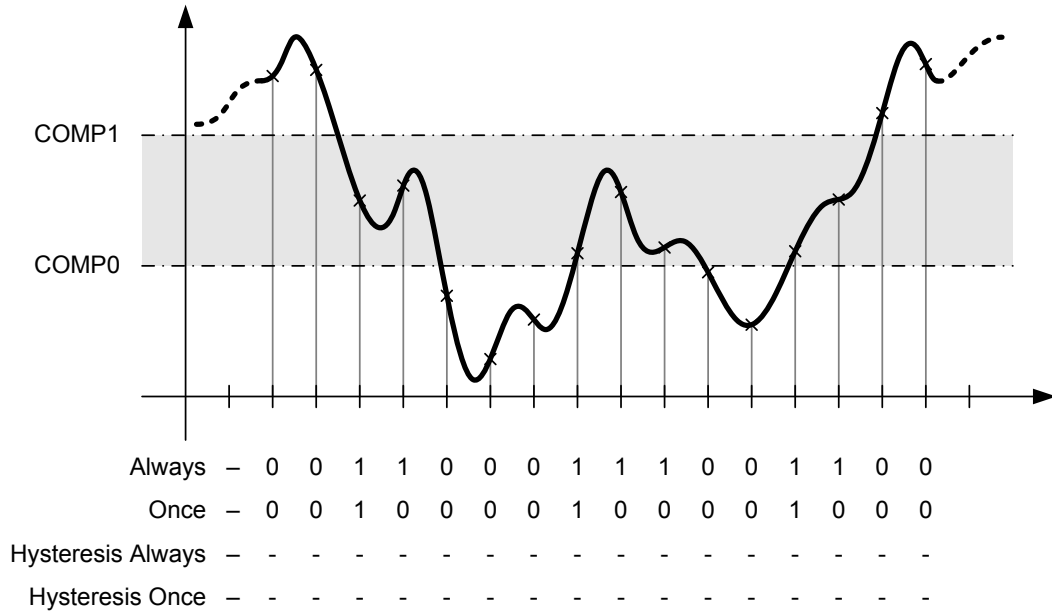
Figure 14-7. Low-Band Operation (CIC=0x0 and/or CTC=0x0)



### Mid-Band Operation

To operate in the mid-band region, either the `CIC` field or the `CTC` field in the `ADCDCCTLn` register must be programmed to `0x1`. This setting causes interrupts or triggers to be generated in the mid-band region according to the operation mode. Only the Always and Once operational modes are available in the mid-band region. An example of the state of the interrupt/trigger signal in the mid-band region for each of the allowed operational modes is shown in Figure 14-8 on page 490. Note that a "0" in a column following the operational mode name (Always or Once) indicates that the interrupt or trigger signal is de-asserted and a "1" indicates that the signal is asserted.

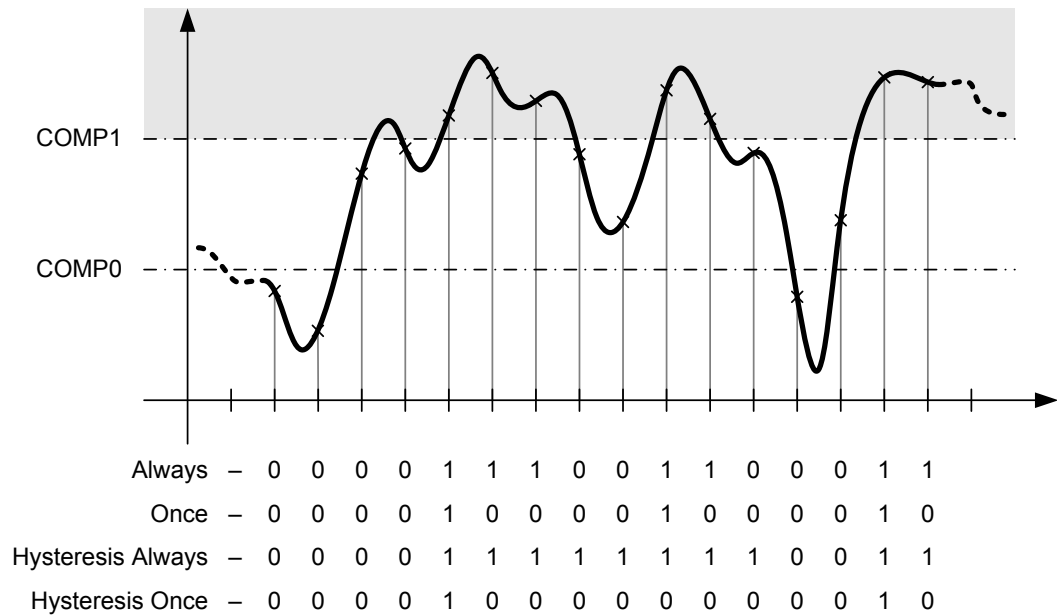
Figure 14-8. Mid-Band Operation (CIC=0x1 and/or CTC=0x1)



**High-Band Operation**

To operate in the high-band region, either the `CIC` field or the `CTC` field in the `ADCDCCTLn` register must be programmed to 0x3. This setting causes interrupts or triggers to be generated in the high-band region according to the operation mode. An example of the state of the interrupt/trigger signal in the high-band region for each of the allowed operational modes is shown in Figure 14-9 on page 491. Note that a "0" in a column following the operational mode name (Always, Once, Hysteresis Always, and Hysteresis Once) indicates that the interrupt or trigger signal is de-asserted and a "1" indicates that the signal is asserted.

Figure 14-9. High-Band Operation (CIC=0x3 and/or CTC=0x3)



## 14.4 Initialization and Configuration

In order for the ADC module to be used, the PLL must be enabled and programmed to a supported crystal frequency in the **RCC** register (see page 107). Using unsupported frequencies can cause faulty operation in the ADC module.

### 14.4.1 Module Initialization

Initialization of the ADC module is a simple process with very few steps: enabling the clock to the ADC, disabling the analog isolation circuit associated with all inputs that are to be used, and reconfiguring the sample sequencer priorities (if needed).

The initialization sequence for the ADC is as follows:

1. Enable the ADC clock by writing a value of 0x0001.0000 to the **RCGC0** register (see page 143).
2. Enable the clock to the appropriate GPIO module via the **RCGC2** register (see page 158). To find out which GPIO port to enable, refer to Table 20-5 on page 722.
3. Set the GPIO **AFSEL** bits for the ADC input pins (see page 310). To determine which GPIOs to configure, see Table 20-4 on page 717.
4. Configure the **PMCn** fields in the **GPIOPCTL** register to assign the **AINx** signals to the appropriate pins (see page 328 and Table 20-5 on page 722).
5. Disable the analog isolation circuit for all ADC input pins that are to be used by writing a 1 to the appropriate bits of the **GPIOAMSEL** register (see page 326) in the associated GPIO block.

- If required by the application, reconfigure the sample sequencer priorities in the **ADCSSPRI** register. The default configuration has Sample Sequencer 0 with the highest priority and Sample Sequencer 3 as the lowest priority.

#### 14.4.2 Sample Sequencer Configuration

Configuration of the sample sequencers is slightly more complex than the module initialization because each sample sequencer is completely programmable.

The configuration for each sample sequencer should be as follows:

- Ensure that the sample sequencer is disabled by clearing the corresponding **ASEN<sub>n</sub>** bit in the **ADCACTSS** register. Programming of the sample sequencers is allowed without having them enabled. Disabling the sequencer during programming prevents erroneous execution if a trigger event were to occur during the configuration process.
- Configure the trigger event for the sample sequencer in the **ADCEMUX** register.
- For each sample in the sample sequence, configure the corresponding input source in the **ADCSSMUX<sub>n</sub>** register.
- For each sample in the sample sequence, configure the sample control bits in the corresponding nibble in the **ADCSSCTL<sub>n</sub>** register. When programming the last nibble, ensure that the **END** bit is set. Failure to set the **END** bit causes unpredictable behavior.
- If interrupts are to be used, set the corresponding **MASK** bit in the **ADCIM** register.
- Enable the sample sequencer logic by setting the corresponding **ASEN<sub>n</sub>** bit in the **ADCACTSS** register.

### 14.5 Register Map

Table 14-4 on page 492 lists the ADC registers. The offset listed is a hexadecimal increment to the register's address, relative to the ADC base address of 0x4003.8000. Note that the ADC module clock must be enabled before the registers can be programmed (see page 143).

**Table 14-4. ADC Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	ADCACTSS	R/W	0x0000.0000	ADC Active Sample Sequencer	495
0x004	ADCRIS	RO	0x0000.0000	ADC Raw Interrupt Status	496
0x008	ADCIM	R/W	0x0000.0000	ADC Interrupt Mask	498
0x00C	ADCISC	R/W1C	0x0000.0000	ADC Interrupt Status and Clear	500
0x010	ADCOSTAT	R/W1C	0x0000.0000	ADC Overflow Status	503
0x014	ADCEMUX	R/W	0x0000.0000	ADC Event Multiplexer Select	505
0x018	ADCUSTAT	R/W1C	0x0000.0000	ADC Underflow Status	508
0x020	ADCSSPRI	R/W	0x0000.3210	ADC Sample Sequencer Priority	509
0x028	ADCPSSI	WO	-	ADC Processor Sample Sequence Initiate	511
0x030	ADCSAC	R/W	0x0000.0000	ADC Sample Averaging Control	513

Table 14-4. ADC Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0x034	ADCDCISC	R/W1C	0x0000.0000	ADC Digital Comparator Interrupt Status and Clear	514
0x040	ADCSSMUX0	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 0	516
0x044	ADCSSCTL0	R/W	0x0000.0000	ADC Sample Sequence Control 0	518
0x048	ADCSSFIFO0	RO	0x0000.0000	ADC Sample Sequence Result FIFO 0	521
0x04C	ADCSSFSTAT0	RO	0x0000.0100	ADC Sample Sequence FIFO 0 Status	522
0x050	ADCSSOP0	R/W	0x0000.0000	ADC Sample Sequence 0 Operation	524
0x054	ADCSSDC0	R/W	0x0000.0000	ADC Sample Sequence 0 Digital Comparator Select	526
0x060	ADCSSMUX1	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 1	528
0x064	ADCSSCTL1	R/W	0x0000.0000	ADC Sample Sequence Control 1	529
0x068	ADCSSFIFO1	RO	0x0000.0000	ADC Sample Sequence Result FIFO 1	521
0x06C	ADCSSFSTAT1	RO	0x0000.0100	ADC Sample Sequence FIFO 1 Status	522
0x070	ADCSSOP1	R/W	0x0000.0000	ADC Sample Sequence 1 Operation	531
0x074	ADCSSDC1	R/W	0x0000.0000	ADC Sample Sequence 1 Digital Comparator Select	532
0x080	ADCSSMUX2	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 2	528
0x084	ADCSSCTL2	R/W	0x0000.0000	ADC Sample Sequence Control 2	529
0x088	ADCSSFIFO2	RO	0x0000.0000	ADC Sample Sequence Result FIFO 2	521
0x08C	ADCSSFSTAT2	RO	0x0000.0100	ADC Sample Sequence FIFO 2 Status	522
0x090	ADCSSOP2	R/W	0x0000.0000	ADC Sample Sequence 2 Operation	531
0x094	ADCSSDC2	R/W	0x0000.0000	ADC Sample Sequence 2 Digital Comparator Select	532
0x0A0	ADCSSMUX3	R/W	0x0000.0000	ADC Sample Sequence Input Multiplexer Select 3	534
0x0A4	ADCSSCTL3	R/W	0x0000.0002	ADC Sample Sequence Control 3	535
0x0A8	ADCSSFIFO3	RO	0x0000.0000	ADC Sample Sequence Result FIFO 3	521
0x0AC	ADCSSFSTAT3	RO	0x0000.0100	ADC Sample Sequence FIFO 3 Status	522
0x0B0	ADCSSOP3	R/W	0x0000.0000	ADC Sample Sequence 3 Operation	536
0x0B4	ADCSSDC3	R/W	0x0000.0000	ADC Sample Sequence 3 Digital Comparator Select	537
0xD00	ADCDCRIC	R/W	0x0000.0000	ADC Digital Comparator Reset Initial Conditions	538
0xE00	ADCDCCTL0	R/W	0x0000.0000	ADC Digital Comparator Control 0	543
0xE04	ADCDCCTL1	R/W	0x0000.0000	ADC Digital Comparator Control 1	543
0xE08	ADCDCCTL2	R/W	0x0000.0000	ADC Digital Comparator Control 2	543
0xE0C	ADCDCCTL3	R/W	0x0000.0000	ADC Digital Comparator Control 3	543
0xE10	ADCDCCTL4	R/W	0x0000.0000	ADC Digital Comparator Control 4	543
0xE14	ADCDCCTL5	R/W	0x0000.0000	ADC Digital Comparator Control 5	543

Table 14-4. ADC Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0xE18	ADCDCCTL6	R/W	0x0000.0000	ADC Digital Comparator Control 6	543
0xE1C	ADCDCCTL7	R/W	0x0000.0000	ADC Digital Comparator Control 7	543
0xE40	ADCDCCMP0	R/W	0x0000.0000	ADC Digital Comparator Range 0	547
0xE44	ADCDCCMP1	R/W	0x0000.0000	ADC Digital Comparator Range 1	547
0xE48	ADCDCCMP2	R/W	0x0000.0000	ADC Digital Comparator Range 2	547
0xE4C	ADCDCCMP3	R/W	0x0000.0000	ADC Digital Comparator Range 3	547
0xE50	ADCDCCMP4	R/W	0x0000.0000	ADC Digital Comparator Range 4	547
0xE54	ADCDCCMP5	R/W	0x0000.0000	ADC Digital Comparator Range 5	547
0xE58	ADCDCCMP6	R/W	0x0000.0000	ADC Digital Comparator Range 6	547
0xE5C	ADCDCCMP7	R/W	0x0000.0000	ADC Digital Comparator Range 7	547

## 14.6 Register Descriptions

The remainder of this section lists and describes the ADC registers, in numerical order by address offset.

## Register 1: ADC Active Sample Sequencer (ADCACTSS), offset 0x000

This register controls the activation of the sample sequencers. Each sample sequencer can be enabled or disabled independently.

### ADC Active Sample Sequencer (ADCACTSS)

Base 0x4003.8000  
Offset 0x000  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												ASEN3	ASEN2	ASEN1	ASEN0	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	ASEN3	R/W	0	ADC SS3 Enable  Value Description 1 Sample Sequencer 3 is enabled. 0 Sample Sequencer 3 is disabled.
2	ASEN2	R/W	0	ADC SS2 Enable  Value Description 1 Sample Sequencer 2 is enabled. 0 Sample Sequencer 2 is disabled.
1	ASEN1	R/W	0	ADC SS1 Enable  Value Description 1 Sample Sequencer 1 is enabled. 0 Sample Sequencer 1 is disabled.
0	ASEN0	R/W	0	ADC SS0 Enable  Value Description 1 Sample Sequencer 0 is enabled. 0 Sample Sequencer 0 is disabled.

## Register 2: ADC Raw Interrupt Status (ADCRIS), offset 0x004

This register shows the status of the raw interrupt signal of each sample sequencer. These bits may be polled by software to look for interrupt conditions without sending the interrupts to the interrupt controller.

### ADC Raw Interrupt Status (ADCRIS)

Base 0x4003.8000  
 Offset 0x004  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															INRDC
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												INR3	INR2	INR1	INR0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:17	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	INRDC	RO	0	Digital Comparator Raw Interrupt Status  Value Description 1 At least one bit in the <b>ADCDCISC</b> register is set, meaning that a digital comparator interrupt has occurred. 0 All bits in the <b>ADCDCISC</b> register are clear.
15:4	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	INR3	RO	0	SS3 Raw Interrupt Status  Value Description 1 A sample has completed conversion and the respective <b>ADCSSCTL3 IEn</b> bit is set, enabling a raw interrupt. 0 An interrupt has not occurred.  This bit is cleared by writing a 1 to the <b>IN3</b> bit in the <b>ADCISC</b> register.
2	INR2	RO	0	SS2 Raw Interrupt Status  Value Description 1 A sample has completed conversion and the respective <b>ADCSSCTL2 IEn</b> bit is set, enabling a raw interrupt. 0 An interrupt has not occurred.  This bit is cleared by writing a 1 to the <b>IN2</b> bit in the <b>ADCISC</b> register.



Bit/Field	Name	Type	Reset	Description
1	INR1	RO	0	<p>SS1 Raw Interrupt Status</p> <p>Value Description</p> <p>1 A sample has completed conversion and the respective <b>ADCSSCTL1</b> <math>I_{En}</math> bit is set, enabling a raw interrupt.</p> <p>0 An interrupt has not occurred.</p> <p>This bit is cleared by writing a 1 to the <math>IN1</math> bit in the <b>ADCISC</b> register.</p>
0	INR0	RO	0	<p>SS0 Raw Interrupt Status</p> <p>Value Description</p> <p>1 A sample has completed conversion and the respective <b>ADCSSCTL0</b> <math>I_{En}</math> bit is set, enabling a raw interrupt.</p> <p>0 An interrupt has not occurred.</p> <p>This bit is cleared by writing a 1 to the <math>IN0</math> bit in the <b>ADCISC</b> register.</p>

### Register 3: ADC Interrupt Mask (ADCIM), offset 0x008

This register controls whether the sample sequencer and digital comparator raw interrupt signals are sent to the interrupt controller. Each raw interrupt signal can be masked independently. Only a single `DCONSSn` bit should be set at any given time. Setting more than one of these bits results in the `INRDC` bit from the **ADCRIS** register being masked, and no interrupt is generated on any of the sample sequencer interrupt lines.

#### ADC Interrupt Mask (ADCIM)

Base 0x4003.8000  
 Offset 0x008  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved												DCONSS3	DCONSS2	DCONSS1	DCONSS0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												MASK3	MASK2	MASK1	MASK0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:20	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	DCONSS3	R/W	0	Digital Comparator Interrupt on SS3  Value Description 1 The raw interrupt signal from the digital comparators ( <code>INRDC</code> bit in the <b>ADCRIS</b> register) is sent to the interrupt controller on the SS3 interrupt line. 0 The status of the digital comparators does not affect the SS3 interrupt status.
18	DCONSS2	R/W	0	Digital Comparator Interrupt on SS2  Value Description 1 The raw interrupt signal from the digital comparators ( <code>INRDC</code> bit in the <b>ADCRIS</b> register) is sent to the interrupt controller on the SS2 interrupt line. 0 The status of the digital comparators does not affect the SS2 interrupt status.
17	DCONSS1	R/W	0	Digital Comparator Interrupt on SS1  Value Description 1 The raw interrupt signal from the digital comparators ( <code>INRDC</code> bit in the <b>ADCRIS</b> register) is sent to the interrupt controller on the SS1 interrupt line. 0 The status of the digital comparators does not affect the SS1 interrupt status.

Bit/Field	Name	Type	Reset	Description
16	DCONSS0	R/W	0	Digital Comparator Interrupt on SS0  Value Description 1 The raw interrupt signal from the digital comparators ( <i>INRDC</i> bit in the <b>ADCRIS</b> register) is sent to the interrupt controller on the SS0 interrupt line. 0 The status of the digital comparators does not affect the SS0 interrupt status.
15:4	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	MASK3	R/W	0	SS3 Interrupt Mask  Value Description 1 The raw interrupt signal from Sample Sequencer 3 ( <b>ADCRIS</b> register <i>INR3</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 3 does not affect the SS3 interrupt status.
2	MASK2	R/W	0	SS2 Interrupt Mask  Value Description 1 The raw interrupt signal from Sample Sequencer 2 ( <b>ADCRIS</b> register <i>INR2</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 2 does not affect the SS2 interrupt status.
1	MASK1	R/W	0	SS1 Interrupt Mask  Value Description 1 The raw interrupt signal from Sample Sequencer 1 ( <b>ADCRIS</b> register <i>INR1</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 1 does not affect the SS1 interrupt status.
0	MASK0	R/W	0	SS0 Interrupt Mask  Value Description 1 The raw interrupt signal from Sample Sequencer 0 ( <b>ADCRIS</b> register <i>INR0</i> bit) is sent to the interrupt controller. 0 The status of Sample Sequencer 0 does not affect the SS0 interrupt status.

### Register 4: ADC Interrupt Status and Clear (ADCISC), offset 0x00C

This register provides the mechanism for clearing sample sequencer interrupt conditions and shows the status of interrupts generated by the sample sequencers and the digital comparators which have been sent to the interrupt controller. When read, each bit field is the logical AND of the respective **INR** and **MASK** bits. Sample sequencer interrupts are cleared by writing a 1 to the corresponding bit position. Digital comparator interrupts are cleared by writing a 1 to the appropriate bits in the **ADCDCISC** register. If software is polling the **ADCRIS** instead of generating interrupts, the sample sequence **INR<sub>n</sub>** bits are still cleared via the **ADCISC** register, even if the **IN<sub>n</sub>** bit is not set.

#### ADC Interrupt Status and Clear (ADCISC)

Base 0x4003.8000  
 Offset 0x00C  
 Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved												DCINSS3	DCINSS2	DCINSS1	DCINSS0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												IN3	IN2	IN1	IN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:20	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
19	DCINSS3	RO	0	Digital Comparator Interrupt Status on SS3  Value Description 1 Both the <b>INRDC</b> bit in the <b>ADCRIS</b> register and the <b>DCONSS3</b> bit in the <b>ADCIM</b> register are set, providing a level-base interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked.  This bit is cleared by writing a 1 to it. Clearing this bit also clears the <b>INRDC</b> bit in the <b>ADCRIS</b> register.
18	DCINSS2	RO	0	Digital Comparator Interrupt Status on SS2  Value Description 1 Both the <b>INRDC</b> bit in the <b>ADCRIS</b> register and the <b>DCONSS2</b> bit in the <b>ADCIM</b> register are set, providing a level-base interrupt to the interrupt controller. 0 No interrupt has occurred or the interrupt is masked.  This bit is cleared by writing a 1 to it. Clearing this bit also clears the <b>INRDC</b> bit in the <b>ADCRIS</b> register.

Bit/Field	Name	Type	Reset	Description
17	DCINSS1	RO	0	<p>Digital Comparator Interrupt Status on SS1</p> <p>Value Description</p> <p>1 Both the <code>INRDC</code> bit in the <b>ADCRIS</b> register and the <code>DCONSS1</code> bit in the <b>ADCIM</b> register are set, providing a level-base interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1 to it. Clearing this bit also clears the <code>INRDC</code> bit in the <b>ADCRIS</b> register.</p>
16	DCINSS0	RO	0	<p>Digital Comparator Interrupt Status on SS0</p> <p>Value Description</p> <p>1 Both the <code>INRDC</code> bit in the <b>ADCRIS</b> register and the <code>DCONSS0</code> bit in the <b>ADCIM</b> register are set, providing a level-base interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1 to it. Clearing this bit also clears the <code>INRDC</code> bit in the <b>ADCRIS</b> register.</p>
15:4	reserved	RO	0x000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	IN3	R/W1C	0	<p>SS3 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Both the <code>INR3</code> bit in the <b>ADCRIS</b> register and the <code>MASK3</code> bit in the <b>ADCIM</b> register are set, providing a level-based interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR3</code> bit in the <b>ADCRIS</b> register.</p>
2	IN2	R/W1C	0	<p>SS2 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Both the <code>INR2</code> bit in the <b>ADCRIS</b> register and the <code>MASK2</code> bit in the <b>ADCIM</b> register are set, providing a level-based interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR2</code> bit in the <b>ADCRIS</b> register.</p>

Bit/Field	Name	Type	Reset	Description
1	IN1	R/W1C	0	<p>SS1 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Both the <code>INR1</code> bit in the <b>ADCRIS</b> register and the <code>MASK1</code> bit in the <b>ADCIM</b> register are set, providing a level-based interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR1</code> bit in the <b>ADCRIS</b> register.</p>
0	IN0	R/W1C	0	<p>SS0 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Both the <code>INR0</code> bit in the <b>ADCRIS</b> register and the <code>MASK0</code> bit in the <b>ADCIM</b> register are set, providing a level-based interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1. Clearing this bit also clears the <code>INR0</code> bit in the <b>ADCRIS</b> register.</p>

## Register 5: ADC Overflow Status (ADCOSTAT), offset 0x010

This register indicates overflow conditions in the sample sequencer FIFOs. Once the overflow condition has been handled by software, the condition can be cleared by writing a 1 to the corresponding bit position.

### ADC Overflow Status (ADCOSTAT)

Base 0x4003.8000

Offset 0x010

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												OV3	OV2	OV1	OV0	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	OV3	R/W1C	0	SS3 FIFO Overflow  Value Description 1 The FIFO for Sample Sequencer 3 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped. 0 The FIFO has not overflowed.  This bit is cleared by writing a 1.
2	OV2	R/W1C	0	SS2 FIFO Overflow  Value Description 1 The FIFO for Sample Sequencer 2 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped. 0 The FIFO has not overflowed.  This bit is cleared by writing a 1.
1	OV1	R/W1C	0	SS1 FIFO Overflow  Value Description 1 The FIFO for Sample Sequencer 1 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped. 0 The FIFO has not overflowed.  This bit is cleared by writing a 1.

Bit/Field	Name	Type	Reset	Description
0	OV0	R/W1C	0	SS0 FIFO Overflow
				Value Description
				1 The FIFO for Sample Sequencer 0 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped.
				0 The FIFO has not overflowed.
				This bit is cleared by writing a 1.



## Register 6: ADC Event Multiplexer Select (ADCEMUX), offset 0x014

The **ADCEMUX** selects the event (trigger) that initiates sampling for each sample sequencer. Each sample sequencer can be configured with a unique trigger source.

### ADC Event Multiplexer Select (ADCEMUX)

Base 0x4003.8000  
Offset 0x014  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EM3				EM2				EM1				EM0			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description																										
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																										
15:12	EM3	R/W	0x0	SS3 Trigger Select This field selects the trigger source for Sample Sequencer 3. The valid configurations for this field are:  <table border="1"> <thead> <tr> <th>Value</th> <th>Event</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Processor (default)</td> </tr> <tr> <td>0x1</td> <td>Analog Comparator 0</td> </tr> <tr> <td>0x2</td> <td>Analog Comparator 1</td> </tr> <tr> <td>0x3</td> <td>reserved</td> </tr> <tr> <td>0x4</td> <td>External (GPIO PB4)</td> </tr> <tr> <td>0x5</td> <td>Timer</td> </tr> </tbody> </table> <p>In addition, the trigger must be enabled with the <math>TnOTE</math> bit in the <b>GPTMCTL</b> register (see page 430).</p> <table border="1"> <tbody> <tr> <td>0x6</td> <td>reserved</td> </tr> <tr> <td>0x7</td> <td>reserved</td> </tr> <tr> <td>0x8</td> <td>reserved</td> </tr> <tr> <td>0x9</td> <td>reserved</td> </tr> <tr> <td>0xA-0xE</td> <td>reserved</td> </tr> <tr> <td>0xF</td> <td>Always (continuously sample)</td> </tr> </tbody> </table>	Value	Event	0x0	Processor (default)	0x1	Analog Comparator 0	0x2	Analog Comparator 1	0x3	reserved	0x4	External (GPIO PB4)	0x5	Timer	0x6	reserved	0x7	reserved	0x8	reserved	0x9	reserved	0xA-0xE	reserved	0xF	Always (continuously sample)
Value	Event																													
0x0	Processor (default)																													
0x1	Analog Comparator 0																													
0x2	Analog Comparator 1																													
0x3	reserved																													
0x4	External (GPIO PB4)																													
0x5	Timer																													
0x6	reserved																													
0x7	reserved																													
0x8	reserved																													
0x9	reserved																													
0xA-0xE	reserved																													
0xF	Always (continuously sample)																													

Bit/Field	Name	Type	Reset	Description																										
11:8	EM2	R/W	0x0	<p>SS2 Trigger Select</p> <p>This field selects the trigger source for Sample Sequencer 2.</p> <p>The valid configurations for this field are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Event</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Processor (default)</td> </tr> <tr> <td>0x1</td> <td>Analog Comparator 0</td> </tr> <tr> <td>0x2</td> <td>Analog Comparator 1</td> </tr> <tr> <td>0x3</td> <td>reserved</td> </tr> <tr> <td>0x4</td> <td>External (GPIO PB4)</td> </tr> <tr> <td>0x5</td> <td>Timer</td> </tr> </tbody> </table> <p>In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the <b>GPTMCTL</b> register (see page 430).</p> <table border="1"> <tbody> <tr> <td>0x6</td> <td>reserved</td> </tr> <tr> <td>0x7</td> <td>reserved</td> </tr> <tr> <td>0x8</td> <td>reserved</td> </tr> <tr> <td>0x9</td> <td>reserved</td> </tr> <tr> <td>0xA-0xE</td> <td>reserved</td> </tr> <tr> <td>0xF</td> <td>Always (continuously sample)</td> </tr> </tbody> </table>	Value	Event	0x0	Processor (default)	0x1	Analog Comparator 0	0x2	Analog Comparator 1	0x3	reserved	0x4	External (GPIO PB4)	0x5	Timer	0x6	reserved	0x7	reserved	0x8	reserved	0x9	reserved	0xA-0xE	reserved	0xF	Always (continuously sample)
Value	Event																													
0x0	Processor (default)																													
0x1	Analog Comparator 0																													
0x2	Analog Comparator 1																													
0x3	reserved																													
0x4	External (GPIO PB4)																													
0x5	Timer																													
0x6	reserved																													
0x7	reserved																													
0x8	reserved																													
0x9	reserved																													
0xA-0xE	reserved																													
0xF	Always (continuously sample)																													
7:4	EM1	R/W	0x0	<p>SS1 Trigger Select</p> <p>This field selects the trigger source for Sample Sequencer 1.</p> <p>The valid configurations for this field are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Event</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Processor (default)</td> </tr> <tr> <td>0x1</td> <td>Analog Comparator 0</td> </tr> <tr> <td>0x2</td> <td>Analog Comparator 1</td> </tr> <tr> <td>0x3</td> <td>reserved</td> </tr> <tr> <td>0x4</td> <td>External (GPIO PB4)</td> </tr> <tr> <td>0x5</td> <td>Timer</td> </tr> </tbody> </table> <p>In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the <b>GPTMCTL</b> register (see page 430).</p> <table border="1"> <tbody> <tr> <td>0x6</td> <td>reserved</td> </tr> <tr> <td>0x7</td> <td>reserved</td> </tr> <tr> <td>0x8</td> <td>reserved</td> </tr> <tr> <td>0x9</td> <td>reserved</td> </tr> <tr> <td>0xA-0xE</td> <td>reserved</td> </tr> <tr> <td>0xF</td> <td>Always (continuously sample)</td> </tr> </tbody> </table>	Value	Event	0x0	Processor (default)	0x1	Analog Comparator 0	0x2	Analog Comparator 1	0x3	reserved	0x4	External (GPIO PB4)	0x5	Timer	0x6	reserved	0x7	reserved	0x8	reserved	0x9	reserved	0xA-0xE	reserved	0xF	Always (continuously sample)
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0x8	reserved																													
0x9	reserved																													
0xA-0xE	reserved																													
0xF	Always (continuously sample)																													

Bit/Field	Name	Type	Reset	Description																										
3:0	EM0	R/W	0x0	<p>SS0 Trigger Select</p> <p>This field selects the trigger source for Sample Sequencer 0</p> <p>The valid configurations for this field are:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Event</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Processor (default)</td> </tr> <tr> <td>0x1</td> <td>Analog Comparator 0</td> </tr> <tr> <td>0x2</td> <td>Analog Comparator 1</td> </tr> <tr> <td>0x3</td> <td>reserved</td> </tr> <tr> <td>0x4</td> <td>External (GPIO PB4)</td> </tr> <tr> <td>0x5</td> <td>Timer</td> </tr> </tbody> </table> <p>In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the <b>GPTMCTL</b> register (see page 430).</p> <table border="1"> <tbody> <tr> <td>0x6</td> <td>reserved</td> </tr> <tr> <td>0x7</td> <td>reserved</td> </tr> <tr> <td>0x8</td> <td>reserved</td> </tr> <tr> <td>0x9</td> <td>reserved</td> </tr> <tr> <td>0xA-0xE</td> <td>reserved</td> </tr> <tr> <td>0xF</td> <td>Always (continuously sample)</td> </tr> </tbody> </table>	Value	Event	0x0	Processor (default)	0x1	Analog Comparator 0	0x2	Analog Comparator 1	0x3	reserved	0x4	External (GPIO PB4)	0x5	Timer	0x6	reserved	0x7	reserved	0x8	reserved	0x9	reserved	0xA-0xE	reserved	0xF	Always (continuously sample)
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0x7	reserved																													
0x8	reserved																													
0x9	reserved																													
0xA-0xE	reserved																													
0xF	Always (continuously sample)																													

### Register 7: ADC Underflow Status (ADCUSTAT), offset 0x018

This register indicates underflow conditions in the sample sequencer FIFOs. The corresponding underflow condition is cleared by writing a 1 to the relevant bit position.

#### ADC Underflow Status (ADCUSTAT)

Base 0x4003.8000  
 Offset 0x018  
 Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												UV3	UV2	UV1	UV0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description						
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
3	UV3	R/W1C	0	<p>SS3 FIFO Underflow</p> <p>The valid configurations for this field are shown below. This bit is cleared by writing a 1.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>The FIFO for the Sample Sequencer has hit an underflow condition, meaning that the FIFO is empty and a read was requested. The problematic read does not move the FIFO pointers, and 0s are returned.</td> </tr> <tr> <td>0</td> <td>The FIFO has not underflowed.</td> </tr> </tbody> </table>	Value	Description	1	The FIFO for the Sample Sequencer has hit an underflow condition, meaning that the FIFO is empty and a read was requested. The problematic read does not move the FIFO pointers, and 0s are returned.	0	The FIFO has not underflowed.
Value	Description									
1	The FIFO for the Sample Sequencer has hit an underflow condition, meaning that the FIFO is empty and a read was requested. The problematic read does not move the FIFO pointers, and 0s are returned.									
0	The FIFO has not underflowed.									
2	UV2	R/W1C	0	<p>SS2 FIFO Underflow</p> <p>The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.</p>						
1	UV1	R/W1C	0	<p>SS1 FIFO Underflow</p> <p>The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.</p>						
0	UV0	R/W1C	0	<p>SS0 FIFO Underflow</p> <p>The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.</p>						

## Register 8: ADC Sample Sequencer Priority (ADCSSPRI), offset 0x020

This register sets the priority for each of the sample sequencers. Out of reset, Sequencer 0 has the highest priority, and Sequencer 3 has the lowest priority. When reconfiguring sequence priorities, each sequence must have a unique priority for the ADC to operate properly.

### ADC Sample Sequencer Priority (ADCSSPRI)

Base 0x4003.8000  
Offset 0x020  
Type R/W, reset 0x0000.3210

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved		SS3		reserved		SS2		reserved		SS1		reserved		SS0	
Type	RO	RO	R/W	R/W	RO	RO	R/W	R/W	RO	RO	R/W	R/W	RO	RO	R/W	R/W
Reset	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:14	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
13:12	SS3	R/W	0x3	SS3 Priority  This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 3. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.
11:10	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9:8	SS2	R/W	0x2	SS2 Priority  This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 2. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.
7:6	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5:4	SS1	R/W	0x1	SS1 Priority  This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 1. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.
3:2	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
1:0	SS0	R/W	0x0	SS0 Priority  This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 0. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.

**Register 9: ADC Processor Sample Sequence Initiate (ADCPSSI), offset 0x028**

This register provides a mechanism for application software to initiate sampling in the sample sequencers. Sample sequences can be initiated individually or in any combination. When multiple sequences are triggered simultaneously, the priority encodings in **ADCSSPRI** dictate execution order.

## ADC Processor Sample Sequence Initiate (ADCPSSI)

Base 0x4003.8000

Offset 0x028

Type WO, reset -

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												SS3	SS2	SS1	SS0	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	-	-	-	-

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	SS3	WO	-	SS3 Initiate  Value Description 1 Begin sampling on Sample Sequencer 3, if the sequencer is enabled in the <b>ADCACTSS</b> register. 0 No effect.  Only a write by software is valid; a read of this register returns no meaningful data.
2	SS2	WO	-	SS2 Initiate  Value Description 1 Begin sampling on Sample Sequencer 2, if the sequencer is enabled in the <b>ADCACTSS</b> register. 0 No effect.  Only a write by software is valid; a read of this register returns no meaningful data.
1	SS1	WO	-	SS1 Initiate  Value Description 1 Begin sampling on Sample Sequencer 1, if the sequencer is enabled in the <b>ADCACTSS</b> register. 0 No effect.  Only a write by software is valid; a read of this register returns no meaningful data.

Bit/Field	Name	Type	Reset	Description
0	SS0	WO	-	SS0 Initiate
				Value Description
				1 Begin sampling on Sample Sequencer 0, if the sequencer is enabled in the <b>ADCACTSS</b> register.
				0 No effect.
				Only a write by software is valid; a read of this register returns no meaningful data.



## Register 10: ADC Sample Averaging Control (ADCSAC), offset 0x030

This register controls the amount of hardware averaging applied to conversion results. The final conversion result stored in the FIFO is averaged from  $2^{\text{AVG}}$  consecutive ADC samples at the specified ADC speed. If AVG is 0, the sample is passed directly through without any averaging. If AVG=6, then 64 consecutive ADC samples are averaged to generate one result in the sequencer FIFO. An AVG = 7 provides unpredictable results.

### ADC Sample Averaging Control (ADCSAC)

Base 0x4003.8000  
Offset 0x030  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													AVG		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	AVG	R/W	0x0	Hardware Averaging Control Specifies the amount of hardware averaging that will be applied to ADC samples. The AVG field can be any value between 0 and 6. Entering a value of 7 creates unpredictable results.
				Value Description
				0x0 No hardware oversampling
				0x1 2x hardware oversampling
				0x2 4x hardware oversampling
				0x3 8x hardware oversampling
				0x4 16x hardware oversampling
				0x5 32x hardware oversampling
				0x6 64x hardware oversampling
				0x7 reserved

### Register 11: ADC Digital Comparator Interrupt Status and Clear (ADCDCISC), offset 0x034

This register provides status and acknowledgement of digital comparator interrupts. One bit is provided for each comparator.

#### ADC Digital Comparator Interrupt Status and Clear (ADCDCISC)

Base 0x4003.8000  
 Offset 0x034  
 Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DCINT7	DCINT6	DCINT5	DCINT4	DCINT3	DCINT2	DCINT1	DCINT0
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	DCINT7	R/W1C	0	Digital Comparator 7 Interrupt Status and Clear  Value Description 1 Digital Comparator 7 has generated an interrupt. 0 No interrupt.  This bit is cleared by writing a 1.
6	DCINT6	R/W1C	0	Digital Comparator 6 Interrupt Status and Clear  Value Description 1 Digital Comparator 6 has generated an interrupt. 0 No interrupt.  This bit is cleared by writing a 1.
5	DCINT5	R/W1C	0	Digital Comparator 5 Interrupt Status and Clear  Value Description 1 Digital Comparator 5 has generated an interrupt. 0 No interrupt.  This bit is cleared by writing a 1.
4	DCINT4	R/W1C	0	Digital Comparator 4 Interrupt Status and Clear  Value Description 1 Digital Comparator 4 has generated an interrupt. 0 No interrupt.  This bit is cleared by writing a 1.

Bit/Field	Name	Type	Reset	Description
3	DCINT3	R/W1C	0	<p>Digital Comparator 3 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Digital Comparator 3 has generated an interrupt.</p> <p>0 No interrupt.</p> <p>This bit is cleared by writing a 1.</p>
2	DCINT2	R/W1C	0	<p>Digital Comparator 2 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Digital Comparator 2 has generated an interrupt.</p> <p>0 No interrupt.</p> <p>This bit is cleared by writing a 1.</p>
1	DCINT1	R/W1C	0	<p>Digital Comparator 1 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Digital Comparator 1 has generated an interrupt.</p> <p>0 No interrupt.</p> <p>This bit is cleared by writing a 1.</p>
0	DCINT0	R/W1C	0	<p>Digital Comparator 0 Interrupt Status and Clear</p> <p>Value Description</p> <p>1 Digital Comparator 0 has generated an interrupt.</p> <p>0 No interrupt.</p> <p>This bit is cleared by writing a 1.</p>

## Register 12: ADC Sample Sequence Input Multiplexer Select 0 (ADCSSMUX0), offset 0x040

This register defines the analog input configuration for each sample in a sequence executed with Sample Sequencer 0. This register is 32 bits wide and contains information for eight possible samples.

### ADC Sample Sequence Input Multiplexer Select 0 (ADCSSMUX0)

Base 0x4003.8000  
 Offset 0x040  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved	MUX7			reserved	MUX6			reserved	MUX5			reserved	MUX4		
Type	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	MUX3			reserved	MUX2			reserved	MUX1			reserved	MUX0		
Type	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
30:28	MUX7	R/W	0x0	8th Sample Input Select  The MUX7 field is used during the eighth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion. The value set here indicates the corresponding pin, for example, a value of 0x1 indicates the input is AIN1.
27	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
26:24	MUX6	R/W	0x0	7th Sample Input Select  The MUX6 field is used during the seventh sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.
23	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
22:20	MUX5	R/W	0x0	6th Sample Input Select  The MUX5 field is used during the sixth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.
19	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
18:16	MUX4	R/W	0x0	<p>5th Sample Input Select</p> <p>The MUX4 field is used during the fifth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</p>
15	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14:12	MUX3	R/W	0x0	<p>4th Sample Input Select</p> <p>The MUX3 field is used during the fourth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</p>
11	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
10:8	MUX2	R/W	0x0	<p>3rd Sample Input Select</p> <p>The MUX2 field is used during the third sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</p>
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6:4	MUX1	R/W	0x0	<p>2nd Sample Input Select</p> <p>The MUX1 field is used during the second sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</p>
3	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	MUX0	R/W	0x0	<p>1st Sample Input Select</p> <p>The MUX0 field is used during the first sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</p>

### Register 13: ADC Sample Sequence Control 0 (ADCSSCTL0), offset 0x044

This register contains the configuration information for each sample for a sequence executed with a sample sequencer. When configuring a sample sequence, the `END` bit must be set for the final sample, whether it be after the first sample, eighth sample, or any sample in between. This register is 32 bits wide and contains information for eight possible samples.

#### ADC Sample Sequence Control 0 (ADCSSCTL0)

Base 0x4003.8000  
 Offset 0x044  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TS7	IE7	END7	D7	TS6	IE6	END6	D6	TS5	IE5	END5	D5	TS4	IE4	END4	D4
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31	TS7	R/W	0	8th Sample Temp Sensor Select
				Value Description
				1 The temperature sensor is read during the eighth sample of the sample sequence.
				0 The input pin specified by the <b>ADCSSMUXn</b> register is read during the eighth sample of the sample sequence.
30	IE7	R/W	0	8th Sample Interrupt Enable
				Value Description
				1 The raw interrupt signal ( <code>INR0</code> bit) is asserted at the end of the eighth sample's conversion. If the <code>MASK0</code> bit in the <b>ADCIM</b> register is set, the interrupt is promoted to the interrupt controller.
				0 The raw interrupt is not asserted to the interrupt controller.
				It is legal to have multiple samples within a sequence generate interrupts.
29	END7	R/W	0	8th Sample is End of Sequence
				Value Description
				1 The eighth sample is the last sample of the sequence.
				0 Another sample in the sequence is the final sample.
				It is possible to end the sequence on any sample position. Software must set an <code>ENDn</code> bit somewhere within the sequence. Samples defined after the sample containing a set <code>ENDn</code> bit are not requested for conversion even though the fields may be non-zero.

Bit/Field	Name	Type	Reset	Description
28	D7	R/W	0	8th Sample Diff Input Select  Value Description 1 The analog input is differentially sampled. The corresponding <b>ADCSSMUXn</b> nibble must be set to the pair number "i", where the paired inputs are "2i and 2i+1". 0 The analog inputs are not differentially sampled.  Because the temperature sensor does not have a differential option, this bit must not be set when the <b>TS7</b> bit is set.
27	TS6	R/W	0	7th Sample Temp Sensor Select Same definition as <b>TS7</b> but used during the seventh sample.
26	IE6	R/W	0	7th Sample Interrupt Enable Same definition as <b>IE7</b> but used during the seventh sample.
25	END6	R/W	0	7th Sample is End of Sequence Same definition as <b>END7</b> but used during the seventh sample.
24	D6	R/W	0	7th Sample Diff Input Select Same definition as <b>D7</b> but used during the seventh sample.
23	TS5	R/W	0	6th Sample Temp Sensor Select Same definition as <b>TS7</b> but used during the sixth sample.
22	IE5	R/W	0	6th Sample Interrupt Enable Same definition as <b>IE7</b> but used during the sixth sample.
21	END5	R/W	0	6th Sample is End of Sequence Same definition as <b>END7</b> but used during the sixth sample.
20	D5	R/W	0	6th Sample Diff Input Select Same definition as <b>D7</b> but used during the sixth sample.
19	TS4	R/W	0	5th Sample Temp Sensor Select Same definition as <b>TS7</b> but used during the fifth sample.
18	IE4	R/W	0	5th Sample Interrupt Enable Same definition as <b>IE7</b> but used during the fifth sample.
17	END4	R/W	0	5th Sample is End of Sequence Same definition as <b>END7</b> but used during the fifth sample.
16	D4	R/W	0	5th Sample Diff Input Select Same definition as <b>D7</b> but used during the fifth sample.
15	TS3	R/W	0	4th Sample Temp Sensor Select Same definition as <b>TS7</b> but used during the fourth sample.

Bit/Field	Name	Type	Reset	Description
14	IE3	R/W	0	4th Sample Interrupt Enable Same definition as IE7 but used during the fourth sample.
13	END3	R/W	0	4th Sample is End of Sequence Same definition as END7 but used during the fourth sample.
12	D3	R/W	0	4th Sample Diff Input Select Same definition as D7 but used during the fourth sample.
11	TS2	R/W	0	3rd Sample Temp Sensor Select Same definition as TS7 but used during the third sample.
10	IE2	R/W	0	3rd Sample Interrupt Enable Same definition as IE7 but used during the third sample.
9	END2	R/W	0	3rd Sample is End of Sequence Same definition as END7 but used during the third sample.
8	D2	R/W	0	3rd Sample Diff Input Select Same definition as D7 but used during the third sample.
7	TS1	R/W	0	2nd Sample Temp Sensor Select Same definition as TS7 but used during the second sample.
6	IE1	R/W	0	2nd Sample Interrupt Enable Same definition as IE7 but used during the second sample.
5	END1	R/W	0	2nd Sample is End of Sequence Same definition as END7 but used during the second sample.
4	D1	R/W	0	2nd Sample Diff Input Select Same definition as D7 but used during the second sample.
3	TS0	R/W	0	1st Sample Temp Sensor Select Same definition as TS7 but used during the first sample.
2	IE0	R/W	0	1st Sample Interrupt Enable Same definition as IE7 but used during the first sample.
1	END0	R/W	0	1st Sample is End of Sequence Same definition as END7 but used during the first sample.
0	D0	R/W	0	1st Sample Diff Input Select Same definition as D7 but used during the first sample.



**Register 14: ADC Sample Sequence Result FIFO 0 (ADCSSFIFO0), offset 0x048**

**Register 15: ADC Sample Sequence Result FIFO 1 (ADCSSFIFO1), offset 0x068**

**Register 16: ADC Sample Sequence Result FIFO 2 (ADCSSFIFO2), offset 0x088**

**Register 17: ADC Sample Sequence Result FIFO 3 (ADCSSFIFO3), offset 0x0A8**

**Important:** Use caution when reading this register. Performing a read may change bit status.

This register contains the conversion results for samples collected with the sample sequencer (the **ADCSSFIFO0** register is used for Sample Sequencer 0, **ADCSSFIFO1** for Sequencer 1, **ADCSSFIFO2** for Sequencer 2, and **ADCSSFIFO3** for Sequencer 3). Reads of this register return conversion result data in the order sample 0, sample 1, and so on, until the FIFO is empty. If the FIFO is not properly handled by software, overflow and underflow conditions are registered in the **ADCOSTAT** and **ADCUSTAT** registers.

#### ADC Sample Sequence Result FIFO 0 (ADCSSFIFO0)

Base 0x4003.8000

Offset 0x048

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						DATA									
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:10	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9:0	DATA	RO	0x000	Conversion Result Data

**Register 18: ADC Sample Sequence FIFO 0 Status (ADCSSFSTAT0), offset 0x04C**

**Register 19: ADC Sample Sequence FIFO 1 Status (ADCSSFSTAT1), offset 0x06C**

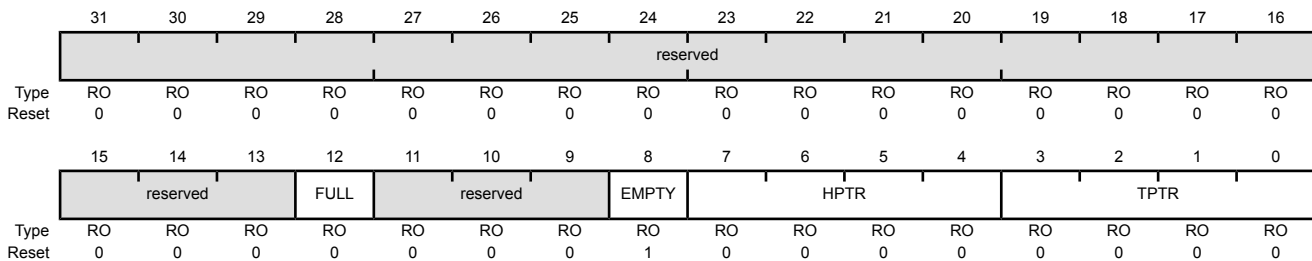
**Register 20: ADC Sample Sequence FIFO 2 Status (ADCSSFSTAT2), offset 0x08C**

**Register 21: ADC Sample Sequence FIFO 3 Status (ADCSSFSTAT3), offset 0x0AC**

This register provides a window into the sample sequencer, providing full/empty status information as well as the positions of the head and tail pointers. The reset value of 0x100 indicates an empty FIFO. The **ADCSSFSTAT0** register provides status on FIFO0, which has 8 entries; **ADCSSFSTAT1** on FIFO1, which has 4 entries; **ADCSSFSTAT2** on FIFO2, which has 4 entries; and **ADCSSFSTAT3** on FIFO3 which has a single entry.

ADC Sample Sequence FIFO 0 Status (ADCSSFSTAT0)

Base 0x4003.8000  
 Offset 0x04C  
 Type RO, reset 0x0000.0100



Bit/Field	Name	Type	Reset	Description
31:13	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	FULL	RO	0	FIFO Full  Value Description 1 The FIFO is currently full. 0 The FIFO is not currently full.
11:9	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	EMPTY	RO	1	FIFO Empty  Value Description 1 The FIFO is currently empty. 0 The FIFO is not currently empty.

Bit/Field	Name	Type	Reset	Description
7:4	HPTR	RO	0x0	FIFO Head Pointer  This field contains the current "head" pointer index for the FIFO, that is, the next entry to be written.
3:0	TPTR	RO	0x0	FIFO Tail Pointer  This field contains the current "tail" pointer index for the FIFO, that is, the next entry to be read.

## Register 22: ADC Sample Sequence 0 Operation (ADCSSOP0), offset 0x050

This register determines whether the sample from the given conversion on Sample Sequence 0 is saved in the Sample Sequence FIFO0 or sent to the digital comparator unit.

### ADC Sample Sequence 0 Operation (ADCSSOP0)

Base 0x4003.8000  
 Offset 0x050  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved			S7DCOP	reserved			S6DCOP	reserved			S5DCOP	reserved			S4DCOP
Type	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved			S3DCOP	reserved			S2DCOP	reserved			S1DCOP	reserved			S0DCOP
Type	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:29	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
28	S7DCOP	R/W	0	Sample 7 Digital Comparator Operation  Value Description 1 The eighth sample is sent to the digital comparator unit specified by the S7DCSEL bit in the ADCSSDC0 register, and the value is not written to the FIFO. 0 The eighth sample is saved in Sample Sequence FIFO0.
27:25	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
24	S6DCOP	R/W	0	Sample 6 Digital Comparator Operation  Same definition as S7DCOP but used during the seventh sample.
23:21	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
20	S5DCOP	R/W	0	Sample 5 Digital Comparator Operation  Same definition as S7DCOP but used during the sixth sample.
19:17	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
16	S4DCOP	R/W	0	Sample 4 Digital Comparator Operation  Same definition as S7DCOP but used during the fifth sample.
15:13	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

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Bit/Field	Name	Type	Reset	Description
12	S3DCOP	R/W	0	Sample 3 Digital Comparator Operation Same definition as S7DCOP but used during the fourth sample.
11:9	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	S2DCOP	R/W	0	Sample 2 Digital Comparator Operation Same definition as S7DCOP but used during the third sample.
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	S1DCOP	R/W	0	Sample 1 Digital Comparator Operation Same definition as S7DCOP but used during the second sample.
3:1	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	S0DCOP	R/W	0	Sample 0 Digital Comparator Operation Same definition as S7DCOP but used during the first sample.

### Register 23: ADC Sample Sequence 0 Digital Comparator Select (ADCSSDC0), offset 0x054

This register determines which digital comparator receives the sample from the given conversion on Sample Sequence 0, if the corresponding  $S_nDCOP$  bit in the **ADCSSOP0** register is set.

#### ADC Sample Sequence 0 Digital Comparator Select (ADCSSDC0)

Base 0x4003.8000  
 Offset 0x054  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	S7DCSEL				S6DCSEL				S5DCSEL				S4DCSEL			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description																		
31:28	S7DCSEL	R/W	0x0	<p>Sample 7 Digital Comparator Select</p> <p>When the <math>S7DCOP</math> bit in the <b>ADCSSOP0</b> register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the eighth sample from Sample Sequencer 0.</p> <p><b>Note:</b> Values not listed are reserved.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>Digital Comparator Unit 0 (<b>ADCDCOMP0</b> and <b>ADCCCTL0</b>)</td></tr> <tr><td>0x1</td><td>Digital Comparator Unit 1 (<b>ADCDCOMP1</b> and <b>ADCCCTL1</b>)</td></tr> <tr><td>0x2</td><td>Digital Comparator Unit 2 (<b>ADCDCOMP2</b> and <b>ADCCCTL2</b>)</td></tr> <tr><td>0x3</td><td>Digital Comparator Unit 3 (<b>ADCDCOMP3</b> and <b>ADCCCTL3</b>)</td></tr> <tr><td>0x4</td><td>Digital Comparator Unit 4 (<b>ADCDCOMP4</b> and <b>ADCCCTL4</b>)</td></tr> <tr><td>0x5</td><td>Digital Comparator Unit 5 (<b>ADCDCOMP5</b> and <b>ADCCCTL5</b>)</td></tr> <tr><td>0x6</td><td>Digital Comparator Unit 6 (<b>ADCDCOMP6</b> and <b>ADCCCTL6</b>)</td></tr> <tr><td>0x7</td><td>Digital Comparator Unit 7 (<b>ADCDCOMP7</b> and <b>ADCCCTL7</b>)</td></tr> </tbody> </table>	Value	Description	0x0	Digital Comparator Unit 0 ( <b>ADCDCOMP0</b> and <b>ADCCCTL0</b> )	0x1	Digital Comparator Unit 1 ( <b>ADCDCOMP1</b> and <b>ADCCCTL1</b> )	0x2	Digital Comparator Unit 2 ( <b>ADCDCOMP2</b> and <b>ADCCCTL2</b> )	0x3	Digital Comparator Unit 3 ( <b>ADCDCOMP3</b> and <b>ADCCCTL3</b> )	0x4	Digital Comparator Unit 4 ( <b>ADCDCOMP4</b> and <b>ADCCCTL4</b> )	0x5	Digital Comparator Unit 5 ( <b>ADCDCOMP5</b> and <b>ADCCCTL5</b> )	0x6	Digital Comparator Unit 6 ( <b>ADCDCOMP6</b> and <b>ADCCCTL6</b> )	0x7	Digital Comparator Unit 7 ( <b>ADCDCOMP7</b> and <b>ADCCCTL7</b> )
Value	Description																					
0x0	Digital Comparator Unit 0 ( <b>ADCDCOMP0</b> and <b>ADCCCTL0</b> )																					
0x1	Digital Comparator Unit 1 ( <b>ADCDCOMP1</b> and <b>ADCCCTL1</b> )																					
0x2	Digital Comparator Unit 2 ( <b>ADCDCOMP2</b> and <b>ADCCCTL2</b> )																					
0x3	Digital Comparator Unit 3 ( <b>ADCDCOMP3</b> and <b>ADCCCTL3</b> )																					
0x4	Digital Comparator Unit 4 ( <b>ADCDCOMP4</b> and <b>ADCCCTL4</b> )																					
0x5	Digital Comparator Unit 5 ( <b>ADCDCOMP5</b> and <b>ADCCCTL5</b> )																					
0x6	Digital Comparator Unit 6 ( <b>ADCDCOMP6</b> and <b>ADCCCTL6</b> )																					
0x7	Digital Comparator Unit 7 ( <b>ADCDCOMP7</b> and <b>ADCCCTL7</b> )																					
27:24	S6DCSEL	R/W	0x0	<p>Sample 6 Digital Comparator Select</p> <p>This field has the same encodings as <math>S7DCSEL</math> but is used during the seventh sample.</p>																		
23:20	S5DCSEL	R/W	0x0	<p>Sample 5 Digital Comparator Select</p> <p>This field has the same encodings as <math>S7DCSEL</math> but is used during the sixth sample.</p>																		
19:16	S4DCSEL	R/W	0x0	<p>Sample 4 Digital Comparator Select</p> <p>This field has the same encodings as <math>S7DCSEL</math> but is used during the fifth sample.</p>																		

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Bit/Field	Name	Type	Reset	Description
15:12	S3DCSEL	R/W	0x0	Sample 3 Digital Comparator Select This field has the same encodings as S7DCSEL but is used during the fourth sample.
11:8	S2DCSEL	R/W	0x0	Sample 2 Digital Comparator Select This field has the same encodings as S7DCSEL but is used during the third sample.
7:4	S1DCSEL	R/W	0x0	Sample 1 Digital Comparator Select This field has the same encodings as S7DCSEL but is used during the second sample.
3:0	S0DCSEL	R/W	0x0	Sample 0 Digital Comparator Select This field has the same encodings as S7DCSEL but is used during the first sample.

**Register 24: ADC Sample Sequence Input Multiplexer Select 1 (ADCSSMUX1), offset 0x060**

**Register 25: ADC Sample Sequence Input Multiplexer Select 2 (ADCSSMUX2), offset 0x080**

This register defines the analog input configuration for each sample in a sequence executed with Sample Sequencer 1 or 2. These registers are 16 bits wide and contain information for four possible samples. See the **ADCSSMUX0** register on page 516 for detailed bit descriptions. The **ADCSSMUX1** register affects Sample Sequencer 1 and the **ADCSSMUX2** register affects Sample Sequencer 2.

ADC Sample Sequence Input Multiplexer Select 1 (ADCSSMUX1)

Base 0x4003.8000  
 Offset 0x060  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved	MUX3			reserved	MUX2			reserved	MUX1			reserved	MUX0		
Type	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:15	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
14:12	MUX3	R/W	0x0	4th Sample Input Select
11	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
10:8	MUX2	R/W	0x0	3rd Sample Input Select
7	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6:4	MUX1	R/W	0x0	2nd Sample Input Select
3	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	MUX0	R/W	0x0	1st Sample Input Select



**Register 26: ADC Sample Sequence Control 1 (ADCSSCTL1), offset 0x064****Register 27: ADC Sample Sequence Control 2 (ADCSSCTL2), offset 0x084**

These registers contain the configuration information for each sample for a sequence executed with Sample Sequencer 1 or 2. When configuring a sample sequence, the **END** bit must be set for the final sample, whether it be after the first sample, fourth sample, or any sample in between. These registers are 16-bits wide and contain information for four possible samples. See the **ADCSSCTL0** register on page 518 for detailed bit descriptions. The **ADCSSCTL1** register configures Sample Sequencer 1 and the **ADCSSCTL2** register configures Sample Sequencer 2.

**ADC Sample Sequence Control 1 (ADCSSCTL1)**

Base 0x4003.8000  
Offset 0x064  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15	TS3	R/W	0	4th Sample Temp Sensor Select Same definition as <b>TS7</b> but used during the fourth sample.
14	IE3	R/W	0	4th Sample Interrupt Enable Same definition as <b>IE7</b> but used during the fourth sample.
13	END3	R/W	0	4th Sample is End of Sequence Same definition as <b>END7</b> but used during the fourth sample.
12	D3	R/W	0	4th Sample Diff Input Select Same definition as <b>D7</b> but used during the fourth sample.
11	TS2	R/W	0	3rd Sample Temp Sensor Select Same definition as <b>TS7</b> but used during the third sample.
10	IE2	R/W	0	3rd Sample Interrupt Enable Same definition as <b>IE7</b> but used during the third sample.
9	END2	R/W	0	3rd Sample is End of Sequence Same definition as <b>END7</b> but used during the third sample.
8	D2	R/W	0	3rd Sample Diff Input Select Same definition as <b>D7</b> but used during the third sample.

Bit/Field	Name	Type	Reset	Description
7	TS1	R/W	0	2nd Sample Temp Sensor Select Same definition as TS7 but used during the second sample.
6	IE1	R/W	0	2nd Sample Interrupt Enable Same definition as IE7 but used during the second sample.
5	END1	R/W	0	2nd Sample is End of Sequence Same definition as END7 but used during the second sample.
4	D1	R/W	0	2nd Sample Diff Input Select Same definition as D7 but used during the second sample.
3	TS0	R/W	0	1st Sample Temp Sensor Select Same definition as TS7 but used during the first sample.
2	IE0	R/W	0	1st Sample Interrupt Enable Same definition as IE7 but used during the first sample.
1	END0	R/W	0	1st Sample is End of Sequence Same definition as END7 but used during the first sample.
0	D0	R/W	0	1st Sample Diff Input Select Same definition as D7 but used during the first sample.

**Register 28: ADC Sample Sequence 1 Operation (ADCSSOP1), offset 0x070****Register 29: ADC Sample Sequence 2 Operation (ADCSSOP2), offset 0x090**

This register determines whether the sample from the given conversion on Sample Sequence n is saved in the Sample Sequence n FIFO or sent to the digital comparator unit. The **ADCSSOP1** register controls Sample Sequencer 1 and the **ADCSSOP2** register controls Sample Sequencer 2.

## ADC Sample Sequence 1 Operation (ADCSSOP1)

Base 0x4003.8000  
Offset 0x070  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved			S3DCOP	reserved			S2DCOP	reserved			S1DCOP	reserved			S0DCOP
Type	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:13	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	S3DCOP	R/W	0	Sample 3 Digital Comparator Operation  Value Description 1 The fourth sample is sent to the digital comparator unit specified by the S3DCSEL bit in the ADCSSDC0n register, and the value is not written to the FIFO. 0 The fourth sample is saved in Sample Sequence FIFO.
11:9	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	S2DCOP	R/W	0	Sample 2 Digital Comparator Operation  Same definition as S3DCOP but used during the third sample.
7:5	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	S1DCOP	R/W	0	Sample 1 Digital Comparator Operation  Same definition as S3DCOP but used during the second sample.
3:1	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	S0DCOP	R/W	0	Sample 0 Digital Comparator Operation  Same definition as S3DCOP but used during the first sample.

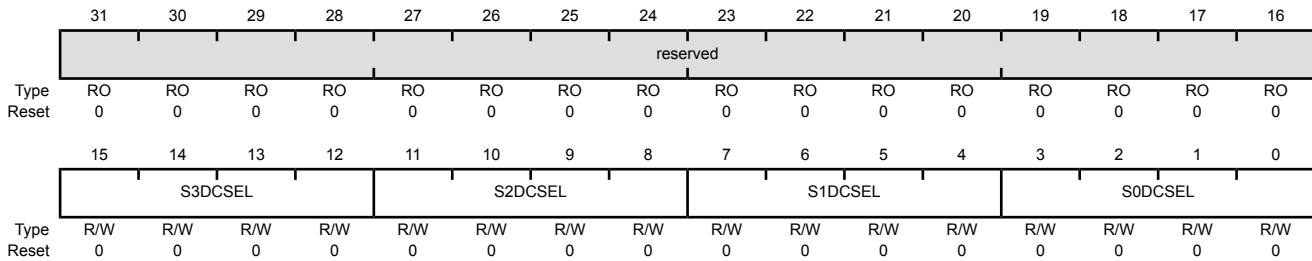
**Register 30: ADC Sample Sequence 1 Digital Comparator Select (ADCSSDC1), offset 0x074**

**Register 31: ADC Sample Sequence 2 Digital Comparator Select (ADCSSDC2), offset 0x094**

These registers determine which digital comparator receives the sample from the given conversion on Sample Sequence n if the corresponding  $S_nDCOP$  bit in the **ADCSSOPn** register is set. The **ADCSSDC1** register controls the selection for Sample Sequencer 1 and the **ADCSSDC2** register controls the selection for Sample Sequencer 2.

ADC Sample Sequence 1 Digital Comparator Select (ADCSSDC1)

Base 0x4003.8000  
 Offset 0x074  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description																		
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.																		
15:12	S3DCSEL	R/W	0x0	<p>Sample 3 Digital Comparator Select</p> <p>When the <math>S3DCOP</math> bit in the <b>ADCSSOPn</b> register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the eighth sample from Sample Sequencer n.</p> <p><b>Note:</b> Values not listed are reserved.</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>Digital Comparator Unit 0 (<b>ADCDCOMP0</b> and <b>ADCCCTL0</b>)</td></tr> <tr><td>0x1</td><td>Digital Comparator Unit 1 (<b>ADCDCOMP1</b> and <b>ADCCCTL1</b>)</td></tr> <tr><td>0x2</td><td>Digital Comparator Unit 2 (<b>ADCDCOMP2</b> and <b>ADCCCTL2</b>)</td></tr> <tr><td>0x3</td><td>Digital Comparator Unit 3 (<b>ADCDCOMP3</b> and <b>ADCCCTL3</b>)</td></tr> <tr><td>0x4</td><td>Digital Comparator Unit 4 (<b>ADCDCOMP4</b> and <b>ADCCCTL4</b>)</td></tr> <tr><td>0x5</td><td>Digital Comparator Unit 5 (<b>ADCDCOMP5</b> and <b>ADCCCTL5</b>)</td></tr> <tr><td>0x6</td><td>Digital Comparator Unit 6 (<b>ADCDCOMP6</b> and <b>ADCCCTL6</b>)</td></tr> <tr><td>0x7</td><td>Digital Comparator Unit 7 (<b>ADCDCOMP7</b> and <b>ADCCCTL7</b>)</td></tr> </tbody> </table>	Value	Description	0x0	Digital Comparator Unit 0 ( <b>ADCDCOMP0</b> and <b>ADCCCTL0</b> )	0x1	Digital Comparator Unit 1 ( <b>ADCDCOMP1</b> and <b>ADCCCTL1</b> )	0x2	Digital Comparator Unit 2 ( <b>ADCDCOMP2</b> and <b>ADCCCTL2</b> )	0x3	Digital Comparator Unit 3 ( <b>ADCDCOMP3</b> and <b>ADCCCTL3</b> )	0x4	Digital Comparator Unit 4 ( <b>ADCDCOMP4</b> and <b>ADCCCTL4</b> )	0x5	Digital Comparator Unit 5 ( <b>ADCDCOMP5</b> and <b>ADCCCTL5</b> )	0x6	Digital Comparator Unit 6 ( <b>ADCDCOMP6</b> and <b>ADCCCTL6</b> )	0x7	Digital Comparator Unit 7 ( <b>ADCDCOMP7</b> and <b>ADCCCTL7</b> )
Value	Description																					
0x0	Digital Comparator Unit 0 ( <b>ADCDCOMP0</b> and <b>ADCCCTL0</b> )																					
0x1	Digital Comparator Unit 1 ( <b>ADCDCOMP1</b> and <b>ADCCCTL1</b> )																					
0x2	Digital Comparator Unit 2 ( <b>ADCDCOMP2</b> and <b>ADCCCTL2</b> )																					
0x3	Digital Comparator Unit 3 ( <b>ADCDCOMP3</b> and <b>ADCCCTL3</b> )																					
0x4	Digital Comparator Unit 4 ( <b>ADCDCOMP4</b> and <b>ADCCCTL4</b> )																					
0x5	Digital Comparator Unit 5 ( <b>ADCDCOMP5</b> and <b>ADCCCTL5</b> )																					
0x6	Digital Comparator Unit 6 ( <b>ADCDCOMP6</b> and <b>ADCCCTL6</b> )																					
0x7	Digital Comparator Unit 7 ( <b>ADCDCOMP7</b> and <b>ADCCCTL7</b> )																					
11:8	S2DCSEL	R/W	0x0	<p>Sample 2 Digital Comparator Select</p> <p>This field has the same encodings as <b>S3DCSEL</b> but is used during the third sample.</p>																		

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Bit/Field	Name	Type	Reset	Description
7:4	S1DCSEL	R/W	0x0	Sample 1 Digital Comparator Select This field has the same encodings as S3DCSEL but is used during the second sample.
3:0	S0DCSEL	R/W	0x0	Sample 0 Digital Comparator Select This field has the same encodings as S3DCSEL but is used during the first sample.

### Register 32: ADC Sample Sequence Input Multiplexer Select 3 (ADCSSMUX3), offset 0x0A0

This register defines the analog input configuration for the sample executed with Sample Sequencer 3. This register is 4 bits wide and contains information for one possible sample. See the **ADCSSMUX0** register on page 516 for detailed bit descriptions.

#### ADC Sample Sequence Input Multiplexer Select 3 (ADCSSMUX3)

Base 0x4003.8000  
 Offset 0x0A0  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													MUX0		
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2:0	MUX0	R/W	0	1st Sample Input Select

**Register 33: ADC Sample Sequence Control 3 (ADCSSCTL3), offset 0x0A4**

This register contains the configuration information for a sample executed with Sample Sequencer 3. The `END0` bit is always set as this sequencer can execute only one sample. This register is 4 bits wide and contains information for one possible sample. See the `ADCSSCTL0` register on page 518 for detailed bit descriptions.

## ADC Sample Sequence Control 3 (ADCSSCTL3)

Base 0x4003.8000  
Offset 0x0A4  
Type R/W, reset 0x0000.0002

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												TS0	IE0	END0	D0	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	TS0	R/W	0	1st Sample Temp Sensor Select Same definition as <code>TS7</code> but used during the first sample.
2	IE0	R/W	0	1st Sample Interrupt Enable Same definition as <code>IE7</code> but used during the first sample.
1	END0	R/W	1	1st Sample is End of Sequence Same definition as <code>END7</code> but used during the first sample. Because this sequencer has only one entry, this bit must be set.
0	D0	R/W	0	1st Sample Diff Input Select Same definition as <code>D7</code> but used during the first sample.

### Register 34: ADC Sample Sequence 3 Operation (ADCSSOP3), offset 0x0B0

This register determines whether the sample from the given conversion on Sample Sequence 3 is saved in the Sample Sequence 3 FIFO or sent to the digital comparator unit.

#### ADC Sample Sequence 3 Operation (ADCSSOP3)

Base 0x4003.8000  
 Offset 0x0B0  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															S0DCOP
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	S0DCOP	R/W	0	Sample 0 Digital Comparator Operation
				Value Description
				1 The sample is sent to the digital comparator unit specified by the S0DCSEL bit in the ADCSSDC03 register, and the value is not written to the FIFO.
				0 The sample is saved in Sample Sequence FIFO3.



## Register 35: ADC Sample Sequence 3 Digital Comparator Select (ADCSSDC3), offset 0x0B4

This register determines which digital comparator receives the sample from the given conversion on Sample Sequence 3 if the corresponding  $S_nDCOP$  bit in the **ADCSSOP3** register is set.

### ADC Sample Sequence 3 Digital Comparator Select (ADCSSDC3)

Base 0x4003.8000  
Offset 0x0B4  
Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved												S0DCSEL			
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3:0	S0DCSEL	R/W	0x0	Sample 0 Digital Comparator Select  When the $S0DCOP$ bit in the <b>ADCSSOP3</b> register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the sample from Sample Sequencer 3.

**Note:** Values not listed are reserved.

#### Value Description

0x0	Digital Comparator Unit 0 ( <b>ADCDCOMP0</b> and <b>ADCCCTL0</b> )
0x1	Digital Comparator Unit 1 ( <b>ADCDCOMP1</b> and <b>ADCCCTL1</b> )
0x2	Digital Comparator Unit 2 ( <b>ADCDCOMP2</b> and <b>ADCCCTL2</b> )
0x3	Digital Comparator Unit 3 ( <b>ADCDCOMP3</b> and <b>ADCCCTL3</b> )
0x4	Digital Comparator Unit 4 ( <b>ADCDCOMP4</b> and <b>ADCCCTL4</b> )
0x5	Digital Comparator Unit 5 ( <b>ADCDCOMP5</b> and <b>ADCCCTL5</b> )
0x6	Digital Comparator Unit 6 ( <b>ADCDCOMP6</b> and <b>ADCCCTL6</b> )
0x7	Digital Comparator Unit 7 ( <b>ADCDCOMP7</b> and <b>ADCCCTL7</b> )

### Register 36: ADC Digital Comparator Reset Initial Conditions (ADCDCRIC), offset 0xD00

This register provides the ability to reset any of the digital comparator interrupt or trigger functions back to their initial conditions. Resetting these functions ensures that the data that is being used by the interrupt and trigger functions in the digital comparator unit is not stale.

#### ADC Digital Comparator Reset Initial Conditions (ADCDCRIC)

Base 0x4003.8000  
 Offset 0xD00  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved								DCTRIG7	DCTRIG6	DCTRIG5	DCTRIG4	DCTRIG3	DCTRIG2	DCTRIG1	DCTRIG0
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DCINT7	DCINT6	DCINT5	DCINT4	DCINT3	DCINT2	DCINT1	DCINT0
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:24	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
23	DCTRIG7	R/W	0	Digital Comparator Trigger 7  Value Description 1 Resets the Digital Comparator 7 trigger unit to its initial conditions. 0 No effect.  When the trigger has been cleared, this bit is automatically cleared.  Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
22	DCTRIG6	R/W	0	Digital Comparator Trigger 6  Value Description 1 Resets the Digital Comparator 6 trigger unit to its initial conditions. 0 No effect.  When the trigger has been cleared, this bit is automatically cleared.  Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

Bit/Field	Name	Type	Reset	Description
21	DCTRIG5	R/W	0	<p>Digital Comparator Trigger 5</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 5 trigger unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the trigger has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
20	DCTRIG4	R/W	0	<p>Digital Comparator Trigger 4</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 4 trigger unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the trigger has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
19	DCTRIG3	R/W	0	<p>Digital Comparator Trigger 3</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 3 trigger unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the trigger has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
18	DCTRIG2	R/W	0	<p>Digital Comparator Trigger 2</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 2 trigger unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the trigger has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>

Bit/Field	Name	Type	Reset	Description
17	DCTRIG1	R/W	0	<p>Digital Comparator Trigger 1</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 1 trigger unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the trigger has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
16	DCTRIG0	R/W	0	<p>Digital Comparator Trigger 0</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 0 trigger unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the trigger has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
15:8	reserved	RO	0x00	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>
7	DCINT7	R/W	0	<p>Digital Comparator Interrupt 7</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 7 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>

Bit/Field	Name	Type	Reset	Description
6	DCINT6	R/W	0	<p>Digital Comparator Interrupt 6</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 6 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
5	DCINT5	R/W	0	<p>Digital Comparator Interrupt 5</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 5 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
4	DCINT4	R/W	0	<p>Digital Comparator Interrupt 4</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 4 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
3	DCINT3	R/W	0	<p>Digital Comparator Interrupt 3</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 3 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>

Bit/Field	Name	Type	Reset	Description
2	DCINT2	R/W	0	<p>Digital Comparator Interrupt 2</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 2 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
1	DCINT1	R/W	0	<p>Digital Comparator Interrupt 1</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 1 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>
0	DCINT0	R/W	0	<p>Digital Comparator Interrupt 0</p> <p>Value Description</p> <p>1 Resets the Digital Comparator 0 interrupt unit to its initial conditions.</p> <p>0 No effect.</p> <p>When the interrupt has been cleared, this bit is automatically cleared.</p> <p>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</p>

**Register 37: ADC Digital Comparator Control 0 (ADCDCCTL0), offset 0xE00**

**Register 38: ADC Digital Comparator Control 1 (ADCDCCTL1), offset 0xE04**

**Register 39: ADC Digital Comparator Control 2 (ADCDCCTL2), offset 0xE08**

**Register 40: ADC Digital Comparator Control 3 (ADCDCCTL3), offset 0xE0C**

**Register 41: ADC Digital Comparator Control 4 (ADCDCCTL4), offset 0xE10**

**Register 42: ADC Digital Comparator Control 5 (ADCDCCTL5), offset 0xE14**

**Register 43: ADC Digital Comparator Control 6 (ADCDCCTL6), offset 0xE18**

**Register 44: ADC Digital Comparator Control 7 (ADCDCCTL7), offset 0xE1C**

This register provides the comparison encodings that generate an interrupt or PWM trigger.

#### ADC Digital Comparator Control 0 (ADCDCCTL0)

Base 0x4003.8000

Offset 0xE00

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
	reserved																	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	reserved			CTE	CTC			CTM			reserved			CIE	CIC		CIM	
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	RO	RO	RO	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit/Field	Name	Type	Reset	Description
31:13	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12	CTE	R/W	0	Comparison Trigger Enable
				Value Description
				1 Enables the trigger function state machine. The ADC conversion data is used to determine if a trigger should be generated according to the programming of the CTC and CTM fields.
				0 Disables the trigger function state machine. ADC conversion data is ignored by the trigger function.

Bit/Field	Name	Type	Reset	Description
11:10	CTC	R/W	0x0	<p>Comparison Trigger Condition</p> <p>This field specifies the operational region in which a trigger is generated when the ADC conversion data is compared against the values of COMP0 and COMP1. The COMP0 and COMP1 fields are defined in the <b>ADCDCMPx</b> registers.</p> <p>Value Description</p> <p>0x0 Low Band ADC Data &lt; COMP0 and &lt; COMP1</p> <p>0x1 Mid Band COMP0 ≤ ADC Data &lt; COMP1</p> <p>0x2 reserved</p> <p>0x3 High Band COMP0 ≤ COMP1 ≤ ADC Data</p>
9:8	CTM	R/W	0x0	<p>Comparison Trigger Mode</p> <p>This field specifies the mode by which the trigger comparison is made.</p> <p>Value Description</p> <p>0x0 Always This mode generates a trigger every time the ADC conversion data falls within the selected operational region.</p> <p>0x1 Once This mode generates a trigger the first time that the ADC conversion data enters the selected operational region.</p> <p>0x2 Hysteresis Always This mode generates a trigger when the ADC conversion data falls within the selected operational region and continues to generate the trigger until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</p> <p>0x3 Hysteresis Once This mode generates a trigger the first time that the ADC conversion data falls within the selected operational region. No additional triggers are generated until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</p>
7:5	reserved	RO	0x0	<p>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</p>



Bit/Field	Name	Type	Reset	Description
4	CIE	R/W	0	<p>Comparison Interrupt Enable</p> <p>Value Description</p> <p>1 Enables the comparison interrupt. The ADC conversion data is used to determine if an interrupt should be generated according to the programming of the CIE and CIM fields.</p> <p>0 Disables the comparison interrupt. ADC conversion data has no effect on interrupt generation.</p>
3:2	CIC	R/W	0x0	<p>Comparison Interrupt Condition</p> <p>This field specifies the operational region in which an interrupt is generated when the ADC conversion data is compared against the values of COMP0 and COMP1. The COMP0 and COMP1 fields are defined in the ADCDCMPx registers.</p> <p>Value Description</p> <p>0x0 Low Band ADC Data &lt; COMP0 and &lt; COMP1</p> <p>0x1 Mid Band COMP0 ≤ ADC Data &lt; COMP1</p> <p>0x2 reserved</p> <p>0x3 High Band COMP0 &lt; COMP1 ≤ ADC Data</p>

Bit/Field	Name	Type	Reset	Description
1:0	CIM	R/W	0x0	<p>Comparison Interrupt Mode</p> <p>This field specifies the mode by which the interrupt comparison is made.</p> <p>Value Description</p> <p>0x0 Always</p> <p>This mode generates an interrupt every time the ADC conversion data falls within the selected operational region.</p> <p>0x1 Once</p> <p>This mode generates an interrupt the first time that the ADC conversion data enters the selected operational region.</p> <p>0x2 Hysteresis Always</p> <p>This mode generates an interrupt when the ADC conversion data falls within the selected operational region and continues to generate the interrupt until the hysteresis condition is cleared by entering the opposite operational region.</p> <p>Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</p> <p>0x3 Hysteresis Once</p> <p>This mode generates an interrupt the first time that the ADC conversion data falls within the selected operational region. No additional interrupts are generated until the hysteresis condition is cleared by entering the opposite operational region.</p> <p>Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</p>

**Register 45: ADC Digital Comparator Range 0 (ADCDCMP0), offset 0xE40**

**Register 46: ADC Digital Comparator Range 1 (ADCDCMP1), offset 0xE44**

**Register 47: ADC Digital Comparator Range 2 (ADCDCMP2), offset 0xE48**

**Register 48: ADC Digital Comparator Range 3 (ADCDCMP3), offset 0xE4C**

**Register 49: ADC Digital Comparator Range 4 (ADCDCMP4), offset 0xE50**

**Register 50: ADC Digital Comparator Range 5 (ADCDCMP5), offset 0xE54**

**Register 51: ADC Digital Comparator Range 6 (ADCDCMP6), offset 0xE58**

**Register 52: ADC Digital Comparator Range 7 (ADCDCMP7), offset 0xE5C**

This register defines the comparison values that are used to determine if the ADC conversion data falls in the appropriate operating region. Note that the value in the COMP1 field must be greater than or equal to the value in the COMP0 field or unexpected results can occur.

#### ADC Digital Comparator Range 0 (ADCDCMP0)

Base 0x4003.8000

Offset 0xE40

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved						COMP1									
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						COMP0									
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:26	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
25:16	COMP1	R/W	0x000	Compare 1  The value in this field is compared against the ADC conversion data. The result of the comparison is used to determine if the data lies within the high-band region.  Note that the value of COMP1 must be greater than or equal to the value of COMP0.
15:10	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9:0	COMP0	R/W	0x000	Compare 0  The value in this field is compared against the ADC conversion data. The result of the comparison is used to determine if the data lies within the low-band region.

## 15 Universal Asynchronous Receivers/Transmitters (UARTs)

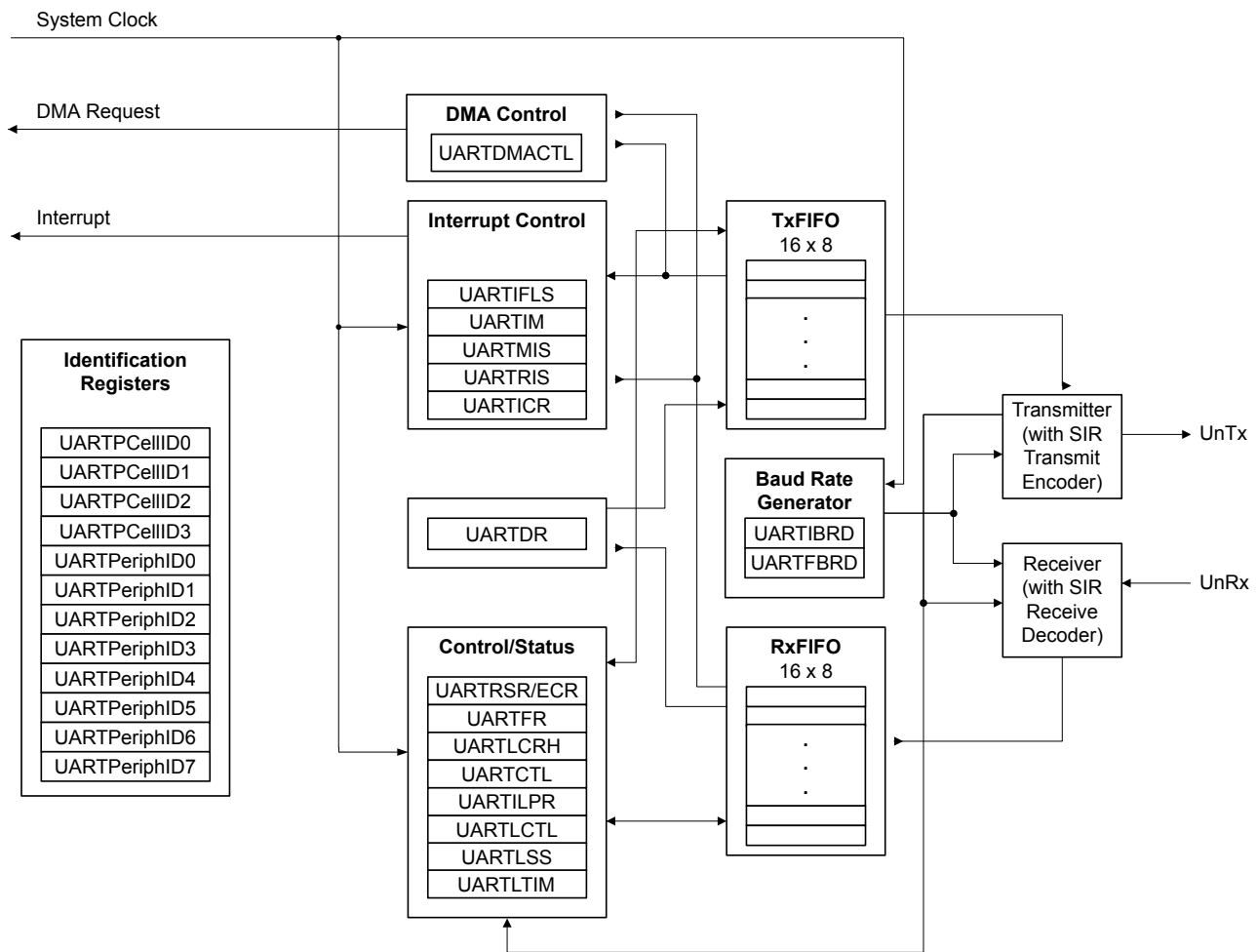
The Stellaris<sup>®</sup> LM3S1811 controller includes three Universal Asynchronous Receiver/Transmitter (UART) with the following features:

- Programmable baud-rate generator allowing speeds up to 3.125 Mbps for regular speed (divide by 16) and 6.25 Mbps for high speed (divide by 8)
- Separate 16x8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- False-start bit detection
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation/detection
  - 1 or 2 stop bit generation
- IrDA serial-IR (SIR) encoder/decoder providing
  - Programmable use of IrDA Serial Infrared (SIR) or UART input/output
  - Support of IrDA SIR encoder/decoder functions for data rates up to 115.2 Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41-2.23  $\mu$ s) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power mode bit duration
- Support for communication with ISO 7816 smart cards
- Full modem handshake support (on UART1)
- LIN protocol support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Separate channels for transmit and receive

- Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
- Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

## 15.1 Block Diagram

Figure 15-1. UART Module Block Diagram



## 15.2 Signal Description

Table 15-1 on page 550 lists the external signals of the UART module and describes the function of each. The UART signals are alternate functions for some GPIO signals and default to be GPIO signals at reset, with the exception of the U0Rx and U0Tx pins which default to the UART function. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for these UART signals. The AFSEL bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) should be set to choose the UART function. The number in parentheses is the encoding that must be programmed into the PMCn field in the **GPIO Port Control (GPIOCTL)** register (page 328) to assign the UART signal to the specified GPIO port pin. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 288.

Table 15-1. Signals for UART

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
U0Rx	26	PA0 (1)	I	TTL	UART module 0 receive. When in IrDA mode, this signal has IrDA modulation.
U0Tx	27	PA1 (1)	O	TTL	UART module 0 transmit. When in IrDA mode, this signal has IrDA modulation.
U1CTS	2 10 34	PE6 (9) PD0 (9) PA6 (9)	I	TTL	UART module 1 Clear To Send modem status input signal.
U1DCD	1 11 35	PE7 (9) PD1 (9) PA7 (9)	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
U1DSR	47	PF0 (9)	I	TTL	UART module 1 Data Set Ready modem output control line.
U1DTR	40 100	PG5 (10) PD7 (9)	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
U1RI	37 41 97	PG6 (10) PG4 (10) PD4 (9)	I	TTL	UART module 1 Ring Indicator modem status input signal.
U1RTS	43 61	PF6 (10) PF1 (9)	O	TTL	UART module 1 Request to Send modem output control line.
U1Rx	10 12 23 26 66 92	PD0 (5) PD2 (1) PC6 (5) PA0 (9) PB0 (5) PB4 (7)	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
U1Tx	11 13 22 27 67 91	PD1 (5) PD3 (1) PC7 (5) PA1 (9) PB1 (5) PB5 (7)	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
U2Rx	10 19 92 98	PD0 (4) PG0 (1) PB4 (4) PD5 (9)	I	TTL	UART module 2 receive. When in IrDA mode, this signal has IrDA modulation.
U2Tx	6 11 18 99	PE4 (5) PD1 (4) PG1 (1) PD6 (9)	O	TTL	UART module 2 transmit. When in IrDA mode, this signal has IrDA modulation.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 15.3 Functional Description

Each Stellaris<sup>®</sup> UART performs the functions of parallel-to-serial and serial-to-parallel conversions. It is similar in functionality to a 16C550 UART, but is not register compatible.

The UART is configured for transmit and/or receive via the TXE and RXE bits of the **UART Control (UARTCTL)** register (see page 574). Transmit and receive are both enabled out of reset. Before any control registers are programmed, the UART must be disabled by clearing the **UARTEN** bit in **UARTCTL**. If the UART is disabled during a TX or RX operation, the current transaction is completed prior to the UART stopping.

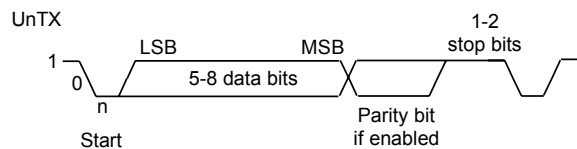
The UART module also includes a serial IR (SIR) encoder/decoder block that can be connected to an infrared transceiver to implement an IrDA SIR physical layer. The SIR function is programmed using the **UARTCTL** register.

### 15.3.1 Transmit/Receive Logic

The transmit logic performs parallel-to-serial conversion on the data read from the transmit FIFO. The control logic outputs the serial bit stream beginning with a start bit and followed by the data bits (LSB first), parity bit, and the stop bits according to the programmed configuration in the control registers. See Figure 15-2 on page 551 for details.

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. Overrun, parity, frame error checking, and line-break detection are also performed, and their status accompanies the data that is written to the receive FIFO.

**Figure 15-2. UART Character Frame**



### 15.3.2 Baud-Rate Generation

The baud-rate divisor is a 22-bit number consisting of a 16-bit integer and a 6-bit fractional part. The number formed by these two values is used by the baud-rate generator to determine the bit period. Having a fractional baud-rate divider allows the UART to generate all the standard baud rates.

The 16-bit integer is loaded through the **UART Integer Baud-Rate Divisor (UARTIBRD)** register (see page 570) and the 6-bit fractional part is loaded with the **UART Fractional Baud-Rate Divisor (UARTFBRD)** register (see page 571). The baud-rate divisor (BRD) has the following relationship to the system clock (where *BRDI* is the integer part of the BRD and *BRDF* is the fractional part, separated by a decimal place.)

$$BRD = BRDI + BRDF = \text{UARTSysClk} / (\text{ClkDiv} * \text{Baud Rate})$$

where *UARTSysClk* is the system clock connected to the UART, and *ClkDiv* is either 16 (if *HSE* in **UARTCTL** is clear) or 8 (if *HSE* is set).

The 6-bit fractional number (that is to be loaded into the *DIVFRAC* bit field in the **UARTFBRD** register) can be calculated by taking the fractional part of the baud-rate divisor, multiplying it by 64, and adding 0.5 to account for rounding errors:

$$\text{UARTFBRD}[\text{DIVFRAC}] = \text{integer}(\text{BRDF} * 64 + 0.5)$$

The UART generates an internal baud-rate reference clock at 8x or 16x the baud-rate (referred to as *Baud8* and *Baud16*, depending on the setting of the *HSE* bit (bit 5) in **UARTCTL**). This reference clock is divided by 8 or 16 to generate the transmit clock, and is used for error detection during receive operations.

Along with the **UART Line Control, High Byte (UARTLCRH)** register (see page 572), the **UARTIBRD** and **UARTFBRD** registers form an internal 30-bit register. This internal register is only updated when a write operation to **UARTLCRH** is performed, so any changes to the baud-rate divisor must be followed by a write to the **UARTLCRH** register for the changes to take effect.

To update the baud-rate registers, there are four possible sequences:

- **UARTIBRD** write, **UARTFBRD** write, and **UARTLCRH** write
- **UARTFBRD** write, **UARTIBRD** write, and **UARTLCRH** write
- **UARTIBRD** write and **UARTLCRH** write
- **UARTFBRD** write and **UARTLCRH** write

### 15.3.3 Data Transmission

Data received or transmitted is stored in two 16-byte FIFOs, though the receive FIFO has an extra four bits per character for status information. For transmission, data is written into the transmit FIFO. If the UART is enabled, it causes a data frame to start transmitting with the parameters indicated in the **UARTLCRH** register. Data continues to be transmitted until there is no data left in the transmit FIFO. The **BUSY** bit in the **UART Flag (UARTFR)** register (see page 566) is asserted as soon as data is written to the transmit FIFO (that is, if the FIFO is non-empty) and remains asserted while data is being transmitted. The **BUSY** bit is negated only when the transmit FIFO is empty, and the last character has been transmitted from the shift register, including the stop bits. The UART can indicate that it is busy even though the UART may no longer be enabled.

When the receiver is idle (the  $UnRx$  signal is continuously 1), and the data input goes Low (a start bit has been received), the receive counter begins running and data is sampled on the eighth cycle of **Baud16** or fourth cycle of **Baud8** depending on the setting of the **HSE** bit (bit 5) in **UARTCTL** (described in “Transmit/Receive Logic” on page 551).

The start bit is valid if the  $UnRx$  signal is still low on the eighth cycle of **Baud16** (**HSE** clear) or the fourth cycle of **Baud 8** (**HSE** set), otherwise a false start bit is detected and is ignored. Start bit errors can be viewed in the **UART Receive Status (UARTSR)** register (see page 563). If the start bit was valid, successive data bits are sampled on every 16th cycle of **Baud16** or 8th cycle of **Baud8** (that is, one bit period later) according to the programmed length of the data characters and value of the **HSE** bit in **UARTCTL**. The parity bit is then checked if parity mode is enabled. Data length and parity are defined in the **UARTLCRH** register.

Lastly, a valid stop bit is confirmed if the  $UnRx$  signal is High, otherwise a framing error has occurred. When a full word is received, the data is stored in the receive FIFO along with any error bits associated with that word.

### 15.3.4 Serial IR (SIR)

The UART peripheral includes an IrDA serial-IR (SIR) encoder/decoder block. The IrDA SIR block provides functionality that converts between an asynchronous UART data stream and a half-duplex serial SIR interface. No analog processing is performed on-chip. The role of the SIR block is to provide a digital encoded output and decoded input to the UART. When enabled, the SIR block uses the  $UnTx$  and  $UnRx$  pins for the SIR protocol. These signals should be connected to an infrared transceiver to implement an IrDA SIR physical layer link. The SIR block can receive and transmit, but it is only half-duplex so it cannot do both at the same time. Transmission must be stopped before data can be received. The IrDA SIR physical layer specifies a minimum 10-ms delay between transmission and reception. The SIR block has two modes of operation:

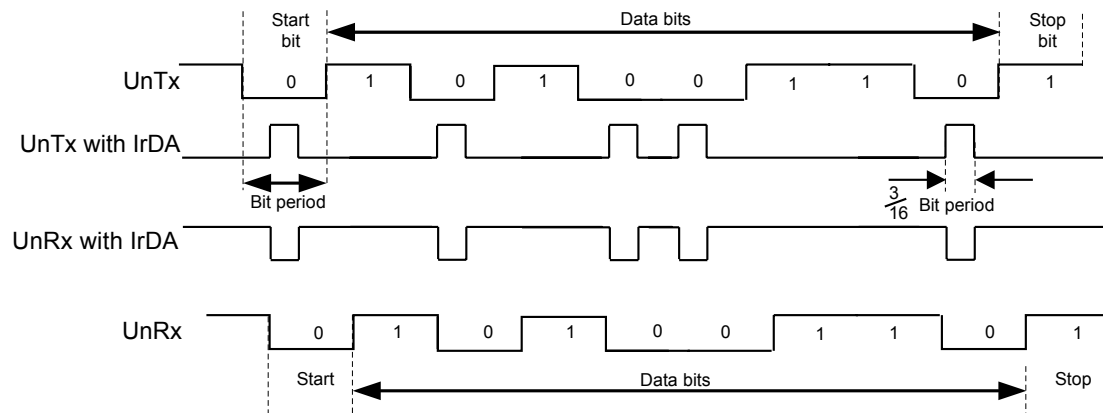
- In normal IrDA mode, a zero logic level is transmitted as a high pulse of 3/16th duration of the selected baud rate bit period on the output pin, while logic one levels are transmitted as a static LOW signal. These levels control the driver of an infrared transmitter, sending a pulse of light for each zero. On the reception side, the incoming light pulses energize the photo transistor base of the receiver, pulling its output LOW and driving the UART input pin LOW.



- In low-power IrDA mode, the width of the transmitted infrared pulse is set to three times the period of the internally generated IrLPBaud16 signal (1.63  $\mu$ s, assuming a nominal 1.8432 MHz frequency) by changing the appropriate bit in the **UARTCR** register. See page 569 for more information on IrDA low-power pulse-duration configuration.

Figure 15-3 on page 553 shows the UART transmit and receive signals, with and without IrDA modulation.

**Figure 15-3. IrDA Data Modulation**



In both normal and low-power IrDA modes:

- During transmission, the UART data bit is used as the base for encoding
- During reception, the decoded bits are transferred to the UART receive logic

The IrDA SIR physical layer specifies a half-duplex communication link, with a minimum 10-ms delay between transmission and reception. This delay must be generated by software because it is not automatically supported by the UART. The delay is required because the infrared receiver electronics might become biased or even saturated from the optical power coupled from the adjacent transmitter LED. This delay is known as latency or receiver setup time.

### 15.3.5 ISO 7816 Support

The UART offers basic support to allow communication with an ISO 7816 smartcard. When bit 3 (**SMART**) of the **UARTCTL** register is set, the **UnTx** signal is used as a bit clock, and the **UnRx** signal is used as the half-duplex communication line connected to the smartcard. A GPIO signal can be used to generate the reset signal to the smartcard. The remaining smartcard signals should be provided by the system design.

When using ISO 7816 mode, the **UARTLCRH** register must be set to transmit 8-bit words (**WLEN** bits 6:5 configured to 0x3) with EVEN parity (**PEN** set and **EPS** set). In this mode, the UART automatically uses 2 stop bits, and the **STP2** bit of the **UARTLCRH** register is ignored.

If a parity error is detected during transmission, **UnRx** is pulled Low during the second stop bit. In this case, the UART aborts the transmission, flushes the transmit FIFO and discards any data it contains, and raises a parity error interrupt, allowing software to detect the problem and initiate retransmission of the affected data. Note that the UART does not support automatic retransmission in this case.

## 15.3.6 Modem Handshake Support

This section describes how to configure and use the modem status signals for UART1 when connected as a DTE (data terminal equipment) or as a DCE (data communications equipment). In general, a modem is a DCE and a computing device that connects to a modem is the DTE.

### 15.3.6.1 Signaling

The status signals provided by UART1 differ based on whether the UART is used as a DTE or DCE. When used as a DTE, the modem status signals are defined as:

- $\overline{\text{UICTS}}$  is Clear To Send
- $\overline{\text{UIDSR}}$  is Data Set Ready
- $\overline{\text{UIDCD}}$  is Data Carrier Detect
- $\overline{\text{UIRI}}$  is Ring Indicator
- $\overline{\text{UIRTS}}$  is Request To Send
- $\overline{\text{UIDTR}}$  is Data Terminal Ready

When used as a DCE, the the modem status signals are defined as:

- $\overline{\text{UICTS}}$  is Request To Send
- $\overline{\text{UIDSR}}$  is Data Terminal Ready
- $\overline{\text{UIRTS}}$  is Clear To Send
- $\overline{\text{UIDTR}}$  is Data Set Ready

Note that the support for DCE functions Data Carrier Detect and Ring Indicator are not provided. If these signals are required, their function can be emulated by using a general-purpose I/O signal and providing software support.

### 15.3.6.2 Flow Control Methods

Flow control can be accomplished by either hardware or software. The following sections describe the different methods.

#### **Hardware Flow Control (RTS/CTS)**

Hardware flow control between two devices is accomplished by connecting the  $\overline{\text{UIRTS}}$  output to the Clear-To-Send input on the receiving device, and connecting the Request-To-Send output on the receiving device to the  $\overline{\text{UICTS}}$  input.

The  $\overline{\text{UICTS}}$  input controls the transmitter. The transmitter may only transmit data when the  $\overline{\text{UICTS}}$  input is asserted. The  $\overline{\text{UIRTS}}$  output signal indicates the state of the receive FIFO.  $\overline{\text{UICTS}}$  remains asserted until the preprogrammed watermark level is reached, indicating that the Receive FIFO has no space to store additional characters.

The **UARTCTL** register bits 15 (CTSEN) and 14 (RTSEN) specify the flow control mode as shown in Table 15-2 on page 555.

**Table 15-2. Flow Control Mode**

CTSEN	RTSEN	Description
1	1	RTS and CTS flow control enabled
1	0	Only CTS flow control enabled
0	1	Only RTS flow control enabled
0	0	Both RTS and CTS flow control disabled

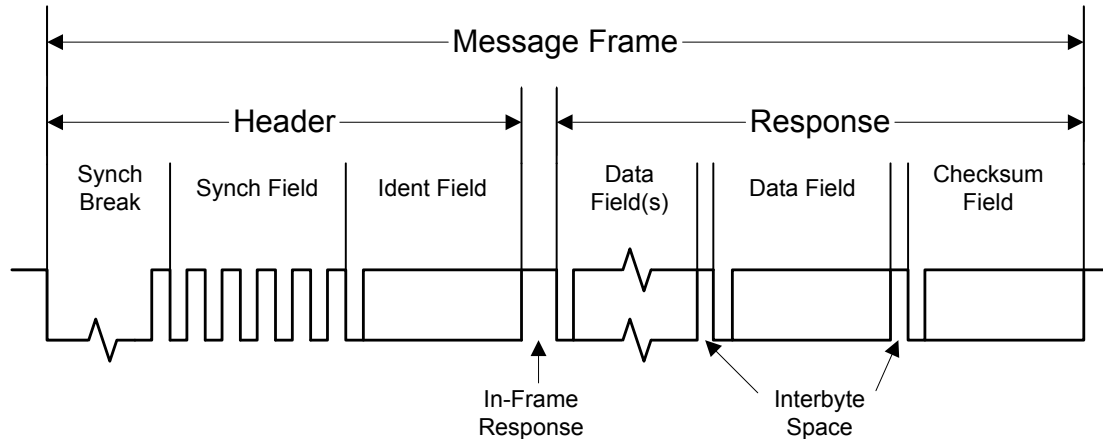
Note that when `RTSEN` is 1, software cannot modify the  $\overline{\text{U}1\text{RTS}}$  output value through the `UARTCTL` register Request to Send (RTS) bit, and the status of the RTS bit should be ignored.

#### Software Flow Control (Modem Status Interrupts)

Software flow control between two devices is accomplished by using interrupts to indicate the status of the UART. Interrupts may be generated for  $\overline{\text{U}1\text{DSR}}$ ,  $\overline{\text{U}1\text{DCD}}$ ,  $\overline{\text{U}1\text{CTS}}$ , and  $\overline{\text{U}1\text{RI}}$  using the `UARTIM` bits 3 through 0 respectively. The raw and masked interrupt status may be checked using the `UARTRIS` and `UARTMIS` register. These interrupts may be cleared using the `UARTICR` register.

### 15.3.7 LIN Support

The UART module offers hardware support for the LIN protocol as either a master or a slave. The LIN mode is enabled by setting the `LIN` bit in the `UARTCTL` register. A LIN message is identified by the use of a Sync Break at the beginning of the message. The Sync Break is a transmission of a series of 0s. The Sync Break is followed by the Sync data field (0x55). Figure 15-4 on page 555 illustrates the structure of a LIN message.

**Figure 15-4. LIN Message**

The UART should be configured as followed to operate in LIN mode:

1. Configure the UART for 1 start bit, 8 data bits, no parity, and 1 stop bit. Enable the Transmit FIFO.
2. Set the `LIN` bit in the `UARTCTL` register.

When preparing to send a LIN message, the TXFIFO should contain the Sync data (0x55) at FIFO location 0 and the Identifier data at location 1, followed by the data to be transmitted, and with the checksum in the final FIFO entry.

### 15.3.7.1 LIN Master

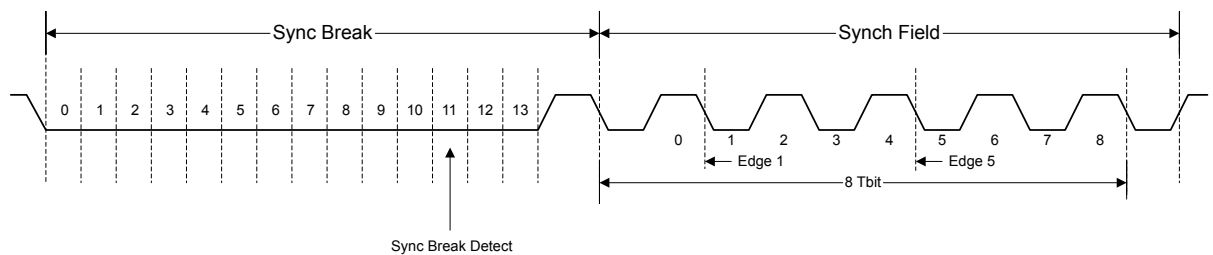
The UART is enabled to be the LIN master by setting the `MASTER` bit in the `UARTLCTL` register. The length of the Sync Break is programmable using the `BLEN` field in the `UARTLCTL` register and can be 13-16 bits (baud clock cycles).

### 15.3.7.2 LIN Slave

The LIN UART slave is required to adjust its baud rate to that of the LIN master. In slave mode, the LIN UART recognizes the Sync Break, which must be at least 13 bits in duration. A timer is provided to capture timing data on the 1st and 5th falling edges of the Sync field so that the baud rate can be adjusted to match the master.

After detecting a Sync Break, the UART waits for the synchronization field. The first falling edge generates an interrupt using the `LME1RIS` bit in the `UARTRIS` register, and the timer value is captured and stored in the `UARTLSS` register (T1). On the fifth falling edge, a second interrupt is generated using the `LME5RIS` bit in the `UARTRIS` register, and the timer value is captured again (T2). The actual baud rate can be calculated using  $(T2-T1)/8$ , and the local baud rate should be adjusted as needed. Figure 15-5 on page 556 illustrates the synchronization field.

**Figure 15-5. LIN Synchronization Field**



### 15.3.8 FIFO Operation

The UART has two 16-entry FIFOs; one for transmit and one for receive. Both FIFOs are accessed via the **UART Data (UARTDR)** register (see page 561). Read operations of the `UARTDR` register return a 12-bit value consisting of 8 data bits and 4 error flags while write operations place 8-bit data in the transmit FIFO.

Out of reset, both FIFOs are disabled and act as 1-byte-deep holding registers. The FIFOs are enabled by setting the `FEN` bit in `UARTLCRH` (page 572).

FIFO status can be monitored via the **UART Flag (UARTFR)** register (see page 566) and the **UART Receive Status (UARTRSR)** register. Hardware monitors empty, full and overrun conditions. The `UARTFR` register contains empty and full flags (`TXFE`, `TXFF`, `RXFE`, and `RXFF` bits), and the `UARTRSR` register shows overrun status via the `OE` bit.

The trigger points at which the FIFOs generate interrupts is controlled via the **UART Interrupt FIFO Level Select (UARTIFLS)** register (see page 578). Both FIFOs can be individually configured to trigger interrupts at different levels. Available configurations include  $\frac{1}{8}$ ,  $\frac{1}{4}$ ,  $\frac{1}{2}$ ,  $\frac{3}{4}$ , and  $\frac{7}{8}$ . For example, if the  $\frac{1}{4}$  option is selected for the receive FIFO, the UART generates a receive interrupt after 4 data bytes are received. Out of reset, both FIFOs are configured to trigger an interrupt at the  $\frac{1}{2}$  mark.

### 15.3.9 Interrupts

The UART can generate interrupts when the following conditions are observed:

- Overrun Error
- Break Error
- Parity Error
- Framing Error
- Receive Timeout
- Transmit (when condition defined in the `TXIFLSEL` bit in the **UARTIFLS** register is met, or if the `EOT` bit in **UARTCTRL** is set, when the last bit of all transmitted data leaves the serializer)
- Receive (when condition defined in the `RXIFLSEL` bit in the **UARTIFLS** register is met)

All of the interrupt events are ORed together before being sent to the interrupt controller, so the UART can only generate a single interrupt request to the controller at any given time. Software can service multiple interrupt events in a single interrupt service routine by reading the **UART Masked Interrupt Status (UARTMIS)** register (see page 588).

The interrupt events that can trigger a controller-level interrupt are defined in the **UART Interrupt Mask (UARTIM)** register (see page 580) by setting the corresponding `IM` bits. If interrupts are not used, the raw interrupt status is always visible via the **UART Raw Interrupt Status (UARTRIS)** register (see page 584).

Interrupts are always cleared (for both the **UARTMIS** and **UARTRIS** registers) by writing a 1 to the corresponding bit in the **UART Interrupt Clear (UARTICR)** register (see page 591).

The receive timeout interrupt is asserted when the receive FIFO is not empty, and no further data is received over a 32-bit period. The receive timeout interrupt is cleared either when the FIFO becomes empty through reading all the data (or by reading the holding register), or when a 1 is written to the corresponding bit in the **UARTICR** register.

### 15.3.10 Loopback Operation

The UART can be placed into an internal loopback mode for diagnostic or debug work by setting the `LBE` bit in the **UARTCTL** register (see page 574). In loopback mode, data transmitted on the `UnTx` output is received on the `UnRx` input.

### 15.3.11 DMA Operation

The UART provides an interface to the  $\mu$ DMA controller with separate channels for transmit and receive. The DMA operation of the UART is enabled through the **UART DMA Control (UARTDMACTL)** register. When DMA operation is enabled, the UART asserts a DMA request on the receive or transmit channel when the associated FIFO can transfer data. For the receive channel, a single transfer request is asserted whenever any data is in the receive FIFO. A burst transfer request is asserted whenever the amount of data in the receive FIFO is at or above the FIFO trigger level configured in the **UARTIFLS** register. For the transmit channel, a single transfer request is asserted whenever there is at least one empty location in the transmit FIFO. The burst request is asserted whenever the transmit FIFO contains fewer characters than the FIFO trigger level. The single and burst DMA transfer requests are handled automatically by the  $\mu$ DMA controller depending on how the DMA channel is configured.

To enable DMA operation for the receive channel, set the `RXDMAE` bit of the **DMA Control (UARTDMACTL)** register. To enable DMA operation for the transmit channel, set the `TXDMAE` bit of the **UARTDMACTL** register. The UART can also be configured to stop using DMA for the receive

channel if a receive error occurs. If the `DMAERR` bit of the `UARTDMACR` register is set and a receive error occurs, the DMA receive requests are automatically disabled. This error condition can be cleared by clearing the appropriate UART error interrupt.

If DMA is enabled, then the  $\mu$ DMA controller triggers an interrupt when a transfer is complete. The interrupt occurs on the UART interrupt vector. Therefore, if interrupts are used for UART operation and DMA is enabled, the UART interrupt handler must be designed to handle the  $\mu$ DMA completion interrupt.

See “Micro Direct Memory Access ( $\mu$ DMA)” on page 230 for more details about programming the  $\mu$ DMA controller.

## 15.4 Initialization and Configuration

To enable and initialize the UART, the following steps are necessary:

1. The peripheral clock must be enabled by setting the `UART0`, `UART1`, or `UART2` bits in the `RCGC1` register (see page 149).
2. The clock to the appropriate GPIO module must be enabled via the `RCGC2` register in the System Control module (see page 158).
3. Set the GPIO `AFSEL` bits for the appropriate pins (see page 310). To determine which GPIOs to configure, see Table 20-4 on page 717.
4. Configure the GPIO current level and/or slew rate as specified for the mode selected (see page 312 and page 320).
5. Configure the `PMCn` fields in the `GPIOPCTL` register to assign the UART signals to the appropriate pins (see page 328 and Table 20-5 on page 722).

To use the UARTs, the peripheral clock must be enabled by setting the `UART0`, `UART1`, or `UART2` bits in the `RCGC1` register (see page 149). In addition, the clock to the appropriate GPIO module must be enabled via the `RCGC2` register in the System Control module (see page 158). To find out which GPIO port to enable, refer to Table 20-5 on page 722.

This section discusses the steps that are required to use a UART module. For this example, the UART clock is assumed to be 20 MHz, and the desired UART configuration is:

- 115200 baud rate
- Data length of 8 bits
- One stop bit
- No parity
- FIFOs disabled
- No interrupts

The first thing to consider when programming the UART is the baud-rate divisor (BRD), because the `UARTIBRD` and `UARTFBRD` registers must be written before the `UARTLCRH` register. Using the equation described in “Baud-Rate Generation” on page 551, the BRD can be calculated:

$$\text{BRD} = 20,000,000 / (16 * 115,200) = 10.8507$$

which means that the `DIVINT` field of the **UARTIBRD** register (see page 570) should be set to 10 decimal or `0xA`. The value to be loaded into the **UARTFBRD** register (see page 571) is calculated by the equation:

$$\text{UARTFBRD}[\text{DIVFRAC}] = \text{integer}(0.8507 * 64 + 0.5) = 54$$

With the BRD values in hand, the UART configuration is written to the module in the following order:

1. Disable the UART by clearing the `UARTEN` bit in the **UARTCTL** register.
2. Write the integer portion of the BRD to the **UARTIBRD** register.
3. Write the fractional portion of the BRD to the **UARTFBRD** register.
4. Write the desired serial parameters to the **UARTLCRH** register (in this case, a value of `0x0000.0060`).
5. Optionally, configure the  $\mu$ DMA channel (see “Micro Direct Memory Access ( $\mu$ DMA)” on page 230) and enable the DMA option(s) in the **UARTDMACTL** register.
6. Enable the UART by setting the `UARTEN` bit in the **UARTCTL** register.

## 15.5 Register Map

Table 15-3 on page 559 lists the UART registers. The offset listed is a hexadecimal increment to the register's address, relative to that UART's base address:

- UART0: `0x4000.C000`
- UART1: `0x4000.D000`
- UART2: `0x4000.E000`

Note that the UART module clock must be enabled before the registers can be programmed (see page 149).

**Note:** The UART must be disabled (see the `UARTEN` bit in the **UARTCTL** register on page 574) before any of the control registers are reprogrammed. When the UART is disabled during a TX or RX operation, the current transaction is completed prior to the UART stopping.

**Table 15-3. UART Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	UARTDR	R/W	0x0000.0000	UART Data	561
0x004	UARTSR/UARTECR	R/W	0x0000.0000	UART Receive Status/Error Clear	563
0x018	UARTFR	RO	0x0000.0090	UART Flag	566
0x020	UARTILPR	R/W	0x0000.0000	UART IrDA Low-Power Register	569
0x024	UARTIBRD	R/W	0x0000.0000	UART Integer Baud-Rate Divisor	570
0x028	UARTFBRD	R/W	0x0000.0000	UART Fractional Baud-Rate Divisor	571
0x02C	UARTLCRH	R/W	0x0000.0000	UART Line Control	572
0x030	UARTCTL	R/W	0x0000.0300	UART Control	574
0x034	UARTIFLS	R/W	0x0000.0012	UART Interrupt FIFO Level Select	578

Table 15-3. UART Register Map (continued)

Offset	Name	Type	Reset	Description	See page
0x038	UARTIM	R/W	0x0000.0000	UART Interrupt Mask	580
0x03C	UARTRIS	RO	0x0000.000F	UART Raw Interrupt Status	584
0x040	UARTMIS	RO	0x0000.0000	UART Masked Interrupt Status	588
0x044	UARTICR	W1C	0x0000.0000	UART Interrupt Clear	591
0x048	UARTDMACTL	R/W	0x0000.0000	UART DMA Control	593
0x090	UARTLCTL	R/W	0x0000.0000	UART LIN Control	594
0x094	UARTLSS	RO	0x0000.0000	UART LIN Snap Shot	595
0x098	UARTLTIM	RO	0x0000.0000	UART LIN Timer	596
0xFD0	UARTPeriphID4	RO	0x0000.0000	UART Peripheral Identification 4	597
0xFD4	UARTPeriphID5	RO	0x0000.0000	UART Peripheral Identification 5	598
0xFD8	UARTPeriphID6	RO	0x0000.0000	UART Peripheral Identification 6	599
0xFDC	UARTPeriphID7	RO	0x0000.0000	UART Peripheral Identification 7	600
0xFE0	UARTPeriphID0	RO	0x0000.0060	UART Peripheral Identification 0	601
0xFE4	UARTPeriphID1	RO	0x0000.0000	UART Peripheral Identification 1	602
0xFE8	UARTPeriphID2	RO	0x0000.0018	UART Peripheral Identification 2	603
0xFEC	UARTPeriphID3	RO	0x0000.0001	UART Peripheral Identification 3	604
0xFF0	UARTPCellID0	RO	0x0000.000D	UART PrimeCell Identification 0	605
0xFF4	UARTPCellID1	RO	0x0000.00F0	UART PrimeCell Identification 1	606
0xFF8	UARTPCellID2	RO	0x0000.0005	UART PrimeCell Identification 2	607
0xFFC	UARTPCellID3	RO	0x0000.00B1	UART PrimeCell Identification 3	608

## 15.6 Register Descriptions

The remainder of this section lists and describes the UART registers, in numerical order by address offset.



## Register 1: UART Data (UARTDR), offset 0x000

**Important:** Use caution when reading this register. Performing a read may change bit status.

This register is the data register (the interface to the FIFOs).

For transmitted data, if the FIFO is enabled, data written to this location is pushed onto the transmit FIFO. If the FIFO is disabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO). A write to this register initiates a transmission from the UART.

For received data, if the FIFO is enabled, the data byte and the 4-bit status (break, frame, parity, and overrun) is pushed onto the 12-bit wide receive FIFO. If the FIFO is disabled, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO). The received data can be retrieved by reading this register.

### UART Data (UARTDR)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x000  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved				OE	BE	PE	FE	DATA							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:12	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	OE	RO	0	UART Overrun Error
				Value Description
				1 New data was received when the FIFO was full, resulting in data loss.
				0 No data has been lost due to a FIFO overrun.
10	BE	RO	0	UART Break Error
				Value Description
				1 A break condition has been detected, indicating that the receive data input was held Low for longer than a full-word transmission time (defined as start, data, parity, and stop bits).
				0 No break condition has occurred
				In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the received data input goes to a 1 (marking state), and the next valid start bit is received.

Bit/Field	Name	Type	Reset	Description
9	PE	RO	0	UART Parity Error  Value Description 1 The parity of the received data character does not match the parity defined by bits 2 and 7 of the <b>UARTLCRH</b> register. 0 No parity error has occurred  In FIFO mode, this error is associated with the character at the top of the FIFO.
8	FE	RO	0	UART Framing Error  Value Description 1 The received character does not have a valid stop bit (a valid stop bit is 1). 0 No framing error has occurred
7:0	DATA	R/W	0x00	Data Transmitted or Received  Data that is to be transmitted via the UART is written to this field.  When read, this field contains the data that was received by the UART.

## Register 2: UART Receive Status/Error Clear (UARTRSR/UARTECR), offset 0x004

The **UARTRSR/UARTECR** register is the receive status register/error clear register.

In addition to the **UARTDR** register, receive status can also be read from the **UARTRSR** register. If the status is read from this register, then the status information corresponds to the entry read from **UARTDR** prior to reading **UARTRSR**. The status information for overrun is set immediately when an overrun condition occurs.

The **UARTRSR** register cannot be written.

A write of any value to the **UARTECR** register clears the framing, parity, break, and overrun errors. All the bits are cleared on reset.

### Read-Only Status Register

#### UART Receive Status/Error Clear (UARTRSR/UARTECR)

UART0 base: 0x4000.C000

UART1 base: 0x4000.D000

UART2 base: 0x4000.E000

Offset 0x004

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													OE	BE	PE	FE
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	OE	RO	0	UART Overrun Error
				Value Description
				1 New data was received when the FIFO was full, resulting in data loss.
				0 No data has been lost due to a FIFO overrun.

This bit is cleared by a write to **UARTECR**.

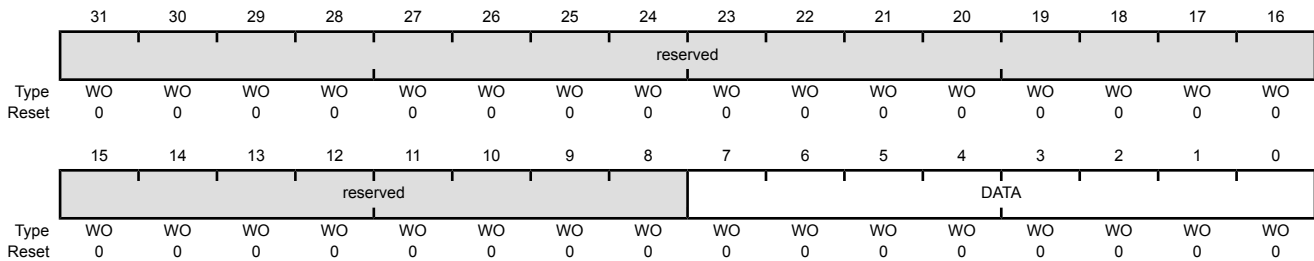
The FIFO contents remain valid because no further data is written when the FIFO is full, only the contents of the shift register are overwritten. The CPU must read the data in order to empty the FIFO.

Bit/Field	Name	Type	Reset	Description
2	BE	RO	0	<p>UART Break Error</p> <p>Value Description</p> <p>1 A break condition has been detected, indicating that the receive data input was held Low for longer than a full-word transmission time (defined as start, data, parity, and stop bits).</p> <p>0 No break condition has occurred</p> <p>This bit is cleared to 0 by a write to <b>UARTECR</b>.</p> <p>In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a 1 (marking state) and the next valid start bit is received.</p>
1	PE	RO	0	<p>UART Parity Error</p> <p>Value Description</p> <p>1 The parity of the received data character does not match the parity defined by bits 2 and 7 of the <b>UARTLCRH</b> register.</p> <p>0 No parity error has occurred</p> <p>This bit is cleared to 0 by a write to <b>UARTECR</b>.</p>
0	FE	RO	0	<p>UART Framing Error</p> <p>Value Description</p> <p>1 The received character does not have a valid stop bit (a valid stop bit is 1).</p> <p>0 No framing error has occurred</p> <p>This bit is cleared to 0 by a write to <b>UARTECR</b>.</p> <p>In FIFO mode, this error is associated with the character at the top of the FIFO.</p>

**Write-Only Error Clear Register**

UART Receive Status/Error Clear (UARTRSR/UARTECR)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x004  
 Type WO, reset 0x0000.0000



---

Bit/Field	Name	Type	Reset	Description
31:8	reserved	WO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DATA	WO	0x00	Error Clear A write to this register of any data clears the framing, parity, break, and overrun flags.

### Register 3: UART Flag (UARTFR), offset 0x018

The **UARTFR** register is the flag register. After reset, the **TXFF**, **RXFF**, and **BUSY** bits are 0, and **TXFE** and **RXFE** bits are 1. The **RI**, **DCD**, **DSR** and **CTS** bits indicate the modem status.

Note that bits [8,2:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

#### UART Flag (UARTFR)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x018  
 Type RO, reset 0x0000.0090

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							RI	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:9	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8	RI	RO	0	Ring Indicator  Value Description 1 The <b>URI</b> signal is asserted. 0 The <b>URI</b> signal is not asserted.  This bit is implemented only on UART1 and is reserved for UART0 and UART2.
7	TXFE	RO	1	UART Transmit FIFO Empty  The meaning of this bit depends on the state of the <b>FEN</b> bit in the <b>UARTLCRH</b> register.  Value Description 1 If the FIFO is disabled ( <b>FEN</b> is 0), the transmit holding register is empty. If the FIFO is enabled ( <b>FEN</b> is 1), the transmit FIFO is empty. 0 The transmitter has data to transmit.

Bit/Field	Name	Type	Reset	Description
6	RXFF	RO	0	<p>UART Receive FIFO Full</p> <p>The meaning of this bit depends on the state of the <code>FEN</code> bit in the <b>UARTLCRH</b> register.</p> <p>Value Description</p> <p>1 If the FIFO is disabled (<code>FEN</code> is 0), the receive holding register is full.</p> <p>If the FIFO is enabled (<code>FEN</code> is 1), the receive FIFO is full.</p> <p>0 The receiver can receive data.</p>
5	TXFF	RO	0	<p>UART Transmit FIFO Full</p> <p>The meaning of this bit depends on the state of the <code>FEN</code> bit in the <b>UARTLCRH</b> register.</p> <p>Value Description</p> <p>1 If the FIFO is disabled (<code>FEN</code> is 0), the transmit holding register is full.</p> <p>If the FIFO is enabled (<code>FEN</code> is 1), the transmit FIFO is full.</p> <p>0 The transmitter is not full.</p>
4	RXFE	RO	1	<p>UART Receive FIFO Empty</p> <p>The meaning of this bit depends on the state of the <code>FEN</code> bit in the <b>UARTLCRH</b> register.</p> <p>Value Description</p> <p>1 If the FIFO is disabled (<code>FEN</code> is 0), the receive holding register is empty.</p> <p>If the FIFO is enabled (<code>FEN</code> is 1), the receive FIFO is empty.</p> <p>0 The receiver is not empty.</p>
3	BUSY	RO	0	<p>UART Busy</p> <p>Value Description</p> <p>1 The UART is busy transmitting data. This bit remains set until the complete byte, including all stop bits, has been sent from the shift register.</p> <p>0 The UART is not busy.</p> <p>This bit is set as soon as the transmit FIFO becomes non-empty (regardless of whether UART is enabled).</p>
2	DCD	RO	0	<p>Data Carrier Detect</p> <p>Value Description</p> <p>1 The <code>U1DCD</code> signal is asserted.</p> <p>0 The <code>U1DCD</code> signal is not asserted.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>

Bit/Field	Name	Type	Reset	Description
1	DSR	RO	0	Data Set Ready  Value Description 1 The U1DSR signal is asserted. 0 The U1DSR signal is not asserted.  This bit is implemented only on UART1 and is reserved for UART0 and UART2.
0	CTS	RO	0	Clear To Send  Value Description 1 The U1CTS signal is asserted. 0 The U1CTS signal is not asserted.  This bit is implemented only on UART1 and is reserved for UART0 and UART2.



## Register 4: UART IrDA Low-Power Register (UARTILPR), offset 0x020

The **UARTILPR** register stores the 8-bit low-power counter divisor value used to derive the low-power SIR pulse width clock by dividing down the system clock (SysClk). All the bits are cleared when reset.

The internal  $F_{IrLPBaud16}$  clock is generated by dividing down SysClk according to the low-power divisor value written to **UARTILPR**. The duration of SIR pulses generated when low-power mode is enabled is three times the period of the  $F_{IrLPBaud16}$  clock. The low-power divisor value is calculated as follows:

$$ILPDVSR = SysClk / F_{IrLPBaud16}$$

where  $F_{IrLPBaud16}$  is nominally 1.8432 MHz.

The divisor must be programmed such that  $1.42 \text{ MHz} < F_{IrLPBaud16} < 2.12 \text{ MHz}$ , resulting in a low-power pulse duration of 1.41–2.11  $\mu\text{s}$  (three times the period of  $F_{IrLPBaud16}$ ). The minimum frequency of  $F_{IrLPBaud16}$  ensures that pulses less than one period of  $F_{IrLPBaud16}$  are rejected, but pulses greater than 1.4  $\mu\text{s}$  are accepted as valid pulses.

**Note:** Zero is an illegal value. Programming a zero value results in no  $F_{IrLPBaud16}$  pulses being generated.

### UART IrDA Low-Power Register (UARTILPR)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x020  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								ILPDVSR							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	ILPDVSR	R/W	0x00	IrDA Low-Power Divisor  This field contains the 8-bit low-power divisor value.

### Register 5: UART Integer Baud-Rate Divisor (UARTIBRD), offset 0x024

The **UARTIBRD** register is the integer part of the baud-rate divisor value. All the bits are cleared on reset. The minimum possible divide ratio is 1 (when **UARTIBRD**=0), in which case the **UARTFBRD** register is ignored. When changing the **UARTIBRD** register, the new value does not take effect until transmission/reception of the current character is complete. Any changes to the baud-rate divisor must be followed by a write to the **UARTLCRH** register. See “Baud-Rate Generation” on page 551 for configuration details.

#### UART Integer Baud-Rate Divisor (UARTIBRD)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x024  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	DIVINT	R/W	0x0000	Integer Baud-Rate Divisor

## Register 6: UART Fractional Baud-Rate Divisor (UARTFBRD), offset 0x028

The **UARTFBRD** register is the fractional part of the baud-rate divisor value. All the bits are cleared on reset. When changing the **UARTFBRD** register, the new value does not take effect until transmission/reception of the current character is complete. Any changes to the baud-rate divisor must be followed by a write to the **UARTLCRH** register. See “Baud-Rate Generation” on page 551 for configuration details.

### UART Fractional Baud-Rate Divisor (UARTFBRD)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x028  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved										DIVFRAC					
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:6	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5:0	DIVFRAC	R/W	0x0	Fractional Baud-Rate Divisor

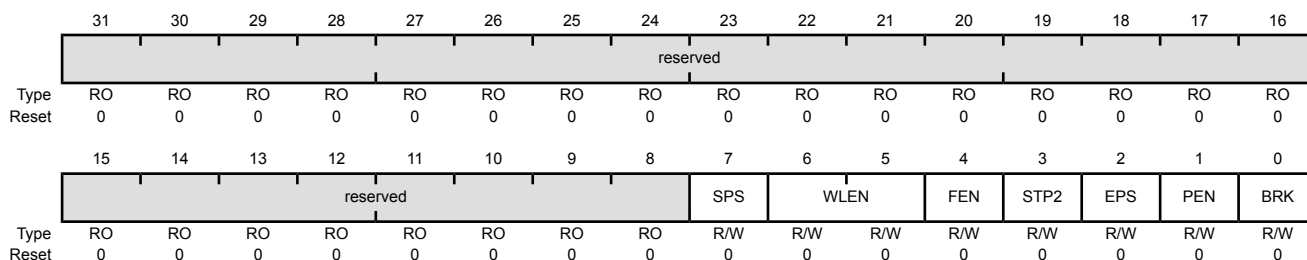
### Register 7: UART Line Control (UARTLCRH), offset 0x02C

The **UARTLCRH** register is the line control register. Serial parameters such as data length, parity, and stop bit selection are implemented in this register.

When updating the baud-rate divisor (**UARTIBRD** and/or **UARTIFRD**), the **UARTLCRH** register must also be written. The write strobe for the baud-rate divisor registers is tied to the **UARTLCRH** register.

#### UART Line Control (UARTLCRH)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x02C  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description										
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										
7	SPS	R/W	0	UART Stick Parity Select  When bits 1, 2, and 7 of <b>UARTLCRH</b> are set, the parity bit is transmitted and checked as a 0. When bits 1 and 7 are set and 2 is cleared, the parity bit is transmitted and checked as a 1.  When this bit is cleared, stick parity is disabled.										
6:5	WLEN	R/W	0x0	UART Word Length  The bits indicate the number of data bits transmitted or received in a frame as follows:  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>5 bits (default)</td> </tr> <tr> <td>0x1</td> <td>6 bits</td> </tr> <tr> <td>0x2</td> <td>7 bits</td> </tr> <tr> <td>0x3</td> <td>8 bits</td> </tr> </tbody> </table>	Value	Description	0x0	5 bits (default)	0x1	6 bits	0x2	7 bits	0x3	8 bits
Value	Description													
0x0	5 bits (default)													
0x1	6 bits													
0x2	7 bits													
0x3	8 bits													
4	FEN	R/W	0	UART Enable FIFOs  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>The transmit and receive FIFO buffers are enabled (FIFO mode).</td> </tr> <tr> <td>0</td> <td>The FIFOs are disabled (Character mode). The FIFOs become 1-byte-deep holding registers.</td> </tr> </tbody> </table>	Value	Description	1	The transmit and receive FIFO buffers are enabled (FIFO mode).	0	The FIFOs are disabled (Character mode). The FIFOs become 1-byte-deep holding registers.				
Value	Description													
1	The transmit and receive FIFO buffers are enabled (FIFO mode).													
0	The FIFOs are disabled (Character mode). The FIFOs become 1-byte-deep holding registers.													

Bit/Field	Name	Type	Reset	Description
3	STP2	R/W	0	UART Two Stop Bits Select  Value Description 1 Two stop bits are transmitted at the end of a frame. The receive logic does not check for two stop bits being received.  When in 7816 smartcard mode (the <code>SMART</code> bit is set in the <code>UARTCTL</code> register), the number of stop bits is forced to 2. 0 One stop bit is transmitted at the end of a frame.
2	EPS	R/W	0	UART Even Parity Select  Value Description 1 Even parity generation and checking is performed during transmission and reception, which checks for an even number of 1s in data and parity bits. 0 Odd parity is performed, which checks for an odd number of 1s.  This bit has no effect when parity is disabled by the <code>PEN</code> bit.
1	PEN	R/W	0	UART Parity Enable  Value Description 1 Parity checking and generation is enabled. 0 Parity is disabled and no parity bit is added to the data frame.
0	BRK	R/W	0	UART Send Break  Value Description 1 A Low level is continually output on the <code>UnTx</code> signal, after completing transmission of the current character. For the proper execution of the break command, software must set this bit for at least two frames (character periods). 0 Normal use.

### Register 8: UART Control (UARTCTL), offset 0x030

The **UARTCTL** register is the control register. All the bits are cleared on reset except for the Transmit Enable (**TXE**) and Receive Enable (**RXE**) bits, which are set.

To enable the UART module, the **UARTEN** bit must be set. If software requires a configuration change in the module, the **UARTEN** bit must be cleared before the configuration changes are written. If the UART is disabled during a transmit or receive operation, the current transaction is completed prior to the UART stopping.

Note that bits [15:14,11:10] are only implemented on UART1. These bits are reserved on UART0 and UART2.

**Note:** The **UARTCTL** register should not be changed while the UART is enabled or else the results are unpredictable. The following sequence is recommended for making changes to the **UARTCTL** register.

1. Disable the UART.
2. Wait for the end of transmission or reception of the current character.
3. Flush the transmit FIFO by clearing bit 4 (**FEN**) in the line control register (**UARTLCRH**).
4. Reprogram the control register.
5. Enable the UART.

#### UART Control (UARTCTL)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x030  
 Type R/W, reset 0x0000.0300

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CTSEN	RTSEN	reserved	RTS	DTR	RXE	TXE	LBE	LIN	HSE	EOT	SMART	SIRLP	SIREN	UARTEN	
Type	R/W	R/W	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Bit/Field	Name	Type	Reset	Description
15	CTSEN	R/W	0	<p>Enable Clear To Send</p> <p>Value Description</p> <p>1 CTS hardware flow control is enabled. Data is only transmitted when the U1CTS signal is asserted.</p> <p>0 CTS hardware flow control is disabled.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
14	RTSEN	R/W	0	<p>Enable Request to Send</p> <p>Value Description</p> <p>1 RTS hardware flow control is enabled. Data is only requested (by asserting U1RTS) when the receive FIFO has available entries.</p> <p>0 RTS hardware flow control is disabled.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
13:12	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	RTS	R/W	0	<p>Request to Send</p> <p>When RTSEN is clear, the status of this bit is reflected on the U1RTS signal. If RTSEN is set, this bit is ignored on a write and should be ignored on read.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
10	DTR	R/W	0	<p>Data Terminal Ready</p> <p>This bit sets the state of the U1DTR output.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
9	RXE	R/W	1	<p>UART Receive Enable</p> <p>Value Description</p> <p>1 The receive section of the UART is enabled.</p> <p>0 The receive section of the UART is disabled.</p> <p>If the UART is disabled in the middle of a receive, it completes the current character before stopping.</p> <p><b>Note:</b> To enable reception, the UARTEN bit must also be set.</p>

Bit/Field	Name	Type	Reset	Description
8	TXE	R/W	1	<p>UART Transmit Enable</p> <p>Value Description</p> <p>1 The transmit section of the UART is enabled.</p> <p>0 The transmit section of the UART is disabled.</p> <p>If the UART is disabled in the middle of a transmission, it completes the current character before stopping.</p> <p><b>Note:</b> To enable transmission, the <code>UARTEN</code> bit must also be set.</p>
7	LBE	R/W	0	<p>UART Loop Back Enable</p> <p>Value Description</p> <p>1 The <code>UnTx</code> path is fed through the <code>UnRx</code> path.</p> <p>0 Normal operation.</p>
6	LIN	R/W	0	<p>LIN Mode Enable</p> <p>Value Description</p> <p>1 The UART operates in LIN mode.</p> <p>0 Normal operation.</p>
5	HSE	R/W	0	<p>High-Speed Enable</p> <p>Value Description</p> <p>1 The UART is clocked using the system clock divided by 16.</p> <p>0 The UART is clocked using the system clock divided by 8.</p> <p><b>Note:</b> System clock used is also dependent on the baud-rate divisor configuration (see page 570) and page 571).</p>
4	EOT	R/W	0	<p>End of Transmission</p> <p>This bit determines the behavior of the <code>TXRIS</code> bit in the <code>UARTRIS</code> register.</p> <p>Value Description</p> <p>1 The <code>TXRIS</code> bit is set only once all transmitted data, including stop bits, have cleared the serializer.</p> <p>0 The <code>TXRIS</code> bit is set when the transmit FIFO condition specified in <code>UARTIFLS</code> is met.</p>



Bit/Field	Name	Type	Reset	Description
3	SMART	R/W	0	<p>ISO 7816 Smart Card Support</p> <p>Value Description</p> <p>1 The UART operates in Smart Card mode.</p> <p>0 Normal operation.</p> <p>The application must ensure that it sets 8-bit word length (<i>WLEN</i> set to 0x3) and even parity (<i>PEN</i> set to 1, <i>EPS</i> set to 1, <i>SPS</i> set to 0) in <b>UARTLCRH</b> when using ISO 7816 mode.</p> <p>In this mode, the value of the <i>STP2</i> bit in <b>UARTLCRH</b> is ignored and the number of stop bits is forced to 2. Note that the UART does not support automatic retransmission on parity errors. If a parity error is detected on transmission, all further transmit operations are aborted and software must handle retransmission of the affected byte or message.</p>
2	SIRLP	R/W	0	<p>UART SIR Low-Power Mode</p> <p>This bit selects the IrDA encoding mode.</p> <p>Value Description</p> <p>1 The UART operates in SIR Low-Power mode. Low-level bits are transmitted with a pulse width which is 3 times the period of the <i>IrLPAud16</i> input signal, regardless of the selected bit rate.</p> <p>0 Low-level bits are transmitted as an active High pulse with a width of 3/16th of the bit period.</p> <p>Setting this bit uses less power, but might reduce transmission distances. See page 569 for more information.</p>
1	SIREN	R/W	0	<p>UART SIR Enable</p> <p>Value Description</p> <p>1 The IrDA SIR block is enabled, and the UART will transmit and receive data using SIR protocol.</p> <p>0 Normal operation.</p>
0	UARTEN	R/W	0	<p>UART Enable</p> <p>Value Description</p> <p>1 The UART is enabled.</p> <p>0 The UART is disabled.</p> <p>If the UART is disabled in the middle of transmission or reception, it completes the current character before stopping.</p>

### Register 9: UART Interrupt FIFO Level Select (UARTIFLS), offset 0x034

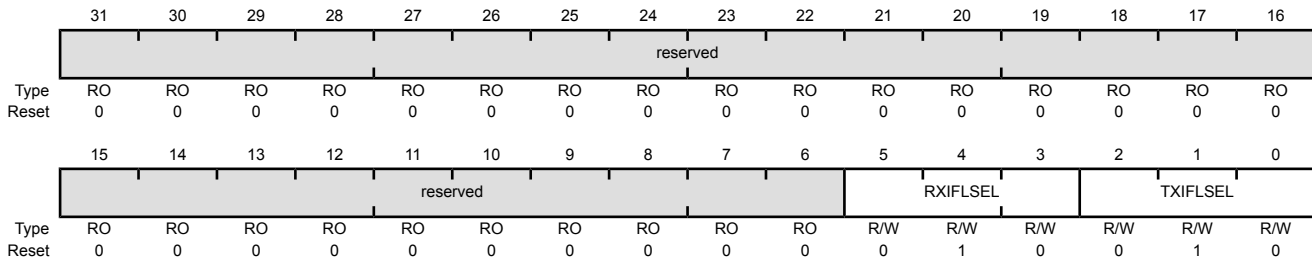
The **UARTIFLS** register is the interrupt FIFO level select register. You can use this register to define the FIFO level at which the **TXRIS** and **RXRIS** bits in the **UARTRIS** register are triggered.

The interrupts are generated based on a transition through a level rather than being based on the level. That is, the interrupts are generated when the fill level progresses through the trigger level. For example, if the receive trigger level is set to the half-way mark, the interrupt is triggered as the module is receiving the 9th character.

Out of reset, the **TXIFLSEL** and **RXIFLSEL** bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

#### UART Interrupt FIFO Level Select (UARTIFLS)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x034  
 Type R/W, reset 0x0000.0012



Bit/Field	Name	Type	Reset	Description
31:6	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5:3	RXIFLSEL	R/W	0x2	UART Receive Interrupt FIFO Level Select

The trigger points for the receive interrupt are as follows:

Value	Description
0x0	RX FIFO $\geq \frac{1}{8}$ full
0x1	RX FIFO $\geq \frac{1}{4}$ full
0x2	RX FIFO $\geq \frac{1}{2}$ full (default)
0x3	RX FIFO $\geq \frac{3}{4}$ full
0x4	RX FIFO $\geq \frac{7}{8}$ full
0x5-0x7	Reserved

Bit/Field	Name	Type	Reset	Description
2:0	TXIFLSEL	R/W	0x2	UART Transmit Interrupt FIFO Level Select The trigger points for the transmit interrupt are as follows:  Value    Description 0x0    TX FIFO $\leq$ $\frac{1}{8}$ full 0x1    TX FIFO $\leq$ $\frac{1}{4}$ full 0x2    TX FIFO $\leq$ $\frac{1}{2}$ full (default) 0x3    TX FIFO $\leq$ $\frac{3}{4}$ full 0x4    TX FIFO $\leq$ $\frac{7}{8}$ full 0x5-0x7 Reserved  <b>Note:</b> If the EOT bit in <b>UARTCTL</b> is set (see page 574), the transmit interrupt is generated once the FIFO is completely empty and all data including stop bits have left the transmit serializer. In this case, the setting of TXIFLSEL is ignored.

### Register 10: UART Interrupt Mask (UARTIM), offset 0x038

The **UARTIM** register is the interrupt mask set/clear register.

On a read, this register gives the current value of the mask on the relevant interrupt. Setting a bit allows the corresponding raw interrupt signal to be routed to the interrupt controller. Clearing a bit prevents the raw interrupt signal from being sent to the interrupt controller.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

#### UART Interrupt Mask (UARTIM)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x038  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LME5IM	LME1IM	LMSBIM	reserved	reserved	OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSRIM	DCDIM	CTSIM	RIIM
Type	R/W	R/W	R/W	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15	LME5IM	R/W	0	LIN Mode Edge 5 Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the LME5RIS bit in the <b>UARTRIS</b> register is set. 0 The LME5RIS interrupt is suppressed and not sent to the interrupt controller.
14	LME1IM	R/W	0	LIN Mode Edge 1 Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the LME1RIS bit in the <b>UARTRIS</b> register is set. 0 The LME1RIS interrupt is suppressed and not sent to the interrupt controller.
13	LMSBIM	R/W	0	LIN Mode Sync Break Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the LMSBRIS bit in the <b>UARTRIS</b> register is set. 0 The LMSBRIS interrupt is suppressed and not sent to the interrupt controller.

Bit/Field	Name	Type	Reset	Description
12:11	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
10	OEIM	R/W	0	UART Overrun Error Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <code>OERIS</code> bit in the <b>UARTRIS</b> register is set. 0 The <code>OERIS</code> interrupt is suppressed and not sent to the interrupt controller.
9	BEIM	R/W	0	UART Break Error Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <code>BERIS</code> bit in the <b>UARTRIS</b> register is set. 0 The <code>BERIS</code> interrupt is suppressed and not sent to the interrupt controller.
8	PEIM	R/W	0	UART Parity Error Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <code>PERIS</code> bit in the <b>UARTRIS</b> register is set. 0 The <code>PERIS</code> interrupt is suppressed and not sent to the interrupt controller.
7	FEIM	R/W	0	UART Framing Error Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <code>FERIS</code> bit in the <b>UARTRIS</b> register is set. 0 The <code>FERIS</code> interrupt is suppressed and not sent to the interrupt controller.
6	RTIM	R/W	0	UART Receive Time-Out Interrupt Mask  Value Description 1 An interrupt is sent to the interrupt controller when the <code>RTRIS</code> bit in the <b>UARTRIS</b> register is set. 0 The <code>RTRIS</code> interrupt is suppressed and not sent to the interrupt controller.

Bit/Field	Name	Type	Reset	Description
5	TXIM	R/W	0	<p>UART Transmit Interrupt Mask</p> <p>Value Description</p> <p>1 An interrupt is sent to the interrupt controller when the TXRIS bit in the <b>UARTRIS</b> register is set.</p> <p>0 The TXRIS interrupt is suppressed and not sent to the interrupt controller.</p>
4	RXIM	R/W	0	<p>UART Receive Interrupt Mask</p> <p>Value Description</p> <p>1 An interrupt is sent to the interrupt controller when the RXRIS bit in the <b>UARTRIS</b> register is set.</p> <p>0 The RXRIS interrupt is suppressed and not sent to the interrupt controller.</p>
3	DSRIM	R/W	0	<p>UART Data Set Ready Modem Interrupt Mask</p> <p>Value Description</p> <p>1 An interrupt is sent to the interrupt controller when the DSRIS bit in the <b>UARTRIS</b> register is set.</p> <p>0 The DSRIS interrupt is suppressed and not sent to the interrupt controller.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
2	DCDIM	R/W	0	<p>UART Data Carrier Detect Modem Interrupt Mask</p> <p>Value Description</p> <p>1 An interrupt is sent to the interrupt controller when the DCDRIS bit in the <b>UARTRIS</b> register is set.</p> <p>0 The DCDRIS interrupt is suppressed and not sent to the interrupt controller.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
1	CTSIM	R/W	0	<p>UART Clear to Send Modem Interrupt Mask</p> <p>Value Description</p> <p>1 An interrupt is sent to the interrupt controller when the CTSRIS bit in the <b>UARTRIS</b> register is set.</p> <p>0 The CTSRIS interrupt is suppressed and not sent to the interrupt controller.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>

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Bit/Field	Name	Type	Reset	Description
0	RIM	R/W	0	UART Ring Indicator Modem Interrupt Mask
				Value Description
			1	An interrupt is sent to the interrupt controller when the <code>RIRIS</code> bit in the <b>UARTRIS</b> register is set.
			0	The <code>RIRIS</code> interrupt is suppressed and not sent to the interrupt controller.
				This bit is implemented only on UART1 and is reserved for UART0 and UART2.

### Register 11: UART Raw Interrupt Status (UARTRIS), offset 0x03C

The **UARTRIS** register is the raw interrupt status register. On a read, this register gives the current raw status value of the corresponding interrupt. A write has no effect.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

#### UART Raw Interrupt Status (UARTRIS)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x03C  
 Type RO, reset 0x0000.000F

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LME5RIS	LME1RIS	LMSBRIS	reserved	OERIS	BERIS	PERIS	FERIS	RTRIS	TXRIS	RXRIS	DSRRIS	DCDRIS	CTSRIS	RIRIS	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15	LME5RIS	RO	0	LIN Mode Edge 5 Raw Interrupt Status  Value Description 1 The timer value at the 5th falling edge of the LIN Sync Field has been captured. 0 No interrupt  This bit is cleared by writing a 1 to the LME5IC bit in the <b>UARTICR</b> register.
14	LME1RIS	RO	0	LIN Mode Edge 1 Raw Interrupt Status  Value Description 1 The timer value at the 1st falling edge of the LIN Sync Field has been captured. 0 No interrupt  This bit is cleared by writing a 1 to the LME1IC bit in the <b>UARTICR</b> register.
13	LMSBRIS	RO	0	LIN Mode Sync Break Raw Interrupt Status  Value Description 1 A LIN Sync Break has been detected. 0 No interrupt  This bit is cleared by writing a 1 to the LMSBIC bit in the <b>UARTICR</b> register.



Bit/Field	Name	Type	Reset	Description
12:11	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
10	OERIS	RO	0	<p>UART Overrun Error Raw Interrupt Status</p> <p>Value Description</p> <p>1 An overrun error has occurred.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the OEIC bit in the <b>UARTICR</b> register.</p>
9	BERIS	RO	0	<p>UART Break Error Raw Interrupt Status</p> <p>Value Description</p> <p>1 A break error has occurred.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the BEIC bit in the <b>UARTICR</b> register.</p>
8	PERIS	RO	0	<p>UART Parity Error Raw Interrupt Status</p> <p>Value Description</p> <p>1 A parity error has occurred.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the PEIC bit in the <b>UARTICR</b> register.</p>
7	FERIS	RO	0	<p>UART Framing Error Raw Interrupt Status</p> <p>Value Description</p> <p>1 A framing error has occurred.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the FEIC bit in the <b>UARTICR</b> register.</p>
6	RTRIS	RO	0	<p>UART Receive Time-Out Raw Interrupt Status</p> <p>Value Description</p> <p>1 A receive time out has occurred.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the RTIC bit in the <b>UARTICR</b> register.</p>

Bit/Field	Name	Type	Reset	Description
5	TXRIS	RO	0	<p>UART Transmit Raw Interrupt Status</p> <p>Value Description</p> <p>1 If the <b>EOT</b> bit in the <b>UARTCTRL</b> register is clear, the transmit FIFO level has passed through the condition defined in the <b>UARTIFLS</b> register.</p> <p>If the <b>EOT</b> bit is clear, the last bit of all transmitted data and flags has left the serializer.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the <b>TXIC</b> bit in the <b>UARTICR</b> register.</p>
4	RXRIS	RO	0	<p>UART Receive Raw Interrupt Status</p> <p>Value Description</p> <p>1 The receive FIFO level has passed through the condition defined in the <b>UARTIFLS</b> register.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the <b>RXIC</b> bit in the <b>UARTICR</b> register.</p>
3	DSRRIS	RO	0	<p>UART Data Set Ready Modem Raw Interrupt Status</p> <p>Value Description</p> <p>1 Data Set Ready used for software flow control.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the <b>DSRIC</b> bit in the <b>UARTICR</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
2	DCCRIS	RO	0	<p>UART Data Carrier Detect Modem Raw Interrupt Status</p> <p>Value Description</p> <p>1 Data Carrier Detect used for software flow control.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the <b>DCDIC</b> bit in the <b>UARTICR</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
1	CTSRIS	RO	0	<p>UART Clear to Send Modem Raw Interrupt Status</p> <p>Value Description</p> <p>1 Clear to Send used for software flow control.</p> <p>0 No interrupt</p> <p>This bit is cleared by writing a 1 to the <b>CTSIC</b> bit in the <b>UARTICR</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>

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Bit/Field	Name	Type	Reset	Description
0	RIRIS	RO	0	UART Ring Indicator Modem Raw Interrupt Status  Value Description 1 Ring Indicator used for software flow control. 0 No interrupt  This bit is cleared by writing a 1 to the RIIIC bit in the <b>UARTICR</b> register. This bit is implemented only on UART1 and is reserved for UART0 and UART2.

### Register 12: UART Masked Interrupt Status (UARTMIS), offset 0x040

The **UARTMIS** register is the masked interrupt status register. On a read, this register gives the current masked status value of the corresponding interrupt. A write has no effect.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

#### UART Masked Interrupt Status (UARTMIS)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x040  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LME5MIS	LME1MIS	LMSBMIS	reserved	OEMIS	BEMIS	PEMIS	FEMIS	RTMIS	TXMIS	RXMIS	DSRMIS	DCDMIS	CTSMIS	RIMIS	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15	LME5MIS	RO	0	LIN Mode Edge 5 Masked Interrupt Status  Value Description 1 An unmasked interrupt was signaled due to the 5th falling edge of the LIN Sync Field. 0 An interrupt has not occurred or is masked.  This bit is cleared by writing a 1 to the LME5IC bit in the <b>UARTICR</b> register.
14	LME1MIS	RO	0	LIN Mode Edge 1 Masked Interrupt Status  Value Description 1 An unmasked interrupt was signaled due to the 1st falling edge of the LIN Sync Field. 0 An interrupt has not occurred or is masked.  This bit is cleared by writing a 1 to the LME1IC bit in the <b>UARTICR</b> register.
13	LMSBMIS	RO	0	LIN Mode Sync Break Masked Interrupt Status  Value Description 1 An unmasked interrupt was signaled due the receipt of a LIN Sync Break. 0 An interrupt has not occurred or is masked.  This bit is cleared by writing a 1 to the LMSBIC bit in the <b>UARTICR</b> register.

Bit/Field	Name	Type	Reset	Description
12:11	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
10	OEMIS	RO	0	<p>UART Overrun Error Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to an overrun error.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the OEIC bit in the <b>UARTICR</b> register.</p>
9	BEMIS	RO	0	<p>UART Break Error Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to a break error.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the BEIC bit in the <b>UARTICR</b> register.</p>
8	PEMIS	RO	0	<p>UART Parity Error Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to a parity error.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the PEIC bit in the <b>UARTICR</b> register.</p>
7	FEMIS	RO	0	<p>UART Framing Error Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to a framing error.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the FEIC bit in the <b>UARTICR</b> register.</p>
6	RTMIS	RO	0	<p>UART Receive Time-Out Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to a receive time out.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the RTIC bit in the <b>UARTICR</b> register.</p>
5	TXMIS	RO	0	<p>UART Transmit Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to passing through the specified transmit FIFO level (if the EOT bit is clear) or due to the transmission of the last data bit (if the EOT bit is set).</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the TXIC bit in the <b>UARTICR</b> register.</p>

Bit/Field	Name	Type	Reset	Description
4	RXMIS	RO	0	<p>UART Receive Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to passing through the specified receive FIFO level.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>RXIC</code> bit in the <b>UARTICR</b> register.</p>
3	DSRMIS	RO	0	<p>UART Data Set Ready Modem Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to Data Set Ready.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>DSRIC</code> bit in the <b>UARTICR</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
2	DCDMIS	RO	0	<p>UART Data Carrier Detect Modem Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to Data Carrier Detect.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>DCDIC</code> bit in the <b>UARTICR</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
1	CTSMIS	RO	0	<p>UART Clear to Send Modem Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to Clear to Send.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>CTSIC</code> bit in the <b>UARTICR</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
0	RIMIS	RO	0	<p>UART Ring Indicator Modem Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked interrupt was signaled due to Ring Indicator.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the <code>RIIC</code> bit in the <b>UARTICR</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>

## Register 13: UART Interrupt Clear (UARTICR), offset 0x044

The **UARTICR** register is the interrupt clear register. On a write of 1, the corresponding interrupt (both raw interrupt and masked interrupt, if enabled) is cleared. A write of 0 has no effect.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

### UART Interrupt Clear (UARTICR)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x044  
 Type W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LME5MIC	LME1MIC	LMSBMIC	reserved	OEIC	BEIC	PEIC	FEIC	RTIC	TXIC	RXIC	DSRMIC	DCDMIC	CTSMIC	RIMIC	
Type	W1C	W1C	W1C	RO	RO	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15	LME5MIC	W1C	0	LIN Mode Edge 5 Interrupt Clear  Writing a 1 to this bit clears the <b>LME5RIS</b> bit in the <b>UARTRIS</b> register and the <b>LME5MIS</b> bit in the <b>UARTMIS</b> register.
14	LME1MIC	W1C	0	LIN Mode Edge 1 Interrupt Clear  Writing a 1 to this bit clears the <b>LME1RIS</b> bit in the <b>UARTRIS</b> register and the <b>LME1MIS</b> bit in the <b>UARTMIS</b> register.
13	LMSBMIC	W1C	0	LIN Mode Sync Break Interrupt Clear  Writing a 1 to this bit clears the <b>LMSBRIS</b> bit in the <b>UARTRIS</b> register and the <b>LMSBMIS</b> bit in the <b>UARTMIS</b> register.
12:11	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
10	OEIC	W1C	0	Overrun Error Interrupt Clear  Writing a 1 to this bit clears the <b>OERIS</b> bit in the <b>UARTRIS</b> register and the <b>OEMIS</b> bit in the <b>UARTMIS</b> register.
9	BEIC	W1C	0	Break Error Interrupt Clear  Writing a 1 to this bit clears the <b>BERIS</b> bit in the <b>UARTRIS</b> register and the <b>BEMIS</b> bit in the <b>UARTMIS</b> register.
8	PEIC	W1C	0	Parity Error Interrupt Clear  Writing a 1 to this bit clears the <b>PERIS</b> bit in the <b>UARTRIS</b> register and the <b>PEMIS</b> bit in the <b>UARTMIS</b> register.

Bit/Field	Name	Type	Reset	Description
7	FEIC	W1C	0	<p>Framing Error Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>FERIS</code> bit in the <b>UARTRIS</b> register and the <code>FEMIS</code> bit in the <b>UARTMIS</b> register.</p>
6	RTIC	W1C	0	<p>Receive Time-Out Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>RTRIS</code> bit in the <b>UARTRIS</b> register and the <code>RTMIS</code> bit in the <b>UARTMIS</b> register.</p>
5	TXIC	W1C	0	<p>Transmit Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>TXRIS</code> bit in the <b>UARTRIS</b> register and the <code>TXMIS</code> bit in the <b>UARTMIS</b> register.</p>
4	RXIC	W1C	0	<p>Receive Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>RXRIS</code> bit in the <b>UARTRIS</b> register and the <code>RXMIS</code> bit in the <b>UARTMIS</b> register.</p>
3	DSRMIC	W1C	0	<p>UART Data Set Ready Modem Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>DSRRIS</code> bit in the <b>UARTRIS</b> register and the <code>DSRMIS</code> bit in the <b>UARTMIS</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
2	DCDMIC	W1C	0	<p>UART Data Carrier Detect Modem Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>DCDRIS</code> bit in the <b>UARTRIS</b> register and the <code>DCDMIS</code> bit in the <b>UARTMIS</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
1	CTSMIC	W1C	0	<p>UART Clear to Send Modem Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>CTSRIS</code> bit in the <b>UARTRIS</b> register and the <code>CTSMIS</code> bit in the <b>UARTMIS</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>
0	RIMIC	W1C	0	<p>UART Ring Indicator Modem Interrupt Clear</p> <p>Writing a 1 to this bit clears the <code>RIRIS</code> bit in the <b>UARTRIS</b> register and the <code>RIMIS</code> bit in the <b>UARTMIS</b> register.</p> <p>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</p>



**Register 14: UART DMA Control (UARTDMACTL), offset 0x048**

The **UARTDMACTL** register is the DMA control register.

**UART DMA Control (UARTDMACTL)**

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x048  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													DMAERR	TXDMAE	RXDMAE
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

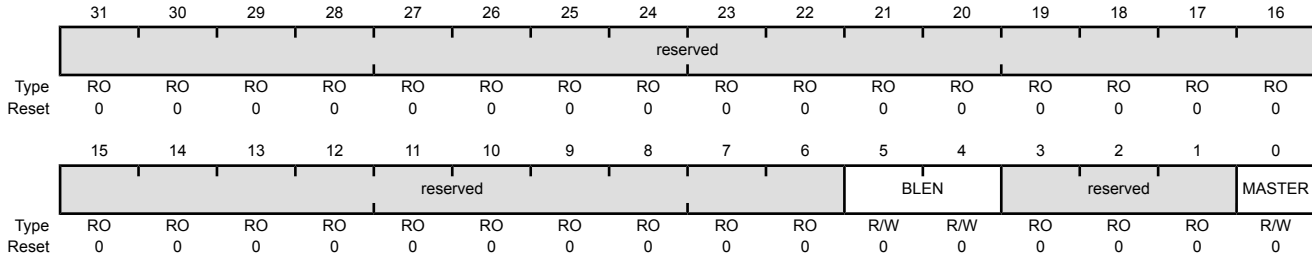
Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x00000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	DMAERR	R/W	0	DMA on Error  Value Description 1     μDMA receive requests are automatically disabled when a receive error occurs. 0     μDMA receive requests are unaffected when a receive error occurs.
1	TXDMAE	R/W	0	Transmit DMA Enable  Value Description 1     μDMA for the transmit FIFO is enabled. 0     μDMA for the transmit FIFO is disabled.
0	RXDMAE	R/W	0	Receive DMA Enable  Value Description 1     μDMA for the receive FIFO is enabled. 0     μDMA for the receive FIFO is disabled.

### Register 15: UART LIN Control (UARTLCTL), offset 0x090

The **UARTLCTL** register is the configures the operation of the UART when in LIN mode.

#### UART LIN Control (UARTLCTL)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x090  
 Type R/W, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:6	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5:4	BLEN	R/W	0x0	Sync Break Length  Value Description 0x3 Sync break length is 16T bits 0x2 Sync break length is 15T bits 0x1 Sync break length is 14T bits 0x0 Sync break length is 13T bits (default)
3:1	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	MASTER	R/W	0	LIN Master Enable  Value Description 1 The UART operates as a LIN master. 0 The UART operates as a LIN slave.

## Register 16: UART LIN Snap Shot (UARTLSS), offset 0x094

The **UARTLSS** register captures the free-running timer value when either the Sync Edge 1 or the Sync Edge 5 is detected in LIN mode.

### UART LIN Snap Shot (UARTLSS)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x094  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSS															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

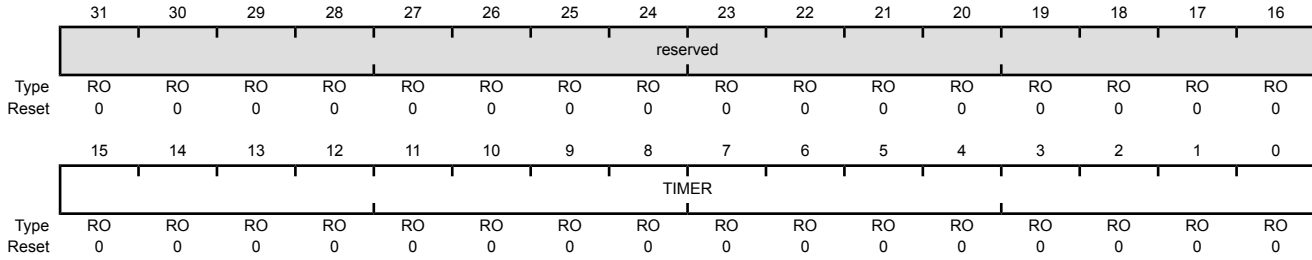
Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	TSS	RO	0x0000	Timer Snap Shot  This field contains the value of the free-running timer when either the Sync Edge 5 or the Sync Edge 1 was detected.

### Register 17: UART LIN Timer (UARTLTIM), offset 0x098

The **UARTLTIM** register contains the current timer value for the free-running timer that is used to calculate the baud rate when in LIN slave mode. The value in this register is used along with the value in the **UART LIN Snap Shot (UARTLSS)** register to adjust the baud rate to match that of the master.

#### UART LIN Timer (UARTLTIM)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0x098  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	TIMER	RO	0x0000	Timer Value This field contains the value of the free-running timer.

**Register 18: UART Peripheral Identification 4 (UARTPeriphID4), offset 0xFD0**

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

## UART Peripheral Identification 4 (UARTPeriphID4)

UART0 base: 0x4000.C000

UART1 base: 0x4000.D000

UART2 base: 0x4000.E000

Offset 0xFD0

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID4							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

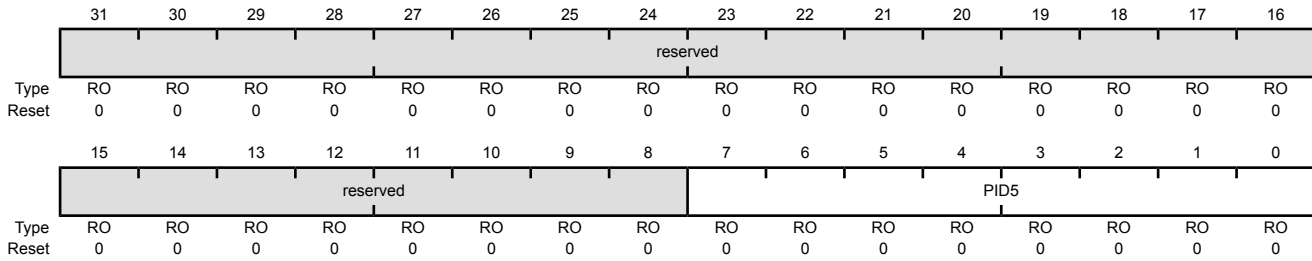
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID4	RO	0x00	UART Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.

### Register 19: UART Peripheral Identification 5 (UARTPeriphID5), offset 0xFD4

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

#### UART Peripheral Identification 5 (UARTPeriphID5)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFD4  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID5	RO	0x00	UART Peripheral ID Register [15:8]  Can be used by software to identify the presence of this peripheral.

**Register 20: UART Peripheral Identification 6 (UARTPeriphID6), offset 0xFD8**

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

## UART Peripheral Identification 6 (UARTPeriphID6)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFD8  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID6							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

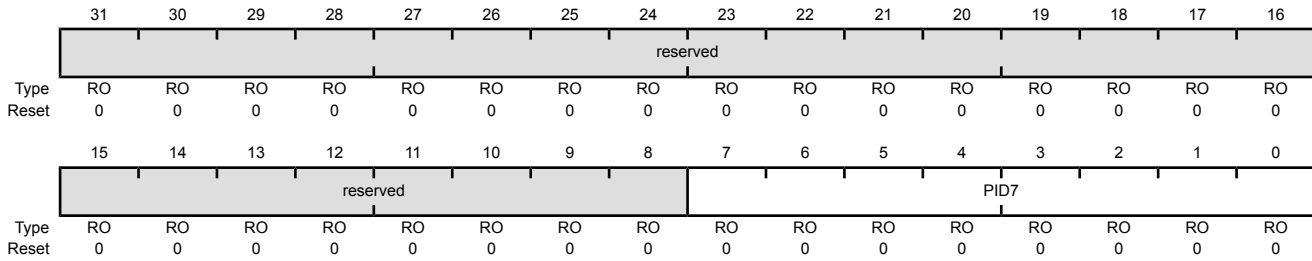
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID6	RO	0x00	UART Peripheral ID Register [23:16]  Can be used by software to identify the presence of this peripheral.

### Register 21: UART Peripheral Identification 7 (UARTPeriphID7), offset 0xFDC

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

#### UART Peripheral Identification 7 (UARTPeriphID7)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFDC  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID7	RO	0x00	UART Peripheral ID Register [31:24]  Can be used by software to identify the presence of this peripheral.



**Register 22: UART Peripheral Identification 0 (UARTPeriphID0), offset 0xFE0**

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

## UART Peripheral Identification 0 (UARTPeriphID0)

UART0 base: 0x4000.C000

UART1 base: 0x4000.D000

UART2 base: 0x4000.E000

Offset 0xFE0

Type RO, reset 0x0000.0060

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID0							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

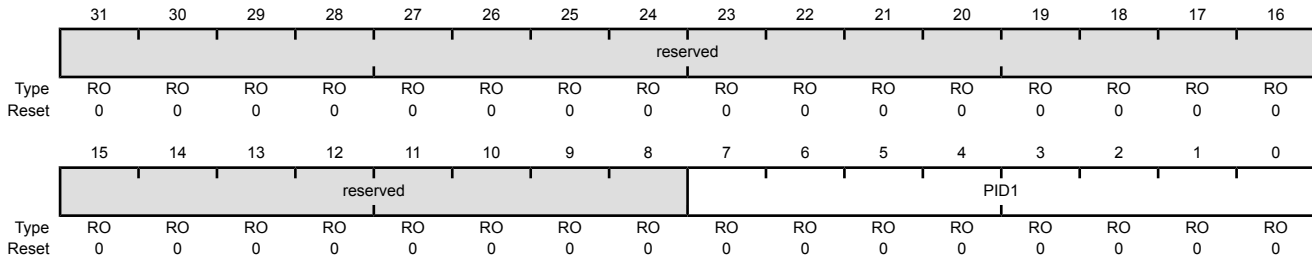
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID0	RO	0x60	UART Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.

### Register 23: UART Peripheral Identification 1 (UARTPeriphID1), offset 0xFE4

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

#### UART Peripheral Identification 1 (UARTPeriphID1)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFE4  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID1	RO	0x00	UART Peripheral ID Register [15:8]  Can be used by software to identify the presence of this peripheral.

**Register 24: UART Peripheral Identification 2 (UARTPeriphID2), offset 0xFE8**

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

## UART Peripheral Identification 2 (UARTPeriphID2)

UART0 base: 0x4000.C000

UART1 base: 0x4000.D000

UART2 base: 0x4000.E000

Offset 0xFE8

Type RO, reset 0x0000.0018

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID2							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

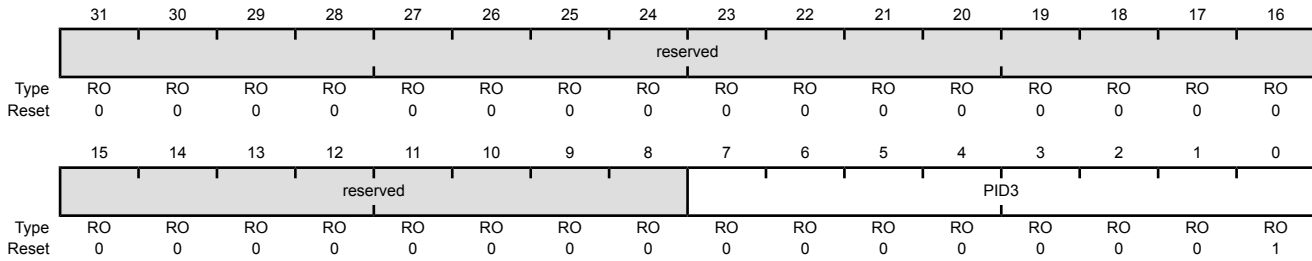
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID2	RO	0x18	UART Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.

### Register 25: UART Peripheral Identification 3 (UARTPeriphID3), offset 0xFEC

The **UARTPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

#### UART Peripheral Identification 3 (UARTPeriphID3)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFEC  
 Type RO, reset 0x0000.0001



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID3	RO	0x01	UART Peripheral ID Register [31:24]  Can be used by software to identify the presence of this peripheral.

**Register 26: UART PrimeCell Identification 0 (UARTPCellID0), offset 0xFF0**

The **UARTPCellIDn** registers are hard-coded and the fields within the registers determine the reset values.

## UART PrimeCell Identification 0 (UARTPCellID0)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFF0  
 Type RO, reset 0x0000.000D

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID0							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

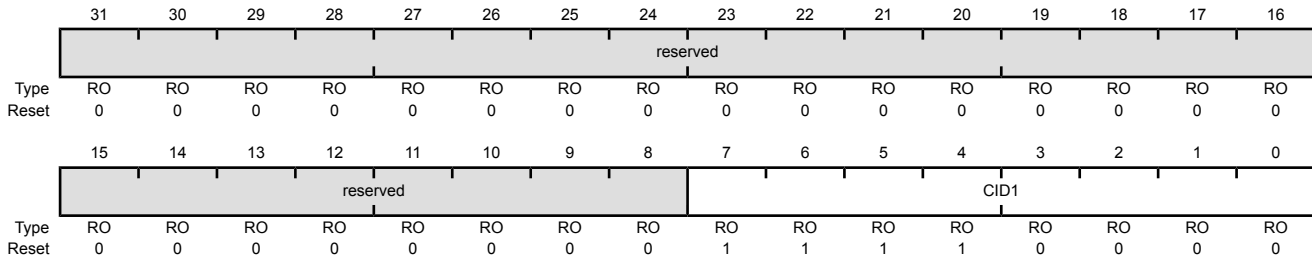
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID0	RO	0x0D	UART PrimeCell ID Register [7:0] Provides software a standard cross-peripheral identification system.

### Register 27: UART PrimeCell Identification 1 (UARTPCellID1), offset 0xFF4

The **UARTPCellIDn** registers are hard-coded and the fields within the registers determine the reset values.

#### UART PrimeCell Identification 1 (UARTPCellID1)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFF4  
 Type RO, reset 0x0000.00F0



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID1	RO	0xF0	UART PrimeCell ID Register [15:8] Provides software a standard cross-peripheral identification system.

**Register 28: UART PrimeCell Identification 2 (UARTPCellID2), offset 0xFF8**

The **UARTPCellIDn** registers are hard-coded and the fields within the registers determine the reset values.

## UART PrimeCell Identification 2 (UARTPCellID2)

UART0 base: 0x4000.C000

UART1 base: 0x4000.D000

UART2 base: 0x4000.E000

Offset 0xFF8

Type RO, reset 0x0000.0005

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID2							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

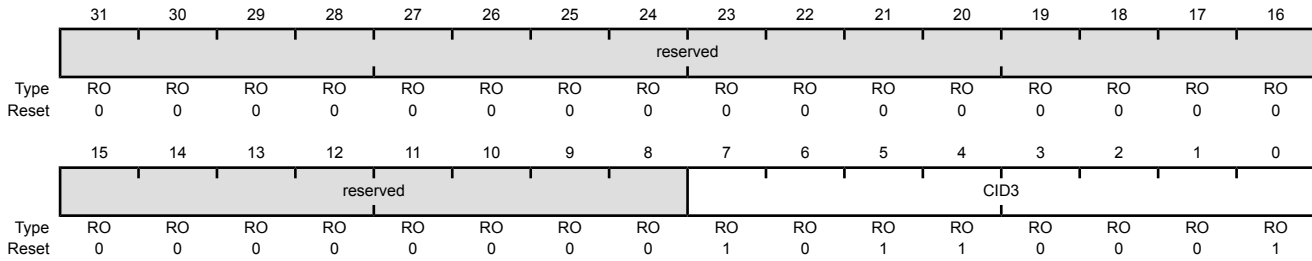
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID2	RO	0x05	UART PrimeCell ID Register [23:16] Provides software a standard cross-peripheral identification system.

### Register 29: UART PrimeCell Identification 3 (UARTPCellID3), offset 0xFFC

The **UARTPCellIDn** registers are hard-coded and the fields within the registers determine the reset values.

#### UART PrimeCell Identification 3 (UARTPCellID3)

UART0 base: 0x4000.C000  
 UART1 base: 0x4000.D000  
 UART2 base: 0x4000.E000  
 Offset 0xFFC  
 Type RO, reset 0x0000.00B1



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID3	RO	0xB1	UART PrimeCell ID Register [31:24] Provides software a standard cross-peripheral identification system.



## 16 Synchronous Serial Interface (SSI)

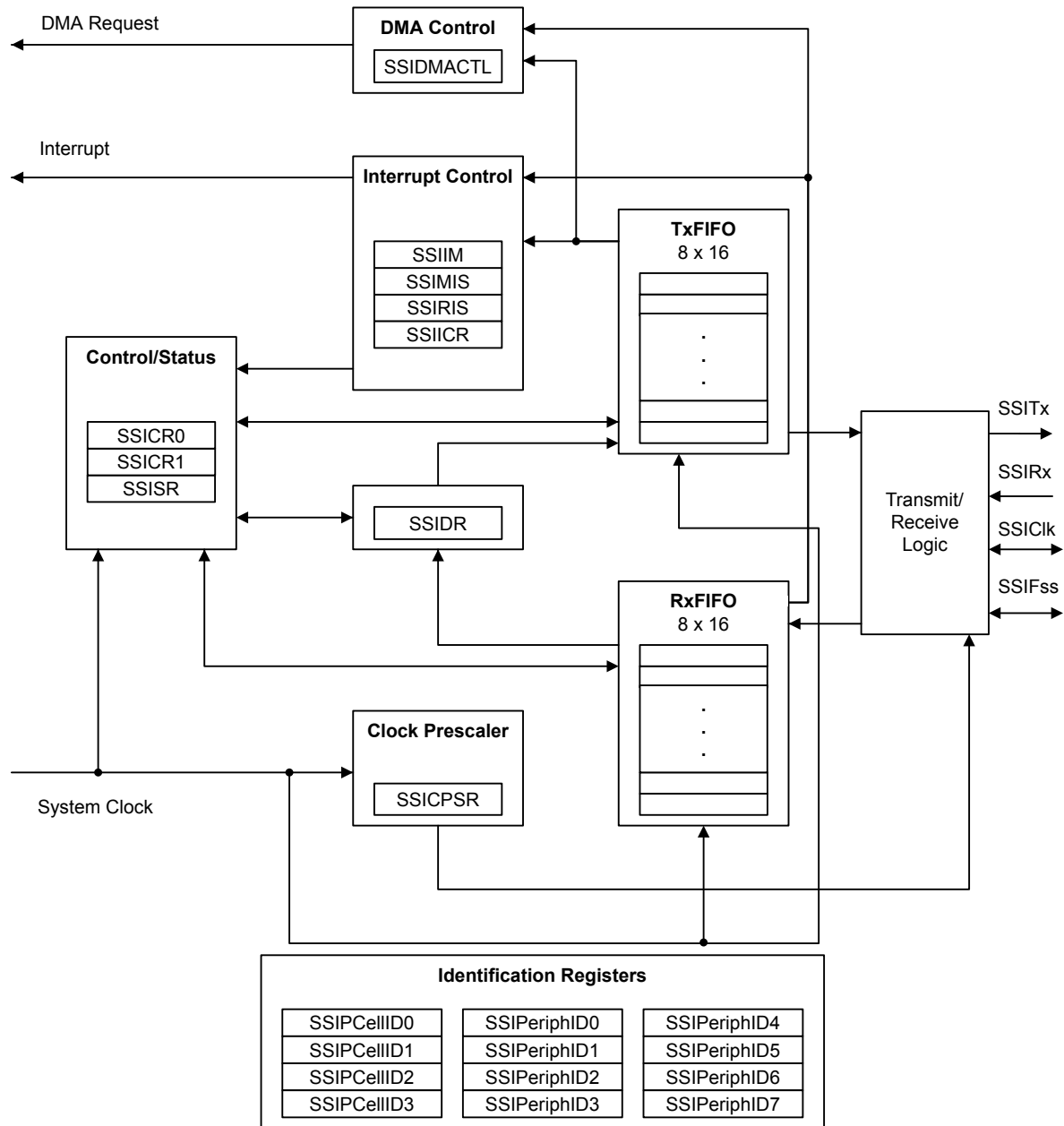
The Stellaris® microcontroller includes two Synchronous Serial Interface (SSI) modules. Each SSI is a master or slave interface for synchronous serial communication with peripheral devices that have either Freescale SPI, MICROWIRE, or Texas Instruments synchronous serial interfaces.

The Stellaris® LM3S1811 controller includes two SSI modules with the following features:

- Programmable interface operation for Freescale SPI, MICROWIRE, or Texas Instruments synchronous serial interfaces
- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive FIFOs, each 16 bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loopback test mode for diagnostic/debug testing
- Standard FIFO-based interrupts and End-of-Transmission interrupt
- Efficient transfers using Micro Direct Memory Access Controller ( $\mu$ DMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains 4 entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when FIFO contains 4 entries

## 16.1 Block Diagram

Figure 16-1. SSI Module Block Diagram



## 16.2 Signal Description

Table 16-1 on page 611 lists the external signals of the SSI module and describes the function of each. The SSI signals are alternate functions for some GPIO signals and default to be GPIO signals at reset., with the exception of the SSIOClk, SSIOFss, SSIORx, and SSIOTx pins which default to the SSI function. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for the SSI signals. The AFSEL bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) should be set to choose the SSI function. The number in

parentheses is the encoding that must be programmed into the `PMCn` field in the **GPIO Port Control (GPIOPCTL)** register (page 328) to assign the SSI signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 288.

**Table 16-1. Signals for SSI**

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
SSI0Clk	28	PA2 (1)	I/O	TTL	SSI module 0 clock.
SSI0Fss	29	PA3 (1)	I/O	TTL	SSI module 0 frame.
SSI0Rx	30	PA4 (1)	I	TTL	SSI module 0 receive.
SSI0Tx	31	PA5 (1)	O	TTL	SSI module 0 transmit.
SSI1Clk	60 74 76	PF2 (9) PE0 (2) PH4 (11)	I/O	TTL	SSI module 1 clock.
SSI1Fss	59 63 75	PF3 (9) PH5 (11) PE1 (2)	I/O	TTL	SSI module 1 frame.
SSI1Rx	58 62 95	PF4 (9) PH6 (11) PE2 (2)	I	TTL	SSI module 1 receive.
SSI1Tx	15 46 96	PH7 (11) PF5 (9) PE3 (2)	O	TTL	SSI module 1 transmit.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 16.3 Functional Description

The SSI performs serial-to-parallel conversion on data received from a peripheral device. The CPU accesses data, control, and status information. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. The SSI also supports the  $\mu$ DMA interface. The transmit and receive FIFOs can be programmed as destination/source addresses in the  $\mu$ DMA module.  $\mu$ DMA operation is enabled by setting the appropriate bit(s) in the **SSIDMACTL** register (see page 638).

### 16.3.1 Bit Rate Generation

The SSI includes a programmable bit rate clock divider and prescaler to generate the serial output clock. Bit rates are supported to 2 MHz and higher, although maximum bit rate is determined by peripheral devices.

The serial bit rate is derived by dividing down the input clock (SysClk). The clock is first divided by an even prescale value `CPSDVSR` from 2 to 254, which is programmed in the **SSI Clock Prescale (SSICPSR)** register (see page 631). The clock is further divided by a value from 1 to 256, which is  $1 + SCR$ , where `SCR` is the value programmed in the **SSI Control 0 (SSICR0)** register (see page 624).

The frequency of the output clock `SSIClk` is defined by:

$$SSIClk = SysClk / (CPSDVSR * (1 + SCR))$$

**Note:** For master mode, the system clock must be at least two times faster than the `SSIClk`. For slave mode, the system clock must be at least 12 times faster than the `SSIClk`.

See “Synchronous Serial Interface (SSI)” on page 743 to view SSI timing parameters.

## 16.3.2 FIFO Operation

### 16.3.2.1 Transmit FIFO

The common transmit FIFO is a 16-bit wide, 8-locations deep, first-in, first-out memory buffer. The CPU writes data to the FIFO by writing the **SSI Data (SSIDR)** register (see page 628), and data is stored in the FIFO until it is read out by the transmission logic.

When configured as a master or a slave, parallel data is written into the transmit FIFO prior to serial conversion and transmission to the attached slave or master, respectively, through the **SSITx** pin.

In slave mode, the SSI transmits data each time the master initiates a transaction. If the transmit FIFO is empty and the master initiates, the slave transmits the 8th most recent value in the transmit FIFO. If less than 8 values have been written to the transmit FIFO since the SSI module clock was enabled using the **SSI** bit in the **RGCG1** register, then 0 is transmitted. Care should be taken to ensure that valid data is in the FIFO as needed. The SSI can be configured to generate an interrupt or a  $\mu$ DMA request when the FIFO is empty.

### 16.3.2.2 Receive FIFO

The common receive FIFO is a 16-bit wide, 8-locations deep, first-in, first-out memory buffer. Received data from the serial interface is stored in the buffer until read out by the CPU, which accesses the read FIFO by reading the **SSIDR** register.

When configured as a master or slave, serial data received through the **SSIRx** pin is registered prior to parallel loading into the attached slave or master receive FIFO, respectively.

## 16.3.3 Interrupts

The SSI can generate interrupts when the following conditions are observed:

- Transmit FIFO service (when the transmit FIFO is half full or less)
- Receive FIFO service (when the receive FIFO is half full or more)
- Receive FIFO time-out
- Receive FIFO overrun
- End of transmission

All of the interrupt events are ORed together before being sent to the interrupt controller, so the SSI generates a single interrupt request to the controller regardless of the number of active interrupts. Each of the four individual maskable interrupts can be masked by clearing the appropriate bit in the **SSI Interrupt Mask (SSIIM)** register (see page 632). Setting the appropriate mask bit enables the interrupt.

The individual outputs, along with a combined interrupt output, allow use of either a global interrupt service routine or modular device drivers to handle interrupts. The transmit and receive dynamic dataflow interrupts have been separated from the status interrupts so that data can be read or written in response to the FIFO trigger levels. The status of the individual interrupt sources can be read from the **SSI Raw Interrupt Status (SSIRIS)** and **SSI Masked Interrupt Status (SSIMIS)** registers (see page 633 and page 635, respectively).

The receive FIFO has a time-out period that is 32 periods at the rate of **SSIClk** (whether or not **SSIClk** is currently active) and is started when the RX FIFO goes from EMPTY to not-EMPTY. If the RX FIFO is emptied before 32 clocks have passed, the time-out period is reset. As a result, the

ISR should clear the Receive FIFO Time-out Interrupt just after reading out the RX FIFO by writing a 1 to the `RTIC` bit in the **SSI Interrupt Clear (SSIICR)** register. The interrupt should not be cleared so late that the ISR returns before the interrupt is actually cleared, or the ISR may be re-activated unnecessarily.

The End-of-Transmission (EOT) interrupt indicates that the data has been transmitted completely. This interrupt can be used to indicate when it is safe to turn off the SSI module clock or enter sleep mode. In addition, because transmitted data and received data complete at exactly the same time, the interrupt can also indicate that read data is ready immediately, without waiting for the receive FIFO time-out period to complete.

### 16.3.4 Frame Formats

Each data frame is between 4 and 16 bits long, depending on the size of data programmed, and is transmitted starting with the MSB. There are three basic frame types that can be selected:

- Texas Instruments synchronous serial
- Freescale SPI
- MICROWIRE

For all three formats, the serial clock (`SSIClk`) is held inactive while the SSI is idle, and `SSIClk` transitions at the programmed frequency only during active transmission or reception of data. The idle state of `SSIClk` is utilized to provide a receive timeout indication that occurs when the receive FIFO still contains data after a timeout period.

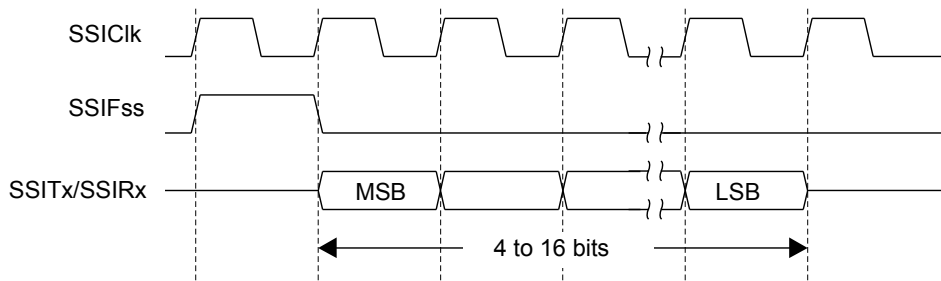
For Freescale SPI and MICROWIRE frame formats, the serial frame (`SSIFSS`) pin is active Low, and is asserted (pulled down) during the entire transmission of the frame.

For Texas Instruments synchronous serial frame format, the `SSIFSS` pin is pulsed for one serial clock period starting at its rising edge, prior to the transmission of each frame. For this frame format, both the SSI and the off-chip slave device drive their output data on the rising edge of `SSIClk` and latch data from the other device on the falling edge.

Unlike the full-duplex transmission of the other two frame formats, the MICROWIRE format uses a special master-slave messaging technique which operates at half-duplex. In this mode, when a frame begins, an 8-bit control message is transmitted to the off-chip slave. During this transmit, no incoming data is received by the SSI. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the requested data. The returned data can be 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

#### 16.3.4.1 Texas Instruments Synchronous Serial Frame Format

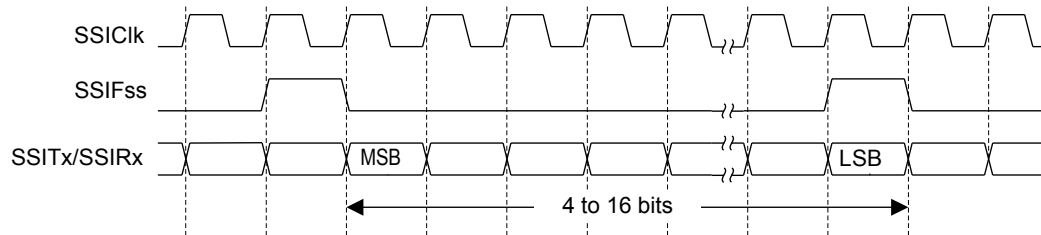
Figure 16-2 on page 614 shows the Texas Instruments synchronous serial frame format for a single transmitted frame.

**Figure 16-2. TI Synchronous Serial Frame Format (Single Transfer)**

In this mode,  $SSIClk$  and  $SSIFss$  are forced Low, and the transmit data line  $SSITx$  is tristated whenever the SSI is idle. Once the bottom entry of the transmit FIFO contains data,  $SSIFss$  is pulsed High for one  $SSIClk$  period. The value to be transmitted is also transferred from the transmit FIFO to the serial shifter of the transmit logic. On the next rising edge of  $SSIClk$ , the MSB of the 4 to 16-bit data frame is shifted out on the  $SSITx$  pin. Likewise, the MSB of the received data is shifted onto the  $SSIRx$  pin by the off-chip serial slave device.

Both the SSI and the off-chip serial slave device then clock each data bit into their serial shifter on each falling edge of  $SSIClk$ . The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of  $SSIClk$  after the LSB has been latched.

Figure 16-3 on page 614 shows the Texas Instruments synchronous serial frame format when back-to-back frames are transmitted.

**Figure 16-3. TI Synchronous Serial Frame Format (Continuous Transfer)**

#### 16.3.4.2 Freescale SPI Frame Format

The Freescale SPI interface is a four-wire interface where the  $SSIFss$  signal behaves as a slave select. The main feature of the Freescale SPI format is that the inactive state and phase of the  $SSIClk$  signal are programmable through the  $SPO$  and  $SPH$  bits in the **SSISCR0** control register.

##### **SPO Clock Polarity Bit**

When the  $SPO$  clock polarity control bit is clear, it produces a steady state Low value on the  $SSIClk$  pin. If the  $SPO$  bit is set, a steady state High value is placed on the  $SSIClk$  pin when data is not being transferred.

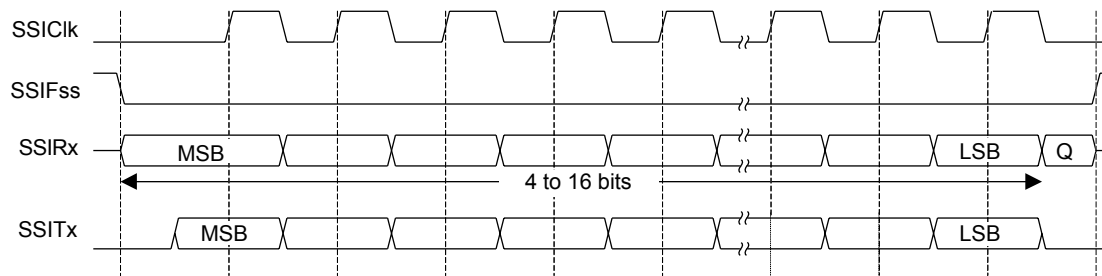
### SPH Phase Control Bit

The *SPH* phase control bit selects the clock edge that captures data and allows it to change state. The state of this bit has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge. When the *SPH* phase control bit is clear, data is captured on the first clock edge transition. If the *SPH* bit is set, data is captured on the second clock edge transition.

#### 16.3.4.3 Freescale SPI Frame Format with *SPO=0* and *SPH=0*

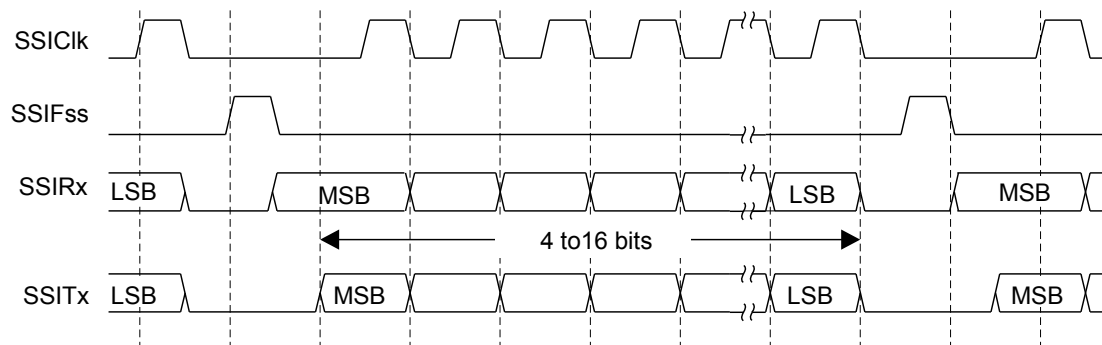
Single and continuous transmission signal sequences for Freescale SPI format with *SPO=0* and *SPH=0* are shown in Figure 16-4 on page 615 and Figure 16-5 on page 615.

**Figure 16-4. Freescale SPI Format (Single Transfer) with *SPO=0* and *SPH=0***



**Note:** Q is undefined.

**Figure 16-5. Freescale SPI Format (Continuous Transfer) with *SPO=0* and *SPH=0***



In this configuration, during idle periods:

- *SSIClk* is forced Low
- *SSIFss* is forced High
- The transmit data line *SSITx* is arbitrarily forced Low
- When the SSI is configured as a master, it enables the *SSIClk* pad
- When the SSI is configured as a slave, it disables the *SSIClk* pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the *SSIFss* master signal being driven Low, causing slave data to be enabled onto the *SSIRx* input line of the master. The master *SSITx* output pad is enabled.

One half  $SSIClk$  period later, valid master data is transferred to the  $SSITx$  pin. Once both the master and slave data have been set, the  $SSIClk$  master clock pin goes High after one additional half  $SSIClk$  period.

The data is now captured on the rising and propagated on the falling edges of the  $SSIClk$  signal.

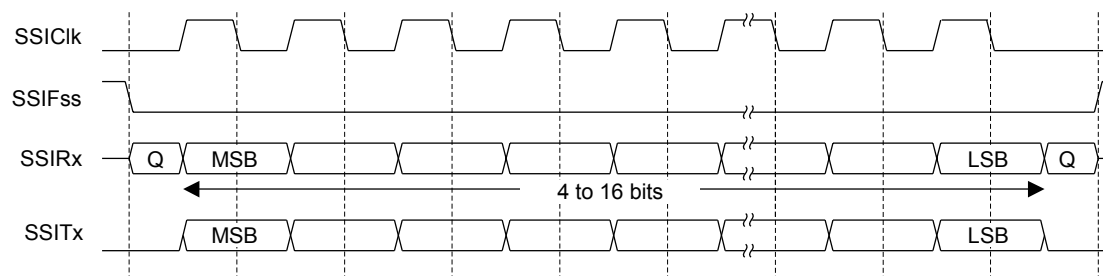
In the case of a single word transmission, after all bits of the data word have been transferred, the  $SSIFss$  line is returned to its idle High state one  $SSIClk$  period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the  $SSIFss$  signal must be pulsed High between each data word transfer because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the  $SPH$  bit is clear. Therefore, the master device must raise the  $SSIFss$  pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the  $SSIFss$  pin is returned to its idle state one  $SSIClk$  period after the last bit has been captured.

#### 16.3.4.4 Freescale SPI Frame Format with $SPO=0$ and $SPH=1$

The transfer signal sequence for Freescale SPI format with  $SPO=0$  and  $SPH=1$  is shown in Figure 16-6 on page 616, which covers both single and continuous transfers.

**Figure 16-6. Freescale SPI Frame Format with  $SPO=0$  and  $SPH=1$**



**Note:** Q is undefined.

In this configuration, during idle periods:

- $SSIClk$  is forced Low
- $SSIFss$  is forced High
- The transmit data line  $SSITx$  is arbitrarily forced Low
- When the SSI is configured as a master, it enables the  $SSIClk$  pad
- When the SSI is configured as a slave, it disables the  $SSIClk$  pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the  $SSIFss$  master signal being driven Low. The master  $SSITx$  output is enabled. After an additional one-half  $SSIClk$  period, both master and slave valid data are enabled onto their respective transmission lines. At the same time, the  $SSIClk$  is enabled with a rising edge transition.

Data is then captured on the falling edges and propagated on the rising edges of the  $SSIClk$  signal.

In the case of a single word transfer, after all bits have been transferred, the  $SSIFss$  line is returned to its idle High state one  $SSIClk$  period after the last bit has been captured.

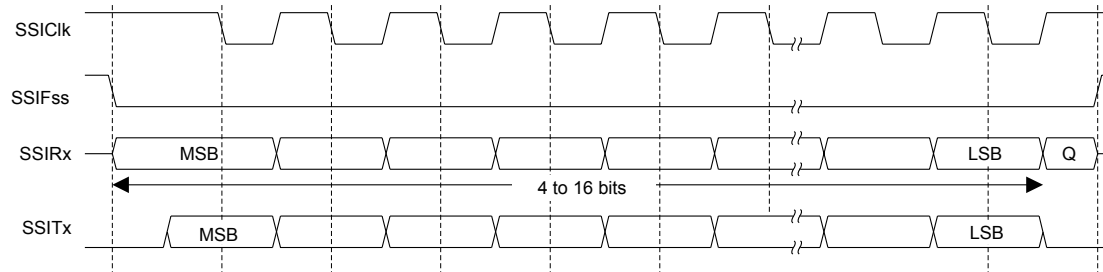


For continuous back-to-back transfers, the  $SSIF_{SS}$  pin is held Low between successive data words, and termination is the same as that of the single word transfer.

#### 16.3.4.5 Freescale SPI Frame Format with $SPO=1$ and $SPH=0$

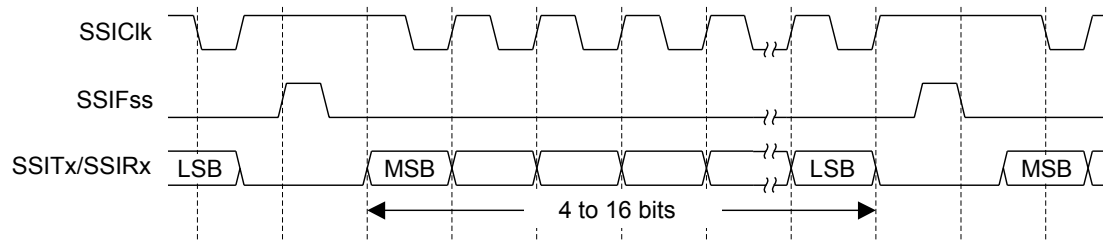
Single and continuous transmission signal sequences for Freescale SPI format with  $SPO=1$  and  $SPH=0$  are shown in Figure 16-7 on page 617 and Figure 16-8 on page 617.

**Figure 16-7. Freescale SPI Frame Format (Single Transfer) with  $SPO=1$  and  $SPH=0$**



**Note:** Q is undefined.

**Figure 16-8. Freescale SPI Frame Format (Continuous Transfer) with  $SPO=1$  and  $SPH=0$**



In this configuration, during idle periods:

- $SSIClk$  is forced High
- $SSIF_{SS}$  is forced High
- The transmit data line  $SSITx$  is arbitrarily forced Low
- When the SSI is configured as a master, it enables the  $SSIClk$  pad
- When the SSI is configured as a slave, it disables the  $SSIClk$  pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the  $SSIF_{SS}$  master signal being driven Low, causing slave data to be immediately transferred onto the  $SSIRx$  line of the master. The master  $SSITx$  output pad is enabled.

One-half period later, valid master data is transferred to the  $SSITx$  line. Once both the master and slave data have been set, the  $SSIClk$  master clock pin becomes Low after one additional half  $SSIClk$  period, meaning that data is captured on the falling edges and propagated on the rising edges of the  $SSIClk$  signal.

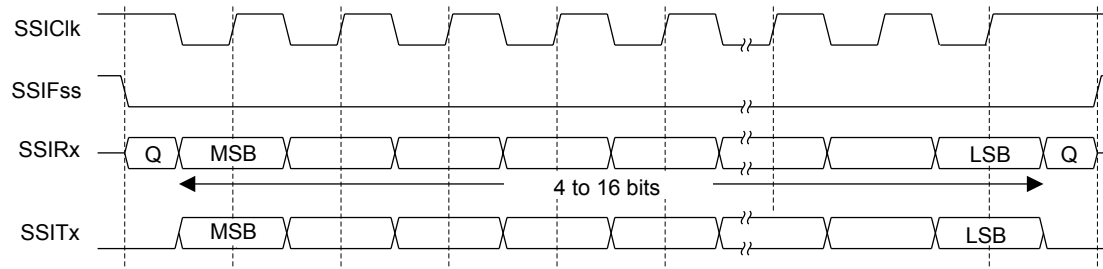
In the case of a single word transmission, after all bits of the data word are transferred, the  $SSIF_{SS}$  line is returned to its idle High state one  $SSIClk$  period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the  $SSIF_{SS}$  signal must be pulsed High between each data word transfer because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the  $SPH$  bit is clear. Therefore, the master device must raise the  $SSIF_{SS}$  pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the  $SSIF_{SS}$  pin is returned to its idle state one  $SSIClk$  period after the last bit has been captured.

#### 16.3.4.6 Freescale SPI Frame Format with $SPO=1$ and $SPH=1$

The transfer signal sequence for Freescale SPI format with  $SPO=1$  and  $SPH=1$  is shown in Figure 16-9 on page 618, which covers both single and continuous transfers.

**Figure 16-9. Freescale SPI Frame Format with  $SPO=1$  and  $SPH=1$**



**Note:** Q is undefined.

In this configuration, during idle periods:

- $SSIClk$  is forced High
- $SSIF_{SS}$  is forced High
- The transmit data line  $SSITx$  is arbitrarily forced Low
- When the SSI is configured as a master, it enables the  $SSIClk$  pad
- When the SSI is configured as a slave, it disables the  $SSIClk$  pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the  $SSIF_{SS}$  master signal being driven Low. The master  $SSITx$  output pad is enabled. After an additional one-half  $SSIClk$  period, both master and slave data are enabled onto their respective transmission lines. At the same time,  $SSIClk$  is enabled with a falling edge transition. Data is then captured on the rising edges and propagated on the falling edges of the  $SSIClk$  signal.

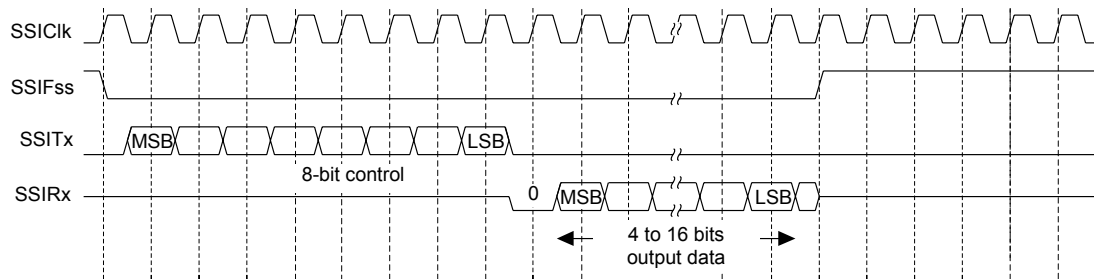
After all bits have been transferred, in the case of a single word transmission, the  $SSIF_{SS}$  line is returned to its idle high state one  $SSIClk$  period after the last bit has been captured.

For continuous back-to-back transmissions, the  $SSIF_{SS}$  pin remains in its active Low state until the final bit of the last word has been captured and then returns to its idle state as described above.

For continuous back-to-back transfers, the  $SSIF_{SS}$  pin is held Low between successive data words and termination is the same as that of the single word transfer.

#### 16.3.4.7 MICROWIRE Frame Format

Figure 16-10 on page 619 shows the MICROWIRE frame format for a single frame. Figure 16-11 on page 620 shows the same format when back-to-back frames are transmitted.

**Figure 16-10. MICROWIRE Frame Format (Single Frame)**

MICROWIRE format is very similar to SPI format, except that transmission is half-duplex instead of full-duplex and uses a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SSI to the off-chip slave device. During this transmission, no incoming data is received by the SSI. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the required data. The returned data is 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

In this configuration, during idle periods:

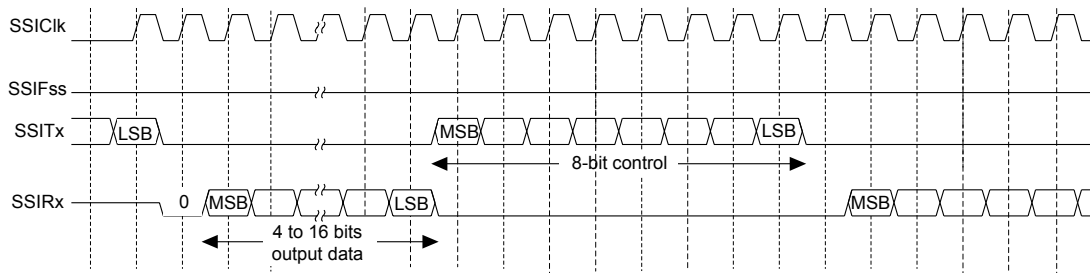
- SSIClk is forced Low
- SSIFss is forced High
- The transmit data line SSITx is arbitrarily forced Low

A transmission is triggered by writing a control byte to the transmit FIFO. The falling edge of SSIFss causes the value contained in the bottom entry of the transmit FIFO to be transferred to the serial shift register of the transmit logic and the MSB of the 8-bit control frame to be shifted out onto the SSITx pin. SSIFss remains Low for the duration of the frame transmission. The SSIRx pin remains tristated during this transmission.

The off-chip serial slave device latches each control bit into its serial shifter on each rising edge of SSIClk. After the last bit is latched by the slave device, the control byte is decoded during a one clock wait-state, and the slave responds by transmitting data back to the SSI. Each bit is driven onto the SSIRx line on the falling edge of SSIClk. The SSI in turn latches each bit on the rising edge of SSIClk. At the end of the frame, for single transfers, the SSIFss signal is pulled High one clock period after the last bit has been latched in the receive serial shifter, causing the data to be transferred to the receive FIFO.

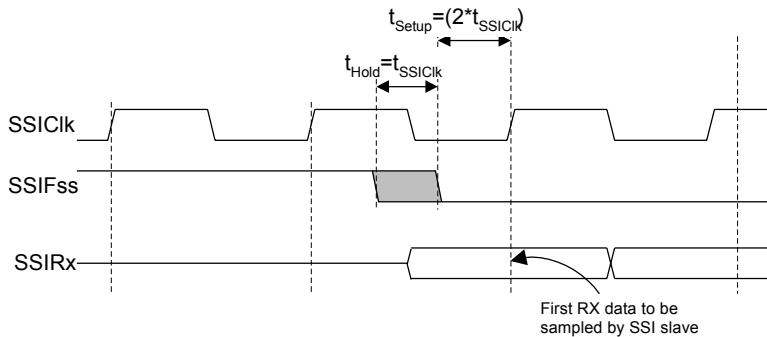
**Note:** The off-chip slave device can tristate the receive line either on the falling edge of SSIClk after the LSB has been latched by the receive shifter or when the SSIFss pin goes High.

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the SSIFss line is continuously asserted (held Low) and transmission of data occurs back-to-back. The control byte of the next frame follows directly after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge of SSIClk, after the LSB of the frame has been latched into the SSI.

**Figure 16-11. MICROWIRE Frame Format (Continuous Transfer)**

In the MICROWIRE mode, the SSI slave samples the first bit of receive data on the rising edge of `SSIClk` after `SSIFss` has gone Low. Masters that drive a free-running `SSIClk` must ensure that the `SSIFss` signal has sufficient setup and hold margins with respect to the rising edge of `SSIClk`.

Figure 16-12 on page 620 illustrates these setup and hold time requirements. With respect to the `SSIClk` rising edge on which the first bit of receive data is to be sampled by the SSI slave, `SSIFss` must have a setup of at least two times the period of `SSIClk` on which the SSI operates. With respect to the `SSIClk` rising edge previous to this edge, `SSIFss` must have a hold of at least one `SSIClk` period.

**Figure 16-12. MICROWIRE Frame Format, SSIFss Input Setup and Hold Requirements**

### 16.3.5 DMA Operation

The SSI peripheral provides an interface to the  $\mu$ DMA controller with separate channels for transmit and receive. The  $\mu$ DMA operation of the SSI is enabled through the **SSI DMA Control (SSIDMACTL)** register. When  $\mu$ DMA operation is enabled, the SSI asserts a  $\mu$ DMA request on the receive or transmit channel when the associated FIFO can transfer data. For the receive channel, a single transfer request is asserted whenever any data is in the receive FIFO. A burst transfer request is asserted whenever the amount of data in the receive FIFO is 4 or more items. For the transmit channel, a single transfer request is asserted whenever at least one empty location is in the transmit FIFO. The burst request is asserted whenever the transmit FIFO has 4 or more empty slots. The single and burst  $\mu$ DMA transfer requests are handled automatically by the  $\mu$ DMA controller depending how the  $\mu$ DMA channel is configured. To enable  $\mu$ DMA operation for the receive channel, the `RXDMAE` bit of the **DMA Control (SSIDMACTL)** register should be set. To enable  $\mu$ DMA operation for the transmit channel, the `TXDMAE` bit of **SSIDMACTL** should be set. If  $\mu$ DMA is enabled, then the  $\mu$ DMA controller triggers an interrupt when a transfer is complete. The interrupt occurs on the SSI interrupt vector. Therefore, if interrupts are used for SSI operation and  $\mu$ DMA is enabled, the SSI interrupt handler must be designed to handle the  $\mu$ DMA completion interrupt.

See “Micro Direct Memory Access ( $\mu$ DMA)” on page 230 for more details about programming the  $\mu$ DMA controller.

## 16.4 Initialization and Configuration

To enable and initialize the SSI, the following steps are necessary:

1. Enable the SSI module by setting the *SSI* bit in the **RCGC1** register (see page 149).
2. Enable the clock to the appropriate GPIO module via the **RCGC2** register (see page 158). To find out which GPIO port to enable, refer to Table 20-5 on page 722.
3. Set the GPIO *AFSEL* bits for the appropriate pins (see page 310). To determine which GPIOs to configure, see Table 20-4 on page 717.
4. Configure the *PMCn* fields in the **GPIOPCTL** register to assign the SSI signals to the appropriate pins. See page 328 and Table 20-5 on page 722.

For each of the frame formats, the SSI is configured using the following steps:

1. Ensure that the *SSE* bit in the **SSICR1** register is clear before making any configuration changes.
2. Select whether the SSI is a master or slave:
  - a. For master operations, set the **SSICR1** register to 0x0000.0000.
  - b. For slave mode (output enabled), set the **SSICR1** register to 0x0000.0004.
  - c. For slave mode (output disabled), set the **SSICR1** register to 0x0000.000C.
3. Configure the clock prescale divisor by writing the **SSICPSR** register.
4. Write the **SSICR0** register with the following configuration:
  - Serial clock rate (*SCR*)
  - Desired clock phase/polarity, if using Freescale SPI mode (*SPH* and *SPO*)
  - The protocol mode: Freescale SPI, TI SSF, MICROWIRE (*FRF*)
  - The data size (*DSS*)
5. Optionally, configure the  $\mu$ DMA channel (see “Micro Direct Memory Access ( $\mu$ DMA)” on page 230) and enable the DMA option(s) in the **SSIDMACTL** register.
6. Enable the SSI by setting the *SSE* bit in the **SSICR1** register.

As an example, assume the SSI must be configured to operate with the following parameters:

- Master operation
- Freescale SPI mode (*SPO*=1, *SPH*=1)
- 1 Mbps bit rate
- 8 data bits

Assuming the system clock is 20 MHz, the bit rate calculation would be:

$$SSIClk = SysClk / (CPSDVSR * (1 + SCR)) \times 10^6 = 20 \times 10^6 / (CPSDVSR * (1 + SCR))$$

In this case, if CPSDVSR=0x2, SCR must be 0x9.

The configuration sequence would be as follows:

1. Ensure that the SSE bit in the **SSICR1** register is clear.
2. Write the **SSICR1** register with a value of 0x0000.0000.
3. Write the **SSICPSR** register with a value of 0x0000.0002.
4. Write the **SSICR0** register with a value of 0x0000.09C7.
5. The SSI is then enabled by setting the SSE bit in the **SSICR1** register.

## 16.5 Register Map

Table 16-2 on page 622 lists the SSI registers. The offset listed is a hexadecimal increment to the register's address, relative to that SSI module's base address:

- SSI0: 0x4000.8000
- SSI1: 0x4000.9000

Note that the SSI module clock must be enabled before the registers can be programmed (see page 149).

**Note:** The SSI must be disabled (see the SSE bit in the **SSICR1** register) before any of the control registers are reprogrammed.

**Table 16-2. SSI Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	SSICR0	R/W	0x0000.0000	SSI Control 0	624
0x004	SSICR1	R/W	0x0000.0000	SSI Control 1	626
0x008	SSIDR	R/W	0x0000.0000	SSI Data	628
0x00C	SSISR	RO	0x0000.0003	SSI Status	629
0x010	SSICPSR	R/W	0x0000.0000	SSI Clock Prescale	631
0x014	SSIIM	R/W	0x0000.0000	SSI Interrupt Mask	632
0x018	SSIRIS	RO	0x0000.0008	SSI Raw Interrupt Status	633
0x01C	SSIMIS	RO	0x0000.0000	SSI Masked Interrupt Status	635
0x020	SSIICR	W1C	0x0000.0000	SSI Interrupt Clear	637
0x024	SSIDMACTL	R/W	0x0000.0000	SSI DMA Control	638
0xFD0	SSIPeriphID4	RO	0x0000.0000	SSI Peripheral Identification 4	639
0xFD4	SSIPeriphID5	RO	0x0000.0000	SSI Peripheral Identification 5	640

**Table 16-2. SSI Register Map (continued)**

Offset	Name	Type	Reset	Description	See page
0xFD8	SSIPeriphID6	RO	0x0000.0000	SSI Peripheral Identification 6	641
0xFDC	SSIPeriphID7	RO	0x0000.0000	SSI Peripheral Identification 7	642
0xFE0	SSIPeriphID0	RO	0x0000.0022	SSI Peripheral Identification 0	643
0xFE4	SSIPeriphID1	RO	0x0000.0000	SSI Peripheral Identification 1	644
0xFE8	SSIPeriphID2	RO	0x0000.0018	SSI Peripheral Identification 2	645
0xFEC	SSIPeriphID3	RO	0x0000.0001	SSI Peripheral Identification 3	646
0xFF0	SSIPCellID0	RO	0x0000.000D	SSI PrimeCell Identification 0	647
0xFF4	SSIPCellID1	RO	0x0000.00F0	SSI PrimeCell Identification 1	648
0xFF8	SSIPCellID2	RO	0x0000.0005	SSI PrimeCell Identification 2	649
0xFFC	SSIPCellID3	RO	0x0000.00B1	SSI PrimeCell Identification 3	650

## 16.6 Register Descriptions

The remainder of this section lists and describes the SSI registers, in numerical order by address offset.

**Register 1: SSI Control 0 (SSICR0), offset 0x000**

The **SSICR0** register contains bit fields that control various functions within the SSI module. Functionality such as protocol mode, clock rate, and data size are configured in this register.

## SSI Control 0 (SSICR0)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x000  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCR								SPH	SPO	FRF		DSS			
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:8	SCR	R/W	0x00	SSI Serial Clock Rate  This bit field is used to generate the transmit and receive bit rate of the SSI. The bit rate is:  $BR = SSI\text{Clk} / (\text{CPSDVSR} * (1 + \text{SCR}))$ where <b>CPSDVSR</b> is an even value from 2-254 programmed in the <b>SSICPSR</b> register, and <b>SCR</b> is a value from 0-255.
7	SPH	R/W	0	SSI Serial Clock Phase  This bit is only applicable to the Freescale SPI Format.  The <b>SPH</b> control bit selects the clock edge that captures data and allows it to change state. This bit has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge.  Value Description 0 Data is captured on the first clock edge transition. 1 Data is captured on the second clock edge transition.
6	SPO	R/W	0	SSI Serial Clock Polarity  Value Description 0 A steady state Low value is placed on the <b>SSIClk</b> pin. 1 A steady state High value is placed on the <b>SSIClk</b> pin when data is not being transferred.



Bit/Field	Name	Type	Reset	Description
5:4	FRF	R/W	0x0	SSI Frame Format Select  Value Frame Format 0x0 Freescale SPI Frame Format 0x1 Texas Instruments Synchronous Serial Frame Format 0x2 MICROWIRE Frame Format 0x3 Reserved
3:0	DSS	R/W	0x0	SSI Data Size Select  Value Data Size 0x0-0x2 Reserved 0x3 4-bit data 0x4 5-bit data 0x5 6-bit data 0x6 7-bit data 0x7 8-bit data 0x8 9-bit data 0x9 10-bit data 0xA 11-bit data 0xB 12-bit data 0xC 13-bit data 0xD 14-bit data 0xE 15-bit data 0xF 16-bit data

**Register 2: SSI Control 1 (SSICR1), offset 0x004**

The **SSICR1** register contains bit fields that control various functions within the SSI module. Master and slave mode functionality is controlled by this register.

## SSI Control 1 (SSICR1)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x004  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												EOT	SOD	MS	SSE	LBM
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:5	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	EOT	R/W	0	End of Transmission  Value Description 0 The TXRIS interrupt indicates that the transmit FIFO is half full or less. 1 The End of Transmit interrupt mode for the TXRIS interrupt is enabled.
3	SOD	R/W	0	SSI Slave Mode Output Disable  This bit is relevant only in the Slave mode ( $MS=1$ ). In multiple-slave systems, it is possible for the SSI master to broadcast a message to all slaves in the system while ensuring that only one slave drives data onto the serial output line. In such systems, the TXD lines from multiple slaves could be tied together. To operate in such a system, the SOD bit can be configured so that the SSI slave does not drive the SSITx pin.  Value Description 0 SSI can drive the SSITx output in Slave mode. 1 SSI must not drive the SSITx output in Slave mode.
2	MS	R/W	0	SSI Master/Slave Select  This bit selects Master or Slave mode and can be modified only when the SSI is disabled ( $SSE=0$ ).  Value Description 0 The SSI is configured as a master. 1 The SSI is configured as a slave.

---

Bit/Field	Name	Type	Reset	Description
1	SSE	R/W	0	SSI Synchronous Serial Port Enable  Value Description 0 SSI operation is disabled. 1 SSI operation is enabled.  <b>Note:</b> This bit must be cleared before any control registers are reprogrammed.
0	LBM	R/W	0	SSI Loopback Mode  Value Description 0 Normal serial port operation enabled. 1 Output of the transmit serial shift register is connected internally to the input of the receive serial shift register.

### Register 3: SSI Data (SSIDR), offset 0x008

**Important:** Use caution when reading this register. Performing a read may change bit status.

The **SSIDR** register is 16-bits wide. When the **SSIDR** register is read, the entry in the receive FIFO that is pointed to by the current FIFO read pointer is accessed. When a data value is removed by the SSI receive logic from the incoming data frame, it is placed into the entry in the receive FIFO pointed to by the current FIFO write pointer.

When the **SSIDR** register is written to, the entry in the transmit FIFO that is pointed to by the write pointer is written to. Data values are removed from the transmit FIFO one value at a time by the transmit logic. Each data value is loaded into the transmit serial shifter, then serially shifted out onto the **SSITx** pin at the programmed bit rate.

When a data size of less than 16 bits is selected, the user must right-justify data written to the transmit FIFO. The transmit logic ignores the unused bits. Received data less than 16 bits is automatically right-justified in the receive buffer.

When the SSI is programmed for MICROWIRE frame format, the default size for transmit data is eight bits (the most significant byte is ignored). The receive data size is controlled by the programmer. The transmit FIFO and the receive FIFO are not cleared even when the **SSE** bit in the **SSICR1** register is cleared, allowing the software to fill the transmit FIFO before enabling the SSI.

#### SSI Data (SSIDR)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x008  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA															
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:16	reserved	RO	0x0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15:0	DATA	R/W	0x0000	SSI Receive/Transmit Data  A read operation reads the receive FIFO. A write operation writes the transmit FIFO.  Software must right-justify data when the SSI is programmed for a data size that is less than 16 bits. Unused bits at the top are ignored by the transmit logic. The receive logic automatically right-justifies the data.

## Register 4: SSI Status (SSISR), offset 0x00C

The **SSISR** register contains bits that indicate the FIFO fill status and the SSI busy status.

### SSI Status (SSISR)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x00C  
 Type RO, reset 0x0000.0003

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved												BSY	RFF	RNE	TNF	TFE
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	

Bit/Field	Name	Type	Reset	Description
31:5	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4	BSY	RO	0	SSI Busy Bit  Value Description 0 The SSI is idle. 1 The SSI is currently transmitting and/or receiving a frame, or the transmit FIFO is not empty.
3	RFF	RO	0	SSI Receive FIFO Full  Value Description 0 The receive FIFO is not full. 1 The receive FIFO is full.
2	RNE	RO	0	SSI Receive FIFO Not Empty  Value Description 0 The receive FIFO is empty. 1 The receive FIFO is not empty.
1	TNF	RO	1	SSI Transmit FIFO Not Full  Value Description 0 The transmit FIFO is full. 1 The transmit FIFO is not full.

Bit/Field	Name	Type	Reset	Description
0	TFE	RO	1	SSI Transmit FIFO Empty
				Value Description
				0 The transmit FIFO is not empty.
				1 The transmit FIFO is empty.

## Register 5: SSI Clock Prescale (SSICPSR), offset 0x010

The **SSICPSR** register specifies the division factor which is used to derive the **SSIClk** from the system clock. The clock is further divided by a value from 1 to 256, which is  $1 + \text{SCR}$ . **SCR** is programmed in the **SSICR0** register. The frequency of the **SSIClk** is defined by:

$$\text{SSIClk} = \text{SysClk} / (\text{CPSDVSR} * (1 + \text{SCR}))$$

The value programmed into this register must be an even number between 2 and 254. The least-significant bit of the programmed number is hard-coded to zero. If an odd number is written to this register, data read back from this register has the least-significant bit as zero.

### SSI Clock Prescale (SSICPSR)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x010  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CPSDVSR							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CPSDVSR	R/W	0x00	SSI Clock Prescale Divisor  This value must be an even number from 2 to 254, depending on the frequency of <b>SSIClk</b> . The LSB always returns 0 on reads.

### Register 6: SSI Interrupt Mask (SSIIM), offset 0x014

The **SSIIM** register is the interrupt mask set or clear register. It is a read/write register and all bits are cleared on reset.

On a read, this register gives the current value of the mask on the corresponding interrupt. Setting a bit sets the mask, preventing the interrupt from being signaled to the interrupt controller. Clearing a bit clears the corresponding mask, enabling the interrupt to be sent to the interrupt controller.

#### SSI Interrupt Mask (SSIIM)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x014  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													TXIM	RXIM	RTIM	RORIM
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	TXIM	R/W	0	SSI Transmit FIFO Interrupt Mask  Value Description 0 The transmit FIFO interrupt is masked. 1 The transmit FIFO interrupt is not masked.
2	RXIM	R/W	0	SSI Receive FIFO Interrupt Mask  Value Description 0 The receive FIFO interrupt is masked. 1 The receive FIFO interrupt is not masked.
1	RTIM	R/W	0	SSI Receive Time-Out Interrupt Mask  Value Description 0 The receive FIFO time-out interrupt is masked. 1 The receive FIFO time-out interrupt is not masked.
0	RORIM	R/W	0	SSI Receive Overrun Interrupt Mask  Value Description 0 The receive FIFO overrun interrupt is masked. 1 The receive FIFO overrun interrupt is not masked.



## Register 7: SSI Raw Interrupt Status (SSIRIS), offset 0x018

The **SSIRIS** register is the raw interrupt status register. On a read, this register gives the current raw status value of the corresponding interrupt prior to masking. A write has no effect.

### SSI Raw Interrupt Status (SSIRIS)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x018  
 Type RO, reset 0x0000.0008

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													TXRIS	RXRIS	RTRIS	RORRIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	TXRIS	RO	1	SSI Transmit FIFO Raw Interrupt Status  Value Description 0 No interrupt. 1 If the <b>EOT</b> bit in the <b>SSICR1</b> register is clear, the transmit FIFO is half full or less.  If the <b>EOT</b> bit is set, the transmit FIFO is empty, and the last bit has been transmitted out of the serializer.  This bit is cleared when the transmit FIFO is more than half full (if the <b>EOT</b> bit is clear) or when it has any data in it (if the <b>EOT</b> bit is set).
2	RXRIS	RO	0	SSI Receive FIFO Raw Interrupt Status  Value Description 0 No interrupt. 1 The receive FIFO is half full or more.  This bit is cleared when the receive FIFO is less than half full.
1	RTRIS	RO	0	SSI Receive Time-Out Raw Interrupt Status  Value Description 0 No interrupt. 1 The receive time-out has occurred.  This bit is cleared when a 1 is written to the <b>RTIC</b> bit in the <b>SSI Interrupt Clear (SSIICR)</b> register.

Bit/Field	Name	Type	Reset	Description
0	RORRIS	RO	0	SSI Receive Overrun Raw Interrupt Status  Value Description 0 No interrupt. 1 The receive FIFO has overflowed  This bit is cleared when a 1 is written to the RORIC bit in the <b>SSI Interrupt Clear (SSIICR)</b> register.

## Register 8: SSI Masked Interrupt Status (SSIMIS), offset 0x01C

The **SSIMIS** register is the masked interrupt status register. On a read, this register gives the current masked status value of the corresponding interrupt. A write has no effect.

### SSI Masked Interrupt Status (SSIMIS)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x01C  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													TXMIS	RXMIS	RTMIS	RORMIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:4	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	TXMIS	RO	0	SSI Transmit FIFO Masked Interrupt Status  Value Description 0 An interrupt has not occurred or is masked. 1 An unmasked interrupt was signaled due to the transmit FIFO being half full or less (if the <code>EOT</code> bit is clear) or due to the transmission of the last data bit (if the <code>EOT</code> bit is set).  This bit is cleared when the transmit FIFO is more than half full (if the <code>EOT</code> bit is clear) or when it has any data in it (if the <code>EOT</code> bit is set).
2	RXMIS	RO	0	SSI Receive FIFO Masked Interrupt Status  Value Description 0 An interrupt has not occurred or is masked. 1 An unmasked interrupt was signaled due to the receive FIFO being half full or less.  This bit is cleared when the receive FIFO is less than half full.
1	RTMIS	RO	0	SSI Receive Time-Out Masked Interrupt Status  Value Description 0 An interrupt has not occurred or is masked. 1 An unmasked interrupt was signaled due to the receive time out.  This bit is cleared when a 1 is written to the <code>RTIC</code> bit in the <b>SSI Interrupt Clear (SSIICR)</b> register.

Bit/Field	Name	Type	Reset	Description
0	RORMIS	RO	0	SSI Receive Overrun Masked Interrupt Status
				Value Description
				0 An interrupt has not occurred or is masked.
				1 An unmasked interrupt was signaled due to the receive FIFO overflowing.
				This bit is cleared when a 1 is written to the RORIC bit in the <b>SSI Interrupt Clear (SSIICR)</b> register.

## Register 9: SSI Interrupt Clear (SSIICR), offset 0x020

The **SSIICR** register is the interrupt clear register. On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.

### SSI Interrupt Clear (SSIICR)

SSI0 base: 0x4000.8000

SSI1 base: 0x4000.9000

Offset 0x020

Type W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved														RTIC	RORIC	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.0000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	RTIC	W1C	0	SSI Receive Time-Out Interrupt Clear  Writing a 1 to this bit clears the <b>RTRIS</b> bit in the <b>SSIRIS</b> register and the <b>RTMIS</b> bit in the <b>SSIMIS</b> register.
0	RORIC	W1C	0	SSI Receive Overrun Interrupt Clear  Writing a 1 to this bit clears the <b>RORRIS</b> bit in the <b>SSIRIS</b> register and the <b>RORMIS</b> bit in the <b>SSIMIS</b> register.

### Register 10: SSI DMA Control (SSIDMACTL), offset 0x024

The **SSIDMACTL** register is the  $\mu$ DMA control register.

#### SSI DMA Control (SSIDMACTL)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0x024  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved														TXDMAE	RXDMAE
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	TXDMAE	R/W	0	Transmit DMA Enable  Value Description 0 $\mu$ DMA for the transmit FIFO is disabled. 1 $\mu$ DMA for the transmit FIFO is enabled.
0	RXDMAE	R/W	0	Receive DMA Enable  Value Description 0 $\mu$ DMA for the receive FIFO is disabled. 1 $\mu$ DMA for the receive FIFO is enabled.

**Register 11: SSI Peripheral Identification 4 (SSIPeriphID4), offset 0xFD0**

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

**SSI Peripheral Identification 4 (SSIPeriphID4)**

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFD0  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID4							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

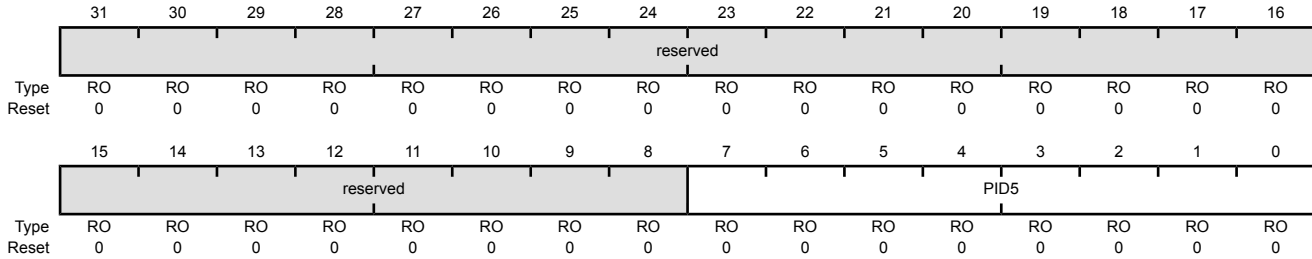
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID4	RO	0x00	SSI Peripheral ID Register [7:0]  Can be used by software to identify the presence of this peripheral.

### Register 12: SSI Peripheral Identification 5 (SSIPeriphID5), offset 0xFD4

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

#### SSI Peripheral Identification 5 (SSIPeriphID5)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFD4  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID5	RO	0x00	SSI Peripheral ID Register [15:8]  Can be used by software to identify the presence of this peripheral.



## Register 13: SSI Peripheral Identification 6 (SSIPeriphID6), offset 0xFD8

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### SSI Peripheral Identification 6 (SSIPeriphID6)

SSI0 base: 0x4000.8000

SSI1 base: 0x4000.9000

Offset 0xFD8

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID6							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID6	RO	0x00	SSI Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.

### Register 14: SSI Peripheral Identification 7 (SSIPeriphID7), offset 0xFDC

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

#### SSI Peripheral Identification 7 (SSIPeriphID7)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFDC  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID7							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID7	RO	0x00	SSI Peripheral ID Register [31:24]  Can be used by software to identify the presence of this peripheral.

**Register 15: SSI Peripheral Identification 0 (SSIPeriphID0), offset 0xFE0**

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

**SSI Peripheral Identification 0 (SSIPeriphID0)**

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFE0  
 Type RO, reset 0x0000.0022

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID0							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0

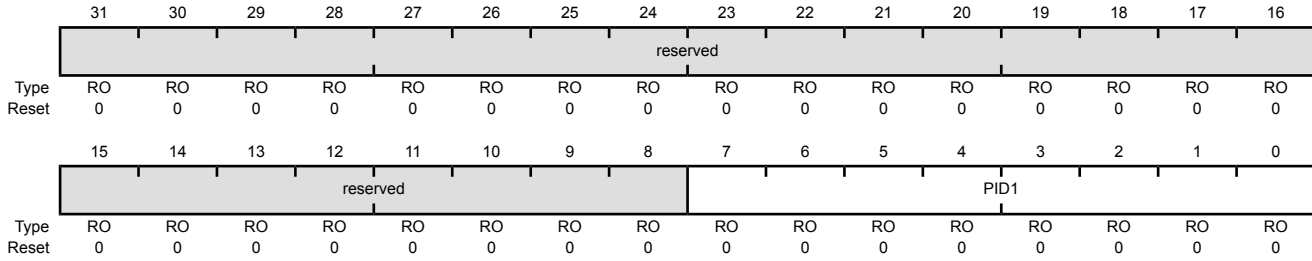
Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID0	RO	0x22	SSI Peripheral ID Register [7:0]  Can be used by software to identify the presence of this peripheral.

### Register 16: SSI Peripheral Identification 1 (SSIPeriphID1), offset 0xFE4

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

#### SSI Peripheral Identification 1 (SSIPeriphID1)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFE4  
 Type RO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID1	RO	0x00	SSI Peripheral ID Register [15:8] Can be used by software to identify the presence of this peripheral.

## Register 17: SSI Peripheral Identification 2 (SSIPeriphID2), offset 0xFE8

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

### SSI Peripheral Identification 2 (SSIPeriphID2)

SSI0 base: 0x4000.8000

SSI1 base: 0x4000.9000

Offset 0xFE8

Type RO, reset 0x0000.0018

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID2							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID2	RO	0x18	SSI Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.

### Register 18: SSI Peripheral Identification 3 (SSIPeriphID3), offset 0xFEC

The **SSIPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

#### SSI Peripheral Identification 3 (SSIPeriphID3)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFEC  
 Type RO, reset 0x0000.0001

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								PID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	PID3	RO	0x01	SSI Peripheral ID Register [31:24]  Can be used by software to identify the presence of this peripheral.

**Register 19: SSI PrimeCell Identification 0 (SSIPCellID0), offset 0xFF0**

The **SSIPCellIDn** registers are hard-coded, and the fields within the register determine the reset value.

**SSI PrimeCell Identification 0 (SSIPCellID0)**

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFF0  
 Type RO, reset 0x0000.000D

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID0							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID0	RO	0x0D	SSI PrimeCell ID Register [7:0] Provides software a standard cross-peripheral identification system.

### Register 20: SSI PrimeCell Identification 1 (SSIPCellID1), offset 0xFF4

The **SSIPCellIDn** registers are hard-coded, and the fields within the register determine the reset value.

#### SSI PrimeCell Identification 1 (SSIPCellID1)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFF4  
 Type RO, reset 0x0000.00F0

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID1							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID1	RO	0xF0	SSI PrimeCell ID Register [15:8] Provides software a standard cross-peripheral identification system.



**Register 21: SSI PrimeCell Identification 2 (SSIPCellID2), offset 0xFF8**

The **SSIPCellIDn** registers are hard-coded, and the fields within the register determine the reset value.

**SSI PrimeCell Identification 2 (SSIPCellID2)**

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFF8  
 Type RO, reset 0x0000.0005

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID2							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID2	RO	0x05	SSI PrimeCell ID Register [23:16] Provides software a standard cross-peripheral identification system.

### Register 22: SSI PrimeCell Identification 3 (SSIPCellID3), offset 0xFFC

The **SSIPCellIDn** registers are hard-coded, and the fields within the register determine the reset value.

#### SSI PrimeCell Identification 3 (SSIPCellID3)

SSI0 base: 0x4000.8000  
 SSI1 base: 0x4000.9000  
 Offset 0xFFC  
 Type RO, reset 0x0000.00B1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								CID3							
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	CID3	RO	0xB1	SSI PrimeCell ID Register [31:24] Provides software a standard cross-peripheral identification system.

## 17 Inter-Integrated Circuit (I<sup>2</sup>C) Interface

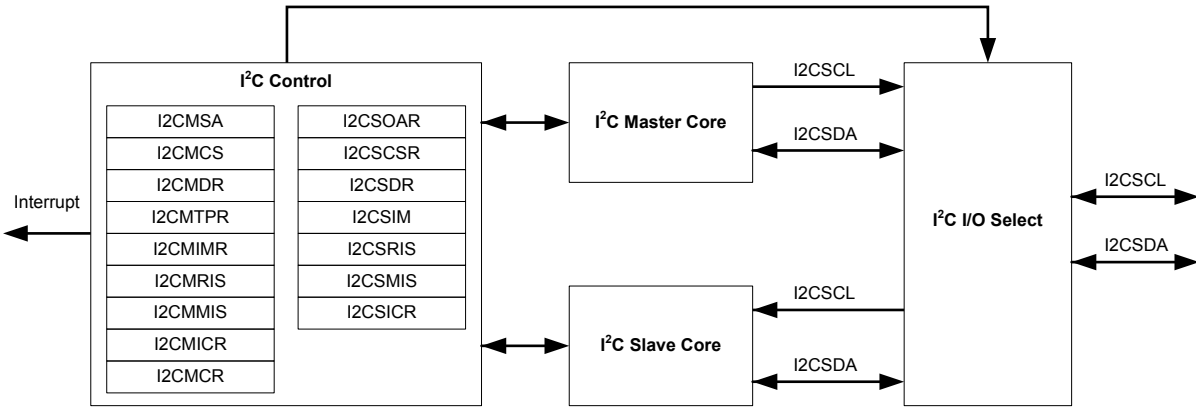
The Inter-Integrated Circuit (I<sup>2</sup>C) bus provides bi-directional data transfer through a two-wire design (a serial data line SDA and a serial clock line SCL), and interfaces to external I<sup>2</sup>C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on. The I<sup>2</sup>C bus may also be used for system testing and diagnostic purposes in product development and manufacture. The LM3S1811 microcontroller includes two I<sup>2</sup>C modules, providing the ability to interact (both transmit and receive) with other I<sup>2</sup>C devices on the bus.

The Stellaris® LM3S1811 controller includes two I<sup>2</sup>C modules with the following features:

- Devices on the I<sup>2</sup>C bus can be designated as either a master or a slave
  - Supports both transmitting and receiving data as either a master or a slave
  - Supports simultaneous master and slave operation
- Four I<sup>2</sup>C modes
  - Master transmit
  - Master receive
  - Slave transmit
  - Slave receive
- Two transmission speeds: Standard (100 Kbps) and Fast (400 Kbps)
- Master and slave interrupt generation
  - Master generates interrupts when a transmit or receive operation completes (or aborts due to an error)
  - Slave generates interrupts when data has been transferred or requested by a master or when a START or STOP condition is detected
- Master with arbitration and clock synchronization, multimaster support, and 7-bit addressing mode

## 17.1 Block Diagram

Figure 17-1. I<sup>2</sup>C Block Diagram



## 17.2 Signal Description

Table 17-1 on page 652 lists the external signals of the I<sup>2</sup>C interface and describes the function of each. The I<sup>2</sup>C interface signals are alternate functions for some GPIO signals and default to be GPIO signals at reset., with the exception of the I<sup>2</sup>C0SCL and I<sup>2</sup>C0SDA pins which default to the I<sup>2</sup>C function. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for the I<sup>2</sup>C signals. The AFSEL bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) should be set to choose the I<sup>2</sup>C function. The number in parentheses is the encoding that must be programmed into the PMC<sub>n</sub> field in the **GPIO Port Control (GPIOPTL)** register (page 328) to assign the I<sup>2</sup>C signal to the specified GPIO port pin. Note that the I<sup>2</sup>C pins should be set to open drain using the **GPIO Open Drain Select (GPIOODR)** register. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 288.

Table 17-1. Signals for I2C

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
I2C0SCL	72	PB2 (1)	I/O	OD	I <sup>2</sup> C module 0 clock.
I2C0SDA	65	PB3 (1)	I/O	OD	I <sup>2</sup> C module 0 data.
I2C1SCL	14	PJ0 (11)	I/O	OD	I <sup>2</sup> C module 1 clock.
	19	PG0 (3)			
	26	PA0 (8)			
	34	PA6 (1)			
I2C1SDA	18	PG1 (3)	I/O	OD	I <sup>2</sup> C module 1 data.
	27	PA1 (8)			
	35	PA7 (1)			
	87	PJ1 (11)			

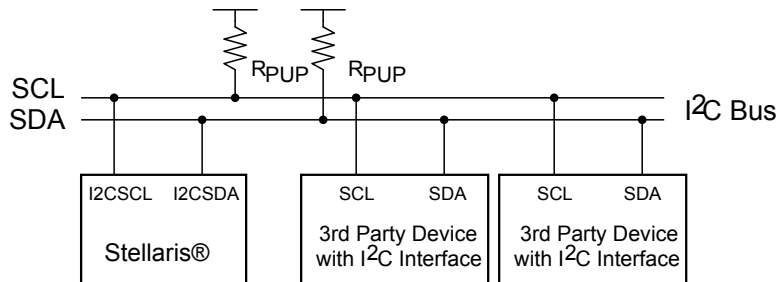
a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 17.3 Functional Description

Each I<sup>2</sup>C module is comprised of both master and slave functions which are implemented as separate peripherals. For proper operation, the SDA and SCL pins must be connected to bi-directional open-drain pads. A typical I<sup>2</sup>C bus configuration is shown in Figure 17-2.

See “Inter-Integrated Circuit (I<sup>2</sup>C) Interface” on page 744 for I<sup>2</sup>C timing diagrams.

**Figure 17-2. I<sup>2</sup>C Bus Configuration**



### 17.3.1 I<sup>2</sup>C Bus Functional Overview

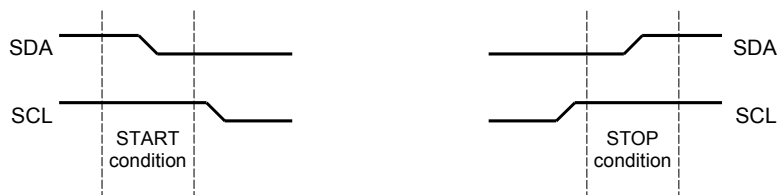
The I<sup>2</sup>C bus uses only two signals: SDA and SCL, named I2CSDA and I2CSCL on Stellaris® microcontrollers. SDA is the bi-directional serial data line and SCL is the bi-directional serial clock line. The bus is considered idle when both lines are High.

Every transaction on the I<sup>2</sup>C bus is nine bits long, consisting of eight data bits and a single acknowledge bit. The number of bytes per transfer (defined as the time between a valid START and STOP condition, described in “START and STOP Conditions” on page 653) is unrestricted, but each byte has to be followed by an acknowledge bit, and data must be transferred MSB first. When a receiver cannot receive another complete byte, it can hold the clock line SCL Low and force the transmitter into a wait state. The data transfer continues when the receiver releases the clock SCL.

#### 17.3.1.1 START and STOP Conditions

The protocol of the I<sup>2</sup>C bus defines two states to begin and end a transaction: START and STOP. A High-to-Low transition on the SDA line while the SCL is High is defined as a START condition, and a Low-to-High transition on the SDA line while SCL is High is defined as a STOP condition. The bus is considered busy after a START condition and free after a STOP condition. See Figure 17-3.

**Figure 17-3. START and STOP Conditions**



The STOP bit determines if the cycle stops at the end of the data cycle or continues on to a repeated START condition. To generate a single transmit cycle, the **I<sup>2</sup>C Master Slave Address (I2CMSA)** register is written with the desired address, the R/S bit is cleared, and the Control register is written with ACK=X (0 or 1), STOP=1, START=1, and RUN=1 to perform the operation and stop. When the operation is completed (or aborted due an error), the interrupt pin becomes active and the data may

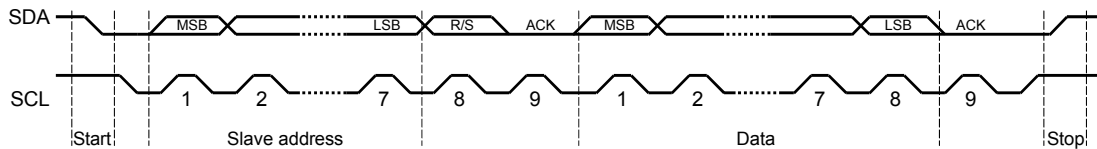
be read from the **I2CMDR** register. When the I<sup>2</sup>C module operates in Master receiver mode, the **ACK** bit is normally set causing the I<sup>2</sup>C bus controller to transmit an acknowledge automatically after each byte. This bit must be cleared when the I<sup>2</sup>C bus controller requires no further data to be transmitted from the slave transmitter.

When operating in slave mode, two bits in the **I2CSRIS** register indicate detection of start and stop conditions on the bus; while two bits in the **I2CSMIS** register allow start and stop conditions to be promoted to controller interrupts (when interrupts are enabled).

### 17.3.1.2 Data Format with 7-Bit Address

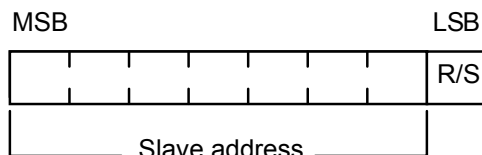
Data transfers follow the format shown in Figure 17-4. After the START condition, a slave address is transmitted. This address is 7-bits long followed by an eighth bit, which is a data direction bit (**R/S** bit in the **I2CMSA** register). If the **R/S** bit is clear, it indicates a transmit operation (send), and if it is set, it indicates a request for data (receive). A data transfer is always terminated by a STOP condition generated by the master, however, a master can initiate communications with another device on the bus by generating a repeated START condition and addressing another slave without first generating a STOP condition. Various combinations of receive/transmit formats are then possible within a single transfer.

**Figure 17-4. Complete Data Transfer with a 7-Bit Address**



The first seven bits of the first byte make up the slave address (see Figure 17-5). The eighth bit determines the direction of the message. A zero in the **R/S** position of the first byte means that the master transmits (sends) data to the selected slave, and a one in this position means that the master receives data from the slave.

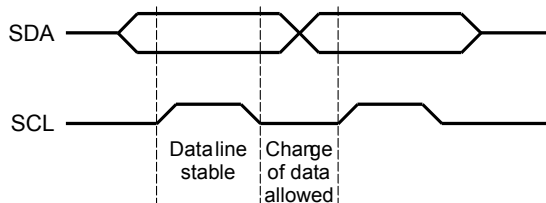
**Figure 17-5. R/S Bit in First Byte**



### 17.3.1.3 Data Validity

The data on the SDA line must be stable during the high period of the clock, and the data line can only change when SCL is Low (see Figure 17-6).

**Figure 17-6. Data Validity During Bit Transfer on the I<sup>2</sup>C Bus**



#### 17.3.1.4 Acknowledge

All bus transactions have a required acknowledge clock cycle that is generated by the master. During the acknowledge cycle, the transmitter (which can be the master or slave) releases the SDA line. To acknowledge the transaction, the receiver must pull down SDA during the acknowledge clock cycle. The data transmitted out by the receiver during the acknowledge cycle must comply with the data validity requirements described in “Data Validity” on page 654.

When a slave receiver does not acknowledge the slave address, SDA must be left High by the slave so that the master can generate a STOP condition and abort the current transfer. If the master device is acting as a receiver during a transfer, it is responsible for acknowledging each transfer made by the slave. Because the master controls the number of bytes in the transfer, it signals the end of data to the slave transmitter by not generating an acknowledge on the last data byte. The slave transmitter must then release SDA to allow the master to generate the STOP or a repeated START condition.

#### 17.3.1.5 Arbitration

A master may start a transfer only if the bus is idle. It's possible for two or more masters to generate a START condition within minimum hold time of the START condition. In these situations, an arbitration scheme takes place on the SDA line, while SCL is High. During arbitration, the first of the competing master devices to place a '1' (High) on SDA while another master transmits a '0' (Low) switches off its data output stage and retires until the bus is idle again.

Arbitration can take place over several bits. Its first stage is a comparison of address bits, and if both masters are trying to address the same device, arbitration continues on to the comparison of data bits.

### 17.3.2 Available Speed Modes

The I<sup>2</sup>C bus can run in either Standard mode (100 kbps) or Fast mode (400 kbps). The selected mode should match the speed of the other I<sup>2</sup>C devices on the bus. The mode is selected by using a value in the **I<sup>2</sup>C Master Timer Period (I2CMTPR)** register that results in an SCL frequency of 100 kbps for Standard mode or 400 kbps for Fast mode.

The I<sup>2</sup>C clock rate is determined by the parameters *CLK\_PRD*, *TIMER\_PRD*, *SCL\_LP*, and *SCL\_HP* where:

*CLK\_PRD* is the system clock period

*SCL\_LP* is the low phase of SCL (fixed at 6)

*SCL\_HP* is the high phase of SCL (fixed at 4)

**TIMER\_PRD** is the programmed value in the **I2CMTPR** register (see page 674).

The I<sup>2</sup>C clock period is calculated as follows:

$$SCL\_PERIOD = 2 \times (1 + TIMER\_PRD) \times (SCL\_LP + SCL\_HP) \times CLK\_PRD$$

For example:

$$CLK\_PRD = 50 \text{ ns}$$

$$TIMER\_PRD = 2$$

$$SCL\_LP = 6$$

$$SCL\_HP = 4$$

yields a SCL frequency of:

$$1/SCL\_PERIOD = 333 \text{ Khz}$$

Table 17-2 gives examples of the timer periods that should be used to generate both Standard and Fast mode SCL frequencies based on various system clock frequencies.

**Table 17-2. Examples of I<sup>2</sup>C Master Timer Period versus Speed Mode**

System Clock	Timer Period	Standard Mode	Timer Period	Fast Mode
4 MHz	0x01	100 Kbps	-	-
6 MHz	0x02	100 Kbps	-	-
12.5 MHz	0x06	89 Kbps	0x01	312 Kbps
16.7 MHz	0x08	93 Kbps	0x02	278 Kbps
20 MHz	0x09	100 Kbps	0x02	333 Kbps
25 MHz	0x0C	96.2 Kbps	0x03	312 Kbps
33 MHz	0x10	97.1 Kbps	0x04	330 Kbps
40 MHz	0x13	100 Kbps	0x04	400 Kbps
50 MHz	0x18	100 Kbps	0x06	357 Kbps

### 17.3.3 Interrupts

The I<sup>2</sup>C can generate interrupts when the following conditions are observed:

- Master transaction completed
- Master transaction error
- Slave transaction received
- Slave transaction requested
- Stop condition on bus detected
- Start condition on bus detected

The I<sup>2</sup>C master and I<sup>2</sup>C slave modules have separate interrupt signals. While both modules can generate interrupts for multiple conditions, only a single interrupt signal is sent to the interrupt controller.

#### 17.3.3.1 I<sup>2</sup>C Master Interrupts

The I<sup>2</sup>C master module generates an interrupt when a transaction completes (either transmit or receive), or when an error occurs during a transaction. To enable the I<sup>2</sup>C master interrupt, software must set the `IM` bit in the **I<sup>2</sup>C Master Interrupt Mask (I2CMIMR)** register. When an interrupt condition is met, software must check the `ERROR` bit in the **I<sup>2</sup>C Master Control/Status (I2CMCS)** register to verify that an error didn't occur during the last transaction. An error condition is asserted if the last transaction wasn't acknowledged by the slave, or if the master was forced to give up ownership of the bus due to a lost arbitration round with another master. If an error is not detected, the application can proceed with the transfer. The interrupt is cleared by writing a 1 to the `IC` bit in the **I<sup>2</sup>C Master Interrupt Clear (I2CMICR)** register.

If the application doesn't require the use of interrupts, the raw interrupt status is always visible via the **I<sup>2</sup>C Master Raw Interrupt Status (I2CMRIS)** register.



### 17.3.3.2 I<sup>2</sup>C Slave Interrupts

The slave module can generate an interrupt when data has been received or requested. This interrupt is enabled by setting the `DATAIM` bit in the **I<sup>2</sup>C Slave Interrupt Mask (I2CSIMR)** register. Software determines whether the module should write (transmit) or read (receive) data from the **I<sup>2</sup>C Slave Data (I2CSDR)** register, by checking the `RREQ` and `TREQ` bits of the **I<sup>2</sup>C Slave Control/Status (I2CCSR)** register. If the slave module is in receive mode and the first byte of a transfer is received, the `FBR` bit is set along with the `RREQ` bit. The interrupt is cleared by setting the `DATAIC` bit in the **I<sup>2</sup>C Slave Interrupt Clear (I2CSICR)** register.

In addition, the slave module can generate an interrupt when a start and stop condition is detected. These interrupts are enabled by setting the `STARTIM` and `STOPIM` bits of the **I<sup>2</sup>C Slave Interrupt Mask (I2CSIMR)** register and cleared by writing a 1 to the `STOPIC` and `STARTIC` bits of the **I<sup>2</sup>C Slave Interrupt Clear (I2CSICR)** register.

If the application doesn't require the use of interrupts, the raw interrupt status is always visible via the **I<sup>2</sup>C Slave Raw Interrupt Status (I2CSRIS)** register.

### 17.3.4 Loopback Operation

The I<sup>2</sup>C modules can be placed into an internal loopback mode for diagnostic or debug work by setting the `LPBK` bit in the **I<sup>2</sup>C Master Configuration (I2CMCR)** register. In loopback mode, the SDA and SCL signals from the master and slave modules are tied together.

### 17.3.5 Command Sequence Flow Charts

This section details the steps required to perform the various I<sup>2</sup>C transfer types in both master and slave mode.

#### 17.3.5.1 I<sup>2</sup>C Master Command Sequences

The figures that follow show the command sequences available for the I<sup>2</sup>C master.

Figure 17-7. Master Single TRANSMIT

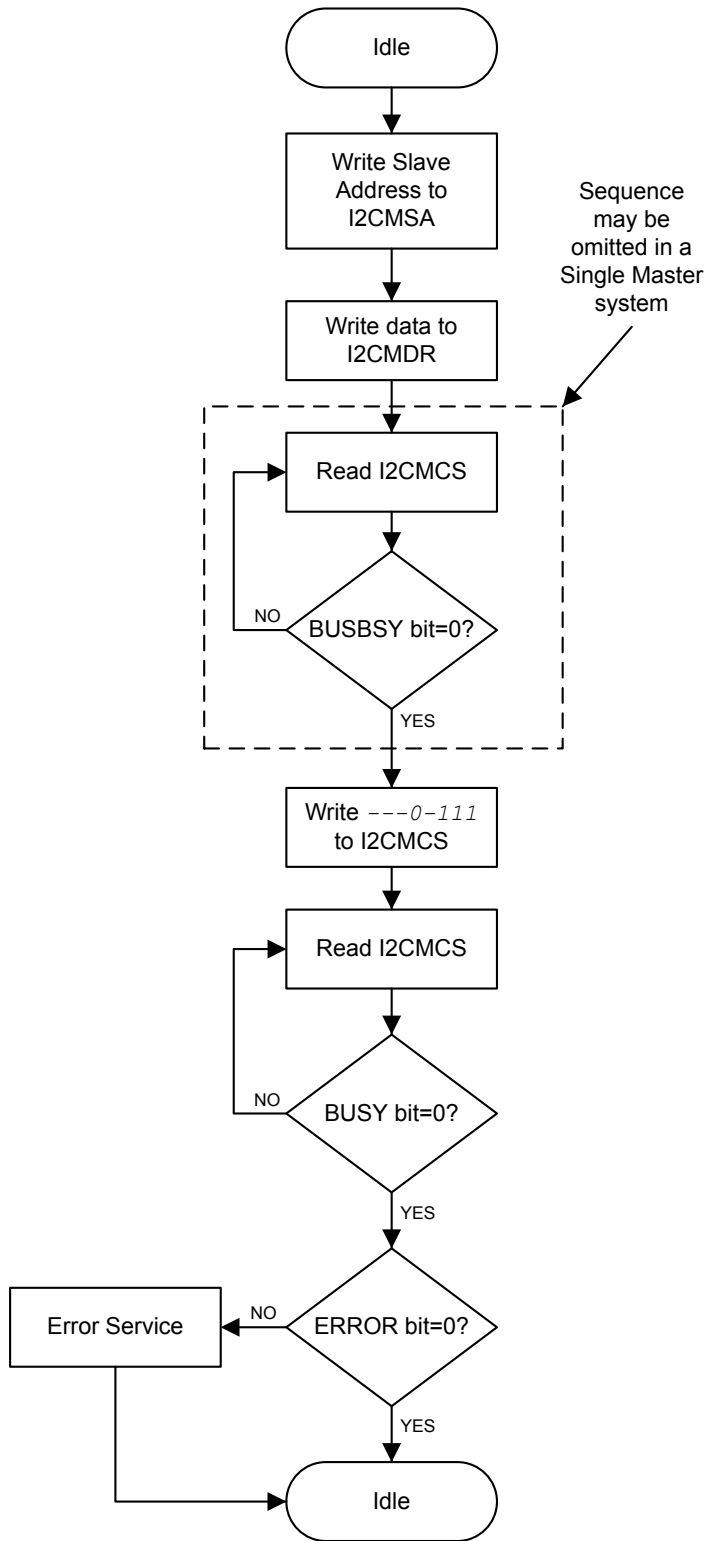


Figure 17-8. Master Single RECEIVE

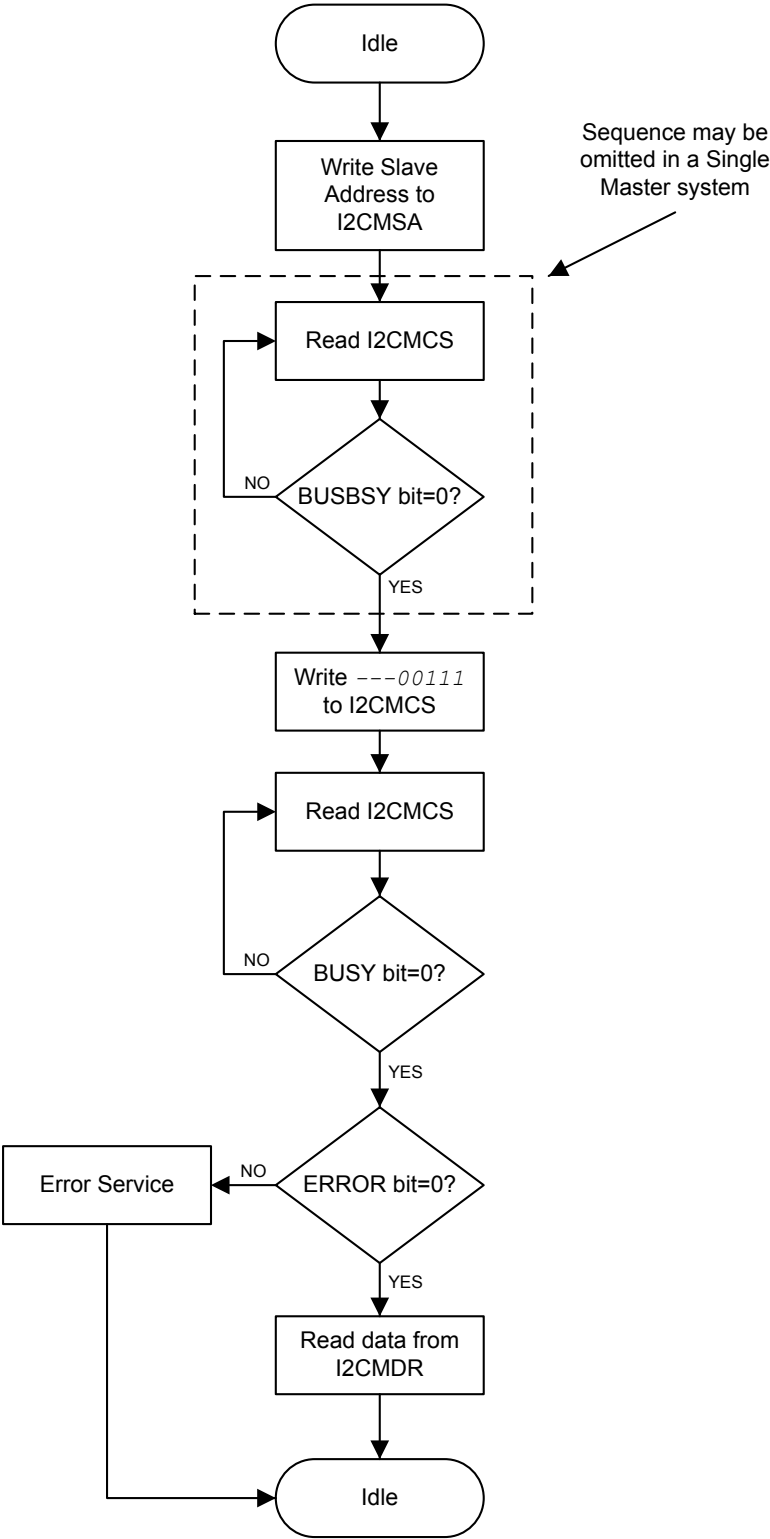


Figure 17-9. Master TRANSMIT with Repeated START

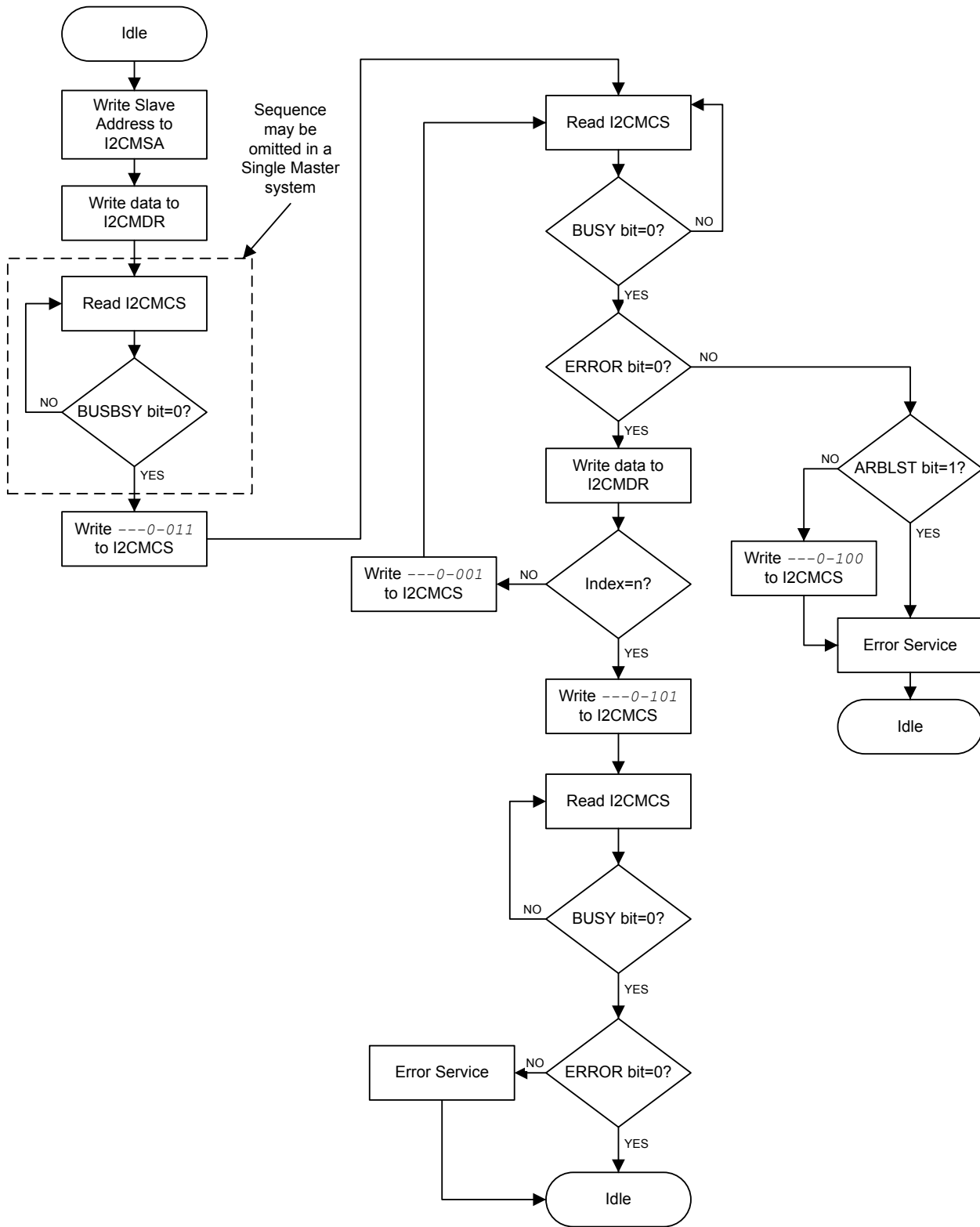


Figure 17-10. Master RECEIVE with Repeated START

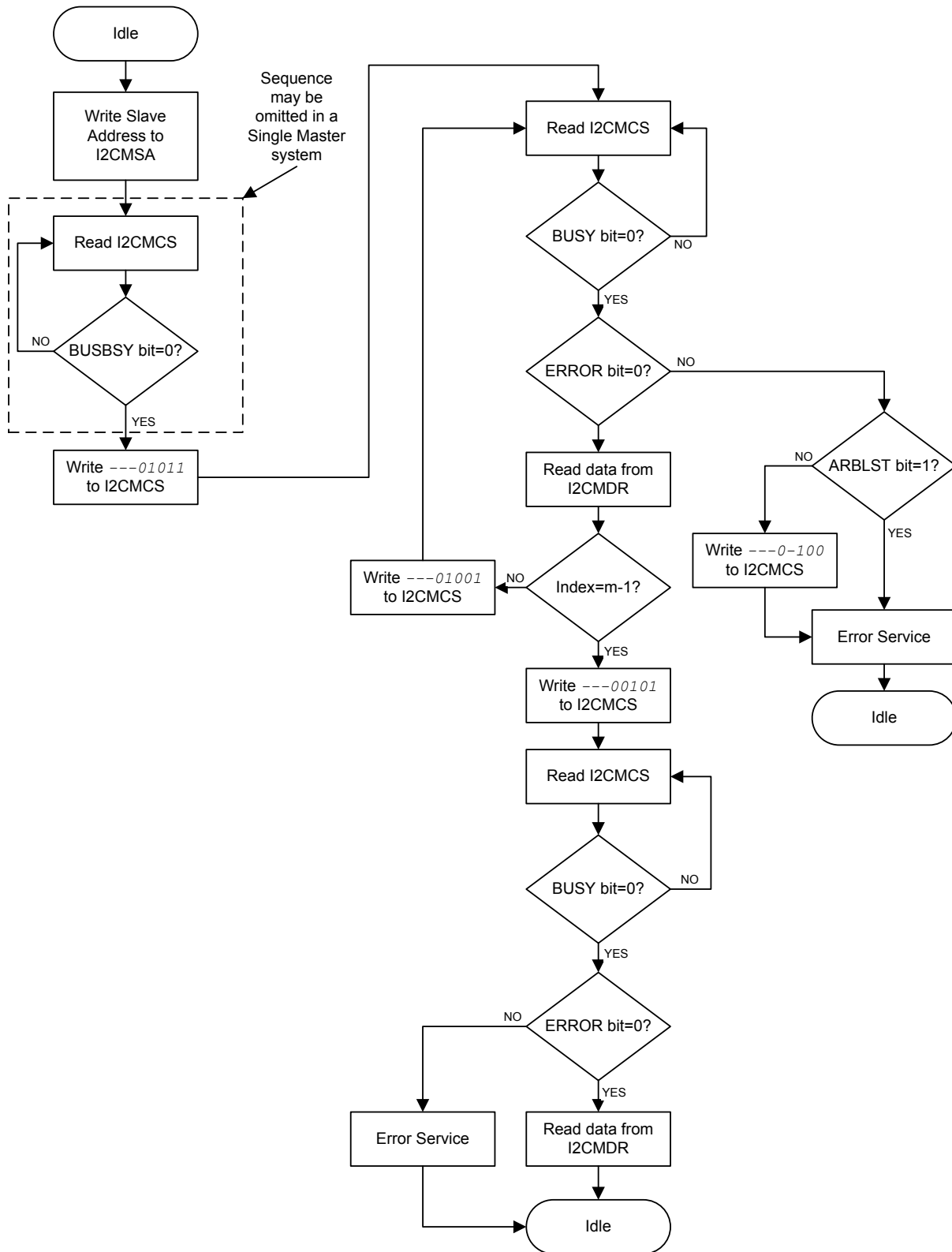
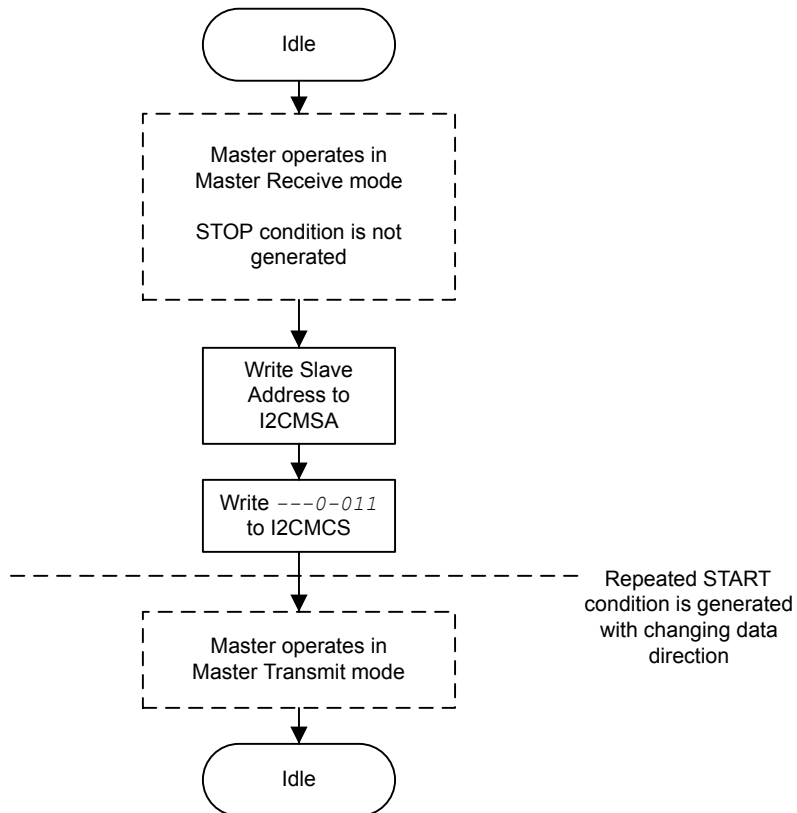


Figure 17-11. Master RECEIVE with Repeated START after TRANSMIT with Repeated START



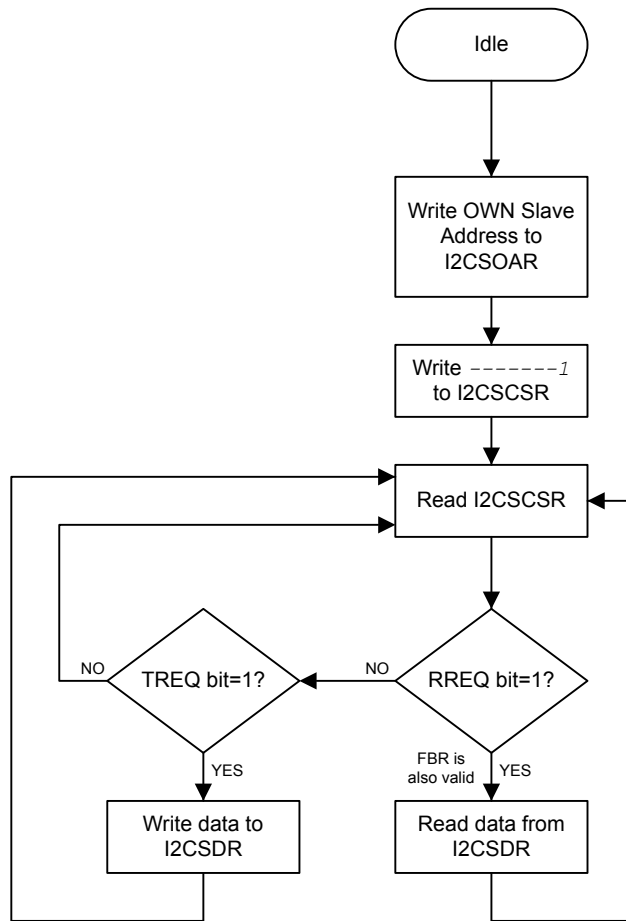
Figure 17-12. Master TRANSMIT with Repeated START after RECEIVE with Repeated START



### 17.3.5.2 I<sup>2</sup>C Slave Command Sequences

Figure 17-13 on page 664 presents the command sequence available for the I<sup>2</sup>C slave.

Figure 17-13. Slave Command Sequence



## 17.4 Initialization and Configuration

The following example shows how to configure the I<sup>2</sup>C module to transmit a single byte as a master. This assumes the system clock is 20 MHz.

1. Enable the I<sup>2</sup>C clock by writing a value of 0x0000.1000 to the **RCGC1** register in the System Control module (see page 149).
2. Enable the clock to the appropriate GPIO module via the **RCGC2** register in the System Control module (see page 158). To find out which GPIO port to enable, refer to Table 20-5 on page 722.
3. In the GPIO module, enable the appropriate pins for their alternate function using the **GPIOAFSEL** register (see page 310). To determine which GPIOs to configure, see Table 20-4 on page 717.
4. Enable the I<sup>2</sup>C pins for Open Drain operation. See page 315.
5. Configure the **PMC<sub>n</sub>** fields in the **GPIOPCTL** register to assign the I<sup>2</sup>C signals to the appropriate pins. See page 328 and Table 20-5 on page 722.
6. Initialize the I<sup>2</sup>C Master by writing the **I2CMCR** register with a value of 0x0000.0010.



7. Set the desired SCL clock speed of 100 Kbps by writing the **I2CMTPR** register with the correct value. The value written to the **I2CMTPR** register represents the number of system clock periods in one SCL clock period. The TPR value is determined by the following equation:

$$\text{TPR} = (\text{System Clock} / (2 * (\text{SCL\_LP} + \text{SCL\_HP}) * \text{SCL\_CLK})) - 1;$$

$$\text{TPR} = (20\text{MHz} / (2 * (6+4) * 100000)) - 1;$$

$$\text{TPR} = 9$$

Write the **I2CMTPR** register with the value of 0x0000.0009.

8. Specify the slave address of the master and that the next operation is a Transmit by writing the **I2CMSA** register with a value of 0x0000.0076. This sets the slave address to 0x3B.
9. Place data (byte) to be transmitted in the data register by writing the **I2CMDR** register with the desired data.
10. Initiate a single byte transmit of the data from Master to Slave by writing the **I2CMCS** register with a value of 0x0000.0007 (STOP, START, RUN).
11. Wait until the transmission completes by polling the **I2CMCS** register's **BUSBSY** bit until it has been cleared.

## 17.5 Register Map

Table 17-3 on page 665 lists the I<sup>2</sup>C registers. All addresses given are relative to the I<sup>2</sup>C base addresses for the master and slave:

- I<sup>2</sup>C Master 0: 0x4002.0000
- I<sup>2</sup>C Slave 0: 0x4002.0800
- I<sup>2</sup>C Master 1: 0x4002.1000
- I<sup>2</sup>C Slave 1: 0x4002.1800

Note that the I<sup>2</sup>C module clock must be enabled before the registers can be programmed (see page 149).

**Table 17-3. Inter-Integrated Circuit (I<sup>2</sup>C) Interface Register Map**

Offset	Name	Type	Reset	Description	See page
<b>I<sup>2</sup>C Master</b>					
0x000	I2CMSA	R/W	0x0000.0000	I2C Master Slave Address	667
0x004	I2CMCS	R/W	0x0000.0000	I2C Master Control/Status	668
0x008	I2CMDR	R/W	0x0000.0000	I2C Master Data	673
0x00C	I2CMTPR	R/W	0x0000.0001	I2C Master Timer Period	674
0x010	I2CMIMR	R/W	0x0000.0000	I2C Master Interrupt Mask	675
0x014	I2CMRIS	RO	0x0000.0000	I2C Master Raw Interrupt Status	676
0x018	I2CMMIS	RO	0x0000.0000	I2C Master Masked Interrupt Status	677
0x01C	I2CMICR	WO	0x0000.0000	I2C Master Interrupt Clear	678
0x020	I2CMCR	R/W	0x0000.0000	I2C Master Configuration	679

Table 17-3. Inter-Integrated Circuit (I<sup>2</sup>C) Interface Register Map (continued)

Offset	Name	Type	Reset	Description	See page
<b>I<sup>2</sup>C Slave</b>					
0x000	I2CSOAR	R/W	0x0000.0000	I2C Slave Own Address	680
0x004	I2CSCSR	RO	0x0000.0000	I2C Slave Control/Status	681
0x008	I2CSDR	R/W	0x0000.0000	I2C Slave Data	683
0x00C	I2CSIMR	R/W	0x0000.0000	I2C Slave Interrupt Mask	684
0x010	I2CSRIS	RO	0x0000.0000	I2C Slave Raw Interrupt Status	685
0x014	I2CSMIS	RO	0x0000.0000	I2C Slave Masked Interrupt Status	686
0x018	I2CSICR	WO	0x0000.0000	I2C Slave Interrupt Clear	687

## 17.6 Register Descriptions (I<sup>2</sup>C Master)

The remainder of this section lists and describes the I<sup>2</sup>C master registers, in numerical order by address offset. See also “Register Descriptions (I<sup>2</sup>C Slave)” on page 679.

## Register 1: I<sup>2</sup>C Master Slave Address (I2CMSA), offset 0x000

This register consists of eight bits: seven address bits (A6-A0), and a Receive/Send bit, which determines if the next operation is a Receive (High), or Transmit (Low).

### I2C Master Slave Address (I2CMSA)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x000

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								SA							R/S
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description						
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.						
7:1	SA	R/W	0x00	I <sup>2</sup> C Slave Address  This field specifies bits A6 through A0 of the slave address.						
0	R/S	R/W	0	Receive/Send  The R/S bit specifies if the next operation is a Receive (High) or Transmit (Low).  <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Transmit</td> </tr> <tr> <td>1</td> <td>Receive</td> </tr> </tbody> </table>	Value	Description	0	Transmit	1	Receive
Value	Description									
0	Transmit									
1	Receive									

## Register 2: I<sup>2</sup>C Master Control/Status (I2CMCS), offset 0x004

This register accesses seven status bits when read and four control bits when written.

The status register consists of seven bits, which when read determine the state of the I<sup>2</sup>C bus controller.

The control register consists of four bits: the RUN, START, STOP, and ACK bits. The START bit generates the START or REPEATED START condition.

The STOP bit determines if the cycle stops at the end of the data cycle or continues on to a repeated START condition. To generate a single transmit cycle, the **I<sup>2</sup>C Master Slave Address (I2CMSA)** register is written with the desired address, the R/S bit is cleared, and the Control register is written with ACK=X (0 or 1), STOP=1, START=1, and RUN=1 to perform the operation and stop. When the operation is completed (or aborted due an error), the interrupt pin becomes active and the data may be read from the **I2CMDR** register. When the I<sup>2</sup>C module operates in Master receiver mode, the ACK bit is normally set causing the I<sup>2</sup>C bus controller to transmit an acknowledge automatically after each byte. This bit must be cleared when the I<sup>2</sup>C bus controller requires no further data to be transmitted from the slave transmitter.

### Read-Only Status Register

#### I2C Master Control/Status (I2CMCS)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x004

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved										BUSBSY	IDLE	ARBLST	DATACK	ADRACK	ERROR	BUSY
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

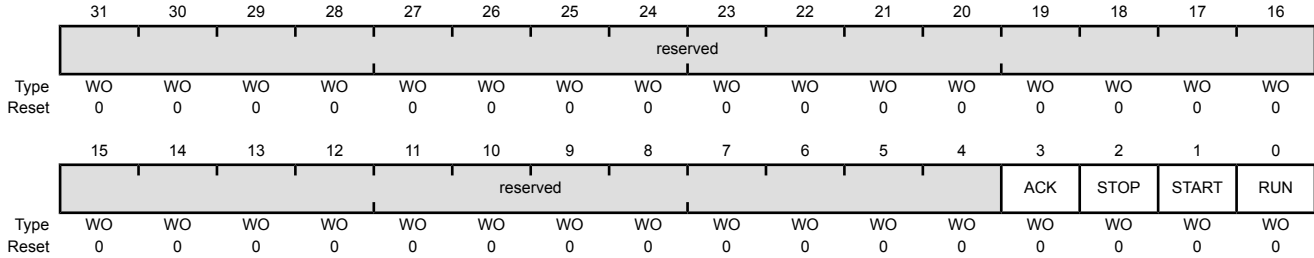
Bit/Field	Name	Type	Reset	Description
31:7	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6	BUSBSY	RO	0	<p>Bus Busy</p> <p>Value Description</p> <p>0 The I<sup>2</sup>C bus is idle.</p> <p>1 The I<sup>2</sup>C bus is busy.</p> <p>The bit changes based on the START and STOP conditions.</p>
5	IDLE	RO	0	<p>I<sup>2</sup>C Idle</p> <p>Value Description</p> <p>0 The I<sup>2</sup>C controller is not idle.</p> <p>1 The I<sup>2</sup>C controller is idle.</p>

Bit/Field	Name	Type	Reset	Description
4	ARBLST	RO	0	Arbitration Lost  Value Description 0 The I <sup>2</sup> C controller won arbitration. 1 The I <sup>2</sup> C controller lost arbitration.
3	DATAACK	RO	0	Acknowledge Data  Value Description 0 The transmitted data was acknowledged 1 The transmitted data was not acknowledged.
2	ADRACK	RO	0	Acknowledge Address  Value Description 0 The transmitted address was acknowledged 1 The transmitted address was not acknowledged.
1	ERROR	RO	0	Error  Value Description 0 No error was detected on the last operation. 1 An error occurred on the last operation.  The error can be from the slave address not being acknowledged, the transmit data not being acknowledged, or because the controller lost arbitration.
0	BUSY	RO	0	I <sup>2</sup> C Busy  Value Description 0 The controller is idle. 1 The controller is busy.  When the <code>BUSY</code> bit is set, the other status bits are not valid.

**Write-Only Control Register**

I<sup>2</sup>C Master Control/Status (I2CMCS)

I<sup>2</sup>C Master 0 base: 0x4002.0000  
 I<sup>2</sup>C Master 1 base: 0x4002.1000  
 Offset 0x004  
 Type WO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:4	reserved	WO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3	ACK	WO	0	Data Acknowledge Enable  Value Description 0 The received data byte is not acknowledged automatically by the master. 1 The received data byte is acknowledged automatically by the master. See field decoding in Table 17-4 on page 671.
2	STOP	WO	0	Generate STOP  Value Description 0 The controller does not generate the STOP condition. 1 The controller generates the STOP condition. See field decoding in Table 17-4 on page 671.
1	START	WO	0	Generate START  Value Description 0 The controller does not generate the START condition. 1 The controller generates the START or repeated START condition. See field decoding in Table 17-4 on page 671.
0	RUN	WO	0	I <sup>2</sup> C Master Enable  Value Description 0 The master is disabled. 1 The master is enabled to transmit or receive data. See field decoding in Table 17-4 on page 671.

Table 17-4. Write Field Decoding for I2CMCS[3:0] Field

Current State	I2CMSA[0]	I2CMCS[3:0]				Description
	R/S	ACK	STOP	START	RUN	
Idle	0	X <sup>a</sup>	0	1	1	START condition followed by TRANSMIT (master goes to the Master Transmit state).
	0	X	1	1	1	START condition followed by a TRANSMIT and STOP condition (master remains in Idle state).
	1	0	0	1	1	START condition followed by RECEIVE operation with negative ACK (master goes to the Master Receive state).
	1	0	1	1	1	START condition followed by RECEIVE and STOP condition (master remains in Idle state).
	1	1	0	1	1	START condition followed by RECEIVE (master goes to the Master Receive state).
	1	1	1	1	1	Illegal
	All other combinations not listed are non-operations.					NOP
Master Transmit	X	X	0	0	1	TRANSMIT operation (master remains in Master Transmit state).
	X	X	1	0	0	STOP condition (master goes to Idle state).
	X	X	1	0	1	TRANSMIT followed by STOP condition (master goes to Idle state).
	0	X	0	1	1	Repeated START condition followed by a TRANSMIT (master remains in Master Transmit state).
	0	X	1	1	1	Repeated START condition followed by TRANSMIT and STOP condition (master goes to Idle state).
	1	0	0	1	1	Repeated START condition followed by a RECEIVE operation with a negative ACK (master goes to Master Receive state).
	1	0	1	1	1	Repeated START condition followed by a TRANSMIT and STOP condition (master goes to Idle state).
	1	1	0	1	1	Repeated START condition followed by RECEIVE (master goes to Master Receive state).
	1	1	1	1	1	Illegal.
All other combinations not listed are non-operations.					NOP.	

Table 17-4. Write Field Decoding for I2CMCS[3:0] Field (continued)

Current State	I2CMSA[0]	I2CMCS[3:0]				Description
	R/S	ACK	STOP	START	RUN	
Master Receive	X	0	0	0	1	RECEIVE operation with negative ACK (master remains in Master Receive state).
	X	X	1	0	0	STOP condition (master goes to Idle state). <sup>b</sup>
	X	0	1	0	1	RECEIVE followed by STOP condition (master goes to Idle state).
	X	1	0	0	1	RECEIVE operation (master remains in Master Receive state).
	X	1	1	0	1	Illegal.
	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with a negative ACK (master remains in Master Receive state).
	1	0	1	1	1	Repeated START condition followed by RECEIVE and STOP condition (master goes to Idle state).
	1	1	0	1	1	Repeated START condition followed by RECEIVE (master remains in Master Receive state).
	0	X	0	1	1	Repeated START condition followed by TRANSMIT (master goes to Master Transmit state).
	0	X	1	1	1	Repeated START condition followed by TRANSMIT and STOP condition (master goes to Idle state).
	All other combinations not listed are non-operations.					

a. An X in a table cell indicates the bit can be 0 or 1.

b. In Master Receive mode, a STOP condition should be generated only after a Data Negative Acknowledge executed by the master or an Address Negative Acknowledge executed by the slave.



### Register 3: I<sup>2</sup>C Master Data (I2CMDR), offset 0x008

**Important:** Use caution when reading this register. Performing a read may change bit status.

This register contains the data to be transmitted when in the Master Transmit state and the data received when in the Master Receive state.

#### I2C Master Data (I2CMDR)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x008

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DATA							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DATA	R/W	0x00	Data Transferred Data transferred during transaction.

## Register 4: I<sup>2</sup>C Master Timer Period (I2CMTPR), offset 0x00C

This register specifies the period of the SCL clock.

### I2C Master Timer Period (I2CMTPR)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x00C

Type R/W, reset 0x0000.0001

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								TPR							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	TPR	R/W	0x1	SCL Clock Period

This field specifies the period of the SCL clock.

$$SCL\_PRD = 2 \times (1 + TPR) \times (SCL\_LP + SCL\_HP) \times CLK\_PRD$$

where:

*SCL\_PRD* is the SCL line period (I<sup>2</sup>C clock).

*TPR* is the Timer Period register value (range of 1 to 255).

*SCL\_LP* is the SCL Low period (fixed at 6).

*SCL\_HP* is the SCL High period (fixed at 4).

*CLK\_PRD* is the system clock period in ns.

## Register 5: I<sup>2</sup>C Master Interrupt Mask (I2CMIMR), offset 0x010

This register controls whether a raw interrupt is promoted to a controller interrupt.

### I2C Master Interrupt Mask (I2CMIMR)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x010

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															IM
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	IM	R/W	0	Interrupt Mask
				Value Description
				1 The master interrupt is sent to the interrupt controller when the <b>RIS</b> bit in the <b>I2CMRIS</b> register is set.
				0 The <b>RIS</b> interrupt is suppressed and not sent to the interrupt controller.

## Register 6: I<sup>2</sup>C Master Raw Interrupt Status (I2CMRIS), offset 0x014

This register specifies whether an interrupt is pending.

### I2C Master Raw Interrupt Status (I2CMRIS)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x014

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															RIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	RIS	RO	0	Raw Interrupt Status

Value Description

1	A master interrupt is pending.
0	No interrupt.

This bit is cleared by writing a 1 to the IC bit in the I2CMICR register.

## Register 7: I<sup>2</sup>C Master Masked Interrupt Status (I2CMMIS), offset 0x018

This register specifies whether an interrupt was signaled.

### I2C Master Masked Interrupt Status (I2CMMIS)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x018

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved															MIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	MIS	RO	0	Masked Interrupt Status

#### Value Description

1	An unmasked master interrupt was signaled is pending.
0	An interrupt has not occurred or is masked.

This bit is cleared by writing a 1 to the IC bit in the I2CMICR register.

## Register 8: I<sup>2</sup>C Master Interrupt Clear (I2CMICR), offset 0x01C

This register clears the raw interrupt.

### I2C Master Interrupt Clear (I2CMICR)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x01C

Type WO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															IC	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	IC	WO	0	<p>Interrupt Clear</p> <p>Writing a 1 to this bit clears the <b>RIS</b> bit in the <b>I2CMRIS</b> register and the <b>MIS</b> bit in the <b>I2CMMIS</b> register.</p> <p>A read of this register returns no meaningful data.</p>

## Register 9: I<sup>2</sup>C Master Configuration (I2CMCR), offset 0x020

This register configures the mode (Master or Slave) and sets the interface for test mode loopback.

### I2C Master Configuration (I2CMCR)

I2C Master 0 base: 0x4002.0000

I2C Master 1 base: 0x4002.1000

Offset 0x020

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved											SFE	MFE	reserved		LPBK	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:6	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
5	SFE	R/W	0	I <sup>2</sup> C Slave Function Enable  Value Description 1 Slave mode is enabled. 0 Slave mode is disabled.
4	MFE	R/W	0	I <sup>2</sup> C Master Function Enable  Value Description 1 Master mode is enabled. 0 Master mode is disabled.
3:1	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0	LPBK	R/W	0	I <sup>2</sup> C Loopback  Value Description 1 The controller in a test mode loopback configuration. 0 Normal operation.

## 17.7 Register Descriptions (I<sup>2</sup>C Slave)

The remainder of this section lists and describes the I<sup>2</sup>C slave registers, in numerical order by address offset. See also "Register Descriptions (I<sup>2</sup>C Master)" on page 666.

### Register 10: I<sup>2</sup>C Slave Own Address (I2CSOAR), offset 0x000

This register consists of seven address bits that identify the Stellaris<sup>®</sup> I<sup>2</sup>C device on the I<sup>2</sup>C bus.

#### I2C Slave Own Address (I2CSOAR)

I2C Slave 0 base: 0x4002.0800

I2C Slave 1 base: 0x4002.1800

Offset 0x000

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved									OAR						
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:7	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
6:0	OAR	R/W	0x00	I <sup>2</sup> C Slave Own Address This field specifies bits A6 through A0 of the slave address.



## Register 11: I<sup>2</sup>C Slave Control/Status (I2CSCSR), offset 0x004

This register accesses one control bit when written, and three status bits when read.

The read-only Status register consists of three bits: the FBR, RREQ, and TREQ bits. The First Byte Received (FBR) bit is set only after the Stellaris® device detects its own slave address and receives the first data byte from the I<sup>2</sup>C master. The Receive Request (RREQ) bit indicates that the Stellaris® I<sup>2</sup>C device has received a data byte from an I<sup>2</sup>C master. Read one data byte from the **I<sup>2</sup>C Slave Data (I2CSDR)** register to clear the RREQ bit. The Transmit Request (TREQ) bit indicates that the Stellaris® I<sup>2</sup>C device is addressed as a Slave Transmitter. Write one data byte into the **I<sup>2</sup>C Slave Data (I2CSDR)** register to clear the TREQ bit.

The write-only Control register consists of one bit: the DA bit. The DA bit enables and disables the Stellaris® I<sup>2</sup>C slave operation.

### Read-Only Status Register

#### I2C Slave Control/Status (I2CSCSR)

I2C Slave 0 base: 0x4002.0800

I2C Slave 1 base: 0x4002.1800

Offset 0x004

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													FBR	TREQ	RREQ
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	FBR	RO	0	<p>First Byte Received</p> <p>Value Description</p> <p>1 The first byte following the slave's own address has been received.</p> <p>0 The first byte has not been received.</p> <p>This bit is only valid when the RREQ bit is set and is automatically cleared when data has been read from the I2CSDR register.</p> <p><b>Note:</b> This bit is not used for slave transmit operations.</p>
1	TREQ	RO	0	<p>Transmit Request</p> <p>Value Description</p> <p>1 The I<sup>2</sup>C controller has been addressed as a slave transmitter and is using clock stretching to delay the master until data has been written to the I2CSDR register.</p> <p>0 No outstanding transmit request.</p>

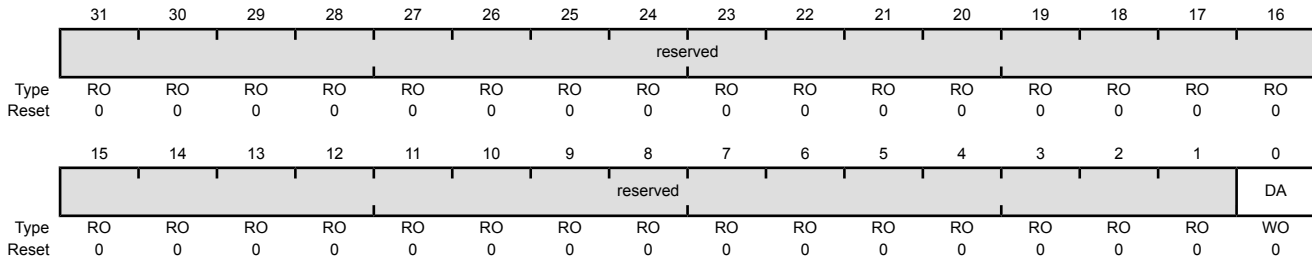
Bit/Field	Name	Type	Reset	Description
0	RREQ	RO	0	Receive Request

Value	Description
1	The I <sup>2</sup> C controller has outstanding receive data from the I <sup>2</sup> C master and is using clock stretching to delay the master until the data has been read from the <b>I2CSDR</b> register.
0	No outstanding receive data.

### Write-Only Control Register

#### I2C Slave Control/Status (I2CSCSR)

I2C Slave 0 base: 0x4002.0800  
 I2C Slave 1 base: 0x4002.1800  
 Offset 0x004  
 Type WO, reset 0x0000.0000



Bit/Field	Name	Type	Reset	Description
31:1	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

0	DA	WO	0	Device Active
---	----	----	---	---------------

Value	Description
0	Disables the I <sup>2</sup> C slave operation.
1	Enables the I <sup>2</sup> C slave operation.

## Register 12: I<sup>2</sup>C Slave Data (I2CSDR), offset 0x008

**Important:** Use caution when reading this register. Performing a read may change bit status.

This register contains the data to be transmitted when in the Slave Transmit state, and the data received when in the Slave Receive state.

### I2C Slave Data (I2CSDR)

I2C Slave 0 base: 0x4002.0800

I2C Slave 1 base: 0x4002.1800

Offset 0x008

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved								DATA							
Type	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:8	reserved	RO	0x0000.00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7:0	DATA	R/W	0x00	Data for Transfer  This field contains the data for transfer during a slave receive or transmit operation.

### Register 13: I<sup>2</sup>C Slave Interrupt Mask (I2CSIMR), offset 0x00C

This register controls whether a raw interrupt is promoted to a controller interrupt.

#### I2C Slave Interrupt Mask (I2CSIMR)

I2C Slave 0 base: 0x4002.0800

I2C Slave 1 base: 0x4002.1800

Offset 0x00C

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													STOPIM	STARTIM	DATAIM
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	STOPIM	RO	0	Stop Condition Interrupt Mask  Value Description 1 The STOP condition interrupt is sent to the interrupt controller when the STOPRIS bit in the I2CSRIS register is set. 0 The STOPRIS interrupt is suppressed and not sent to the interrupt controller.
1	STARTIM	RO	0	Start Condition Interrupt Mask  Value Description 1 The START condition interrupt is sent to the interrupt controller when the STARTRIS bit in the I2CSRIS register is set. 0 The STARTRIS interrupt is suppressed and not sent to the interrupt controller.
0	DATAIM	R/W	0	Data Interrupt Mask  Value Description 1 The data received or data requested interrupt is sent to the interrupt controller when the DATARIS bit in the I2CSRIS register is set. 0 The DATARIS interrupt is suppressed and not sent to the interrupt controller.

## Register 14: I<sup>2</sup>C Slave Raw Interrupt Status (I2CSRIS), offset 0x010

This register specifies whether an interrupt is pending.

### I2C Slave Raw Interrupt Status (I2CSRIS)

I2C Slave 0 base: 0x4002.0800

I2C Slave 1 base: 0x4002.1800

Offset 0x010

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved													STOPRIS	STARTRIS	DATARIS
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	STOPRIS	RO	0	<p>Stop Condition Raw Interrupt Status</p> <p>Value Description</p> <p>1 A STOP condition interrupt is pending.</p> <p>0 No interrupt.</p> <p>This bit is cleared by writing a 1 to the STOPIC bit in the I2CSICR register.</p>
1	STARTRIS	RO	0	<p>Start Condition Raw Interrupt Status</p> <p>Value Description</p> <p>1 A START condition interrupt is pending.</p> <p>0 No interrupt.</p> <p>This bit is cleared by writing a 1 to the STARTIC bit in the I2CSICR register.</p>
0	DATARIS	RO	0	<p>Data Raw Interrupt Status</p> <p>Value Description</p> <p>1 A data received or data requested interrupt is pending.</p> <p>0 No interrupt.</p> <p>This bit is cleared by writing a 1 to the DATAIC bit in the I2CSICR register.</p>

## Register 15: I<sup>2</sup>C Slave Masked Interrupt Status (I2CSMIS), offset 0x014

This register specifies whether an interrupt was signaled.

### I2C Slave Masked Interrupt Status (I2CSMIS)

I2C Slave 0 base: 0x4002.0800

I2C Slave 1 base: 0x4002.1800

Offset 0x014

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													STOPMIS	STARTMIS	DATAMIS	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	STOPMIS	R/W	0	<p>Stop Condition Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked STOP condition interrupt was signaled is pending.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the STOPIC bit in the I2CSICR register.</p>
1	STARTMIS	R/W	0	<p>Start Condition Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked START condition interrupt was signaled is pending.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the STARTIC bit in the I2CSICR register.</p>
0	DATAMIS	RO	0	<p>Data Masked Interrupt Status</p> <p>Value Description</p> <p>1 An unmasked data received or data requested interrupt was signaled is pending.</p> <p>0 An interrupt has not occurred or is masked.</p> <p>This bit is cleared by writing a 1 to the DATAIC bit in the I2CSICR register.</p>

## Register 16: I<sup>2</sup>C Slave Interrupt Clear (I2CSICR), offset 0x018

This register clears the raw interrupt. A read of this register returns no meaningful data.

### I2C Slave Interrupt Clear (I2CSICR)

I2C Slave 0 base: 0x4002.0800

I2C Slave 1 base: 0x4002.1800

Offset 0x018

Type WO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved													STOPIC	STARTIC	DATAIC	
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:3	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
2	STOPIC	WO	0	Stop Condition Interrupt Clear  Writing a 1 to this bit clears the <i>STOPRIS</i> bit in the <b>I2CSRIS</b> register and the <i>STOPMIS</i> bit in the <b>I2CSMIS</b> register.  A read of this register returns no meaningful data.
1	STARTIC	WO	0	Start Condition Interrupt Clear  Writing a 1 to this bit clears the <i>STOPRIS</i> bit in the <b>I2CSRIS</b> register and the <i>STOPMIS</i> bit in the <b>I2CSMIS</b> register.  A read of this register returns no meaningful data.
0	DATAIC	WO	0	Data Interrupt Clear  Writing a 1 to this bit clears the <i>STOPRIS</i> bit in the <b>I2CSRIS</b> register and the <i>STOPMIS</i> bit in the <b>I2CSMIS</b> register.  A read of this register returns no meaningful data.

## 18 Analog Comparators

An analog comparator is a peripheral that compares two analog voltages and provides a logical output that signals the comparison result.

**Note:** Not all comparators have the option to drive an output pin.

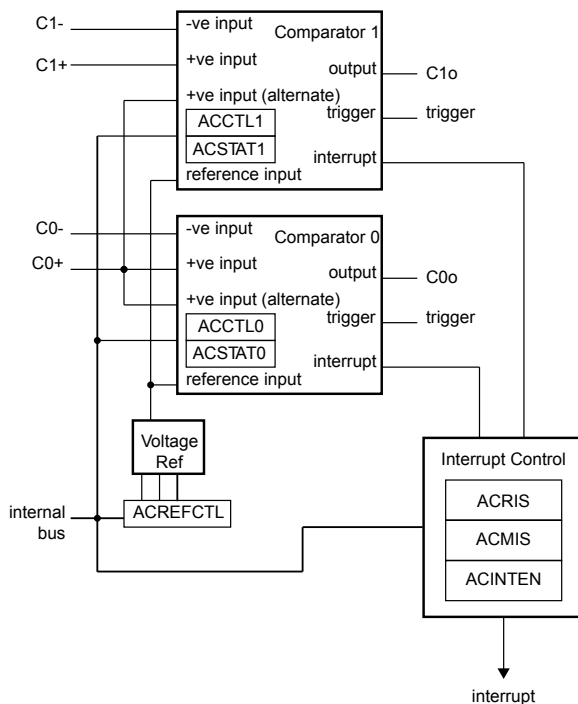
The comparator can provide its output to a device pin, acting as a replacement for an analog comparator on the board. In addition, the comparator can signal the application via interrupts or trigger the start of a sample sequence in the ADC. The interrupt generation and ADC triggering logic is separate and independent. This flexibility means, for example, that an interrupt can be generated on a rising edge and the ADC triggered on a falling edge.

The Stellaris<sup>®</sup> LM3S1811 microcontroller provides two independent integrated analog comparators with the following functions:

- Compare external pin input to external pin input or to internal programmable voltage reference
- Compare a test voltage against any one of the following voltages:
  - An individual external reference voltage
  - A shared single external reference voltage
  - A shared internal reference voltage

### 18.1 Block Diagram

Figure 18-1. Analog Comparator Module Block Diagram





## 18.2 Signal Description

Table 18-1 on page 689 lists the external signals of the Analog Comparators and describes the function of each. The Analog Comparator output signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for the Analog Comparator signals. The **AFSEL** bit in the **GPIO Alternate Function Select (GPIOAFSEL)** register (page 310) should be set to choose the Analog Comparator function. The number in parentheses is the encoding that must be programmed into the **PMC<sub>n</sub>** field in the **GPIO Port Control (GPIOCTL)** register (page 328) to assign the Analog Comparator signal to the specified GPIO port pin. The positive and negative input signals are configured by clearing the **DEN** bit in the **GPIO Digital Enable (GPIODEN)** register. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 288.

**Table 18-1. Signals for Analog Comparators**

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
C0+	90	PB6	I	Analog	Analog comparator 0 positive input.
C0-	92	PB4	I	Analog	Analog comparator 0 negative input.
C0o	24 58 90 91 100	PC5 (3) PF4 (2) PB6 (3) PB5 (1) PD7 (2)	O	TTL	Analog comparator 0 output.
C1+	24	PC5	I	Analog	Analog comparator 1 positive input.
C1-	91	PB5	I	Analog	Analog comparator 1 negative input.
C1o	2 22 24 46 84	PE6 (2) PC7 (7) PC5 (2) PF5 (2) PH2 (2)	O	TTL	Analog comparator 1 output.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

## 18.3 Functional Description

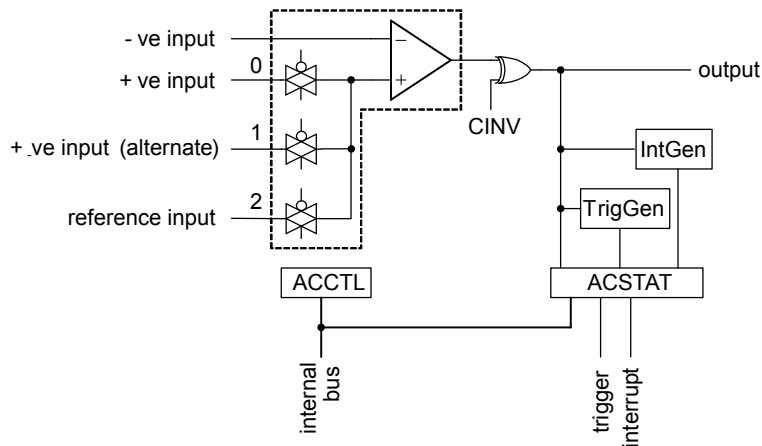
The comparator compares the VIN- and VIN+ inputs to produce an output, VOUT.

$$VIN- < VIN+, VOUT = 1$$

$$VIN- > VIN+, VOUT = 0$$

As shown in Figure 18-2 on page 690, the input source for VIN- is an external input, C<sub>n-</sub>. In addition to an external input, C<sub>n+</sub>, input sources for VIN+ can be the C0+ or an internal reference, V<sub>REF</sub>.

**Figure 18-2. Structure of Comparator Unit**



A comparator is configured through two status/control registers, **Analog Comparator Control (ACCTL)** and **Analog Comparator Status (ACSTAT)**. The internal reference is configured through one control register, **Analog Comparator Reference Voltage Control (ACREFCTL)**. Interrupt status and control are configured through three registers, **Analog Comparator Masked Interrupt Status (ACMIS)**, **Analog Comparator Raw Interrupt Status (ACRIS)**, and **Analog Comparator Interrupt Enable (ACINTEN)**.

Typically, the comparator output is used internally to generate an interrupt as controlled by the `ISEN` bit in the **ACCTL** register. The output may also be used to drive an external pin, `Co` or generate an analog-to-digital converter (ADC) trigger.

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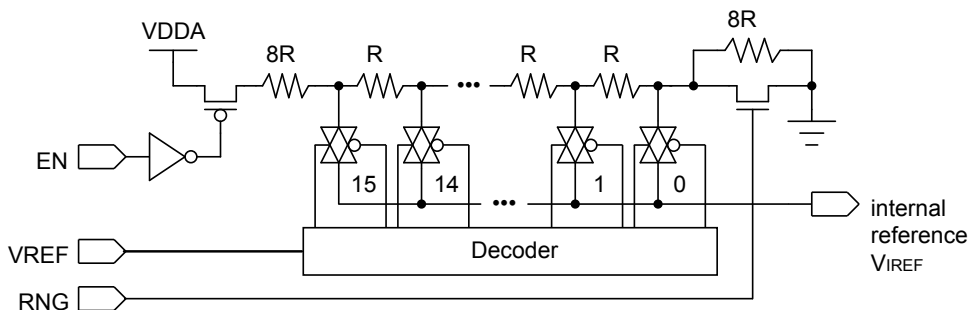
**Important:** The `ASRCP` bits in the **ACCTL** register must be set before using the analog comparators.

---

### 18.3.1 Internal Reference Programming

The structure of the internal reference is shown in Figure 18-3 on page 690. The internal reference is controlled by a single configuration register (**ACREFCTL**). Table 18-2 on page 691 shows the programming options to develop specific internal reference values, to compare an external voltage against a particular voltage generated internally ( $V_{IREF}$ ).

**Figure 18-3. Comparator Internal Reference Structure**



**Table 18-2. Internal Reference Voltage and ACREFACTL Field Values**

ACREFACTL Register		Output Reference Voltage Based on VREF Field Value
EN Bit Value	RNG Bit Value	
EN=0	RNG=X	0 V (GND) for any value of VREF; however, it is recommended that RNG=1 and VREF=0 for the least noisy ground reference.
EN=1	RNG=0	<p>Total resistance in ladder is 31 R.</p> $V_{IREF} = V_{DDA} \times \frac{RV_{REF}}{R_T}$ $V_{IREF} = V_{DDA} \times \frac{(V_{REF} + 8)}{31}$ $V_{IREF} = 0.85 + 0.106 \times V_{REF}$ <p>The range of internal reference in this mode is 0.85-2.448 V.</p>
	RNG=1	<p>Total resistance in ladder is 23 R.</p> $V_{IREF} = V_{DDA} \times \frac{RV_{REF}}{R_T}$ $V_{IREF} = V_{DDA} \times \frac{V_{REF}}{23}$ $V_{IREF} = 0.143 \times V_{REF}$ <p>The range of internal reference for this mode is 0-2.152 V.</p>

## 18.4 Initialization and Configuration

The following example shows how to configure an analog comparator to read back its output value from an internal register.

1. Enable the analog comparator 0 clock by writing a value of 0x0010.0000 to the **RCGC1** register in the System Control module (see page 149).
2. In the GPIO module, enable the GPIO port/pin associated with the input signals as GPIO inputs. To determine which GPIO to configure, see Table 20-4 on page 717.
3. Configure the **PMCn** fields in the **GPIOCTL** register to assign the analog comparator output signals to the appropriate pins (see page 328 and Table 20-5 on page 722).

4. Configure the internal voltage reference to 1.65 V by writing the **ACREFCTL** register with the value 0x0000.030C.
5. Configure the comparator to use the internal voltage reference and to *not* invert the output by writing the **ACCTLn** register with the value of 0x0000.040C.
6. Delay for 10  $\mu$ s.
7. Read the comparator output value by reading the **ACSTATn** register's **OVAL** value.

Change the level of the comparator negative input signal C<sup>-</sup> to see the **OVAL** value change.

## 18.5 Register Map

Table 18-3 on page 692 lists the comparator registers. The offset listed is a hexadecimal increment to the register's address, relative to the Analog Comparator base address of 0x4003.C000. Note that the analog comparator clock must be enabled before the registers can be programmed (see page 149).

**Table 18-3. Analog Comparators Register Map**

Offset	Name	Type	Reset	Description	See page
0x000	ACMIS	R/W1C	0x0000.0000	Analog Comparator Masked Interrupt Status	693
0x004	ACRIS	RO	0x0000.0000	Analog Comparator Raw Interrupt Status	694
0x008	ACINTEN	R/W	0x0000.0000	Analog Comparator Interrupt Enable	695
0x010	ACREFCTL	R/W	0x0000.0000	Analog Comparator Reference Voltage Control	696
0x020	ACSTAT0	RO	0x0000.0000	Analog Comparator Status 0	697
0x024	ACCTL0	R/W	0x0000.0000	Analog Comparator Control 0	698
0x040	ACSTAT1	RO	0x0000.0000	Analog Comparator Status 1	697
0x044	ACCTL1	R/W	0x0000.0000	Analog Comparator Control 1	698

## 18.6 Register Descriptions

The remainder of this section lists and describes the Analog Comparator registers, in numerical order by address offset.

**Register 1: Analog Comparator Masked Interrupt Status (ACMIS), offset 0x000**

This register provides a summary of the interrupt status (masked) of the comparator.

**Analog Comparator Masked Interrupt Status (ACMIS)**

Base 0x4003.C000

Offset 0x000

Type R/W1C, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															IN1	IN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	IN1	R/W1C	0	<p>Comparator 1 Masked Interrupt Status</p> <p><b>Value Description</b></p> <p>1 The <b>IN1</b> bits in the <b>ACRIS</b> register and the <b>ACINTEN</b> registers are set, providing an interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1. Clearing this bit also clears the <b>IN1</b> bit in the <b>ACRIS</b> register.</p>
0	IN0	R/W1C	0	<p>Comparator 0 Masked Interrupt Status</p> <p><b>Value Description</b></p> <p>1 The <b>IN0</b> bits in the <b>ACRIS</b> register and the <b>ACINTEN</b> registers are set, providing an interrupt to the interrupt controller.</p> <p>0 No interrupt has occurred or the interrupt is masked.</p> <p>This bit is cleared by writing a 1. Clearing this bit also clears the <b>IN0</b> bit in the <b>ACRIS</b> register.</p>

## Register 2: Analog Comparator Raw Interrupt Status (ACRIS), offset 0x004

This register provides a summary of the interrupt status (raw) of the comparator. The bits in this register must be enabled to generate interrupts using the **ACINTEN** register.

### Analog Comparator Raw Interrupt Status (ACRIS)

Base 0x4003.C000  
 Offset 0x004  
 Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															IN1	IN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	IN1	RO	0	<p>Comparator 1 Interrupt Status</p> <p>Value Description</p> <p>1 Comparator 1 has generated an interrupt for an event as configured by the <b>ISEN</b> bit in the <b>ACCTL1</b> register.</p> <p>0 An interrupt has not occurred.</p> <p>This bit is cleared by writing a 1 to the <b>IN1</b> bit in the <b>ACMIS</b> register.</p>
0	IN0	RO	0	<p>Comparator 0 Interrupt Status</p> <p>Value Description</p> <p>1 Comparator 0 has generated an interrupt for an event as configured by the <b>ISEN</b> bit in the <b>ACCTL0</b> register.</p> <p>0 An interrupt has not occurred.</p> <p>This bit is cleared by writing a 1 to the <b>IN0</b> bit in the <b>ACMIS</b> register.</p>

**Register 3: Analog Comparator Interrupt Enable (ACINTEN), offset 0x008**

This register provides the interrupt enable for the comparators.

**Analog Comparator Interrupt Enable (ACINTEN)**

Base 0x4003.C000

Offset 0x008

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															IN1	IN0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x00	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	IN1	R/W	0	Comparator 1 Interrupt Enable  Value Description 1 The raw interrupt signal comparator 1 is sent to the interrupt controller. 0 A comparator 1 interrupt does not affect the interrupt status.
0	IN0	R/W	0	Comparator 0 Interrupt Enable  Value Description 1 The raw interrupt signal comparator 0 is sent to the interrupt controller. 0 A comparator 0 interrupt does not affect the interrupt status.

## Register 4: Analog Comparator Reference Voltage Control (ACREFCTL), offset 0x010

This register specifies whether the resistor ladder is powered on as well as the range and tap.

### Analog Comparator Reference Voltage Control (ACREFCTL)

Base 0x4003.C000

Offset 0x010

Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	reserved															
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						EN	RNG	reserved				VREF			
Type	RO	RO	RO	RO	RO	RO	R/W	R/W	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:10	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
9	EN	R/W	0	Resistor Ladder Enable  Value Description 0 The resistor ladder is unpowered. 1 Powers on the resistor ladder. The resistor ladder is connected to $V_{DDA}$ .  This bit is cleared at reset so that the internal reference consumes the least amount of power if it is not used.
8	RNG	R/W	0	Resistor Ladder Range  Value Description 0 The resistor ladder has a total resistance of 31 R. 1 The resistor ladder has a total resistance of 23 R.
7:4	reserved	RO	0x0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3:0	VREF	R/W	0x0	Resistor Ladder Voltage Ref  The VREF bit field specifies the resistor ladder tap that is passed through an analog multiplexer. The voltage corresponding to the tap position is the internal reference voltage available for comparison. See Table 18-2 on page 691 for some output reference voltage examples.



**Register 5: Analog Comparator Status 0 (ACSTAT0), offset 0x020****Register 6: Analog Comparator Status 1 (ACSTAT1), offset 0x040**

These registers specify the current output value of the comparator.

**Analog Comparator Status 0 (ACSTAT0)**

Base 0x4003.C000

Offset 0x020

Type RO, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved															OVAL	reserved
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit/Field	Name	Type	Reset	Description
31:2	reserved	RO	0x0000.000	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
1	OVAL	RO	0	<p>Comparator Output Value</p> <p>Value Description</p> <p>0 VIN- &gt; VIN+</p> <p>1 VIN- &lt; VIN+</p> <p>VIN- is the voltage on the Cn- pin. VIN+ is the voltage on the Cn+ pin, the C0+ pin, or the internal voltage reference (V<sub>IREF</sub>) as defined by the ASRCP bit in the ACCTL register.</p>
0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

**Register 7: Analog Comparator Control 0 (ACCTL0), offset 0x024**

**Register 8: Analog Comparator Control 1 (ACCTL1), offset 0x044**

These registers configure the comparator's input and output.

Analog Comparator Control 0 (ACCTL0)

Base 0x4003.C000  
 Offset 0x024  
 Type R/W, reset 0x0000.0000

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
	reserved																
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	reserved				TOEN	ASRCP			reserved	TSLVAL	TSEN		ISLVAL	ISEN		CINV	reserved
Type	RO	RO	RO	RO	R/W	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit/Field	Name	Type	Reset	Description
31:12	reserved	RO	0x0000.0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
11	TOEN	R/W	0	Trigger Output Enable  Value Description 0 ADC events are suppressed and not sent to the ADC. 1 ADC events are sent to the ADC.
10:9	ASRCP	R/W	0x0	Analog Source Positive  The ASRCP field specifies the source of input voltage to the VIN+ terminal of the comparator. The encodings for this field are as follows:  Value Description 0x0 Pin value of Cn+ 0x1 Pin value of C0+ 0x2 Internal voltage reference (V <sub>IREF</sub> ) 0x3 Reserved
8	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7	TSLVAL	R/W	0	Trigger Sense Level Value  Value Description 0 An ADC event is generated if the comparator output is Low. 1 An ADC event is generated if the comparator output is High.

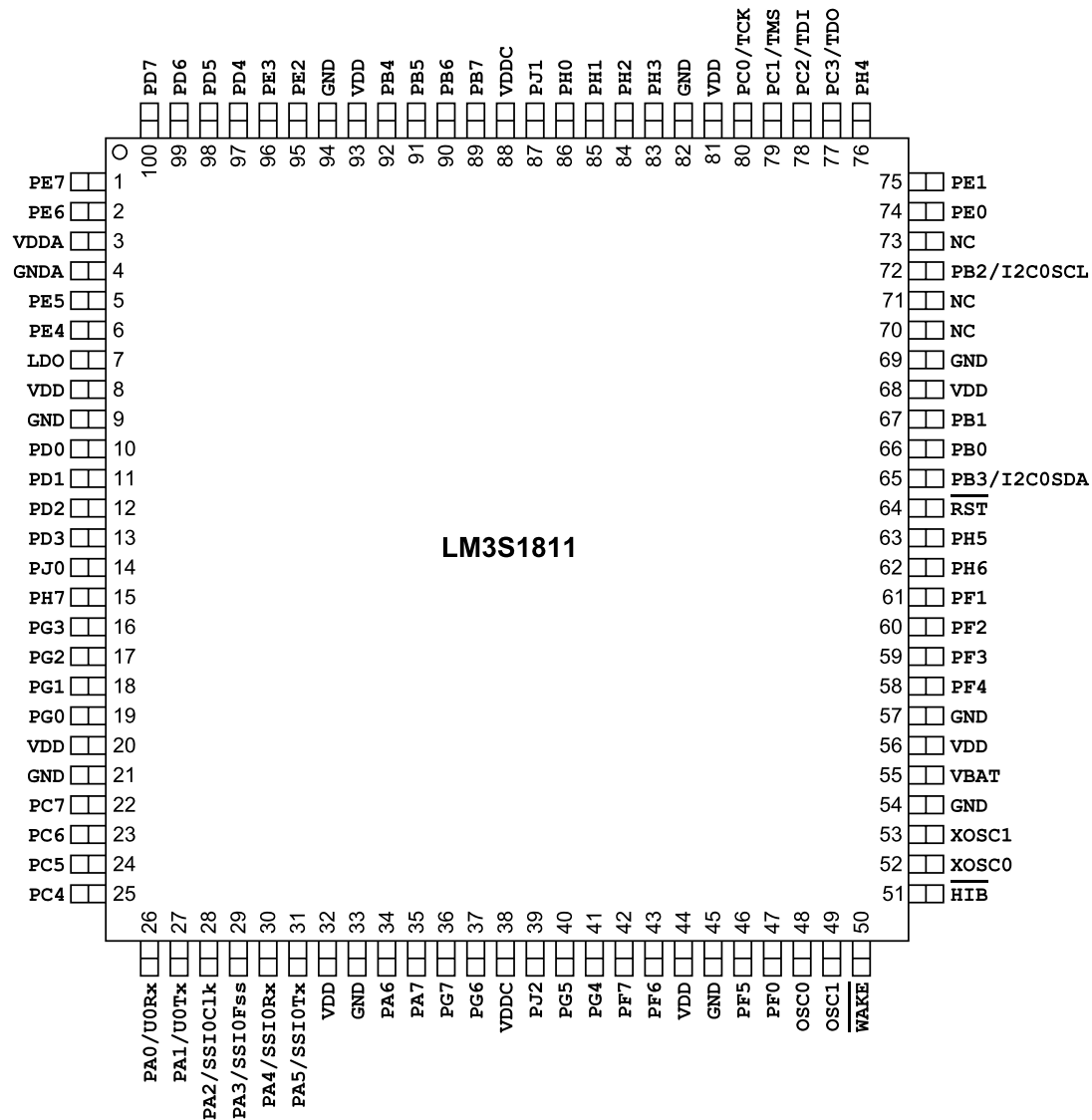
Bit/Field	Name	Type	Reset	Description										
6:5	TSEN	R/W	0x0	<p>Trigger Sense</p> <p>The TSEN field specifies the sense of the comparator output that generates an ADC event. The sense conditioning is as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Level sense, see TSLVAL</td> </tr> <tr> <td>0x1</td> <td>Falling edge</td> </tr> <tr> <td>0x2</td> <td>Rising edge</td> </tr> <tr> <td>0x3</td> <td>Either edge</td> </tr> </tbody> </table>	Value	Description	0x0	Level sense, see TSLVAL	0x1	Falling edge	0x2	Rising edge	0x3	Either edge
Value	Description													
0x0	Level sense, see TSLVAL													
0x1	Falling edge													
0x2	Rising edge													
0x3	Either edge													
4	ISLVAL	R/W	0	<p>Interrupt Sense Level Value</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>An interrupt is generated if the comparator output is Low.</td> </tr> <tr> <td>1</td> <td>An interrupt is generated if the comparator output is High.</td> </tr> </tbody> </table>	Value	Description	0	An interrupt is generated if the comparator output is Low.	1	An interrupt is generated if the comparator output is High.				
Value	Description													
0	An interrupt is generated if the comparator output is Low.													
1	An interrupt is generated if the comparator output is High.													
3:2	ISEN	R/W	0x0	<p>Interrupt Sense</p> <p>The ISEN field specifies the sense of the comparator output that generates an interrupt. The sense conditioning is as follows:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Level sense, see ISLVAL</td> </tr> <tr> <td>0x1</td> <td>Falling edge</td> </tr> <tr> <td>0x2</td> <td>Rising edge</td> </tr> <tr> <td>0x3</td> <td>Either edge</td> </tr> </tbody> </table>	Value	Description	0x0	Level sense, see ISLVAL	0x1	Falling edge	0x2	Rising edge	0x3	Either edge
Value	Description													
0x0	Level sense, see ISLVAL													
0x1	Falling edge													
0x2	Rising edge													
0x3	Either edge													
1	CINV	R/W	0	<p>Comparator Output Invert</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The output of the comparator is unchanged.</td> </tr> <tr> <td>1</td> <td>The output of the comparator is inverted prior to being processed by hardware.</td> </tr> </tbody> </table>	Value	Description	0	The output of the comparator is unchanged.	1	The output of the comparator is inverted prior to being processed by hardware.				
Value	Description													
0	The output of the comparator is unchanged.													
1	The output of the comparator is inverted prior to being processed by hardware.													
0	reserved	RO	0	Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.										

# 19 Pin Diagram

The LM3S1811 microcontroller pin diagram is shown below.

Each GPIO signal is identified by its GPIO port unless it defaults to an alternate function on reset. In this case, the GPIO port name is followed by the default alternate function. To see a complete list of possible functions for each pin, see Table 20-5 on page 722.

Figure 19-1. 100-Pin LQFP Package Pin Diagram



## 20 Signal Tables

The following tables list the signals available for each pin. Signals are configured as GPIOs on reset, except for those noted below. Use the **GPIOAMSEL** register (see page 326) to select analog mode. For a GPIO pin to be used for an alternate digital function, the corresponding bit in the **GPIOAFSEL** register (see page 310) must be set. Further pin muxing options are provided through the  $PMC_x$  bit field in the **GPIOPCTL** register (see page 328), which selects one of several available peripheral functions for that GPIO.

**Important:** All GPIO pins are configured as GPIOs by default with the exception of the pins shown in the table below. A Power-On-Reset ( $\overline{POR}$ ) or asserting  $\overline{RST}$  puts the pins back to their default state.

**Table 20-1. GPIO Pins With Default Alternate Functions**

GPIO Pin	Default State	GPIOAFSEL Bit	GPIOPCTL $PMC_x$ Bit Field
PA[1:0]	UART0	1	0x1
PA[5:2]	SSI0	1	0x1
PB[3:2]	I <sup>2</sup> C0	1	0x1
PC[3:0]	JTAG/SWD	1	0x3

Table 20-2 on page 701 shows the pin-to-signal-name mapping, including functional characteristics of the signals. Each possible alternate analog and digital function is listed for each pin.

Table 20-3 on page 709 lists the signals in alphabetical order by signal name. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed. The "Pin Mux" column indicates the GPIO and the encoding needed in the  $PMC_x$  bit field in the **GPIOPCTL** register.

Table 20-4 on page 717 groups the signals by functionality, except for GPIOs. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed.

Table 20-5 on page 722 lists the GPIO pins and their analog and digital alternate functions. The  $A_{INx}$  analog signals are not 5-V tolerant and go through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding **DEN** bit in the **GPIO Digital Enable (GPIODEN)** register and setting the corresponding **AMSEL** bit in the **GPIO Analog Mode Select (GPIOAMSEL)** register. Other analog signals are 5-V tolerant and are connected directly to their circuitry ( $C0-$ ,  $C0+$ ,  $C1-$ ,  $C1+$ ). These signals are configured by clearing the **DEN** bit in the **GPIO Digital Enable (GPIODEN)** register. The digital signals are enabled by setting the appropriate bit in the **GPIO Alternate Function Select (GPIOAFSEL)** and **GPIODEN** registers and configuring the  $PMC_x$  bit field in the **GPIO Port Control (GPIOPCTL)** register to the numeric encoding shown in the table below. Table entries that are shaded gray are the default values for the corresponding GPIO pin.

**Table 20-2. Signals by Pin Number**

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
1	PE7	I/O	TTL	GPIO port E bit 7.
	AIN0	I	Analog	Analog-to-digital converter input 0.
	U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.

Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
2	PE6	I/O	TTL	GPIO port E bit 6.
	AIN1	I	Analog	Analog-to-digital converter input 1.
	Cl <sub>o</sub>	O	TTL	Analog comparator 1 output.
	U1CTS	I	TTL	UART module 1 Clear To Send modem status input signal.
3	VDDA	-	Power	The positive supply (3.3 V) for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions.
4	GNDA	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
5	PE5	I/O	TTL	GPIO port E bit 5.
	AIN2	I	Analog	Analog-to-digital converter input 2.
	CCP5	I/O	TTL	Capture/Compare/PWM 5.
6	PE4	I/O	TTL	GPIO port E bit 4.
	AIN3	I	Analog	Analog-to-digital converter input 3.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	U2Tx	O	TTL	UART module 2 transmit. When in IrDA mode, this signal has IrDA modulation.
6	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	7	LDO	-	Power
8	VDD	-	Power	Positive supply for I/O and some logic.
9	GND	-	Power	Ground reference for logic and I/O pins.
10	PD0	I/O	TTL	GPIO port D bit 0.
	U2Rx	I	TTL	UART module 2 receive. When in IrDA mode, this signal has IrDA modulation.
	U1Rx	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
	CCP6	I/O	TTL	Capture/Compare/PWM 6.
	U1CTS	I	TTL	UART module 1 Clear To Send modem status input signal.
11	PD1	I/O	TTL	GPIO port D bit 1.
	U2Tx	O	TTL	UART module 2 transmit. When in IrDA mode, this signal has IrDA modulation.
	U1Tx	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
	CCP7	I/O	TTL	Capture/Compare/PWM 7.
	U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.

Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
12	PD2	I/O	TTL	GPIO port D bit 2.
	U1Rx	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
	CCP6	I/O	TTL	Capture/Compare/PWM 6.
	CCP5	I/O	TTL	Capture/Compare/PWM 5.
	EPI0S20	I/O	TTL	EPI module 0 signal 20.
13	PD3	I/O	TTL	GPIO port D bit 3.
	U1Tx	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
	CCP7	I/O	TTL	Capture/Compare/PWM 7.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
	EPI0S21	I/O	TTL	EPI module 0 signal 21.
14	PJ0	I/O	TTL	GPIO port J bit 0.
	EPI0S16	I/O	TTL	EPI module 0 signal 16.
	I2C1SCL	I/O	OD	I <sup>2</sup> C module 1 clock.
15	PH7	I/O	TTL	GPIO port H bit 7.
	EPI0S27	I/O	TTL	EPI module 0 signal 27.
	SSI1Tx	O	TTL	SSI module 1 transmit.
16	PG3	I/O	TTL	GPIO port G bit 3.
17	PG2	I/O	TTL	GPIO port G bit 2.
18	PG1	I/O	TTL	GPIO port G bit 1.
	U2Tx	O	TTL	UART module 2 transmit. When in IrDA mode, this signal has IrDA modulation.
	I2C1SDA	I/O	OD	I <sup>2</sup> C module 1 data.
	EPI0S14	I/O	TTL	EPI module 0 signal 14.
19	PG0	I/O	TTL	GPIO port G bit 0.
	U2Rx	I	TTL	UART module 2 receive. When in IrDA mode, this signal has IrDA modulation.
	I2C1SCL	I/O	OD	I <sup>2</sup> C module 1 clock.
	EPI0S13	I/O	TTL	EPI module 0 signal 13.
20	VDD	-	Power	Positive supply for I/O and some logic.
21	GND	-	Power	Ground reference for logic and I/O pins.
22	PC7	I/O	TTL	GPIO port C bit 7.
	CCP4	I/O	TTL	Capture/Compare/PWM 4.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
	U1Tx	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
	C1o	O	TTL	Analog comparator 1 output.
	EPI0S5	I/O	TTL	EPI module 0 signal 5.

Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
23	PC6	I/O	TTL	GPIO port C bit 6.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	U1Rx	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
	EPI0S4	I/O	TTL	EPI module 0 signal 4.
24	PC5	I/O	TTL	GPIO port C bit 5.
	C1+	I	Analog	Analog comparator 1 positive input.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
	C1o	O	TTL	Analog comparator 1 output.
	C0o	O	TTL	Analog comparator 0 output.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	EPI0S3	I/O	TTL	EPI module 0 signal 3.
25	PC4	I/O	TTL	GPIO port C bit 4.
	CCP5	I/O	TTL	Capture/Compare/PWM 5.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	CCP4	I/O	TTL	Capture/Compare/PWM 4.
	EPI0S2	I/O	TTL	EPI module 0 signal 2.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
26	PA0	I/O	TTL	GPIO port A bit 0.
	U0Rx	I	TTL	UART module 0 receive. When in IrDA mode, this signal has IrDA modulation.
	I2C1SCL	I/O	OD	I <sup>2</sup> C module 1 clock.
	U1Rx	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
27	PA1	I/O	TTL	GPIO port A bit 1.
	U0Tx	O	TTL	UART module 0 transmit. When in IrDA mode, this signal has IrDA modulation.
	I2C1SDA	I/O	OD	I <sup>2</sup> C module 1 data.
	U1Tx	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
28	PA2	I/O	TTL	GPIO port A bit 2.
	SSI0Clk	I/O	TTL	SSI module 0 clock.
29	PA3	I/O	TTL	GPIO port A bit 3.
	SSI0Fss	I/O	TTL	SSI module 0 frame.
30	PA4	I/O	TTL	GPIO port A bit 4.
	SSI0Rx	I	TTL	SSI module 0 receive.
31	PA5	I/O	TTL	GPIO port A bit 5.
	SSI0Tx	O	TTL	SSI module 0 transmit.
32	VDD	-	Power	Positive supply for I/O and some logic.
33	GND	-	Power	Ground reference for logic and I/O pins.



Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
34	PA6	I/O	TTL	GPIO port A bit 6.
	I2C1SCL	I/O	OD	I <sup>2</sup> C module 1 clock.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
	U1CTS	I	TTL	UART module 1 Clear To Send modem status input signal.
35	PA7	I/O	TTL	GPIO port A bit 7.
	I2C1SDA	I/O	OD	I <sup>2</sup> C module 1 data.
	CCP4	I/O	TTL	Capture/Compare/PWM 4.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
36	PG7	I/O	TTL	GPIO port G bit 7.
	CCP5	I/O	TTL	Capture/Compare/PWM 5.
	EPI0S31	I/O	TTL	EPI module 0 signal 31.
37	PG6	I/O	TTL	GPIO port G bit 6.
	U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.
38	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals.
39	PJ2	I/O	TTL	GPIO port J bit 2.
	EPI0S18	I/O	TTL	EPI module 0 signal 18.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
40	PG5	I/O	TTL	GPIO port G bit 5.
	CCP5	I/O	TTL	Capture/Compare/PWM 5.
	U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
41	PG4	I/O	TTL	GPIO port G bit 4.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	EPI0S15	I/O	TTL	EPI module 0 signal 15.
	U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.
42	PF7	I/O	TTL	GPIO port F bit 7.
	CCP4	I/O	TTL	Capture/Compare/PWM 4.
	EPI0S12	I/O	TTL	EPI module 0 signal 12.
43	PF6	I/O	TTL	GPIO port F bit 6.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
	U1RTS	O	TTL	UART module 1 Request to Send modem output control line.
44	VDD	-	Power	Positive supply for I/O and some logic.
45	GND	-	Power	Ground reference for logic and I/O pins.
46	PF5	I/O	TTL	GPIO port F bit 5.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	C1o	O	TTL	Analog comparator 1 output.
	EPI0S15	I/O	TTL	EPI module 0 signal 15.
	SSI1Tx	O	TTL	SSI module 1 transmit.
47	PF0	I/O	TTL	GPIO port F bit 0.
	U1DSR	I	TTL	UART module 1 Data Set Ready modem output control line.

Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
48	OSC0	I	Analog	Main oscillator crystal input or an external clock reference input.
49	OSC1	O	Analog	Main oscillator crystal output.
50	$\overline{\text{WAKE}}$	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
51	$\overline{\text{HIB}}$	O	OD	An open-drain output that indicates the processor is in Hibernate mode.
52	XOSC0	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 4.194304-MHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC. See the CLKSEL bit in the HIBCTL register.
53	XOSC1	O	Analog	Hibernation module oscillator crystal output.
54	GND	-	Power	Ground reference for logic and I/O pins.
55	VBAT	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
56	VDD	-	Power	Positive supply for I/O and some logic.
57	GND	-	Power	Ground reference for logic and I/O pins.
58	PF4	I/O	TTL	GPIO port F bit 4.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
	CO <sub>0</sub>	O	TTL	Analog comparator 0 output.
	EPI0S12	I/O	TTL	EPI module 0 signal 12.
	SSI1Rx	I	TTL	SSI module 1 receive.
59	PF3	I/O	TTL	GPIO port F bit 3.
	SSI1Fss	I/O	TTL	SSI module 1 frame.
60	PF2	I/O	TTL	GPIO port F bit 2.
	SSI1Clk	I/O	TTL	SSI module 1 clock.
61	PF1	I/O	TTL	GPIO port F bit 1.
	U1RTS	O	TTL	UART module 1 Request to Send modem output control line.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
62	PH6	I/O	TTL	GPIO port H bit 6.
	EPI0S26	I/O	TTL	EPI module 0 signal 26.
	SSI1Rx	I	TTL	SSI module 1 receive.
63	PH5	I/O	TTL	GPIO port H bit 5.
	EPI0S11	I/O	TTL	EPI module 0 signal 11.
	SSI1Fss	I/O	TTL	SSI module 1 frame.
64	RST	I	TTL	System reset input.
65	PB3	I/O	TTL	GPIO port B bit 3.
	I2C0SDA	I/O	OD	I <sup>2</sup> C module 0 data.
66	PB0	I/O	TTL	GPIO port B bit 0.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
	U1Rx	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.

Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
67	PB1	I/O	TTL	GPIO port B bit 1.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
	U1Tx	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
68	VDD	-	Power	Positive supply for I/O and some logic.
69	GND	-	Power	Ground reference for logic and I/O pins.
70	NC	-	-	No connect. Leave the pin electrically unconnected/isolated.
71	NC	-	-	No connect. Leave the pin electrically unconnected/isolated.
72	PB2	I/O	TTL	GPIO port B bit 2.
	I2C0SCL	I/O	OD	I <sup>2</sup> C module 0 clock.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
73	NC	-	-	No connect. Leave the pin electrically unconnected/isolated.
74	PE0	I/O	TTL	GPIO port E bit 0.
	SSI1Clk	I/O	TTL	SSI module 1 clock.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	EPI0S8	I/O	TTL	EPI module 0 signal 8.
75	PE1	I/O	TTL	GPIO port E bit 1.
	SSI1Fss	I/O	TTL	SSI module 1 frame.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	CCP6	I/O	TTL	Capture/Compare/PWM 6.
	EPI0S9	I/O	TTL	EPI module 0 signal 9.
76	PH4	I/O	TTL	GPIO port H bit 4.
	EPI0S10	I/O	TTL	EPI module 0 signal 10.
	SSI1Clk	I/O	TTL	SSI module 1 clock.
77	PC3	I/O	TTL	GPIO port C bit 3.
	TDO	O	TTL	JTAG TDO and SWO.
	SWO	O	TTL	JTAG TDO and SWO.
78	PC2	I/O	TTL	GPIO port C bit 2.
	TDI	I	TTL	JTAG TDI.
79	PC1	I/O	TTL	GPIO port C bit 1.
	TMS	I	TTL	JTAG TMS and SWDIO.
	SWDIO	I/O	TTL	JTAG TMS and SWDIO.
80	PC0	I/O	TTL	GPIO port C bit 0.
	TCK	I	TTL	JTAG/SWD CLK.
	SWCLK	I	TTL	JTAG/SWD CLK.
81	VDD	-	Power	Positive supply for I/O and some logic.
82	GND	-	Power	Ground reference for logic and I/O pins.
83	PH3	I/O	TTL	GPIO port H bit 3.
	EPI0S0	I/O	TTL	EPI module 0 signal 0.

Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
84	PH2	I/O	TTL	GPIO port H bit 2.
	C1o	O	TTL	Analog comparator 1 output.
	EPI0S1	I/O	TTL	EPI module 0 signal 1.
85	PH1	I/O	TTL	GPIO port H bit 1.
	CCP7	I/O	TTL	Capture/Compare/PWM 7.
	EPI0S7	I/O	TTL	EPI module 0 signal 7.
86	PH0	I/O	TTL	GPIO port H bit 0.
	CCP6	I/O	TTL	Capture/Compare/PWM 6.
	EPI0S6	I/O	TTL	EPI module 0 signal 6.
87	PJ1	I/O	TTL	GPIO port J bit 1.
	EPI0S17	I/O	TTL	EPI module 0 signal 17.
	I2C1SDA	I/O	OD	I <sup>2</sup> C module 1 data.
88	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals.
89	PB7	I/O	TTL	GPIO port B bit 7.
	NMI	I	TTL	Non-maskable interrupt.
90	PB6	I/O	TTL	GPIO port B bit 6.
	VREFA	I	Analog	This input provides a reference voltage used to specify the input voltage at which the ADC converts to a maximum value. In other words, the voltage that is applied to VREFA is the voltage with which an AIN <sub>n</sub> signal is converted to 1023. The VREFA input is limited to the range specified in Table 22-2 on page 726.
	C0+	I	Analog	Analog comparator 0 positive input.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
	CCP7	I/O	TTL	Capture/Compare/PWM 7.
	C0o	O	TTL	Analog comparator 0 output.
	CCP5	I/O	TTL	Capture/Compare/PWM 5.
91	PB5	I/O	TTL	GPIO port B bit 5.
	C1-	I	Analog	Analog comparator 1 negative input.
	C0o	O	TTL	Analog comparator 0 output.
	CCP5	I/O	TTL	Capture/Compare/PWM 5.
	CCP6	I/O	TTL	Capture/Compare/PWM 6.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	U1Tx	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
EPI0S22	I/O	TTL	EPI module 0 signal 22.	
92	PB4	I/O	TTL	GPIO port B bit 4.
	C0-	I	Analog	Analog comparator 0 negative input.
	U2Rx	I	TTL	UART module 2 receive. When in IrDA mode, this signal has IrDA modulation.
	U1Rx	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
	EPI0S23	I/O	TTL	EPI module 0 signal 23.

Table 20-2. Signals by Pin Number (continued)

Pin Number	Pin Name	Pin Type	Buffer Type <sup>a</sup>	Description
93	VDD	-	Power	Positive supply for I/O and some logic.
94	GND	-	Power	Ground reference for logic and I/O pins.
95	PE2	I/O	TTL	GPIO port E bit 2.
	CCP4	I/O	TTL	Capture/Compare/PWM 4.
	SSI1Rx	I	TTL	SSI module 1 receive.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	EPI0S24	I/O	TTL	EPI module 0 signal 24.
96	PE3	I/O	TTL	GPIO port E bit 3.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
	SSI1Tx	O	TTL	SSI module 1 transmit.
	CCP7	I/O	TTL	Capture/Compare/PWM 7.
	EPI0S25	I/O	TTL	EPI module 0 signal 25.
97	PD4	I/O	TTL	GPIO port D bit 4.
	AIN7	I	Analog	Analog-to-digital converter input 7.
	CCP0	I/O	TTL	Capture/Compare/PWM 0.
	CCP3	I/O	TTL	Capture/Compare/PWM 3.
	U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.
	EPI0S19	I/O	TTL	EPI module 0 signal 19.
98	PD5	I/O	TTL	GPIO port D bit 5.
	AIN6	I	Analog	Analog-to-digital converter input 6.
	CCP2	I/O	TTL	Capture/Compare/PWM 2.
	CCP4	I/O	TTL	Capture/Compare/PWM 4.
	U2Rx	I	TTL	UART module 2 receive. When in IrDA mode, this signal has IrDA modulation.
	EPI0S28	I/O	TTL	EPI module 0 signal 28.
99	PD6	I/O	TTL	GPIO port D bit 6.
	AIN5	I	Analog	Analog-to-digital converter input 5.
	U2Tx	O	TTL	UART module 2 transmit. When in IrDA mode, this signal has IrDA modulation.
	EPI0S29	I/O	TTL	EPI module 0 signal 29.
100	PD7	I/O	TTL	GPIO port D bit 7.
	AIN4	I	Analog	Analog-to-digital converter input 4.
	CO <sub>0</sub>	O	TTL	Analog comparator 0 output.
	CCP1	I/O	TTL	Capture/Compare/PWM 1.
	U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
	EPI0S30	I/O	TTL	EPI module 0 signal 30.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

Table 20-3. Signals by Signal Name

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
AIN0	1	PE7	I	Analog	Analog-to-digital converter input 0.

Table 20-3. Signals by Signal Name (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
AIN1	2	PE6	I	Analog	Analog-to-digital converter input 1.
AIN2	5	PE5	I	Analog	Analog-to-digital converter input 2.
AIN3	6	PE4	I	Analog	Analog-to-digital converter input 3.
AIN4	100	PD7	I	Analog	Analog-to-digital converter input 4.
AIN5	99	PD6	I	Analog	Analog-to-digital converter input 5.
AIN6	98	PD5	I	Analog	Analog-to-digital converter input 6.
AIN7	97	PD4	I	Analog	Analog-to-digital converter input 7.
C0+	90	PB6	I	Analog	Analog comparator 0 positive input.
C0-	92	PB4	I	Analog	Analog comparator 0 negative input.
C0o	24 58 90 91 100	PC5 (3) PF4 (2) PB6 (3) PB5 (1) PD7 (2)	O	TTL	Analog comparator 0 output.
C1+	24	PC5	I	Analog	Analog comparator 1 positive input.
C1-	91	PB5	I	Analog	Analog comparator 1 negative input.
C1o	2 22 24 46 84	PE6 (2) PC7 (7) PC5 (2) PF5 (2) PH2 (2)	O	TTL	Analog comparator 1 output.
CCP0	13 22 23 39 58 66 72 91 97	PD3 (4) PC7 (4) PC6 (6) PJ2 (9) PF4 (1) PB0 (1) PB2 (5) PB5 (4) PD4 (1)	I/O	TTL	Capture/Compare/PWM 0.
CCP1	24 25 34 43 67 90 96 100	PC5 (1) PC4 (9) PA6 (2) PF6 (1) PB1 (4) PB6 (1) PE3 (1) PD7 (3)	I/O	TTL	Capture/Compare/PWM 1.
CCP2	6 11 25 46 67 75 91 95 98	PE4 (6) PD1 (10) PC4 (5) PF5 (1) PB1 (1) PE1 (4) PB5 (6) PE2 (5) PD5 (1)	I/O	TTL	Capture/Compare/PWM 2.

Table 20-3. Signals by Signal Name (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
CCP3	6 23 24 35 41 61 72 74 97	PE4 (1) PC6 (1) PC5 (5) PA7 (7) PG4 (1) PF1 (10) PB2 (4) PE0 (3) PD4 (2)	I/O	TTL	Capture/Compare/PWM 3.
CCP4	22 25 35 42 95 98	PC7 (1) PC4 (6) PA7 (2) PF7 (1) PE2 (1) PD5 (2)	I/O	TTL	Capture/Compare/PWM 4.
CCP5	5 12 25 36 40 90 91	PE5 (1) PD2 (4) PC4 (1) PG7 (8) PG5 (1) PB6 (6) PB5 (2)	I/O	TTL	Capture/Compare/PWM 5.
CCP6	10 12 75 86 91	PD0 (6) PD2 (2) PE1 (5) PH0 (1) PB5 (3)	I/O	TTL	Capture/Compare/PWM 6.
CCP7	11 13 85 90 96	PD1 (6) PD3 (2) PH1 (1) PB6 (2) PE3 (5)	I/O	TTL	Capture/Compare/PWM 7.
EPI0S0	83	PH3 (8)	I/O	TTL	EPI module 0 signal 0.
EPI0S1	84	PH2 (8)	I/O	TTL	EPI module 0 signal 1.
EPI0S2	25	PC4 (8)	I/O	TTL	EPI module 0 signal 2.
EPI0S3	24	PC5 (8)	I/O	TTL	EPI module 0 signal 3.
EPI0S4	23	PC6 (8)	I/O	TTL	EPI module 0 signal 4.
EPI0S5	22	PC7 (8)	I/O	TTL	EPI module 0 signal 5.
EPI0S6	86	PH0 (8)	I/O	TTL	EPI module 0 signal 6.
EPI0S7	85	PH1 (8)	I/O	TTL	EPI module 0 signal 7.
EPI0S8	74	PE0 (8)	I/O	TTL	EPI module 0 signal 8.
EPI0S9	75	PE1 (8)	I/O	TTL	EPI module 0 signal 9.
EPI0S10	76	PH4 (8)	I/O	TTL	EPI module 0 signal 10.
EPI0S11	63	PH5 (8)	I/O	TTL	EPI module 0 signal 11.
EPI0S12	42 58	PF7 (8) PF4 (8)	I/O	TTL	EPI module 0 signal 12.
EPI0S13	19	PG0 (8)	I/O	TTL	EPI module 0 signal 13.
EPI0S14	18	PG1 (8)	I/O	TTL	EPI module 0 signal 14.
EPI0S15	41 46	PG4 (8) PF5 (8)	I/O	TTL	EPI module 0 signal 15.

Table 20-3. Signals by Signal Name (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
EPI0S16	14	PJ0 (8)	I/O	TTL	EPI module 0 signal 16.
EPI0S17	87	PJ1 (8)	I/O	TTL	EPI module 0 signal 17.
EPI0S18	39	PJ2 (8)	I/O	TTL	EPI module 0 signal 18.
EPI0S19	97	PD4 (10)	I/O	TTL	EPI module 0 signal 19.
EPI0S20	12	PD2 (8)	I/O	TTL	EPI module 0 signal 20.
EPI0S21	13	PD3 (8)	I/O	TTL	EPI module 0 signal 21.
EPI0S22	91	PB5 (8)	I/O	TTL	EPI module 0 signal 22.
EPI0S23	92	PB4 (8)	I/O	TTL	EPI module 0 signal 23.
EPI0S24	95	PE2 (8)	I/O	TTL	EPI module 0 signal 24.
EPI0S25	96	PE3 (8)	I/O	TTL	EPI module 0 signal 25.
EPI0S26	62	PH6 (8)	I/O	TTL	EPI module 0 signal 26.
EPI0S27	15	PH7 (8)	I/O	TTL	EPI module 0 signal 27.
EPI0S28	98	PD5 (10)	I/O	TTL	EPI module 0 signal 28.
EPI0S29	99	PD6 (10)	I/O	TTL	EPI module 0 signal 29.
EPI0S30	100	PD7 (10)	I/O	TTL	EPI module 0 signal 30.
EPI0S31	36	PG7 (9)	I/O	TTL	EPI module 0 signal 31.
GND	9 21 33 45 54 57 69 82 94	fixed	-	Power	Ground reference for logic and I/O pins.
GNDA	4	fixed	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
HIB	51	fixed	O	OD	An open-drain output that indicates the processor is in Hibernate mode.
I2C0SCL	72	PB2 (1)	I/O	OD	I <sup>2</sup> C module 0 clock.
I2C0SDA	65	PB3 (1)	I/O	OD	I <sup>2</sup> C module 0 data.
I2C1SCL	14 19 26 34	PJ0 (11) PG0 (3) PA0 (8) PA6 (1)	I/O	OD	I <sup>2</sup> C module 1 clock.
I2C1SDA	18 27 35 87	PG1 (3) PA1 (8) PA7 (1) PJ1 (11)	I/O	OD	I <sup>2</sup> C module 1 data.
LDO	7	fixed	-	Power	Low drop-out regulator output voltage. This pin requires an external capacitor between the pin and GND of 1 $\mu$ F or greater. When the on-chip LDO is used to provide power to the logic, the LDO pin must also be connected to the VDDC pins at the board level in addition to the decoupling capacitor(s).



Table 20-3. Signals by Signal Name (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
NC	70 71 73	fixed	-	-	No connect. Leave the pin electrically unconnected/isolated.
NMI	89	PB7 (4)	I	TTL	Non-maskable interrupt.
OSC0	48	fixed	I	Analog	Main oscillator crystal input or an external clock reference input.
OSC1	49	fixed	O	Analog	Main oscillator crystal output.
PA0	26	-	I/O	TTL	GPIO port A bit 0.
PA1	27	-	I/O	TTL	GPIO port A bit 1.
PA2	28	-	I/O	TTL	GPIO port A bit 2.
PA3	29	-	I/O	TTL	GPIO port A bit 3.
PA4	30	-	I/O	TTL	GPIO port A bit 4.
PA5	31	-	I/O	TTL	GPIO port A bit 5.
PA6	34	-	I/O	TTL	GPIO port A bit 6.
PA7	35	-	I/O	TTL	GPIO port A bit 7.
PB0	66	-	I/O	TTL	GPIO port B bit 0.
PB1	67	-	I/O	TTL	GPIO port B bit 1.
PB2	72	-	I/O	TTL	GPIO port B bit 2.
PB3	65	-	I/O	TTL	GPIO port B bit 3.
PB4	92	-	I/O	TTL	GPIO port B bit 4.
PB5	91	-	I/O	TTL	GPIO port B bit 5.
PB6	90	-	I/O	TTL	GPIO port B bit 6.
PB7	89	-	I/O	TTL	GPIO port B bit 7.
PC0	80	-	I/O	TTL	GPIO port C bit 0.
PC1	79	-	I/O	TTL	GPIO port C bit 1.
PC2	78	-	I/O	TTL	GPIO port C bit 2.
PC3	77	-	I/O	TTL	GPIO port C bit 3.
PC4	25	-	I/O	TTL	GPIO port C bit 4.
PC5	24	-	I/O	TTL	GPIO port C bit 5.
PC6	23	-	I/O	TTL	GPIO port C bit 6.
PC7	22	-	I/O	TTL	GPIO port C bit 7.
PD0	10	-	I/O	TTL	GPIO port D bit 0.
PD1	11	-	I/O	TTL	GPIO port D bit 1.
PD2	12	-	I/O	TTL	GPIO port D bit 2.
PD3	13	-	I/O	TTL	GPIO port D bit 3.
PD4	97	-	I/O	TTL	GPIO port D bit 4.
PD5	98	-	I/O	TTL	GPIO port D bit 5.
PD6	99	-	I/O	TTL	GPIO port D bit 6.
PD7	100	-	I/O	TTL	GPIO port D bit 7.
PE0	74	-	I/O	TTL	GPIO port E bit 0.
PE1	75	-	I/O	TTL	GPIO port E bit 1.

Table 20-3. Signals by Signal Name (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
PE2	95	-	I/O	TTL	GPIO port E bit 2.
PE3	96	-	I/O	TTL	GPIO port E bit 3.
PE4	6	-	I/O	TTL	GPIO port E bit 4.
PE5	5	-	I/O	TTL	GPIO port E bit 5.
PE6	2	-	I/O	TTL	GPIO port E bit 6.
PE7	1	-	I/O	TTL	GPIO port E bit 7.
PF0	47	-	I/O	TTL	GPIO port F bit 0.
PF1	61	-	I/O	TTL	GPIO port F bit 1.
PF2	60	-	I/O	TTL	GPIO port F bit 2.
PF3	59	-	I/O	TTL	GPIO port F bit 3.
PF4	58	-	I/O	TTL	GPIO port F bit 4.
PF5	46	-	I/O	TTL	GPIO port F bit 5.
PF6	43	-	I/O	TTL	GPIO port F bit 6.
PF7	42	-	I/O	TTL	GPIO port F bit 7.
PG0	19	-	I/O	TTL	GPIO port G bit 0.
PG1	18	-	I/O	TTL	GPIO port G bit 1.
PG2	17	-	I/O	TTL	GPIO port G bit 2.
PG3	16	-	I/O	TTL	GPIO port G bit 3.
PG4	41	-	I/O	TTL	GPIO port G bit 4.
PG5	40	-	I/O	TTL	GPIO port G bit 5.
PG6	37	-	I/O	TTL	GPIO port G bit 6.
PG7	36	-	I/O	TTL	GPIO port G bit 7.
PH0	86	-	I/O	TTL	GPIO port H bit 0.
PH1	85	-	I/O	TTL	GPIO port H bit 1.
PH2	84	-	I/O	TTL	GPIO port H bit 2.
PH3	83	-	I/O	TTL	GPIO port H bit 3.
PH4	76	-	I/O	TTL	GPIO port H bit 4.
PH5	63	-	I/O	TTL	GPIO port H bit 5.
PH6	62	-	I/O	TTL	GPIO port H bit 6.
PH7	15	-	I/O	TTL	GPIO port H bit 7.
PJ0	14	-	I/O	TTL	GPIO port J bit 0.
PJ1	87	-	I/O	TTL	GPIO port J bit 1.
PJ2	39	-	I/O	TTL	GPIO port J bit 2.
RST	64	fixed	I	TTL	System reset input.
SSI0Clk	28	PA2 (1)	I/O	TTL	SSI module 0 clock.
SSI0Fss	29	PA3 (1)	I/O	TTL	SSI module 0 frame.
SSI0Rx	30	PA4 (1)	I	TTL	SSI module 0 receive.
SSI0Tx	31	PA5 (1)	O	TTL	SSI module 0 transmit.
SSI1Clk	60 74 76	PF2 (9) PE0 (2) PH4 (11)	I/O	TTL	SSI module 1 clock.

Table 20-3. Signals by Signal Name (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
SSI1Fss	59 63 75	PF3 (9) PH5 (11) PE1 (2)	I/O	TTL	SSI module 1 frame.
SSI1Rx	58 62 95	PF4 (9) PH6 (11) PE2 (2)	I	TTL	SSI module 1 receive.
SSI1Tx	15 46 96	PH7 (11) PF5 (9) PE3 (2)	O	TTL	SSI module 1 transmit.
SWCLK	80	PC0 (3)	I	TTL	JTAG/SWD CLK.
SWDIO	79	PC1 (3)	I/O	TTL	JTAG TMS and SWDIO.
SWO	77	PC3 (3)	O	TTL	JTAG TDO and SWO.
TCK	80	PC0 (3)	I	TTL	JTAG/SWD CLK.
TDI	78	PC2 (3)	I	TTL	JTAG TDI.
TDO	77	PC3 (3)	O	TTL	JTAG TDO and SWO.
TMS	79	PC1 (3)	I	TTL	JTAG TMS and SWDIO.
U0Rx	26	PA0 (1)	I	TTL	UART module 0 receive. When in IrDA mode, this signal has IrDA modulation.
U0Tx	27	PA1 (1)	O	TTL	UART module 0 transmit. When in IrDA mode, this signal has IrDA modulation.
U1CTS	2 10 34	PE6 (9) PD0 (9) PA6 (9)	I	TTL	UART module 1 Clear To Send modem status input signal.
U1DCD	1 11 35	PE7 (9) PD1 (9) PA7 (9)	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
U1DSR	47	PF0 (9)	I	TTL	UART module 1 Data Set Ready modem output control line.
U1DTR	40 100	PG5 (10) PD7 (9)	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
U1RI	37 41 97	PG6 (10) PG4 (10) PD4 (9)	I	TTL	UART module 1 Ring Indicator modem status input signal.
U1RTS	43 61	PF6 (10) PF1 (9)	O	TTL	UART module 1 Request to Send modem output control line.
U1Rx	10 12 23 26 66 92	PD0 (5) PD2 (1) PC6 (5) PA0 (9) PB0 (5) PB4 (7)	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
U1Tx	11 13 22 27 67 91	PD1 (5) PD3 (1) PC7 (5) PA1 (9) PB1 (5) PB5 (7)	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.

Table 20-3. Signals by Signal Name (continued)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type <sup>a</sup>	Description
U2Rx	10 19 92 98	PD0 (4) PG0 (1) PB4 (4) PD5 (9)	I	TTL	UART module 2 receive. When in IrDA mode, this signal has IrDA modulation.
U2Tx	6 11 18 99	PE4 (5) PD1 (4) PG1 (1) PD6 (9)	O	TTL	UART module 2 transmit. When in IrDA mode, this signal has IrDA modulation.
VBAT	55	fixed	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
VDD	8 20 32 44 56 68 81 93	fixed	-	Power	Positive supply for I/O and some logic.
VDDA	3	fixed	-	Power	The positive supply (3.3 V) for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions.
VDDC	38 88	fixed	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals.
VREFA	90	PB6	I	Analog	This input provides a reference voltage used to specify the input voltage at which the ADC converts to a maximum value. In other words, the voltage that is applied to VREFA is the voltage with which an AIN <sub>n</sub> signal is converted to 1023. The VREFA input is limited to the range specified in Table 22-2 on page 726.
WAKE	50	fixed	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
XOSC0	52	fixed	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 4.194304-MHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC. See the CLKSEL bit in the HIBCTL register.
XOSC1	53	fixed	O	Analog	Hibernation module oscillator crystal output.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

Table 20-4. Signals by Function, Except for GPIO

Function	Pin Name	Pin Number	Pin Type	Buffer Type <sup>a</sup>	Description
ADC	AIN0	1	I	Analog	Analog-to-digital converter input 0.
	AIN1	2	I	Analog	Analog-to-digital converter input 1.
	AIN2	5	I	Analog	Analog-to-digital converter input 2.
	AIN3	6	I	Analog	Analog-to-digital converter input 3.
	AIN4	100	I	Analog	Analog-to-digital converter input 4.
	AIN5	99	I	Analog	Analog-to-digital converter input 5.
	AIN6	98	I	Analog	Analog-to-digital converter input 6.
	AIN7	97	I	Analog	Analog-to-digital converter input 7.
	VREFA	90	I	Analog	This input provides a reference voltage used to specify the input voltage at which the ADC converts to a maximum value. In other words, the voltage that is applied to VREFA is the voltage with which an AIN <sub>n</sub> signal is converted to 1023. The VREFA input is limited to the range specified in Table 22-2 on page 726.
Analog Comparators	C0+	90	I	Analog	Analog comparator 0 positive input.
	C0-	92	I	Analog	Analog comparator 0 negative input.
	C0o	24 58 90 91 100	O	TTL	Analog comparator 0 output.
	C1+	24	I	Analog	Analog comparator 1 positive input.
	C1-	91	I	Analog	Analog comparator 1 negative input.
	C1o	2 22 24 46 84	O	TTL	Analog comparator 1 output.

Table 20-4. Signals by Function, Except for GPIO (continued)

Function	Pin Name	Pin Number	Pin Type	Buffer Type <sup>a</sup>	Description
External Peripheral Interface	EPI0S0	83	I/O	TTL	EPI module 0 signal 0.
	EPI0S1	84	I/O	TTL	EPI module 0 signal 1.
	EPI0S2	25	I/O	TTL	EPI module 0 signal 2.
	EPI0S3	24	I/O	TTL	EPI module 0 signal 3.
	EPI0S4	23	I/O	TTL	EPI module 0 signal 4.
	EPI0S5	22	I/O	TTL	EPI module 0 signal 5.
	EPI0S6	86	I/O	TTL	EPI module 0 signal 6.
	EPI0S7	85	I/O	TTL	EPI module 0 signal 7.
	EPI0S8	74	I/O	TTL	EPI module 0 signal 8.
	EPI0S9	75	I/O	TTL	EPI module 0 signal 9.
	EPI0S10	76	I/O	TTL	EPI module 0 signal 10.
	EPI0S11	63	I/O	TTL	EPI module 0 signal 11.
	EPI0S12	42 58	I/O	TTL	EPI module 0 signal 12.
	EPI0S13	19	I/O	TTL	EPI module 0 signal 13.
	EPI0S14	18	I/O	TTL	EPI module 0 signal 14.
	EPI0S15	41 46	I/O	TTL	EPI module 0 signal 15.
	EPI0S16	14	I/O	TTL	EPI module 0 signal 16.
	EPI0S17	87	I/O	TTL	EPI module 0 signal 17.
	EPI0S18	39	I/O	TTL	EPI module 0 signal 18.
	EPI0S19	97	I/O	TTL	EPI module 0 signal 19.
	EPI0S20	12	I/O	TTL	EPI module 0 signal 20.
	EPI0S21	13	I/O	TTL	EPI module 0 signal 21.
	EPI0S22	91	I/O	TTL	EPI module 0 signal 22.
	EPI0S23	92	I/O	TTL	EPI module 0 signal 23.
	EPI0S24	95	I/O	TTL	EPI module 0 signal 24.
	EPI0S25	96	I/O	TTL	EPI module 0 signal 25.
	EPI0S26	62	I/O	TTL	EPI module 0 signal 26.
	EPI0S27	15	I/O	TTL	EPI module 0 signal 27.
	EPI0S28	98	I/O	TTL	EPI module 0 signal 28.
	EPI0S29	99	I/O	TTL	EPI module 0 signal 29.
	EPI0S30	100	I/O	TTL	EPI module 0 signal 30.
EPI0S31	36	I/O	TTL	EPI module 0 signal 31.	

Table 20-4. Signals by Function, Except for GPIO (continued)

Function	Pin Name	Pin Number	Pin Type	Buffer Type <sup>a</sup>	Description
General-Purpose Timers	CCP0	13 22 23 39 58 66 72 91 97	I/O	TTL	Capture/Compare/PWM 0.
	CCP1	24 25 34 43 67 90 96 100	I/O	TTL	Capture/Compare/PWM 1.
	CCP2	6 11 25 46 67 75 91 95 98	I/O	TTL	Capture/Compare/PWM 2.
	CCP3	6 23 24 35 41 61 72 74 97	I/O	TTL	Capture/Compare/PWM 3.
	CCP4	22 25 35 42 95 98	I/O	TTL	Capture/Compare/PWM 4.
	CCP5	5 12 25 36 40 90 91	I/O	TTL	Capture/Compare/PWM 5.
	CCP6	10 12 75 86 91	I/O	TTL	Capture/Compare/PWM 6.
	CCP7		I/O	TTL	Capture/Compare/PWM 7.

Table 20-4. Signals by Function, Except for GPIO (continued)

Function	Pin Name	Pin Number	Pin Type	Buffer Type <sup>a</sup>	Description
		11 13 85 90 96			
Hibernate	HIB	51	O	OD	An open-drain output that indicates the processor is in Hibernate mode.
	VBAT	55	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
	WAKE	50	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
	XOSC0	52	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 4.194304-MHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC. See the CLKSEL bit in the HIBCTL register.
	XOSC1	53	O	Analog	Hibernation module oscillator crystal output.
I2C	I2C0SCL	72	I/O	OD	I <sup>2</sup> C module 0 clock.
	I2C0SDA	65	I/O	OD	I <sup>2</sup> C module 0 data.
	I2C1SCL	14 19 26 34	I/O	OD	I <sup>2</sup> C module 1 clock.
	I2C1SDA	18 27 35 87	I/O	OD	I <sup>2</sup> C module 1 data.
JTAG/SWD/SWO	SWCLK	80	I	TTL	JTAG/SWD CLK.
	SWDIO	79	I/O	TTL	JTAG TMS and SWDIO.
	SWO	77	O	TTL	JTAG TDO and SWO.
	TCK	80	I	TTL	JTAG/SWD CLK.
	TDI	78	I	TTL	JTAG TDI.
	TDO	77	O	TTL	JTAG TDO and SWO.
	TMS	79	I	TTL	JTAG TMS and SWDIO.



Table 20-4. Signals by Function, Except for GPIO (continued)

Function	Pin Name	Pin Number	Pin Type	Buffer Type <sup>a</sup>	Description
Power	GND	9 21 33 45 54 57 69 82 94	-	Power	Ground reference for logic and I/O pins.
	GNDA	4	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
	LDO	7	-	Power	Low drop-out regulator output voltage. This pin requires an external capacitor between the pin and GND of 1 $\mu$ F or greater. When the on-chip LDO is used to provide power to the logic, the LDO pin must also be connected to the VDDC pins at the board level in addition to the decoupling capacitor(s).
	VDD	8 20 32 44 56 68 81 93	-	Power	Positive supply for I/O and some logic.
	VDDA	3	-	Power	The positive supply (3.3 V) for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions.
	VDDC	38 88	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals.
SSI	SSI0Clk	28	I/O	TTL	SSI module 0 clock.
	SSI0Fss	29	I/O	TTL	SSI module 0 frame.
	SSI0Rx	30	I	TTL	SSI module 0 receive.
	SSI0Tx	31	O	TTL	SSI module 0 transmit.
	SSI1Clk	60 74 76	I/O	TTL	SSI module 1 clock.
	SSI1Fss	59 63 75	I/O	TTL	SSI module 1 frame.
	SSI1Rx	58 62 95	I	TTL	SSI module 1 receive.
	SSI1Tx	15 46 96	O	TTL	SSI module 1 transmit.

Table 20-4. Signals by Function, Except for GPIO (continued)

Function	Pin Name	Pin Number	Pin Type	Buffer Type <sup>a</sup>	Description
System Control & Clocks	NMI	89	I	TTL	Non-maskable interrupt.
	OSC0	48	I	Analog	Main oscillator crystal input or an external clock reference input.
	OSC1	49	O	Analog	Main oscillator crystal output.
	RST	64	I	TTL	System reset input.
UART	U0Rx	26	I	TTL	UART module 0 receive. When in IrDA mode, this signal has IrDA modulation.
	U0Tx	27	O	TTL	UART module 0 transmit. When in IrDA mode, this signal has IrDA modulation.
	U1CTS	2 10 34	I	TTL	UART module 1 Clear To Send modem status input signal.
	U1DCD	1 11 35	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
	U1DSR	47	I	TTL	UART module 1 Data Set Ready modem output control line.
	U1DTR	40 100	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
	U1RI	37 41 97	I	TTL	UART module 1 Ring Indicator modem status input signal.
	U1RTS	43 61	O	TTL	UART module 1 Request to Send modem output control line.
	U1Rx	10 12 23 26 66 92	I	TTL	UART module 1 receive. When in IrDA mode, this signal has IrDA modulation.
	U1Tx	11 13 22 27 67 91	O	TTL	UART module 1 transmit. When in IrDA mode, this signal has IrDA modulation.
	U2Rx	10 19 92 98	I	TTL	UART module 2 receive. When in IrDA mode, this signal has IrDA modulation.
	U2Tx	6 11 18 99	O	TTL	UART module 2 transmit. When in IrDA mode, this signal has IrDA modulation.

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

Table 20-5. GPIO Pins and Alternate Functions

IO	Pin	Analog Function	Digital Function (GPIOCTL PMCx Bit Field Encoding) <sup>a</sup>											
			1	2	3	4	5	6	7	8	9	10	11	
PA0	26	-	U0Rx	-	-	-	-	-	-	-	I2C1SCL	U1Rx	-	-

Table 20-5. GPIO Pins and Alternate Functions (continued)

IO	Pin	Analog Function	Digital Function (GPIOCTL PMCx Bit Field Encoding) <sup>a</sup>											
			1	2	3	4	5	6	7	8	9	10	11	
PA1	27	-	U0Tx	-	-	-	-	-	-	-	I2C1SDA	U1Tx	-	-
PA2	28	-	SSI0Clk	-	-	-	-	-	-	-	-	-	-	-
PA3	29	-	SSI0Fss	-	-	-	-	-	-	-	-	-	-	-
PA4	30	-	SSI0Rx	-	-	-	-	-	-	-	-	-	-	-
PA5	31	-	SSI0Tx	-	-	-	-	-	-	-	-	-	-	-
PA6	34	-	I2C1SCL	CCP1	-	-	-	-	-	-	-	U1CTS	-	-
PA7	35	-	I2C1SDA	CCP4	-	-	-	-	-	CCP3	-	U1DCD	-	-
PB0	66	-	CCP0	-	-	-	-	U1Rx	-	-	-	-	-	-
PB1	67	-	CCP2	-	-	-	CCP1	U1Tx	-	-	-	-	-	-
PB2	72	-	I2C0SCL	-	-	-	CCP3	CCP0	-	-	-	-	-	-
PB3	65	-	I2C0SDA	-	-	-	-	-	-	-	-	-	-	-
PB4	92	C0-	-	-	-	-	U2Rx	-	-	U1Rx	EPI0S23	-	-	-
PB5	91	C1-	C0o	CCP5	CCP6	CCP0	-	CCP2	U1Tx	EPI0S22	-	-	-	-
PB6	90	VREFA C0+	CCP1	CCP7	C0o	-	-	CCP5	-	-	-	-	-	-
PB7	89	-	-	-	-	-	NMI	-	-	-	-	-	-	-
PC0	80	-	-	-	TCK SWCLK	-	-	-	-	-	-	-	-	-
PC1	79	-	-	-	TMS SWDIO	-	-	-	-	-	-	-	-	-
PC2	78	-	-	-	TDI	-	-	-	-	-	-	-	-	-
PC3	77	-	-	-	TDO SWO	-	-	-	-	-	-	-	-	-
PC4	25	-	CCP5	-	-	-	CCP2	CCP4	-	EPI0S2	CCP1	-	-	-
PC5	24	C1+	CCP1	C1o	C0o	-	CCP3	-	-	EPI0S3	-	-	-	-
PC6	23	-	CCP3	-	-	-	U1Rx	CCP0	-	EPI0S4	-	-	-	-
PC7	22	-	CCP4	-	-	-	CCP0	U1Tx	-	C1o	EPI0S5	-	-	-
PD0	10	-	-	-	-	-	U2Rx	U1Rx	CCP6	-	-	U1CTS	-	-
PD1	11	-	-	-	-	-	U2Tx	U1Tx	CCP7	-	-	U1DCD	CCP2	-
PD2	12	-	U1Rx	CCP6	-	-	CCP5	-	-	-	EPI0S20	-	-	-
PD3	13	-	U1Tx	CCP7	-	-	CCP0	-	-	-	EPI0S21	-	-	-
PD4	97	AIN7	CCP0	CCP3	-	-	-	-	-	-	U1RI	EPI0S19	-	-
PD5	98	AIN6	CCP2	CCP4	-	-	-	-	-	-	U2Rx	EPI0S28	-	-
PD6	99	AIN5	-	-	-	-	-	-	-	-	U2Tx	EPI0S29	-	-
PD7	100	AIN4	-	C0o	CCP1	-	-	-	-	-	U1DTR	EPI0S30	-	-
PE0	74	-	-	SSI1Clk	CCP3	-	-	-	-	-	EPI0S8	-	-	-
PE1	75	-	-	SSI1Fss	-	CCP2	CCP6	-	-	-	EPI0S9	-	-	-
PE2	95	-	CCP4	SSI1Rx	-	-	CCP2	-	-	-	EPI0S24	-	-	-
PE3	96	-	CCP1	SSI1Tx	-	-	CCP7	-	-	-	EPI0S25	-	-	-
PE4	6	AIN3	CCP3	-	-	-	U2Tx	CCP2	-	-	-	-	-	-
PE5	5	AIN2	CCP5	-	-	-	-	-	-	-	-	-	-	-
PE6	2	AIN1	-	C1o	-	-	-	-	-	-	U1CTS	-	-	-

Table 20-5. GPIO Pins and Alternate Functions (continued)

IO	Pin	Analog Function	Digital Function (GPIOCTL PMCx Bit Field Encoding) <sup>a</sup>											
			1	2	3	4	5	6	7	8	9	10	11	
PE7	1	AIN0	-	-	-	-	-	-	-	-	-	U1DCD	-	-
PF0	47	-	-	-	-	-	-	-	-	-	-	U1DSR	-	-
PF1	61	-	-	-	-	-	-	-	-	-	-	U1RTS	CCP3	-
PF2	60	-	-	-	-	-	-	-	-	-	-	SSI1Clk	-	-
PF3	59	-	-	-	-	-	-	-	-	-	-	SSI1Fss	-	-
PF4	58	-	CCP0	C0o	-	-	-	-	-	-	EPI0S12	SSI1Rx	-	-
PF5	46	-	CCP2	C1o	-	-	-	-	-	-	EPI0S15	SSI1Tx	-	-
PF6	43	-	CCP1	-	-	-	-	-	-	-	-	-	U1RTS	-
PF7	42	-	CCP4	-	-	-	-	-	-	-	EPI0S12	-	-	-
PG0	19	-	U2Rx	-	I2C1SCL	-	-	-	-	-	EPI0S13	-	-	-
PG1	18	-	U2Tx	-	I2C1SDA	-	-	-	-	-	EPI0S14	-	-	-
PG2	17	-	-	-	-	-	-	-	-	-	-	-	-	-
PG3	16	-	-	-	-	-	-	-	-	-	-	-	-	-
PG4	41	-	CCP3	-	-	-	-	-	-	-	EPI0S15	-	U1RI	-
PG5	40	-	CCP5	-	-	-	-	-	-	-	-	-	U1DTR	-
PG6	37	-	-	-	-	-	-	-	-	-	-	-	U1RI	-
PG7	36	-	-	-	-	-	-	-	-	-	CCP5	EPI0S31	-	-
PH0	86	-	CCP6	-	-	-	-	-	-	-	EPI0S6	-	-	-
PH1	85	-	CCP7	-	-	-	-	-	-	-	EPI0S7	-	-	-
PH2	84	-	-	C1o	-	-	-	-	-	-	EPI0S1	-	-	-
PH3	83	-	-	-	-	-	-	-	-	-	EPI0S0	-	-	-
PH4	76	-	-	-	-	-	-	-	-	-	EPI0S10	-	-	SSI1Clk
PH5	63	-	-	-	-	-	-	-	-	-	EPI0S11	-	-	SSI1Fss
PH6	62	-	-	-	-	-	-	-	-	-	EPI0S26	-	-	SSI1Rx
PH7	15	-	-	-	-	-	-	-	-	-	EPI0S27	-	-	SSI1Tx
PJ0	14	-	-	-	-	-	-	-	-	-	EPI0S16	-	-	I2C1SCL
PJ1	87	-	-	-	-	-	-	-	-	-	EPI0S17	-	-	I2C1SDA
PJ2	39	-	-	-	-	-	-	-	-	-	EPI0S18	CCP0	-	-

a. The digital signals that are shaded gray are the power-on default values for the corresponding GPIO pin.

## 21 Operating Characteristics

**Table 21-1. Temperature Characteristics**

Characteristic <sup>a</sup>	Symbol	Value	Unit
Industrial operating temperature range	$T_A$	-40 to +85	°C

a. Maximum storage temperature is 150°C.

**Table 21-2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal resistance (junction to ambient) <sup>a</sup>	$\Theta_{JA}$	34	°C/W
Average junction temperature <sup>b</sup>	$T_J$	$T_A + (P_{AVG} \cdot \Theta_{JA})$	°C

a. Junction to ambient thermal resistance  $\Theta_{JA}$  numbers are determined by a package simulator.

b. Power dissipation is a function of temperature.

## 22 Electrical Characteristics

### 22.1 DC Characteristics

#### 22.1.1 Maximum Ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device.

**Note:** The device is not guaranteed to operate properly at the maximum ratings.

**Table 22-1. Maximum Ratings**

Parameter	Parameter Name <sup>a</sup>	Value		Unit
		Min	Max	
V <sub>DD</sub>	I/O supply voltage (V <sub>DD</sub> )	0	4	V
V <sub>DDA</sub>	Analog supply voltage (V <sub>DDA</sub> )	0	4	V
V <sub>BAT</sub>	Battery supply voltage (V <sub>BAT</sub> )	0	4	V
V <sub>IN</sub>	Input voltage	-0.3	5.5	V
I	Maximum current per output pins	-	25	mA

a. Voltages are measured with respect to GND.

**Important:** This device contains circuitry to protect the inputs against damage due to high-static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either GND or V<sub>DD</sub>).

#### 22.1.2 Recommended DC Operating Conditions

For special high-current applications, the GPIO output buffers may be used with the following restrictions. With the GPIO pins configured as 8-mA output drivers, a total of four GPIO outputs may be used to sink current loads up to 18 mA each. At 18-mA sink current loading, the V<sub>OL</sub> value is specified as 1.2 V. The high-current GPIO package pins must be selected such that there are only a maximum of two per side of the physical package with the total number of high-current GPIO outputs not exceeding four for the entire package.

**Table 22-2. Recommended DC Operating Conditions**

Parameter	Parameter Name	Min	Nom	Max	Unit
V <sub>DD</sub>	I/O supply voltage	3.0	3.3	3.6	V
V <sub>DDA</sub>	Analog supply voltage	3.0	3.3	3.6	V
V <sub>DDC</sub> <sup>a</sup>	Core supply voltage	1.08	1.2	1.32	V
V <sub>IH</sub>	High-level input voltage	2.0	-	5.0	V
V <sub>IL</sub>	Low-level input voltage	-0.3	-	1.3	V
V <sub>OH</sub> <sup>b</sup>	High-level output voltage	2.4	-	-	V
V <sub>OL</sub> <sup>a</sup>	Low-level output voltage	-	-	0.4	V

**Table 22-2. Recommended DC Operating Conditions (continued)**

Parameter	Parameter Name	Min	Nom	Max	Unit
I <sub>OH</sub>	High-level source current, V <sub>OH</sub> =2.4 V				
	2-mA Drive	2.0	-	-	mA
	4-mA Drive	4.0	-	-	mA
	8-mA Drive	8.0	-	-	mA
I <sub>OL</sub>	Low-level sink current, V <sub>OL</sub> =0.4 V				
	2-mA Drive	2.0	-	-	mA
	4-mA Drive	4.0	-	-	mA
	8-mA Drive	8.0	-	-	mA

a. V<sub>DDC</sub> is supplied from the output of the LDO.

b. V<sub>OL</sub> and V<sub>OH</sub> shift to 1.2 V when using high-current GPIOs.

### 22.1.3 On-Chip Low Drop-Out (LDO) Regulator Characteristics

**Table 22-3. LDO Regulator Characteristics**

Parameter	Parameter Name	Min	Nom	Max	Unit
C <sub>LDO</sub>	External filter capacitor size for internal power supply	1.0	-	3.0	μF
V <sub>LDO</sub>	LDO output voltage	1.08	1.2	1.32	V

### 22.1.4 Hibernation Module Characteristics

**Table 22-4. Hibernation Module DC Characteristics**

Parameter	Parameter Name	Min	Nominal	Max	Unit
V <sub>BAT</sub>	Battery supply voltage	2.4	3.0	3.6	V
V <sub>LOWBAT</sub>	Low battery detect voltage	-	2.35	-	V

### 22.1.5 Flash Memory Characteristics

**Table 22-5. Flash Memory Characteristics**

Parameter	Parameter Name	Min	Nom	Max	Unit
PE <sub>CYC</sub>	Number of guaranteed mass program/erase cycles before failure <sup>a</sup>	15,000	-	-	cycles
T <sub>RET</sub>	Data retention at average operating temperature of 125°C	10	-	-	years
T <sub>PROG</sub>	Word program time	-	-	1	ms
T <sub>BPROG</sub>	Buffer program time	-	-	1	ms
T <sub>ERASE</sub>	Page erase time	-	-	12	ms
T <sub>ME</sub>	Mass erase time	-	-	12	ms

a. A program/erase cycle is defined as switching the bits from 1-> 0 -> 1. Caution should be used when performing block erases, as repeated block erases can shorten the number of guaranteed erase cycles, see "Flash Memory Programming" on page 199.

## 22.1.6 GPIO Module Characteristics

**Table 22-6. GPIO Module DC Characteristics**

Parameter	Parameter Name	Min	Nom	Max	Unit
R <sub>GPIOPU</sub>	GPIO internal pull-up resistor	50	-	110	kΩ
R <sub>GPIOPD</sub>	GPIO internal pull-down resistor	55	-	180	kΩ

## 22.1.7 Current Specifications

This section provides information on typical and maximum power consumption under various conditions.

### 22.1.7.1 Preliminary Current Consumption Specifications

The following table provides preliminary figures for current consumption while ongoing characterization is completed.

**Table 22-7. Preliminary Current Consumption**

Parameter	Parameter Name	Conditions	Nom	Max	Unit
I <sub>DD_RUN</sub>	Run mode 1 (Flash loop)	V <sub>DD</sub> = 3.3 V Code= while(1){} executed in Flash Peripherals = All ON System Clock = 50 MHz (with PLL) Temp = 25°C	56	-	mA
I <sub>DD_SLEEP</sub>	Sleep mode	V <sub>DD</sub> = 3.3 V Peripherals = All clock gated System Clock = 50 MHz (with PLL) Temp = 25°C	8	-	mA
I <sub>DD_DEEPSLEEP</sub>	Deep-sleep mode	Peripherals = All OFF System Clock = IOS30KHZ/64 Temp = 25°C	-	550	μA
I <sub>HIB_NORTC</sub>	Hibernate mode (external wake, RTC disabled, I/O not powered <sup>a</sup> )	V <sub>BAT</sub> = 3.0 V V <sub>DD</sub> = 0 V V <sub>DDA</sub> = 0 V Peripherals = All OFF System Clock = OFF Hibernate Module = 0 kHz	8	-	μA
I <sub>HIB_RTC</sub>	Hibernate mode (RTC enabled, I/O not powered <sup>a</sup> )	V <sub>BAT</sub> = 3.0 V V <sub>DD</sub> = 3.3 V V <sub>DDA</sub> = 3.3 V Peripherals = All OFF System Clock = OFF Hibernate Module = 32 kHz	18	-	μA

a. The VDD3ON mode must be disabled for the I/O ring to be unpowered.

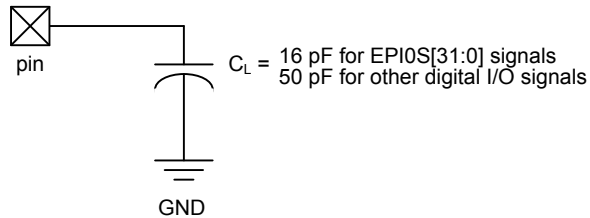


## 22.2 AC Characteristics

### 22.2.1 Load Conditions

Unless otherwise specified, the following conditions are true for all timing measurements.

**Figure 22-1. Load Conditions**



### 22.2.2 Clocks

The following sections provide specifications on the various clock sources and mode.

#### 22.2.2.1 PLL Specifications

The following tables provide specifications for using the PLL.

**Table 22-8. Phase Locked Loop (PLL) Characteristics**

Parameter	Parameter Name	Min	Nom	Max	Unit
$f_{\text{REF\_XTAL}}$	Crystal reference <sup>a</sup>	3.579545	-	16.384	MHz
$f_{\text{REF\_EXT}}$	External clock reference <sup>a</sup>	3.579545	-	16.384	MHz
$f_{\text{PLL}}$	PLL frequency <sup>b</sup>	-	400	-	MHz
$T_{\text{READY}}$	PLL lock time	0.562 <sup>c</sup>	-	1.38 <sup>d</sup>	ms

a. The exact value is determined by the crystal value programmed into the XTAL field of the **Run-Mode Clock Configuration (RCC)** register.

b. PLL frequency is automatically calculated by the hardware based on the XTAL field of the **RCC** register.

c. Using a 16.384-MHz crystal

d. Using 3.5795-MHz crystal

Table 22-9 on page 729 shows the actual frequency of the PLL based on the crystal frequency used (defined by the XTAL field in the **RCC** register).

**Table 22-9. Actual PLL Frequency**

XTAL	Crystal Frequency (MHz)	PLL Frequency (MHz)	Error
0x04	3.5795	400.904	0.0023%
0x05	3.6864	398.1312	0.0047%
0x06	4.0	400	-
0x07	4.096	401.408	0.0035%
0x08	4.9152	398.1312	0.0047%
0x09	5.0	400	-
0x0A	5.12	399.36	0.0016%
0x0B	6.0	400	-
0x0C	6.144	399.36	0.0016%

Table 22-9. Actual PLL Frequency (continued)

XTAL	Crystal Frequency (MHz)	PLL Frequency (MHz)	Error
0x0D	7.3728	398.1312	0.0047%
0x0E	8.0	400	0.0047%
0x0F	8.192	398.6773333	0.0033%
0x10	10.0	400	-
0x11	12.0	400	-
0x12	12.288	401.408	0.0035%
0x13	13.56	397.76	0.0056%
0x14	14.318	400.90904	0.0023%
0x15	16.0	400	-
0x16	16.384	404.1386667	0.010%

### 22.2.2.2 PIOSC Specifications

Table 22-10. PIOSC Clock Characteristics

Parameter	Parameter Name	Min	Nom	Max	Unit
f <sub>PIOSC25</sub>	Internal 16-MHz precision oscillator frequency variance, factory calibrated at 25 °C	-	±0.25%	±1%	-
f <sub>PIOSCT</sub>	Internal 16-MHz precision oscillator frequency variance, factory calibrated at 25 °C, across specified temperature range	-	-	±3%	-
f <sub>PIOSCUCAL</sub>	Internal 16-MHz precision oscillator frequency variance, user calibrated at a chosen temperature	-	±0.25%	±1%	-

### 22.2.2.3 Internal 30-kHz Oscillator Specifications

Table 22-11. 30-kHz Clock Characteristics

Parameter	Parameter Name	Min	Nom	Max	Unit
f <sub>IOSC30KHZ</sub>	Internal 30-KHz oscillator frequency	15	30	45	KHz

### 22.2.2.4 Hibernation Clock Source Specifications

Table 22-12. Hibernation Clock Characteristics

Parameter	Parameter Name	Min	Nom	Max	Unit
f <sub>HIBOSC</sub>	Hibernation module oscillator frequency	-	4.194304	-	MHz
f <sub>HIBOSC_XTAL</sub>	Crystal reference for hibernation oscillator	-	4.194304	-	MHz
f <sub>HIBOSC_EXT</sub>	External clock reference for hibernation module	-	32.768	-	KHz
t <sub>HIBOSC_SETTLE</sub>	Hibernation oscillator settling time <sup>a</sup>	-	-	10	ms

a. This parameter is highly sensitive to PCB layout and trace lengths, which may make this parameter time longer. Care must be taken in PCB design to minimize trace lengths and RLC (resistance, inductance, capacitance).

Table 22-13. HIB Oscillator Input Characteristics

Name	Value	Condition
Frequency	4.194304	MHz

Table 22-13. HIB Oscillator Input Characteristics (continued)

Name	Value	Condition
Frequency tolerance	±100	PPM
Oscillation mode	parallel	-
Equivalent series resistance (max)	200	Ω
Load capacitance	16	pF
Drive level (typ)	100	μw

### 22.2.2.5 Main Oscillator Specifications

Table 22-14. Main Oscillator Clock Characteristics

Parameter	Parameter Name	Min	Nom	Max	Unit
f <sub>MOSC</sub>	Main oscillator frequency	1	-	16.384	MHz
t <sub>MOSC_PER</sub>	Main oscillator period	61	-	1000	ns
t <sub>MOSC_SETTLE</sub>	Main oscillator settling time	17.5	-	20	ms
f <sub>REF_XTAL_BYPASS</sub>	Crystal reference using the main oscillator (PLL in BYPASS mode) <sup>a</sup>	1	-	16.384	MHz
f <sub>REF_EXT_BYPASS</sub>	External clock reference (PLL in BYPASS mode) <sup>a</sup>	0	-	50	MHz

a. The ADC must be clocked from the PLL or directly from a 16-MHz clock source to operate properly.

Table 22-15. MOSC Oscillator Input Characteristics

Name	Value						Condition
	16	12	8	6	4	3.5	
Frequency	16	12	8	6	4	3.5	MHz
Frequency tolerance	±100	±100	±100	±100	±100	±100	PPM
Oscillation mode	parallel	parallel	parallel	parallel	parallel	parallel	-
Equivalent series resistance (max)	70	90	120	160	200	220	Ω
Load capacitance	16	16	16	16	16	16	pF
Drive level (typ)	100	100	100	100	100	100	μw

### 22.2.2.6 System Clock Specifications with ADC Operation

Table 22-16. System Clock Characteristics with ADC Operation

Parameter	Parameter Name	Min	Nom	Max	Unit
f <sub>sysadc</sub>	System clock frequency when the ADC module is operating (when PLL is bypassed)	16	-	-	MHz

### 22.2.3 JTAG and Boundary Scan

Table 22-17. JTAG Characteristics

Parameter No.	Parameter	Parameter Name	Min	Nom	Max	Unit
J1	f <sub>TCK</sub>	TCK operational clock frequency	0	-	10	MHz
J2	t <sub>TCK</sub>	TCK operational clock period	100	-	-	ns

Table 22-17. JTAG Characteristics (continued)

Parameter No.	Parameter	Parameter Name	Min	Nom	Max	Unit
J3	$t_{TCK\_LOW}$	TCK clock Low time	-	$t_{TCK}$	-	ns
J4	$t_{TCK\_HIGH}$	TCK clock High time	-	$t_{TCK}$	-	ns
J5	$t_{TCK\_R}$	TCK rise time	0	-	10	ns
J6	$t_{TCK\_F}$	TCK fall time	0	-	10	ns
J7	$t_{TMS\_SU}$	TMS setup time to TCK rise	20	-	-	ns
J8	$t_{TMS\_HLD}$	TMS hold time from TCK rise	20	-	-	ns
J9	$t_{TDI\_SU}$	TDI setup time to TCK rise	25	-	-	ns
J10	$t_{TDI\_HLD}$	TDI hold time from TCK rise	25	-	-	ns
J11 $t_{TDO\_ZDV}$	TCK fall to Data Valid from High-Z	2-mA drive	-	23	35	ns
		4-mA drive		15	26	ns
		8-mA drive		14	25	ns
		8-mA drive with slew rate control		18	29	ns
J12 $t_{TDO\_DV}$	TCK fall to Data Valid from Data Valid	2-mA drive	-	21	35	ns
		4-mA drive		14	25	ns
		8-mA drive		13	24	ns
		8-mA drive with slew rate control		18	28	ns
J13 $t_{TDO\_DVZ}$	TCK fall to High-Z from Data Valid	2-mA drive	-	9	11	ns
		4-mA drive		7	9	ns
		8-mA drive		6	8	ns
		8-mA drive with slew rate control		7	9	ns

Figure 22-2. JTAG Test Clock Input Timing

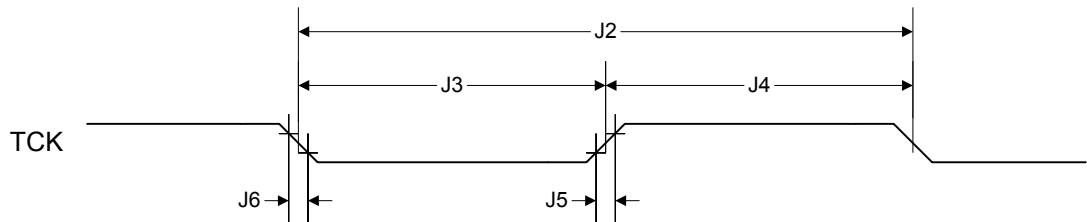
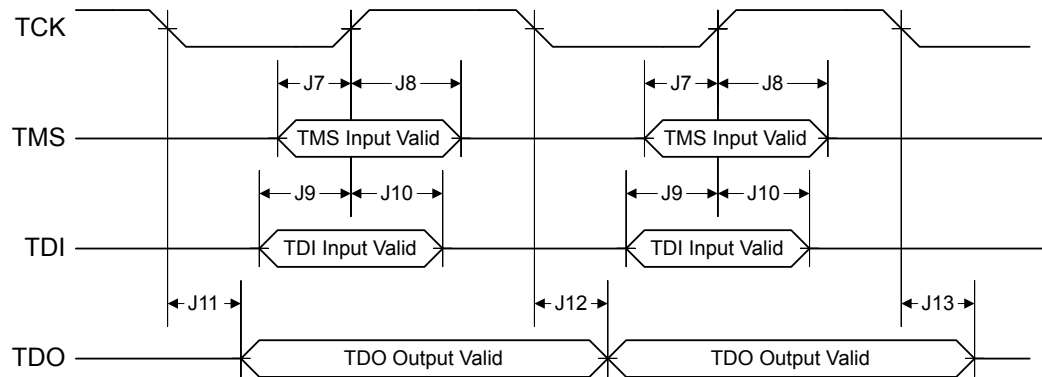


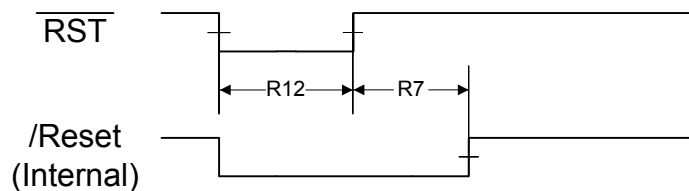
Figure 22-3. JTAG Test Access Port (TAP) Timing



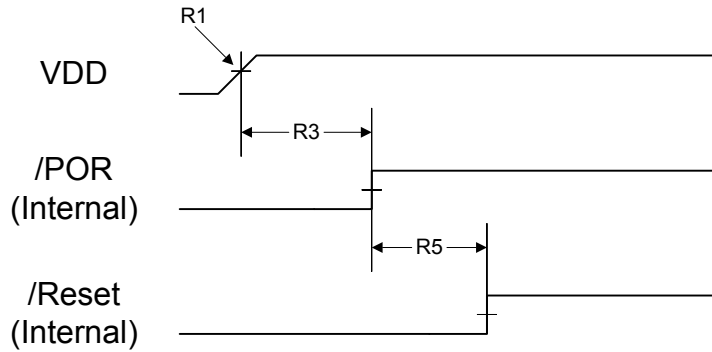
## 22.2.4 Reset

Table 22-18. Reset Characteristics

Parameter No.	Parameter	Parameter Name	Min	Nom	Max	Unit
R1	$V_{TH}$	Reset threshold	-	2.0	-	V
R2	$V_{BTH}$	Brown-Out threshold	2.85	2.9	2.95	V
R3	$T_{POR}$	Power-On Reset timeout	-	10	-	ms
R4	$T_{BOR}$	Brown-Out timeout	-	500	-	$\mu$ s
R5	$T_{IRPOR}$	Internal reset timeout after POR	-	-	95	system clocks
R6	$T_{IRBOR}$	Internal reset timeout after BOR	-	-	7	system clocks
R7	$T_{IRHWR}$	Internal reset timeout after hardware reset ( $\overline{RST}$ pin)	-	-	7	system clocks
R8	$T_{IRSWR}$	Internal reset timeout after software-initiated system reset	-	-	16	system clocks
R9	$T_{IRWDR}$	Internal reset timeout after watchdog reset	-	-	16	system clocks
R10	$T_{IRMFR}$	Internal reset timeout after MOSC failure reset	-	-	32	system clocks
R11	$T_{VDDRISE}$	Supply voltage ( $V_{DD}$ ) rise time (0V-3.3V)	-	-	250	ms
R12	$T_{MIN}$	Minimum $\overline{RST}$ pulse width	2	-	-	$\mu$ s

Figure 22-4. External Reset Timing ( $\overline{RST}$ )

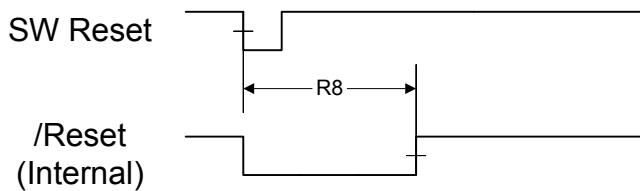
**Figure 22-5. Power-On Reset Timing**



**Figure 22-6. Brown-Out Reset Timing**



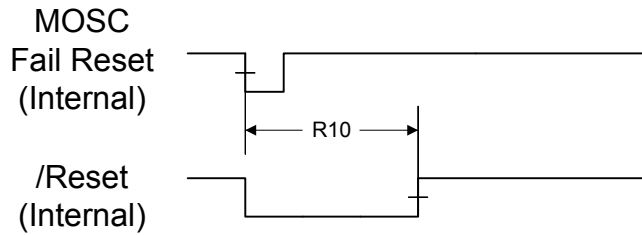
**Figure 22-7. Software Reset Timing**



**Figure 22-8. Watchdog Reset Timing**



Figure 22-9. MOSC Failure Reset Timing



## 22.2.5 Deep-Sleep Mode

Table 22-19. Deep-Sleep Mode AC Characteristics

Parameter No	Parameter	Parameter Name	Min	Nom	Max	Unit
D1	$t_{\text{ENTER\_DS}}$	Time to enter deep-sleep mode from sleep request	-	0	16 <sup>a</sup>	ms

a. Nominal specification occurs 99.9995% of the time.

## 22.2.6 Hibernation Module

The Hibernation Module requires special system implementation considerations because it is intended to power down all other sections of its host device, refer to “Hibernation Module” on page 171.

Table 22-20. Hibernation Module AC Characteristics

Parameter No	Parameter	Parameter Name	Min	Nom	Max	Unit
H1	$t_{\text{HIB\_LOW}}$	Internal 32.768 KHz clock reference rising edge to $\overline{\text{HIB}}$ asserted	20	-	-	$\mu\text{s}$
H2	$t_{\text{HIB\_HIGH}}$	Internal 32.768 KHz clock reference rising edge to $\overline{\text{HIB}}$ deasserted	-	30	-	$\mu\text{s}$
H3	$t_{\text{WAKE\_TO\_HIB}}$	$\overline{\text{WAKE}}$ assert to $\overline{\text{HIB}}$ desassert (wake up time), internal Hibernation oscillator running during hibernation	62	-	124	$\mu\text{s}$
H4	$t_{\text{WAKE\_TO\_HIB}}$	$\overline{\text{WAKE}}$ assert to $\overline{\text{HIB}}$ desassert (wake up time), internal Hibernation oscillator stopped during hibernation	-	-	10	ms
H5	$t_{\text{WAKE\_CLOCK}}$	$\overline{\text{WAKE}}$ assertion time, internal Hibernation oscillator running during hibernation	62	-	-	$\mu\text{s}$
H6	$t_{\text{WAKE\_NOCLOCK}}$	$\overline{\text{WAKE}}$ assertion time, internal Hibernation oscillator stopped during hibernation <sup>a</sup>	10	-	-	ms
H7	$t_{\text{HIB\_REG\_ACCESS}}$	Access time to or from a non-volatile register in HIB module to complete	92	-	-	$\mu\text{s}$
H8	$t_{\text{HIB\_TO\_HIB}}$	$\overline{\text{HIB}}$ high time between assertions	100	-	-	ms
H9	$t_{\text{ENTER\_HIB}}$	Time to enter hibernation mode from hibernation request	-	0	50 <sup>b</sup>	ms

a. This mode is used when the  $\text{PINWEN}$  bit is set and the  $\text{RTCEN}$  bit is clear in the  $\text{HIBCTL}$  register.

b. Nominal specification occurs 99.998% of the time.

Figure 22-10. Hibernation Module Timing with Internal Oscillator Running in Hibernation

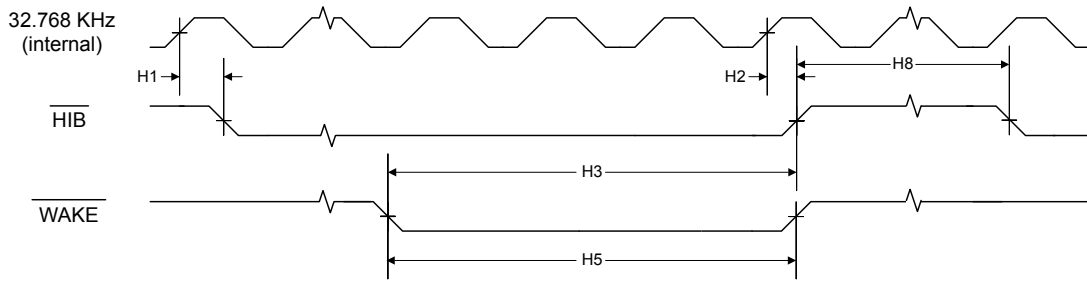
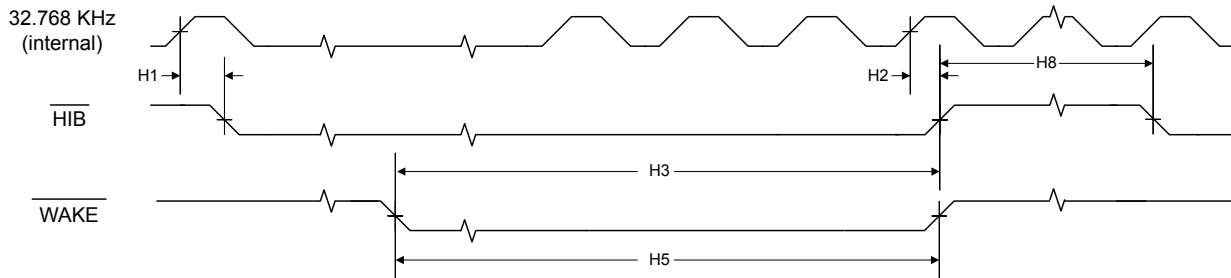


Figure 22-11. Hibernation Module Timing with Internal Oscillator Stopped in Hibernation



### 22.2.7 General-Purpose I/O (GPIO)

**Note:** All GPIOs are 5-V tolerant.

Table 22-21. GPIO Characteristics

Parameter	Parameter Name	Condition	Min	Nom	Max	Unit
$t_{GPIOR}$	GPIO Rise Time (from 20% to 80% of $V_{DD}$ )	2-mA drive	-	14	20	ns
		4-mA drive		7	10	ns
		8-mA drive		4	5	ns
		8-mA drive with slew rate control		6	8	ns
$t_{GPIOF}$	GPIO Fall Time (from 80% to 20% of $V_{DD}$ )	2-mA drive	-	14	21	ns
		4-mA drive		7	11	ns
		8-mA drive		4	6	ns
		8-mA drive with slew rate control		6	8	ns

### 22.2.8 External Peripheral Interface (EPI)

When the EPI module is in SDRAM mode, the drive strength must be configured to 8 mA. Table 22-22 on page 736 shows the rise and fall times in SDRAM mode with 16 pF load conditions. When the EPI module is in Host-Bus or General-Purpose mode, the values in Table 22-21 on page 736 should be used.

Table 22-22. EPI SDRAM Characteristics

Parameter	Parameter Name	Condition	Min	Nom	Max	Unit
$t_{SDRAMR}$	EPI Rise Time (from 20% to 80% of $V_{DD}$ )	8-mA drive, $C_L = 16$ pF	-	2	3	ns



Table 22-22. EPI SDRAM Characteristics (continued)

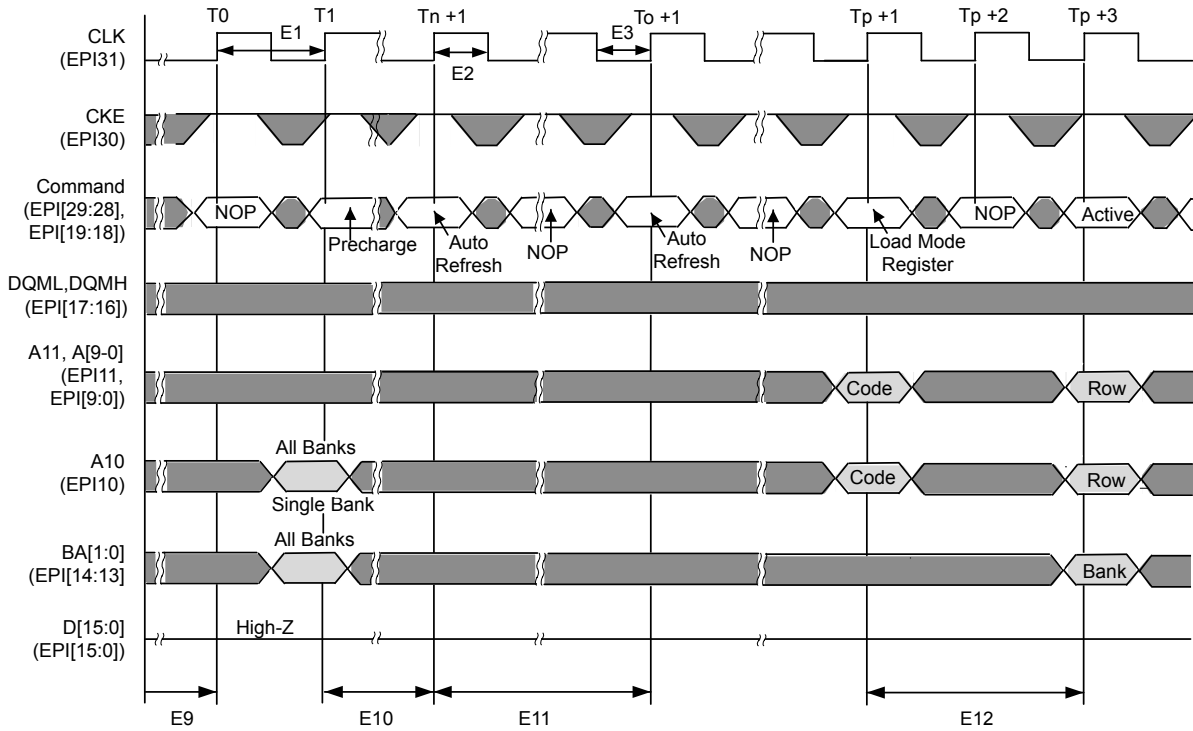
Parameter	Parameter Name	Condition	Min	Nom	Max	Unit
$t_{\text{SDRAMF}}$	EPI Fall Time (from 80% to 20% of $V_{\text{DD}}$ )	8-mA drive, $C_L = 16 \text{ pF}$	-	2	3	ns

Table 22-23. EPI SDRAM Interface Characteristics<sup>a</sup>

Parameter No	Parameter	Parameter Name	Min	Nom	Max	Unit
E1	$t_{\text{CK}}$	SDRAM Clock period	20	-	-	ns
E2	$t_{\text{CH}}$	SDRAM Clock high time	10	-	-	ns
E3	$t_{\text{CL}}$	SDRAM Clock low time	10	-	-	ns
E4	$t_{\text{COV}}$	CLK to output valid	-5	-	5	ns
E5	$t_{\text{COI}}$	CLK to output invalid	-5	-	5	ns
E6	$t_{\text{COT}}$	CLK to output tristate	-5	-	5	ns
E7	$t_{\text{S}}$	Input set up to CLK	10	-	-	ns
E8	$t_{\text{H}}$	CLK to input hold	0	-	-	ns
E9	$t_{\text{PU}}$	Power-up time	100	-	-	$\mu\text{s}$
E10	$t_{\text{RP}}$	Precharge all banks	20	-	-	ns
E11	$t_{\text{RFC}}$	Auto refresh	66	-	-	ns
E12	$t_{\text{MRD}}$	Program mode register	40	40	40	ns

a. The EPI SDRAM interface must use 8-mA drive.

Figure 22-12. SDRAM Initialization and Load Mode Register Timing



Notes:

1. If CS is high at clock high time, all applied commands are NOP.
2. The **Mode** register may be loaded prior to the auto refresh cycles if desired.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed High-Z after command is issued.

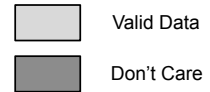


Figure 22-13. SDRAM Read Timing

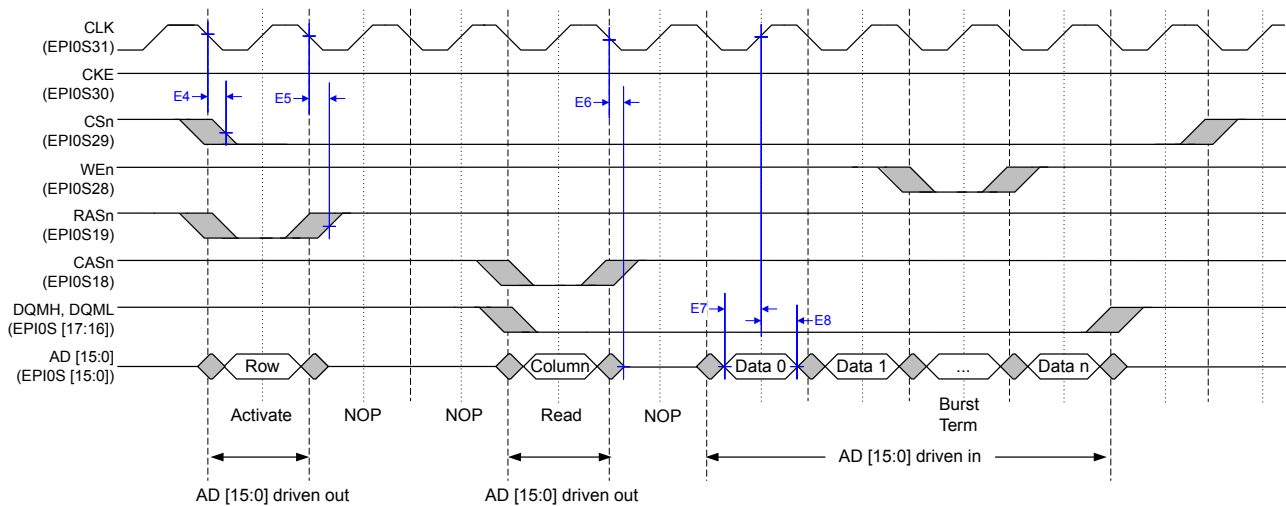


Figure 22-14. SDRAM Write Timing

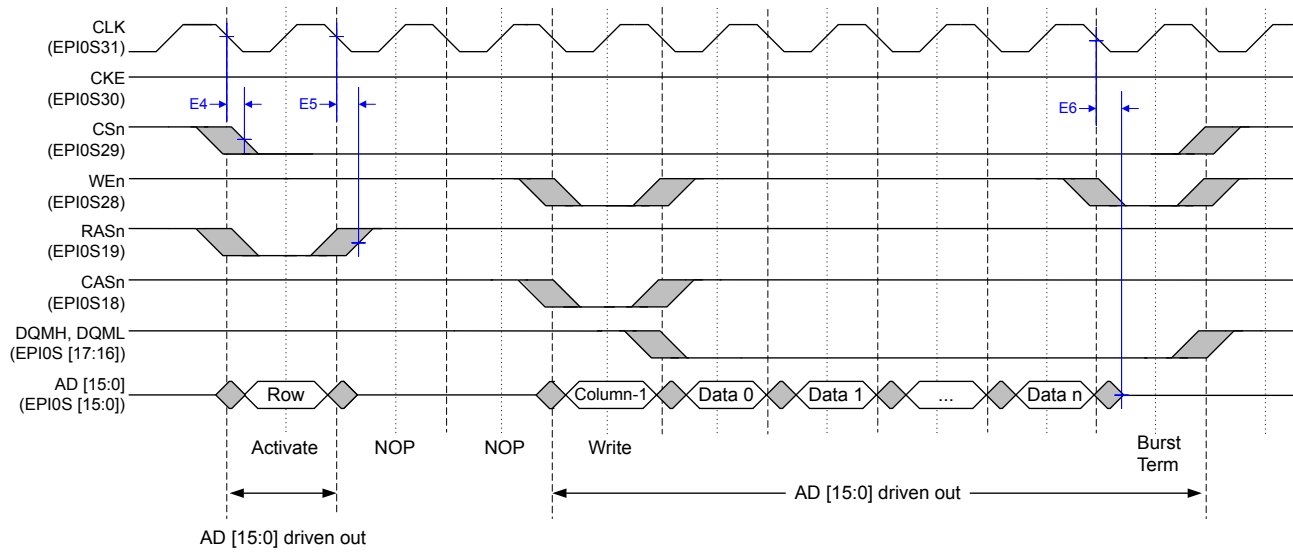


Table 22-24. EPI Host-Bus 8 and Host-Bus 16 Interface Characteristics

Parameter No	Parameter	Parameter Name	Min	Nom	Max	Unit
E14	$t_{ISU}$	Read data set up time	10	-	-	ns
E15	$t_{IH}$	Read data hold time	10	-	-	ns
E16	$t_{DV}$	WEn to write data valid	-	-	5	ns
E17	$t_{DI}$	Data hold from WEn invalid	2	-	-	EPI Clocks
E18	$t_{OV}$	CSn to output valid	-5	-	5	ns
E19	$t_{OINV}$	CSn to output invalid	-5	-	5	ns
E20	$t_{STLOW}$	WEn / RDn strobe width low	2	-	-	EPI Clocks
E21	$t_{FIFO}$	FEMPTY and FFULL setup time to clock edge	2	-	-	System Clocks
E22	$t_{ALEHIGH}$	ALE width high	1	-	-	EPI Clocks
E23	$t_{CSLOW}$	CSn width low	4	-	-	EPI Clocks
E24	$t_{ALEST}$	ALE rising to WEn / RDn strobe falling	2	-	-	EPI Clocks

Figure 22-15. Host-Bus 8/16 Mode Read Timing

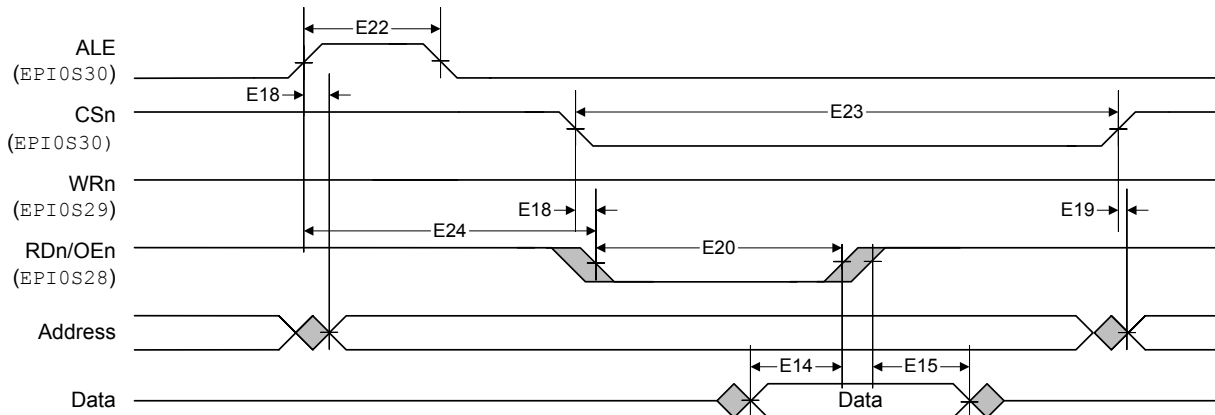


Figure 22-16. Host-Bus 8/16 Mode Write Timing

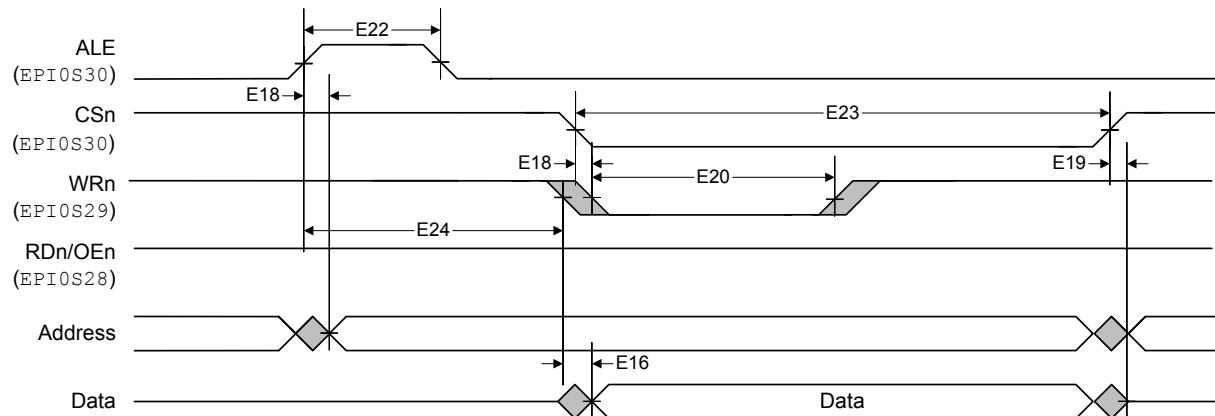
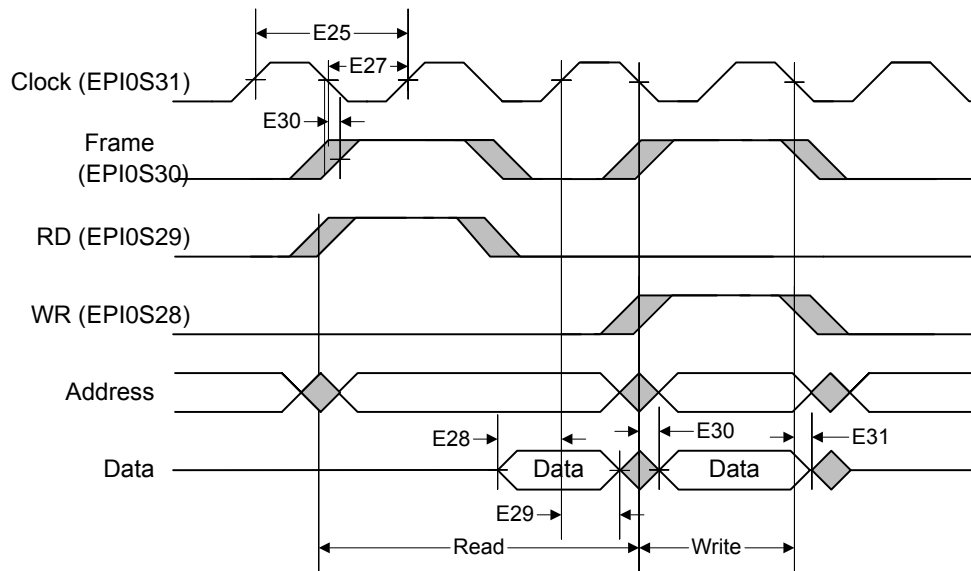
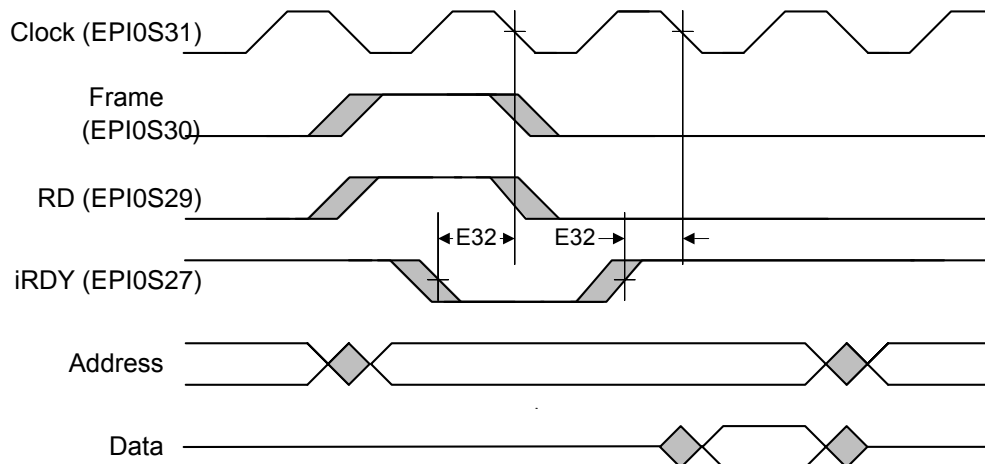


Table 22-25. EPI General-Purpose Interface Characteristics

Parameter No	Parameter	Parameter Name	Min	Nom	Max	Unit
E25	$t_{CK}$	General-Purpose Clock period	20	-	-	ns
E26	$t_{CH}$	General-Purpose Clock high time	10	-	-	ns
E27	$t_{CL}$	General-Purpose Clock low time	10	-	-	ns
E28	$t_{ISU}$	Input signal set up time to rising clock edge	10	-	-	ns
E29	$t_{IH}$	Input signal hold time from rising clock edge	10	-	-	ns
E30	$t_{DV}$	Falling clock edge to output valid	-5	-	5	ns
E31	$t_{DI}$	Falling clock edge to output invalid	-5	-	5	ns
E32	$t_{RDYSU}$	iRDY assertion or deassertion set up time to falling clock edge	20	-	-	ns

**Figure 22-17. General-Purpose Mode Read and Write Timing**

The above figure illustrates accesses where the `FRM50` bit is clear, the `FRMCNT` field is `0x0`, the `RD2CYC` bit is clear, and the `WR2CYC` bit is clear.

**Figure 22-18. General-Purpose Mode iRDY Timing**

## 22.2.9 Analog-to-Digital Converter

**Table 22-26. ADC Characteristics<sup>a</sup>**

Parameter	Parameter Name	Min	Nom	Max	Unit
$V_{ADCIN}$	Maximum single-ended, full-scale analog input voltage	-	-	3.0	V
	Minimum single-ended, full-scale analog input voltage	0.0	-	-	V
	Maximum differential, full-scale analog input voltage	-	-	1.5	V
	Minimum differential, full-scale analog input voltage	0.0	-	-	V

Table 22-26. ADC Characteristics (continued)

Parameter	Parameter Name	Min	Nom	Max	Unit
N	Resolution	10			bits
$f_{ADC}$	ADC internal clock frequency <sup>b</sup>	14	16	18	MHz
$t_{ADCCONV}$	Conversion time <sup>c</sup>	1			$\mu$ s
$f_{ADCCONV}$	Conversion rate <sup>c</sup>	1000			k samples/s
$t_{LT}$	Latency from trigger to start of conversion	-	2	-	system clocks
$I_L$	ADC input leakage	-	-	$\pm 1.0$	$\mu$ A
$R_{ADC}$	ADC equivalent resistance	-	-	10	k $\Omega$
$C_{ADC}$	ADC equivalent capacitance	0.9	1.0	1.1	pF
$E_L$	Integral nonlinearity error	-	-	$\pm 1$	LSB
$E_D$	Differential nonlinearity error	-	-	$\pm 1$	LSB
$E_O$	Offset error	-	-	$\pm 1$	LSB
$E_G$	Full-scale gain error	-	-	$\pm 3$	LSB
$E_{TS}$	Temperature sensor accuracy	-	-	$\pm 5$	$^{\circ}$ C

- a. The ADC reference voltage is 3.0 V. This reference voltage is internally generated from the 3.3 VDDA supply by a band gap circuit.
- b. The ADC must be clocked from the PLL or directly from an external clock source to operate properly.
- c. The conversion time and rate scale from the specified number if the ADC internal clock frequency is any value other than 16 MHz.

Figure 22-19. ADC Input Equivalency Diagram

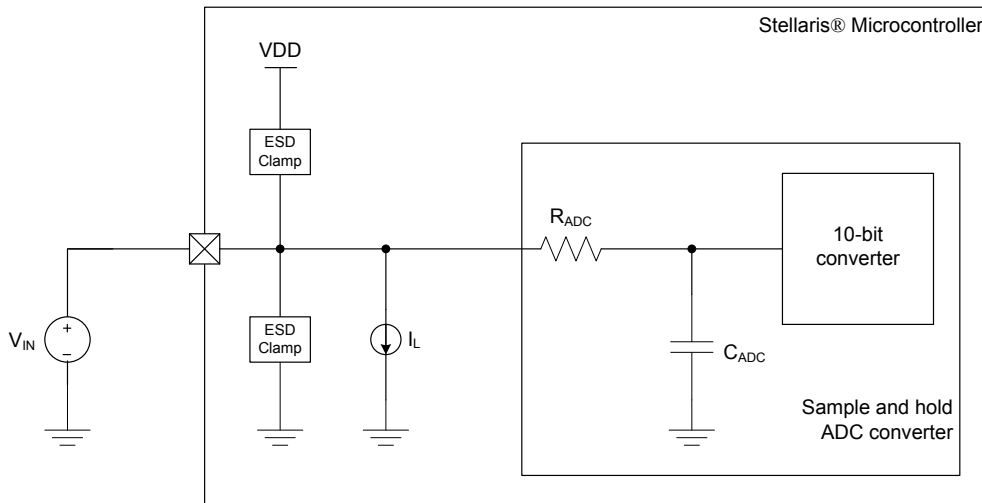


Table 22-27. ADC Module External Reference Characteristics<sup>a</sup>

Parameter	Parameter Name	Min	Nom	Max	Unit
$I_L$	External voltage reference leakage current	-	$\pm 1.0$	-	$\mu$ A

- a. Care must be taken to supply a reference voltage of acceptable quality.

Table 22-28. ADC Module Internal Reference Characteristics

Parameter	Parameter Name	Min	Nom	Max	Unit
V <sub>REFI</sub>	Internal voltage reference for ADC	-	3.0	-	V
E <sub>IR</sub>	Internal voltage reference error	-	-	±2.5	%

## 22.2.10 Synchronous Serial Interface (SSI)

Table 22-29. SSI Characteristics

Parameter No.	Parameter	Parameter Name	Min	Nom	Max	Unit
S1	t <sub>CLK_PER</sub>	SSIClk cycle time	2	-	65024	system clocks
S2	t <sub>CLK_HIGH</sub>	SSIClk high time	-	0.5	-	t clk_per
S3	t <sub>CLK_LOW</sub>	SSIClk low time	-	0.5	-	t clk_per
S4	t <sub>CLKRF</sub>	SSIClk rise/fall time	-	7.4	26	ns
S5	t <sub>DMD</sub>	Data from master valid delay time	0	-	1	system clocks
S6	t <sub>DMS</sub>	Data from master setup time	1	-	-	system clocks
S7	t <sub>DMH</sub>	Data from master hold time	2	-	-	system clocks
S8	t <sub>DSS</sub>	Data from slave setup time	1	-	-	system clocks
S9	t <sub>DSH</sub>	Data from slave hold time	2	-	-	system clocks

Figure 22-20. SSI Timing for TI Frame Format (FRF=01), Single Transfer Timing Measurement

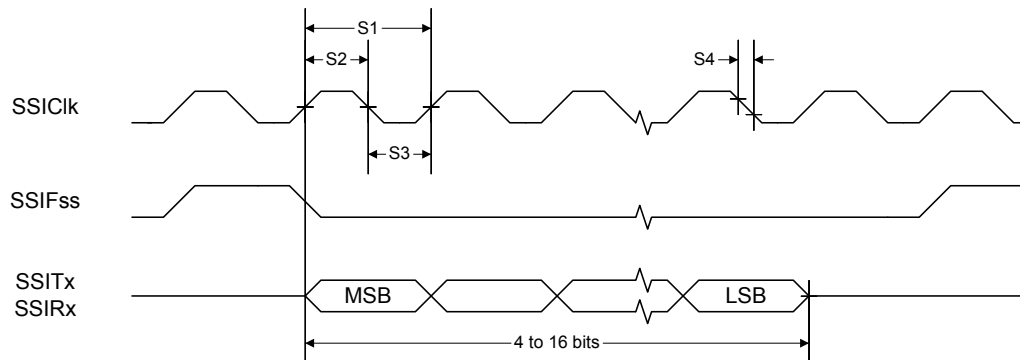


Figure 22-21. SSI Timing for MICROWIRE Frame Format (FRF=10), Single Transfer

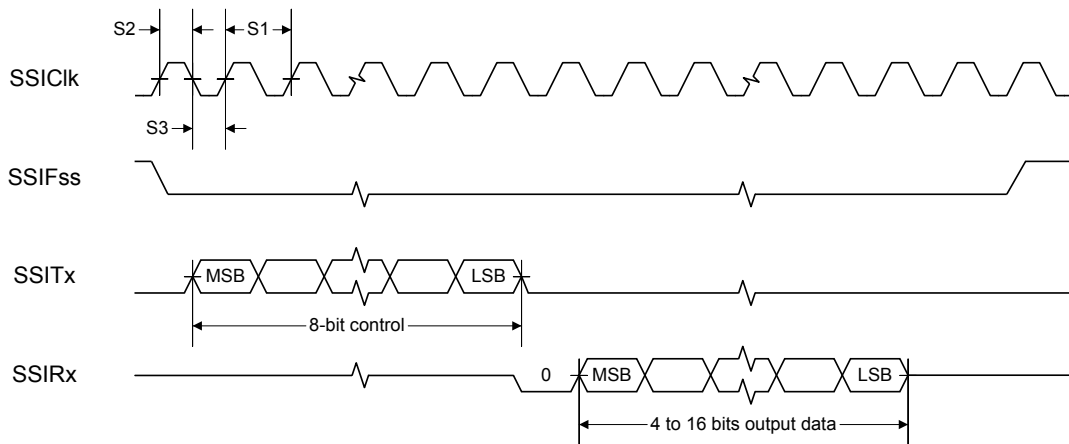
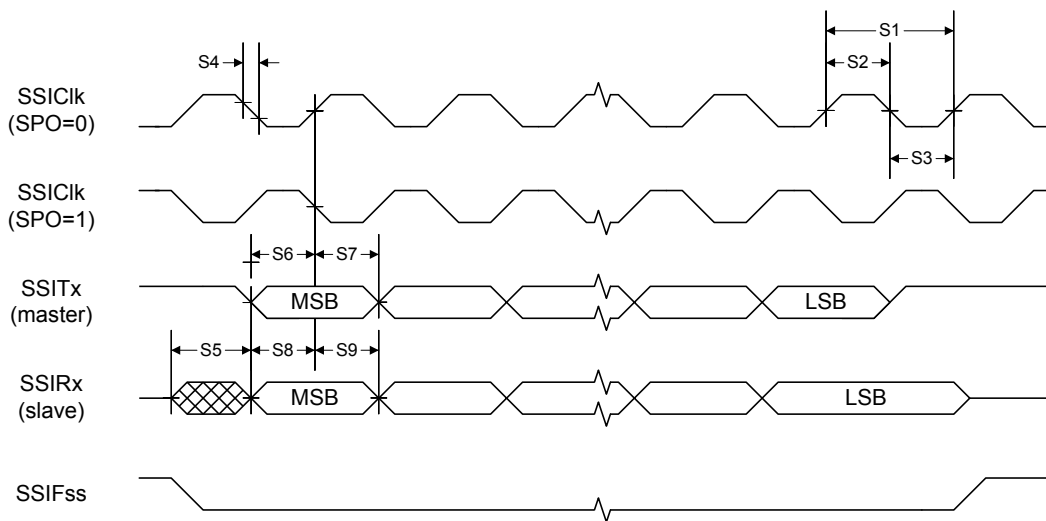
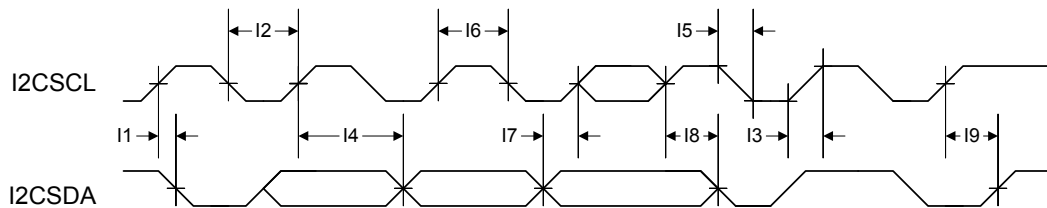


Figure 22-22. SSI Timing for SPI Frame Format (FRF=00), with SPH=1



### 22.2.11 Inter-Integrated Circuit (I<sup>2</sup>C) Interface

Figure 22-23. I<sup>2</sup>C Timing





## 22.2.12 Analog Comparator

**Table 22-30. Analog Comparator Characteristics**

Parameter	Parameter Name	Min	Nom	Max	Unit
V <sub>OS</sub>	Input offset voltage	-	±10	±25	mV
V <sub>CM</sub>	Input common mode voltage range	0	-	V <sub>DD</sub> -1.5	V
C <sub>MRR</sub>	Common mode rejection ratio	50	-	-	dB
T <sub>RT</sub>	Response time	-	-	1	µs
T <sub>MC</sub>	Comparator mode change to Output Valid	-	-	10	µs

**Table 22-31. Analog Comparator Voltage Reference Characteristics**

Parameter	Parameter Name	Min	Nom	Max	Unit
R <sub>HR</sub>	Resolution high range	-	V <sub>DD</sub> /31	-	LSB
R <sub>LR</sub>	Resolution low range	-	V <sub>DD</sub> /23	-	LSB
A <sub>HR</sub>	Absolute accuracy high range	-	-	±1/2	LSB
A <sub>LR</sub>	Absolute accuracy low range	-	-	±1/4	LSB

# A Boot Loader

## A.1 Boot Loader Overview

The Stellaris<sup>®</sup> Boot Loader is executed from the ROM when the Flash memory is empty and is used to download code to the Flash memory of a device without the use of a debug interface. The boot loader uses a simple packet interface to provide synchronous communication with the device. The speed of the boot loader is determined by the internal oscillator (PIOSC) frequency as it does not enable the PLL. The following serial interfaces can be used:

- UART0
- SSI0
- I<sup>2</sup>C0

For simplicity, both the data format and communication protocol are identical for all serial interfaces.

See the *Stellaris<sup>®</sup> Boot Loader User's Guide* for information on the boot loader software.

## A.2 Serial Interfaces

This section describes how the boot loader operates using a serial interface.

### A.2.1 Serial Configuration

Once communication with the boot loader is established via one of the serial interfaces, that interface is used until the boot loader is reset or new code takes over. For example, once you start communicating using the SSI port, communications with the boot loader via the UART are disabled until the device is reset.

#### A.2.1.1 UART

The Universal Asynchronous Receivers/Transmitters (UART) communication uses a fixed serial format of 8 bits of data, no parity, and 1 stop bit. The baud rate used for communication is automatically detected by the boot loader and can be any valid baud rate supported by the host and the device. The auto detection sequence requires that the baud rate should be no more than 1/32 the internal oscillator (PIOSC) frequency of the board that is running the boot loader (which is at least 8.4 MHz, providing support for up to 262,500 baud). The maximum regular speed baud rate for any UART on a Stellaris<sup>®</sup> device is calculated as follows:

$$\text{Max Baud Rate} = \text{System Clock Frequency} / 16$$

In order to determine the baud rate, the boot loader must determine the relationship between the internal oscillator and the baud rate. With this information, the boot loader can configure the UART to the same baud rate as the host. This automatic baud-rate detection allows the host to use any valid baud rate to communicate with the device.

The method used to perform this automatic synchronization requires the host to send the boot loader two bytes that are both 0x55. With this series of pulses, the boot loader can calculate the ratios needed to program the UART to match the host's baud rate. After the host sends the pattern, it attempts to read back one byte of data from the UART. The boot loader returns the value of 0xCC to indicate successful detection of the baud rate. If this byte is not received after at least twice the time required to transfer the two bytes, the host can resend another pattern of 0x55, 0x55, and wait for the 0xCC byte again until the boot loader acknowledges that it has received a synchronization

pattern correctly. For example, the time to wait for data back from the boot loader should be calculated as at least  $2 \times (20 \text{ (bits/sync) / baud rate (bits/sec)})$ . For a baud rate of 115200, this time is  $2 \times (20 / 115200)$  or 0.35 ms.

### A.2.1.2 SSI

The Synchronous Serial Interface (SSI) port also uses a fixed serial format for communications, with the default framing defined as Motorola format with both the `SPH` and `SPO` bits set in the **SSICRO** register. See “Frame Formats” on page 613 for more information on formats for this transfer protocol. Like the UART, this interface has hardware requirements that limit the maximum frequency of the `SSIClk` signal to be at most 1/12 the internal oscillator (PIOSC) frequency of the board running the boot loader (which is at least 8.4 MHz, providing support for up to 700 KHz). Because the host device is the master, the SSI on the boot loader device does not need to determine the clock as it is provided directly by the host.

### A.2.1.3 I<sup>2</sup>C

The Inter-Integrated Circuit (I<sup>2</sup>C) port operates in slave mode with a slave address of 0x42. The I<sup>2</sup>C port works at both 100-kHz and 400-kHz `I2CSCL` clock frequency. Because the host device is the master, the I<sup>2</sup>C on the boot loader device does not need to determine the clock as it is provided directly by the host.

## A.2.2 Serial Packet Handling

All communications, with the exception of the UART auto-baud, are done via defined packets that are acknowledged (ACK) or not acknowledged (NAK) by the devices. The packets use the same format for receiving and sending packets, including the method used to acknowledge successful or unsuccessful reception of a packet.

### A.2.2.1 Packet Format

All packets sent and received from the device use the following byte-packed format.

```
struct
{
    unsigned char ucSize;
    unsigned char ucChecksum;
    unsigned char Data[];
};
```

<code>ucSize</code>	The first byte received holds the total size of the transfer including the size and checksum bytes.
<code>ucChecksum</code>	This holds a simple checksum of the bytes in the data buffer only. The algorithm is <code>Data[0]+Data[1]+...+Data[ucSize-3]</code> .
<code>Data</code>	This is the raw data intended for the device, which is formatted in some form of command interface. There should be <code>ucSize-2</code> bytes of data provided in this buffer to or from the device.

### A.2.2.2 Sending Packets

The actual bytes of the packet can be sent individually or all at once; the only limitation is that commands that cause Flash memory access should limit the download sizes to prevent losing bytes during Flash memory programming. This limitation is discussed further in the section that describes

the boot loader command, `COMMAND_SEND_DATA` (see “`COMMAND_SEND_DATA` (0x24)” on page 749).

Once the packet has been formatted correctly by the host, it should be sent out over the serial interface. Then the host should poll the interface for the first non-zero data returned from the device. The first non-zero byte is either an ACK (0xCC) or a NAK (0x33) byte from the device indicating the packet was received successfully (ACK) or unsuccessfully (NAK). This response does not indicate that the actual contents of the command issued in the data portion of the packet were valid, just that the packet was received correctly.

### **A.2.2.3 Receiving Packets**

The boot loader sends a packet of data in the same format that it receives a packet. The boot loader may transfer leading zero data before the first actual byte of data is sent out. The first non-zero byte is the size of the packet followed by a checksum byte and finally followed by the data itself. The data is sent without a break after the first non-zero byte is sent from the boot loader. Once the device communicating with the boot loader receives all the bytes, it must either ACK or NAK the packet to indicate that the transmission was successful. The appropriate response after sending a NAK to the boot loader is to resend the command that failed and request the data again. If needed, the host may send leading zeros before sending down the ACK/NAK signal to the boot loader, as the boot loader only accepts the first non-zero data as a valid response. This zero padding is needed by the SSI interface in order to receive data to or from the boot loader.

## **A.2.3 Serial Commands**

The next section defines the list of commands that can be sent to the boot loader. The first byte of the data should always be one of the defined commands, followed by data or parameters as determined by the command that is sent.

### **A.2.3.1 COMMAND\_PING (0X20)**

This command simply accepts the command and sets the global status to success. The format of the packet is as follows:

```
Byte[0] = 0x03;  
Byte[1] = checksum(Byte[2]);  
Byte[2] = COMMAND_PING;
```

The ping command has 3 bytes and the value for `COMMAND_PING` is 0x20 and the checksum of one byte is that same byte, making `Byte[1]` also 0x20. Because the ping command has no real return status, the receipt of an ACK can be interpreted as a successful ping to the boot loader.

### **A.2.3.2 COMMAND\_DOWNLOAD (0x21)**

This command is sent to the boot loader to indicate where to store data and how many bytes will be sent by the `COMMAND_SEND_DATA` commands that follow. The command consists of two 32-bit values that are both transferred MSB first. The first 32-bit value is the address to start programming data into, while the second is the 32-bit size of the data that will be sent. This command also triggers an erase of the full area to be programmed so this command takes longer than other commands and results in a longer time to receive the ACK/NAK back from the board. This command should be followed by a `COMMAND_GET_STATUS` to ensure that the Program Address and Program size are valid for the device running the boot loader.

The format of the packet to send this command is a follows:

```

Byte[0] = 11
Byte[1] = checksum(Bytes[2:10])
Byte[2] = COMMAND_DOWNLOAD
Byte[3] = Program Address [31:24]
Byte[4] = Program Address [23:16]
Byte[5] = Program Address [15:8]
Byte[6] = Program Address [7:0]
Byte[7] = Program Size [31:24]
Byte[8] = Program Size [23:16]
Byte[9] = Program Size [15:8]
Byte[10] = Program Size [7:0]

```

### A.2.3.3 COMMAND\_RUN (0x22)

This command is used to tell the boot loader to execute from the address passed as the parameter in this command. This command consists of a single 32-bit value that is interpreted as the address to execute. The 32-bit value is transmitted MSB first and the boot loader responds with an ACK signal back to the host device before actually executing the code at the given address. The ACK response tells the host that the command was received successfully, and the code is running.

```

Byte[0] = 7
Byte[1] = checksum(Bytes[2:6])
Byte[2] = COMMAND_RUN
Byte[3] = Execute Address[31:24]
Byte[4] = Execute Address[23:16]
Byte[5] = Execute Address[15:8]
Byte[6] = Execute Address[7:0]

```

### A.2.3.4 COMMAND\_GET\_STATUS (0x23)

This command returns the status of the last command that was issued. Typically, this command should be sent after every command to ensure that the previous command was successful or to properly respond to a failure. The command requires one byte in the data of the packet and should be followed by reading a packet with one byte of data that contains a status code. The last step is to ACK or NAK the received data so the boot loader knows that the data has been read.

```

Byte[0] = 0x03
Byte[1] = checksum(Byte[2])
Byte[2] = COMMAND_GET_STATUS

```

### A.2.3.5 COMMAND\_SEND\_DATA (0x24)

This command should only follow a COMMAND\_DOWNLOAD command or another COMMAND\_SEND\_DATA command if more data is needed. Consecutive send data commands automatically increment address and continue programming from the previous location. For packets which do not contain the final portion of the downloaded data, a multiple of four bytes should always be transferred. The command terminates programming once the number of bytes indicated by the COMMAND\_DOWNLOAD command has been received. Each time this function is called, it should be followed by a COMMAND\_GET\_STATUS to ensure that the data was successfully programmed into the Flash memory. If the boot loader sends a NAK to this command, the boot loader does not increment the current address to allow retransmission of the previous data. The following example shows a COMMAND\_SEND\_DATA packet with 8 bytes of packet data:

```
Byte[0] = 11
Byte[1] = checksum(Bytes[2:10])
Byte[2] = COMMAND_SEND_DATA
Byte[3] = Data[0]
Byte[4] = Data[1]
Byte[5] = Data[2]
Byte[6] = Data[3]
Byte[7] = Data[4]
Byte[8] = Data[5]
Byte[9] = Data[6]
Byte[10] = Data[7]
```

### **A.2.3.6 COMMAND\_RESET (0x25)**

This command is used to tell the boot loader device to reset. Unlike the `COMMAND_RUN`, this command allows the initial stack pointer to be read by the hardware and set up for the new code. `COMMAND_RESET` can also be used to reset the boot loader if a critical error occurs, and the host device wants to restart communication with the boot loader.

```
Byte[0] = 3
Byte[1] = checksum(Byte[2])
Byte[2] = COMMAND_RESET
```

The boot loader responds with an ACK signal back to the host device before actually executing the software reset to the device running the boot loader. The ACK tells the host that the command was received successfully and the part will be reset.

## B ROM DriverLib Functions

### B.1 DriverLib Functions Included in the Integrated ROM

The Stellaris® Peripheral Driver Library (DriverLib) APIs that are available in the integrated ROM of the Stellaris® family of devices are listed below. The detailed description of each function is available in the *Stellaris® ROM User's Guide*.

ROM\_ADCHardwareOversampleConfigure  
// Configures the hardware oversampling factor of the ADC.

ROM\_ADCIntClear  
// Clears sample sequence interrupt source.

ROM\_ADCIntDisable  
// Disables a sample sequence interrupt.

ROM\_ADCIntEnable  
// Enables a sample sequence interrupt.

ROM\_ADCIntStatus  
// Gets the current interrupt status.

ROM\_ADCProcessorTrigger  
// Causes a processor trigger for a sample sequence.

ROM\_ADCSequenceConfigure  
// Configures the trigger source and priority of a sample sequence.

ROM\_ADCSequenceDataGet  
// Gets the captured data for a sample sequence.

ROM\_ADCSequenceDisable  
// Disables a sample sequence.

ROM\_ADCSequenceEnable  
// Enables a sample sequence.

ROM\_ADCSequenceOverflow  
// Determines if a sample sequence overflow occurred.

ROM\_ADCSequenceOverflowClear  
// Clears the overflow condition on a sample sequence.

ROM\_ADCSequenceStepConfigure  
// Configure a step of the sample sequencer.

ROM\_ADCSequenceUnderflow  
// Determines if a sample sequence underflow occurred.

ROM\_ADCSequenceUnderflowClear  
// Clears the underflow condition on a sample sequence.

ROM\_ComparatorConfigure  
// Configures a comparator.

ROM\_ComparatorIntClear  
// Clears a comparator interrupt.

ROM\_ComparatorIntDisable  
// Disables the comparator interrupt.

ROM\_ComparatorIntEnable  
// Enables the comparator interrupt.

ROM\_ComparatorIntStatus  
// Gets the current interrupt status.

ROM\_ComparatorRefSet  
// Sets the internal reference voltage.

ROM\_ComparatorValueGet  
// Gets the current comparator output value.

ROM\_Crc16Array  
// Calculates the CRC-16 of an array of words.

ROM\_Crc16Array3  
// Calculates three CRC-16s of an array of words.

ROM\_FlashErase  
// Erases a block of flash.

ROM\_FlashIntClear  
// Clears flash controller interrupt sources.

ROM\_FlashIntDisable  
// Disables individual flash controller interrupt sources.

ROM\_FlashIntEnable  
// Enables individual flash controller interrupt sources.

ROM\_FlashIntGetStatus  
// Gets the current interrupt status.

ROM\_FlashProgram  
// Programs flash.

ROM\_FlashProtectGet  
// Gets the protection setting for a block of flash.

ROM\_FlashProtectSave  
// Saves the flash protection settings.

ROM\_FlashProtectSet  
// Sets the protection setting for a block of flash.



```
ROM_FlashUsecGet
    // Gets the number of processor clocks per micro-second.

ROM_FlashUsecSet
    // Sets the number of processor clocks per micro-second.

ROM_FlashUserGet
    // Gets the user registers.

ROM_FlashUserSave
    // Saves the user registers.

ROM_FlashUserSet
    // Sets the user registers.

ROM_GPIODirModeGet
    // Gets the direction and mode of a pin.

ROM_GPIODirModeSet
    // Sets the direction and mode of the specified pin(s).

ROM_GPIOIntTypeGet
    // Gets the interrupt type for a pin.

ROM_GPIOIntTypeSet
    // Sets the interrupt type for the specified pin(s).

ROM_GPIOPadConfigGet
    // Gets the pad configuration for a pin.

ROM_GPIOPadConfigSet
    // Sets the pad configuration for the specified pin(s).

ROM_GPIOPinConfigure
    // Configures the alternate function of a GPIO pin.

ROM_GPIOPinIntClear
    // Clears the interrupt for the specified pin(s).

ROM_GPIOPinIntDisable
    // Disables interrupts for the specified pin(s).

ROM_GPIOPinIntEnable
    // Enables interrupts for the specified pin(s).

ROM_GPIOPinIntStatus
    // Gets interrupt status for the specified GPIO port.

ROM_GPIOPinRead
    // Reads the values present of the specified pin(s).

ROM_GPIOPinTypeADC
    // Configures pin(s) for use as analog-to-digital converter inputs.
```

ROM\_GPIOPinTypeComparator  
// Configures pin(s) for use as an analog comparator input.

ROM\_GPIOPinTypeGPIOInput  
// Configures pin(s) for use as GPIO inputs.

ROM\_GPIOPinTypeGPIOOutput  
// Configures pin(s) for use as GPIO outputs.

ROM\_GPIOPinTypeGPIOOutputOD  
// Configures pin(s) for use as GPIO open drain outputs.

ROM\_GPIOPinTypeI2C  
// Configures pin(s) for use by the I2C peripheral.

ROM\_GPIOPinTypeSSI  
// Configures pin(s) for use by the SSI peripheral.

ROM\_GPIOPinTypeTimer  
// Configures pin(s) for use by the Timer peripheral.

ROM\_GPIOPinTypeUART  
// Configures pin(s) for use by the UART peripheral.

ROM\_GPIOPinWrite  
// Writes a value to the specified pin(s).

ROM\_HibernateClockSelect  
// Selects the clock input for the Hibernation module.

ROM\_HibernateDataGet  
// Reads a set of data from the non-volatile memory of the Hibernation module.

ROM\_HibernateDataSet  
// Stores data in the non-volatile memory of the Hibernation module.

ROM\_HibernateDisable  
// Disables the Hibernation module for operation.

ROM\_HibernateEnableExpClk  
// Enables the Hibernation module for operation.

ROM\_HibernateIntClear  
// Clears pending interrupts from the Hibernation module.

ROM\_HibernateIntDisable  
// Disables interrupts for the Hibernation module.

ROM\_HibernateIntEnable  
// Enables interrupts for the Hibernation module.

ROM\_HibernateIntStatus  
// Gets the current interrupt status of the Hibernation module.

ROM\_HibernatelsActive  
// Checks to see if the Hibernation module is already powered up.

ROM\_HibernateLowBatGet  
// Gets the currently configured low battery detection behavior.

ROM\_HibernateLowBatSet  
// Configures the low battery detection.

ROM\_HibernateRequest  
// Requests hibernation mode.

ROM\_HibernateRTCDisable  
// Disables the RTC feature of the Hibernation module.

ROM\_HibernateRTCEnable  
// Enables the RTC feature of the Hibernation module.

ROM\_HibernateRTCGet  
// Gets the value of the real time clock (RTC) counter.

ROM\_HibernateRTCMatch0Get  
// Gets the value of the RTC match 0 register.

ROM\_HibernateRTCMatch0Set  
// Sets the value of the RTC match 0 register.

ROM\_HibernateRTCMatch1Get  
// Gets the value of the RTC match 1 register.

ROM\_HibernateRTCMatch1Set  
// Sets the value of the RTC match 1 register.

ROM\_HibernateRTCSet  
// Sets the value of the real time clock (RTC) counter.

ROM\_HibernateRTCTrimGet  
// Gets the value of the RTC predivider trim register.

ROM\_HibernateRTCTrimSet  
// Sets the value of the RTC predivider trim register.

ROM\_HibernateWakeGet  
// Gets the currently configured wake conditions for the Hibernation module.

ROM\_HibernateWakeSet  
// Configures the wake conditions for the Hibernation module.

ROM\_I2CMasterBusBusy  
// Indicates whether or not the I2C bus is busy.

ROM\_I2CMasterBusy  
// Indicates whether or not the I2C Master is busy.

ROM\_I2CMasterControl  
// Controls the state of the I2C Master module.

ROM\_I2CMasterDataGet  
// Receives a byte that has been sent to the I2C Master.

ROM\_I2CMasterDataPut  
// Transmits a byte from the I2C Master.

ROM\_I2CMasterDisable  
// Disables the I2C master block.

ROM\_I2CMasterEnable  
// Enables the I2C Master block.

ROM\_I2CMasterErr  
// Gets the error status of the I2C Master module.

ROM\_I2CMasterInitExpClk  
// Initializes the I2C Master block.

ROM\_I2CMasterIntClear  
// Clears I2C Master interrupt sources.

ROM\_I2CMasterIntDisable  
// Disables the I2C Master interrupt.

ROM\_I2CMasterIntEnable  
// Enables the I2C Master interrupt.

ROM\_I2CMasterIntStatus  
// Gets the current I2C Master interrupt status.

ROM\_I2CMasterSlaveAddrSet  
// Sets the address that the I2C Master will place on the bus.

ROM\_I2CSlaveDataGet  
// Receives a byte that has been sent to the I2C Slave.

ROM\_I2CSlaveDataPut  
// Transmits a byte from the I2C Slave.

ROM\_I2CSlaveDisable  
// Disables the I2C slave block.

ROM\_I2CSlaveEnable  
// Enables the I2C Slave block.

ROM\_I2CSlaveInit  
// Initializes the I2C Slave block.

ROM\_I2CSlaveIntClear  
// Clears I2C Slave interrupt sources.

```
ROM_I2CSlaveIntClearEx
    // Clears I2C Slave interrupt sources.

ROM_I2CSlaveIntDisable
    // Disables the I2C Slave interrupt.

ROM_I2CSlaveIntDisableEx
    // Disables individual I2C Slave interrupt sources.

ROM_I2CSlaveIntEnable
    // Enables the I2C Slave interrupt.

ROM_I2CSlaveIntEnableEx
    // Enables individual I2C Slave interrupt sources.

ROM_I2CSlaveIntStatus
    // Gets the current I2C Slave interrupt status.

ROM_I2CSlaveIntStatusEx
    // Gets the current I2C Slave interrupt status.

ROM_I2CSlaveStatus
    // Gets the I2C Slave module status.

ROM_IntDisable
    // Disables an interrupt.

ROM_IntEnable
    // Enables an interrupt.

ROM_IntMasterDisable
    // Disables the processor interrupt.

ROM_IntMasterEnable
    // Enables the processor interrupt.

ROM_IntPriorityGet
    // Gets the priority of an interrupt.

ROM_IntPriorityGroupingGet
    // Gets the priority grouping of the interrupt controller.

ROM_IntPriorityGroupingSet
    // Sets the priority grouping of the interrupt controller.

ROM_IntPrioritySet
    // Sets the priority of an interrupt.

ROM_MPUDisable
    // Disables the MPU for use.

ROM_MPUEnable
    // Enables and configures the MPU for use.
```

ROM\_MPURegionCountGet  
// Gets the count of regions supported by th MPU.

ROM\_MPURegionDisable  
// Disables a specific region.

ROM\_MPURegionEnable  
// Enables a specific region.

ROM\_MPURegionGet  
// Gets the current settings for a specific region.

ROM\_MPURegionSet  
// Sets up the access rules for a specific region.

ROM\_SSIConfigSetExpClk  
// Configures the synchronous serial interface.

ROM\_SSIDataGet  
// Gets a data element from the SSI receive FIFO.

ROM\_SSIDataGetNonBlocking  
// Gets a data element from the SSI receive FIFO.

ROM\_SSIDataPut  
// Puts a data element into the SSI transmit FIFO.

ROM\_SSIDataPutNonBlocking  
// Puts a data element into the SSI transmit FIFO.

ROM\_SSIDisable  
// Disables the synchronous serial interface.

ROM\_SSIDMADisable  
// Disable SSI DMA operation.

ROM\_SSIDMAEnable  
// Enable SSI DMA operation.

ROM\_SSIEnable  
// Enables the synchronous serial interface.

ROM\_SSIIntClear  
// Clears SSI interrupt sources.

ROM\_SSIIntDisable  
// Disables individual SSI interrupt sources.

ROM\_SSIIntEnable  
// Enables individual SSI interrupt sources.

ROM\_SSIIntStatus  
// Gets the current interrupt status.

ROM\_SysCtlADCSpeedGet  
// Gets the sample rate of the ADC.

ROM\_SysCtlADCSpeedSet  
// Sets the sample rate of the ADC.

ROM\_SysCtlClockGet  
// Gets the processor clock rate.

ROM\_SysCtlClockSet  
// Sets the clocking of the device.

ROM\_SysCtlDeepSleep  
// Puts the processor into deep-sleep mode.

ROM\_SysCtlDelay  
// Provides a small delay.

ROM\_SysCtlFlashSizeGet  
// Gets the size of the flash.

ROM\_SysCtlGPIOAHBDisable  
// Disables a GPIO peripheral for access from the AHB.

ROM\_SysCtlGPIOAHBEnable  
// Enables a GPIO peripheral for access from the AHB.

ROM\_SysCtlIntClear  
// Clears system control interrupt sources.

ROM\_SysCtlIntDisable  
// Disables individual system control interrupt sources.

ROM\_SysCtlIntEnable  
// Enables individual system control interrupt sources.

ROM\_SysCtlIntStatus  
// Gets the current interrupt status.

ROM\_SysCtlLDOGet  
// Gets the output voltage of the LDO.

ROM\_SysCtlLDOSet  
// Sets the output voltage of the LDO.

ROM\_SysCtlPeripheralClockGating  
// Controls peripheral clock gating in sleep and deep-sleep mode.

ROM\_SysCtlPeripheralDeepSleepDisable  
// Disables a peripheral in deep-sleep mode.

ROM\_SysCtlPeripheralDeepSleepEnable  
// Enables a peripheral in deep-sleep mode.

ROM\_SysCtlPeripheralDisable  
// Disables a peripheral.

ROM\_SysCtlPeripheralEnable  
// Enables a peripheral.

ROM\_SysCtlPeripheralPresent  
// Determines if a peripheral is present.

ROM\_SysCtlPeripheralReset  
// Performs a software reset of a peripheral.

ROM\_SysCtlPeripheralSleepDisable  
// Disables a peripheral in sleep mode.

ROM\_SysCtlPeripheralSleepEnable  
// Enables a peripheral in sleep mode.

ROM\_SysCtlPinPresent  
// Determines if a pin is present.

ROM\_SysCtlReset  
// Resets the device.

ROM\_SysCtlResetCauseClear  
// Clears reset reasons.

ROM\_SysCtlResetCauseGet  
// Gets the reason for a reset.

ROM\_SysCtlSleep  
// Puts the processor into sleep mode.

ROM\_SysCtlSRAMSizeGet  
// Gets the size of the SRAM.

ROM\_SysTickDisable  
// Disables the SysTick counter.

ROM\_SysTickEnable  
// Enables the SysTick counter.

ROM\_SysTickIntDisable  
// Disables the SysTick interrupt.

ROM\_SysTickIntEnable  
// Enables the SysTick interrupt.

ROM\_SysTickPeriodGet  
// Gets the period of the SysTick counter.

ROM\_SysTickPeriodSet  
// Sets the period of the SysTick counter.



---

```
ROM_SysTickValueGet
    // Gets the current value of the SysTick counter.

ROM_TimerConfigure
    // Configures the timer(s).

ROM_TimerControlEvent
    // Controls the event type.

ROM_TimerControlLevel
    // Controls the output level.

ROM_TimerControlStall
    // Controls the stall handling.

ROM_TimerControlTrigger
    // Enables or disables the trigger output.

ROM_TimerDisable
    // Disables the timer(s).

ROM_TimerEnable
    // Enables the timer(s).

ROM_TimerIntClear
    // Clears timer interrupt sources.

ROM_TimerIntDisable
    // Disables individual timer interrupt sources.

ROM_TimerIntEnable
    // Enables individual timer interrupt sources.

ROM_TimerIntStatus
    // Gets the current interrupt status.

ROM_TimerLoadGet
    // Gets the timer load value.

ROM_TimerLoadSet
    // Sets the timer load value.

ROM_TimerMatchGet
    // Gets the timer match value.

ROM_TimerMatchSet
    // Sets the timer match value.

ROM_TimerPrescaleGet
    // Get the timer prescale value.

ROM_TimerPrescaleSet
    // Set the timer prescale value.
```

ROM\_TimerRTCDisable  
// Disable RTC counting.

ROM\_TimerRTCEnable  
// Enable RTC counting.

ROM\_TimerValueGet  
// Gets the current timer value.

ROM\_UARTBreakCtl  
// Causes a BREAK to be sent.

ROM\_UARTBusy  
// Determines whether the UART transmitter is busy or not.

ROM\_UARTCharGet  
// Waits for a character from the specified port.

ROM\_UARTCharGetNonBlocking  
// Receives a character from the specified port.

ROM\_UARTCharPut  
// Waits to send a character from the specified port.

ROM\_UARTCharPutNonBlocking  
// Sends a character to the specified port.

ROM\_UARTCharsAvail  
// Determines if there are any characters in the receive FIFO.

ROM\_UARTConfigGetExpClk  
// Gets the current configuration of a UART.

ROM\_UARTConfigSetExpClk  
// Sets the configuration of a UART.

ROM\_UARTDisable  
// Disables transmitting and receiving.

ROM\_UARTDisableSIR  
// Disables SIR (IrDA) mode on the specified UART.

ROM\_UARTDMADisable  
// Disable UART DMA operation.

ROM\_UARTDMAEnable  
// Enable UART DMA operation.

ROM\_UARTEnable  
// Enables transmitting and receiving.

ROM\_UARTEnableSIR  
// Enables SIR (IrDA) mode on the specified UART.

ROM\_UARTFIFODisable  
// Disables the transmit and receive FIFOs.

ROM\_UARTFIFOEnable  
// Enables the transmit and receive FIFOs.

ROM\_UARTFIFOLevelGet  
// Gets the FIFO level at which interrupts are generated.

ROM\_UARTFIFOLevelSet  
// Sets the FIFO level at which interrupts are generated.

ROM\_UARTIntClear  
// Clears UART interrupt sources.

ROM\_UARTIntDisable  
// Disables individual UART interrupt sources.

ROM\_UARTIntEnable  
// Enables individual UART interrupt sources.

ROM\_UARTIntStatus  
// Gets the current interrupt status.

ROM\_UARTParityModeGet  
// Gets the type of parity currently being used.

ROM\_UARTParityModeSet  
// Sets the type of parity.

ROM\_UARTRxErrorClear  
// Clears all reported receiver errors.

ROM\_UARTRxErrorGet  
// Gets current receiver errors.

ROM\_UARTSpaceAvail  
// Determines if there is any space in the transmit FIFO.

ROM\_UARTTxIntModeGet  
// Returns the current operating mode for the UART transmit interrupt.

ROM\_UARTTxIntModeSet  
// Sets the operating mode for the UART transmit interrupt.

ROM\_uDMAChannelAttributeDisable  
// Disables attributes of a uDMA channel.

ROM\_uDMAChannelAttributeEnable  
// Enables attributes of a uDMA channel.

ROM\_uDMAChannelAttributeGet  
// Gets the enabled attributes of a uDMA channel.

ROM\_uDMAChannelControlSet  
// Sets the control parameters for a uDMA channel.

ROM\_uDMAChannelDisable  
// Disables a uDMA channel for operation.

ROM\_uDMAChannelEnable  
// Enables a uDMA channel for operation.

ROM\_uDMAChannelsEnabled  
// Checks if a uDMA channel is enabled for operation.

ROM\_uDMAChannelModeGet  
// Gets the transfer mode for a uDMA channel.

ROM\_uDMAChannelRequest  
// Requests a uDMA channel to start a transfer.

ROM\_uDMAChannelSelectDefault  
// Select the default peripheral for a set of uDMA channels.

ROM\_uDMAChannelSelectSecondary  
// Select the secondary peripheral for a set of uDMA channels.

ROM\_uDMAChannelSizeGet  
// Gets the current transfer size for a uDMA channel.

ROM\_uDMAChannelTransferSet  
// Sets the transfer parameters for a uDMA channel.

ROM\_uDMAControlBaseGet  
// Gets the base address for the channel control table.

ROM\_uDMAControlBaseSet  
// Sets the base address for the channel control table.

ROM\_uDMADisable  
// Disables the uDMA controller for use.

ROM\_uDMAEnable  
// Enables the uDMA controller for use.

ROM\_uDMAErrorStatusClear  
// Clears the uDMA error interrupt.

ROM\_uDMAErrorStatusGet  
// Gets the uDMA error status.

ROM\_uDMAIntClear  
// Clears uDMA interrupt status.

ROM\_uDMAIntStatus  
// Gets the uDMA controller channel interrupt status.

ROM\_UpdateI2C  
// Starts an update over the I2C0 interface.

ROM\_UpdateSSI  
// Starts an update over the SSI0 interface.

ROM\_UpdateUART  
// Starts an update over the UART0 interface.

ROM\_WatchdogEnable  
// Enables the watchdog timer.

ROM\_WatchdogIntClear  
// Clears the watchdog timer interrupt.

ROM\_WatchdogIntEnable  
// Enables the watchdog timer interrupt.

ROM\_WatchdogIntStatus  
// Gets the current watchdog timer interrupt status.

ROM\_WatchdogLock  
// Enables the watchdog timer lock mechanism.

ROM\_WatchdogLockState  
// Gets the state of the watchdog timer lock mechanism.

ROM\_WatchdogReloadGet  
// Gets the watchdog timer reload value.

ROM\_WatchdogReloadSet  
// Sets the watchdog timer reload value.

ROM\_WatchdogResetDisable  
// Disables the watchdog timer reset.

ROM\_WatchdogResetEnable  
// Enables the watchdog timer reset.

ROM\_WatchdogRunning  
// Determines if the watchdog timer is enabled.

ROM\_WatchdogStallDisable  
// Disables stalling of the watchdog timer during debug events.

ROM\_WatchdogStallEnable  
// Enables stalling of the watchdog timer during debug events.

ROM\_WatchdogUnlock  
// Disables the watchdog timer lock mechanism.

ROM\_WatchdogValueGet  
// Gets the current watchdog timer value.

# C Register Quick Reference

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
<b>System Control</b> Base 0x400F.E000																					
<b>DID0, type RO, offset 0x000, reset -</b>																					
VER								CLASS													
MAJOR								MINOR													
<b>PBORCTL, type R/W, offset 0x030, reset 0x0000.7FFD</b>																					
														BORIOR							
<b>RIS, type RO, offset 0x050, reset 0x0000.0000</b>																					
								MOSCPUPRIS				PLLLRIS				BORRIS					
<b>IMC, type R/W, offset 0x054, reset 0x0000.0000</b>																					
								MOSCPUPIM				PLLLIM				BORIM					
<b>MISC, type R/W1C, offset 0x058, reset 0x0000.0000</b>																					
								MOSCPUPMS				PLLLMIS				BORMIS					
<b>RESC, type R/W, offset 0x05C, reset -</b>																					
														MOSCFAIL							
				WDT1				SW		WDT0		BOR		POR		EXT					
<b>RCC, type R/W, offset 0x060, reset 0x0780.3AD1</b>																					
PWRDN				ACG		SYSDIV				USESYSIDV											
				BYPASS		XTAL				OSCSRC				IOSCDIS		MOSCDIS					
<b>PLLCFG, type RO, offset 0x064, reset -</b>																					
F								R													
<b>GPIOHBCTL, type R/W, offset 0x06C, reset 0x0000.0000</b>																					
				PORTJ		PORTH		PORTG		PORTF		PORTE		PORTD		PORTC		PORTB		PORTA	
<b>RCC2, type R/W, offset 0x070, reset 0x0780.6810</b>																					
USERCC2		DIV400		SYSDIV2				SYSDIV2LSB													
				PWRDN2		BYPASS2		OSCSRC2													
<b>MOSCCCTL, type R/W, offset 0x07C, reset 0x0000.0000</b>																					
														CVAL							
<b>DSLCLKCFG, type R/W, offset 0x144, reset 0x0780.0000</b>																					
DSDIVORIDE								DSOSCSRC													
<b>PIOSCCAL, type R/W, offset 0x150, reset 0x0000.0000</b>																					
UTEN				CAL				UPDATE				UT									
<b>PIOSCCSTAT, type RO, offset 0x154, reset 0x0000.0040</b>																					
								RESULT				DT				CT					
<b>DID1, type RO, offset 0x004, reset -</b>																					
VER				FAM				PARTNO													
PINCOUNT								TEMP				PKG		ROHS		QUAL					
<b>DC0, type RO, offset 0x008, reset 0x007F.007F</b>																					
								SRAMSZ													
								FLASHSZ													

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>DC1, type RO, offset 0x010, reset -</b>																
			WDT1												ADC0	
MINSYSDIV						MAXADC0SPD		MPU	HIB	TEMPSNS	PLL	WDT0	SWO	SWD	JTAG	
<b>DC2, type RO, offset 0x014, reset 0x430F.5037</b>																
	EPI0					COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0	
	I2C1		I2C0							SSI1	SSI0		UART2	UART1	UART0	
<b>DC3, type RO, offset 0x018, reset 0xBFFF.0FC0</b>																
32KHZ		CCP5	CCP4	CCP3	CCP2	CCP1	CCP0	ADC0AIN7	ADC0AIN6	ADC0AIN5	ADC0AIN4	ADC0AIN3	ADC0AIN2	ADC0AIN1	ADC0AIN0	
				C10	C1PLUS	C1MINUS	C00	C0PLUS	C0MINUS							
<b>DC4, type RO, offset 0x01C, reset 0x0004.F1FF</b>																
													PICAL			
CCP7	CCP6	UDMA	ROM				GPI0J	GPI0H	GPI0G	GPI0F	GPI0E	GPI0D	GPI0C	GPI0B	GPI0A	
<b>DC5, type RO, offset 0x020, reset 0x0000.0000</b>																
<b>DC6, type RO, offset 0x024, reset 0x0000.0000</b>																
<b>DC7, type RO, offset 0x028, reset 0xFFFF.FFFF</b>																
	DMACH30	DMACH29	DMACH28	DMACH27	DMACH26	DMACH25	DMACH24	DMACH23	DMACH22	DMACH21	DMACH20	DMACH19	DMACH18	DMACH17	DMACH16	
DMACH15	DMACH14	DMACH13	DMACH12	DMACH11	DMACH10	DMACH9	DMACH8	DMACH7	DMACH6	DMACH5	DMACH4	DMACH3	DMACH2	DMACH1	DMACH0	
<b>DC8, type RO, offset 0x02C, reset 0x0000.00FF</b>																
								ADC0AIN7	ADC0AIN6	ADC0AIN5	ADC0AIN4	ADC0AIN3	ADC0AIN2	ADC0AIN1	ADC0AIN0	
<b>DC9, type RO, offset 0x190, reset 0x0000.00FF</b>																
								ADC0DC7	ADC0DC6	ADC0DC5	ADC0DC4	ADC0DC3	ADC0DC2	ADC0DC1	ADC0DC0	
<b>NVMSTAT, type RO, offset 0x1A0, reset 0x0000.0001</b>																
															FWB	
<b>RCGC0, type R/W, offset 0x100, reset 0x00000040</b>																
			WDT1												ADC0	
						MAXADC0SPD			HIB			WDT0				
<b>SCGC0, type R/W, offset 0x110, reset 0x00000040</b>																
			WDT1												ADC0	
						MAXADC0SPD			HIB			WDT0				
<b>DCGC0, type R/W, offset 0x120, reset 0x00000040</b>																
			WDT1												ADC0	
									HIB			WDT0				
<b>RCGC1, type R/W, offset 0x104, reset 0x00000000</b>																
	EPI0					COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0	
	I2C1		I2C0							SSI1	SSI0		UART2	UART1	UART0	
<b>SCGC1, type R/W, offset 0x114, reset 0x00000000</b>																
	EPI0					COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0	
	I2C1		I2C0							SSI1	SSI0		UART2	UART1	UART0	
<b>DCGC1, type R/W, offset 0x124, reset 0x00000000</b>																
	EPI0					COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0	
	I2C1		I2C0							SSI1	SSI0		UART2	UART1	UART0	
<b>RCGC2, type R/W, offset 0x108, reset 0x00000000</b>																
		UDMA						GPI0J	GPI0H	GPI0G	GPI0F	GPI0E	GPI0D	GPI0C	GPI0B	GPI0A

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>SCGC2, type R/W, offset 0x118, reset 0x00000000</b>																
			UDMA					GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
<b>DCGC2, type R/W, offset 0x128, reset 0x00000000</b>																
			UDMA					GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
<b>SRCR0, type R/W, offset 0x040, reset 0x00000000</b>																
				WDT1												ADC0
									HIB				WDT0			
<b>SRCR1, type R/W, offset 0x044, reset 0x00000000</b>																
		EPI0					COMP1	COMP0					TIMER3	TIMER2	TIMER1	TIMER0
		I2C1		I2C0							SSI1	SSI0		UART2	UART1	UART0
<b>SRCR2, type R/W, offset 0x048, reset 0x00000000</b>																
			UDMA					GPIOJ	GPIOH	GPIOG	GPIOF	GPIOE	GPIOD	GPIOC	GPIOB	GPIOA
<b>Hibernation Module</b>																
Base 0x400F.C000																
<b>HIBRTCC, type RO, offset 0x000, reset 0x0000.0000</b>																
																RTCC
																RTCC
<b>HIBRTCM0, type R/W, offset 0x004, reset 0xFFFF.FFFF</b>																
																RTCM0
																RTCM0
<b>HIBRTCM1, type R/W, offset 0x008, reset 0xFFFF.FFFF</b>																
																RTCM1
																RTCM1
<b>HIBRTCLD, type R/W, offset 0x00C, reset 0xFFFF.FFFF</b>																
																RTCLD
																RTCLD
<b>HIBCTL, type R/W, offset 0x010, reset 0x8000.0000</b>																
		WRC														
							VDD30N	VABORT	CLK32EN	LOWBATEN	PINWEN	RTCWEN	CLKSEL	HIBREQ	RTCEN	
<b>HIBIM, type R/W, offset 0x014, reset 0x0000.0000</b>																
														EXTW	LOWBAT	RTCALT1
														EXTW	LOWBAT	RTCALT0
<b>HIBRIS, type RO, offset 0x018, reset 0x0000.0000</b>																
														EXTW	LOWBAT	RTCALT1
														EXTW	LOWBAT	RTCALT0
<b>HIBMIS, type RO, offset 0x01C, reset 0x0000.0000</b>																
														EXTW	LOWBAT	RTCALT1
														EXTW	LOWBAT	RTCALT0
<b>HIBIC, type R/W1C, offset 0x020, reset 0x0000.0000</b>																
														EXTW	LOWBAT	RTCALT1
														EXTW	LOWBAT	RTCALT0
<b>HIBRTCT, type R/W, offset 0x024, reset 0x0000.7FFF</b>																
																TRIM
<b>HIBDATA, type R/W, offset 0x030-0x12C, reset -</b>																
																RTD
																RTD



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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>Internal Memory</b>															
<b>Flash Memory Registers (Flash Control Offset)</b>															
Base 0x400F.D000															
<b>FMA, type R/W, offset 0x000, reset 0x0000.0000</b>															
												OFFSET			
OFFSET															
<b>FMD, type R/W, offset 0x004, reset 0x0000.0000</b>															
DATA															
DATA															
<b>FMC, type R/W, offset 0x008, reset 0x0000.0000</b>															
WRKEY															
												COMT	MERASE	ERASE	WRITE
<b>FCRIS, type RO, offset 0x00C, reset 0x0000.0000</b>															
												PRIS		ARIS	
<b>FCIM, type R/W, offset 0x010, reset 0x0000.0000</b>															
												PMASK		AMASK	
<b>FCMISC, type R/W1C, offset 0x014, reset 0x0000.0000</b>															
												PMISC		AMISC	
<b>FMC2, type R/W, offset 0x020, reset 0x0000.0000</b>															
WRKEY															
												WRBUF			
<b>FWBVAL, type R/W, offset 0x030, reset 0x0000.0000</b>															
FWB[n]															
FWB[n]															
<b>FWBn, type R/W, offset 0x100 - 0x17C, reset 0x0000.0000</b>															
DATA															
DATA															
<b>FCTL, type R/W, offset 0x0F8, reset 0x0000.0000</b>															
												USDACK		USDREQ	
<b>Internal Memory</b>															
<b>Memory Registers (System Control Offset)</b>															
Base 0x400F.E000															
<b>RMCTL, type R/W1C, offset 0x0F0, reset -</b>															
												BA			
<b>RMVER, type RO, offset 0x0F4, reset 0x0505.0400</b>															
CONT								SIZE							
VER								REV							
<b>FMPRE0, type R/W, offset 0x130 and 0x200, reset 0xFFFF.FFFF</b>															
READ_ENABLE															
READ_ENABLE															
<b>FMPPE0, type R/W, offset 0x134 and 0x400, reset 0xFFFF.FFFF</b>															
PROG_ENABLE															
PROG_ENABLE															
<b>USER_DBG, type R/W, offset 0x1D0, reset 0xFFFF.FFFE</b>															
NW				DATA											
DATA												DBG1		DBG0	

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
<b>USER_REG0, type R/W, offset 0x1E0, reset 0xFFFF.FFFF</b>																	
NW		DATA															
DATA																	
<b>USER_REG1, type R/W, offset 0x1E4, reset 0xFFFF.FFFF</b>																	
NW		DATA															
DATA																	
<b>USER_REG2, type R/W, offset 0x1E8, reset 0xFFFF.FFFF</b>																	
NW		DATA															
DATA																	
<b>USER_REG3, type R/W, offset 0x1EC, reset 0xFFFF.FFFF</b>																	
NW		DATA															
DATA																	
<b>FMPRE1, type R/W, offset 0x204, reset 0xFFFF.FFFF</b>																	
														READ_ENABLE			
														READ_ENABLE			
<b>FMPRE2, type R/W, offset 0x208, reset 0xFFFF.FFFF</b>																	
														READ_ENABLE			
														READ_ENABLE			
<b>FMPRE3, type R/W, offset 0x20C, reset 0xFFFF.FFFF</b>																	
														READ_ENABLE			
														READ_ENABLE			
<b>FMPPE1, type R/W, offset 0x404, reset 0xFFFF.FFFF</b>																	
														PROG_ENABLE			
														PROG_ENABLE			
<b>FMPPE2, type R/W, offset 0x408, reset 0xFFFF.FFFF</b>																	
														PROG_ENABLE			
														PROG_ENABLE			
<b>FMPPE3, type R/W, offset 0x40C, reset 0xFFFF.FFFF</b>																	
														PROG_ENABLE			
														PROG_ENABLE			
<b>Micro Direct Memory Access (μDMA)</b>																	
<b>μDMA Channel Control Structure (Offset from Channel Control Table Base)</b>																	
Base n/a																	
<b>DMASRCNDP, type R/W, offset 0x000, reset -</b>																	
														ADDR			
														ADDR			
<b>DMADSTNDP, type R/W, offset 0x004, reset -</b>																	
														ADDR			
														ADDR			
<b>DMACHCTL, type R/W, offset 0x008, reset -</b>																	
DSTINC		DSTSIZE		SRCINC		SRCSIZE								ARBSIZE			
ARBSIZE						XFERSIZE				NXTUSEBURST		XFERMODE					
<b>Micro Direct Memory Access (μDMA)</b>																	
<b>μDMA Registers (Offset from μDMA Base Address)</b>																	
Base 0x400F.F000																	
<b>DMASTAT, type RO, offset 0x000, reset 0x001F.0000</b>																	
														DMACHANS			
														STATE		MASTEN	
<b>DMACFG, type WO, offset 0x004, reset -</b>																	
																MASTEN	

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>DMACTLBASE, type R/W, offset 0x008, reset 0x0000.0000</b>															
								ADDR							
ADDR															
<b>DMAALTBASE, type RO, offset 0x00C, reset 0x0000.0200</b>															
								ADDR							
								ADDR							
<b>DMAWAITSTAT, type RO, offset 0x010, reset 0x0000.0000</b>															
								WAITREQ[n]							
								WAITREQ[n]							
<b>DMAWREQ, type WO, offset 0x014, reset -</b>															
								SWREQ[n]							
								SWREQ[n]							
<b>DMAUSEBURSTSET, type R/W, offset 0x018, reset 0x0000.0000</b>															
								SET[n]							
								SET[n]							
<b>DMAUSEBURSTCLR, type WO, offset 0x01C, reset -</b>															
								CLR[n]							
								CLR[n]							
<b>DMAREQMASKSET, type R/W, offset 0x020, reset 0x0000.0000</b>															
								SET[n]							
								SET[n]							
<b>DMAREQMASKCLR, type WO, offset 0x024, reset -</b>															
								CLR[n]							
								CLR[n]							
<b>DMAENASET, type R/W, offset 0x028, reset 0x0000.0000</b>															
								SET[n]							
								SET[n]							
<b>DMAENACL, type WO, offset 0x02C, reset -</b>															
								CLR[n]							
								CLR[n]							
<b>DMAALTSET, type R/W, offset 0x030, reset 0x0000.0000</b>															
								SET[n]							
								SET[n]							
<b>DMAALTCLR, type WO, offset 0x034, reset -</b>															
								CLR[n]							
								CLR[n]							
<b>DMAPRIOSET, type R/W, offset 0x038, reset 0x0000.0000</b>															
								SET[n]							
								SET[n]							
<b>DMAPRIOCLR, type WO, offset 0x03C, reset -</b>															
								CLR[n]							
								CLR[n]							
<b>DMAERRCLR, type R/W, offset 0x04C, reset 0x0000.0000</b>															
															ERRCLR
<b>DMACHALT, type R/W, offset 0x500, reset 0x0000.0000</b>															
								CHALT[n]							
								CHALT[n]							
<b>DMAPeriphID0, type RO, offset 0xFE0, reset 0x0000.0030</b>															
												PID0			

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>DMAPeriphID1, type RO, offset 0xFE4, reset 0x0000.00B2</b>															
												PID1			
<b>DMAPeriphID2, type RO, offset 0xFE8, reset 0x0000.000B</b>															
												PID2			
<b>DMAPeriphID3, type RO, offset 0xFEC, reset 0x0000.0000</b>															
												PID3			
<b>DMAPeriphID4, type RO, offset 0xFD0, reset 0x0000.0004</b>															
												PID4			
<b>DMAPEllID0, type RO, offset 0xFF0, reset 0x0000.000D</b>															
												CID0			
<b>DMAPEllID1, type RO, offset 0xFF4, reset 0x0000.00F0</b>															
												CID1			
<b>DMAPEllID2, type RO, offset 0xFF8, reset 0x0000.0005</b>															
												CID2			
<b>DMAPEllID3, type RO, offset 0xFFC, reset 0x0000.00B1</b>															
												CID3			
<b>General-Purpose Input/Outputs (GPIOs)</b>															
GPIO Port A (APB) base: 0x4000.4000															
GPIO Port A (AHB) base: 0x4005.8000															
GPIO Port B (APB) base: 0x4000.5000															
GPIO Port B (AHB) base: 0x4005.9000															
GPIO Port C (APB) base: 0x4000.6000															
GPIO Port C (AHB) base: 0x4005.A000															
GPIO Port D (APB) base: 0x4000.7000															
GPIO Port D (AHB) base: 0x4005.B000															
GPIO Port E (APB) base: 0x4002.4000															
GPIO Port E (AHB) base: 0x4005.C000															
GPIO Port F (APB) base: 0x4002.5000															
GPIO Port F (AHB) base: 0x4005.D000															
GPIO Port G (APB) base: 0x4002.6000															
GPIO Port G (AHB) base: 0x4005.E000															
GPIO Port H (APB) base: 0x4002.7000															
GPIO Port H (AHB) base: 0x4005.F000															
GPIO Port J (APB) base: 0x4003.D000															
GPIO Port J (AHB) base: 0x4006.0000															
<b>GPIODATA, type R/W, offset 0x000, reset 0x0000.0000</b>															
												DATA			
<b>GPIODIR, type R/W, offset 0x400, reset 0x0000.0000</b>															
												DIR			
<b>GPIOIS, type R/W, offset 0x404, reset 0x0000.0000</b>															
												IS			
<b>GPIOIBE, type R/W, offset 0x408, reset 0x0000.0000</b>															
												IBE			
<b>GPIOIEV, type R/W, offset 0x40C, reset 0x0000.0000</b>															
												IEV			

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIOIM, type R/W, offset 0x410, reset 0x0000.0000															
												IME			
GPIORIS, type RO, offset 0x414, reset 0x0000.0000															
												RIS			
GPIOMIS, type RO, offset 0x418, reset 0x0000.0000															
												MIS			
GPIOICR, type W1C, offset 0x41C, reset 0x0000.0000															
												IC			
GPIOAFSEL, type R/W, offset 0x420, reset -															
												AFSEL			
GPIODR2R, type R/W, offset 0x500, reset 0x0000.00FF															
												DRV2			
GPIODR4R, type R/W, offset 0x504, reset 0x0000.0000															
												DRV4			
GPIODR8R, type R/W, offset 0x508, reset 0x0000.0000															
												DRV8			
GPIOODR, type R/W, offset 0x50C, reset 0x0000.0000															
												ODE			
GPIOPUR, type R/W, offset 0x510, reset -															
												PUE			
GPIOPDR, type R/W, offset 0x514, reset 0x0000.0000															
												PDE			
GPIOSLR, type R/W, offset 0x518, reset 0x0000.0000															
												SRL			
GPIODEN, type R/W, offset 0x51C, reset -															
												DEN			
GPIOLOCK, type R/W, offset 0x520, reset 0x0000.0001															
												LOCK			
												LOCK			
GPIOCR, type -, offset 0x524, reset -															
												CR			
GPIOAMSEL, type R/W, offset 0x528, reset 0x0000.0000															
												GPIOAMSEL			
GPIOPTL, type R/W, offset 0x52C, reset -															
PMC7				PMC6				PMC5				PMC4			
PMC3				PMC2				PMC1				PMC0			

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
<b>GPIOPeriphID4, type RO, offset 0xFD0, reset 0x0000.0000</b>																			
												PID4							
<b>GPIOPeriphID5, type RO, offset 0xFD4, reset 0x0000.0000</b>																			
												PID5							
<b>GPIOPeriphID6, type RO, offset 0xFD8, reset 0x0000.0000</b>																			
												PID6							
<b>GPIOPeriphID7, type RO, offset 0xFDC, reset 0x0000.0000</b>																			
												PID7							
<b>GPIOPeriphID0, type RO, offset 0xFE0, reset 0x0000.0061</b>																			
												PID0							
<b>GPIOPeriphID1, type RO, offset 0xFE4, reset 0x0000.0000</b>																			
												PID1							
<b>GPIOPeriphID2, type RO, offset 0xFE8, reset 0x0000.0018</b>																			
												PID2							
<b>GPIOPeriphID3, type RO, offset 0xFEC, reset 0x0000.0001</b>																			
												PID3							
<b>GPIOPCellID0, type RO, offset 0xFF0, reset 0x0000.000D</b>																			
												CID0							
<b>GPIOPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0</b>																			
												CID1							
<b>GPIOPCellID2, type RO, offset 0xFF8, reset 0x0000.0005</b>																			
												CID2							
<b>GPIOPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1</b>																			
												CID3							
<b>External Peripheral Interface (EPI)</b> Base 0x400D.0000																			
<b>EPICFG, type R/W, offset 0x000, reset 0x0000.0000</b>																			
												BLKEN		MODE					
<b>EPIBAUD, type R/W, offset 0x004, reset 0x0000.0000</b>																			
												COUNT1							
												COUNT0							
<b>EPISDRAMCFG, type R/W, offset 0x010, reset 0x42EE.0000</b>																			
FREQ						RFSH													
												SLEEP		SIZE					
<b>EPIHB8CFG, type R/W, offset 0x010, reset 0x0000.FF00</b>																			
MAXWAIT												XFFEN		XFEEN		WRHIGH		RDHIGH	
												WRWS		RDWS		MODE			
<b>EPIHB16CFG, type R/W, offset 0x010, reset 0x0000.FF00</b>																			
MAXWAIT												XFFEN		XFEEN		WRHIGH		RDHIGH	
												WRWS		RDWS		BSEL		MODE	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>EPIGPCFG, type R/W, offset 0x010, reset 0x0000.FF00</b>															
CLKPIN	CLKGATE		RDYEN	FRMPIN	FRM50		FRMCNT			RW		WR2CYC	RD2CYC		
MAXWAIT										ASIZE		DSIZE			
<b>EPIHB8CFG2, type R/W, offset 0x014, reset 0x0000.0000</b>															
WORD					CSBAUD		CSCFG								
<b>EPIHB16CFG2, type R/W, offset 0x014, reset 0x0000.0000</b>															
WORD					CSBAUD		CSCFG								
<b>EPIGPCFG2, type R/W, offset 0x014, reset 0x0000.0000</b>															
WORD															
<b>EPIADDRMAP, type R/W, offset 0x01C, reset 0x0000.0000</b>															
								EPSZ		EPADR		ERSZ		ERADR	
<b>EPIRSIZE0, type R/W, offset 0x020, reset 0x0000.0003</b>															
															SIZE
<b>EPIRSIZE1, type R/W, offset 0x030, reset 0x0000.0003</b>															
															SIZE
<b>EPIRADDR0, type R/W, offset 0x024, reset 0x0000.0000</b>															
															ADDR
															ADDR
<b>EPIRADDR1, type R/W, offset 0x034, reset 0x0000.0000</b>															
															ADDR
															ADDR
<b>EPIRPSTD0, type R/W, offset 0x028, reset 0x0000.0000</b>															
															POSTCNT
<b>EPIRPSTD1, type R/W, offset 0x038, reset 0x0000.0000</b>															
															POSTCNT
<b>EPISTAT, type RO, offset 0x060, reset 0x0000.0000</b>															
								CELOW	XFFULL	XFEMPTY	INITSEQ	WBUSY	NBRBUSY		ACTIVE
<b>EPIRFIFOCNT, type RO, offset 0x06C, reset -</b>															
															COUNT
<b>EPIREADFIFO, type RO, offset 0x070, reset -</b>															
															DATA
															DATA
<b>EPIREADFIFO1, type RO, offset 0x074, reset -</b>															
															DATA
															DATA
<b>EPIREADFIFO2, type RO, offset 0x078, reset -</b>															
															DATA
															DATA
<b>EPIREADFIFO3, type RO, offset 0x07C, reset -</b>															
															DATA
															DATA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16						
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
<b>EPIREADFIFO4, type RO, offset 0x080, reset -</b>																					
DATA																					
DATA																					
<b>EPIREADFIFO5, type RO, offset 0x084, reset -</b>																					
DATA																					
DATA																					
<b>EPIREADFIFO6, type RO, offset 0x088, reset -</b>																					
DATA																					
DATA																					
<b>EPIREADFIFO7, type RO, offset 0x08C, reset -</b>																					
DATA																					
DATA																					
<b>EPIFIFOLVL, type R/W, offset 0x200, reset 0x0000.0033</b>																					
												WFERR	RSERR								
WRFIFO												RDFIFO									
<b>EPIWFIFOCNT, type RO, offset 0x204, reset 0x0000.0000</b>																					
WTAV																					
<b>EPIIM, type R/W, offset 0x210, reset 0x0000.0000</b>																					
WRIM																RDIM	ERRIM				
<b>EPIRIS, type RO, offset 0x214, reset 0x0000.0000</b>																					
WRRIS																RDRIS	ERRRIS				
<b>EPIMIS, type RO, offset 0x218, reset 0x0000.0000</b>																					
WRMIS																RDMIS	ERRMIS				
<b>EPIEISC, type R/W1C, offset 0x21C, reset 0x0000.0000</b>																					
WTFULL																RSTALL	TOUT				
<b>General-Purpose Timers</b>																					
Timer0 base: 0x4003.0000																					
Timer1 base: 0x4003.1000																					
Timer2 base: 0x4003.2000																					
Timer3 base: 0x4003.3000																					
<b>GPTMCFG, type R/W, offset 0x000, reset 0x0000.0000</b>																					
GPTMCFG																					
<b>GPTMTAMR, type R/W, offset 0x004, reset 0x0000.0000</b>																					
												TASNAPS	TAWOT	TAMIE	TACDIR	TAAMS	TACMR	TAMR			
<b>GPTMTBMR, type R/W, offset 0x008, reset 0x0000.0000</b>																					
												TBSNAPS	TBWOT	TBMIE	TBCDIR	TBAMS	TBCMR	TBMR			
<b>GPTMCTL, type R/W, offset 0x00C, reset 0x0000.0000</b>																					
TBPWML		TBOTE		TBEVENT		TBSTALL		TBEN		TAPWML		TAOTE		RTCEN		TAEVENT		TASTALL		TAEN	
<b>GPTMIMR, type R/W, offset 0x018, reset 0x0000.0000</b>																					
				TBMIM	CBEIM	CBMIM	TBTOIM					TAMIM	RTCIM	CAEIM	CAMIM	TATOIM					
<b>GPTMRIS, type RO, offset 0x01C, reset 0x0000.0000</b>																					
				TBMRIS	CBERIS	CBMRIS	TBTORIS					TAMRIS	RTCRIIS	CAERIS	CAMRIS	TATORIS					



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>GPTMMIS, type RO, offset 0x020, reset 0x0000.0000</b>																
				TBMMIS	CBEMIS	CBMMIS	TBTOMIS					TAMMIS	RTCMIS	CAEMIS	CAMMIS	TATOMIS
<b>GPTMICR, type W1C, offset 0x024, reset 0x0000.0000</b>																
				TBMCINT	CBECINT	CBMCINT	TBTCINT					TAMCINT	RTCCINT	CAECINT	CAMCINT	TATOCINT
<b>GPTMTAILR, type R/W, offset 0x028, reset 0xFFFF.FFFF</b>																
								TAILRH								
								TAILRL								
<b>GPTMTBILR, type R/W, offset 0x02C, reset 0x0000.FFFF</b>																
								TBILRL								
<b>GPTMTAMATCHR, type R/W, offset 0x030, reset 0xFFFF.FFFF</b>																
								TAMRH								
								TAMRL								
<b>GPTMTBMATCHR, type R/W, offset 0x034, reset 0x0000.FFFF</b>																
								TBMRL								
<b>GPTMTAPR, type R/W, offset 0x038, reset 0x0000.0000</b>																
								TAPSR								
<b>GPTMTBPR, type R/W, offset 0x03C, reset 0x0000.0000</b>																
								TBPSR								
<b>GPTMTAR, type RO, offset 0x048, reset 0xFFFF.FFFF</b>																
								TARH								
								TARL								
<b>GPTMTBR, type RO, offset 0x04C, reset 0x0000.FFFF</b>																
								TBRL								
<b>GPTMTAV, type RO, offset 0x050, reset 0xFFFF.FFFF</b>																
								TAVH								
								TAVL								
<b>GPTMTBV, type RO, offset 0x054, reset 0x0000.FFFF</b>																
								TBVL								
<b>Watchdog Timers</b>																
WDT0 base: 0x4000.0000																
WDT1 base: 0x4000.1000																
<b>WDTLOAD, type R/W, offset 0x000, reset 0xFFFF.FFFF</b>																
								WDTLOAD								
								WDTLOAD								
<b>WDTVALUE, type RO, offset 0x004, reset 0xFFFF.FFFF</b>																
								WDTVALUE								
								WDTVALUE								
<b>WDTCTL, type R/W, offset 0x008, reset 0x0000.0000 (WDT0) and 0x8000.0000 (WDT1)</b>																
WRC																
														RESEN	INTEN	
<b>WDTICR, type WO, offset 0x00C, reset -</b>																
								WDTINTCLR								
								WDTINTCLR								

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>WDTRIS, type RO, offset 0x010, reset 0x0000.0000</b>															
															WDTRIS
<b>WDTMIS, type RO, offset 0x014, reset 0x0000.0000</b>															
															WDTMIS
<b>WDTTST, type R/W, offset 0x418, reset 0x0000.0000</b>															
															STALL
<b>WDTLOCK, type R/W, offset 0xC00, reset 0x0000.0000</b>															
WDTLOCK															
WDTLOCK															
<b>WDTPeriphID4, type RO, offset 0xFD0, reset 0x0000.0000</b>															
															PID4
<b>WDTPeriphID5, type RO, offset 0xFD4, reset 0x0000.0000</b>															
															PID5
<b>WDTPeriphID6, type RO, offset 0xFD8, reset 0x0000.0000</b>															
															PID6
<b>WDTPeriphID7, type RO, offset 0xFDC, reset 0x0000.0000</b>															
															PID7
<b>WDTPeriphID0, type RO, offset 0xFE0, reset 0x0000.0005</b>															
															PID0
<b>WDTPeriphID1, type RO, offset 0xFE4, reset 0x0000.0018</b>															
															PID1
<b>WDTPeriphID2, type RO, offset 0xFE8, reset 0x0000.0018</b>															
															PID2
<b>WDTPeriphID3, type RO, offset 0xFEC, reset 0x0000.0001</b>															
															PID3
<b>WDTPCellID0, type RO, offset 0xFF0, reset 0x0000.000D</b>															
															CID0
<b>WDTPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0</b>															
															CID1
<b>WDTPCellID2, type RO, offset 0xFF8, reset 0x0000.0006</b>															
															CID2
<b>WDTPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1</b>															
															CID3
<b>Analog-to-Digital Converter (ADC)</b>															
Base 0x4003.8000															
<b>ADCACTSS, type R/W, offset 0x000, reset 0x0000.0000</b>															
												ASEN3	ASEN2	ASEN1	ASEN0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																
<b>ADCRIS, type RO, offset 0x004, reset 0x0000.0000</b>																															
												INR3		INR2		INR1		INR0													
<b>ADCIM, type R/W, offset 0x008, reset 0x0000.0000</b>																															
												DCONSS3		DCONSS2		DCONSS1		DCONSS0													
												MASK3		MASK2		MASK1		MASK0													
<b>ADCISC, type R/W1C, offset 0x00C, reset 0x0000.0000</b>																															
												DCINSS3		DCINSS2		DCINSS1		DCINSS0													
												IN3		IN2		IN1		IN0													
<b>ADCOSTAT, type R/W1C, offset 0x010, reset 0x0000.0000</b>																															
												OV3		OV2		OV1		OV0													
<b>ADCEMUX, type R/W, offset 0x014, reset 0x0000.0000</b>																															
EM3				EM2				EM1				EM0																			
<b>ADCUSTAT, type R/W1C, offset 0x018, reset 0x0000.0000</b>																															
												UV3		UV2		UV1		UV0													
<b>ADCSSPRI, type R/W, offset 0x020, reset 0x0000.3210</b>																															
SS3				SS2				SS1				SS0																			
<b>ADCPSSI, type WO, offset 0x028, reset -</b>																															
												SS3		SS2		SS1		SS0													
<b>ADCSAC, type R/W, offset 0x030, reset 0x0000.0000</b>																															
												AVG																			
<b>ADCDCISC, type R/W1C, offset 0x034, reset 0x0000.0000</b>																															
								DCINT7		DCINT6		DCINT5		DCINT4		DCINT3		DCINT2		DCINT1		DCINT0									
<b>ADCSSMUX0, type R/W, offset 0x040, reset 0x0000.0000</b>																															
MUX7				MUX6				MUX5				MUX4																			
MUX3				MUX2				MUX1				MUX0																			
<b>ADCSSCTL0, type R/W, offset 0x044, reset 0x0000.0000</b>																															
TS7		IE7		END7		D7		TS6		IE6		END6		D6		TS5		IE5		END5		D5		TS4		IE4		END4		D4	
TS3		IE3		END3		D3		TS2		IE2		END2		D2		TS1		IE1		END1		D1		TS0		IE0		END0		D0	
<b>ADCSSFIFO0, type RO, offset 0x048, reset 0x0000.0000</b>																															
												DATA																			
<b>ADCSSFIFO1, type RO, offset 0x068, reset 0x0000.0000</b>																															
												DATA																			
<b>ADCSSFIFO2, type RO, offset 0x088, reset 0x0000.0000</b>																															
												DATA																			
<b>ADCSSFIFO3, type RO, offset 0x0A8, reset 0x0000.0000</b>																															
												DATA																			
<b>ADCSSFSTAT0, type RO, offset 0x04C, reset 0x0000.0100</b>																															
FULL				EMPTY				HPTR				TPTR																			

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>ADCSSFSTAT1, type RO, offset 0x06C, reset 0x0000.0100</b>															
FULL				EMPTY				HPTR				TPTR			
<b>ADCSSFSTAT2, type RO, offset 0x08C, reset 0x0000.0100</b>															
FULL				EMPTY				HPTR				TPTR			
<b>ADCSSFSTAT3, type RO, offset 0x0AC, reset 0x0000.0100</b>															
FULL				EMPTY				HPTR				TPTR			
<b>ADCSSOP0, type R/W, offset 0x050, reset 0x0000.0000</b>															
S7DCOP				S6DCOP				S5DCOP				S4DCOP			
S3DCOP				S2DCOP				S1DCOP				S0DCOP			
<b>ADCSSDC0, type R/W, offset 0x054, reset 0x0000.0000</b>															
S7DCSEL				S6DCSEL				S5DCSEL				S4DCSEL			
S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
<b>ADCSSMUX1, type R/W, offset 0x060, reset 0x0000.0000</b>															
MUX3				MUX2				MUX1				MUX0			
<b>ADCSSMUX2, type R/W, offset 0x080, reset 0x0000.0000</b>															
MUX3				MUX2				MUX1				MUX0			
<b>ADCSSCTL1, type R/W, offset 0x064, reset 0x0000.0000</b>															
TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
<b>ADCSSCTL2, type R/W, offset 0x084, reset 0x0000.0000</b>															
TS3	IE3	END3	D3	TS2	IE2	END2	D2	TS1	IE1	END1	D1	TS0	IE0	END0	D0
<b>ADCSSOP1, type R/W, offset 0x070, reset 0x0000.0000</b>															
S3DCOP				S2DCOP				S1DCOP				S0DCOP			
<b>ADCSSOP2, type R/W, offset 0x090, reset 0x0000.0000</b>															
S3DCOP				S2DCOP				S1DCOP				S0DCOP			
<b>ADCSSDC1, type R/W, offset 0x074, reset 0x0000.0000</b>															
S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
<b>ADCSSDC2, type R/W, offset 0x094, reset 0x0000.0000</b>															
S3DCSEL				S2DCSEL				S1DCSEL				S0DCSEL			
<b>ADCSSMUX3, type R/W, offset 0x0A0, reset 0x0000.0000</b>															
												MUX0			
<b>ADCSSCTL3, type R/W, offset 0x0A4, reset 0x0000.0002</b>															
												TS0	IE0	END0	D0
<b>ADCSSOP3, type R/W, offset 0x0B0, reset 0x0000.0000</b>															
												S0DCOP			
<b>ADCSSDC3, type R/W, offset 0x0B4, reset 0x0000.0000</b>															
												S0DCSEL			

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>ADDCR1C, type R/W, offset 0xD00, reset 0x0000.0000</b>															
								DCTRIG7	DCTRIG6	DCTRIG5	DCTRIG4	DCTRIG3	DCTRIG2	DCTRIG1	DCTRIG0
								DCINT7	DCINT6	DCINT5	DCINT4	DCINT3	DCINT2	DCINT1	DCINT0
<b>ADDCCTL0, type R/W, offset 0xE00, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCTL1, type R/W, offset 0xE04, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCTL2, type R/W, offset 0xE08, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCTL3, type R/W, offset 0xE0C, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCTL4, type R/W, offset 0xE10, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCTL5, type R/W, offset 0xE14, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCTL6, type R/W, offset 0xE18, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCTL7, type R/W, offset 0xE1C, reset 0x0000.0000</b>															
				CTE	CTC	CTM						CIE	CIC	CIM	
<b>ADDCCMP0, type R/W, offset 0xE40, reset 0x0000.0000</b>															
												COMP1			
												COMP0			
<b>ADDCCMP1, type R/W, offset 0xE44, reset 0x0000.0000</b>															
												COMP1			
												COMP0			
<b>ADDCCMP2, type R/W, offset 0xE48, reset 0x0000.0000</b>															
												COMP1			
												COMP0			
<b>ADDCCMP3, type R/W, offset 0xE4C, reset 0x0000.0000</b>															
												COMP1			
												COMP0			
<b>ADDCCMP4, type R/W, offset 0xE50, reset 0x0000.0000</b>															
												COMP1			
												COMP0			
<b>ADDCCMP5, type R/W, offset 0xE54, reset 0x0000.0000</b>															
												COMP1			
												COMP0			
<b>ADDCCMP6, type R/W, offset 0xE58, reset 0x0000.0000</b>															
												COMP1			
												COMP0			
<b>ADDCCMP7, type R/W, offset 0xE5C, reset 0x0000.0000</b>															
												COMP1			
												COMP0			

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>Universal Asynchronous Receivers/Transmitters (UARTs)</b>																
UART0 base: 0x4000.C000 UART1 base: 0x4000.D000 UART2 base: 0x4000.E000																
<b>UARTDR, type R/W, offset 0x000, reset 0x0000.0000</b>																
				OE	BE	PE	FE	DATA								
<b>UARTRSR/UARTECR, type RO, offset 0x004, reset 0x0000.0000 (Read-Only Status Register)</b>																
												OE	BE	PE	FE	
<b>UARTRSR/UARTECR, type WO, offset 0x004, reset 0x0000.0000 (Write-Only Error Clear Register)</b>																
												DATA				
<b>UARTFR, type RO, offset 0x018, reset 0x0000.0090</b>																
								RI	TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS
<b>UARTILPR, type R/W, offset 0x020, reset 0x0000.0000</b>																
												ILPDVSR				
<b>UARTIBRD, type R/W, offset 0x024, reset 0x0000.0000</b>																
												DIVINT				
<b>UARTFBRD, type R/W, offset 0x028, reset 0x0000.0000</b>																
												DIVFRAC				
<b>UARTLCRH, type R/W, offset 0x02C, reset 0x0000.0000</b>																
								SPS	WLEN	FEN	STP2	EPS	PEN	BRK		
<b>UARTCTL, type R/W, offset 0x030, reset 0x0000.0300</b>																
CTSEN	RTSEN			RTS	DTR	RXE	TXE	LBE	LIN	HSE	EOT	SMART	SIRLP	SIREN	UARTEN	
<b>UARTIFLS, type R/W, offset 0x034, reset 0x0000.0012</b>																
												RXIFLSEL		TXIFLSEL		
<b>UARTIM, type R/W, offset 0x038, reset 0x0000.0000</b>																
LME5IM	LME1IM	LMSBIM		OEIM	BEIM	PEIM	FEIM	RTIM	TXIM	RXIM	DSRIM	DCDIM	CTSIM	RIIM		
<b>UARTRIS, type RO, offset 0x03C, reset 0x0000.000F</b>																
LME5RIS	LME1RIS	LMSBRIS		OERIS	BERIS	PERIS	FERIS	RTRIS	TXRIS	RXRIS	DSRRIS	DCDRIS	CTSRIS	RIRIS		
<b>UARTMIS, type RO, offset 0x040, reset 0x0000.0000</b>																
LME5MIS	LME1MIS	LMSBMIS		OEMIS	BEMIS	PEMIS	FEMIS	RTMIS	TXMIS	RXMIS	DSRMIS	DCDMIS	CTSMIS	RIMIS		
<b>UARTICR, type W1C, offset 0x044, reset 0x0000.0000</b>																
LME5MIC	LME1MIC	LMSBMIC		OEIC	BEIC	PEIC	FEIC	RTIC	TXIC	RXIC	DSRMIC	DCDMIC	CTSMIC	RIMIC		
<b>UARTDMACTL, type R/W, offset 0x048, reset 0x0000.0000</b>																
												DMAERR	TXDMAE	RXDMAE		
<b>UARTLCTL, type R/W, offset 0x090, reset 0x0000.0000</b>																
												BLEN	MASTER			



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<b>SSIDR, type R/W, offset 0x008, reset 0x0000.0000</b>																
DATA																
<b>SSISR, type RO, offset 0x00C, reset 0x0000.0003</b>																
												BSY	RFF	RNE	TNF	TFE
<b>SSICPSR, type R/W, offset 0x010, reset 0x0000.0000</b>																
CPSDVSR																
<b>SSIIM, type R/W, offset 0x014, reset 0x0000.0000</b>																
												TXIM	RXIM	RTIM	RORIM	
<b>SSIRIS, type RO, offset 0x018, reset 0x0000.0008</b>																
												TXRIS	RXRIS	RTRIS	RORRIS	
<b>SSIMIS, type RO, offset 0x01C, reset 0x0000.0000</b>																
												TXMIS	RXMIS	RTMIS	RORMIS	
<b>SSIICR, type W1C, offset 0x020, reset 0x0000.0000</b>																
														RTIC	RORIC	
<b>SSIDMACTL, type R/W, offset 0x024, reset 0x0000.0000</b>																
														TXDMAE	RXDMAE	
<b>SSIPeriphID4, type RO, offset 0xFD0, reset 0x0000.0000</b>																
PID4																
<b>SSIPeriphID5, type RO, offset 0xFD4, reset 0x0000.0000</b>																
PID5																
<b>SSIPeriphID6, type RO, offset 0xFD8, reset 0x0000.0000</b>																
PID6																
<b>SSIPeriphID7, type RO, offset 0xFDC, reset 0x0000.0000</b>																
PID7																
<b>SSIPeriphID0, type RO, offset 0xFE0, reset 0x0000.0022</b>																
PID0																
<b>SSIPeriphID1, type RO, offset 0xFE4, reset 0x0000.0000</b>																
PID1																
<b>SSIPeriphID2, type RO, offset 0xFE8, reset 0x0000.0018</b>																
PID2																
<b>SSIPeriphID3, type RO, offset 0xFEC, reset 0x0000.0001</b>																
PID3																
<b>SSIPCellID0, type RO, offset 0xFF0, reset 0x0000.000D</b>																
CID0																

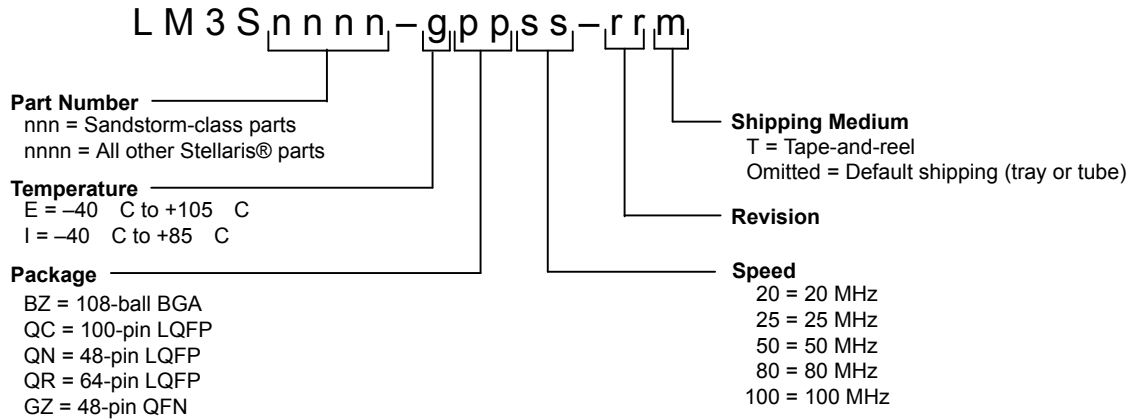


31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>SSIPCellID1, type RO, offset 0xFF4, reset 0x0000.00F0</b>															
												CID1			
<b>SSIPCellID2, type RO, offset 0xFF8, reset 0x0000.0005</b>															
												CID2			
<b>SSIPCellID3, type RO, offset 0xFFC, reset 0x0000.00B1</b>															
												CID3			
<b>Inter-Integrated Circuit (I<sup>2</sup>C) Interface</b>															
<b>I<sup>2</sup>C Master</b>															
I2C Master 0 base: 0x4002.0000															
I2C Master 1 base: 0x4002.1000															
<b>I2CMSA, type R/W, offset 0x000, reset 0x0000.0000</b>															
												SA		R/S	
<b>I2CMCS, type RO, offset 0x004, reset 0x0000.0000 (Read-Only Status Register)</b>															
								BUSBSY	IDLE	ARBLST	DATAACK	ADRACK	ERROR	BUSY	
<b>I2CMCS, type WO, offset 0x004, reset 0x0000.0000 (Write-Only Control Register)</b>															
												ACK	STOP	START	RUN
<b>I2CMDR, type R/W, offset 0x008, reset 0x0000.0000</b>															
												DATA			
<b>I2CMTPR, type R/W, offset 0x00C, reset 0x0000.0001</b>															
												TPR			
<b>I2CMIMR, type R/W, offset 0x010, reset 0x0000.0000</b>															
												IM			
<b>I2CMRIS, type RO, offset 0x014, reset 0x0000.0000</b>															
												RIS			
<b>I2CMMIS, type RO, offset 0x018, reset 0x0000.0000</b>															
												MIS			
<b>I2CMICR, type WO, offset 0x01C, reset 0x0000.0000</b>															
												IC			
<b>I2CMCR, type R/W, offset 0x020, reset 0x0000.0000</b>															
								SFE	MFE			LPBK			
<b>Inter-Integrated Circuit (I<sup>2</sup>C) Interface</b>															
<b>I<sup>2</sup>C Slave</b>															
I2C Slave 0 base: 0x4002.0800															
I2C Slave 1 base: 0x4002.1800															
<b>I2CSOAR, type R/W, offset 0x000, reset 0x0000.0000</b>															
												OAR			
<b>I2CCSR, type RO, offset 0x004, reset 0x0000.0000 (Read-Only Status Register)</b>															
												FBR	TREQ	RREQ	

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>I2CCSR, type WO, offset 0x004, reset 0x0000.0000 (Write-Only Control Register)</b>															
															DA
<b>I2CSDR, type R/W, offset 0x008, reset 0x0000.0000</b>															
															DATA
<b>I2CSIMR, type R/W, offset 0x00C, reset 0x0000.0000</b>															
													STOPIM	STARTIM	DATAIM
<b>I2CSRIS, type RO, offset 0x010, reset 0x0000.0000</b>															
													STOPRIS	STARTRIS	DATARIS
<b>I2CSMIS, type RO, offset 0x014, reset 0x0000.0000</b>															
													STOPMIS	STARTMIS	DATAMIS
<b>I2CSICR, type WO, offset 0x018, reset 0x0000.0000</b>															
													STOPIC	STARTIC	DATAIC
<b>Analog Comparators</b>															
Base 0x4003.C000															
<b>ACMIS, type R/W1C, offset 0x000, reset 0x0000.0000</b>															
													IN1	IN0	
<b>ACRIS, type RO, offset 0x004, reset 0x0000.0000</b>															
													IN1	IN0	
<b>ACINTEN, type R/W, offset 0x008, reset 0x0000.0000</b>															
													IN1	IN0	
<b>ACREFCTL, type R/W, offset 0x010, reset 0x0000.0000</b>															
						EN	RNG							VREF	
<b>ACSTAT0, type RO, offset 0x020, reset 0x0000.0000</b>															
													OVAL		
<b>ACSTAT1, type RO, offset 0x040, reset 0x0000.0000</b>															
													OVAL		
<b>ACCTL0, type R/W, offset 0x024, reset 0x0000.0000</b>															
				TOEN	ASRCP			TSLVAL	TSEN	ISLVAL			ISEN	CINV	
<b>ACCTL1, type R/W, offset 0x044, reset 0x0000.0000</b>															
				TOEN	ASRCP			TSLVAL	TSEN	ISLVAL			ISEN	CINV	

## D Ordering and Contact Information

### D.1 Ordering Information



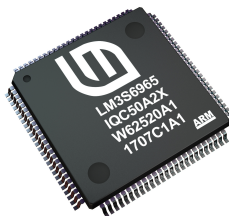
**Table D-1. Part Ordering Information**

Orderable Part Number	Description
LM3S1811-IQC50-C0	Stellaris® LM3S1811 Microcontroller Industrial Temperature 100-pin LQFP
LM3S1811-IQC50-C0T	Stellaris® LM3S1811 Microcontroller Industrial Temperature 100-pin LQFP Tape-and-reel

### D.2 Part Markings

The Stellaris® microcontrollers are marked with an identifying number. This code contains the following information:

- The first line indicates the part number. In the example figure below, this is the LM3S6965.
- The first seven characters in the second line indicate the temperature, package, speed, and revision. In the example figure below, this is an Industrial temperature (I), 100-pin LQFP package (QC), 50-MHz (50), revision A2 (A2) device.
- The remaining characters contain internal tracking numbers.



### D.3 Kits

The Stellaris® Family provides the hardware and software tools that engineers need to begin development quickly.

- Reference Design Kits accelerate product development by providing ready-to-run hardware and comprehensive documentation including hardware design files:  
[http://www.luminarymicro.com/products/reference\\_design\\_kits/](http://www.luminarymicro.com/products/reference_design_kits/)
- Evaluation Kits provide a low-cost and effective means of evaluating Stellaris<sup>®</sup> microcontrollers before purchase:  
<http://www.luminarymicro.com/products/kits.html>
- Development Kits provide you with all the tools you need to develop and prototype embedded applications right out of the box:  
[http://www.luminarymicro.com/products/development\\_kits.html](http://www.luminarymicro.com/products/development_kits.html)

See the website for the latest tools available, or ask your distributor.

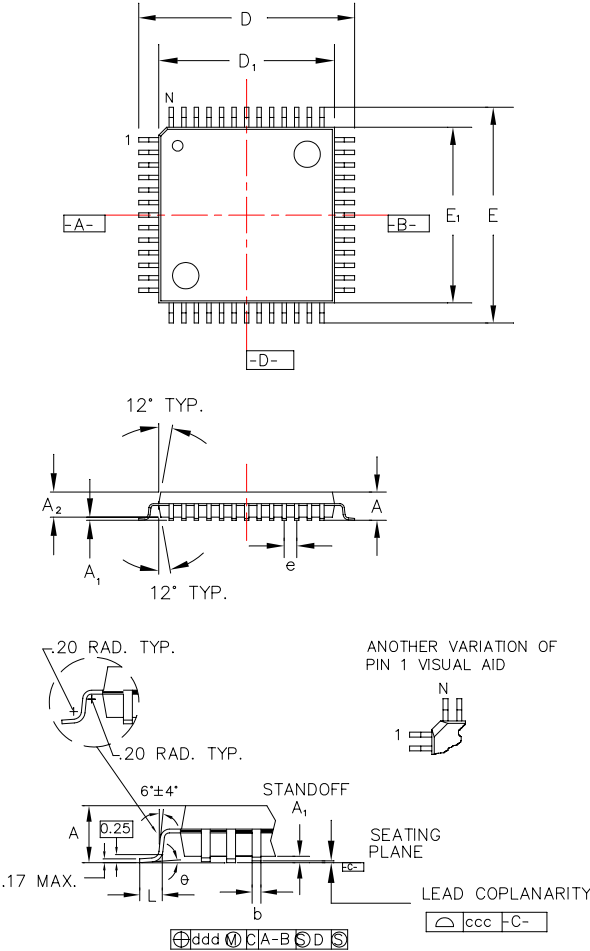
## **D.4 Support Information**

For support on Stellaris<sup>®</sup> products, contact:

[support\\_lmi@ti.com](mailto:support_lmi@ti.com)

# E Package Information

Figure E-1. 100-Pin LQFP Package



**Note:** The following notes apply to the package drawing.

1. All dimensions shown in mm.
2. Dimensions shown are nominal with tolerances indicated.
3. Foot length 'L' is measured at gage plane 0.25 mm above seating plane.

Body +2.00 mm Footprint, 1.4 mm package thickness		
Symbols	Leads	100L
A	Max.	1.60
A <sub>1</sub>	-	0.05 Min./0.15 Max.
A <sub>2</sub>	±0.05	1.40
D	±0.20	16.00
D <sub>1</sub>	±0.05	14.00
E	±0.20	16.00
E <sub>1</sub>	±0.05	14.00
L	+0.15/-0.10	0.60
e	Basic	0.50
b	+0.05	0.22
θ	-	0°-7°
ddd	Max.	0.08
ccc	Max.	0.08
JEDEC Reference Drawing		MS-026
Variation Designator		BED

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