FUJITSU SEMICONDUCTOR
DATA SHEET

DS706-00038-2v0-E

32-bit ARM™ Cortex™-M3 based Microcontroller

FM3 MB9AA40NA Series

MB9AFA41LA/MA/NA, MB9AFA42LA/MA/NA, MB9AFA44LA/MA/NA

■ DESCRIPTION

The MB9AA40NA Series are highly integrated 32-bit microcontrollers dedicated for embedded controllers with low-power consumption mode and competitive cost.

These series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as various timers, ADCs, LCDC and Communication Interfaces (UART, CSIO, I^2C).

The products which are described in this data sheet are placed into TYPE6 product categories in "FM3 Family PERIPHERAL MANUAL".

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ARM™

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■ FEATURES

- 32-bit ARM Cortex-M3 Core
  - Processor version: r2p1
  - Up to 40 MHz Frequency Operation
  - Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
  - 24-bit System timer (Sys Tick): System timer for OS task management

- On-chip Memories

[Flash memory]

  - Dual operation Flash memory
    - Dual Operation Flash memory has the upper bank and the lower bank. So, this series could implement erase, write and read operations for each bank simultaneously.
    - Main area: Up to 256 Kbytes (Up to 240Kbytes upper bank + 16Kbytes lower bank)
    - Work area: 32 Kbytes (lower bank)
  - Read cycle: 0 wait-cycle
  - Security function for code protection

[SRAM]

This Series on-chip SRAM is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus or D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

  - SRAM0: Up to 16 Kbytes
  - SRAM1: Up to 16 Kbytes

- External Bus Interface*
  - Supports SRAM, NOR Flash memory device
  - Up to 8 chip selects
  - 8/16-bit Data width
  - Up to 25-bit Address bit
  - Supports Address/Data multiplex
  - Supports external RDY function

  * : MB9AFA41LA, FA42LA and FA44LA do not support External Bus Interface.

- LCD Controller (LCDC)
  - Up to 40 SEG × 8COM
  - 8COM or 4COM mode can be selected.
  - Built-in internal dividing resistor
  - LCD drive power supply (bias) pin (VV4 to VV0)
  - With blinking function

- Multi-function Serial Interface (Max 8channels)
  - 4 channels with 16steps×9-bit FIFO (ch.4 to ch.7), 4 channels without FIFO (ch.0 to ch.3)
  - Operation mode is selectable from the followings for each channel.
    - UART
    - CSIO
    - I^2C

[UART]
- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control* : Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

  * : MB9AFA41LA, FA42LA and FA44LA do not support Hardware Flow control.

[CSIO]
- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[I^2C]

Standard mode (Max 100kbps) / High-speed mode (Max 400kbps) supported

- DMA Controller (8channels)

  The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

  - 8 independently configured and operated channels
  - Transfer can be started by software or request from the built-in peripherals
  - Transfer address area: 32-bit (4 Gbytes)
  - Transfer mode: Block transfer/Burst transfer/Demand transfer
  - Transfer data type: byte/half-word/word
  - Transfer block count: 1 to 16
  - Number of transfers: 1 to 65536

- A/D Converter (Max 24channels)

[12-bit A/D Converter]
- Successive Approximation type
- Built-in 2units
- Conversion time: 2.0µs @ 2.7V to 3.6V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

- Base Timer (Max 8channels)

  Operation mode is selectable from the followings for each channel.

  - 16-bit PWM timer
  - 16-bit PPG timer
  - 16/32-bit reload timer
  - 16/32-bit PWC timer

- General-Purpose I/O Port

  This series can use its pins as general-purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

  - Capable of pull-up control per pin
  - Capable of reading pin level directly
  - Built-in the port relocate function
  - Up to 83 fast general-purpose I/O Ports@100pin Package
  - Some ports are 5V tolerant I/O.

    See "■PIN DESCRIPTION" to confirm the corresponding pins.

- Dual Timer (32/16-bit Down Counter)

  The Dual Timer consists of two programmable 32/16-bit down counters.
  Operation mode is selectable from the followings for each channel.

  - Free-running
  - Periodic (=Reload)
  - One-shot

- HDMI-CEC/Remote Control Receiver (Up to 2channels)
  - HDMI-CEC transmitter
    - Header block automatic transmission by judging Signal free
    - Generating status interrupt by detecting Arbitration lost
    - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
    - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
  - HDMI-CEC receiver
    - Automatic ACK reply function available
    - Line error detection function available
  - Remote control receiver
    - 4 bytes reception buffer
    - Repeat code detection function available

- Real-time clock (RTC)

  The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

  - The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
  - Timer interrupt function after set time or each set time.
  - Capable of rewriting the time with continuing the time count.
  - Leap year automatic count is available.

- Watch Counter

  The Watch counter is used for wake up from sleep and timer mode.

  Interval timer: up to 64s (Max) @ Sub Clock : 32.768 kHz

- External Interrupt Controller Unit
  - Up to 16 external interrupt input pins
  - Include one non-maskable interrupt (NMI) input pin

- Watchdog Timer (2channels)

  A watchdog timer can generate interrupts or a reset when a time-out value is reached.

  This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

  The "Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption modes except RTC, STOP, Deep standby RTC, Deep standby STOP modes.

- CRC (Cyclic Redundancy Check) Accelerator

  The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

  CCITT CRC16 and IEEE-802.3 CRC32 are supported.

  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

- Clock and Reset

  [Clocks]

  Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillator, and Main PLL).

  - Main Clock : 4 MHz to 48 MHz
  - Sub Clock : 32.768 kHz
  - Built-in high-speed CR Clock : 4 MHz
  - Built-in low-speed CR Clock : 100 kHz
  - Main PLL Clock

  [Resets]

  - Reset requests from INITX pin
  - Power-on reset
  - Software reset
  - Watchdog timers reset
  - Low-voltage detection reset
  - Clock super visor reset

- Clock Super Visor (CSV)

  Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

  - External clock failure (clock stop) is detected, reset is asserted.
  - External frequency anomaly is detected, interrupt or reset is asserted.

- Low-Voltage Detector (LVD)

  This Series includes 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

  - LVD1: error reporting via interrupt
  - LVD2: auto-reset operation

- Low-Power Consumption Mode

  Six low-power consumption modes supported.

  - SLEEP
  - TIMER
  - RTC
  - STOP
  - Deep standby RTC (selectable between keeping the value of RAM and not)
  - Deep standby STOP (selectable between keeping the value of RAM and not)

- Debug
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Embedded Trace Macrocells (ETM)*

    *: MB9AFA41LA/MA, FA42LA/MA and FA44LA/MA support only SWJ-DP.

- Unique ID

  Unique value of the device (41-bit) is set.

- Power Supply

  Wide range voltage : VCC = 1.65V to 3.6V
  : VCC = 2.2V to 3.6V (when LCDC is used)

■ PRODUCT LINEUP

● Memory size

Product name		MB9AFA41LA/MA/NA	MB9AFA42LA/MA/NA	MB9AFA44LA/MA/NA
On-chip Flash memory	Main area	64 Kbytes	128 Kbytes	256 Kbytes
	Work area	32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM	SRAM0	8 Kbytes	8 Kbytes	16 Kbytes
	SRAM1	8 Kbytes	8 Kbytes	16 Kbytes
	Total	16 Kbytes	16 Kbytes	32 Kbytes

● Function

Product name		MB9AFA41LA MB9AFA42LA MB9AFA44LA	MB9AFA41MA MB9AFA42MA MB9AFA44MA	MB9AFA41NA MB9AFA42NA MB9AFA44NA
Pin count		64	80/96	100/112
CPU		Cortex-M3		
	Freq.	40 MHz		
Power supply voltage range		1.65V to 3.6V		
DMAC		8ch.		
External Bus Interface		-	Addr: 21-bit (Max) R/W Data: 8-bit (Max) CS: 4 (Max) Support: SRAM, NOR Flash memory	Addr: 25-bit (Max) R/W Data: 8/16-bit (Max) CS: 8 (Max) Support: SRAM, NOR Flash memory
LCD Controller		20 SEG × 8COM (Max)	33 SEG × 8COM (Max)	40 SEG × 8COM (Max)
Multi-function Serial Interface (UART/CSIO/I^{2}C)		8ch. (Max) ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO		
Base Timer (PWC/Reload timer/PWM/PPG)		8ch. (Max)		
Dual Timer		1 unit		
HDMI-CEC/ Remote Control Receiver		2ch. (Max)		
Real-Time Clock		1 unit		
Watch Counter		1 unit		
CRC Accelerator		Yes		
Watchdog timer		1ch. (SW) + 1ch. (HW)		
External Interrupts		8pins (Max) + NMI × 1	11pins (Max) + NMI × 1	16pins (Max) + NMI × 1
I/O ports		51pins (Max)	66pins (Max)	83pins (Max)
12-bit A/D converter		12ch. (2 units)	17ch. (2 units)	24ch. (2 units)
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2ch.		
Built-in CR	High-speed	4 MHz (± 2%)		
	Low-speed	100 kHz (Typ)		
Debug Function		SWJ-DP		SWJ-DP/ETM
Unique ID		Yes		

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.

■ PACKAGES

Package \ Product name	MB9AFA41LA MB9AFA42LA MB9AFA44LA	MB9AFA41MA MB9AFA42MA MB9AFA44MA	MB9AFA41NA MB9AFA42NA MB9AFA44NA
LQFP: FPT-64P-M38 (0.5mm pitch)	❍	-	-
LQFP: FPT-64P-M39 (0.65mm pitch)	❍	-	-
QFN: LCC-64P-M24 (0.5mm pitch)	❍	-	-
LQFP: FPT-80P-M37 (0.5mm pitch)	-	❍	-
LQFP: FPT-80P-M40 (0.65mm pitch)	-	❍	-
BGA: BGA-96P-M07 (0.5mm pitch)	-	❍	-
LQFP: FPT-100P-M23 (0.5mm pitch)	-	-	❍
QFP: FPT-100P-M36 (0.65mm pitch)	-	-	❍
BGA: BGA-112P-M04 (0.8mm pitch)	-	-	❍

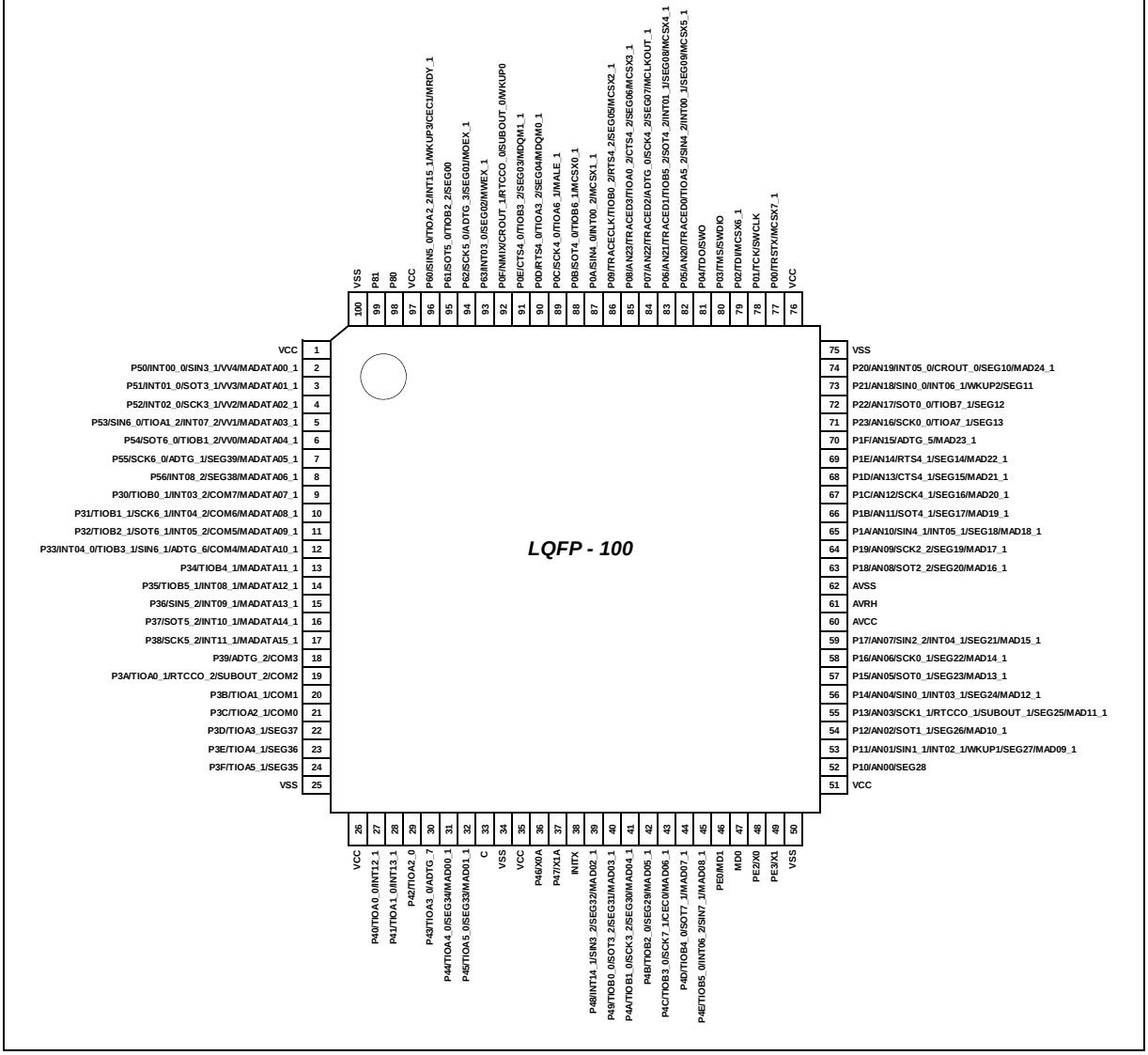
❍ : Supported

Note: See "■PACKAGE DIMENSIONS" for detailed information on each package.

■ PIN ASSIGNMENT

- FPT-100P-M23

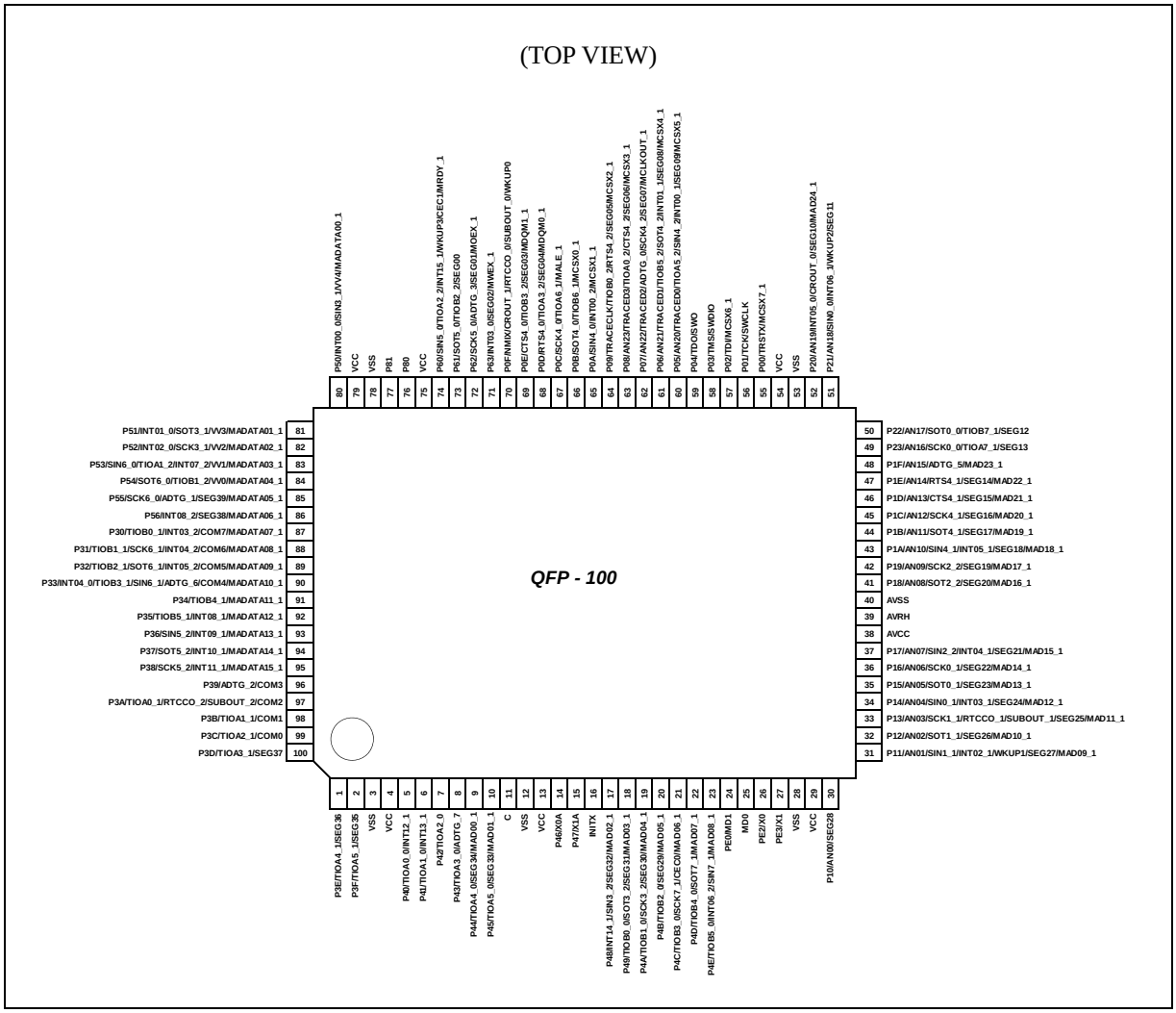
(TOP VIEW)



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

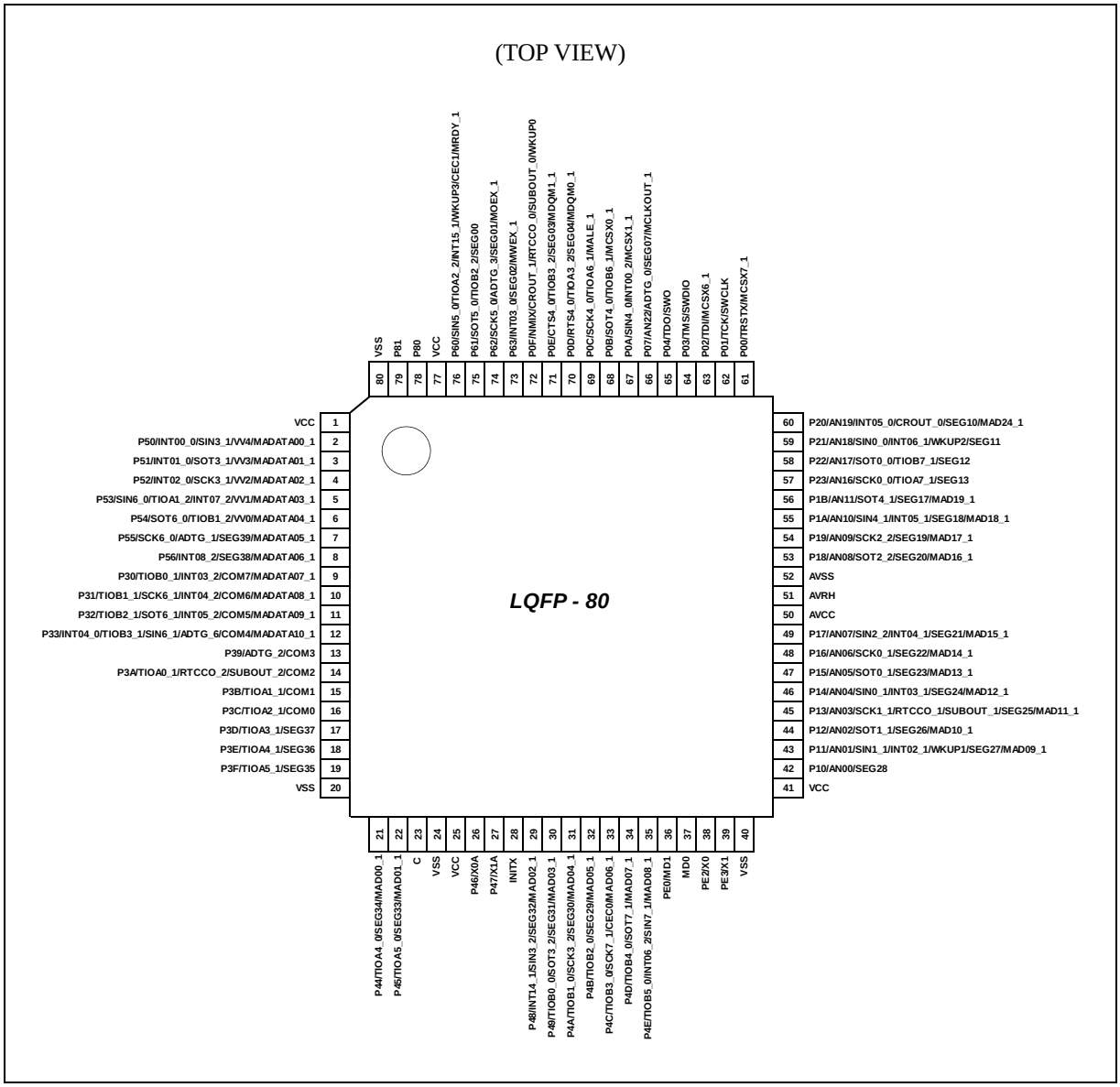
- FPT-100P-M36



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

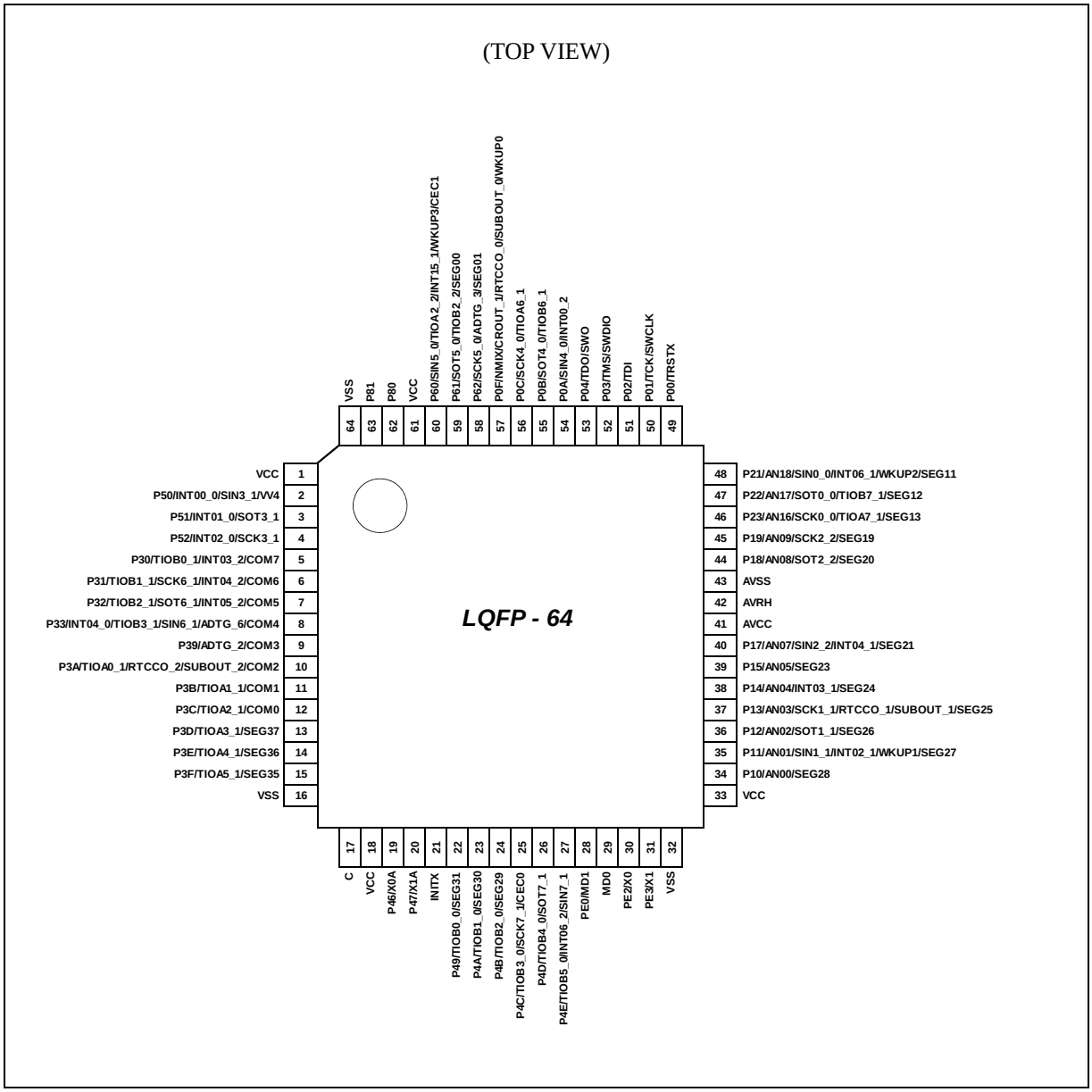
- FPT-80P-M37/M40



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

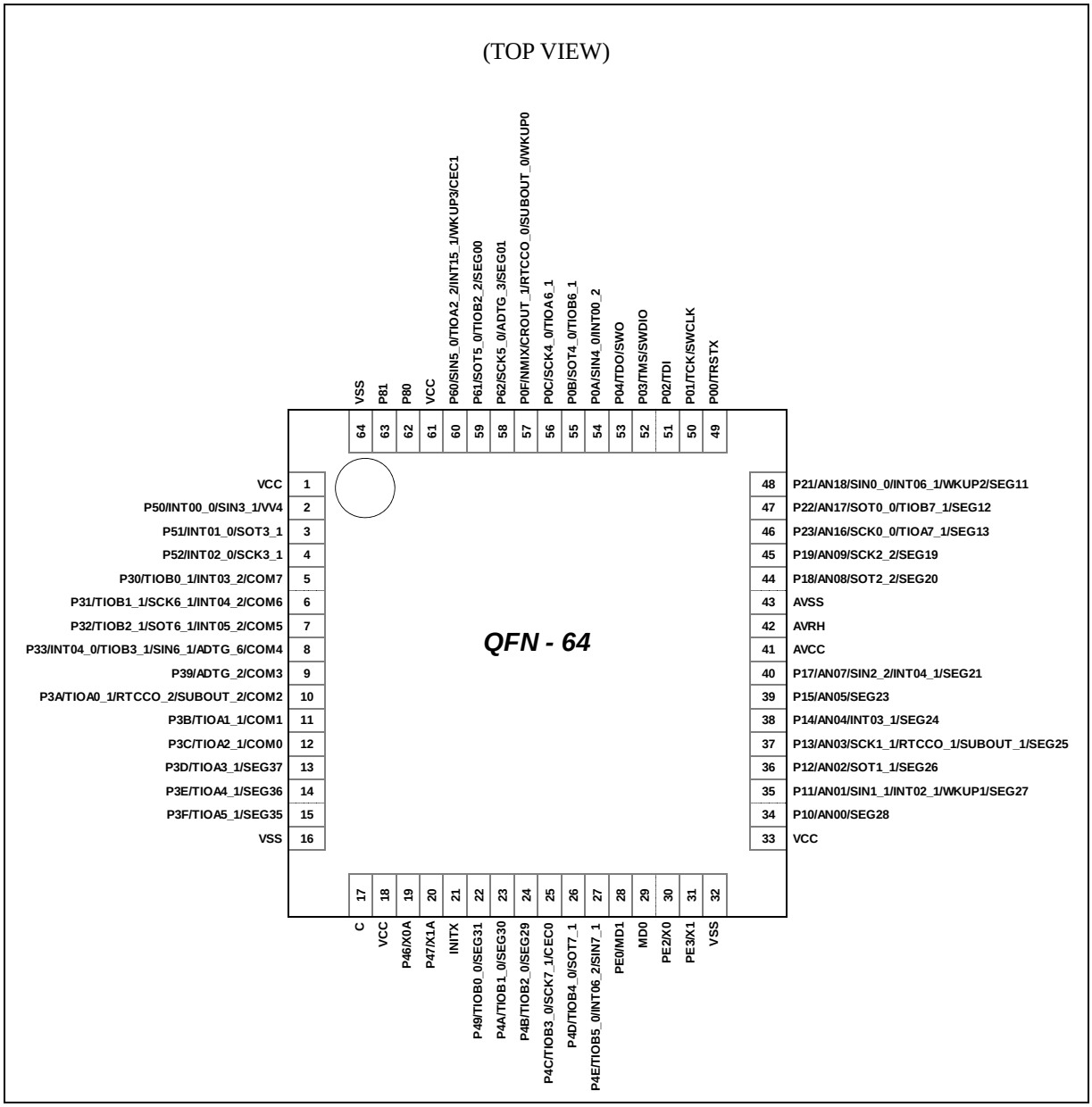
- FPT-64P-M38/M39



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

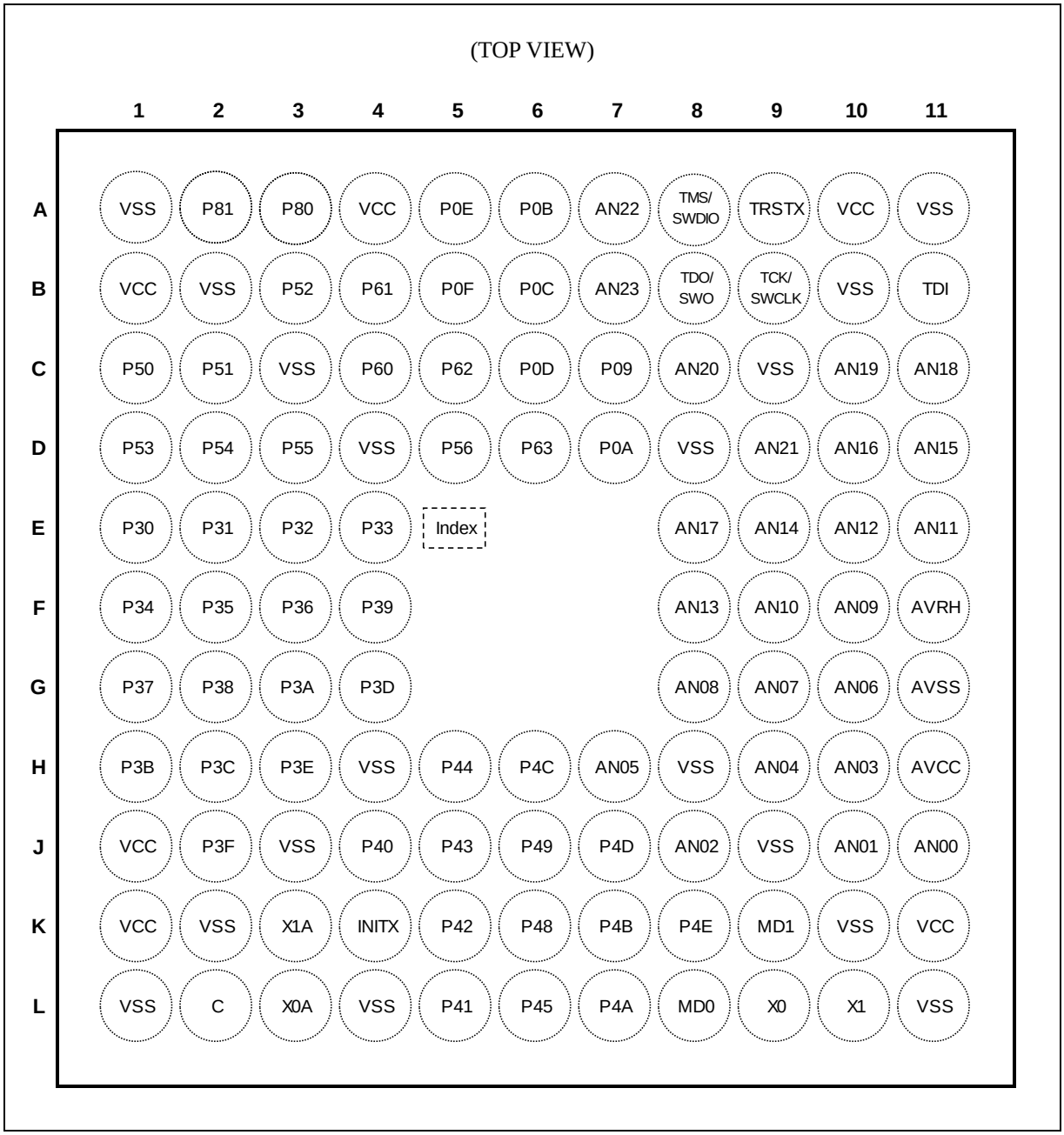
- LCC-64P-M24



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

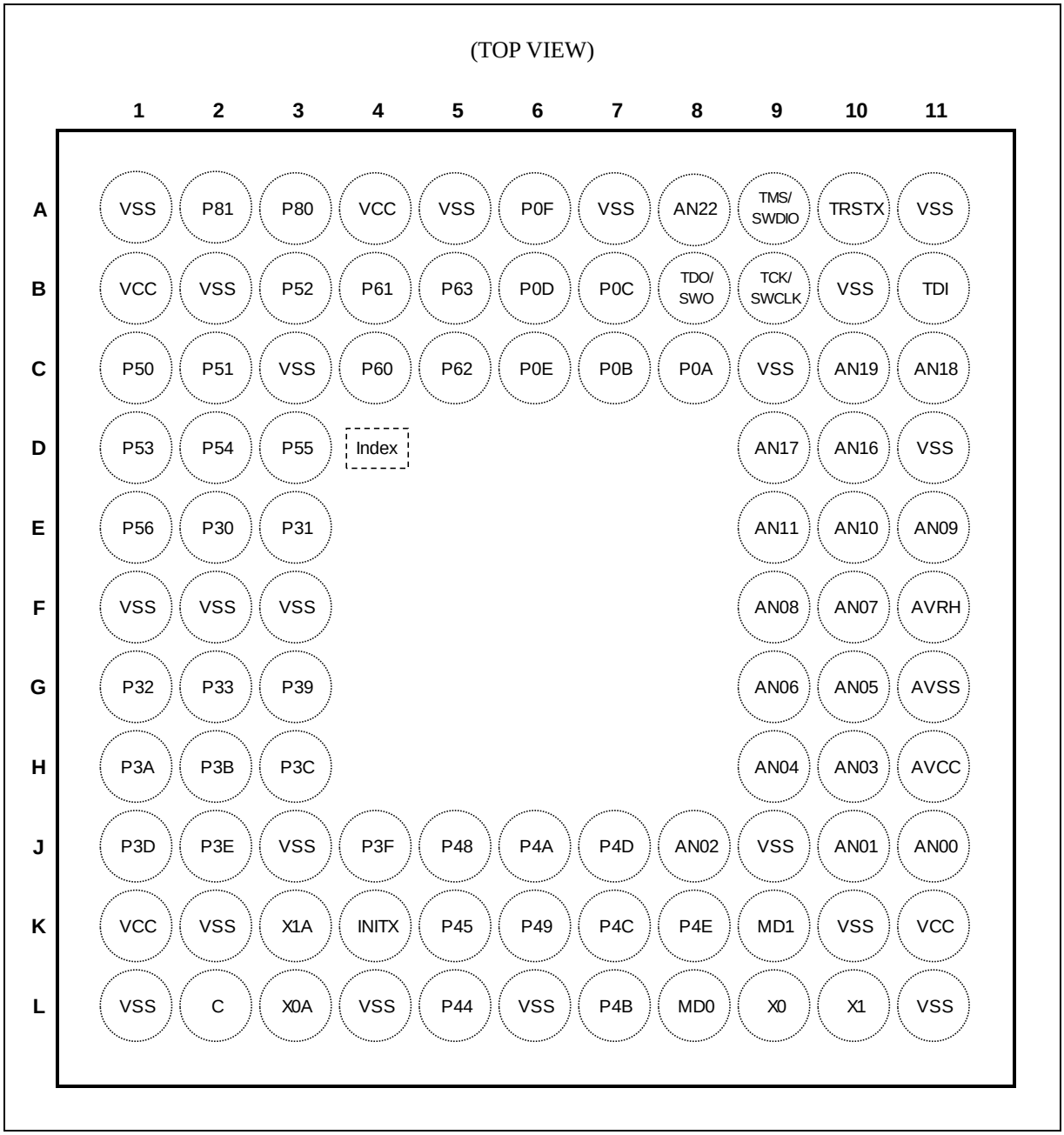
- BGA-112P-M04



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

- BGA-96P-M07



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ LIST OF PIN FUNCTIONS

- List of pin numbers

  The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
1	79	B1	1	B1	1	VCC	-	
2	80	C1	2	C1	2	P50	J	Y
						INT00_0		
						SIN3_1		
						VV4		
					-	MADATA00_1		
3	81	C2	3	C2	-	P51	J	Y
						INT01_0		
						SOT3_1 (SDA3_1)		
						VV3		
						MADATA01_1		
-	-	-	-	-	3	P51	E	L
						INT01_0		
						SOT3_1 (SDA3_1)		
4	82	B3	4	B3	-	P52	J	Y
						INT02_0		
						SCK3_1 (SCL3_1)		
						VV2		
						MADATA02_1		
-	-	-	-	-	4	P52	E	L
						INT02_0		
						SCK3_1 (SCL3_1)		
5	83	D1	5	D1	-	P53	J	Y
						SIN6_0		
						TIOA1_2		
						INT07_2		
						VV1		
						MADATA03_1		
6	84	D2	6	D2	-	P54	J	X
						SOT6_0 (SDA6_0)		
						TIOB1_2		
						VV0		
						MADATA04_1		

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
7	85	D3	7	D3	-	P55 SCK6_0 (SCL6_0) ADTG_1 SEG39 MADATA05_1	K	U
8	86	D5	8	E1	-	P56 INT08_2 SEG38 MADATA06_1	K	V
9	87	E1	9	E2	5	P30 TIOB0_1 INT03_2 COM7	K	V
					-	MADATA07_1		
10	88	E2	10	E3	6	P31 TIOB1_1 SCK6_1 (SCL6_1) INT04_2 COM6	K	V
					-	MADATA08_1		
11	89	E3	11	G1	7	P32 TIOB2_1 SOT6_1 (SDA6_1) INT05_2 COM5	K	V
					-	MADATA09_1		
12	90	E4	12	G2	8	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6 COM4	K	V
					-	MADATA10_1		
13	91	F1	-	-	-	P34 TIOB4_1 MADATA11_1	E	K
14	92	F2	-	-	-	P35 TIOB5_1 INT08_1 MADATA12_1	E	L

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
15	93	F3	-	-	-	P36 SIN5_2 INT09_1 MADATA13_1	E	L
-	-	-	-	F1	-	VSS	-	
-	-	-	-	F2	-	VSS	-	
-	-	-	-	F3	-	VSS	-	
16	94	G1	-	-	-	P37 SOT5_2 (SDA5_2) INT10_1 MADATA14_1	E	L
17	95	G2	-	-	-	P38 SCK5_2 (SCL5_2) INT11_1 MADATA15_1	E	L
18	96	F4	13	G3	9	P39 ADTG_2 COM3	K	U
19	97	G3	14	H1	10	P3A TIOA0_1 RTCCO_2 SUBOUT_2 COM2	K	U
20	98	H1	15	H2	11	P3B TIOA1_1 COM1	K	U
21	99	H2	16	H3	12	P3C TIOA2_1 COM0	K	U
22	100	G4	17	J1	13	P3D TIOA3_1 SEG37	K	U
-	-	B2	-	B2	-	VSS	-	
23	1	H3	18	J2	14	P3E TIOA4_1 SEG36	K	U
24	2	J2	19	J4	15	P3F TIOA5_1 SEG35	K	U
25	3	L1	20	L1	16	VSS	-	
26	4	J1	-	-	-	VCC	-	

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
27	5	J4	-	-	-	P40	E	L
						TIOA0_0		
						INT12_1		
28	6	L5	-	-	-	P41	E	L
						TIOA1_0		
						INT13_1		
29	7	K5	-	-	-	P42	E	K
						TIOA2_0		
30	8	J5	-	-	-	P43	E	K
						TIOA3_0		
						ADTG_7		
31	9	H5	21	L5	-	P44	K	U
						TIOA4_0		
						SEG34		
						MAD00_1		
32	10	L6	22	K5	-	P45	K	U
						TIOA5_0		
						SEG33		
						MAD01_1		
-	-	K2	-	K2	-	VSS	-	
-	-	J3	-	J3	-	VSS	-	
-	-	H4	-	-	-	VSS	-	
-	-	-	-	L6	-	VSS	-	
33	11	L2	23	L2	17	C	-	
34	12	L4	24	L4	-	VSS	-	
35	13	K1	25	K1	18	VCC	-	
36	14	L3	26	L3	19	P46	D	F
						X0A		
37	15	K3	27	K3	20	P47	D	G
						X1A		
38	16	K4	28	K4	21	INITX	B	C
39	17	K6	29	J5	-	P48	K	V
						INT14_1		
						SIN3_2		
						SEG32		
						MAD02_1		
40	18	J6	30	K6	22	P49	K	U
						TIOB0_0		
						SEG31		
					-	SOT3_2 (SDA3_2)		
						MAD03_1		

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
41	19	L7	31	J6	23	P4A	K	U
						TIOB1_0		
						SEG30		
					-	SCK3_2 (SCL3_2)		
						MAD04_1		
42	20	K7	32	L7	24	P4B	K	U
						TIOB2_0		
						SEG29		
					-	MAD05_1		
43	21	H6	33	K7	25	P4C	I*	S
						TIOB3_0		
						SCK7_1 (SCL7_1)		
						CEC0		
					-	MAD06_1		
44	22	J7	34	J7	26	P4D	I*	K
						TIOB4_0		
						SOT7_1 (SDA7_1)		
					-	MAD07_1		
45	23	K8	35	K8	27	P4E	I*	L
						TIOB5_0		
						INT06_2		
						SIN7_1		
					-	MAD08_1		
46	24	K9	36	K9	28	MD1	C	E
						PE0		
47	25	L8	37	L8	29	MD0	G	D
48	26	L9	38	L9	30	X0	A	A
						PE2		
49	27	L10	39	L10	31	X1	A	B
						PE3		
50	28	L11	40	L11	32	VSS	-	
51	29	K11	41	K11	33	VCC	-	
52	30	J11	42	J11	34	P10	L	W
						AN00		
						SEG28		
53	31	J10	43	J10	35	P11	L	R
						AN01		
						SIN1_1		
						INT02_1		
						WKUP1		
						SEG27		
					-	MAD09_1		

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
54	32	J8	44	J8	36	P12	L	W
						AN02		
						SOT1_1 (SDA1_1)		
						SEG26		
					-	MAD10_1		
-	-	K10	-	K10	-	VSS	-	
-	-	J9	-	J9	-	VSS	-	
55	33	H10	45	H10	37	P13	L	W
						AN03		
						SCK1_1 (SCL1_1)		
						RTCCO_1		
						SEG25		
						SUBOUT_1		
					-	MAD11_1		
56	34	H9	46	H9	38	P14	L	N
						AN04		
						INT03_1		
						SEG24		
					-	SIN0_1		
						MAD12_1		
57	35	H7	47	G10	39	P15	L	W
						AN05		
						SEG23		
					-	SOT0_1 (SDA0_1)		
						MAD13_1		
58	36	G10	48	G9	-	P16	L	W
						AN06		
						SCK0_1 (SCL0_1)		
						SEG22		
						MAD14_1		
59	37	G9	49	F10	40	P17	L	N
						AN07		
						SIN2_2		
						INT04_1		
						SEG21		
					-	MAD15_1		
60	38	H11	50	H11	41	AVCC	-	
61	39	F11	51	F11	42	AVRH	-	
62	40	G11	52	G11	43	AVSS	-	

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
63	41	G8	53	F9	44	P18	L	W
						AN08		
						SOT2_2 (SDA2_2)		
						SEG20		
					-	MAD16_1		
64	42	F10	54	E11	45	P19	L	W
						AN09		
						SCK2_2 (SCL2_2)		
						SEG19		
					-	MAD17_1		
-	-	H8	-	-	-	VSS	-	
65	43	F9	55	E10	-	P1A	L	N
						AN10		
						SIN4_1		
						INT05_1		
						SEG18		
						MAD18_1		
66	44	E11	56	E9	-	P1B	L	W
						AN11		
						SOT4_1 (SDA4_1)		
						SEG17		
						MAD19_1		
67	45	E10	-	-	-	P1C	L	W
						AN12		
						SCK4_1 (SCL4_1)		
						SEG16		
						MAD20_1		
68	46	F8	-	-	-	P1D	L	W
						AN13		
						CTS4_1		
						SEG15		
						MAD21_1		
69	47	E9	-	-	-	P1E	L	W
						AN14		
						RTS4_1		
						SEG14		
						MAD22_1		
70	48	D11	-	-	-	P1F	F	M
						AN15		
						ADTG_5		
						MAD23_1		

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
-	-	B10	-	B10	-	VSS	-	
-	-	C9	-	C9	-	VSS	-	
-	-	-	-	D11	-	VSS	-	
71	49	D10	57	D10	46	P23 AN16 SCK0_0 (SCL0_0) TIOA7_1 SEG13	L	W
72	50	E8	58	D9	47	P22 AN17 SOT0_0 (SDA0_0) TIOB7_1 SEG12	L	W
73	51	C11	59	C11	48	P21 AN18 SIN0_0 INT06_1 WKUP2 SEG11	L	R
74	52	C10	60	C10	-	P20 AN19 INT05_0 CROUT_0 SEG10 MAD24_1	L	N
75	53	A11	-	A11	-	VSS	-	
76	54	A10	-	-	-	VCC	-	
77	55	A9	61	A10	49	P00 TRSTX	E	J
					-	MCSX7_1		
78	56	B9	62	B9	50	P01 TCK SWCLK	E	J
79	57	B11	63	B11	51	P02 TDI	E	J
					-	MCSX6_1		
80	58	A8	64	A9	52	P03 TMS SWDIO	E	J
81	59	B8	65	B8	53	P04 TDO SWO	E	J

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
82	60	C8	-	-	-	P05 AN20 TRACED0 TIOA5_2 SIN4_2 INT00_1 SEG09 MCSX5_1	L	Q
-	-	D8	-	-	-	VSS	-	
83	61	D9	-	-	-	P06 AN21 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 SEG08 MCSX4_1	L	Q
84	62	A7	66	A8	-	P07 AN22 ADTG_0 SEG07 MCLKOUT_1	L	P
			-	-		TRACED2 SCK4_2 (SCL4_2)		
-	-	-	-	A7	-	VSS	-	
85	63	B7	-	-	-	P08 AN23 TRACED3 TIOA0_2 CTS4_2 SEG06 MCSX3_1	L	P
86	64	C7	-	-	-	P09 TRACECLK TIOB0_2 RTS4_2 SEG05 MCSX2_1	K	O
87	65	D7	67	C8	54	P0A SIN4_0 INT00_2	I*	L
					-	MCSX1_1		

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
88	66	A6	68	C7	55	P0B	I*	K
						SOT4_0 (SDA4_0)		
						TIOB6_1		
					-	MCSX0_1		
89	67	B6	69	B7	56	P0C	I*	K
						SCK4_0 (SCL4_0)		
						TIOA6_1		
					-	MALE_1		
-	-	D4	-	-	-	VSS	-	
-	-	C3	-	C3	-	VSS	-	
90	68	C6	70	B6	-	P0D	K	U
						RTS4_0		
						TIOA3_2		
						SEG04		
						MDQM0_1		
91	69	A5	71	C6	-	P0E	K	U
						CTS4_0		
						TIOB3_2		
						SEG03		
						MDQM1_1		
-	-	-	-	A5	-	VSS	-	
92	70	B5	72	A6	57	P0F	E	I
						NMIX		
						CROUT_1		
						RTCCO_0		
						SUBOUT_0		
						WKUP0		
93	71	D6	73	B5	-	P63	K	V
						INT03_0		
						SEG02		
						MWEX_1		
94	72	C5	74	C5	58	P62	K	U
						SCK5_0 (SCL5_0)		
						ADTG_3		
						SEG01		
					-	MOEX_1		
95	73	B4	75	B4	59	P61	K	U
						SOT5_0 (SDA5_0)		
						TIOB2_2		
						SEG00		

Pin No						Pin Name	I/O circuit type	Pin state type
LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP-64 QFN-64			
96	74	C4	76	C4	60	P60	I*	T
						SIN5_0		
						TIOA2_2		
						INT15_1		
						WKUP3		
						CEC1		
					-	MRDY_1		
97	75	A4	77	A4	61	VCC	-	
98	76	A3	78	A3	62	P80	H	H
99	77	A2	79	A2	63	P81	H	H
100	78	A1	80	A1	64	VSS	-	-

*: 5V tolerant I/O

- List of pin functions
  The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
ADC	ADTG_0	A/D converter external trigger input pin	84	62	A7	66	A8	-
	ADTG_1		7	85	D3	7	D3	-
	ADTG_2		18	96	F4	13	G3	9
	ADTG_3		94	72	C5	74	C5	58
	ADTG_4		-	-	-	-	-	-
	ADTG_5		70	48	D11	-	-	-
	ADTG_6		12	90	E4	12	G2	8
	ADTG_7		30	8	J5	-	-	-
	ADTG_8		-	-	-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	52	30	J11	42	J11	34
	AN01		53	31	J10	43	J10	35
	AN02		54	32	J8	44	J8	36
	AN03		55	33	H10	45	H10	37
	AN04		56	34	H9	46	H9	38
	AN05		57	35	H7	47	G10	39
	AN06		58	36	G10	48	G9	-
	AN07		59	37	G9	49	F10	40
	AN08		63	41	G8	53	F9	44
	AN09		64	42	F10	54	E11	45
	AN10		65	43	F9	55	E10	-
	AN11		66	44	E11	56	E9	-
	AN12		67	45	E10	-	-	-
	AN13		68	46	F8	-	-	-
	AN14		69	47	E9	-	-	-
	AN15		70	48	D11	-	-	-
	AN16		71	49	D10	57	D10	46
	AN17		72	50	E8	58	D9	47
	AN18		73	51	C11	59	C11	48
	AN19		74	52	C10	60	C10	-
	AN20		82	60	C8	-	-	-
	AN21		83	61	D9	-	-	-
	AN22		84	62	A7	66	A8	-
	AN23		85	63	B7	-	-	-

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	27	5	J4	-	-	-
	TIOA0_1		19	97	G3	14	H1	10
	TIOA0_2		85	63	B7	-	-	-
	TIOB0_0	Base timer ch.0 TIOB pin	40	18	J6	30	K6	22
	TIOB0_1		9	87	E1	9	E2	5
	TIOB0_2		86	64	C7	-	-	-
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	28	6	L5	-	-	-
	TIOA1_1		20	98	H1	15	H2	11
	TIOA1_2		5	83	D1	5	D1	-
	TIOB1_0	Base timer ch.1 TIOB pin	41	19	L7	31	J6	23
	TIOB1_1		10	88	E2	10	E3	6
	TIOB1_2		6	84	D2	6	D2	-
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	29	7	K5	-	-	-
	TIOA2_1		21	99	H2	16	H3	12
	TIOA2_2		96	74	C4	76	C4	60
	TIOB2_0	Base timer ch.2 TIOB pin	42	20	K7	32	L7	24
	TIOB2_1		11	89	E3	11	G1	7
	TIOB2_2		95	73	B4	75	B4	59
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	30	8	J5	-	-	-
	TIOA3_1		22	100	G4	17	J1	13
	TIOA3_2		90	68	C6	70	B6	-
	TIOB3_0	Base timer ch.3 TIOB pin	43	21	H6	33	K7	25
	TIOB3_1		12	90	E4	12	G2	8
	TIOB3_2		91	69	A5	71	C6	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	31	9	H5	21	L5	-
	TIOA4_1		23	1	H3	18	J2	14
	TIOA4_2		-	-	-	-	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	44	22	J7	34	J7	26
	TIOB4_1		13	91	F1	-	-	-
	TIOB4_2		-	-	-	-	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	32	10	L6	22	K5	-
	TIOA5_1		24	2	J2	19	J4	15
	TIOA5_2		82	60	C8	-	-	-
	TIOB5_0	Base timer ch.5 TIOB pin	45	23	K8	35	K8	27
	TIOB5_1		14	92	F2	-	-	-
	TIOB5_2		83	61	D9	-	-	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	89	67	B6	69	B7	56
	TIOB6_1	Base timer ch.6 TIOB pin	88	66	A6	68	C7	55
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-	-	-	-	-
	TIOA7_1		71	49	D10	57	D10	46
	TIOA7_2		-	-	-	-	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-	-	-	-	-
	TIOB7_1		72	50	E8	58	D9	47
	TIOB7_2		-	-	-	-	-	-

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Debugger	SWCLK	Serial wire debug interface clock input pin	78	56	B9	62	B9	50
	SWDIO	Serial wire debug interface data input / output pin	80	58	A8	64	A9	52
	SWO	Serial wire viewer output pin	81	59	B8	65	B8	53
	TCK	J-TAG test clock input pin	78	56	B9	62	B9	50
	TDI	J-TAG test data input pin	79	57	B11	63	B11	51
	TDO	J-TAG debug data output pin	81	59	B8	65	B8	53
	TMS	J-TAG test mode state input/output pin	80	58	A8	64	A9	52
	TRACECLK	Trace CLK output pin of ETM	86	64	C7	-	-	-
	TRACED0	Trace data output pins of ETM	82	60	C8	-	-	-
	TRACED1		83	61	D9	-	-	-
	TRACED2		84	62	A7	-	-	-
	TRACED3		85	63	B7	-	-	-
	TRSTX	J-TAG test reset input pin	77	55	A9	61	A10	49
External Bus	MAD00_1	External bus interface address bus	31	9	H5	21	L5	-
	MAD01_1		32	10	L6	22	K5	-
	MAD02_1		39	17	K6	29	J5	-
	MAD03_1		40	18	J6	30	K6	-
	MAD04_1		41	19	L7	31	J6	-
	MAD05_1		42	20	K7	32	L7	-
	MAD06_1		43	21	H6	33	K7	-
	MAD07_1		44	22	J7	34	J7	-
	MAD08_1		45	23	K8	35	K8	-
	MAD09_1		53	31	J10	43	J10	-
	MAD10_1		54	32	J8	44	J8	-
	MAD11_1		55	33	H10	45	H10	-
	MAD12_1		56	34	H9	46	H9	-
	MAD13_1		57	35	H7	47	G10	-
	MAD14_1		58	36	G10	48	G9	-
	MAD15_1		59	37	G9	49	F10	-
	MAD16_1		63	41	G8	53	F9	-
	MAD17_1		64	42	F10	54	E11	-
	MAD18_1		65	43	F9	55	E10	-
	MAD19_1		66	44	E11	56	E9	-
	MAD20_1		67	45	E10	-	-	-
	MAD21_1		68	46	F8	-	-	-
	MAD22_1		69	47	E9	-	-	-
	MAD23_1		70	48	D11	-	-	-
	MAD24_1		74	52	C10	60	C10	-

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
External Bus	MCSX0_1	External bus interface chip select output pin	88	66	A6	68	C7	-
	MCSX1_1		87	65	D7	67	C8	-
	MCSX2_1		86	64	C7	-	-	-
	MCSX3_1		85	63	B7	-	-	-
	MCSX4_1		83	61	D9	-	-	-
	MCSX5_1		82	60	C8	-	-	-
	MCSX6_1		79	57	B11	63	B11	-
	MCSX7_1		77	55	A9	61	A10	-
	MDQM0_1	External bus interface byte mask signal output pin	90	68	C6	70	B6	-
	MDQM1_1		91	69	A5	71	C6	-
	MOEX_1	External bus interface read enable signal for SRAM	94	72	C5	74	C5	-
	MWEX_1	External bus interface write enable signal for SRAM	93	71	D6	73	B5	-
	MADATA00_1	External bus interface data bus	2	80	C1	2	C1	-
	MADATA01_1		3	81	C2	3	C2	-
	MADATA02_1		4	82	B3	4	B3	-
	MADATA03_1		5	83	D1	5	D1	-
	MADATA04_1		6	84	D2	6	D2	-
	MADATA05_1		7	85	D3	7	D3	-
	MADATA06_1		8	86	D5	8	E1	-
	MADATA07_1		9	87	E1	9	E2	-
	MADATA08_1		10	88	E2	10	E3	-
	MADATA09_1		11	89	E3	11	G1	-
	MADATA10_1		12	90	E4	12	G2	-
	MADATA11_1		13	91	F1	-	-	-
	MADATA12_1		14	92	F2	-	-	-
	MADATA13_1		15	93	F3	-	-	-
	MADATA14_1		16	94	G1	-	-	-
	MADATA15_1		17	95	G2	-	-	-
	MALE_1	Address Latch enable signal for multiplex	89	67	B6	69	B7	-
	MRDY_1	External RDY input signal	96	74	C4	76	C4	-
	MCLKOUT_1	External bus clock output pin	84	62	A7	66	A8	-

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
External Interrupt	INT00_0	External interrupt request 00 input pin	2	80	C1	2	C1	2
	INT00_1		82	60	C8	-	-	-
	INT00_2		87	65	D7	67	C8	54
	INT01_0	External interrupt request 01 input pin	3	81	C2	3	C2	3
	INT01_1		83	61	D9	-	-	-
	INT02_0	External interrupt request 02 input pin	4	82	B3	4	B3	4
	INT02_1		53	31	J10	43	J10	35
	INT03_0	External interrupt request 03 input pin	93	71	D6	73	B5	-
	INT03_1		56	34	H9	46	H9	38
	INT03_2		9	87	E1	9	E2	5
	INT04_0	External interrupt request 04 input pin	12	90	E4	12	G2	8
	INT04_1		59	37	G9	49	F10	40
	INT04_2		10	88	E2	10	E3	6
	INT05_0	External interrupt request 05 input pin	74	52	C10	60	C10	-
	INT05_1		65	43	F9	55	E10	-
	INT05_2		11	89	E3	11	G1	7
	INT06_1	External interrupt request 06 input pin	73	51	C11	59	C11	48
	INT06_2		45	23	K8	35	K8	27
	INT07_2	External interrupt request 07 input pin	5	83	D1	5	D1	-
	INT08_1	External interrupt request 08 input pin	14	92	F2	-	-	-
	INT08_2		8	86	D5	8	E1	-
	INT09_1	External interrupt request 09 input pin	15	93	F3	-	-	-
	INT10_1	External interrupt request 10 input pin	16	94	G1	-	-	-
	INT11_1	External interrupt request 11 input pin	17	95	G2	-	-	-
	INT12_1	External interrupt request 12 input pin	27	5	J4	-	-	-
	INT13_1	External interrupt request 13 input pin	28	6	L5	-	-	-
	INT14_1	External interrupt request 14 input pin	39	17	K6	29	J5	-
	INT15_1	External interrupt request 15 input pin	96	74	C4	76	C4	60
	NMIX	Non-Maskable Interrupt input pin	92	70	B5	72	A6	57

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
GPIO	P00	General-purpose I/O port 0	77	55	A9	61	A10	49
	P01		78	56	B9	62	B9	50
	P02		79	57	B11	63	B11	51
	P03		80	58	A8	64	A9	52
	P04		81	59	B8	65	B8	53
	P05		82	60	C8	-	-	-
	P06		83	61	D9	-	-	-
	P07		84	62	A7	66	A8	-
	P08		85	63	B7	-	-	-
	P09		86	64	C7	-	-	-
	P0A		87	65	D7	67	C8	54
	P0B		88	66	A6	68	C7	55
	P0C		89	67	B6	69	B7	56
	P0D		90	68	C6	70	B6	-
	P0E		91	69	A5	71	C6	-
	P0F		92	70	B5	72	A6	57
	P10	General-purpose I/O port 1	52	30	J11	42	J11	34
	P11		53	31	J10	43	J10	35
	P12		54	32	J8	44	J8	36
	P13		55	33	H10	45	H10	37
	P14		56	34	H9	46	H9	38
	P15		57	35	H7	47	G10	39
	P16		58	36	G10	48	G9	-
	P17		59	37	G9	49	F10	40
	P18		63	41	G8	53	F9	44
	P19		64	42	F10	54	E11	45
	P1A		65	43	F9	55	E10	-
	P1B		66	44	E11	56	E9	-
	P1C		67	45	E10	-	-	-
	P1D		68	46	F8	-	-	-
	P1E		69	47	E9	-	-	-
	P1F		70	48	D11	-	-	-
	P20	General-purpose I/O port 2	74	52	C10	60	C10	-
	P21		73	51	C11	59	C11	48
	P22		72	50	E8	58	D9	47
	P23		71	49	D10	57	D10	46

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
GPIO	P30	General-purpose I/O port 3	9	87	E1	9	E2	5
	P31		10	88	E2	10	E3	6
	P32		11	89	E3	11	G1	7
	P33		12	90	E4	12	G2	8
	P34		13	91	F1	-	-	-
	P35		14	92	F2	-	-	-
	P36		15	93	F3	-	-	-
	P37		16	94	G1	-	-	-
	P38		17	95	G2	-	-	-
	P39		18	96	F4	13	G3	9
	P3A		19	97	G3	14	H1	10
	P3B		20	98	H1	15	H2	11
	P3C		21	99	H2	16	H3	12
	P3D		22	100	G4	17	J1	13
	P3E		23	1	H3	18	J2	14
	P3F		24	2	J2	19	J4	15
	P40	General-purpose I/O port 4	27	5	J4	-	-	-
	P41		28	6	L5	-	-	-
	P42		29	7	K5	-	-	-
	P43		30	8	J5	-	-	-
	P44		31	9	H5	21	L5	-
	P45		32	10	L6	22	K5	-
	P46		36	14	L3	26	L3	19
	P47		37	15	K3	27	K3	20
	P48		39	17	K6	29	J5	-
	P49		40	18	J6	30	K6	22
	P4A		41	19	L7	31	J6	23
	P4B		42	20	K7	32	L7	24
	P4C		43	21	H6	33	K7	25
	P4D		44	22	J7	34	J7	26
	P4E		45	23	K8	35	K8	27
	P50	General-purpose I/O port 5	2	80	C1	2	C1	2
	P51		3	81	C2	3	C2	3
	P52		4	82	B3	4	B3	4
	P53		5	83	D1	5	D1	-
	P54		6	84	D2	6	D2	-
	P55		7	85	D3	7	D3	-
	P56		8	86	D5	8	E1	-
	P60	General-purpose I/O port 6	96	74	C4	76	C4	60
	P61		95	73	B4	75	B4	59
	P62		94	72	C5	74	C5	58
	P63		93	71	D6	73	B5	-
	P80	General-purpose I/O port 8	98	76	A3	78	A3	62
	P81		99	77	A2	79	A2	63
	PE0	General-purpose I/O port E	46	24	K9	36	K9	28
	PE2		48	26	L9	38	L9	30
	PE3		49	27	L10	39	L10	31

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	73	51	C11	59	C11	48
	SIN0_1		56	34	H9	46	H9	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I^2C (operation mode 4).	72	50	E8	58	D9	47
	SOT0_1 (SDA0_1)		57	35	H7	47	G10	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I^2C (operation mode 4).	71	49	D10	57	D10	46
	SCK0_1 (SCL0_1)		58	36	G10	48	G9	-
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	53	31	J10	43	J10	35
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I^2C (operation mode 4).	54	32	J8	44	J8	36
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I^2C (operation mode 4).	55	33	H10	45	H10	37

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Multi-function Serial 2	SIN2_2	Multi-function serial interface ch.2 input pin	59	37	G9	49	F10	40
	SOT2_2 (SDA2_2)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I^2C (operation mode 4).	63	41	G8	53	F9	44
	SCK2_2 (SCL2_2)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	64	42	F10	54	E11	45
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	80	C1	2	C1	2
	SIN3_2		39	17	K6	29	J5	-
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I^2C (operation mode 4).	3	81	C2	3	C2	3
	SOT3_2 (SDA3_2)		40	18	J6	30	K6	-
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	82	B3	4	B3	4
	SCK3_2 (SCL3_2)		41	19	L7	31	J6	-

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	87	65	D7	67	C8	54
	SIN4_1		65	43	F9	55	E10	-
	SIN4_2		82	60	C8	-	-	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I^2C (operation mode 4).	88	66	A6	68	C7	55
	SOT4_1 (SDA4_1)		66	44	E11	56	E9	-
	SOT4_2 (SDA4_2)		83	61	D9	-	-	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	89	67	B6	69	B7	56
	SCK4_1 (SCL4_1)		67	45	E10	-	-	-
	SCK4_2 (SCL4_2)		84	62	A7	-	-	-
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	90	68	C6	70	B6	-
	RTS4_1		69	47	E9	-	-	-
	RTS4_2		86	64	C7	-	-	-
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	91	69	A5	71	C6	-
	CTS4_1		68	46	F8	-	-	-
	CTS4_2		85	63	B7	-	-	-
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	96	74	C4	76	C4	60
	SIN5_2		15	93	F3	-	-	-
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I^2C (operation mode 4).	95	73	B4	75	B4	59
	SOT5_2 (SDA5_2)		16	94	G1	-	-	-
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I^2C (operation mode 4).	94	72	C5	74	C5	58
	SCK5_2 (SCL5_2)		17	95	G2	-	-	-

Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	5	83	D1	5	D1	-
	SIN6_1		12	90	E4	12	G2	8
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I^2C (operation mode 4).	6	84	D2	6	D2	-
	SOT6_1 (SDA6_1)		11	89	E3	11	G1	7
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	85	D3	7	D3	-
	SCK6_1 (SCL6_1)		10	88	E2	10	E3	6
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	45	23	K8	35	K8	27
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I^2C (operation mode 4).	44	22	J7	34	J7	26
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	43	21	H6	33	K7	25

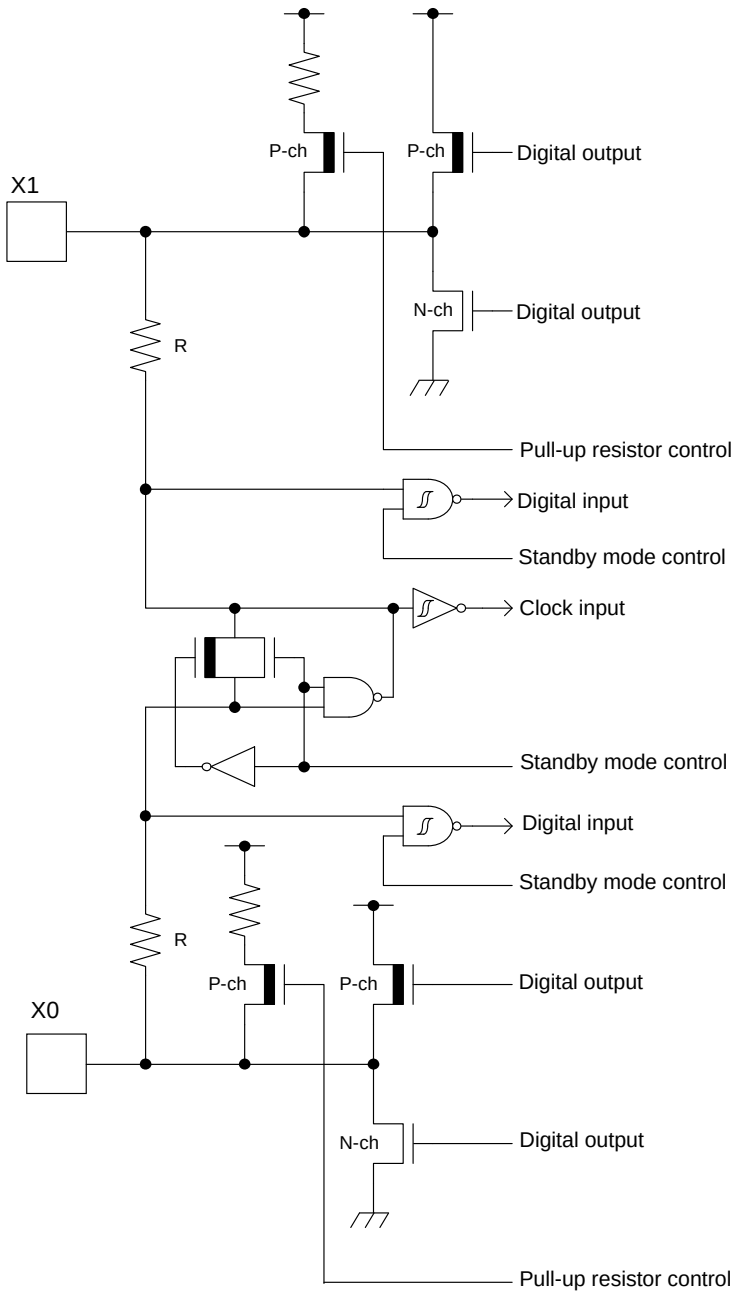
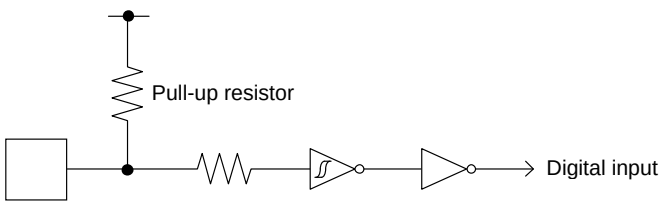
Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	92	70	B5	72	A6	57
	RTCCO_1		55	33	H10	45	H10	37
	RTCCO_2		19	97	G3	14	H1	10
	SUBOUT_0	Sub clock output pin	92	70	B5	72	A6	57
	SUBOUT_1		55	33	H10	45	H10	37
	SUBOUT_2		19	97	G3	14	H1	10
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	92	70	B5	72	A6	57
	WKUP1	Deep standby mode return signal input pin 1	53	31	J10	43	J10	35
	WKUP2	Deep standby mode return signal input pin 2	73	51	C11	59	C11	48
	WKUP3	Deep standby mode return signal input pin 3	96	74	C4	76	C4	60
HDMI-CEC/ Remote Control Reception	CEC0	HDMI-CEC/RemoteControl Reception ch.0 input/output pin	43	21	H6	33	K7	25
	CEC1	HDMI-CEC/RemoteControl Reception ch.1 input/output pin	96	74	C4	76	C4	60
LCDC	VV0	LCD drive power supply pin	6	84	D2	6	D2	-
	VV1		5	83	D1	5	D1	-
	VV2		4	82	B3	4	B3	-
	VV3		3	81	C2	3	C2	-
	VV4		2	80	C1	2	C1	2
	COM0	LCD common output pin	21	99	H2	16	H3	12
	COM1		20	98	H1	15	H2	11
	COM2		19	97	G3	14	H1	10
	COM3		18	96	F4	13	G3	9
	COM4		12	90	E4	12	G2	8
	COM5		11	89	E3	11	G1	7
	COM6		10	88	E2	10	E3	6
	COM7		9	87	E1	9	E2	5

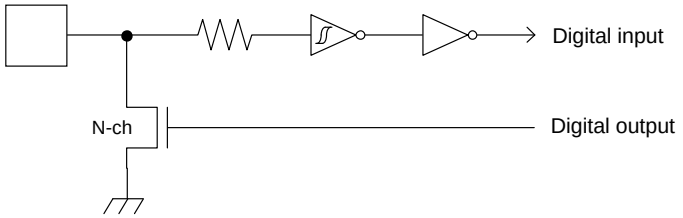
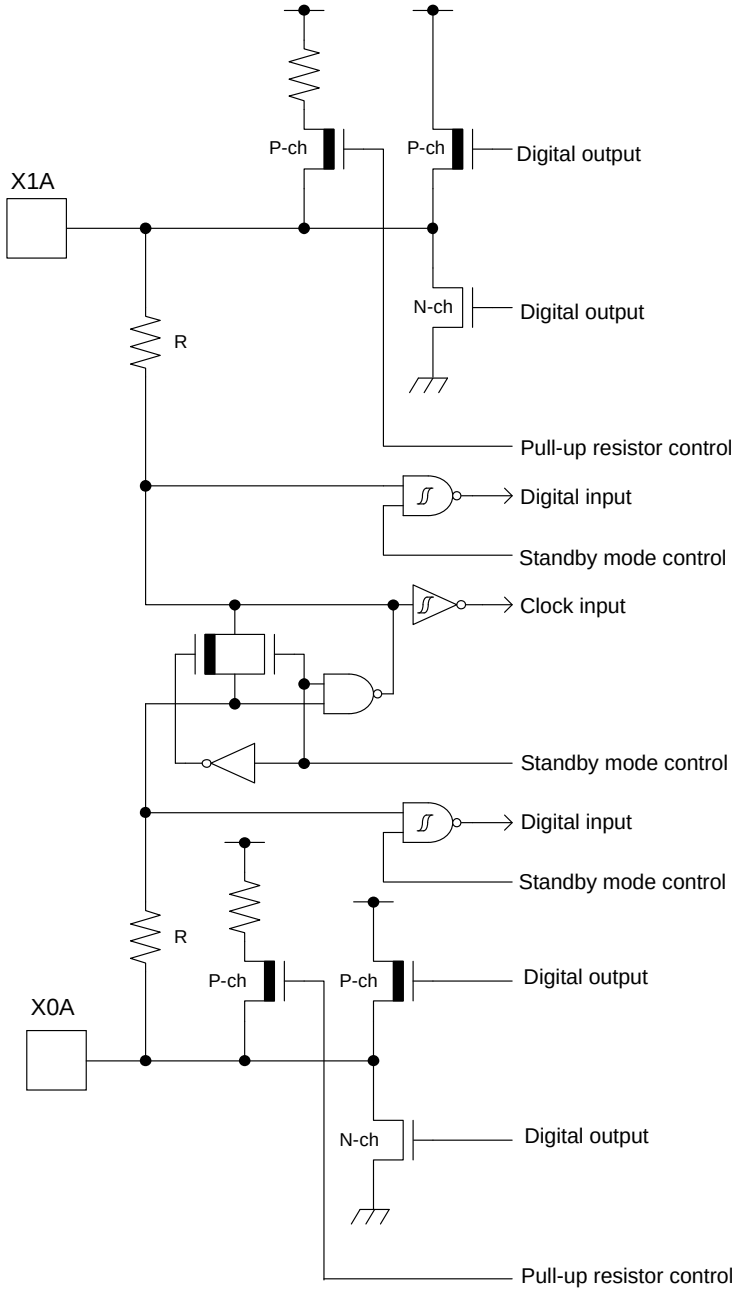
Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
LCDC	SEG00	LCD segment output pin	95	73	B4	75	B4	59
	SEG01		94	72	C5	74	C5	58
	SEG02		93	71	D6	73	B5	-
	SEG03		91	69	A5	71	C6	-
	SEG04		90	68	C6	70	B6	-
	SEG05		86	64	C7	-	-	-
	SEG06		85	63	B7	-	-	-
	SEG07		84	62	A7	66	A8	-
	SEG08		83	61	D9	-	-	-
	SEG09		82	60	C8	-	-	-
	SEG10		74	52	C10	60	C10	-
	SEG11		73	51	C11	59	C11	48
	SEG12		72	50	E8	58	D9	47
	SEG13		71	49	D10	57	D10	46
	SEG14		69	47	E9	-	-	-
	SEG15		68	46	F8	-	-	-
	SEG16		67	45	E10	-	-	-
	SEG17		66	44	E11	56	E9	-
	SEG18		65	43	F9	55	E10	-
	SEG19		64	42	F10	54	E11	45
	SEG20		63	41	G8	53	F9	44
	SEG21		59	37	G9	49	F10	40
	SEG22		58	36	G10	48	G9	-
	SEG23		57	35	H7	47	G10	39
	SEG24		56	34	H9	46	H9	38
	SEG25		55	33	H10	45	H10	37
	SEG26		54	32	J8	44	J8	36
	SEG27		53	31	J10	43	J10	35
	SEG28		52	30	J11	42	J11	34
	SEG29		42	20	K7	32	L7	24
	SEG30		41	19	L7	31	J6	23
	SEG31		40	18	J6	30	K6	22
	SEG32		39	17	K6	29	J5	-
	SEG33		32	10	L6	22	K5	-
	SEG34		31	9	H5	21	L5	-
	SEG35		24	2	J2	19	J4	15
	SEG36		23	1	H3	18	J2	14
	SEG37		22	100	G4	17	J1	13
	SEG38		8	86	D5	8	E1	-
	SEG39		7	85	D3	7	D3	-

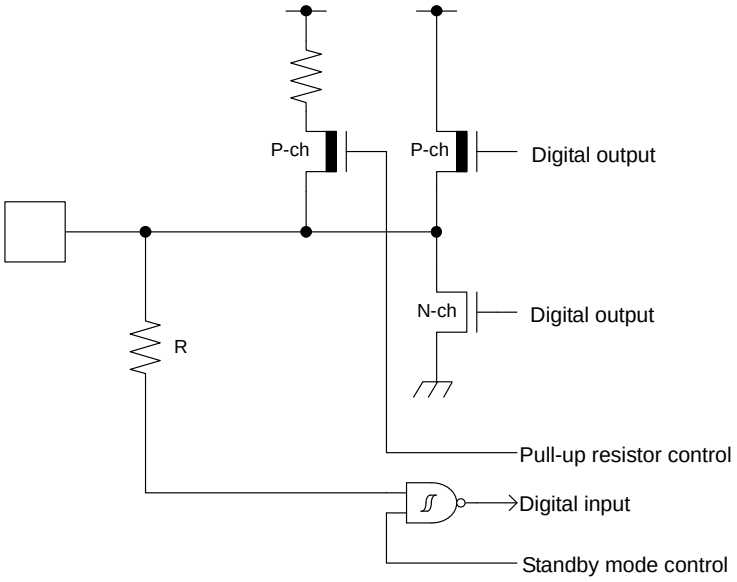
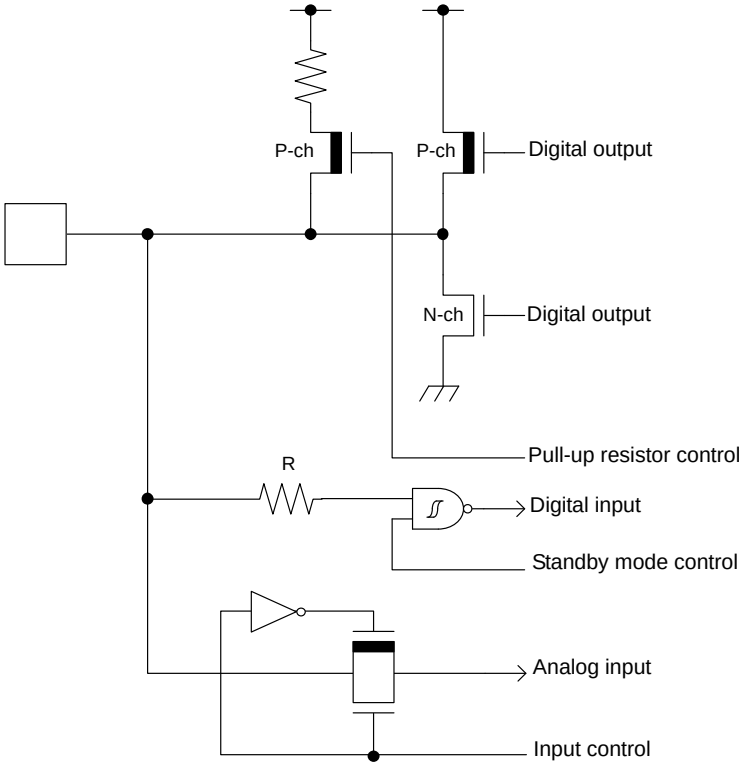
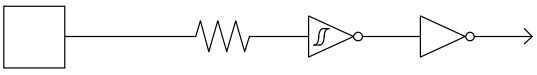
Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	38	16	K4	28	K4	21
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	47	25	L8	37	L8	29
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	46	24	K9	36	K9	28
POWER	VCC	Power supply Pin	1	79	B1	1	B1	1
	VCC	Power supply Pin	26	4	J1	-	-	-
	VCC	Power supply Pin	35	13	K1	25	K1	18
	VCC	Power supply Pin	51	29	K11	41	K11	33
	VCC	Power supply Pin	76	54	A10	-	-	-
	VCC	Power supply Pin	97	75	A4	77	A4	61
GND	VSS	GND Pin	-	-	-	-	F1	-
	VSS	GND Pin	-	-	-	-	F2	-
	VSS	GND Pin	-	-	-	-	F3	-
	VSS	GND Pin	-	-	B2	-	B2	-
	VSS	GND Pin	25	3	L1	20	L1	16
	VSS	GND Pin	-	-	K2	-	K2	-
	VSS	GND Pin	-	-	J3	-	J3	-
	VSS	GND Pin	-	-	H4	-	-	-
	VSS	GND Pin	-	-	-	-	L6	-
	VSS	GND Pin	34	12	L4	24	L4	-
	VSS	GND Pin	50	28	L11	40	L11	32
	VSS	GND Pin	-	-	K10	-	K10	-
	VSS	GND Pin	-	-	J9	-	J9	-
	VSS	GND Pin	-	-	H8	-	-	-
	VSS	GND Pin	-	-	B10	-	B10	-
	VSS	GND Pin	-	-	C9	-	C9	-
	VSS	GND Pin	-	-	-	-	D11	-
	VSS	GND Pin	75	53	A11	-	A11	-
	VSS	GND Pin	-	-	D8	-	-	-
	VSS	GND Pin	-	-	-	-	A7	-
	VSS	GND Pin	-	-	D4	-	-	-
	VSS	GND Pin	-	-	C3	-	C3	-
	VSS	GND Pin	-	-	-	-	A5	-
	VSS	GND Pin	100	78	A1	80	A1	64

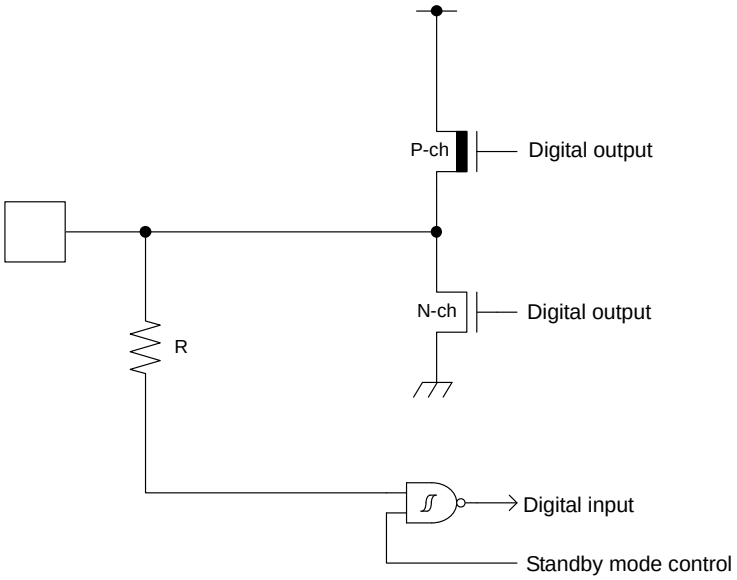
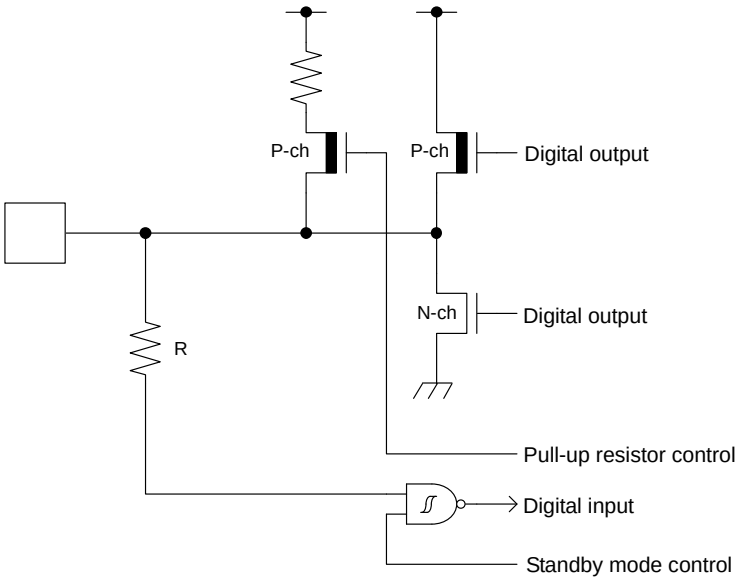
Pin function	Pin name	Function description	Pin No					
			LQFP-100	QFP-100	BGA-112	LQFP-80	BGA-96	LQFP/QFN-64
CLOCK	X0	Main clock (oscillation) input pin	48	26	L9	38	L9	30
	X0A	Sub clock (oscillation) input pin	36	14	L3	26	L3	19
	X1	Main clock (oscillation) I/O pin	49	27	L10	39	L10	31
	X1A	Sub clock (oscillation) I/O pin	37	15	K3	27	K3	20
	CROUT_0	Built-in high-speed CR-osc clock output port	74	52	C10	60	C10	-
	CROUT_1		92	70	B5	72	A6	57
ADC POWER	AVCC	A/D converter analog power supply pin	60	38	H11	50	H11	41
	AVRH	A/D converter analog reference voltage input pin	61	39	F11	51	F11	42
ADC GND	AVSS	A/D converter GND pin	62	40	G11	52	G11	43
C pin	C	Power supply stabilization capacity pin	33	11	L2	23	L2	17

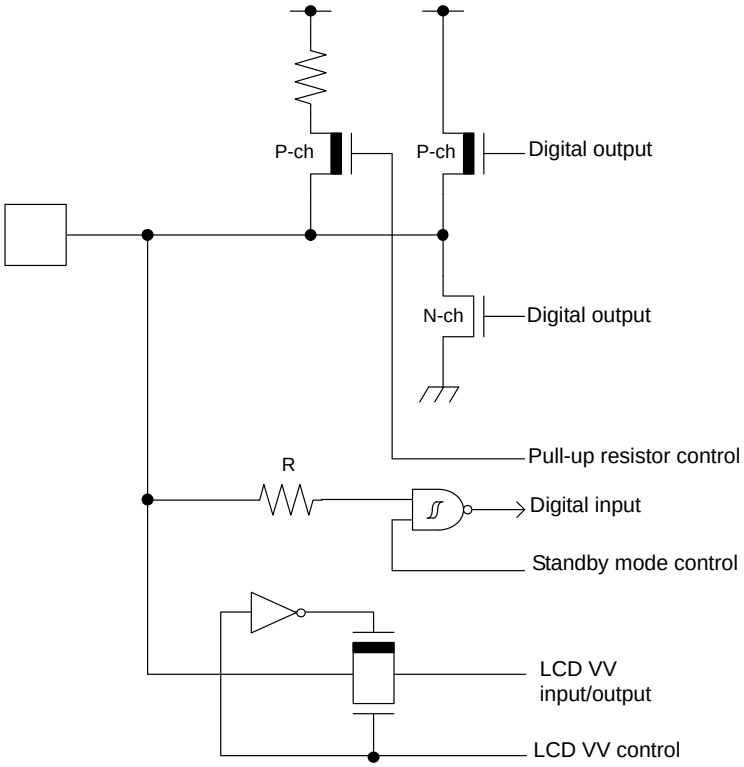
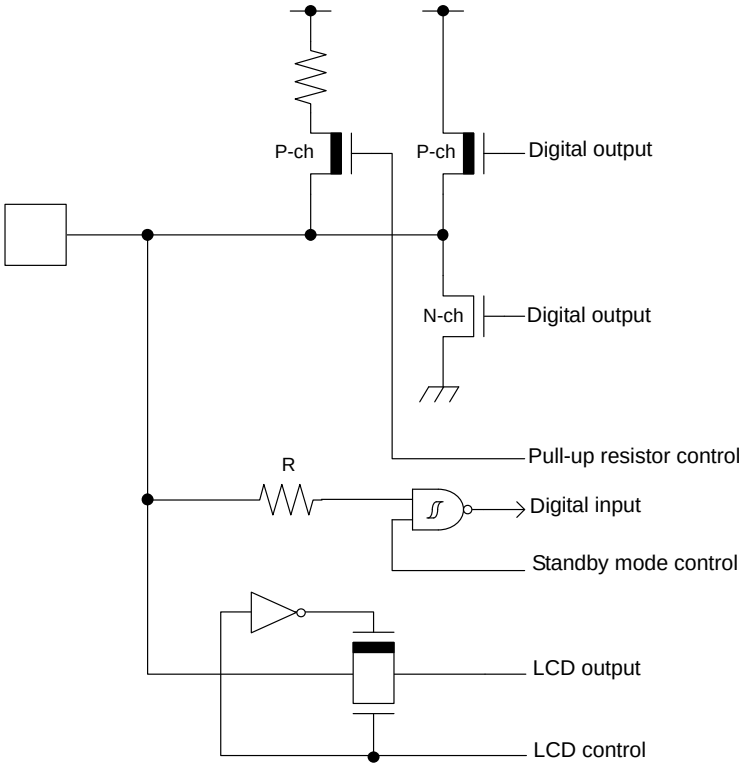
■ I/O CIRCUIT TYPE

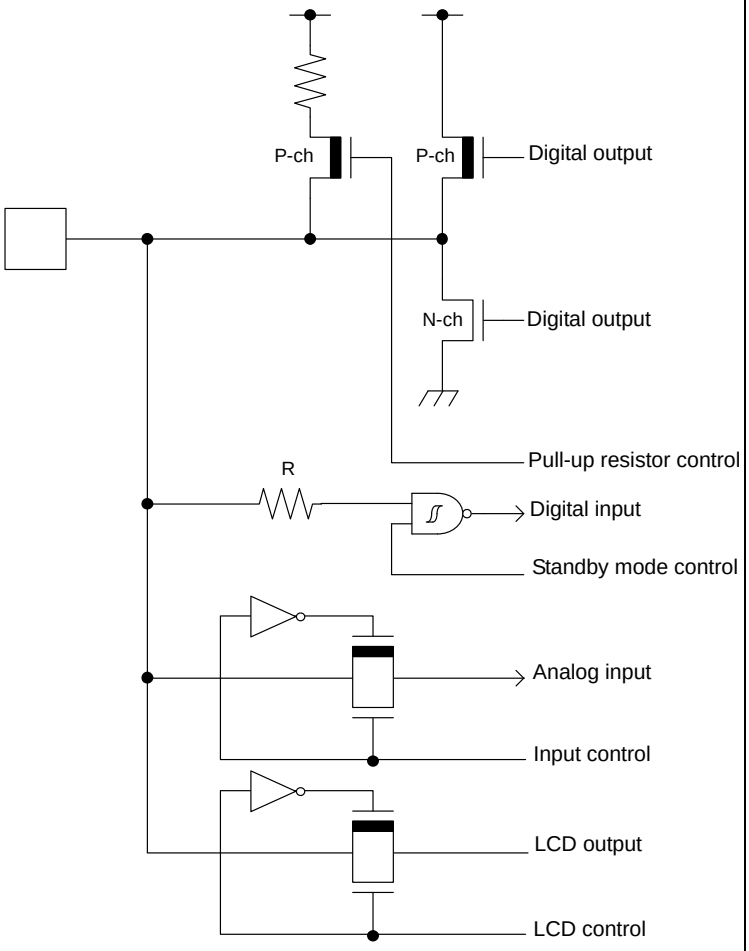
Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. ・ Oscillation feedback resistor : Approximately 1MΩ ・ With Standby mode control When the GPIO is selected. ・ CMOS level output. ・ CMOS level hysteresis input ・ With pull-up resistor control ・ With standby mode control ・ Pull-up resistor : Approximately 33kΩ ・ I_{OH}= -4mA, I_{OL}= 4mA
B		・ CMOS level hysteresis input ・ Pull-up resistor : Approximately 33kΩ

Type	Circuit	Remarks
C		・ Open drain output ・ CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. ・ Oscillation feedback resistor : Approximately 5MΩ ・ With Standby mode control When the GPIO is selected. ・ CMOS level output. ・ CMOS level hysteresis input ・ With pull-up resistor control ・ With standby mode control ・ Pull-up resistor : Approximately 33kΩ ・ I_{OH}= -4mA, I_{OL}= 4mA

Type	Circuit	Remarks
E		・CMOS level output ・CMOS level hysteresis input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・I_{OH}= -4mA, I_{OL}= 4mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
F		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・I_{OH}= -4mA, I_{OL}= 4mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
G		CMOS level hysteresis input

Type	Circuit	Remarks
H		・CMOS level output ・CMOS level hysteresis input ・With standby mode control ・I_{OH} = - 12.0mA, I_{OL} = 10.5mA
I		・CMOS level output ・CMOS level hysteresis input ・5V tolerant ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・I_{OH}= -4mA, I_{OL}= 4mA ・Available to control PZR registers. ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
J		・CMOS level output ・CMOS level hysteresis input ・With input control ・LCD-VV input/output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・I_{OH}= -4mA, I_{OL}= 4mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
K		・CMOS level output ・CMOS level hysteresis input ・With input control ・LCD output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・I_{OH}= -4mA, I_{OL}= 4mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
L		・CMOS level output ・CMOS level hysteresis input ・With input control ・Analog input ・LCD output ・With pull-up resistor control ・With standby mode control ・Pull-up resistor : Approximately 33kΩ ・I_{OH}= -4mA, I_{OL}= 4mA ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Code: DS00-00004-2Ea

- Observance of Safety Regulations and Standards

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

  FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- Lead-Free Packaging

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://edevice.fujitsu.com/fj/handling-e.pdf

■ HANDLING DEVICES

● Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin near this device.

● Stabilizing supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/µs when there is a momentary fluctuation on switching the power supply.

● Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

● Sub crystal oscillator

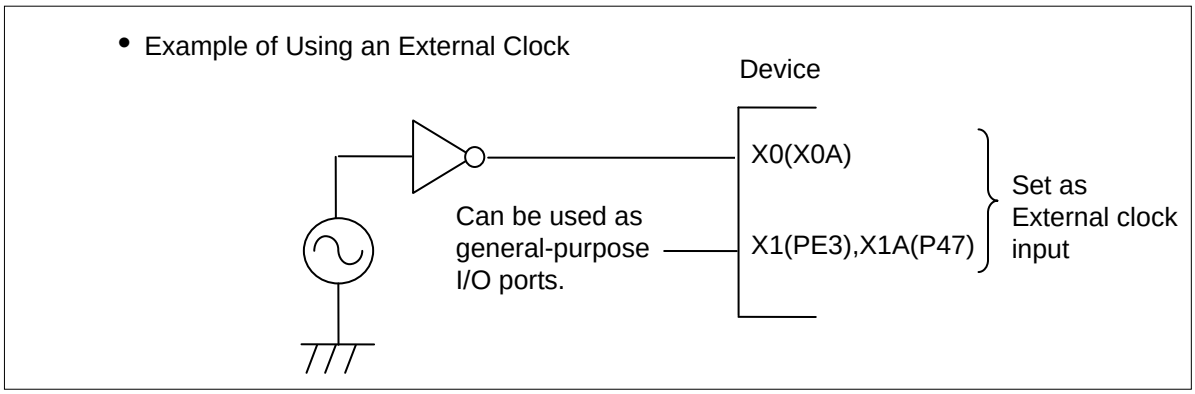
This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size : More than 3.2mm × 1.5mm
  - Load capacitance : Approximately 6pF to 7pF

- Lead type
  - Load capacitance : Approximately 6pF to 7pF

- Using an external clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

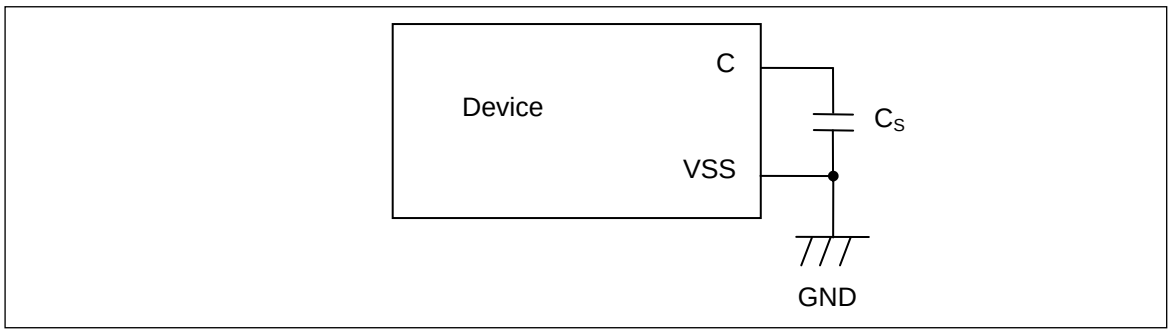


- Handling when using Multi-function serial pin as I^2C pin

If it is using the multi-function serial pin as I^2C pins, P-ch transistor of digital output is always disabled. However, I^2C pins need to keep the electrical characteristic like other pins and not to connect to the external I^2C bus system with power OFF.

- C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.A smoothing capacitor of about 4.7µF would be recommended for this series.



- Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on

  Turn power-on/off in the following order or at the same time.
  If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

  Turning on : VCC →AVCC → AVRH

  Turning off : AVRH → AVCC → VCC

- Serial Communication

  There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
  Therefore, design a printed circuit board so as to avoid noise.
  Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

- Differences in features among the products with different memory sizes and between Flash memory products and MASK products

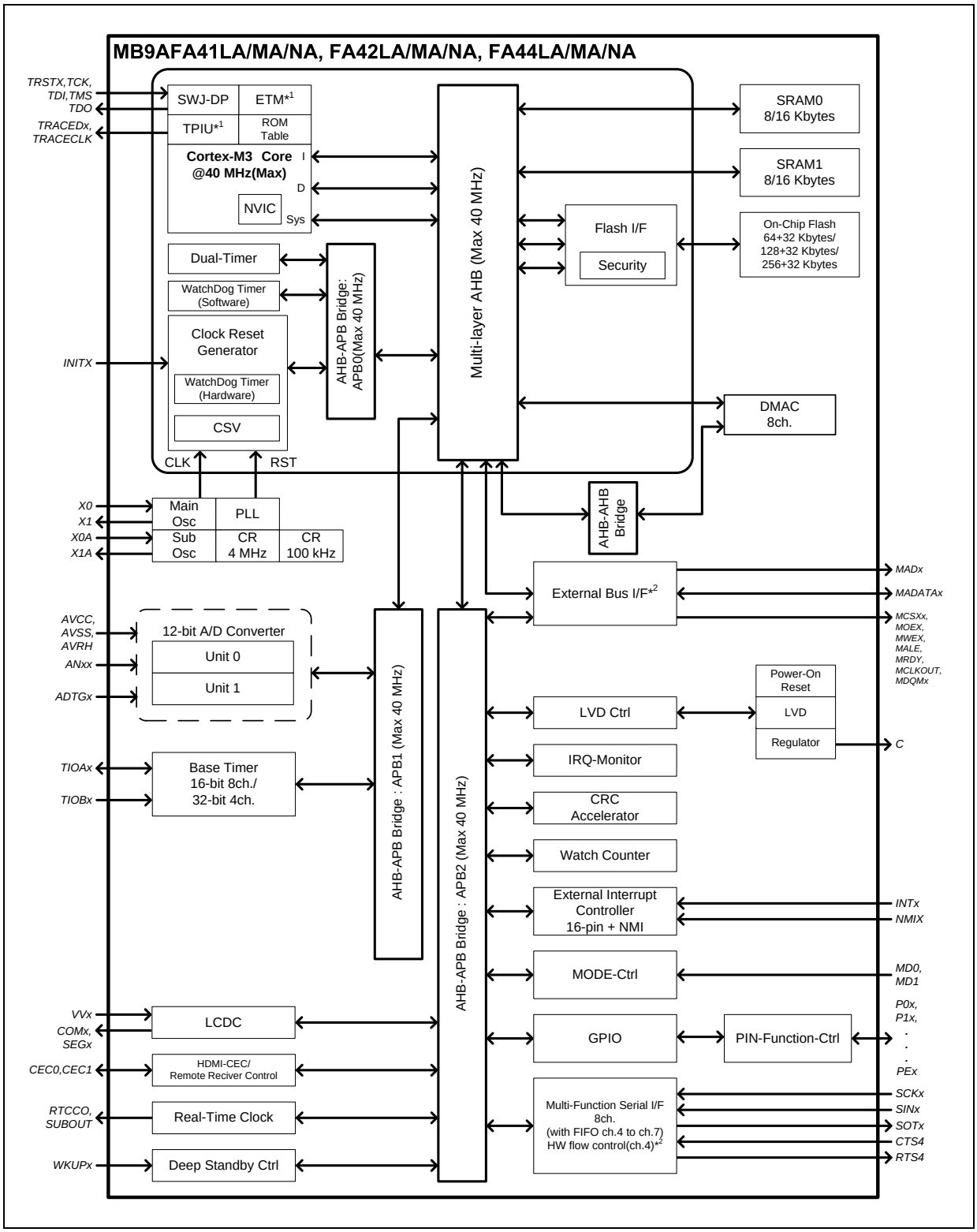
  The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

  If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

- Pull-Up function of 5V tolerant I/O

  Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

■ BLOCK DIAGRAM



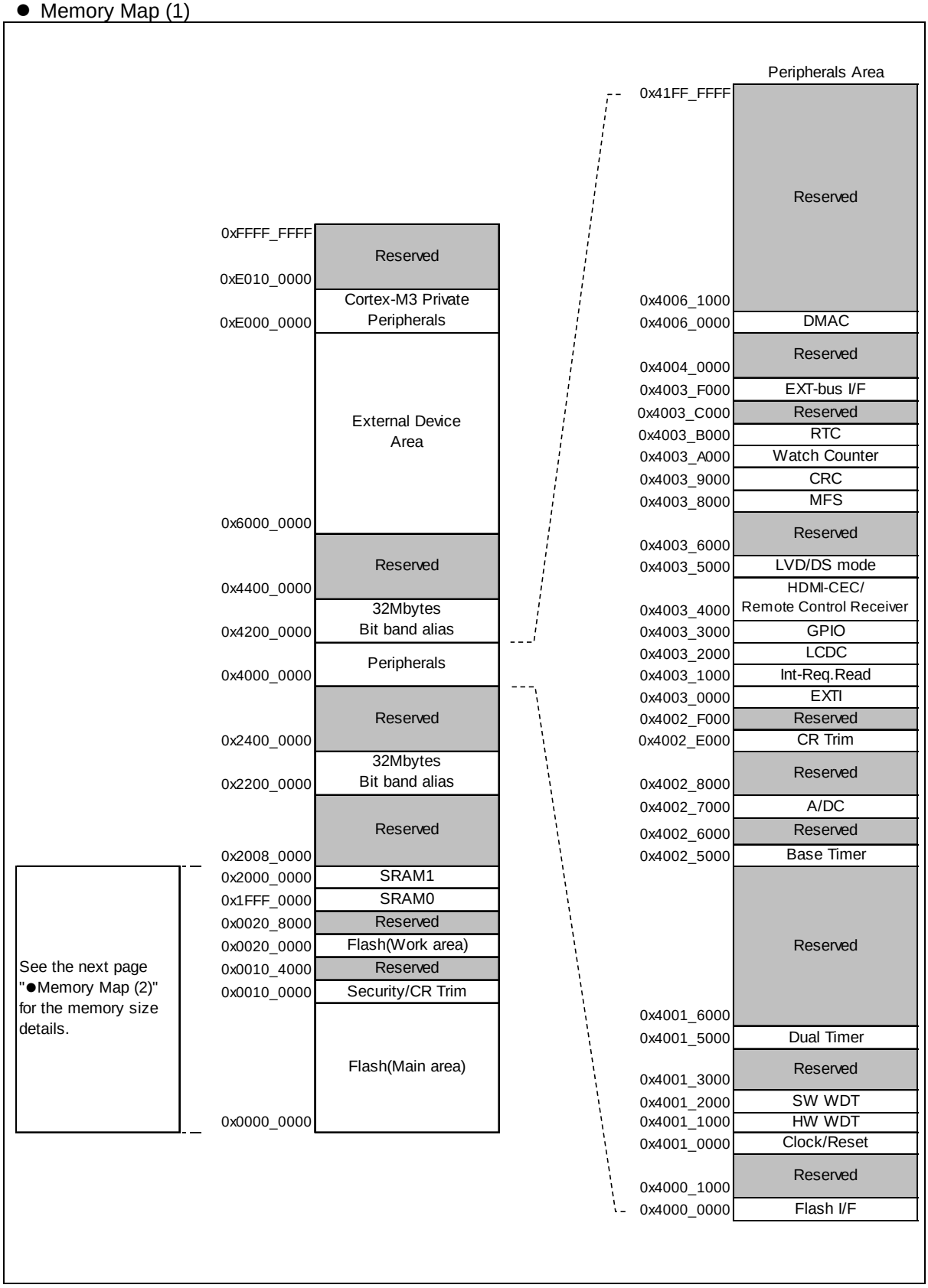
*1: For the MB9AFA41LA/MA, MB9AFA42LA/MA, and MB9AFA44LA/MA, ETM is not available.
*2: For the MB9AFA41LA, MB9AFA42LA and MB9AFA44LA, the External Bus Interface is not available. And the Multi-function Serial Interface does not support hardware flow control in these products.

■ MEMORY SIZE

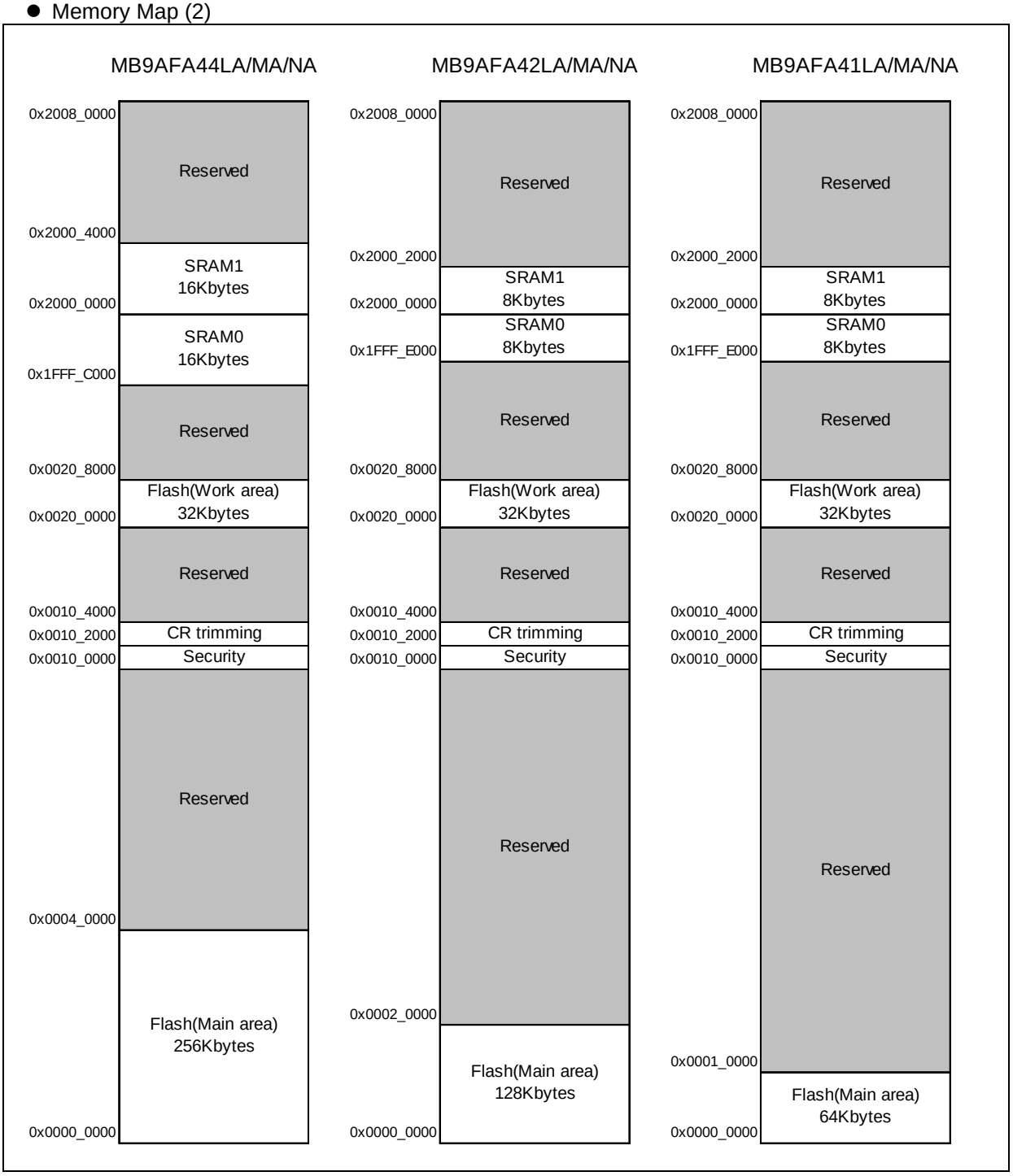
See " • Memory size" in "■PRODUCT LINEUP" to confirm the memory size.

■ MEMORY MAP

● Memory Map (1)



- Memory Map (2)



Refer to the programming manual for the detail of Flash main area.

・MB9AB40N/A40N/340N/140N/150R,MB9B520M/320M/120M Series Flash Programming Manual

- Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_4FFF	APB1	Reserved
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		LCDC
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/Remote control Receiver
0x4003_5000	0x4003_57FF		Low-Voltage Detector
0x4003_5800	0x4003_5FFF		Deep stand-by mode Controller
0x4003_6000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4005_FFFF	AHB	Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x41FF_FFFF		Reserved

■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- INITX=0
  This is the period when the INITX pin is the "L" level.
- INITX=1
  This is the period when the INITX pin is the "H" level.
- SPL=0
  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".
- SPL=1
  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".
- Input enabled
  Indicates that the input function can be used.
- Internal input fixed at "0"
  This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z
  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled
  Indicates that the setting is disabled.
- Maintain previous state
  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.
- Analog input is enabled
  Indicates that the analog input is enabled.
- Trace output
  Indicates that the trace function can be used.
- GPIO selected
  In Deep standby mode, pins switch to the general-purpose I/O port.

● List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or SLEEP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or SLEEP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL=1	-
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
G	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z/ Internal input fixed at "0"	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"	Maintain previous state/When oscillation stops*2, Hi-Z/ Internal input fixed at "0"
H	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or SLEEP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL=1	-
I	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
J	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
K	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or SLEEP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL=1	-
N	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									
O	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or SLEEP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL=1	-
Q	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"
	External interrupt enabled selected						Maintain previous state			
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									
R	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected Internal input fixed at "0"
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected									
S	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or SLEEP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL=1	-
T	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
U	Resource selected	Hi-Z	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"
	GPIO selected									
V	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"			Hi-Z / Internal input fixed at "0"			
	GPIO selected									
W	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"
	GPIO selected									
X	Resource selected	Hi-Z	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"
	GPIO selected									

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or SLEEP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL=1	-
Y	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"			Hi-Z / Internal input fixed at "0"			
	GPIO selected									

*1 : Oscillation is stopped at Sub timer mode, Low-Speed CR timer mode, RTC mode, STOP mode, Deep standby RTC mode, and Deep standby STOP mode.

*2 : Oscillation is stopped at STOP mode and Deep standby STOP mode.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog power supply voltage*1, *3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 4.6	V	
Analog reference voltage*1, *3	AVRH	V_{SS} - 0.5	V_{SS} + 4.6	V	
LCD input voltage *1, *3	VV0 to VV4	V_{SS} - 0.5	V_{SS} + 4.6	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 4.6V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 4.6V)	V	
"L" level maximum output current*4	I_{OL}	-	10	mA	
			39	mA	P81, P80 pins
"L" level average output current*5	I_{OLAV}	-	4	mA	
			10.5	mA	P81, P80 pins
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*4	I_{OH}	-	- 10	mA	
			- 39	mA	P81, P80 pins
"H" level average output current*5	I_{OHAV}	-	- 4	mA	
			- 12	mA	P81, P80 pins
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	300	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1 : These parameters are based on the condition that $V_{SS} = AV_{SS} = 0V$.
*2 : V_{CC} must not drop below V_{SS} - 0.5V.
*3 : Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.
*4 : The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
*5 : The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.
*6 : The total average output current is defined as the average current value flowing through all of corresponding pins for a 100ms.

<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	-	1.65	3.6	V	*1
			2.2	3.6		*2
LCD input voltage	VV4	-	2.2	V_{CC}	V	
Analog power supply voltage	AV_{CC}	-	1.65	3.6	V	AV_{CC} = V_{CC}
Analog reference voltage	AVRH	-	2.7	AV_{CC}	V	$AV_{CC} \geq 2.7V$
			AV_{CC}	AV_{CC}	V	AV_{CC}<2.7V
Smoothing capacitor	C_S	-	1	10	µF	For Regulator*3
Operating temperature	Ta	-	- 40	+ 85	°C	

*1: When LCD Controller is not used.
*2: When LCD Controller is used.
*3: See "•C Pin" in "■HANDLING DEVICES" for the connection of the smoothing capacitor.

<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

3. DC Characteristics

(1) Current Rating

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	-	15.5	21	mA	CPU : 40 MHz, Peripheral : 40 MHz, *1
				-	8.7	12	mA	CPU : 40 MHz, Peripheral : the clock stops NOP operation *1
			Normal operation (built-in high-speed CR)	-	1.8	2.9	mA	CPU/ Peripheral : 4 MHz*2 *1
			Normal operation (sub oscillation)	-	110	680	µA	CPU/ Peripheral : 32 kHz *1
			Normal operation (built-in low-speed CR)	-	125	700	µA	CPU/ Peripheral : 100 kHz *1
	I_{CCS}		SLEEP operation (PLL)	-	9	12.5	mA	Peripheral : 40 MHz *1
			SLEEP operation (built-in high-speed CR)	-	0.8	1.6	mA	Peripheral : 4 MHz*2 *1
			SLEEP operation (sub oscillation)	-	96	670	µA	Peripheral : 32 kHz *1
			SLEEP operation (built-in low-speed CR)	-	110	680	µA	Peripheral : 100 kHz *1
	I_{CCH}		STOP mode	-	9	28	µA	Ta = + 25°C, When LVD is off *1
				-	-	270	µA	Ta = + 85°C, When LVD is off *1
	I_{CCT}		TIMER mode (sub oscillation)	-	12	35	mA	Ta = + 25°C, When LVD is off *1
				-	-	330	mA	Ta = + 85°C, When LVD is off *1
	I_{CCR}		RTC mode (sub oscillation)	-	9.8	29	µA	Ta = + 25°C, When LVD is off *1
				-	-	280	µA	Ta = + 85°C, When LVD is off *1

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCHD}	VCC	Deep Standby STOP mode	-	1.25	7	µA	Ta = + 25°C, When LVD is off, RAM hold off *1, *3
					5.3	18	µA	Ta = + 25°C, When LVD is off, RAM hold on *1, *3
				-	-	70	µA	Ta = + 85°C, When LVD is off, RAM hold off *1, *3
						100	µA	Ta = + 85°C, When LVD is off, RAM hold on *1, *3
	I_{CCRD}		Deep Standby RTC mode (sub oscillation)	-	1.9	9	µA	Ta = + 25°C, When LVD is off, RAM hold off *1, *3
					5.9	20	µA	Ta = + 25°C, When LVD is off, RAM hold on *1, *3
				-	-	75	µA	Ta = + 85°C, When LVD is off, RAM hold off *1, *3
						105	µA	Ta = + 85°C, When LVD is off, RAM hold on *1, *3
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}		At operation	-	0.13	0.3	µA	For occurrence of reset
				-	0.13	0.3	µA	For occurrence of interrupt
Flash memory write/erase current	$I_{CCFLASH}$		At Write/Erase	-	9.5	11.2	mA	*4

*1: When all ports are fixed.
*2: When setting it to 4 MHz by trimming.
*3: RAM hold setting is on-chip SRAM only.
*4: The current at which to write or erase Flash memory, "$I_{CCFLASH}$" is added to "I_{CC}".

(2) Pin Characteristics

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
		5V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
			$V_{CC} < 2.7$ V	$V_{CC} \times 0.7$				
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	$V_{CC} \geq 2.7$ V	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
		5V tolerant input pin	$V_{CC} \geq 2.7$ V	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
			$V_{CC} < 2.7$ V			$V_{CC} \times 0.3$		
"H" level output voltage	V_{OH}	4mA type	$V_{CC} \geq 2.7$ V, I_{OH} = - 4mA	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 2mA	$V_{CC} - 0.45$				
		P80/P81	$V_{CC} \geq 2.7$ V, I_{OH} = - 12.0mA	$V_{CC} - 0.4$	-	V_{CC}	V	
			$V_{CC} < 2.7$ V, I_{OH} = - 6.5mA					
"L" level output voltage	V_{OL}	4mA type	$V_{CC} \geq 2.7$ V, I_{OL} = 4mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL} = 2mA					
		P80/P81	$V_{CC} \geq 2.7$ V, I_{OL} = 10.5mA	V_{SS}	-	0.4	V	
			$V_{CC} < 2.7$ V, I_{OL} = 5mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 2.7$ V	21	33	66	kΩ	
			$V_{CC} < 2.7$ V	-	-	134		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

4. LCD Characteristics

(V_{CC} = 2.2V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
VV0 to VV3 Output voltage (1/4 bias)	V_{VV0}	VV0	When using internal dividing resistor	0	-	V_{VV4} × 5%	V	
	V_{VV1}	VV1		V_{VV4} × 1/4 -10%	-	V_{VV4} × 1/4 +10%		
	V_{VV2}	VV2		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
	V_{VV3}	VV3		V_{VV4} × 3/4 -10%	-	V_{VV4} × 3/4 +10%		
VV0 to VV3 Output voltage (1/3 bias)	V_{VV0}	VV0	When using internal dividing resistor	0	-	V_{VV4} × 5%	V	
	V_{VV1}	VV1		V_{VV4} × 1/3 -10%	-	V_{VV4} × 1/3 +10%		
	V_{VV2}	VV2		V_{VV4} × 2/3 -10%	-	V_{VV4} × 2/3 +10%		
	V_{VV3}	VV3		V_{VV4} × 2/3 -10%	-	V_{VV4} × 2/3 +10%		
VV0 to VV3 Output voltage (1/2 bias)	V_{VV0}	VV0	When using internal dividing resistor	0	-	V_{VV4} × 5%	V	
	V_{VV1}	VV1		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
	V_{VV2}	VV2		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
	V_{VV3}	VV3		V_{VV4} × 1/2 -10%	-	V_{VV4} × 1/2 +10%		
VV4 Active current (1/4 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing resistor	-	10	20	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing resistor	-	100	160	µA	
VV4 Active current (1/3 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing resistor	-	12	30	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing resistor	-	120	180	µA	
VV4 Active current (1/2 bias)	I_{R100K}	VV4	When using 100 kΩ internal dividing resistor	-	18	40	µA	
	I_{R10K}	VV4	When using 10 kΩ internal dividing resistor	-	180	270	µA	
VV4 Static current	Ioff_vv4	VV4	When LCD stops	-	0.5	1.5	µA	
VV0 Output Voltage in using external resistor	V_{VV0E}	VV0	I_{OL}=1mA	-	-	0.66	V	

5. AC Characteristics

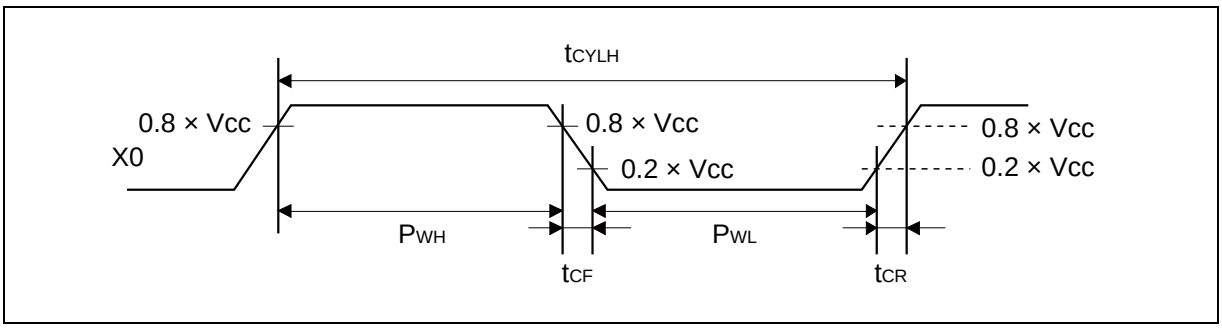
(1) Main Clock Input Characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	$V_{CC} \geq 2.7V$	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 2.7V$	4	20		
			-	4	48	MHz	When using external clock
Input clock cycle	t_{CYLH}		-	20.83	250	ns	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	40	MHz	Master clock
	F_{CC}	-	-	-	40	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	40	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	40	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	40	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	25	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	25	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	25	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

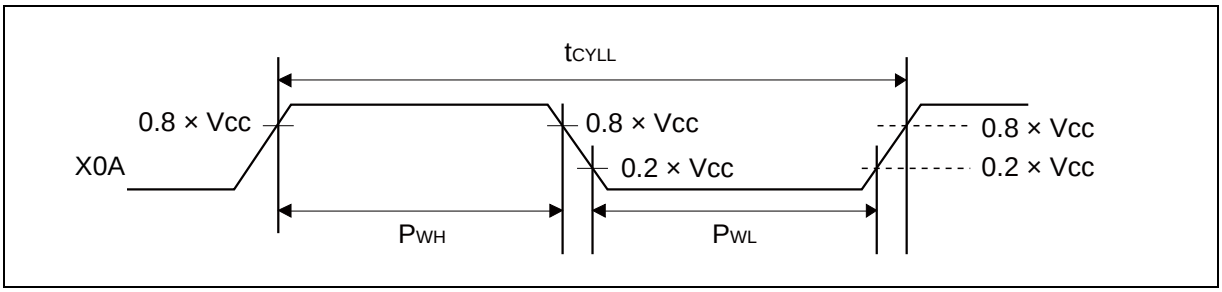
*2: For about each APB bus which each peripheral is connected to, see "■ BLOCK DIAGRAM" in this data sheet.



(2) Sub Clock Input Characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



(3) Built-in CR Oscillation Characteristics

・ Built-in high-speed CR

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRH}	Ta = + 25°C $V_{CC} \geq$ 2.7V	3.96	4	4.04	MHz	When trimming*1
		Ta = + 25°C V_{CC} < 2.7V	3.9	4	4.1		
		Ta = - 40°C to + 85°C	3.84	4	4.16		
		Ta = - 40°C to + 85°C	2.8	4	5.2		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.
*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value.
This period is able to use high-speed CR clock as source clock.

・ Built-in low-speed CR

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

(4-1) Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	75	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

(4-2) Operating Conditions of Main PLL (In the case of using the built-in high-speed CR for the input clock of the main PLL)

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.8	4	4.2	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	F_{PLLO}	72	-	150	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	40	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

Note: Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency has been trimmed.

(5) Reset Input Characteristics

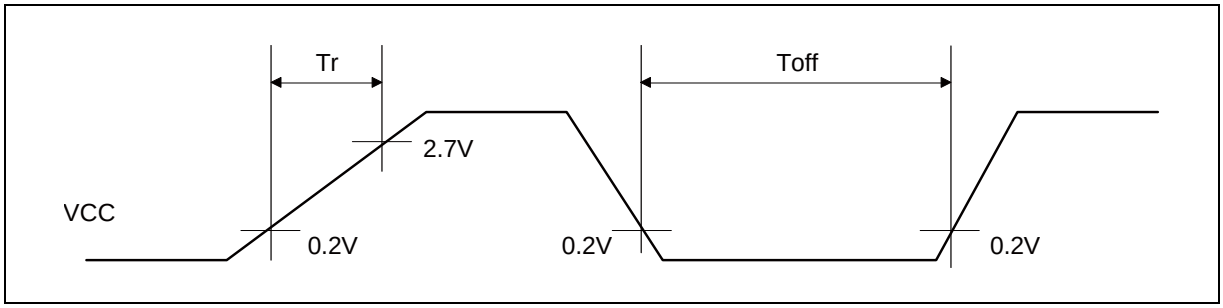
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

(6) Power-on Reset Timing

(V_{CC}= 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	VCC	0	-	ms	
Power supply shut down time	Toff		1	-	ms	



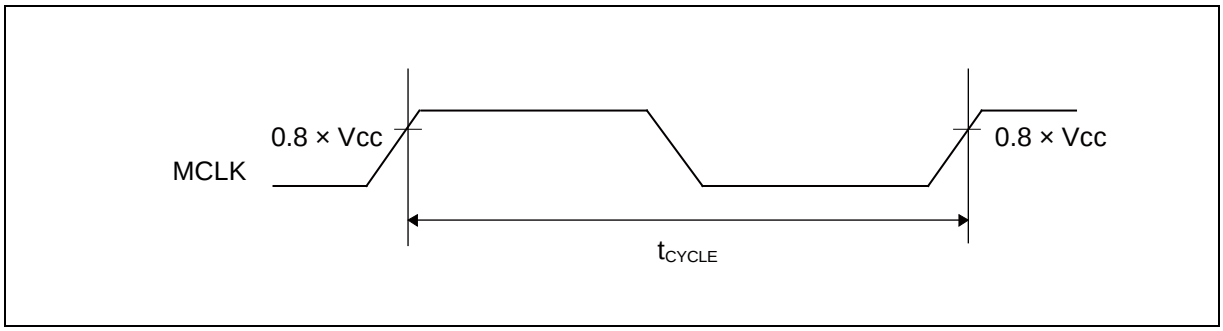
(7) External Bus Timing

・ External bus clock output characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{CYCLE}	MCLKOUT*	$V_{CC} \geq 2.7$ V	-	40	MHz
			$V_{CC} < 2.7$ V	-	20	MHz

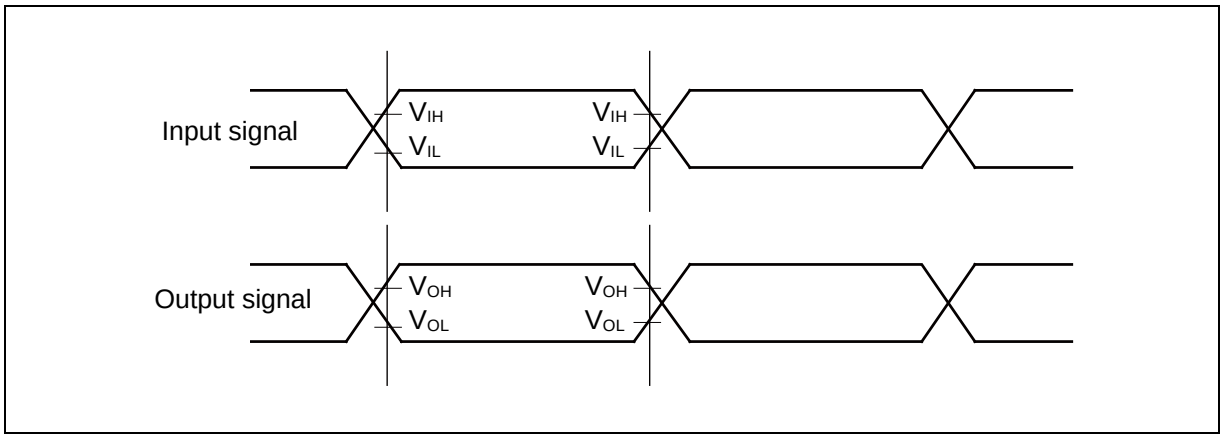
*: The external bus clock output (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see "Chapter: External Bus Interface" in "FM3 Family PERIPHERAL MANUAL".



・ External bus signal input/output characteristics

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	

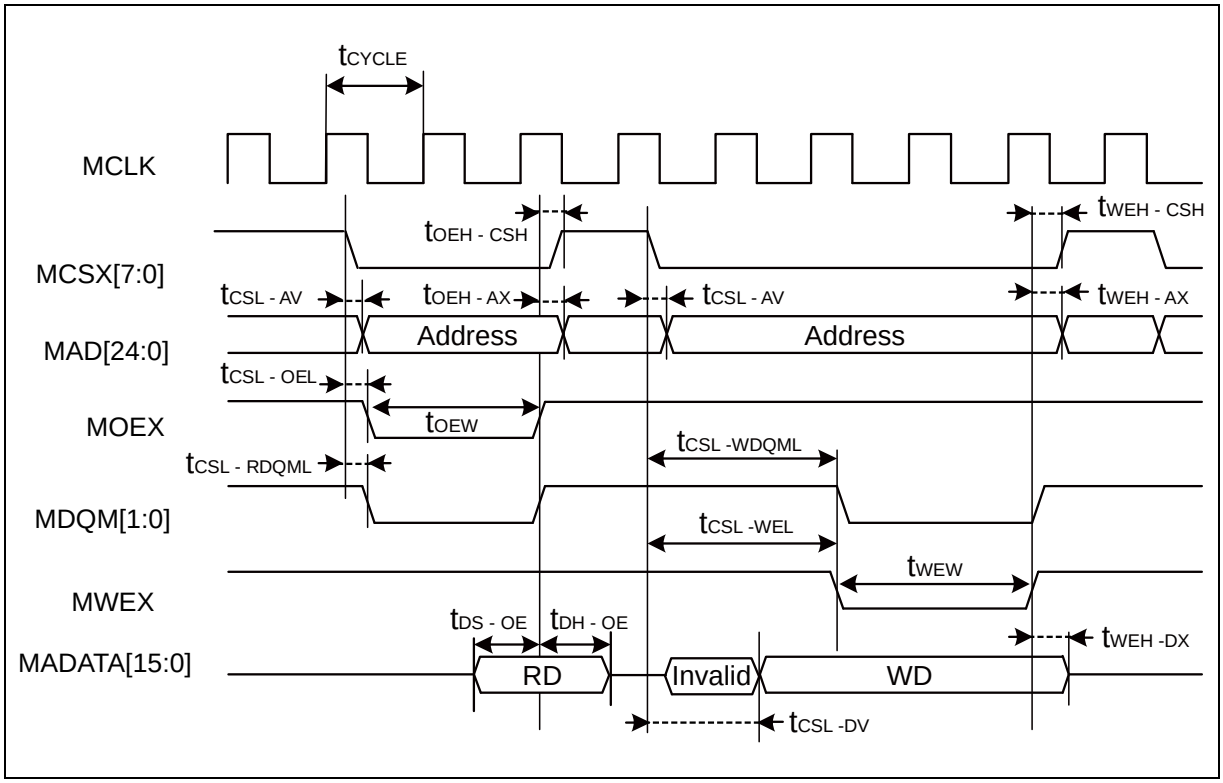


- Separate Bus Access Asynchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MOEX Min pulse width	t_{OEW}	MOEX	$V_{CC} \geq 2.7V$	MCLK×n-3	-	ns
			$V_{CC} < 2.7V$			
MCSX ↓ → Address output delay time	$t_{CSL - AV}$	MCSX[7:0], MAD[24:0]	$V_{CC} \geq 2.7V$	-9	+9	ns
			$V_{CC} < 2.7V$	-12	+12	
MOEX ↑ → Address hold time	$t_{OEH - AX}$	MOEX, MAD[24:0]	$V_{CC} \geq 2.7V$	0	MCLK×m+9	ns
			$V_{CC} < 2.7V$		MCLK×m+12	
MCSX ↓ → MOEX ↓ delay time	$t_{CSL - OEL}$	MOEX, MCSX[7:0]	$V_{CC} \geq 2.7V$	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7V$	MCLK×m-12	MCLK×m+12	
MOEX ↑ → MCSX ↑ time	$t_{OEH - CSH}$		$V_{CC} \geq 2.7V$	0	MCLK×m+9	ns
			$V_{CC} < 2.7V$		MCLK×m+12	
MCSX ↓ → MDQM ↓ delay time	$t_{CSL - RDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 2.7V$	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 2.7V$	MCLK×m-12	MCLK×m+12	
Data set up → MOEX ↑ time	$t_{DS - OE}$	MOEX, MADATA[15:0]	$V_{CC} \geq 2.7V$	30	-	ns
			$V_{CC} < 2.7V$	38	-	
MOEX ↑ → Data hold time	$t_{DH - OE}$	MOEX, MADATA[15:0]	$V_{CC} \geq 2.7V$	0	-	ns
			$V_{CC} < 2.7V$			
MWEX Min pulse width	t_{WEW}	MWEX	$V_{CC} \geq 2.7V$	MCLK×n-3	-	ns
			$V_{CC} < 2.7V$			
MWEX ↑ → Address output delay time	$t_{WEH - AX}$	MWEX, MAD[24:0]	$V_{CC} \geq 2.7V$	0	MCLK×m+9	ns
			$V_{CC} < 2.7V$		MCLK×m+12	
MCSX ↓ → MWEX ↓ delay time	$t_{CSL - WEL}$	MWEX, MCSX[7:0]	$V_{CC} \geq 2.7V$	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 2.7V$	MCLK×n-12	MCLK×n+12	
MWEX ↑ → MCSX ↑ delay time	$t_{WEH - CSH}$		$V_{CC} \geq 2.7V$	0	MCLK×m+9	ns
			$V_{CC} < 2.7V$		MCLK×m+12	
MCSX ↓→ MDQM ↓ delay time	$t_{CSL-WDQML}$	MCSX, MDQM[1:0]	$V_{CC} \geq 2.7V$	MCLK×n-9	MCLK×n+9	ns
			$V_{CC} < 2.7V$	MCLK×n-12	MCLK×n+12	
MWEX ↓→ Data output time	$t_{CSL - DV}$	MCSX, MADATA[15:0]	$V_{CC} \geq 2.7V$	MCLK-9	MCLK+9	ns
			$V_{CC} < 2.7V$	MCLK-12	MCLK+12	
MWEX ↑ → Data hold time	$t_{WEH - DX}$	MWEX, MADATA[15:0]	$V_{CC} \geq 2.7V$	0	MCLK×m+9	ns
			$V_{CC} < 2.7V$		MCLK×m+12	

Note: When the external load capacitance C_L = 30pF (m = 0 to 15, n = 1 to 16).

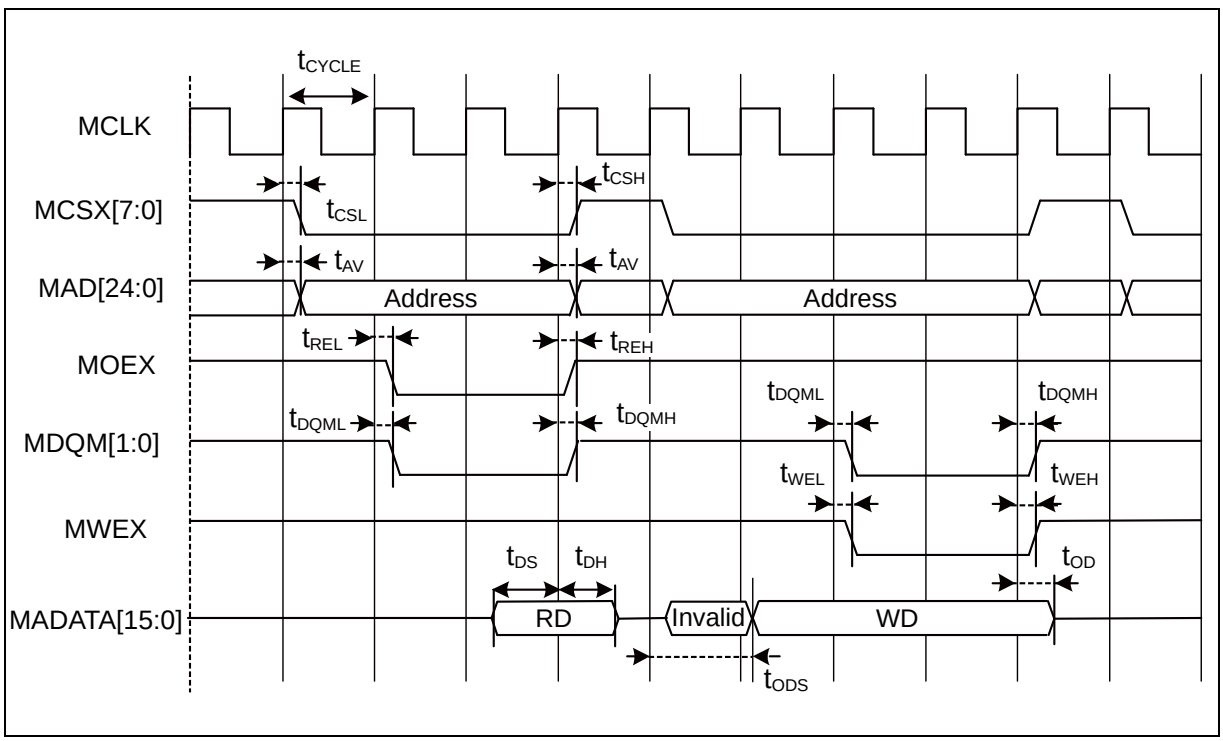

tCYCLE
MCLK
tOEH - CSH
tWEH - CSH
MCSX[7:0]
tCSL - AV
tOEH - AX
tCSL - AV
tWEH - AX
MAD[24:0]
Address
Address
tCSL - OEL
tOEW
MOEX
tCSL -WDQML
tCSL - RDQML
MDQM[1:0]
tCSL -WEL
tWEW
MWEX
tDS - OE
tDH - OE
tWEH -DX
MADATA[15:0]
RD
Invalid
WD
tCSL -DV

- Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Address delay time	t_{AV}	MCLK, MAD[24:0]	$V_{CC} \geq 2.7V$	1	12	ns
			$V_{CC} < 2.7V$		13	
MCSX delay time	t_{CSL}	MCLK, MCSX[7:0]	$V_{CC} \geq 2.7V$	1	12	ns
			$V_{CC} < 2.7V$			
	t_{CSH}		$V_{CC} \geq 2.7V$	1	9	ns
			$V_{CC} < 2.7V$		12	
MOEX delay time	t_{REL}	MCLK, MOEX	$V_{CC} \geq 2.7V$	1	9	ns
			$V_{CC} < 2.7V$		12	
	t_{REH}		$V_{CC} \geq 2.7V$	1	9	ns
			$V_{CC} < 2.7V$		12	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7V$	24	-	ns
			$V_{CC} < 2.7V$	37		
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7V$	0	-	ns
			$V_{CC} < 2.7V$			
MWEX delay time	t_{WEL}	MCLK, MWEX	$V_{CC} \geq 2.7V$	1	9	ns
			$V_{CC} < 2.7V$		12	
	t_{WEH}		$V_{CC} \geq 2.7V$	1	9	ns
			$V_{CC} < 2.7V$		12	
MDQM[1:0] delay time	t_{DQML}	MCLK, MDQM[1:0]	$V_{CC} \geq 2.7V$	1	9	ns
			$V_{CC} < 2.7V$		12	
	t_{DQMH}		$V_{CC} \geq 2.7V$	1	9	ns
			$V_{CC} < 2.7V$		12	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7V$	MCLK + 1	MCLK + 18	ns
			V_{CC}<2.7V		MCLK + 24	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7V$	1	18	ns
			$V_{CC} < 2.7V$		24	

Note: When the external load capacitance C_L = 30pF.

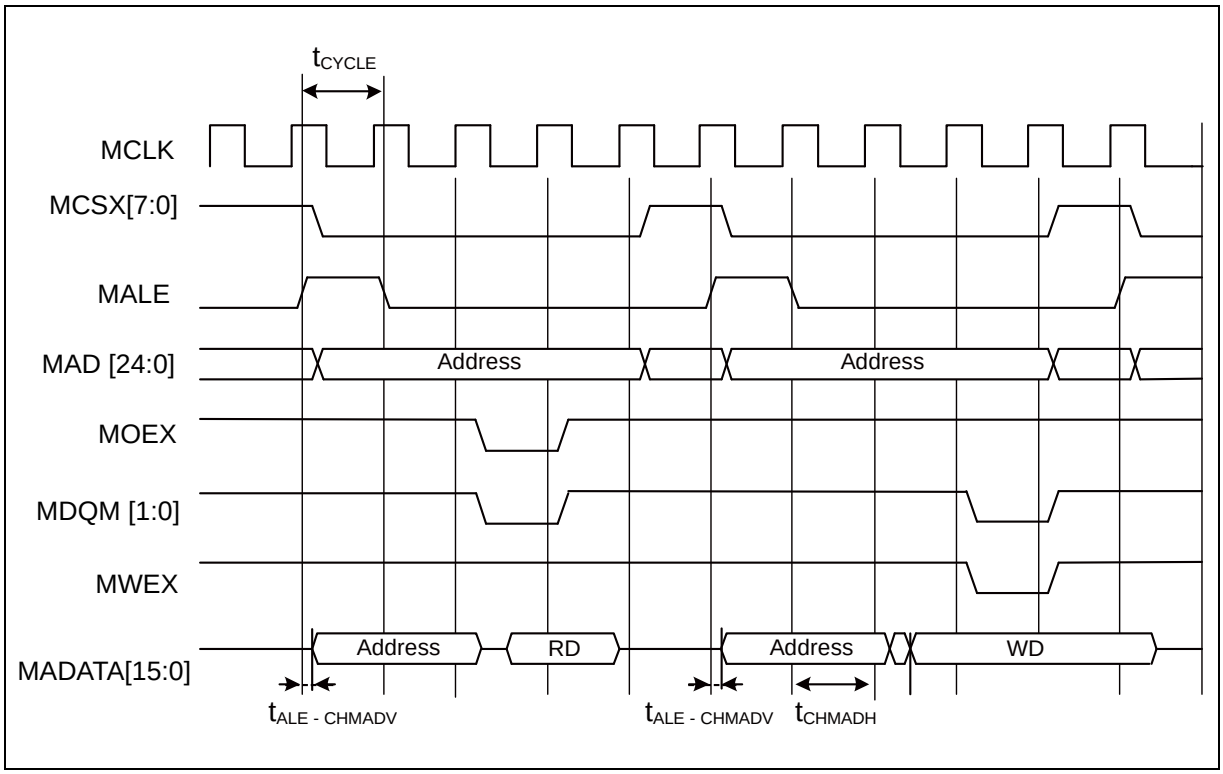


- Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MADATA[15:0]	$V_{CC} \geq 2.7V$	- 2	+ 10	ns
			$V_{CC} < 2.7V$		+ 20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 2.7V$	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 2.7V$	MCLK×n+0	MCLK×n+20	

Note: When the external load capacitance C_L = 30pF (m = 0 to 15, n = 1 to 16).

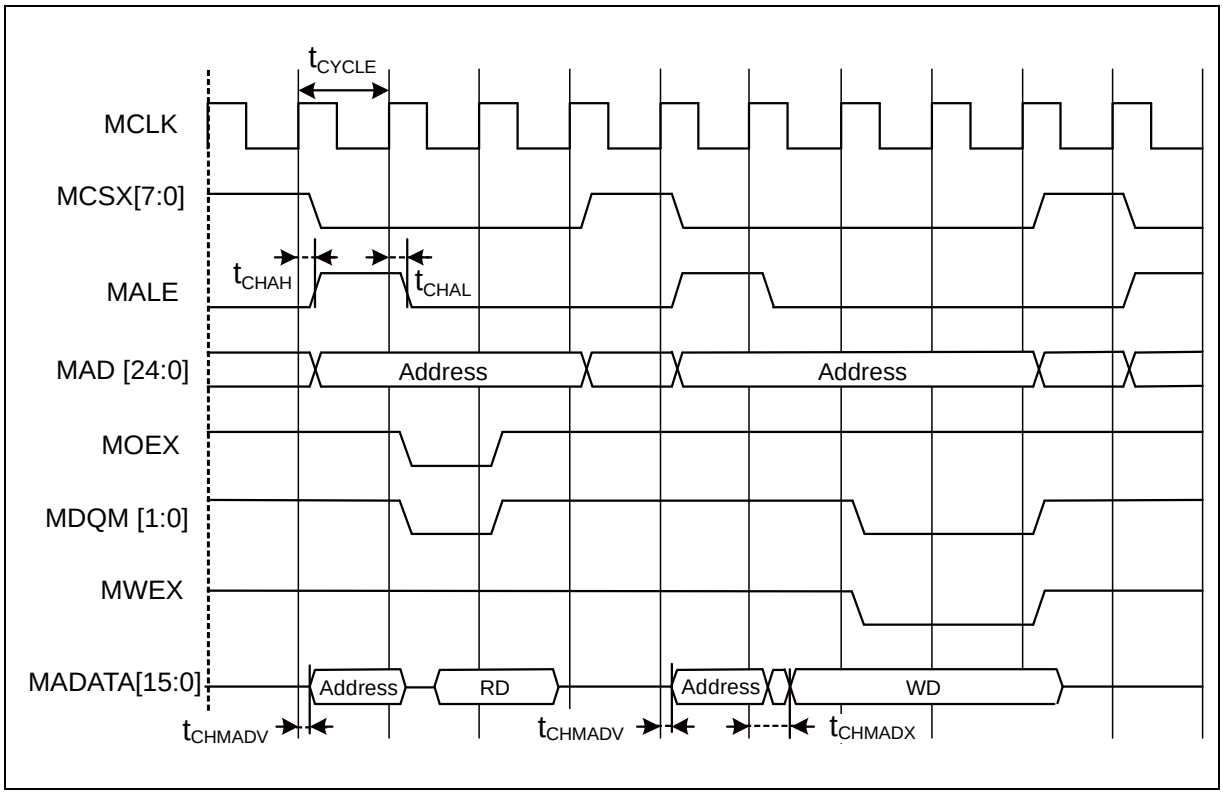


- Multiplexed Bus Access Synchronous SRAM Mode

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MALE delay time	t_{CHAL}	MCLK, ALE	$V_{CC} \geq 2.7V$	1	9	ns	
			$V_{CC} < 2.7V$		12	ns	
	t_{CHAH}		$V_{CC} \geq 2.7V$	1	9	ns	
			$V_{CC} < 2.7V$		12	ns	
MCLK ↑ → Multiplexed Address delay time	t_{CHMADV}	MCLK, MADATA[15:0]	$V_{CC} \geq 2.7V$	1	t_{OD}	ns	
			$V_{CC} < 2.7V$				
MCLK ↑ → Multiplexed Data output time	t_{CHMADX}		$V_{CC} \geq 2.7V$	1	t_{OD}	ns	
			$V_{CC} < 2.7V$				

Note: When the external load capacitance C_L = 30pF.

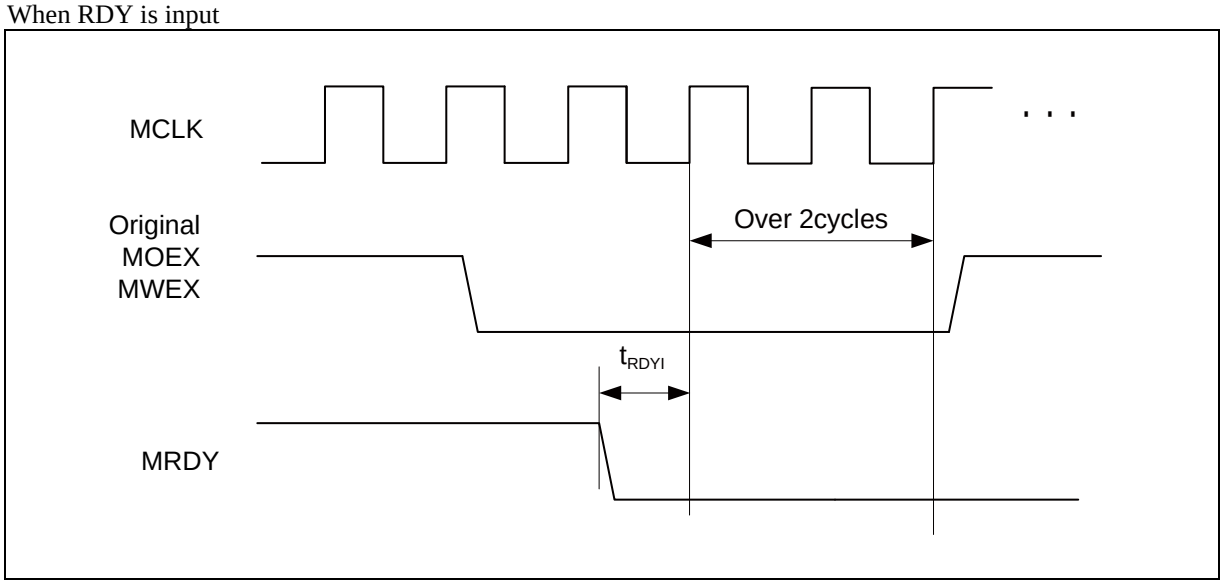


- External Ready Input Timing

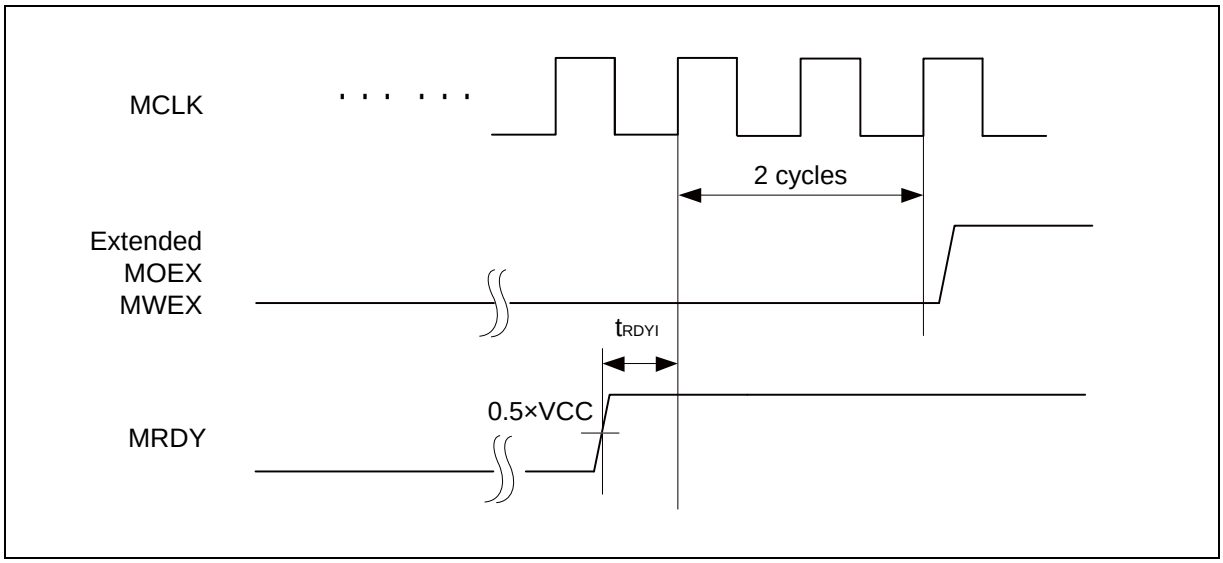
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK ↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	$V_{CC} \geq 2.7V$	23	-	ns	
			$V_{CC} < 2.7V$	37			

When RDY is input



When RDY is released

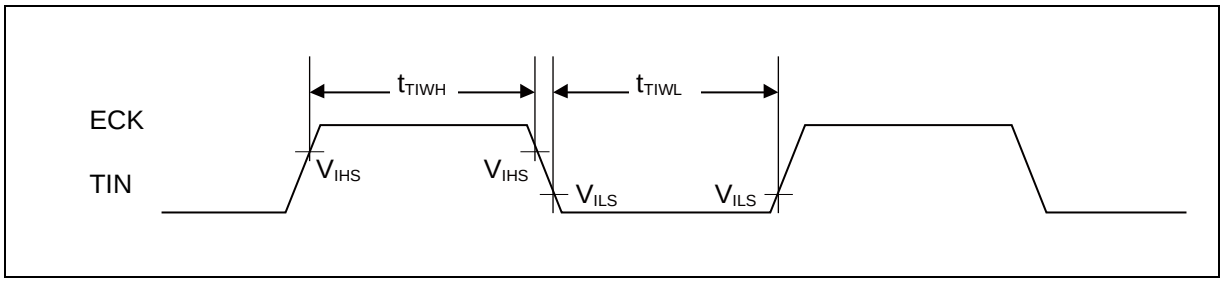


(8) Base Timer Input Timing

- Timer input timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

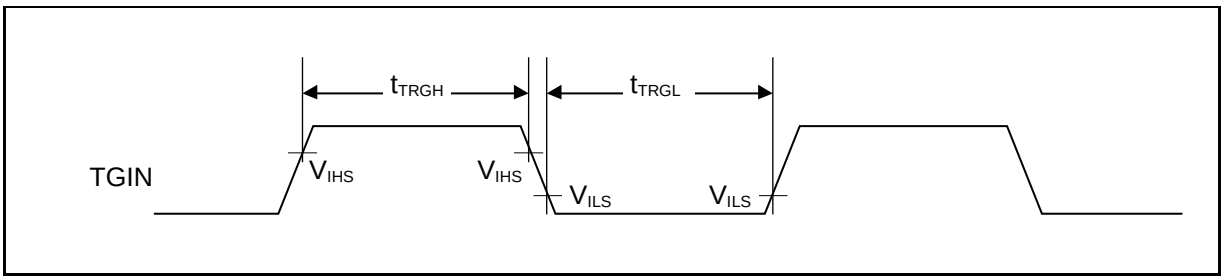
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



- Trigger input timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note: t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which the Base Timer is connected to, see "■BLOCK DIAGRAM" in this data sheet.

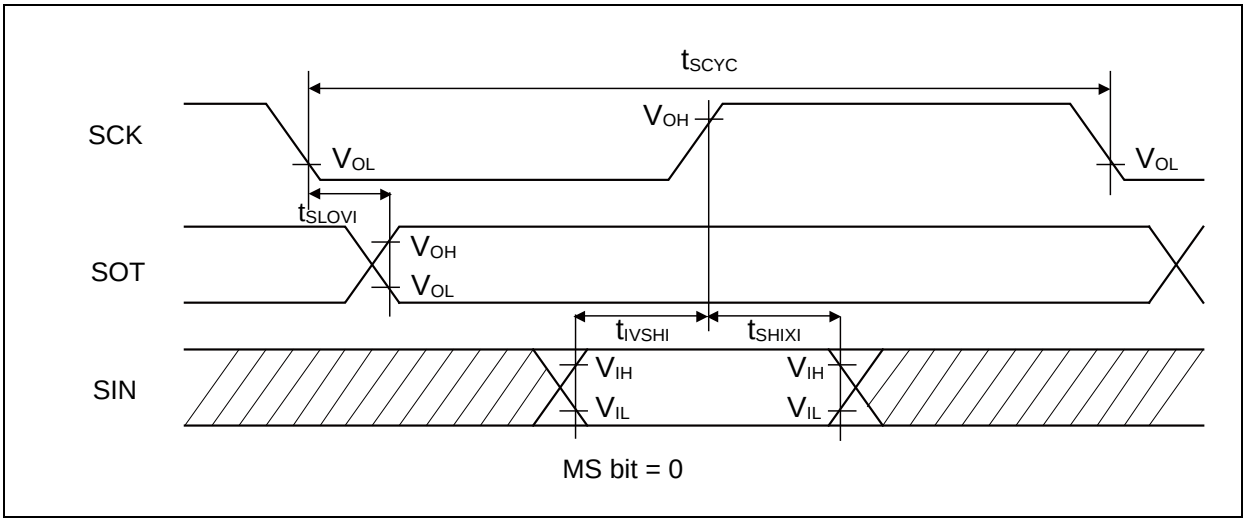
(9) CSIO Timing

- Synchronous serial (SPI = 0, SCINV = 0)

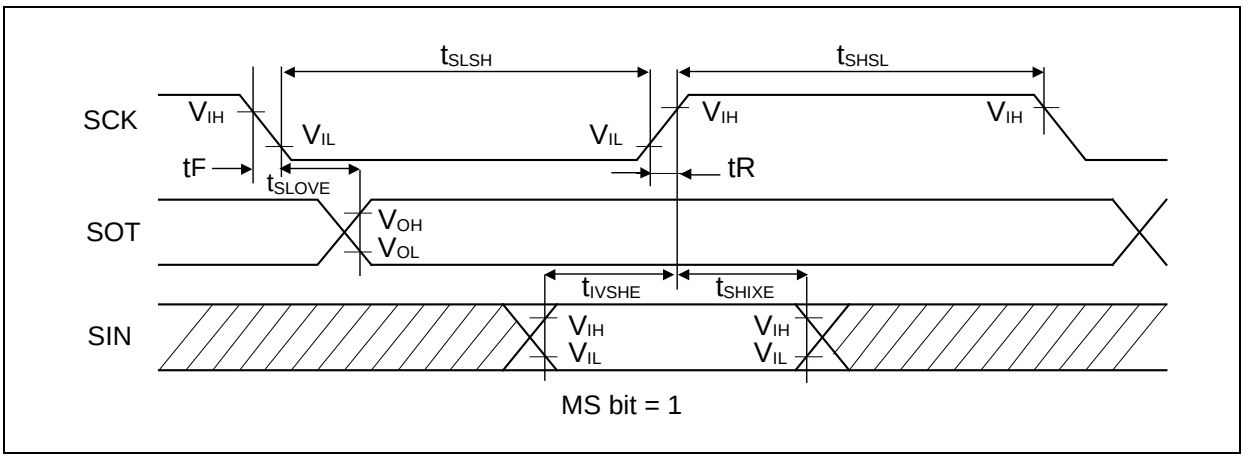
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		V_{CC} ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.



MS bit = 0



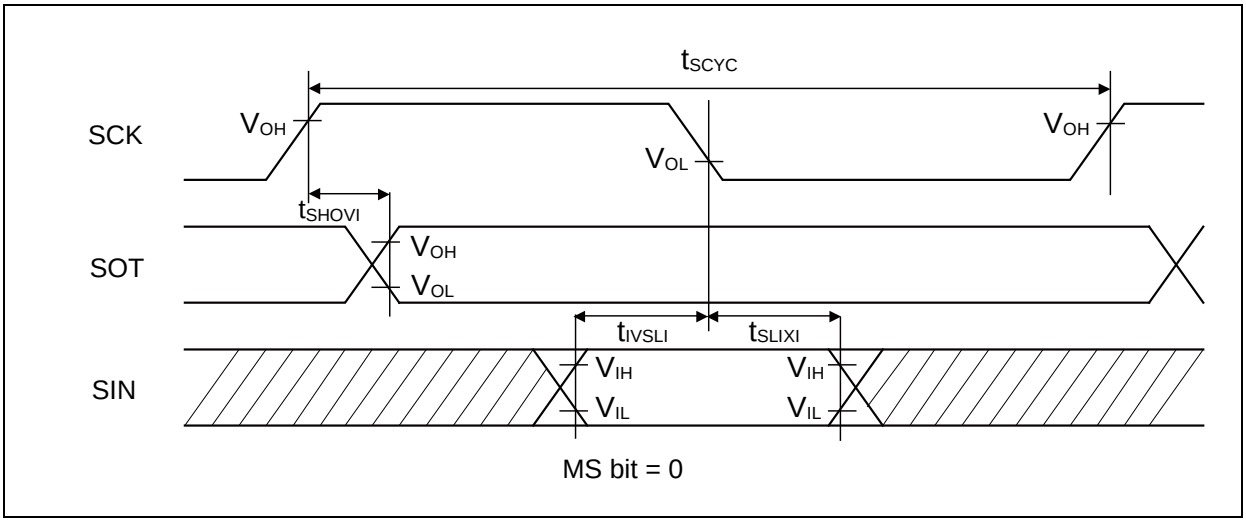
MS bit = 1

- Synchronous serial (SPI = 0, SCINV = 1)

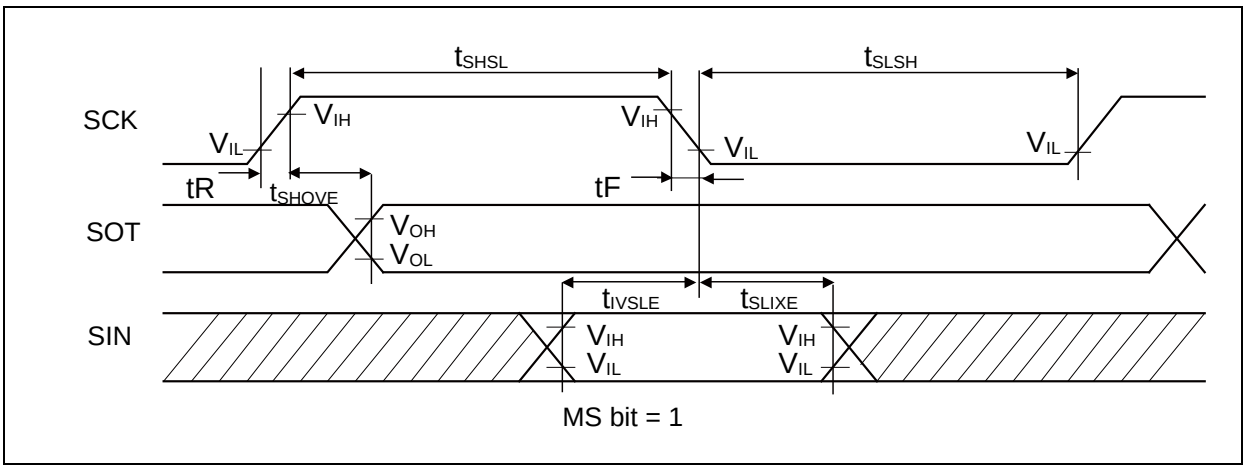
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		V_{CC} ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	36	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.



MS bit = 0



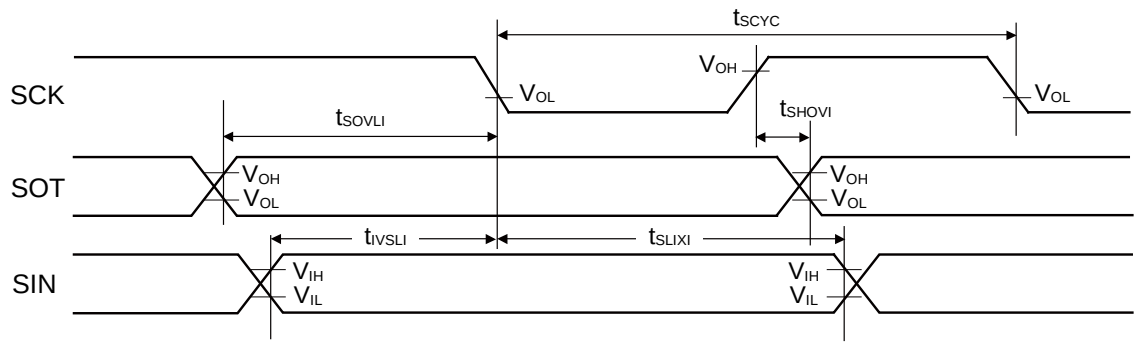
MS bit = 1

- Synchronous serial (SPI = 1, SCINV = 0)

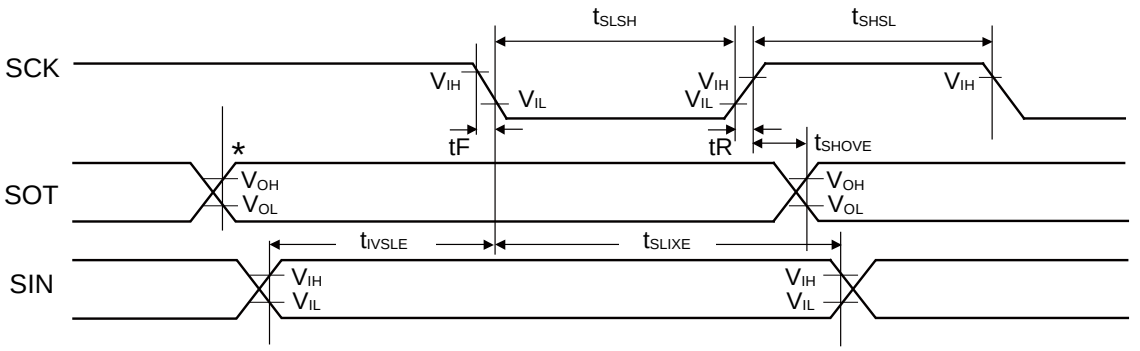
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		V_{CC} ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	36	-	ns
SCK ↓→ SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 34	-	$2t_{CYCP}$ - 34	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK ↓→ SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.



MS bit = 0



MS bit = 1

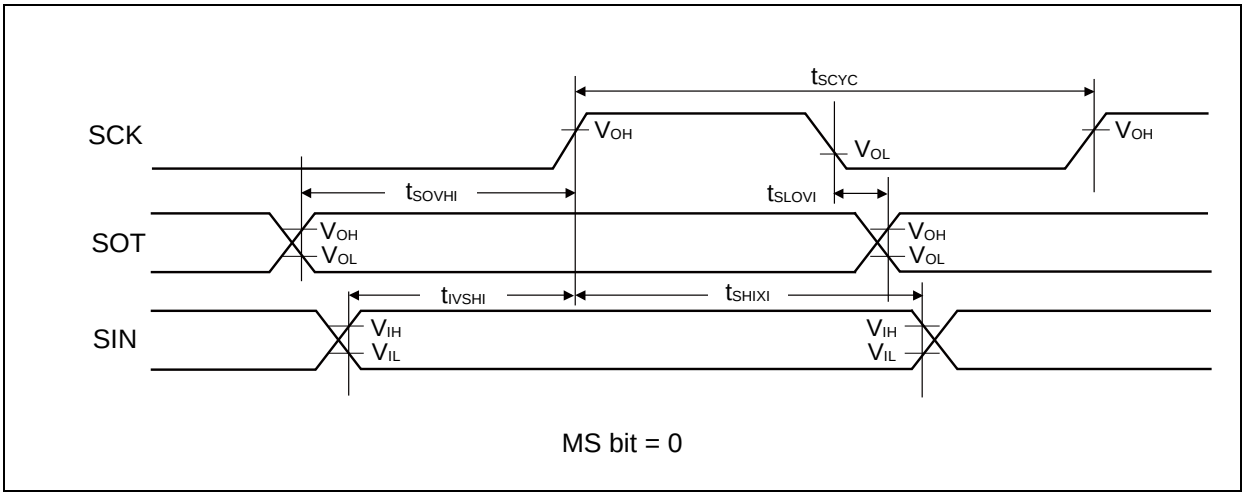
*: Changes when writing to TDR register

- Synchronous serial (SPI = 1, SCINV = 1)

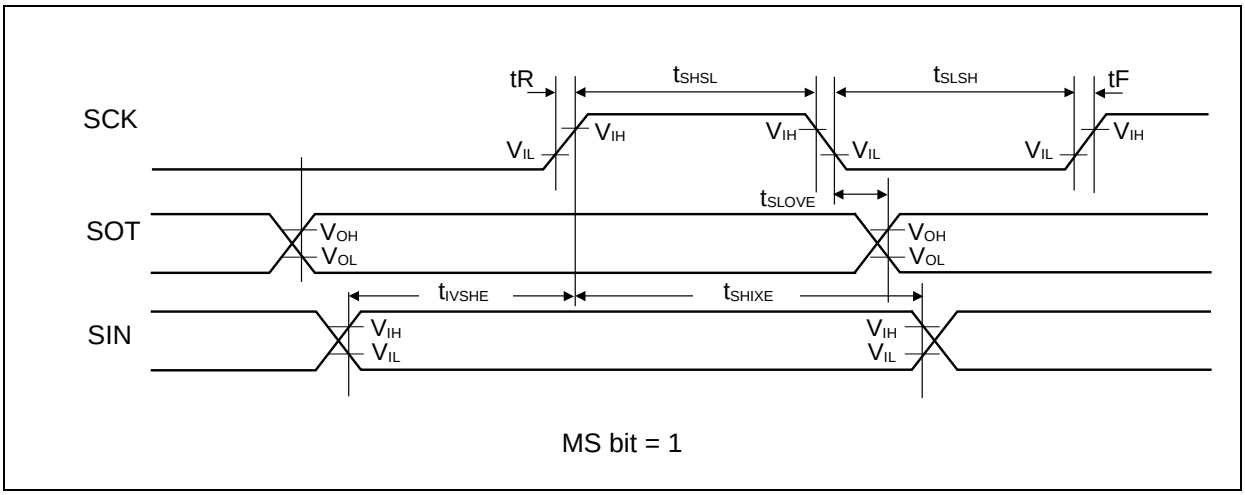
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		V_{CC} ≥ 2.7V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	36	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 34	-	$2t_{CYCP}$ - 34	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	33	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which Multi-function serial is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30pF.



MS bit = 0

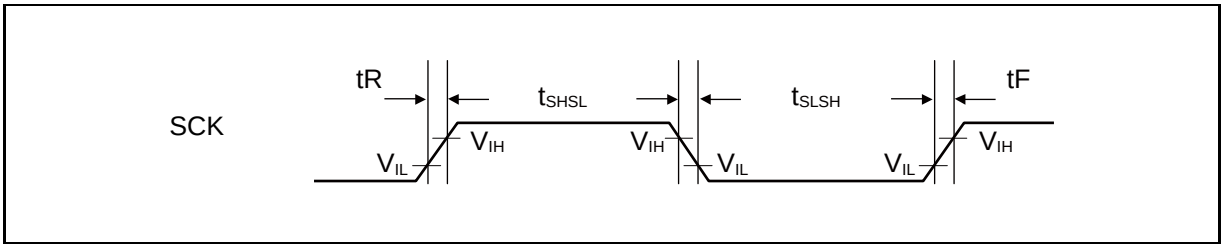


MS bit = 1

- External clock (EXT = 1) : asynchronous only

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 30pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	



(10) External Input Timing

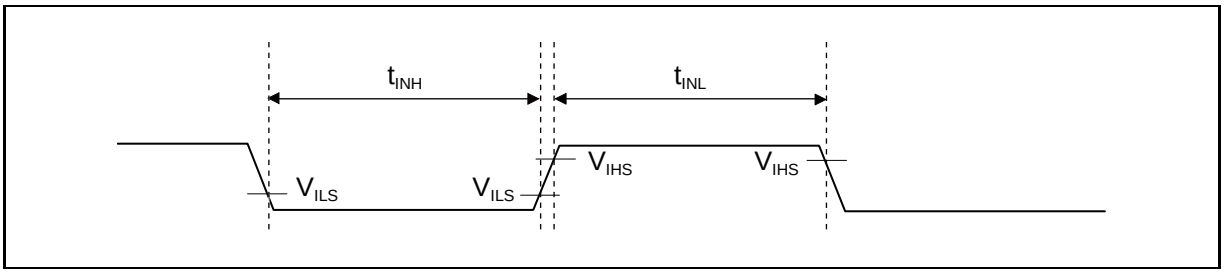
(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		INT00 to INT15, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	600*3	-	ns	Deep standby wake up

*1 : t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode, in timer mode.
About the APB bus number which the Multi-function Timer is connected to, see "■BLOCK DIAGRAM" in this data sheet.

*2 : When in stop mode, in timer mode.

*3 : When in deep standby RTC mode, in deep standby stop mode.



(11) I^2C Timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

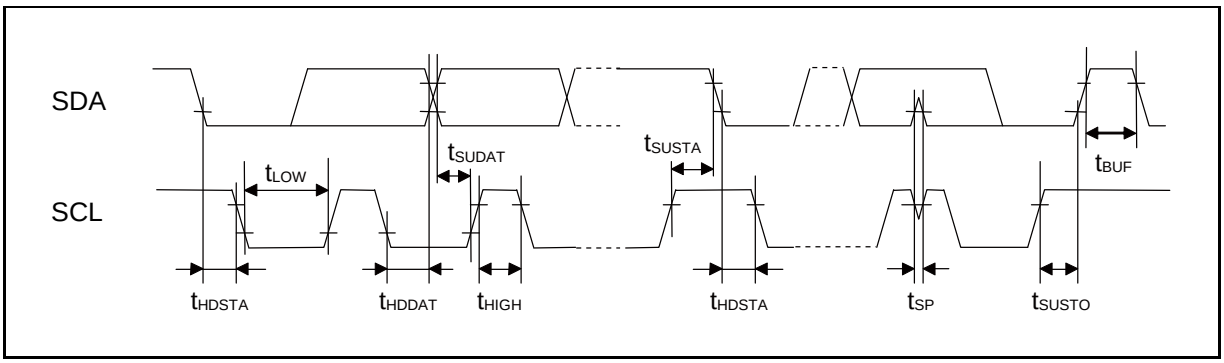
Parameter	Symbol	Conditions	Typical mode		High-speed mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1: R and C represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see "■BLOCK DIAGRAM" in this data sheet.
To use standard mode, set the APB bus clock at 2MHz or more.
To use high-speed mode, set the APB bus clock at 8MHz or more.

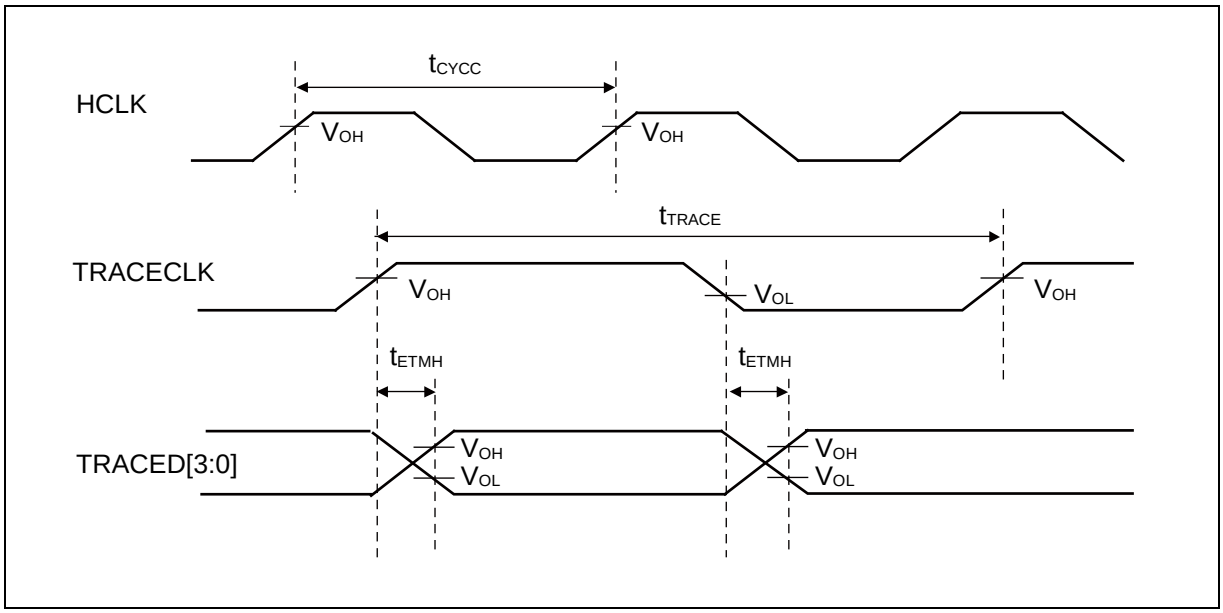


(12) ETM Timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[3:0]	$V_{CC} \geq 2.7V$	2	9	ns	
			$V_{CC} < 2.7V$	2	15		
TRACECLK frequency	1/ t_{TRACE}	TRACECLK	$V_{CC} \geq 2.7V$	-	40	MHz	
			$V_{CC} < 2.7V$	-	20	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{CC} \geq 2.7V$	20	-	ns	
			$V_{CC} < 2.7V$	50	-	ns	

Note: When the external load capacitance C_L = 30pF.

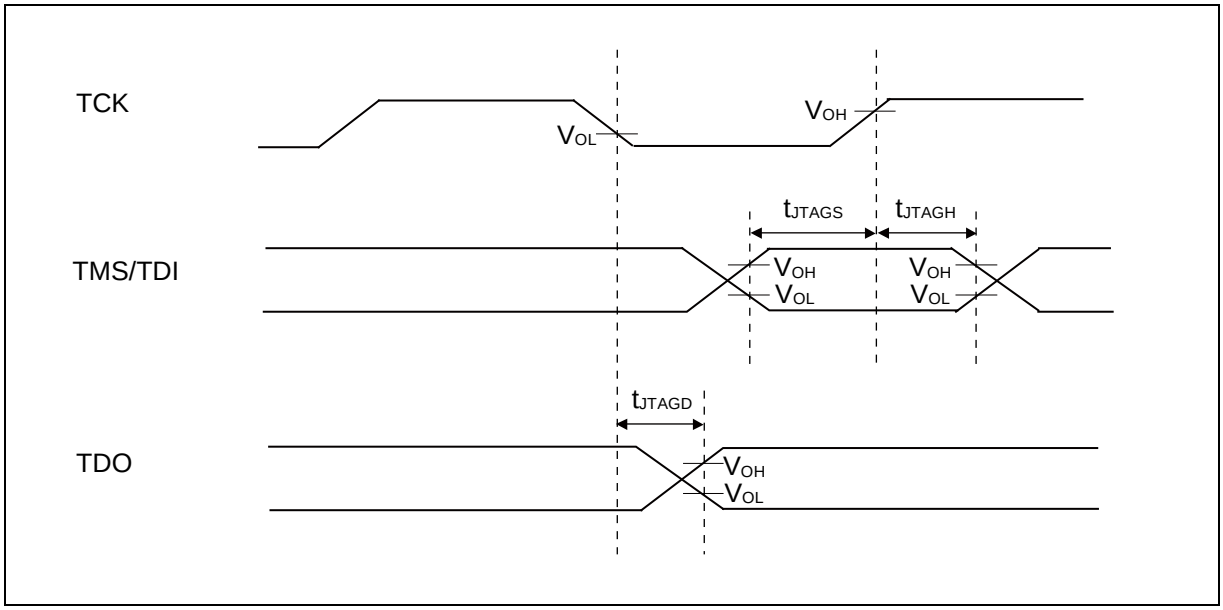


(13) JTAG Timing

(V_{CC} = 1.65V to 3.6V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 2.7V$	15	-	ns	
			$V_{CC} < 2.7V$				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 2.7V$	15	-	ns	
			$V_{CC} < 2.7V$				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 2.7V$	-	25	ns	
			$V_{CC} < 2.7V$	-	45		

Note: When the external load capacitance C_L = 30pF.



6. 12-bit A/D Converter

• Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 1.65V to 3.6V, V_{SS} =AV_{SS} = 0V, Ta = - 40°C to + 85°C)

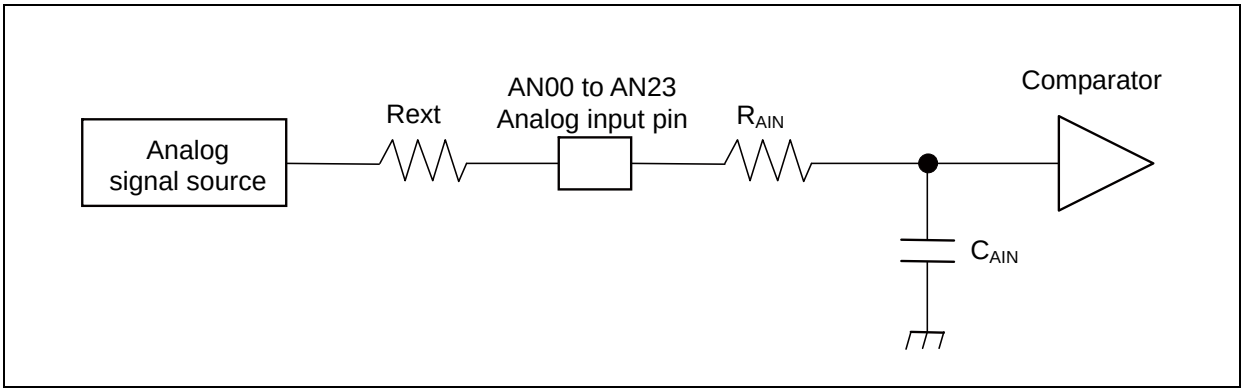
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	AN00 to AN23	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	AN00 to AN23	AVRH - 15	-	AVRH + 15	mV	
Conversion time	-	-	2.0*1	-	-	µs	$AV_{CC} \geq 2.7V$
Sampling time	Ts	-	*2	-	10	us	$AV_{CC} \geq 2.7V$
			*2	-			$1.8V \leq AV_{CC} < 2.7V$
			*2				$1.65V \leq AV_{CC} < 1.8V$
Compare clock cycle*3	Tcck	-	100	-	1000	ns	$AV_{CC} \geq 2.7V$
			200				$1.8V \leq AV_{CC} < 2.7V$
			500				$1.65V \leq AV_{CC} < 1.8V$
State transition time to operation permission	Tstt	-	1	-	-	µs	
Power supply current (analog + digital)	-	AVCC	-	0.27	0.42	mA	A/D 1unit operation
			-	0.03	10	µA	When A/D stop
Reference power supply current (between AVRH to AVSS)	-	AVRH	-	0.72	1.29	mA	A/D 1unit operation AVRH=3.6V
			-	0.02	2.6	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	9.4	pF	
Analog input resistor	R_{AIN}	-	-	-	2.2	kΩ	$AV_{CC} \geq 2.7V$
					5.5		$1.8V \leq AV_{CC} < 2.7V$
					10.5		$1.65V \leq AV_{CC} < 1.8V$
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	AN00 to AN23	-	-	5	µA	
Analog input voltage	-	AN00 to AN23	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	$AV_{CC} \geq 2.7V$
			AV_{CC}				$AV_{CC} < 2.7V$

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is the value of sampling time: 600ns and the value of compare time: 1400ns ($AV_{CC} \geq 2.7V$).
Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting*4 of the sampling time and compare clock cycle, see "Chapter: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Port".
The A/D Converter register is set at the peripheral clock timing. The sampling clock and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance.
Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).

*4: The register setting of the A/D Converter is set at the timing of the APB bus clock.
The sampling clock and compare clock are set in base clock (HCLK).
About the APB bus number which the A/D Converter is connected to, see "■BLOCK DIAGRAM" in this data sheet.



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

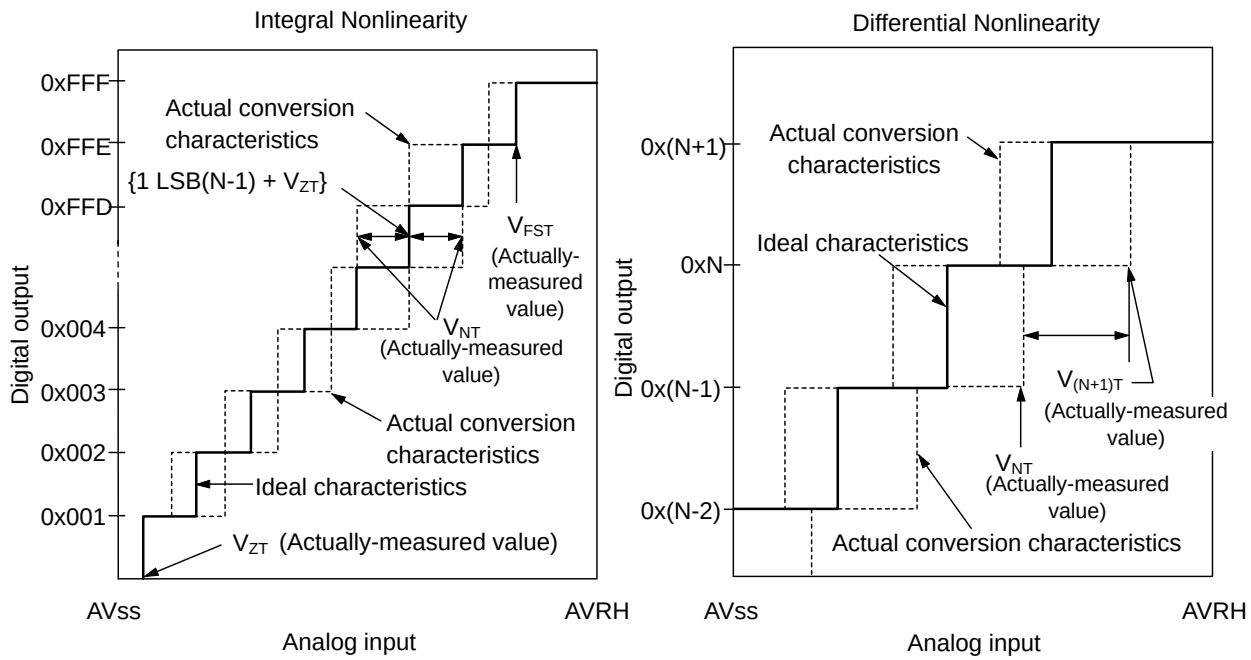
Ts : Sampling time[ns]
R_{AIN} : input resistor of A/D[kΩ] = 2.2kΩ at 2.7V ≤ AVCC ≤ 3.6V
input resistor of A/D[kΩ] = 5.5kΩ at 1.8V ≤ AVCC ≤ 2.7V
input resistor of A/D[kΩ] = 10.5kΩ at 1.65V ≤ AVCC ≤ 1.8V
C_{AIN} : input capacity of A/D[pF] = 9.4pF at 1.65V ≤ AVCC ≤ 3.6V
Rext : Output impedance of external circuit[kΩ]

(Equation 2) $Tc = Tcck \times 14$

Tc : Compare time
Tcck : Compare clock cycle

- Definition of 12-bit A/D Converter Terms

  - Resolution : Analog variation that is recognized by an A/D converter.
  - Integral Nonlinearity : Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
  - Differential Nonlinearity : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N : A/D converter digital output value.
V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

7. Low-Voltage Detection Characteristics

(1) Low-Voltage Detection Reset

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHR*1 = 00000	1.38	1.50	1.60	V	When voltage drops
Released voltage	VDH		1.43	1.55	1.65	V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00001	1.43	1.55	1.65	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00010	1.47	1.60	1.73	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00011	1.52	1.65	1.78	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
Detected voltage	VDL	SVHR*1 = 10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		Same as SVHR = 00000 value			V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	5200 × t_{CYCP}*2	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*1: The SVHR bit of Low-Voltage Detection Voltage Control Register (LVD_CTL) is initialized to "00000" by Low-Voltage Detection Reset.

*2: t_{CYCP} indicates the APB2 bus clock cycle time.

(2) Interrupt of Low-Voltage Detection

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH		1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI = 00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH		1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI = 00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH		1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI = 00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH		1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH		1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH		1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI = 01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH		1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI = 01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH		1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH		2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI = 01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH		2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH		2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH		2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI = 10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI = 10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH		2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI = 10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH		3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	5200 × t_{CYCP}*	µs	
LVD detection delay time	T_{LVDDL}	-	-	-	200	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

8. Flash Memory Write/Erase Characteristics

(V_{CC} = 1.65V to 3.6V, Ta = - 40°C to + 85°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	1.1	2.7	s	Includes write time prior to internal erase
	Small Sector		0.3	0.9		
Half word (16-bit) write time		-	30	528	µs	Not including system-level overhead time
Chip erase time		-	6.8	18	s	Includes write time prior to internal erase

Write cycles and data hold time

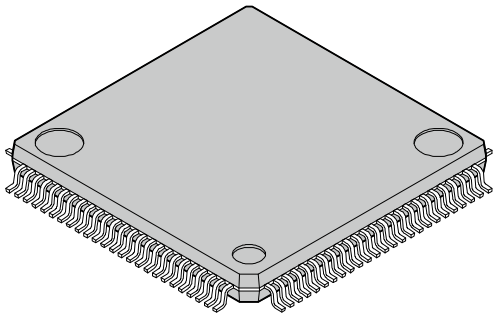
Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

■ ORDERING INFORMATION

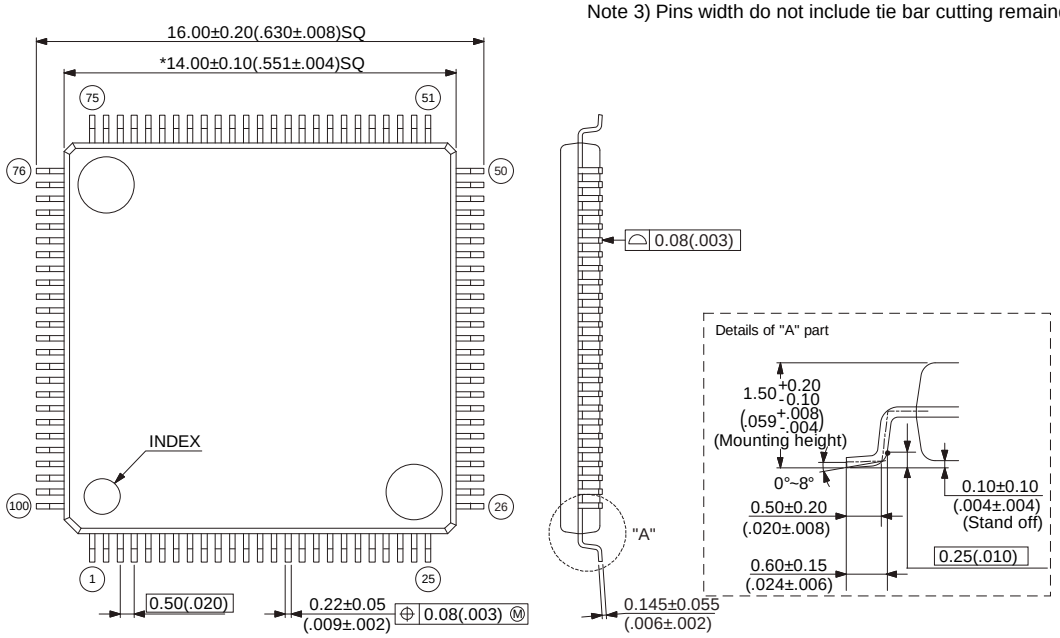
Part number	Package
MB9AFA41LAPMC1	Plastic・LQFP 64-pin (0.5mm pitch), (FPT-64P-M38)
MB9AFA42LAPMC1	
MB9AFA44LAPMC1	
MB9AFA41LAPMC	Plastic・LQFP 64-pin (0.65mm pitch), (FPT-64P-M39)
MB9AFA42LAPMC	
MB9AFA44LAPMC	
MB9AFA41LAQN	Plastic・QFN 64-pin (0.5mm pitch), (LCC-64P-M24)
MB9AFA42LAQN	
MB9AFA44LAQN	
MB9AFA41MAPMC	Plastic・LQFP 80-pin (0.5mm pitch), (FPT-80P-M37)
MB9AFA42MAPMC	
MB9AFA44MAPMC	
MB9AFA41MAPMC1	Plastic・LQFP 80-pin (0.65mm pitch), (FPT-80P-M40)
MB9AFA42MAPMC1	
MB9AFA44MAPMC1	
MB9AFA41MABGL	Plastic・PFBGA 96-pin (0.5mm pitch), (BGA-96P-M07)
MB9AFA42MABGL	
MB9AFA44MABGL	
MB9AFA41NAPMC	Plastic・LQFP 100-pin (0.5mm pitch), (FPT-100P-M23)
MB9AFA42NAPMC	
MB9AFA44NAPMC	
MB9AFA41NAPQC	Plastic・QFP 100-pin (0.65mm pitch), (FPT-100P-M36)
MB9AFA42NAPQC	
MB9AFA44NAPQC	
MB9AFA41NABGL	Plastic・PFBGA 112-pin (0.8mm pitch), (BGA-112P-M04)
MB9AFA42NABGL	
MB9AFA44NABGL	

■ PACKAGE DIMENSIONS

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.00 mm × 14.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-100P-M23)	Weight	0.65 g

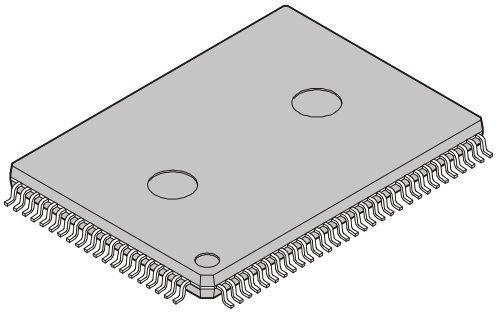
100-pin plastic LQFP
(FPT-100P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



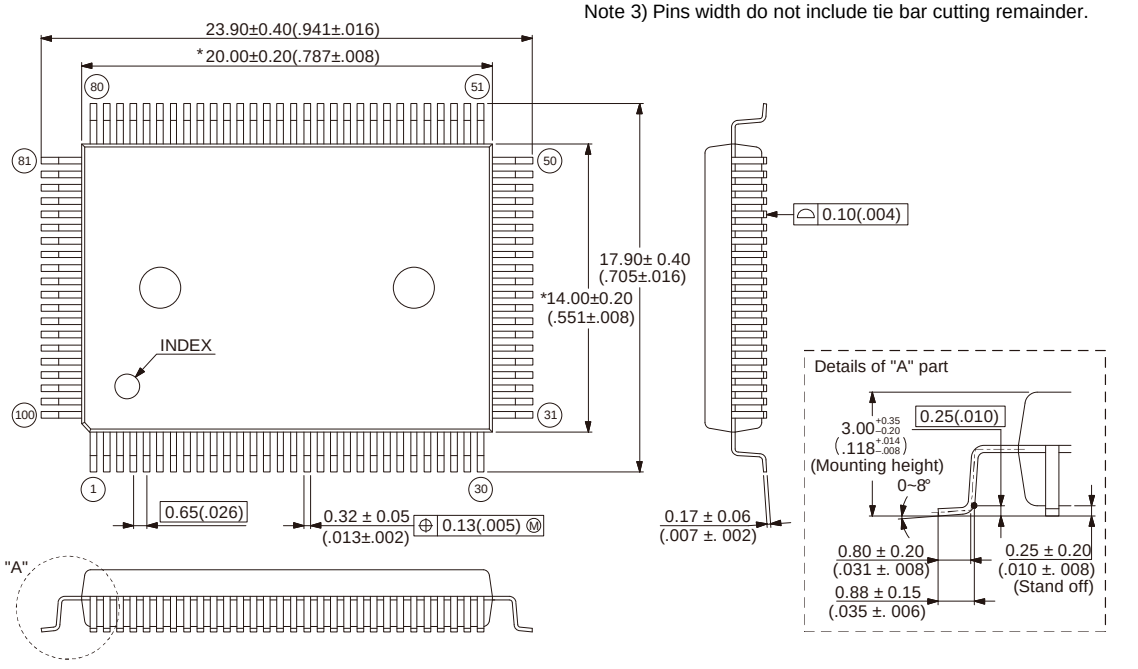
Dimensions in mm (inches).
Note:The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

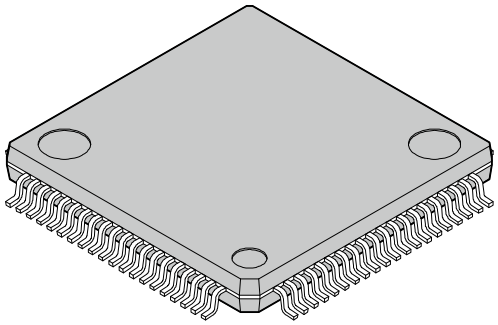
100-pin plastic QFP		
 (FPT-100P-M36)	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14 × 20-0.65

100-pin plastic QFP
(FPT-100P-M36)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

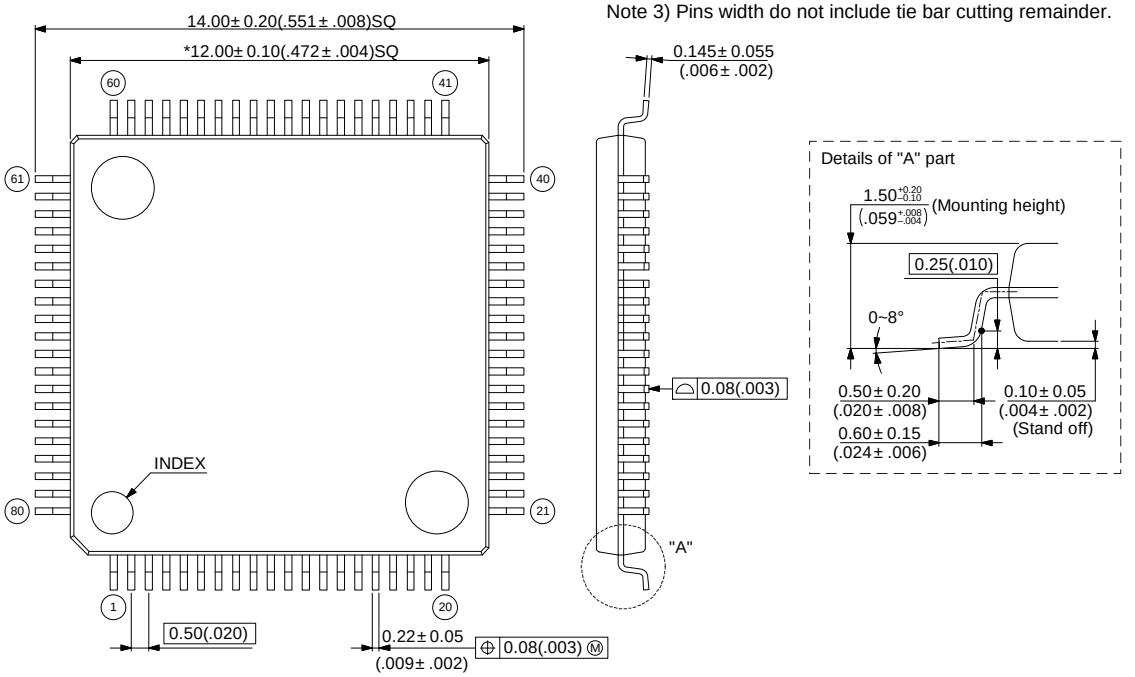


Dimensions in mm (inches).
Note: The valuesin parentheses are referencevalues.

80-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-80P-M37)	Weight	0.47 g

80-pin plastic LQFP
(FPT-80P-M37)

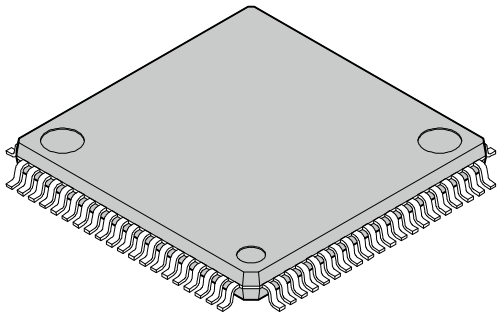
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

80-pin plastic LQFP

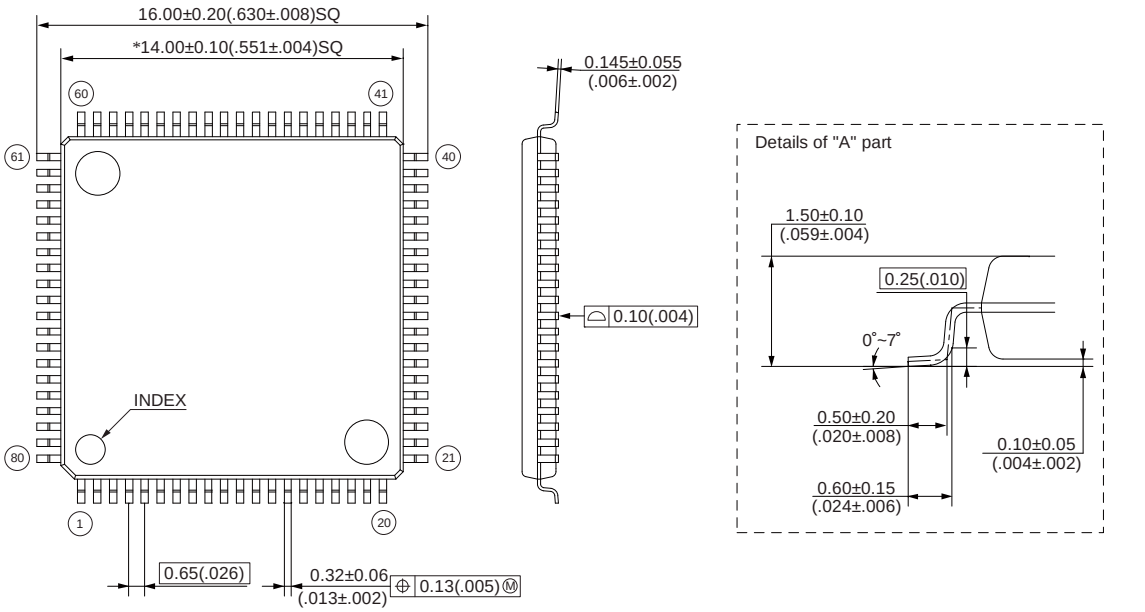


(FPT-80P-M40)

Lead pitch	0.65 mm
Package width × package length	14.00 mm × 14.00 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.60 mm Max.
Code (Reference)	P-LQFP80-14 × 14-0.65

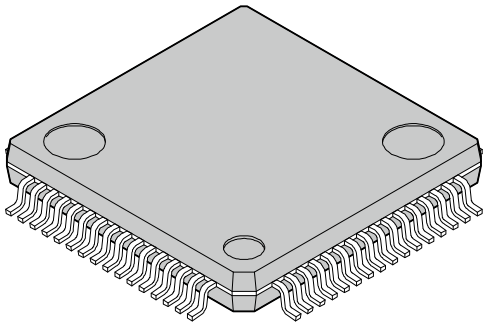
80-pin plastic LQFP
(FPT-80P-M40)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include



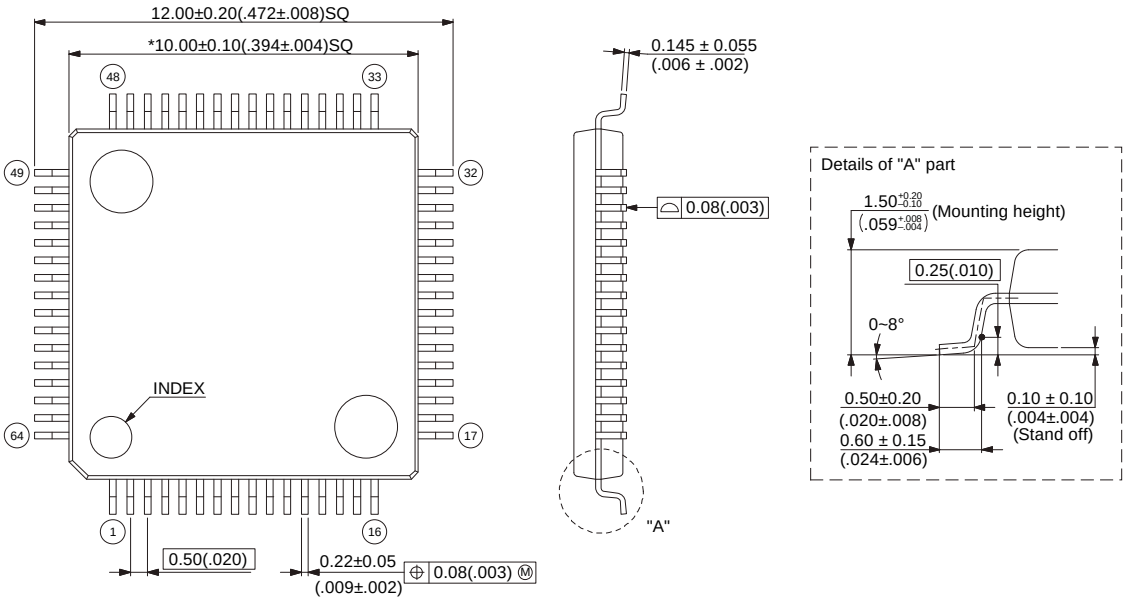
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.00 mm × 10.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-64P-M38)	Weight	0.32 g

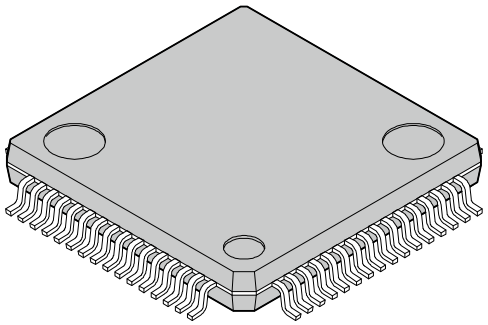
64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



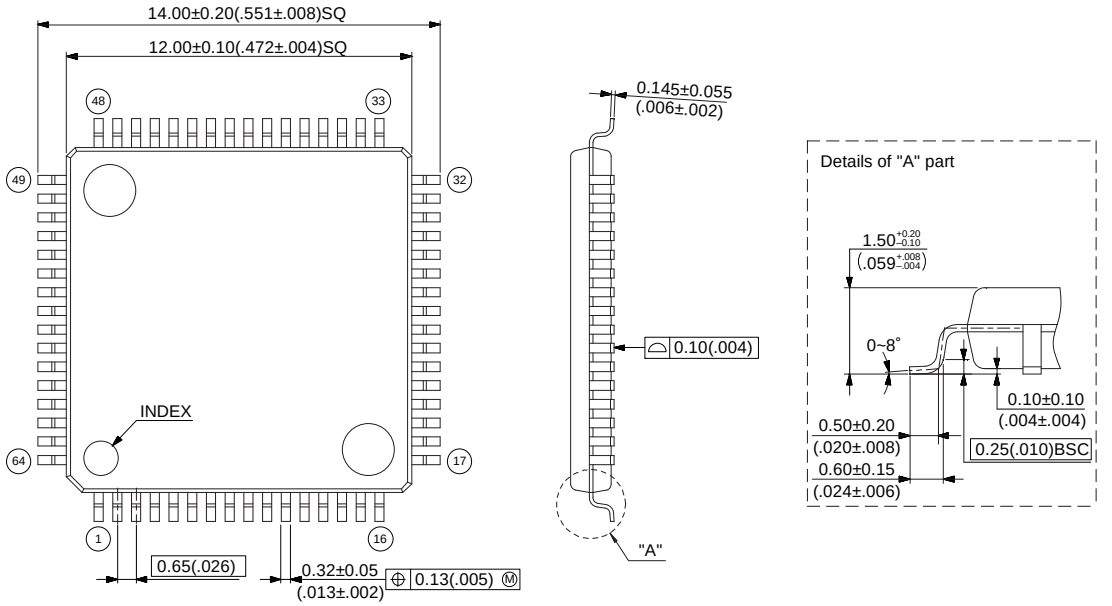
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
(FPT-64P-M39)		

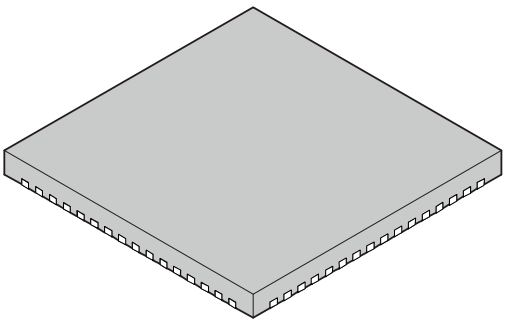
64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.

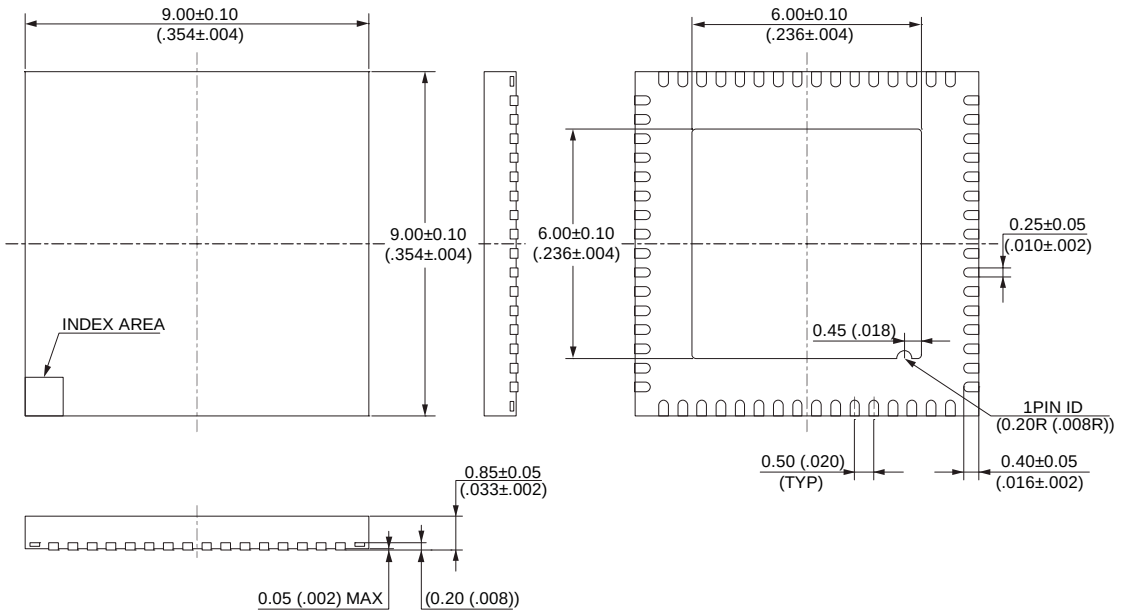


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

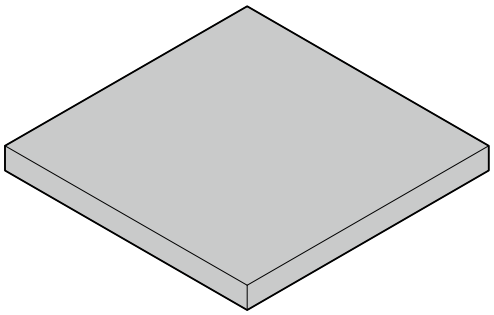
64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	-
(LCC-64P-M24)		

64-pin plastic QFN
(LCC-64P-M24)

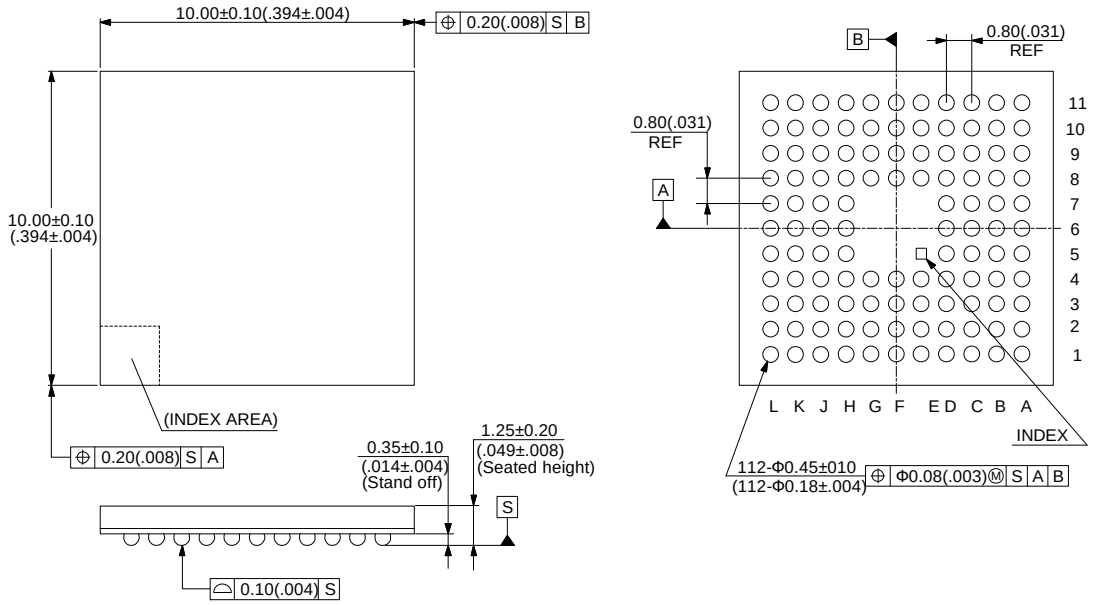


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

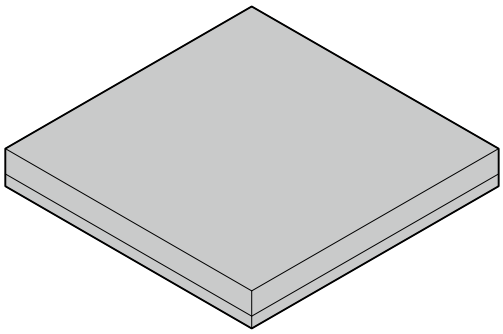
112-ball plastic PFBGA		
	Ball pitch	0.80 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Φ 0.45 mm
	Mounting height	1.45 mm Max.
(BGA-112P-M04)	Weight	0.22 g

112-ball plastic PFBGA
(BGA-112P-M04)

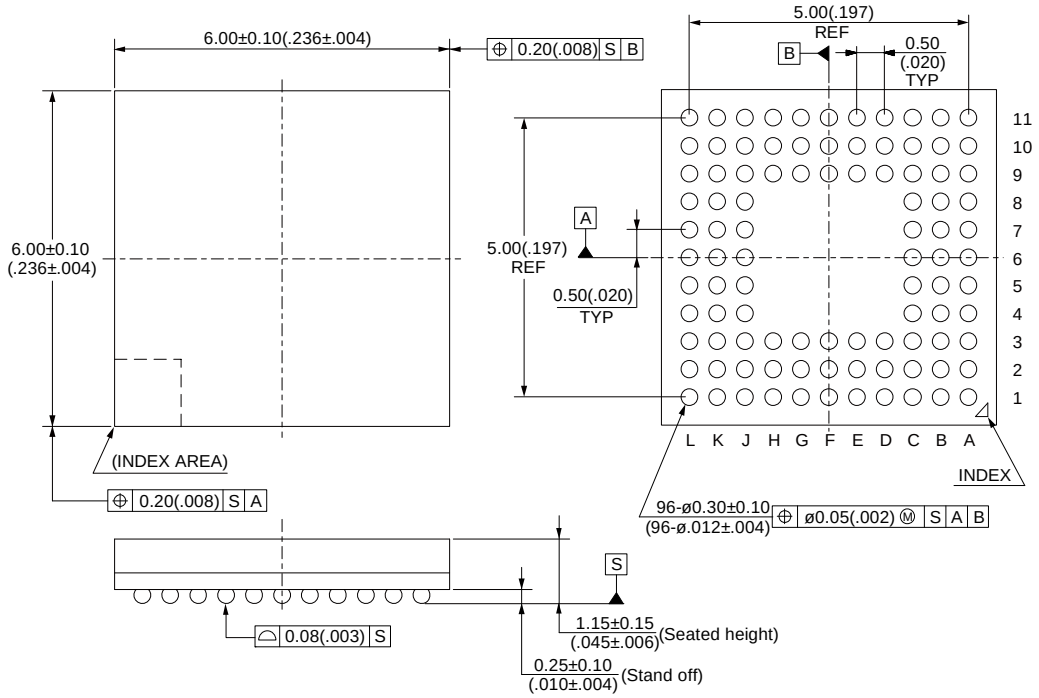


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

96-pin plastic FBGA		
	Lead pitch	0.5 mm
	Package width × package length	6.00 mm × 6.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	1.30 mm MAX
	Weight	0.08 g
(BGA-96P-M07)		

96-pin plastic FBGA
(BGA-96P-M07)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
2	■FEATURE ・On-chip Memories	Revised the descriptions of [Flash memory].
5	・Unique ID	Added the descriptions of "Unique ID".
7	■PRODUCT LINEUP ・Function	
52	■HANDLING DEVICES	Added the descriptions.
57	■MEMORY MAP ・Memory Map (2)	
62	■PIN STATUS IN EACH CPU STATE ・List of Pin Status	Revised the Pin status type of "I".
70	■ELECTRICAL CHARACTERISTICS 3.DC Characteristics (1) Current rating	・Revised the descriptions of Power supply current. ・Added the "Flash memory write/erase current". ・Added the footnote.
74	5.AC Characteristics (3) Built-in CR Oscillation Characteristics ・Built-in high-speed CR	Revised the table and the footnote.
78, 79	(7) External Bus Timing ・Separate Bus Access Asynchronous SRAM Mode	Revised the table and the figure.
80	・Separate Bus Access Synchronous SRAM Mode	
85, 87, 89, 91	(9) CSIO Timing	・Revised the title to "CSIO Timing". ・Revised the note.
94	(11) I^2C Timing	Revised the footnote.
97	6. 12-bit A/D Converter • Electrical Characteristics for the A/D Converter	• Revised the parameter. • Revised the symbol. • Corrected the value.
99	• Definition of 12-bit A/D Converter Terms	• Revised the parameter. • Revised the symbol.
100	7. Low-Voltage Detection Characteristics (1) Low-Voltage Detection Reset	• Corrected "Conditions" and "Value" in the table. • Added the Item. • Added the footnote.
101	(2) Interrupt of Low-Voltage Detection	Added the Item.

MEMO

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