

## 32-bit ARM™ Cortex™-M3 based Microcontroller

# FM3 MB9A310K Series

## MB9AF311K, MB9AF312K

### ■ DESCRIPTION

The MB9A310K Series are a highly integrated 32-bit microcontrollers dedicated for embedded controllers with high-performance and low cost.

These series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (USB, UART, CSIO, I<sup>2</sup>C, LIN).

The products which are described in this data sheet are placed into TYPE5 product categories in "FM3 Family PERIPHERAL MANUAL".

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# MB9A310K Series

## ■ FEATURES

- 32-bit ARM Cortex-M3 Core
  - Processor version: r2p1
  - Up to 40MHz Frequency Operation
  - Integrated Nested Vectored Interrupt Controller (NVIC) : 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
  - 24-bit System timer (Sys Tick) : System timer for OS task management

- On-chip Memories

### [Flash memory]

This Series are based on two independent on-chip Flash memories.

- MainFlash
  - Up to 128Kbyte
  - Read cycle : 0 wait-cycle
  - Security function for code protection
- WorkFlash
  - 32Kbyte
  - Read cycle : 0 wait-cycle
  - Security function is shared with code protection

### [SRAM]

This Series contain a total of up to 16Kbyte on-chip SRAM memories. This is composed of two independent SRAM (SRAM0, SRAM1) . SRAM0 is connected to I-code bus or D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0 : 8 Kbyte
- SRAM1 : 8 Kbyte

- USB Interface

USB interface is composed of Function and Host.

### [USB function]

- USB2.0 Full-Speed supported
- Max 6 EndPoint supported
  - EndPoint 0 is control transfer
  - EndPoint 1, 2 can be selected Bulk-transfer, Interrupt-transfer or Isochronous-transfer
  - EndPoint 3 to 5 can be selected Bulk-transfer or Interrupt-transfer
- EndPoint 1 to 5 is comprised Double Buffer

### [USB host]

- USB2.0 Full/Low-speed supported
- Bulk-transfer, interrupt-transfer and Isochronous-transfer support
- USB Device connected/dis-connected automatically detect
- IN/OUT token handshake packet automatically
- Max 256-byte packet-length supported
- Wake-up function supported

- Multi-function Serial Interface (Max 4channels)

- 2 channels with 16-steps × 9-bits FIFO (ch.0, ch.1), 2 channels without FIFO (ch.3, ch.5)
- Operation mode is selectable from the followings for each channel.  
(In ch.5, only UART and LIN are available.)
  - UART
  - CSIO
  - LIN
  - I<sup>2</sup>C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13 to 16-bit length)
- LIN break delimiter generate (can be changed 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[I<sup>2</sup>C]

Standard mode (Max 100kbps) / High-speed mode (Max 400kbps) supported

- DMA Controller (4channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4Gbyte)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

- A/D Converter (Max 8channels)

[12-bit A/D Converter]

- Successive Approximation Register type
- Built-in 2unit
- Conversion time: 1.0μs@5V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage  
(for SCAN conversion: 16steps, for Priority conversion: 4steps)

# MB9A310K Series

- **Base Timer (Max 8channels)**

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

- **General Purpose I/O Port**

This series can use its pins as General Purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up 36 fast General Purpose I/O Ports
- Some pin is 5V tolerant I/O.

See "■PIN DESCRIPTION" to confirm the corresponding pins.

- **Multi-function Timer**

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch.
- Input capture × 4ch.
- Output compare × 6ch.
- A/D activating compare × 3ch.
- Waveform generator × 3ch.
- 16-bit PPG timer × 3ch.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

- **Real-time clock (RTC)**

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

- **Quadrature Position/Revolution Counter (QPRC)**

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

- **Dual Timer (32/16-bit Down Counter)**

The Dual Timer consists of two programmable 32/16-bit down counters. Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

- **Watch Counter**

The Watch counter is used for wake up from Low Power Consumption mode.

- Interval timer: up to 64s (Max) @ Sub Clock : 32.768kHz

- **External Interrupt Controller Unit**

- Up to 6 external interrupt input pin
- Include one non-maskable interrupt (NMI)

- **Watchdog Timer (2channels)**

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except RTC and STOP and Deep stand-by RTC and Deep stand-by STOP.

- **CRC (Cyclic Redundancy Check) Accelerator**

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

# MB9A310K Series

- Clock and Reset

[Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main Clock : 4MHz to 48MHz
- Sub Clock : 32.768kHz
- High-speed internal CR Clock : 4MHz
- Low-speed internal CR Clock : 100kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock supervisor reset

- Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

- Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

- Low Power Consumption Mode

Six Low Power Consumption modes supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep stand-by RTC
- Deep stand-by STOP

- Debug

Serial Wire JTAG Debug Port (SWJ-DP)

- Power Supply

- Wide range voltage : VCC = 2.7V to 5.5V
- Power supply for USB I/O : USBVCC0 = 3.0V to 3.6V (when USB is used)  
= 2.7V to 5.5V (when GPIO is used)

# MB9A310K Series

## ■ PRODUCT LINEUP

### ● Memory size

Product name		MB9AF311K	MB9AF312K
On-chip Flash	MainFlash	64Kbyte	128Kbyte
	WorkFlash	32Kbyte	32Kbyte
On-chip SRAM	SRAM0	8Kbyte	8Kbyte
	SRAM1	8Kbyte	8Kbyte
	Total	16Kbyte	16Kbyte

### ● Function

Product name		MB9AF311K MB9AF312K
Pin count		48/52
CPU		Cortex-M3
	Freq.	40MHz
Power supply voltage range		2.7V to 5.5V (USBVCC:3.0V to 3.6V)
USB2.0 (Function/Host)		1ch. (Max)
DMAC		4ch. (Max)
Multi-function Serial Interface (UART/CSIO/LIN/I <sup>2</sup> C)		4ch. (Max) with 16-steps × 9-bits FIFO : ch.0, ch.1 without FIFO : ch.3, ch.5 (In ch.5, only UART and LIN are available.)
Base Timer (PWC/ Reload timer/PWM/PPG)		8ch. (Max)
MF-Timer	A/D activation compare	3ch.
	Input capture	4ch.
	Free-run timer	3ch.
	Output compare	6ch.
	Waveform generator	3ch.
	PPG	3ch.
QPRC		1ch. (Max)
Dual Timer		1 unit
Real-time clock		1 unit
Watch Counter		1 unit
CRC Accelerator		Yes
Watchdog timer		1ch. (SW) + 1ch. (HW)
External Interrupts		6pins (Max) + NMI × 1
General Purpose I/O ports		36pins (Max)
12-bit A/D converter		8ch. (2 units)
CSV (Clock Super Visor)		Yes
LVD (Low-Voltage Detector)		2ch.
Internal OSC	High-speed	4MHz (±2%)
	Low-speed	100kHz (Typ)
Debug Function		SWJ-DP

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.

It is necessary to use the port relocate function of the General I/O port according to your function use.

# MB9A310K Series

## ■ PACKAGES

Package	Product name	MB9AF311K MB9AF312K
LQFP: FPT-48P-M49 (0.5mm pitch)		○
QFN: LCC-48P-M73 (0.5mm pitch)		○
LQFP: FPT-52P-M02 (0.65mm pitch)		○

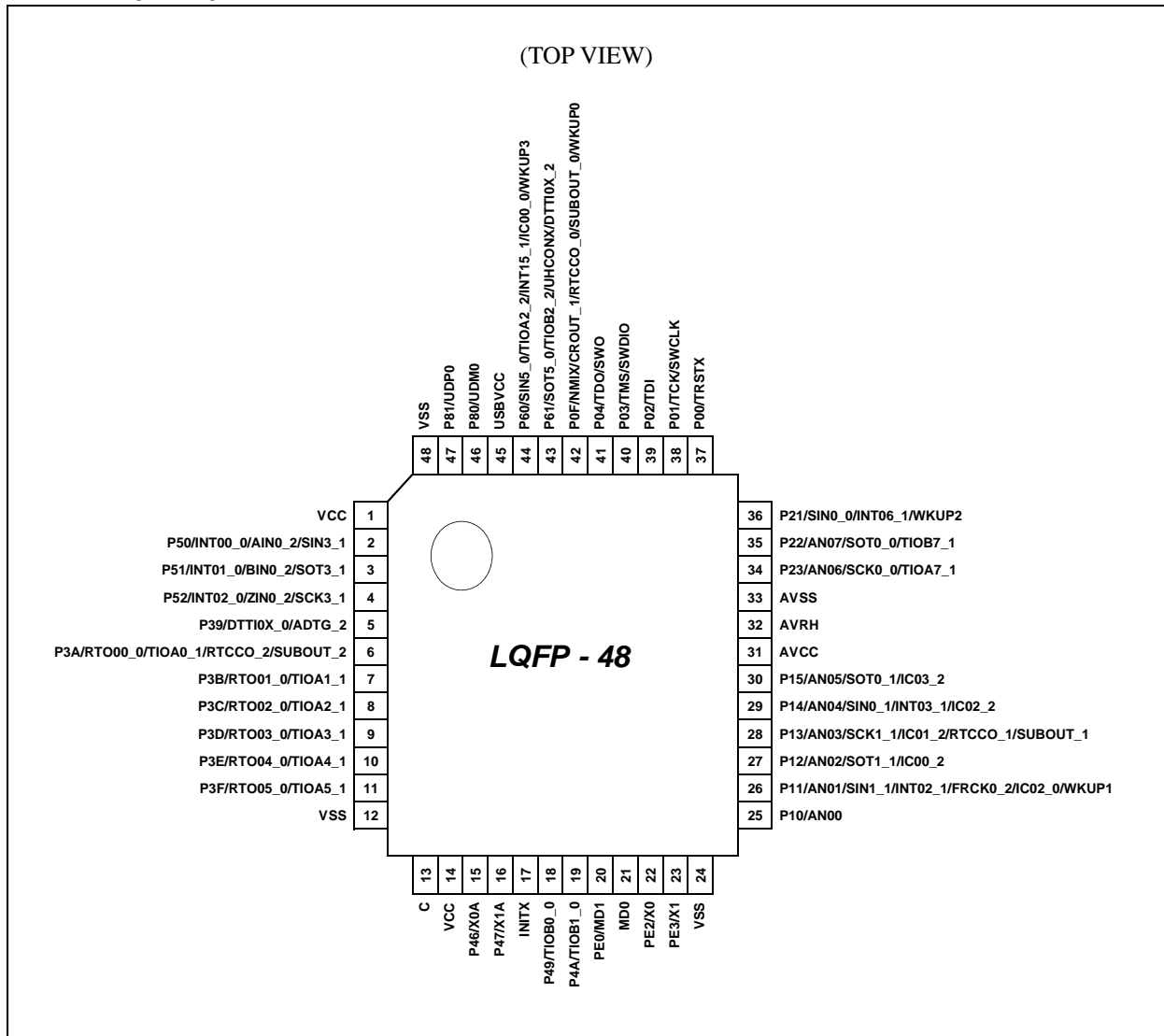
○ : Supported

Note : See "■PACKAGE DIMENSIONS" for detailed information on each package.



## ■ PIN ASSIGNMENT

- FPT-48P-M49

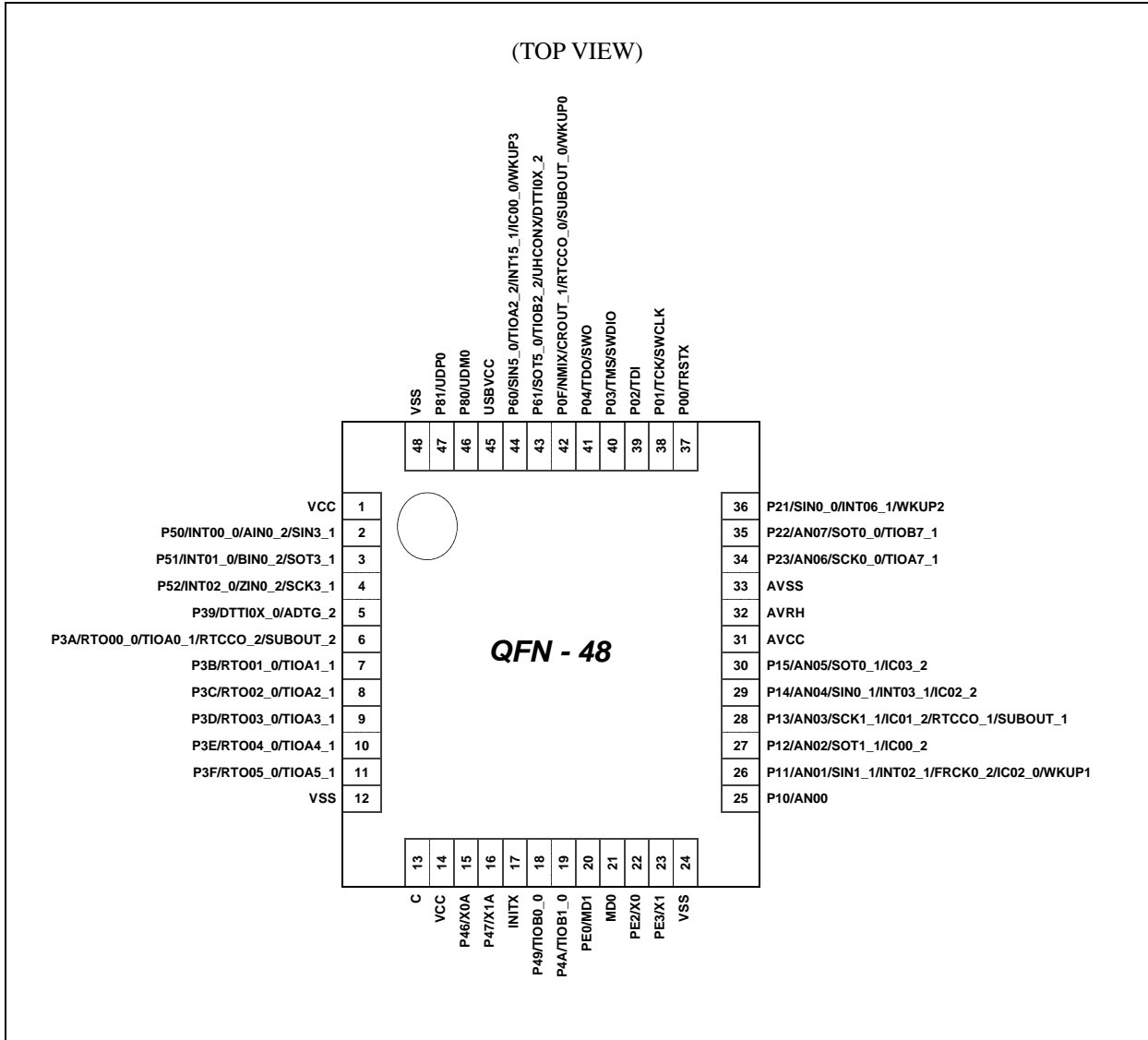


### <Note>

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

# MB9A310K Series

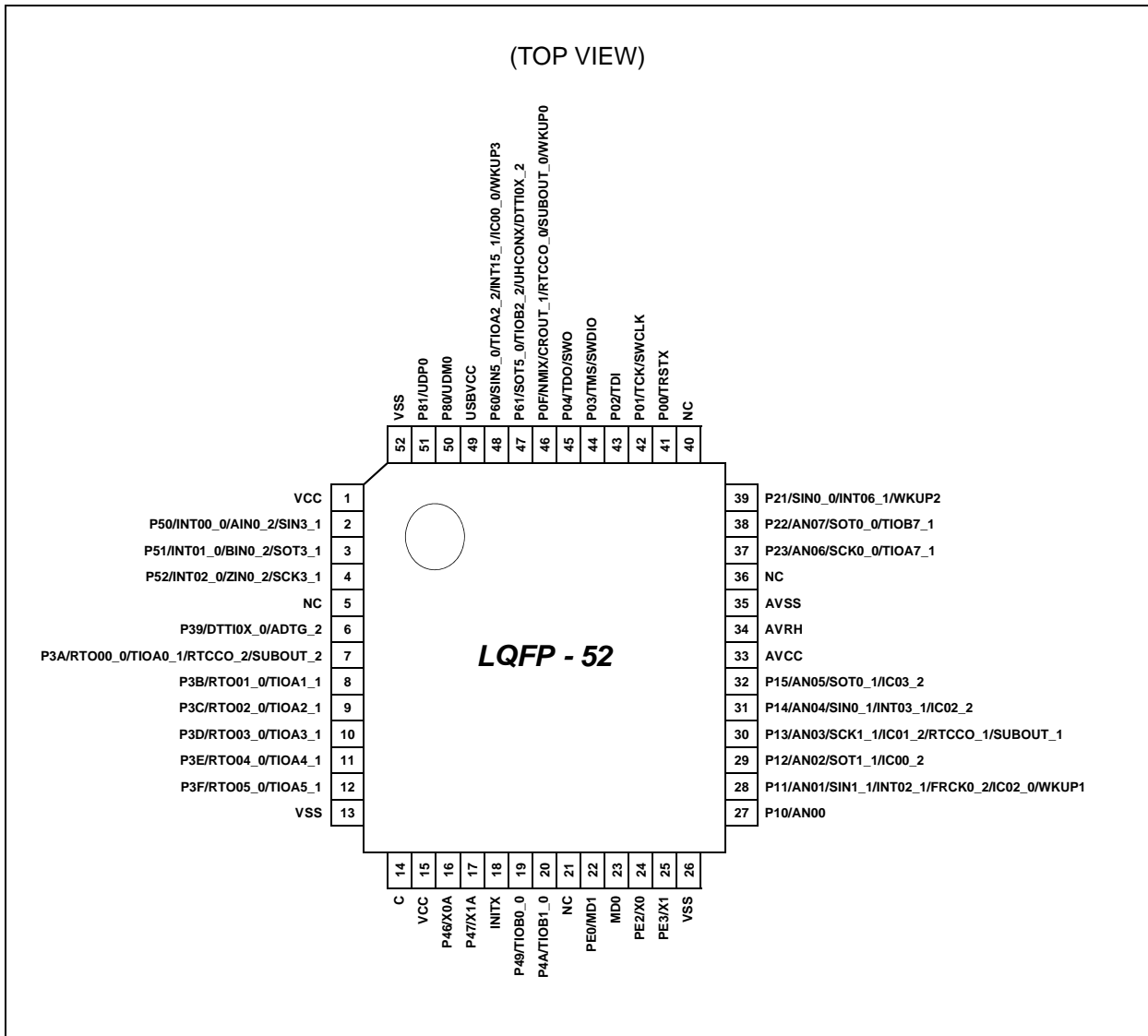
● LCC-48P-M73



**<Note>**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

● FPT-52P-M02



**<Note>**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

# MB9A310K Series

## ■ PIN DESCRIPTION

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No		Pin Name	I/O circuit type	Pin state type
LQFP-48 QFN-48	LQFP-52			
1	1	VCC	-	
2	2	P50	I *	H
		INT00_0		
		AIN0_2		
		SIN3_1		
3	3	P51	I *	H
		INT01_0		
		BIN0_2		
		SOT3_1		
4	4	P52	I *	H
		INT02_0		
		ZIN0_2		
		SCK3_1		
-	5	NC	-	
5	6	P39	E	I
		DTTIOX_0		
		ADTG_2		
6	7	P3A	G	I
		RTO00_0		
		TIOA0_1		
		RTCCO_2		
		SUBOUT_2		
7	8	P3B	G	I
		RTO01_0		
		TIOA1_1		
8	9	P3C	G	I
		RTO02_0		
		TIOA2_1		
9	10	P3D	G	I
		RTO03_0		
		TIOA3_1		
10	11	P3E	G	I
		RTO04_0		
		TIOA4_1		
11	12	P3F	G	I
		RTO05_0		
		TIOA5_1		
12	13	VSS	-	

# MB9A310K Series

Pin No		Pin Name	I/O circuit type	Pin state type
LQFP-48 QFN-48	LQFP-52			
13	14	C	-	
14	15	VCC	-	
15	16	P46	D	M
		X0A		
16	17	P47	D	N
		X1A		
17	18	INITX	B	C
18	19	P49	E	I
		TIOB0_0		
19	20	P4A	E	I
		TIOB1_0		
-	21	NC	-	
20	22	PE0	C	P
		MD1		
21	23	MD0	J	D
22	24	PE2	A	A
		X0		
23	25	PE3	A	B
		X1		
24	26	VSS	-	
25	27	P10	F	K
		AN00		
26	28	P11	F	F
		AN01		
		SIN1_1		
		INT02_1		
		FRCK0_2		
		IC02_0		
27	29	WKUP1	F	K
		P12		
		AN02		
		SOT1_1		
28	30	IC00_2	F	K
		P13		
		AN03		
		SCK1_1		
		IC01_2		
		RTCCO_1		
29	31	SUBOUT_1	F	L
		P14		
		AN04		
		SIN0_1		
		INT03_1		
		IC02_2		

# MB9A310K Series

Pin No		Pin Name	I/O circuit type	Pin state type
LQFP-48 QFN-48	LQFP-52			
30	32	P15	F	K
		AN05		
		SOT0_1		
		IC03_2		
31	33	AVCC	-	
32	34	AVRH	-	
33	35	AVSS	-	
-	36	NC	-	
34	37	P23	F	K
		AN06		
		SCK0_0		
		TIOA7_1		
35	38	P22	F	K
		AN07		
		SOT0_0		
		TIOB7_1		
36	39	P21	E	G
		SIN0_0		
		INT06_1		
		WKUP2		
-	40	NC	-	
37	41	P00	E	E
		TRSTX		
38	42	P01	E	E
		TCK		
		SWCLK		
39	43	P02	E	E
		TDI		
40	44	P03	E	E
		TMS		
		SWDIO		
41	45	P04	E	E
		TDO		
		SWO		
42	46	P0F	E	J
		NMIX		
		CROUT_1		
		RTCCO_0		
		SUBOUT_0		
		WKUP0		
43	47	P61	E	I
		SOT5_0		
		TIOB2_2		
		UHCONX		
		DTTIOX_2		

# MB9A310K Series

Pin No		Pin Name	I/O circuit type	Pin state type
LQFP-48 QFN-48	LQFP-52			
44	48	P60	I *	G
		SIN5_0		
		TIOA2_2		
		INT15_1		
		IC00_0		
		WKUP3		
45	49	USBVCC	-	
46	50	P80	H	O
		UDM0		
47	51	P81	H	O
		UDP0		
48	52	VSS	-	

\*: 5V tolerant I/O

# MB9A310K Series

## ■ SIGNAL DESCRIPTION

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No	
			LQFP-48 QFN-48	LQFP-52
ADC	ADTG_2	A/D converter external trigger input pin	5	6
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	25	27
	AN01		26	28
	AN02		27	29
	AN03		28	30
	AN04		29	31
	AN05		30	32
	AN06		34	37
	AN07		35	38
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	6	7
	TIOB0_0	Base timer ch.0 TIOB pin	18	19
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	7	8
	TIOB1_0	Base timer ch.1 TIOB pin	19	20
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	8	9
	TIOA2_2		44	48
	TIOB2_2	Base timer ch.2 TIOB pin	43	47
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	9	10
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	10	11
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	11	12
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	34	37
	TIOB7_1	Base timer ch.7 TIOB pin	35	38
Debugger	SWCLK	Serial wire debug interface clock input pin	38	42
	SWDIO	Serial wire debug interface data input/output pin	40	44
	SWO	Serial wire viewer output pin	41	45
	TCK	J-TAG test clock input pin	38	42
	TDI	J-TAG test data input pin	39	43
	TDO	J-TAG debug data output pin	41	45
	TMS	J-TAG test mode state input/output pin	40	44
	TRSTX	J-TAG test reset Input pin	37	41
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2
	INT01_0	External interrupt request 01 input pin	3	3
	INT02_0	External interrupt request 02 input pin	4	4
	INT02_1		26	28
	INT03_1	External interrupt request 03 input pin	29	31
	INT06_1	External interrupt request 06 input pin	36	39
	INT15_1	External interrupt request 15 input pin	44	48
	NMIX	Non-Maskable Interrupt input pin	42	46



# MB9A310K Series

Module	Pin name	Function	Pin No	
			LQFP-48 QFN-48	LQFP-52
GPIO	P00	General-purpose I/O port 0	37	41
	P01		38	42
	P02		39	43
	P03		40	44
	P04		41	45
	P0F		42	46
	P10	General-purpose I/O port 1	25	27
	P11		26	28
	P12		27	29
	P13		28	30
	P14		29	31
	P15		30	32
	P21	General-purpose I/O port 2	36	39
	P22		35	38
	P23		34	37
	P39	General-purpose I/O port 3	5	6
	P3A		6	7
	P3B		7	8
	P3C		8	9
	P3D		9	10
	P3E		10	11
	P3F		11	12
	P46	General-purpose I/O port 4	15	16
	P47		16	17
	P49		18	19
	P4A		19	20
	P50	General-purpose I/O port 5	2	2
	P51		3	3
	P52		4	4
	P60	General-purpose I/O port 6	44	48
	P61		43	47
	P80	General-purpose I/O port 8	46	50
P81	47		51	
PE0	General-purpose I/O port E	20	22	
PE2		22	24	
PE3		23	25	

# MB9A310K Series

Module	Pin name	Function	Pin No.	
			LQFP-48 QFN-48	LQFP-52
Multi- function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	36	39
	SIN0_1		29	31
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I <sup>2</sup> C (operation mode 4).	35	38
	SOT0_1 (SDA0_1)		30	32
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation modes 2) and as SCL0 when it is used in an I <sup>2</sup> C (operation mode 4).	34	37
Multi- function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	26	28
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I <sup>2</sup> C (operation mode 4).	27	29
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an I <sup>2</sup> C (operation mode 4).	28	30

# MB9A310K Series

Module	Pin name	Function	Pin No.	
			LQFP-48 QFN-48	LQFP-52
Multi- function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	2
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I <sup>2</sup> C (operation mode 4).	3	3
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I <sup>2</sup> C (operation mode 4).	4	4
Multi- function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	44	48
	SOT5_0	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/LIN (operation modes 0, 1, 3).	43	47

# MB9A310K Series

Module	Pin name	Function	Pin No	
			LQFP-48 QFN-48	LQFP-52
Multi- function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	5	6
	DTTI0X_2		43	47
	FRCK0_2	16-bit free-run timer ch.0 external clock input pin	26	28
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0. ICxx describes channel number.	44	48
	IC00_2		27	29
	IC01_2		28	30
	IC02_0		26	28
	IC02_2		29	31
	IC03_2		30	32
	RTO00_0 (PPG00_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	6	7
	RTO01_0 (PPG00_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	7	8
	RTO02_0 (PPG02_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	8	9
	RTO03_0 (PPG02_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	9	10
	RTO04_0 (PPG04_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	10	11
RTO05_0 (PPG04_0)	Wave form generator output pin of multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	11	12	

# MB9A310K Series

Module	Pin name	Function	Pin No	
			LQFP-48 QFN-48	LQFP-52
Quadrature Position/ Revolution Counter 0	AIN0_2	QPRC ch.0 AIN input pin	2	2
	BIN0_2	QPRC ch.0 BIN input pin	3	3
	ZIN0_2	QPRC ch.0 ZIN input pin	4	4
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	42	46
	RTCCO_1		28	30
	RTCCO_2		6	7
	SUBOUT_0	Sub clock output pin	42	46
	SUBOUT_1		28	30
	SUBOUT_2		6	7
Low Power Consumption Mode	WKUP0	Deep stand-by mode return signal input pin 0	42	46
	WKUP1	Deep stand-by mode return signal input pin 1	26	28
	WKUP2	Deep stand-by mode return signal input pin 2	36	39
	WKUP3	Deep stand-by mode return signal input pin 3	44	48
USB	UDM0	USB ch.0 function/host D – pin	46	50
	UDP0	USB ch.0 function/host D + pin	47	51
	UHCONX	USB external pull-up control pin	43	47

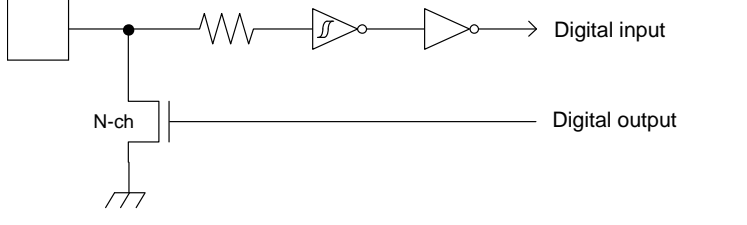
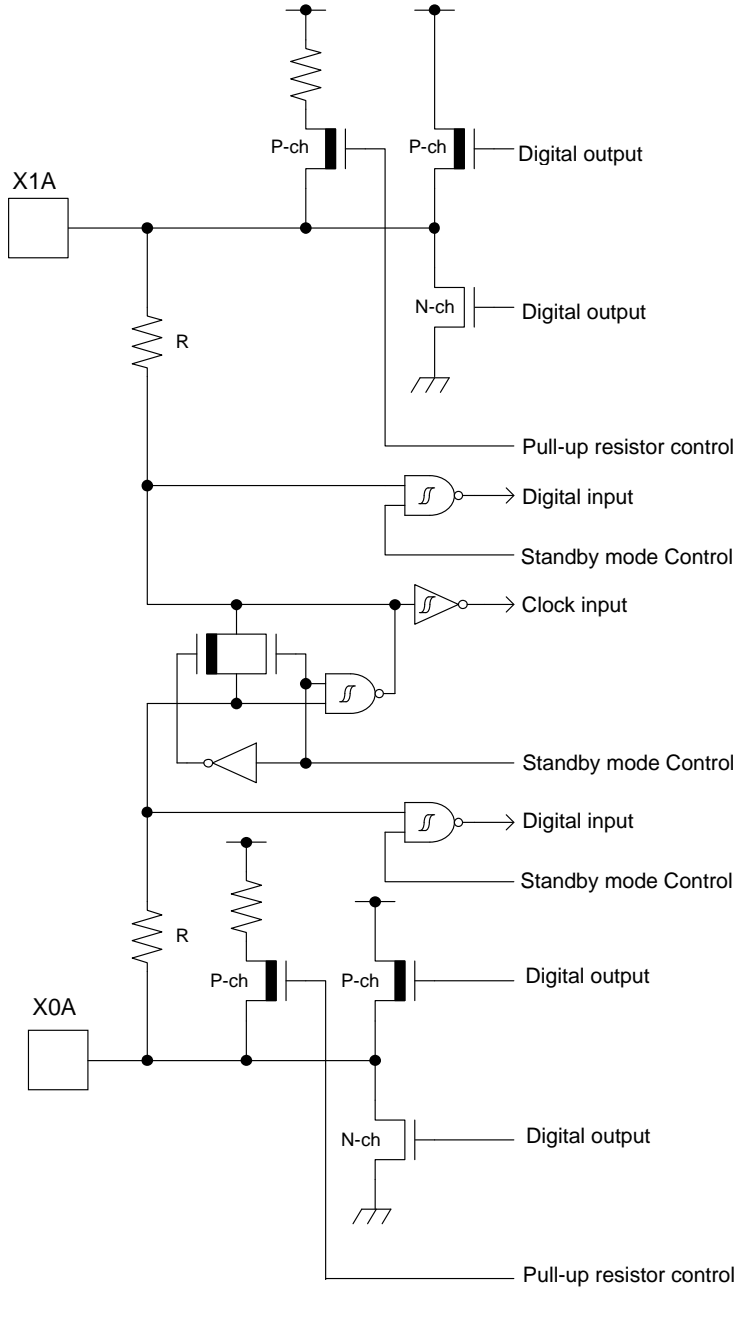
# MB9A310K Series

Module	Pin name	Function	Pin No	
			LQFP-48 QFN-48	LQFP-52
RESET	INITX	External Reset Input pin. A reset is valid when INITX="L".	17	18
Mode	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	21	23
	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	20	22
POWER	VCC	Power supply Pin	1	1
	VCC	Power supply Pin	14	15
	USBVCC	3.3V Power supply port for USB I/O	45	49
GND	VSS	GND Pin	12	13
	VSS	GND Pin	24	26
	VSS	GND Pin	48	52
CLOCK	X0	Main clock (oscillation) input pin	22	24
	X0A	Sub clock (oscillation) input pin	15	16
	X1	Main clock (oscillation) I/O pin	23	25
	X1A	Sub clock (oscillation) I/O pin	16	17
	CROUT_1	Internal CR-osc clock output port	42	46
ADC POWER	AVCC	A/D converter analog power pin	31	33
	AVRH	A/D converter analog reference voltage input pin	32	34
ADC GND	AVSS	A/D converter GND pin	33	35
C pin	C	Power stabilization capacity pin	13	14
NC pin	NC	NC pin. NC pin should be kept open.	-	5
	NC	NC pin. NC pin should be kept open.	-	21
	NC	NC pin. NC pin should be kept open.	-	36
	NC	NC pin. NC pin should be kept open.	-	40

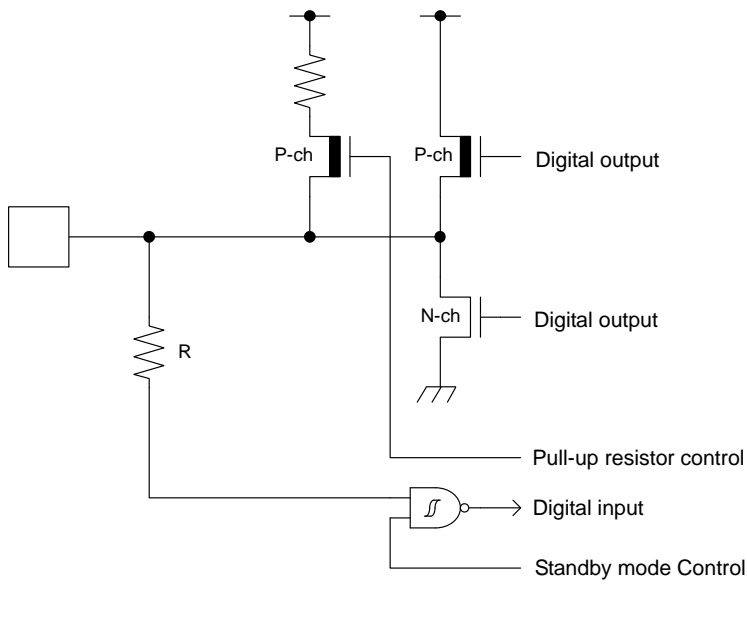
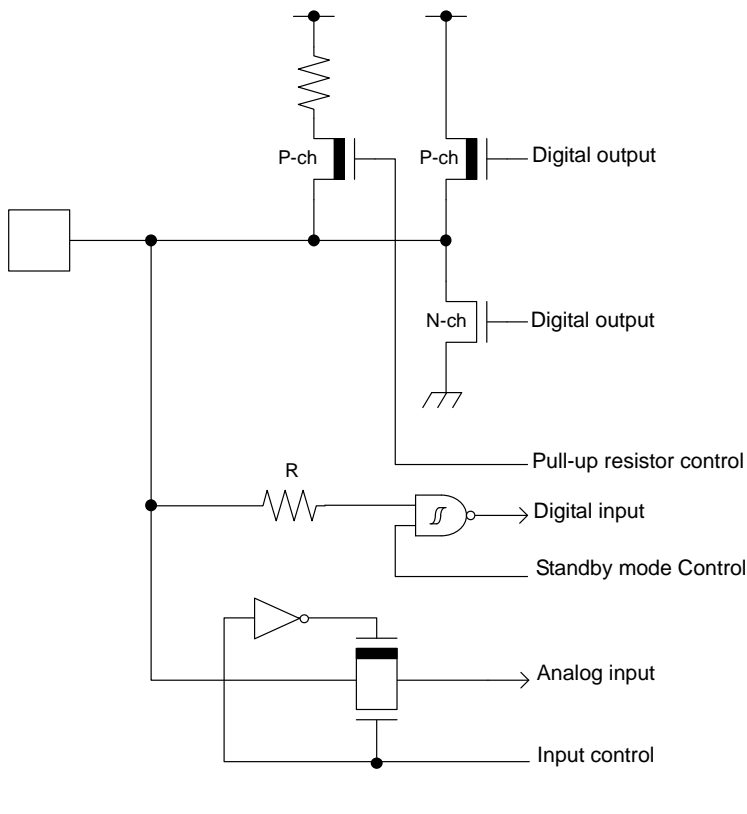
## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected.</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor : Approximately 1M<math>\Omega</math></li> <li>• With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50k<math>\Omega</math></li> <li>• I<sub>OH</sub>= -4mA, I<sub>OL</sub>= 4mA</li> </ul>
B		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> <li>• Pull-up resistor : Approximately 50k<math>\Omega</math></li> </ul>

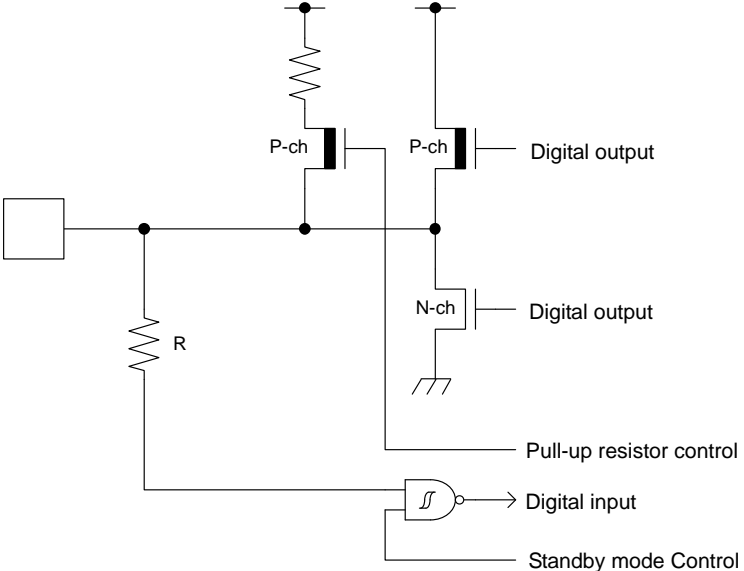
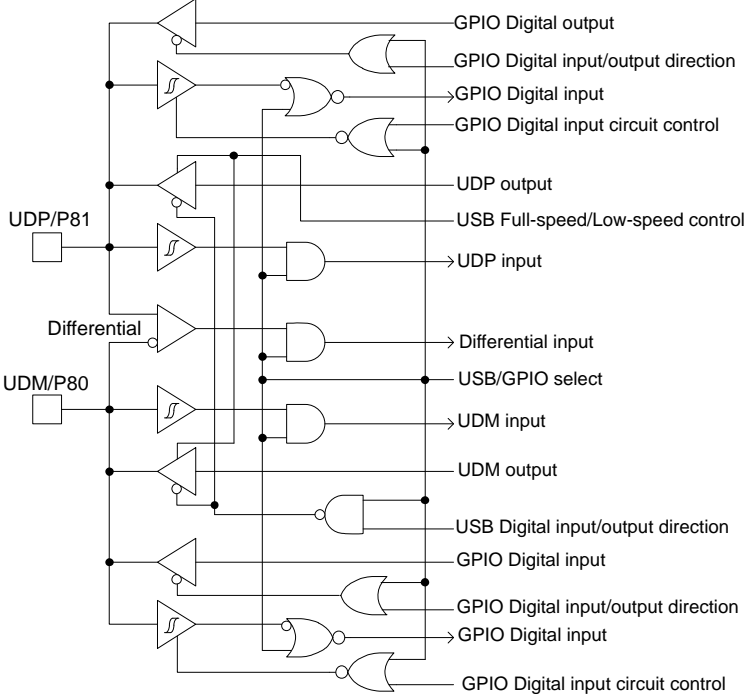
# MB9A310K Series

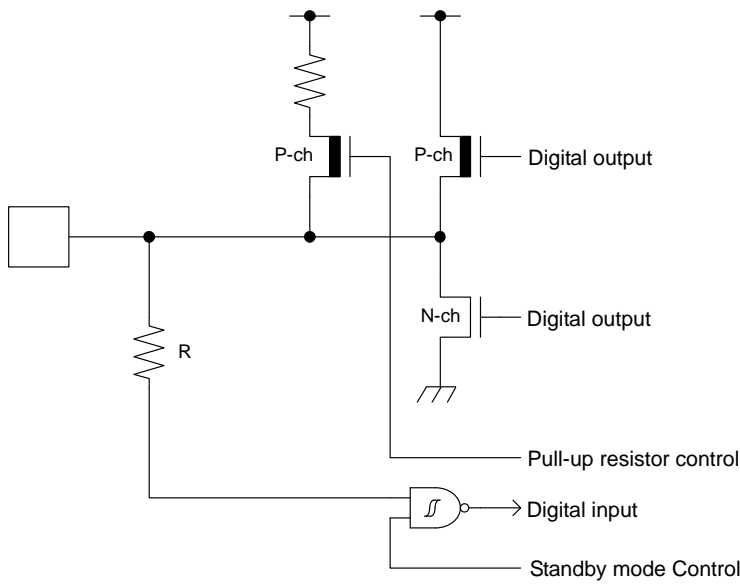
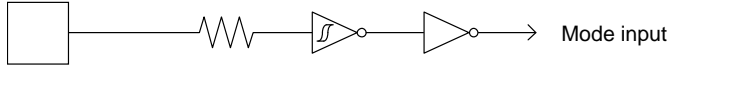
Type	Circuit	Remarks
C	 <p>The diagram shows a square box representing an open-drain output. A resistor is connected between this output and a digital input pin. An N-channel MOSFET is connected between the output and ground, with its gate also connected to the digital input pin.</p>	<ul style="list-style-type: none"> <li>• Open drain output</li> <li>• CMOS level hysteresis input</li> </ul>
D	 <p>The diagram illustrates two oscillator sections, X1A and X0A. Each oscillator consists of a crystal connected to a P-channel MOSFET (pull-up) and an N-channel MOSFET (pull-down). The X1A section includes a pull-up resistor R and a pull-up resistor control signal. The X0A section also includes a pull-up resistor R and a pull-up resistor control signal. Various digital inputs and outputs are shown, including digital inputs with hysteresis, digital outputs, and clock inputs. Standby mode control signals are also present, connected to various logic gates and MOSFET gates.</p>	<p>It is possible to select the sub oscillation / GPIO function</p> <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor : Approximately 5M<math>\Omega</math></li> <li>• With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output.</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50k<math>\Omega</math></li> <li>• I<sub>OH</sub>= -4mA, I<sub>OL</sub>= 4mA</li> </ul>



Type	Circuit	Remarks
E	 <p>The circuit diagram for Type E shows a CMOS output stage. A pull-up resistor R is connected to the output node. The output node is connected to a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-channel MOSFET is controlled by a digital input signal. The N-channel MOSFET is controlled by a standby mode control signal. The output node is also connected to a digital output terminal. A pull-up resistor control signal is also shown.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50kΩ</li> <li>• <math>I_{OH} = -4\text{mA}</math>, <math>I_{OL} = 4\text{mA}</math></li> </ul>
F	 <p>The circuit diagram for Type F shows a CMOS output stage similar to Type E, but with an additional analog input. A pull-up resistor R is connected to the output node. The output node is connected to a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-channel MOSFET is controlled by a digital input signal. The N-channel MOSFET is controlled by a standby mode control signal. The output node is also connected to a digital output terminal. A pull-up resistor control signal is also shown. An analog input signal is connected to the output node through an input control signal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50kΩ</li> <li>• <math>I_{OH} = -4\text{mA}</math>, <math>I_{OL} = 4\text{mA}</math></li> </ul>

# MB9A310K Series

Type	Circuit	Remarks
G	 <p>The diagram shows a CMOS output stage. A pull-up resistor 'R' is connected to the output node. The output node is driven by a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's gate is connected to a 'Pull-up resistor control' signal. The N-ch MOSFET's gate is connected to a 'Standby mode Control' signal. The output node is also connected to a 'Digital input' through an inverter. The output node is labeled 'Digital output'.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50kΩ</li> <li>• <math>I_{OH} = -12\text{mA}</math>, <math>I_{OL} = 12\text{mA}</math></li> </ul>
H	 <p>The diagram shows a complex digital I/O circuit. It includes several input and output pins: UDP/P81, Differential, UDM/P80, and GPIO Digital input/output direction. The circuit uses a combination of inverters, NAND gates, and OR gates to implement various functions. Labels include: GPIO Digital output, GPIO Digital input/output direction, GPIO Digital input, GPIO Digital input circuit control, UDP output, USB Full-speed/Low-speed control, UDP input, Differential input, USB/GPIO select, UDM input, UDM output, USB Digital input/output direction, and GPIO Digital input circuit control.</p>	<p>It is possible to select the USB I/O / GPIO function.</p> <p>When the USB I/O is selected.</p> <ul style="list-style-type: none"> <li>• Full-speed, Low-speed control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby mode control</li> <li><math>I_{OH} = -20.5\text{mA}</math>, <math>I_{OL} = 18.5\text{mA}</math></li> </ul>

Type	Circuit	Remarks
I	 <p>The diagram shows a CMOS output stage. A pull-up resistor R is connected to the output node. A pull-up resistor control input is connected to the gate of the P-channel MOSFET. A digital input is connected to the gate of the N-channel MOSFET. A standby mode control input is connected to the gate of the P-channel MOSFET. The output is labeled 'Digital output'.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5V tolerant</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 50kΩ</li> <li>• <math>I_{OH} = -4mA</math>, <math>I_{OL} = 4mA</math></li> <li>• Available to control of PZR registers.</li> </ul>
J	 <p>The diagram shows a CMOS level hysteresis input circuit. A resistor is connected to the input of the first inverter. The output of the first inverter is connected to the input of the second inverter. The output of the second inverter is labeled 'Mode input'.</p>	<p>CMOS level hysteresis input</p>

## ■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

### 1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### • Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### • Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### • Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

##### (1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

##### (2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

##### (3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation.

Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

#### • Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

**CAUTION:** The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

**CAUTION:** Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

# MB9A310K Series

- Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.  
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

Condition: 125°C/24 h

- Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).  
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

### 3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

#### (1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

#### (2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

#### (3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

#### (4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

#### (5) Smoke, Flame

**CAUTION:** Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

<http://edevice.fujitsu.com/fj/handling-e.pdf>

# MB9A310K Series

## ■ HANDLING DEVICES

- Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between each Power supply pins and GND pins near this device.

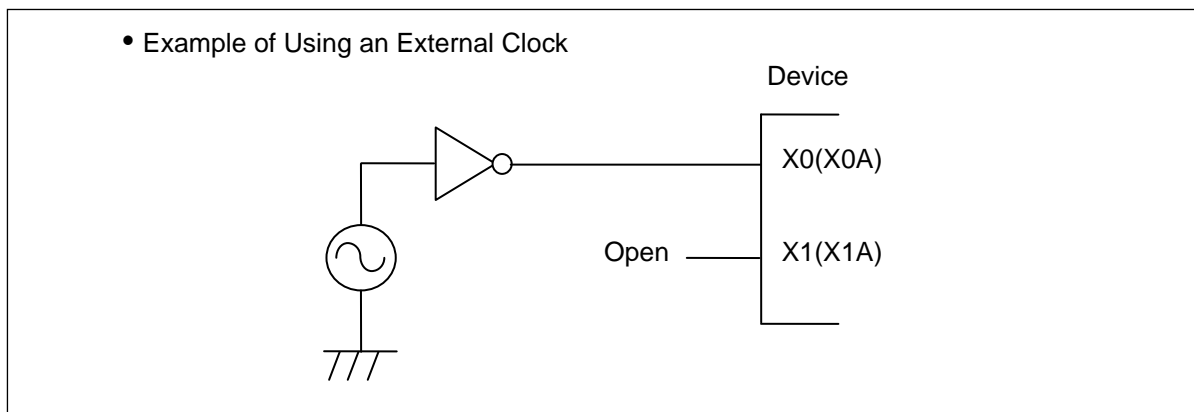
- Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

- Using an external clock

When using an external clock, the clock signal should be input to the X0, X0A pin only and the X1, X1A pin should be kept open.



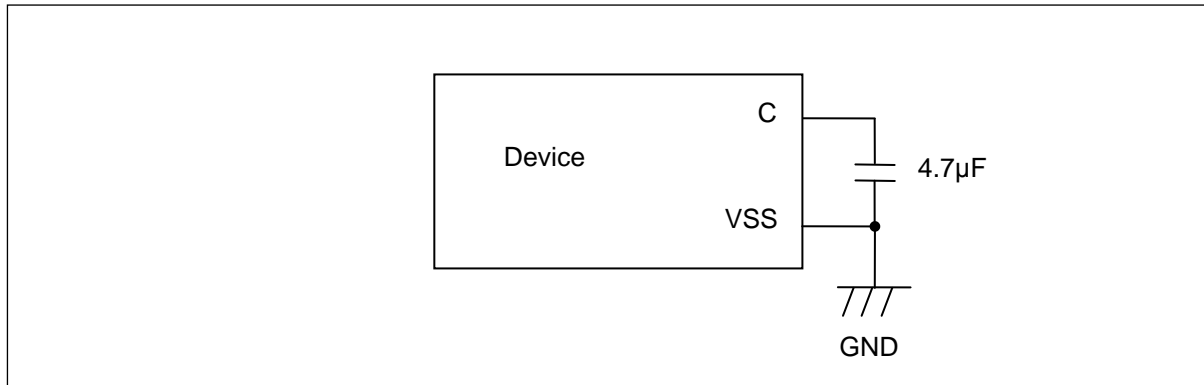
- Handling when using Multi-function serial pin as I<sup>2</sup>C pin

If it is using Multi-function serial pin as I<sup>2</sup>C pins, P-ch transistor of digital output is always disable. However, I<sup>2</sup>C pins need to keep the electrical characteristic like other pins and not to connect to external I<sup>2</sup>C bus system with power OFF.



- C pin

As this series includes an internal regulator, always connect a bypass capacitor of approximately 4.7  $\mu\text{F}$  to the C pin for use by the regulator.



- Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- NC pins

NC pin should be kept open.

- Notes on power-on

Turn power on/off in the following order or at the same time.

If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC  $\rightarrow$  USBVCC

VCC  $\rightarrow$  AVCC  $\rightarrow$  AVRH

Turning off : USBVCC  $\rightarrow$  VCC

AVRH  $\rightarrow$  AVCC  $\rightarrow$  VCC

- Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

- Differences in features among the products with different memory sizes and between Flash products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

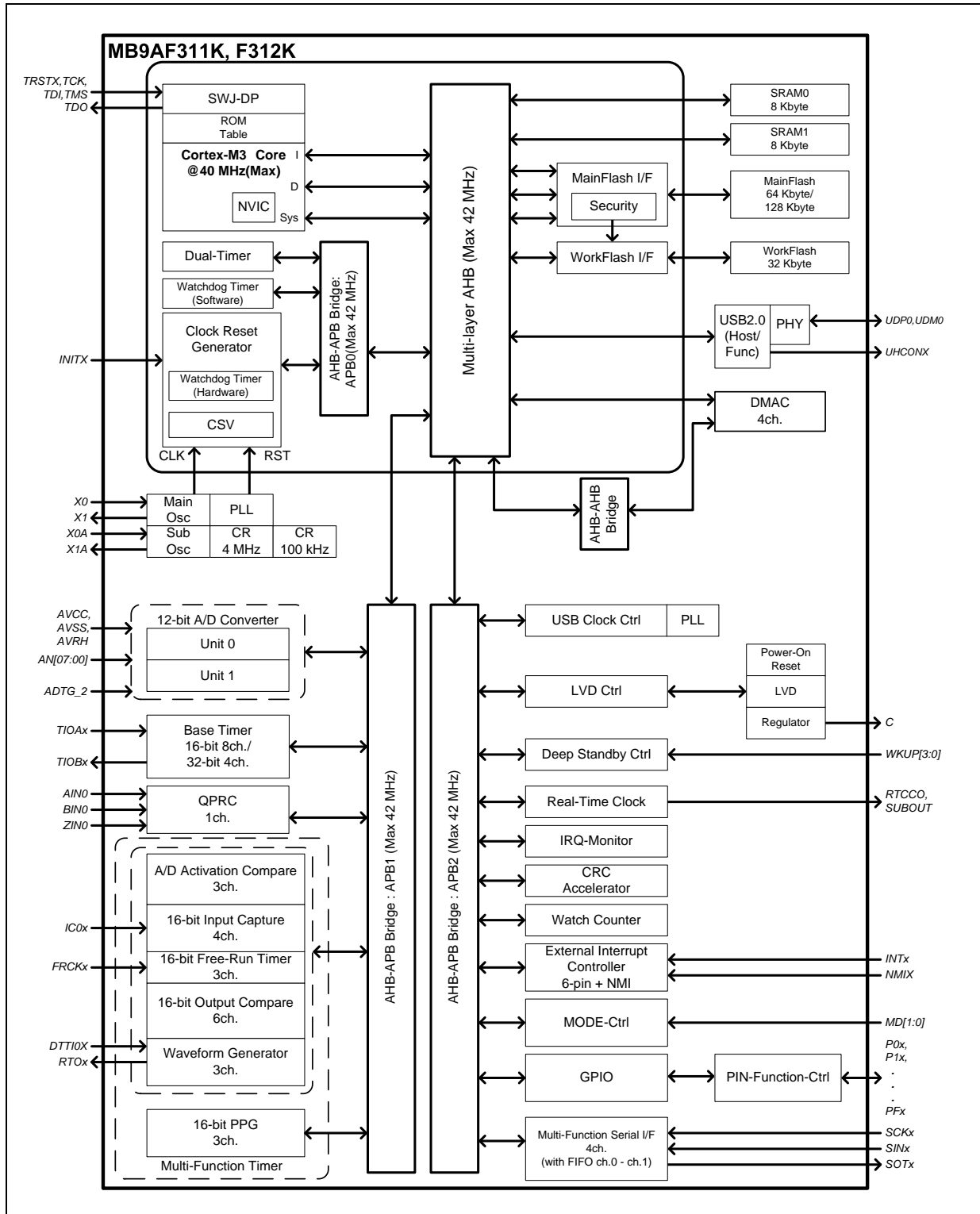
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

- Pull-Up function of 5V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5V tolerant I/O.

# MB9A310K Series

## ■ BLOCK DIAGRAM

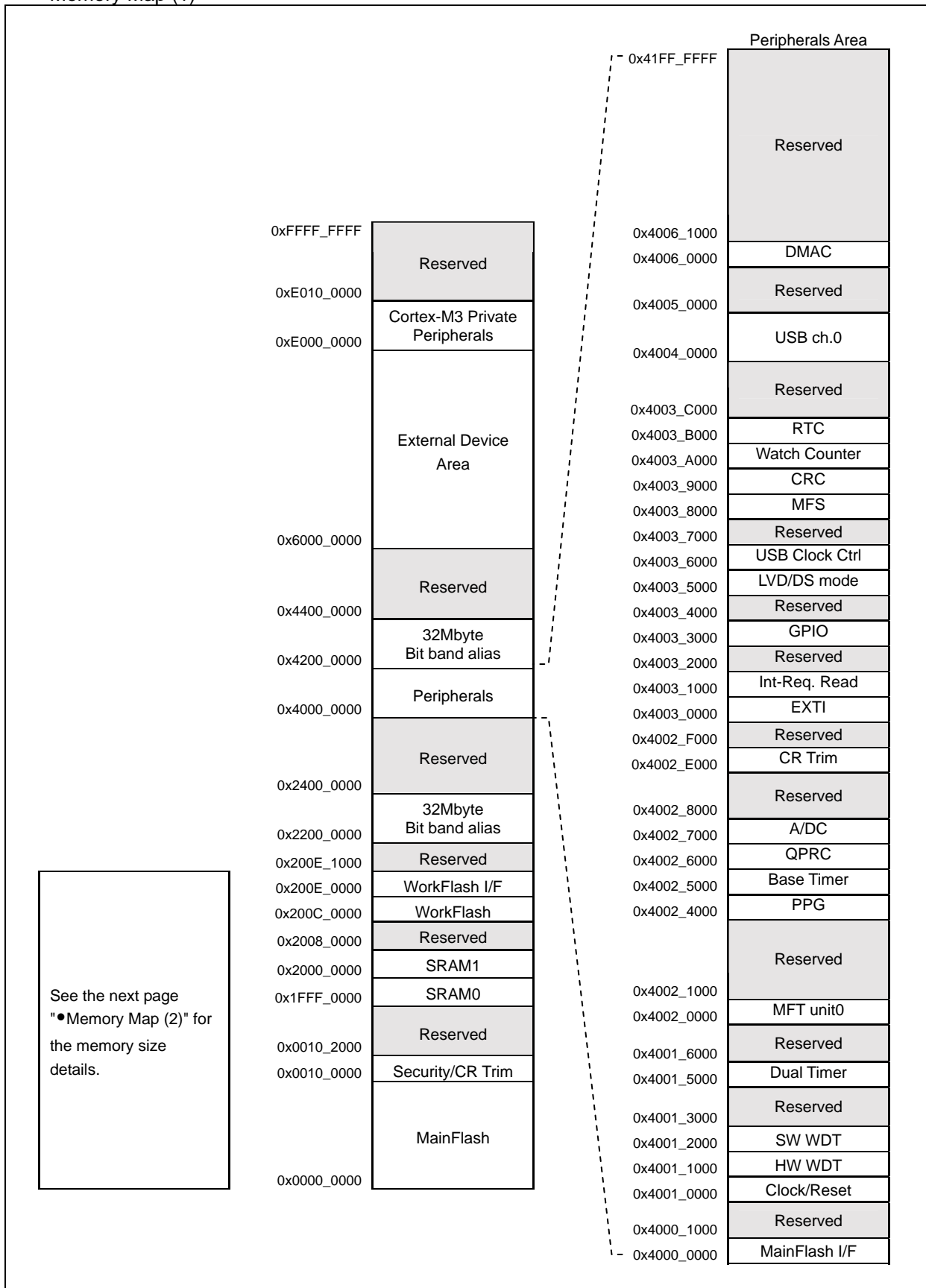


## ■ MEMORY SIZE

See "●Memory size" in "■PRODUCT LINEUP" to confirm the memory size.

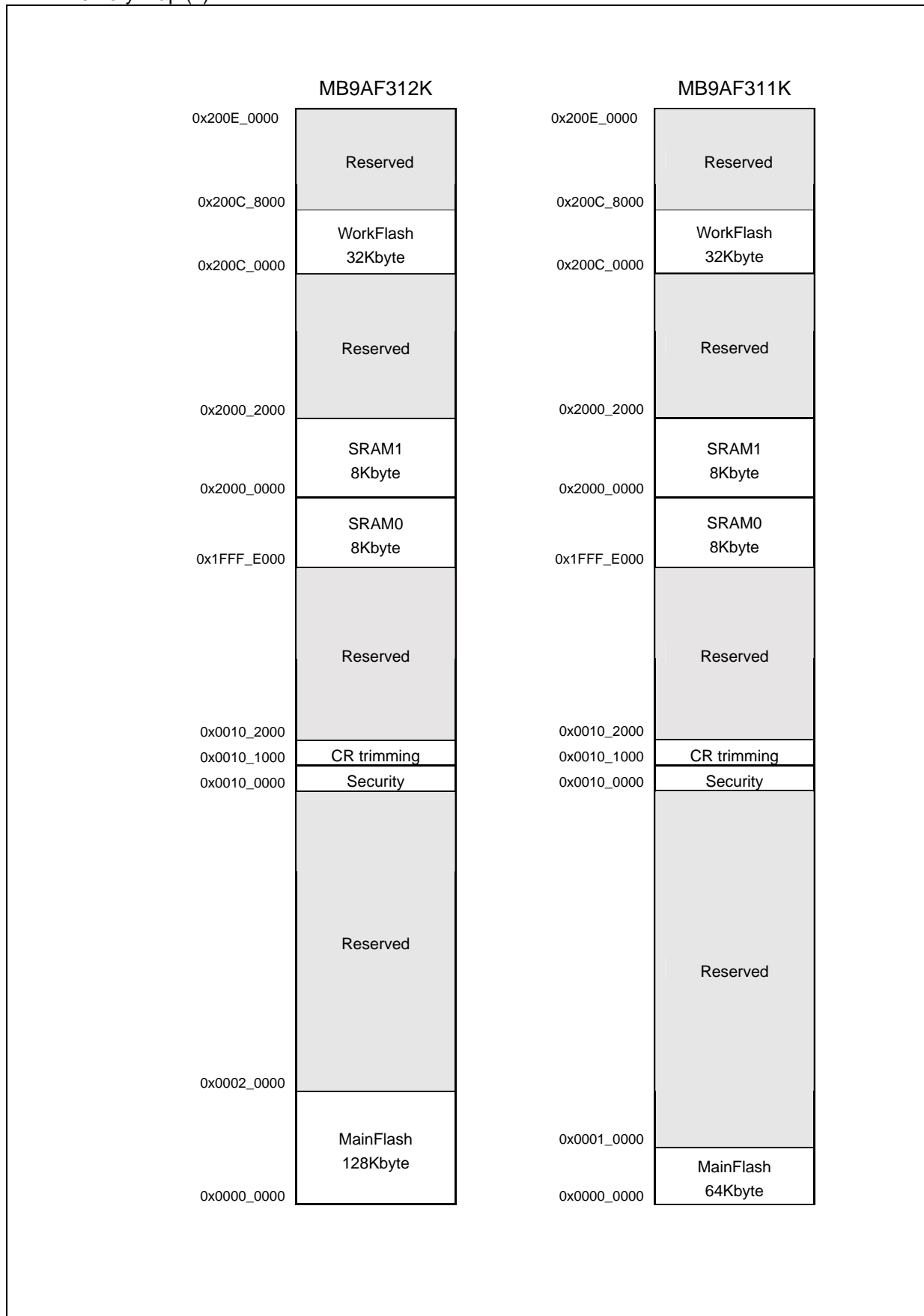
## ■ MEMORY MAP

### ● Memory Map (1)



# MB9A310K Series

- Memory Map (2)



# MB9A310K Series

## ● Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF		APB1
0x4002_1000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	PPG	
0x4002_5000	0x4002_5FFF	Base Timer	
0x4002_6000	0x4002_6FFF	Quadrature Position/Revolution Counter	
0x4002_7000	0x4002_7FFF	A/D Converter	
0x4002_8000	0x4002_DFFF	Reserved	
0x4002_E000	0x4002_EFFF	Internal CR trimming	
0x4002_F000	0x4002_FFFF	Reserved	
0x4003_0000	0x4003_0FFF	APB2	
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low-Voltage Detector
0x4003_5800	0x4003_5FFF		Deep stand-by mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF		AHB
0x4005_0000	0x4005_FFFF	Reserved	
0x4006_0000	0x4006_0FFF	DMAC register	
0x4006_1000	0x41FF_FFFF	Reserved	
0x200E_0000	0x200E_FFFF	WorkFlash I/F register	

## ■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- INITX=0  
This is the period when the INITX pin is the "L" level.
- INITX=1  
This is the period when the INITX pin is the "H" level.
- SPL=0  
This is the status that standby pin level setting bit (SPL) in standby mode control register (STB\_CTL) is set to "0".
- SPL=1  
This is the status that standby pin level setting bit (SPL) in standby mode control register (STB\_CTL) is set to "1".
- Input enabled  
Indicates that the input function can be used.
- Internal input fixed at "0"  
This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z  
Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled  
Indicates that the setting is disabled.
- Maintain previous state  
Maintains the state that was immediately prior to entering the current mode.  
If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.
- Analog input is enabled  
Indicates that the analog input is enabled.
- GPIO selected  
In Deep stand-by mode, pins switch to the general-purpose I/O port.

● List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or sleep mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0" / or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state / When oscillation stop*1, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z / Internal input fixed at "0"
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state

# MB9A310K Series

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or sleep mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
F	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
GPIO selected	Maintain previous state									
G	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected		Maintain previous state							
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected		Maintain previous state							
I	resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected		Maintain previous state							



# MB9A310K Series

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or sleep mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-	
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"				Maintain previous state
	GPIO selected						Maintain previous state				
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	
	Resource other than above selected		Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected							Maintain previous state			
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	
	External interrupt enabled selected		Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected							Hi-Z / Internal input fixed at "0"			
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	
M	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	

# MB9A310K Series

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or sleep mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0" / or Input enable	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state / When oscillation stop*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*2, Hi-Z / Internal input fixed at "0"
O	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Hi-Z at transmission / Input enabled / Internal input fixed at "0" at reception	Hi-Z at transmission / Input enabled / Internal input fixed at "0" at reception	Hi-Z / Input enabled	Hi-Z / Input enabled	Hi-Z / Input enabled
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	Maintain previous state	Hi-Z / Input enabled	Maintain previous state

\*1 : Oscillation is stopped at Sub timer mode, Low-speed CR timer mode, RTC mode, STOP mode, Deep stand-by RTC mode, and Deep stand-by STOP mode.

\*2 : Oscillation is stopped at STOP mode and Deep stand-by STOP mode.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Power supply voltage (for USB) *1, *3	USBV <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Analog power supply voltage *1, *4	AV <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Analog reference voltage *1, *4	AV <sub>RH</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Input voltage	V <sub>I</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤6.5V)	V	Except for USB pin
		V <sub>SS</sub> - 0.5	USBV <sub>CC</sub> + 0.5 (≤6.5V)	V	USB pin
		V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	5V tolerant
Analog pin input voltage	V <sub>IA</sub>	V <sub>SS</sub> - 0.5	AV <sub>CC</sub> + 0.5 (≤6.5V)	V	
Output voltage	V <sub>O</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤6.5V)	V	
"L" level maximum output current *5	I <sub>OL</sub>	-	10	mA	4mA type
			20	mA	12mA type
"L" level average output current *6	I <sub>OLAV</sub>	-	4	mA	4mA type
			12	mA	12mA type
"L" level total maximum output current	∑I <sub>OL</sub>	-	100	mA	
"L" level total average output current *7	∑I <sub>OLAV</sub>	-	50	mA	
"H" level maximum output current *5	I <sub>OH</sub>	-	- 10	mA	4mA type
			- 20	mA	12mA type
"H" level average output current *6	I <sub>OHAV</sub>	-	- 4	mA	4mA type
			- 12	mA	12mA type
"H" level total maximum output current	∑I <sub>OH</sub>	-	- 100	mA	
"H" level total average output current *7	∑I <sub>OHAV</sub>	-	- 50	mA	
Power consumption	P <sub>D</sub>	-	300	mW	
Storage temperature	T <sub>STG</sub>	- 55	+ 150	°C	

\*1 : These parameters are based on the condition that V<sub>SS</sub> = AV<sub>SS</sub> = 0.0V.

\*2 : V<sub>CC</sub> must not drop below V<sub>SS</sub> - 0.5V.

\*3 : USBV<sub>CC</sub> must not drop below V<sub>SS</sub> - 0.5V.

\*4 : Ensure that the voltage does not to exceed V<sub>CC</sub> + 0.5 V, for example, when the power is turned on.

\*5 : The maximum output current is the peak value for a single pin.

\*6 : The average output is the average current for a single pin over a period of 100 ms.

\*7 : The total average output current is the average current for all pins over a period of 100 ms.

### <WARNING>

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB9A310K Series

## 2. Recommended Operating Conditions

(V<sub>SS</sub> = AV<sub>SS</sub> = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V <sub>CC</sub>	-	2.7	5.5	V	
Power supply voltage for USB	USBV <sub>CC</sub>	-	3.0	3.6 (≤V <sub>CC</sub> )	V	*1
			2.7	5.5 (≤V <sub>CC</sub> )		*2
Analog power supply voltage	AV <sub>CC</sub>	-	2.7	5.5	V	AV <sub>CC</sub> =V <sub>CC</sub>
Analog reference voltage	AVRH	-	AV <sub>SS</sub>	AV <sub>CC</sub>	V	
Operating temperature	T <sub>a</sub>	-	- 40	+ 105	°C	

\*1: When P81/UDP0 and P80/UDM0 pin are used as USB (UDP0, UDM0).

\*2: When P81/UDP0 and P80/UDM0 pin are used as GPIO (P81, P80).

### <WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

### 3. DC Characteristics

#### (1) Current Rating

(V<sub>cc</sub> = AV<sub>cc</sub> = 2.7V to 5.5V, USBV<sub>cc</sub> = 3.0V to 3.6V, V<sub>ss</sub> = AV<sub>ss</sub> = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I <sub>cc</sub>	VCC	Normal operation (PLL)	-	32	41	mA	CPU : 40MHz, Peripheral : 40MHz, MainFlash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
				-	21	28	mA	CPU : 40MHz, Peripheral : 40MHz, MainFlash 3Wait FRWTR.RWT = 00 FSYNDN.SD = 011 *1
			Normal operation (high-speed internal CR)	-	3.9	7.7	mA	CPU/Peripheral : 4MHz *1, *2 MainFlash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000
			Normal operation (sub oscillation)	-	0.15	3.2	mA	CPU/Peripheral : 32kHz MainFlash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
			Normal operation (low-speed internal CR)	-	0.2	3.3	mA	CPU/Peripheral : 100kHz Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
			SLEEP operation (PLL)	-	10	15	mA	Peripheral : 40MHz *1
	I <sub>ccs</sub>	VCC	SLEEP operation (high-speed internal CR)	-	1.2	4.4	mA	Peripheral : 4MHz *1, *2
			SLEEP operation (sub oscillation)	-	0.1	3.1	mA	Peripheral : 32kHz *1
			SLEEP operation (low-speed internal CR)	-	0.1	3.1	mA	Peripheral : 100kHz *1
			STOP mode	-	35	200	μA	Ta = + 25°C, When LVD is off *1
	I <sub>cch</sub>	VCC	STOP mode	-	-	3	mA	Ta = + 105°C, When LVD is off *1
			TIMER mode (sub oscillation)	-	60	230	μA	Ta = + 25°C, When LVD is off *1
	I <sub>cct</sub>	VCC	TIMER mode (sub oscillation)	-	-	3.1	mA	Ta = + 105°C, When LVD is off *1

# MB9A310K Series

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks	
				Min	Typ	Max			
Power supply current	I <sub>CCR</sub>	VCC	RTC mode	-	50	210	μA	Ta = + 25°C, When LVD is off *1, *3	
				-	-	3.1	μA	Ta = + 105°C, When LVD is off *1, *3	
	I <sub>CHD</sub>		Deep stand-by STOP mode	-	20	150	μA	Ta = + 25°C, When LVD is off RAM hold off *1, *4	
				-	23	150	μA	Ta = + 25°C, When LVD is off RAM hold on *1, *4	
			-	-	-	-	600	μA	Ta = + 105°C, When LVD is off RAM hold off *1, *4
					-	-	610	μA	Ta = + 105°C, When LVD is off RAM hold on *1, *4
	I <sub>CRD</sub>		Deep stand-by RTC mode	-	-	30	160	μA	Ta = + 25°C, When LVD is off RAM hold off *1, *3, *4
					-	33	160	μA	Ta = + 25°C, When LVD is off RAM hold on *1, *3, *4
			-	-	-	-	600	μA	Ta = + 105°C, When LVD is off RAM hold off *1, *3, *4
					-	-	610	μA	Ta = + 105°C, When LVD is off RAM hold on *1, *3, *4
Low-voltage detection circuit (LVD) power supply current	I <sub>CCLVD</sub>		At operation	-	4	7	μA	For occurrence of interrupt	

\*1: When all ports are fixed.

\*2: When setting it to 4MHz by trimming.

\*3: When using sub crystal oscillator.

\*4: RAM hold setting is on-chip SRAM only.

# MB9A310K Series

## (2) Pin Characteristics

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_a = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	$V_{IHS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
		5V tolerant input pin	-	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
"L" level input voltage (hysteresis input)	$V_{ILS}$	CMOS hysteresis input pin, MD0, MD1	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		5V tolerant input pin	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
"H" level output voltage	$V_{OH}$	4mA type	$V_{CC} \geq 4.5 V$ $I_{OH} = -4mA$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -2mA$					
		12mA type	$V_{CC} \geq 4.5 V$ $I_{OH} = -12mA$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -8mA$					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5 V$ $I_{OH} = -20.5 mA$	$USBV_{CC} - 0.4$	-	$USBV_{CC}$	V	
			$USBV_{CC} < 4.5 V$ $I_{OH} = -13.0 mA$					

# MB9A310K Series

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	$V_{OL}$	4mA type	$V_{CC} \geq 4.5\text{ V}$ $I_{OL} = 4\text{ mA}$	$V_{SS}$	-	0.4	V	
			$V_{CC} < 4.5\text{ V}$ $I_{OL} = 2\text{ mA}$					
		12mA type	$V_{CC} \geq 4.5\text{ V}$ $I_{OL} = 12\text{ mA}$	$V_{SS}$	-	0.4	V	
			$V_{CC} < 4.5\text{ V}$ $I_{OL} = 8\text{ mA}$					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5\text{ V}$ $I_{OL} = 18.5\text{ mA}$	$V_{SS}$	-	0.4	V	
			$USBV_{CC} < 4.5\text{ V}$ $I_{OL} = 10.5\text{ mA}$					
Input leak current	$I_{IL}$	-	-	- 5	-	+ 5	$\mu\text{A}$	
Pull-up resistance value	$R_{PU}$	Pull-up pin	$V_{CC} \geq 4.5\text{ V}$	25	50	100	$\text{k}\Omega$	
			$V_{CC} < 4.5\text{ V}$	30	80	200		
Input capacitance	$C_{IN}$	Other than VCC, USBVCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	



## 4. AC Characteristics

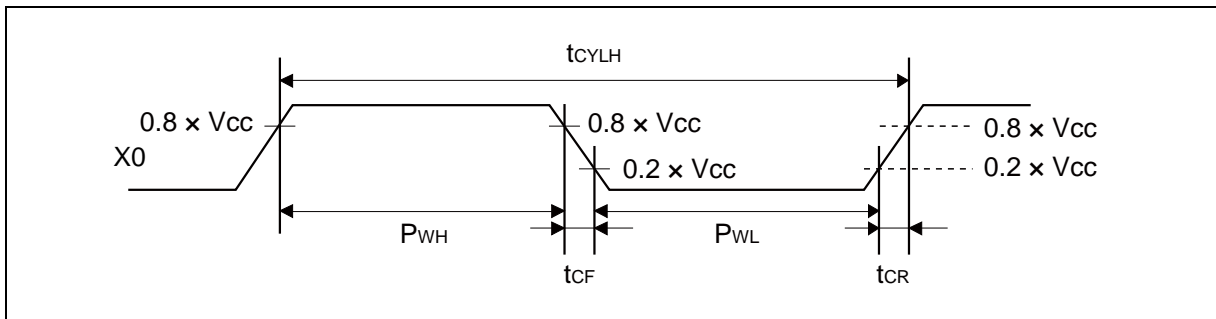
### (1) Main Clock Input Characteristics

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F <sub>CH</sub>	X0 X1	V <sub>CC</sub> ≥ 4.5V	4	48	MHz	When crystal oscillator is connected
			V <sub>CC</sub> < 4.5V	4	20		
			V <sub>CC</sub> ≥ 4.5V	4	48	MHz	
			V <sub>CC</sub> < 4.5V	4	20		
Input clock cycle	t <sub>CY LH</sub>		V <sub>CC</sub> ≥ 4.5V	20.83	250	ns	When using external clock
			V <sub>CC</sub> < 4.5V	50	250		
Input clock pulse width	-		P <sub>WH</sub> /t <sub>CY LH</sub>	45	55	%	When using external clock
			P <sub>WL</sub> /t <sub>CY LH</sub>				
Input clock rise time and fall time	t <sub>CF</sub> , t <sub>CR</sub>	-	-	5	ns	When using external clock	
Internal operating clock frequency* <sup>1</sup>	F <sub>CC</sub>	-	-	-	42	MHz	Base clock (HCLK/FCLK)
	F <sub>CP0</sub>	-	-	-	42	MHz	APB0 bus clock* <sup>2</sup>
	F <sub>CP1</sub>	-	-	-	42	MHz	APB1 bus clock* <sup>2</sup>
	F <sub>CP2</sub>	-	-	-	42	MHz	APB2 bus clock* <sup>2</sup>
Internal operating clock cycle time* <sup>1</sup>	t <sub>CYCC</sub>	-	-	23.8	-	ns	Base clock (HCLK/FCLK)
	t <sub>CYCP0</sub>	-	-	23.8	-	ns	APB0 bus clock* <sup>2</sup>
	t <sub>CYCP1</sub>	-	-	23.8	-	ns	APB1 bus clock* <sup>2</sup>
	t <sub>CYCP2</sub>	-	-	23.8	-	ns	APB2 bus clock* <sup>2</sup>

\*1: For more information about each internal operating clock, see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

\*2: For about each APB bus which each peripheral is connected to, see "■ BLOCK DIAGRAM" in this data sheet.

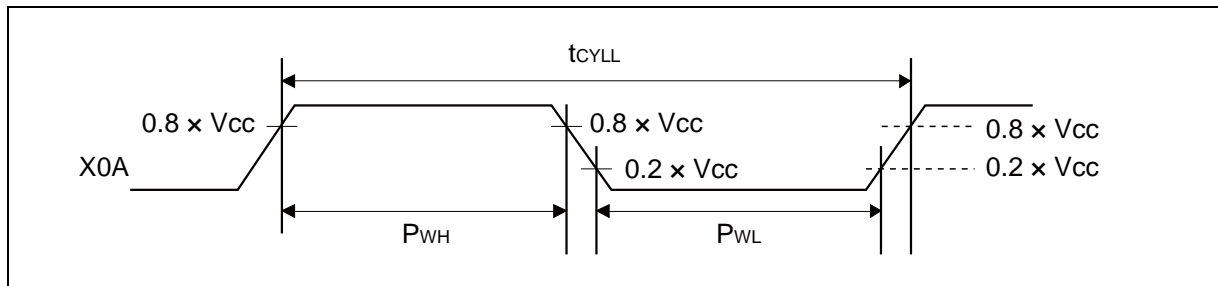


# MB9A310K Series

## (2) Sub Clock Input Characteristics

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t <sub>CYLL</sub>	X0A X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100		kHz
Input clock cycle	t <sub>CYLL</sub>		-	10	-	31.25	μs	When using external clock
Input clock pulse width	-		P <sub>WH</sub> /t <sub>CYLL</sub> P <sub>WL</sub> /t <sub>CYLL</sub>	45	-	55	%	When using external clock



## (3) Internal CR Oscillation Characteristics

- High-speed Internal CR

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F <sub>CRH</sub>	T <sub>a</sub> = + 25°C	3.96	4	4.04	MHz	When trimming*
		T <sub>a</sub> = 0°C to + 70°C	3.84	4	4.16		
		T <sub>a</sub> = - 40°C to + 85°C	3.8	4	4.2		
		T <sub>a</sub> = - 40°C to + 85°C	3	4	5		When not trimming

\*: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

- Low-speed Internal CR

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F <sub>CRL</sub>	-	50	100	150	kHz	

(4-1) Operating Conditions of Main and USB PLL (In the case of using main clock for input of PLL)  
 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* (LOCK UP time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	F <sub>PLLI</sub>	4	-	16	MHz	
PLL multiple rate	-	13	-	75	multiple	
PLL macro oscillation clock frequency	F <sub>PLLO</sub>	200	-	300	MHz	

\*: Time from when the PLL starts operating until the oscillation stabilizes.

(4-2) Operating Conditions of Main PLL (In the case of using high-speed internal CR)  
 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* (LOCK UP time)	t <sub>LOCK</sub>	100	-	-	μs	
PLL input clock frequency	F <sub>PLLI</sub>	3.8	4	4.2	MHz	
PLL multiple rate	-	50	-	71	multiple	
PLL macro oscillation clock frequency	F <sub>PLLO</sub>	190	-	300	MHz	

\*: Time from when the PLL starts operating until the oscillation stabilizes.

Note : It needs to input to PLL by internal CR trimming frequency.

(5) Reset Input Characteristics

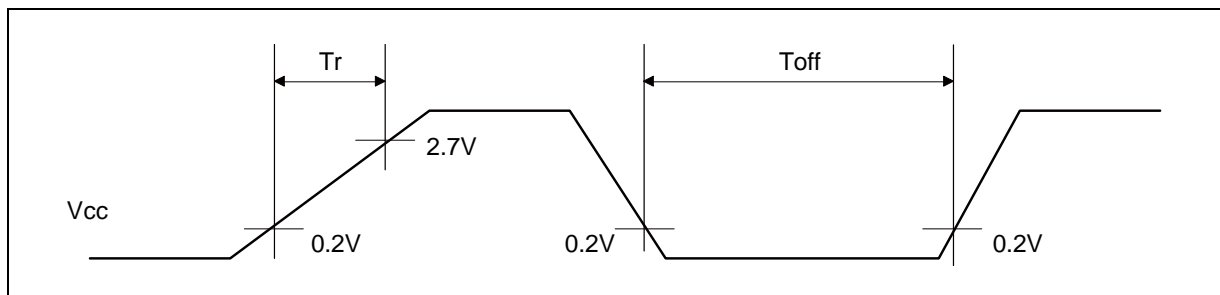
(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t <sub>INITX</sub>	INITX	-	500	-	ns	

(6) Power-on Reset Timing

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	VCC	0	-	ms	
Power supply shut down time	Toff		1	-	ms	



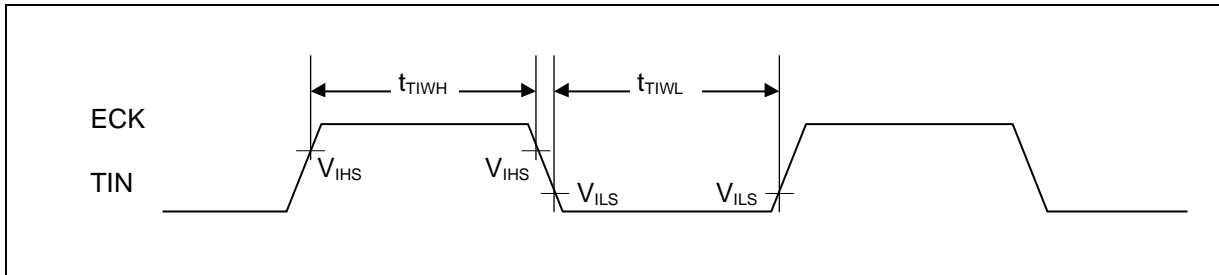
# MB9A310K Series

## (7) Base Timer Input Timing

- Timer input timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40^{\circ}C$  to  $+105^{\circ}C$ )

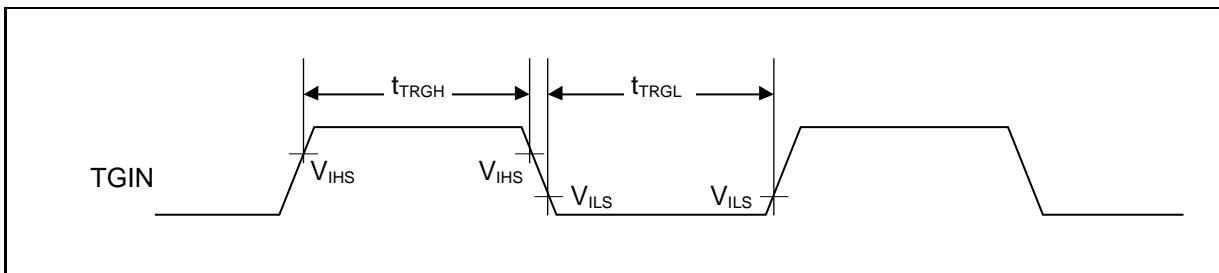
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ $t_{TIWL}$	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



- Trigger input timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ $t_{TRGL}$	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:  $t_{CYCP}$  indicates the APB bus clock cycle time.

About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.

## (8) UART Timing

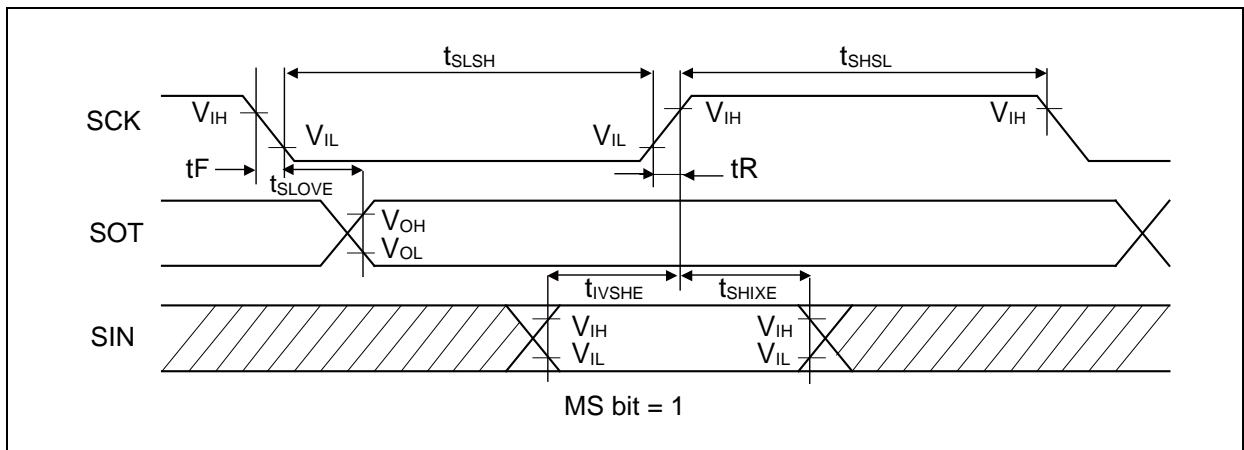
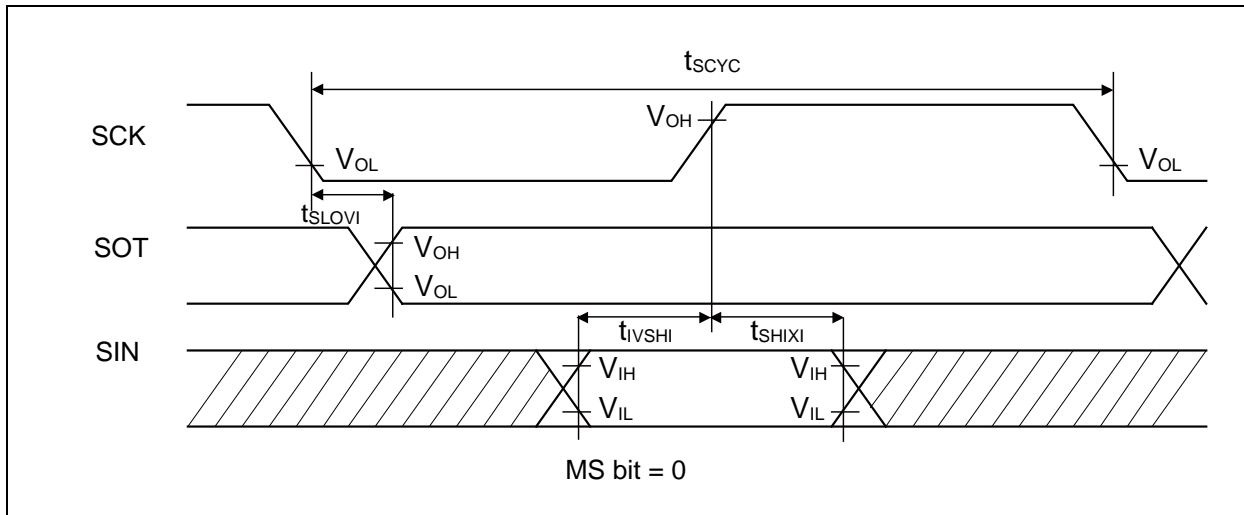
- Synchronous serial (SPI = 0, SCINV = 0)

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 4.5V		V <sub>CC</sub> ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK <sub>X</sub>	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↓ → SOT delay time	t <sub>SLOVI</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t <sub>IVSHI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		50	-	30	-	ns
SCK ↑ → SIN hold time	t <sub>SHIXI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		0	-	0	-	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCK <sub>X</sub>	External shift clock operation	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK <sub>X</sub>		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ → SOT delay time	t <sub>SLOVE</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		-	50	-	30	ns
SIN → SCK ↑ setup time	t <sub>IVSHE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		10	-	10	-	ns
SCK ↑ → SIN hold time	t <sub>SHIXE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCK <sub>X</sub>		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCK <sub>X</sub>		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
  - t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
  - These characteristics only guarantee the same relocate port number.  
For example, the combination of SCLK<sub>x\_0</sub> and SOT<sub>x\_1</sub> is not guaranteed.
  - When the external load capacitance = 30pF.

# MB9A310K Series



# MB9A310K Series

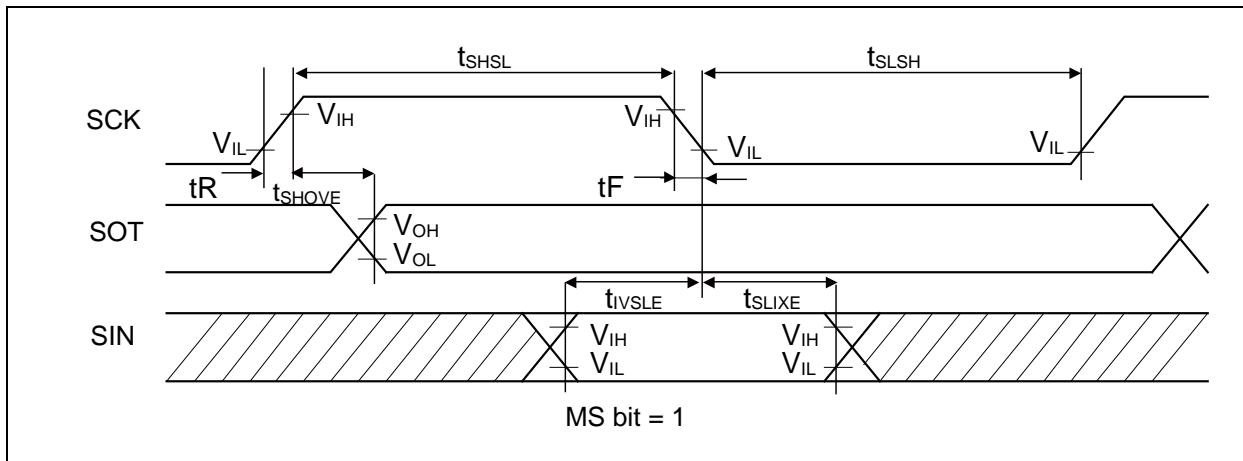
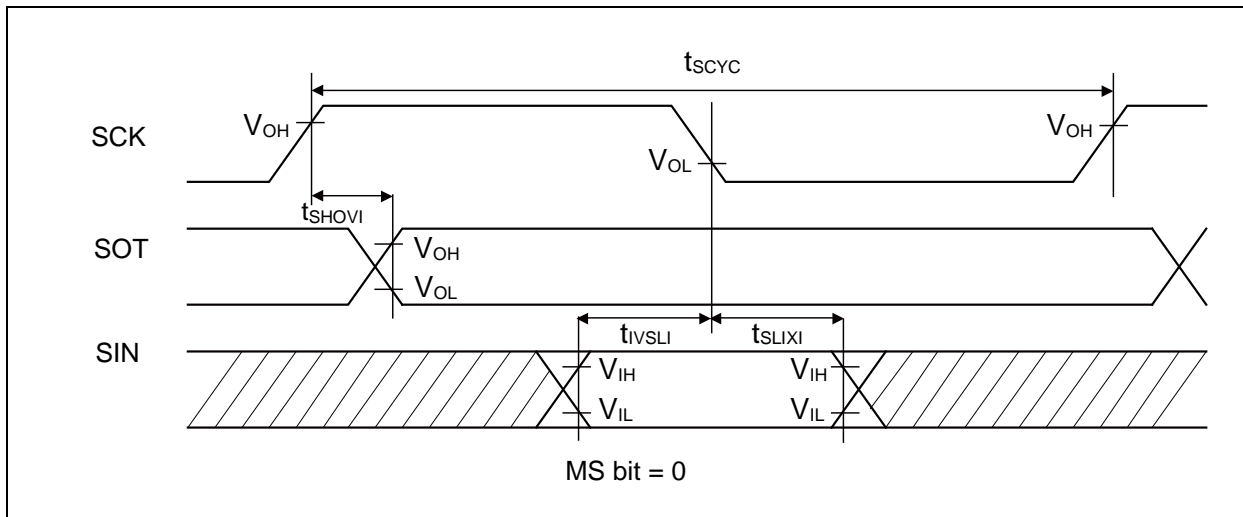
- Synchronous serial (SPI = 0, SCINV = 1)

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 4.5V		V <sub>CC</sub> ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK <sub>X</sub>	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t <sub>IVSLI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		50	-	30	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		0	-	0	-	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCK <sub>X</sub>	External shift clock operation	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK <sub>X</sub>		tcycp + 10	-	tcycp + 10	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		-	50	-	30	ns
SIN → SCK ↓ setup time	t <sub>IVSLE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		10	-	10	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCK <sub>X</sub>		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCK <sub>X</sub>		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
  - t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
  - These characteristics only guarantee the same relocate port number.  
For example, the combination of SCLK<sub>x\_0</sub> and SOT<sub>x\_1</sub> is not guaranteed.
  - When the external load capacitance = 30pF.

# MB9A310K Series





# MB9A310K Series

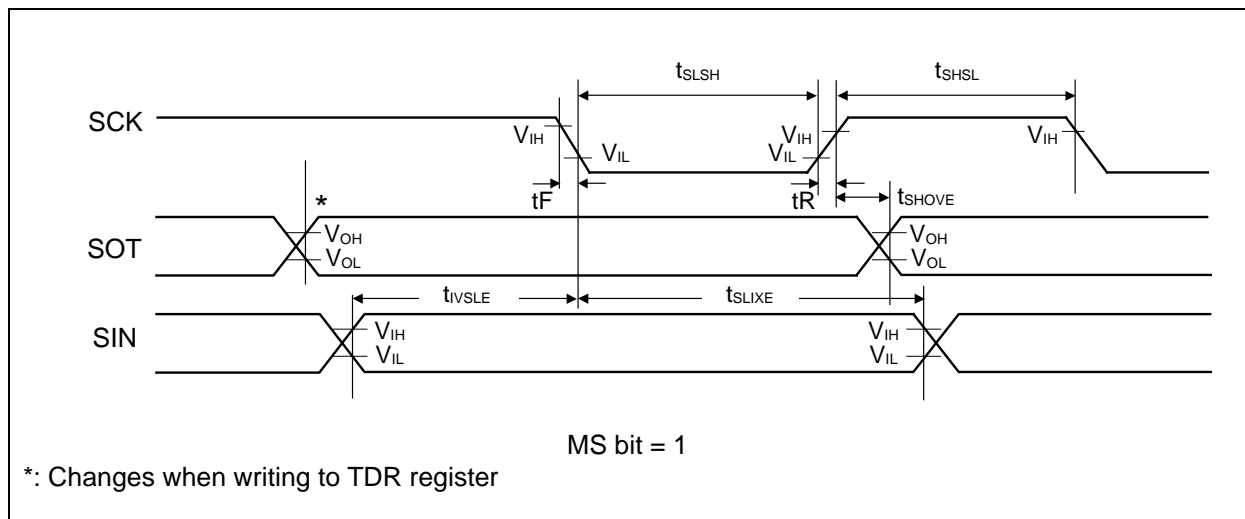
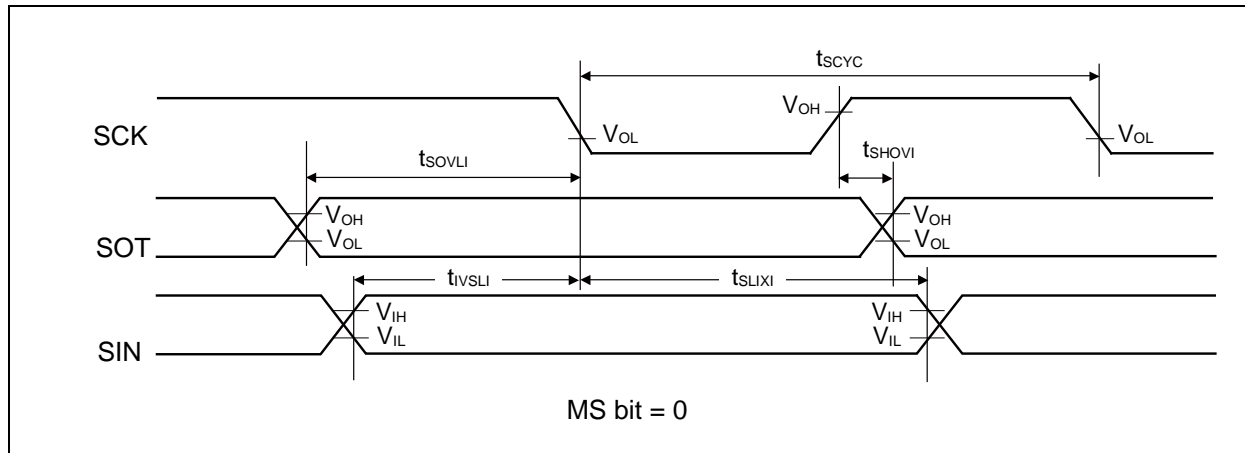
- Synchronous serial (SPI = 1, SCINV = 0)

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 4.5V		V <sub>CC</sub> ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK <sub>X</sub>	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t <sub>IVSLI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		50	-	30	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		0	-	0	-	ns
SOT → SCK ↓ delay time	t <sub>SOVLI</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCK <sub>X</sub>		2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK <sub>X</sub>	tcycp + 10	-	tcycp + 10	-	ns	
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCK <sub>X</sub> SOT <sub>X</sub>	External shift clock operation	-	50	-	30	ns
SIN → SCK ↓ setup time	t <sub>IVSLE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		10	-	10	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCK <sub>X</sub>		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCK <sub>X</sub>		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
  - t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
  - These characteristics only guarantee the same relocate port number.  
For example, the combination of SCLK<sub>X\_0</sub> and SOT<sub>X\_1</sub> is not guaranteed.
  - When the external load capacitance = 30pF.

# MB9A310K Series



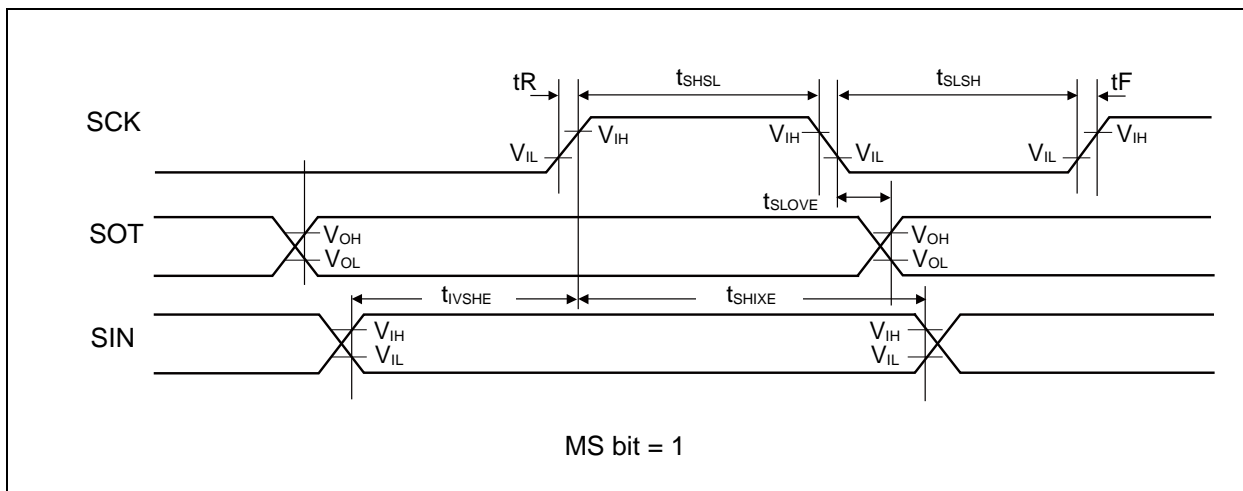
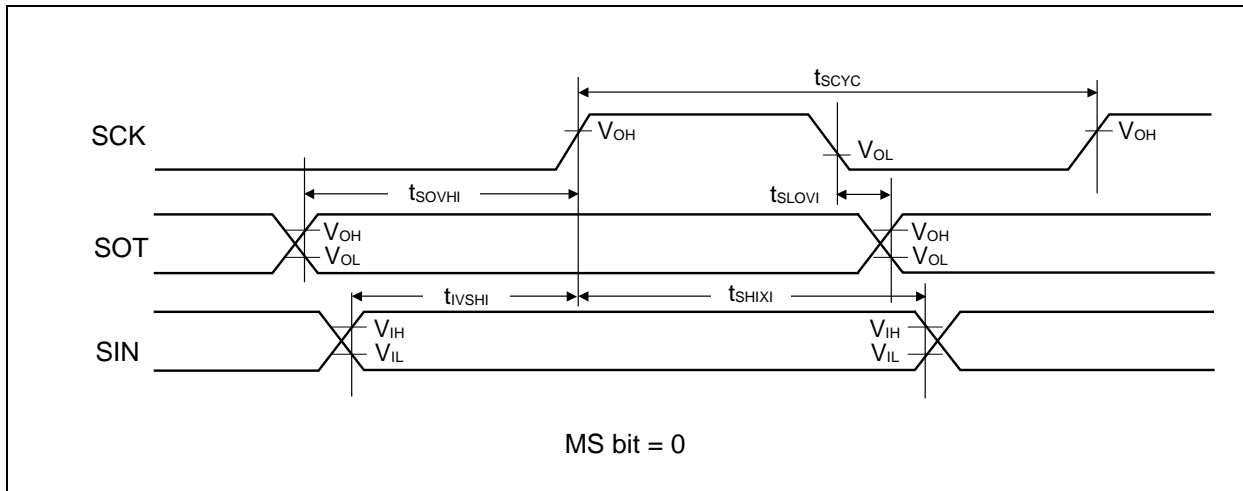
- Synchronous serial (SPI = 1, SCINV = 1)

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	V <sub>CC</sub> < 4.5V		V <sub>CC</sub> ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK <sub>X</sub>	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↓ → SOT delay time	t <sub>SLOVI</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	t <sub>IVSHI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		50	-	30	-	ns
SCK ↑ → SIN hold time	t <sub>SHIXI</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		0	-	0	-	ns
SOT → SCK ↑ delay time	t <sub>SOVHI</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCK <sub>X</sub>		2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK <sub>X</sub>	External shift clock operation	tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ → SOT delay time	t <sub>SLOVE</sub>	SCK <sub>X</sub> SOT <sub>X</sub>		-	50	-	30	ns
SIN → SCK ↑ setup time	t <sub>IVSHE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		10	-	10	-	ns
SCK ↑ → SIN hold time	t <sub>SHIXE</sub>	SCK <sub>X</sub> SIN <sub>X</sub>		20	-	20	-	ns
SCK fall time	t <sub>F</sub>	SCK <sub>X</sub>		-	5	-	5	ns
SCK rise time	t <sub>R</sub>	SCK <sub>X</sub>		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
  - t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
  - These characteristics only guarantee the same relocate port number.  
For example, the combination of SCLK<sub>X\_0</sub> and SOT<sub>X\_1</sub> is not guaranteed.
  - When the external load capacitance = 30pF.

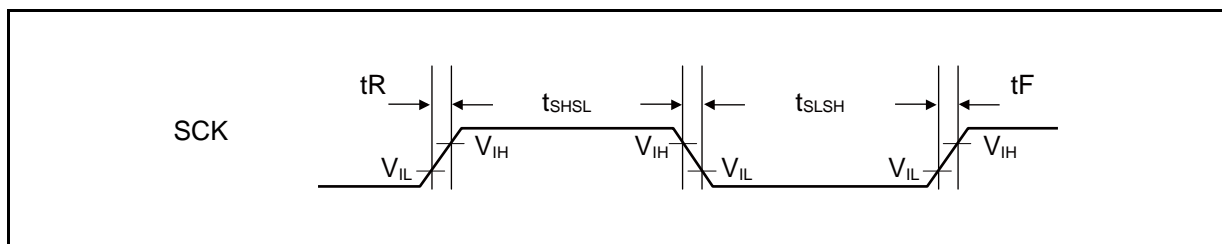
# MB9A310K Series



- External clock (EXT = 1) : asynchronous only

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock "L" pulse width	$t_{SLSH}$	$C_L = 30pF$	$t_{cycp} + 10$	-	ns	
Serial clock "H" pulse width	$t_{SHSL}$		$t_{cycp} + 10$	-	ns	
SCK fall time	$t_F$		-	5	ns	
SCK rise time	$t_R$		-	5	ns	



## (9) External Input Timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40^{\circ}C$  to  $+105^{\circ}C$ )

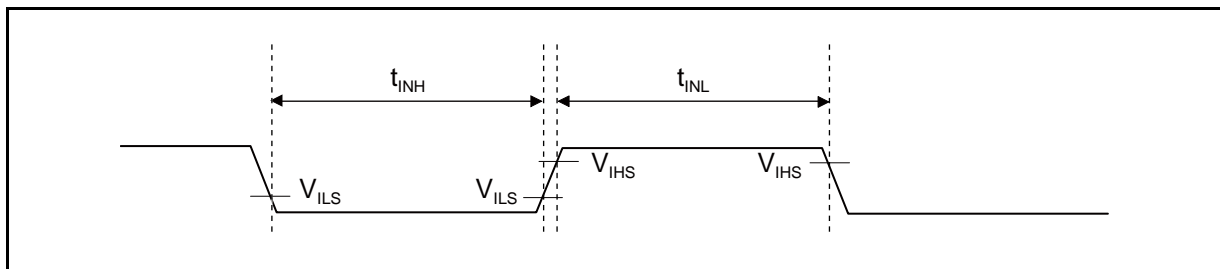
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{INH}$ , $t_{INL}$	ADTG	-	$2t_{CYCP}^{*1}$	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}^{*1}$	-	ns	Wave form generator
		INT00 to INT15	-	$2t_{CYCP} + 100^{*1}$	-	ns	External interrupt
		NMIX	-	$500^{*2}$	-	ns	NMI
WKUPx	-	$820^{*3}$	-	ns	Deep stand-by wake up		

\*1 :  $t_{CYCP}$  indicates the APB bus clock cycle time except stop when in stop mode, in rtc mode, in timer mode.

About the APB bus number which A/D converter, Multi-function Timer, External interrupt are connected to, see "■BLOCK DIAGRAM" in this data sheet.

\*2 : When in stop mode, in rtc mode, in timer mode.

\*3 : When in deep stand-by stop mode, in deep stand-by rtc mode.



# MB9A310K Series

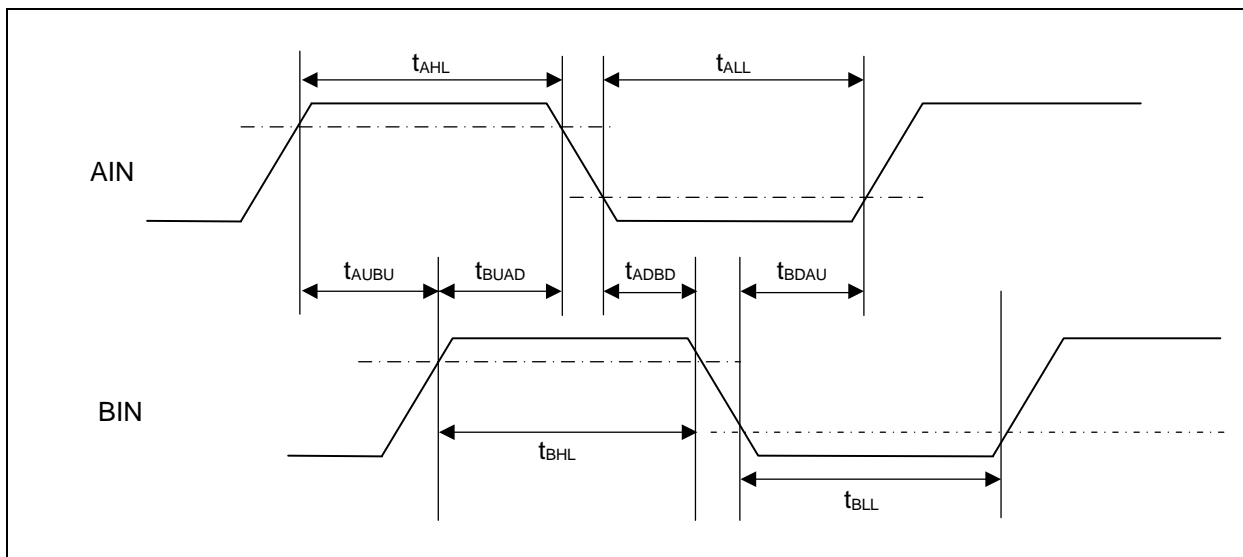
## (10) Quadrature Position/Revolution Counter timing

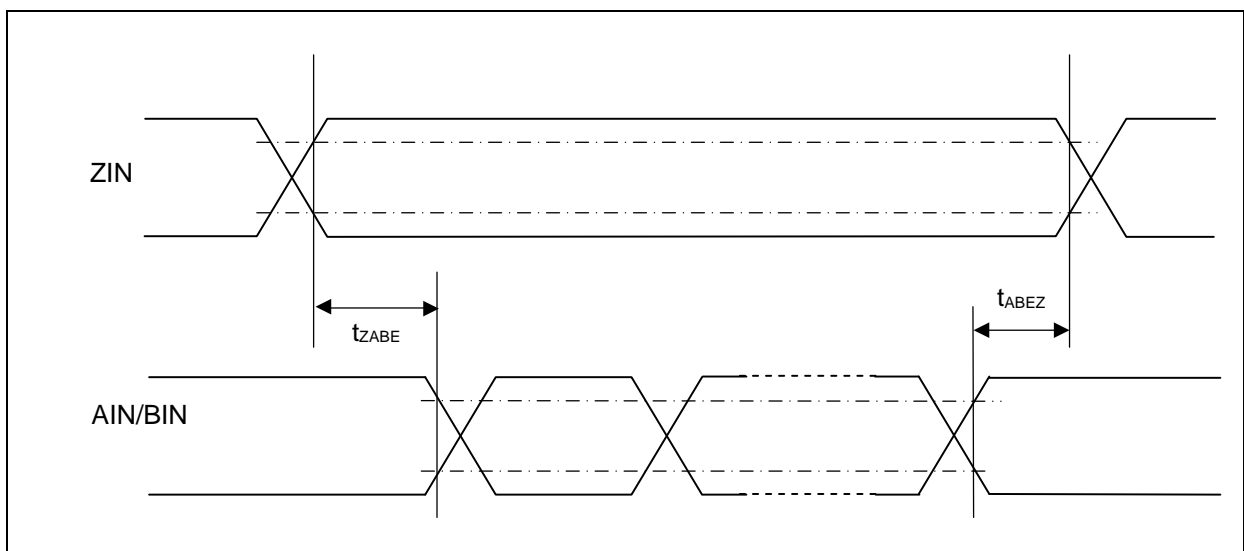
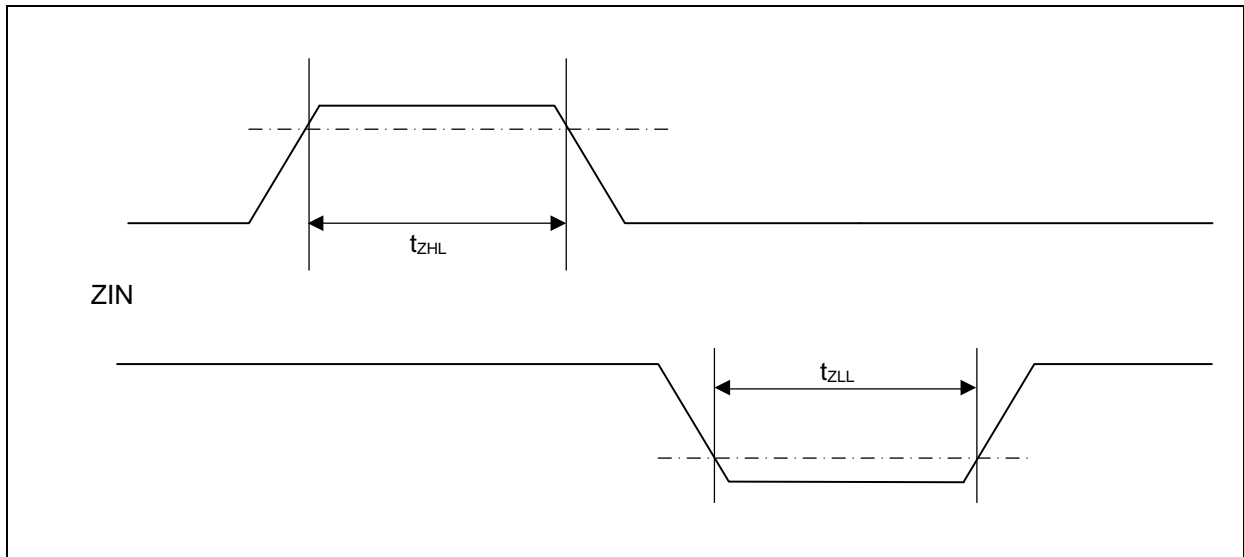
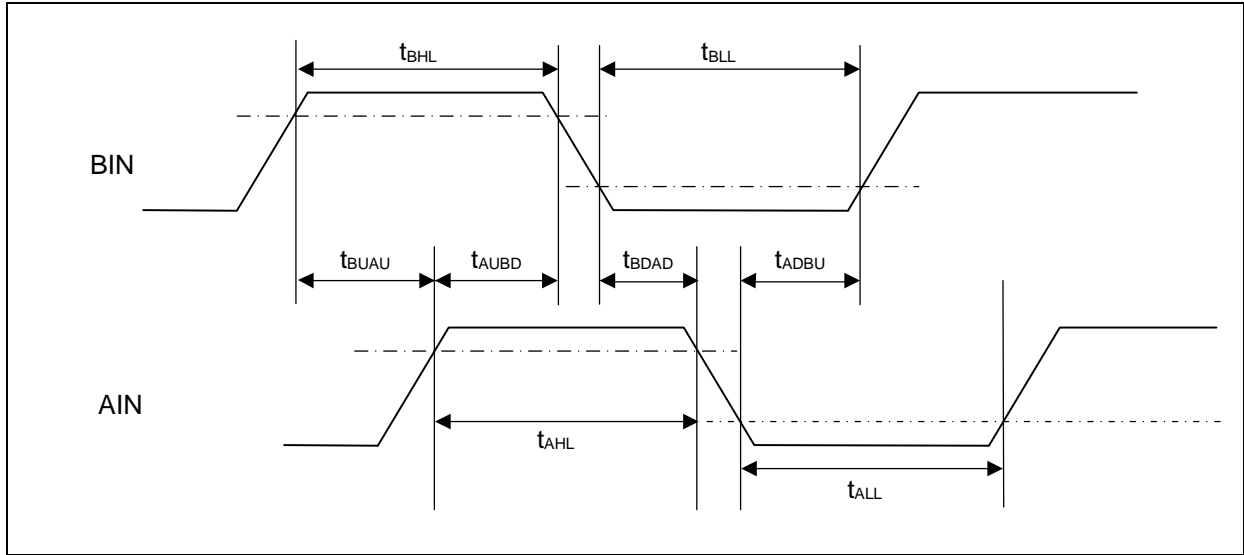
(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	t <sub>AHL</sub>	-	2t <sub>CYCP</sub> *	-	ns
AIN pin "L" width	t <sub>ALL</sub>	-			
BIN pin "H" width	t <sub>BHL</sub>	-			
BIN pin "L" width	t <sub>BLL</sub>	-			
BIN rise time from AIN pin "H" level	t <sub>AUBU</sub>	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	t <sub>BUAD</sub>	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	t <sub>ADBD</sub>	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	t <sub>BDAU</sub>	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	t <sub>BUAU</sub>	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	t <sub>AUBD</sub>	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	t <sub>BDAD</sub>	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	t <sub>ADBU</sub>	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	t <sub>ZHL</sub>	QCR:CGSC="0"			
ZIN pin "L" width	t <sub>ZLL</sub>	QCR:CGSC="0"			
AIN/BIN rise and fall time from determined ZIN level	t <sub>ZABE</sub>	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rise and fall time	t <sub>ABEZ</sub>	QCR:CGSC="1"			

\*: t<sub>CYCP</sub> indicates the APB bus clock cycle time except stop when in stop mode, in timer mode.

About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "■BLOCK DIAGRAM" in this data sheet.





# MB9A310K Series

## (11) I<sup>2</sup>C Timing

(V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>a</sub> = -40°C to +105°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F <sub>SCL</sub>		0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>	C <sub>L</sub> = 30pF, R = (V <sub>p</sub> /I <sub>OL</sub> )* <sup>1</sup>	4.0	-	0.6	-	μs	
SCLclock "L" width	t <sub>LOW</sub>		4.7	-	1.3	-	μs	
SCLclock "H" width	t <sub>HIGH</sub>		4.0	-	0.6	-	μs	
(Repeated) START setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45* <sup>2</sup>	0	0.9* <sup>3</sup>	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	-	0.6	-	μs	
Bus free time between "STOP condition" and "START condition"	t <sub>BUF</sub>		4.7	-	1.3	-	μs	
Noise filter	t <sub>SP</sub>		-	2 t <sub>CYCP</sub> * <sup>4</sup>	-	2 t <sub>CYCP</sub> * <sup>4</sup>	-	ns

\*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.

V<sub>p</sub> indicates the power supply voltage of the pull-up resistance and I<sub>OL</sub> indicates V<sub>OL</sub> guaranteed current.

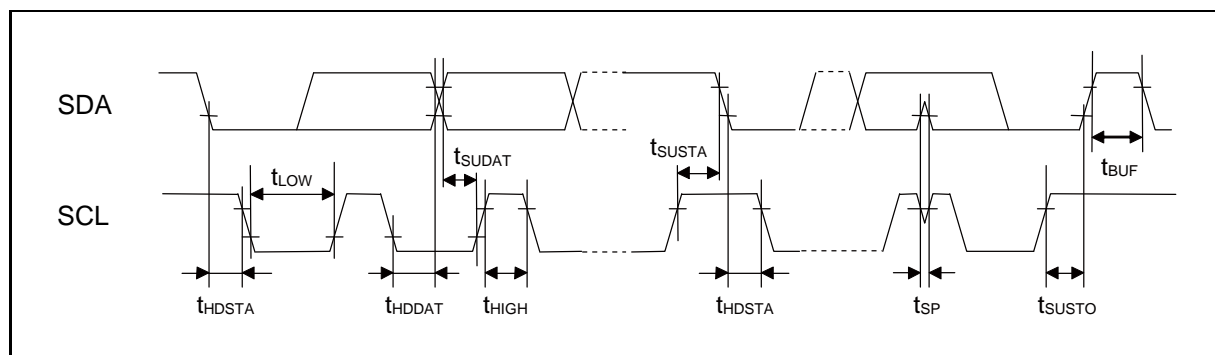
\*2 : The maximum t<sub>HDDAT</sub> must satisfy that it does not extend at least "L" period (t<sub>LOW</sub>) of device's SCL signal.

\*3 : A high-speed mode I<sup>2</sup>C bus device can be used on a standard mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of "t<sub>SUDAT</sub> ≥ 250 ns".

\*4 : t<sub>CYCP</sub> is the APB bus clock cycle time.

About the APB bus number that I<sup>2</sup>C is connected to, see "■BLOCK DIAGRAM" in this data sheet.

To use I<sup>2</sup>C, set the peripheral bus clock at 8 MHz or more.



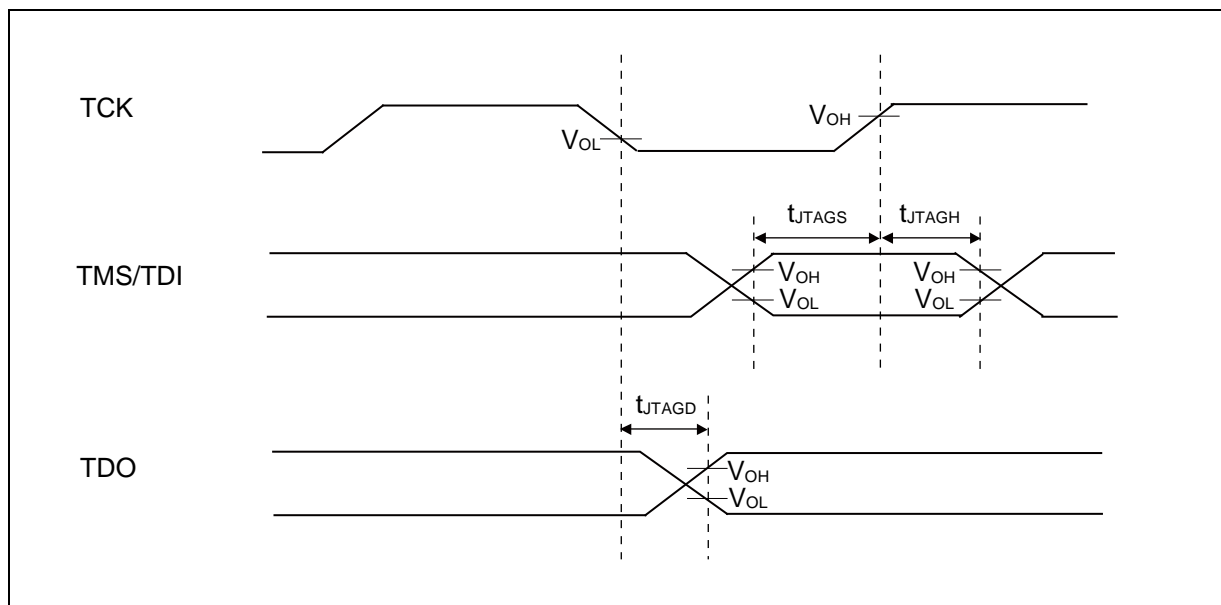


## (12) JTAG Timing

( $V_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_a = -40^{\circ}C$  to  $+105^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	$t_{JTAGS}$	TCK, TMS, TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TMS, TDI hold time	$t_{JTAGH}$	TCK, TMS, TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TDO delay time	$t_{JTAGD}$	TCK, TDO	$V_{CC} \geq 4.5V$	-	25	ns	
			$V_{CC} < 4.5V$	-	45		

Note: When the external load capacitance = 30pF.



# MB9A310K Series

## 5. 12-bit A/D Converter

- Electrical characteristics for the A/D converter

(V<sub>cc</sub> = AV<sub>cc</sub> = 2.7V to 5.5V, V<sub>ss</sub> = AV<sub>ss</sub> = 0V, Ta = - 40°C to + 105°C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	-	-	-	12	bit	
Linearity error	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7V to 5.5V
Differential linearity error	-	-2.5	-	+ 2.5	LSB	
Zero transition voltage	AN0 to AN7	- 20	-	+ 20	mV	
Full-scale transition voltage	AN0 to AN7	AVRH - 20	-	AVRH + 20	mV	
Conversion time	-	1.0* <sup>1</sup>	-	-	μs	AV <sub>cc</sub> ≥ 4.5V
Sampling time	Ts	*2	-	-	ns	AV <sub>cc</sub> ≥ 4.5V
		*2	-	-		AV <sub>cc</sub> < 4.5V
Compare clock cycle* <sup>3</sup>	T <sub>ck</sub>	50	-	2000	ns	AV <sub>cc</sub> ≥ 4.5V
						AV <sub>cc</sub> < 4.5V
State transition time to operation permission	T <sub>stt</sub>	1.0	-	-	μs	
Power supply current (analog + digital)	AV <sub>CC</sub>	-	0.57	0.72	mA	A/D 1unit operation
		-	0.06	20	μA	When A/D stop
Reference power supply current (between AVRH to AVSS)	AVRH	-	1.1	1.96	mA	A/D 1unit operation AVRH=5.5V
		-	0.06	4	μA	When A/D stop (1unit)
Analog input capacity	C <sub>in</sub>	-	-	12.9	pF	
Analog input resistance	R <sub>in</sub>	-	-	2	kΩ	AV <sub>cc</sub> ≥ 4.5V
				3.8		AV <sub>cc</sub> < 4.5V
Interchannel disparity	-	-	-	4	LSB	
Analog port input current	AN0 to AN7	-	-	5	μA	
Analog input voltage	AN0 to AN7	AV <sub>SS</sub>	-	AVRH	V	
Reference voltage	AVRH	2.7	-	AV <sub>CC</sub>	V	

\*1: Conversion time is the value of sampling time (Ts) + compare time (Tc).

The condition of the minimum conversion time is the value of sampling time: 300ns, the value of sampling time: 700ns (AV<sub>cc</sub> ≥ 4.5V).

Ensure that it satisfies the value of sampling time (Ts) and compare clock cycle (T<sub>ck</sub>).

For setting\*<sup>4</sup> of sampling time and compare clock cycle, see "Chapter:A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".

\*2: A necessary sampling time changes by external impedance.

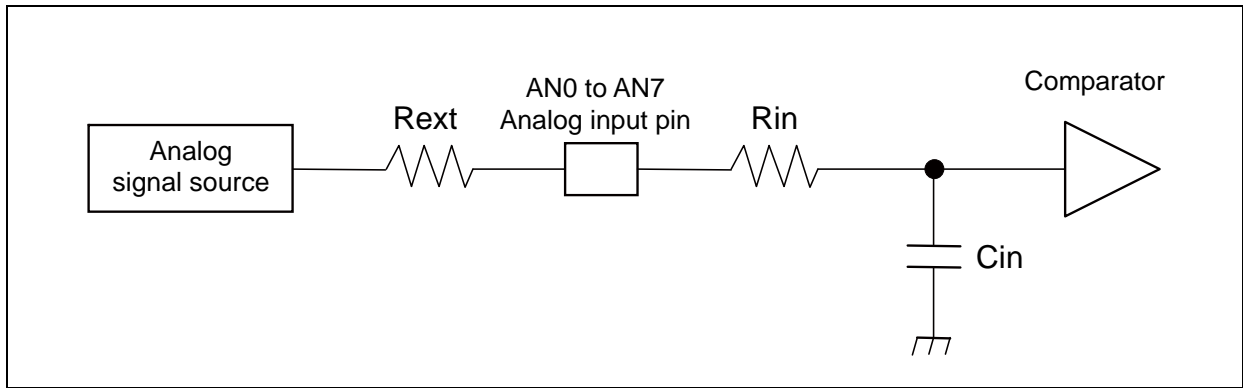
Ensure that it set the sampling time to satisfy (Equation 1).

\*3: Compare time (Tc) is the value of (Equation 2).

\*4: The register setting of the A/D Converter is reflected by the timing of the APB bus clock.

Sampling clock and compare clock are set in base clock (HCLK).

About the APB bus number which A/D Converter is connected to, see "■BLOCK DIAGRAM" in this data sheet.



(Equation 1)  $T_s \geq (R_{in} + R_{ext}) \times C_{in} \times 9$

$T_s$  : Sampling time

$R_{in}$  : input resistance of A/D =  $2\text{k}\Omega$  at  $4.5 \leq AVCC \leq 5.5$   
input resistance of A/D =  $3.8\text{k}\Omega$  at  $2.7 \leq AVCC \leq 4.5$

$C_{in}$  : input capacity of A/D =  $12.9\text{pF}$  at  $2.7 \leq AVCC \leq 5.5$

$R_{ext}$  : Output impedance of external circuit

(Equation 2)  $T_c = T_{cck} \times 14$

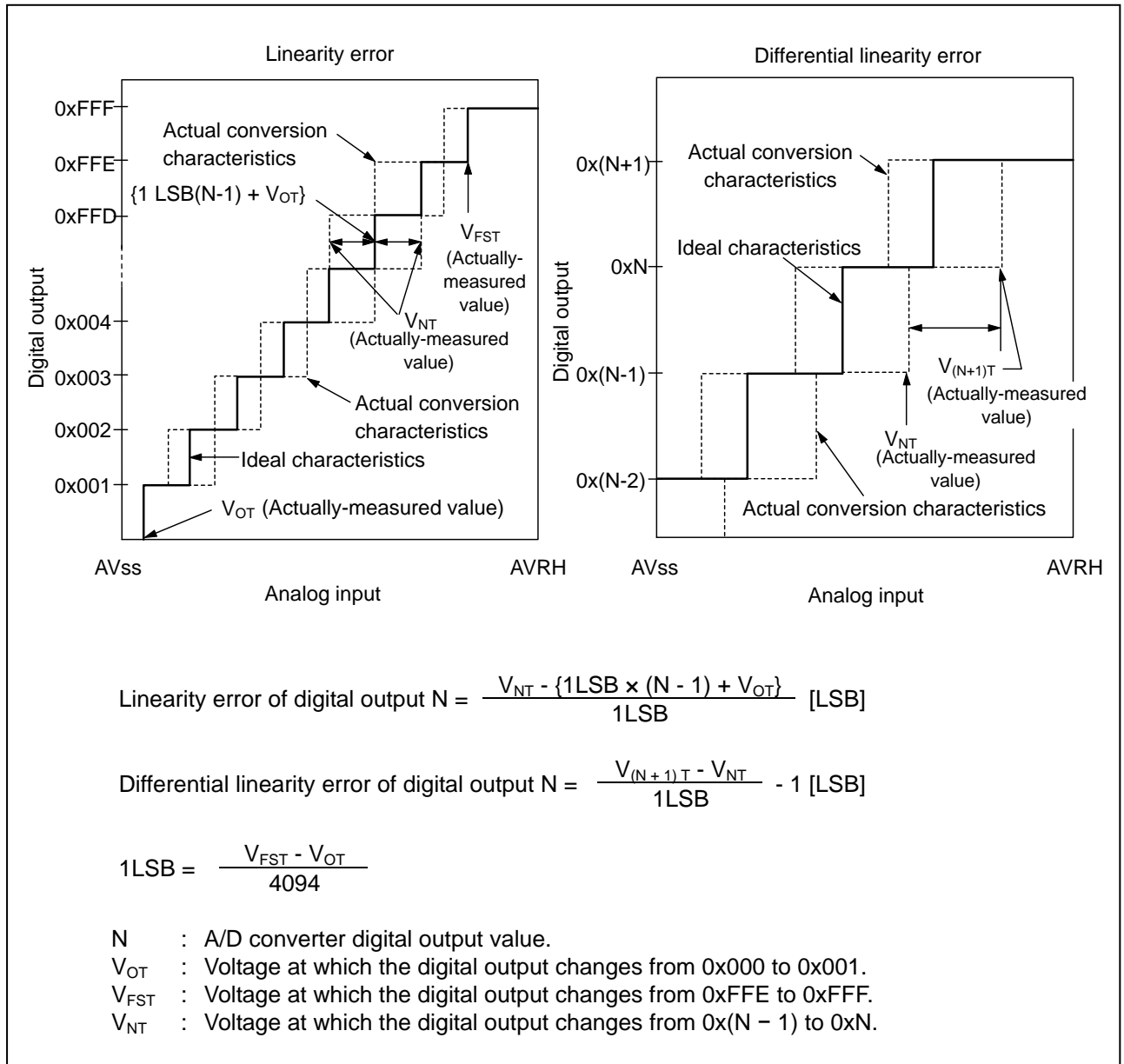
$T_c$  : Compare time

$T_{cck}$  : Compare clock cycle

# MB9A310K Series

• Definition of 12-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0b000000000000 ←→ 0b000000000001) and the full-scale transition point (0b111111111110 ←→ 0b111111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



## 6. USB Characteristics

(V<sub>cc</sub> = 2.7V to 5.5V, USBV<sub>cc</sub> = 3.0V to 3.6V, V<sub>ss</sub> = 0V, Ta = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input characteristics	Input "H" level voltage	V <sub>IH</sub>	-	2.0	USBV <sub>cc</sub> + 0.3	V	*1
	Input "L" level voltage	V <sub>IL</sub>	-	V <sub>ss</sub> - 0.3	0.8	V	*1
	Differential input sensitivity	V <sub>DI</sub>	-	0.2	-	V	*2
	Different common mode input voltage	V <sub>CM</sub>	-	0.8	2.5	V	*2
Output characteristics	Output "H" level voltage	V <sub>OH</sub>	External pull-down resistance = 15kΩ	2.8	3.6	V	*3
	Output "L" level voltage	V <sub>OL</sub>	External pull-up resistance = 1.5kΩ	0.0	0.3	V	*3
	Crossover voltage	V <sub>CRS</sub>	-	1.3	2.0	V	*4
	Rise time	t <sub>FR</sub>	Full-Speed	4	20	ns	*5
	Fall time	t <sub>FF</sub>	Full-Speed	4	20	ns	*5
	Rise/ fall time matching	t <sub>FRFM</sub>	Full-Speed	90	111.11	%	*5
	Output impedance	Z <sub>DRV</sub>	Full-Speed	28	44	Ω	*6
	Rise time	t <sub>LR</sub>	Low-Speed	75	300	ns	*7
	Fall time	t <sub>LF</sub>	Low-Speed	75	300	ns	*7
	Rise/ fall time matching	t <sub>LRFM</sub>	Low-Speed	80	125	%	*7

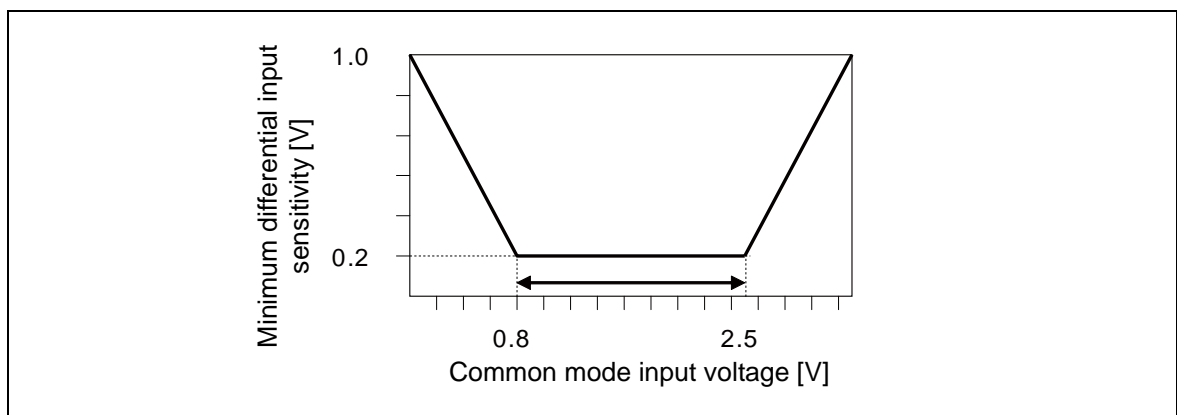
\*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V<sub>IL</sub> (Max) = 0.8V, V<sub>IH</sub> (Min) = 2.0 V (TTL input standard).

There are some hysteresis to lower noise sensitivity.

\*2 : Use differential-Receiver to receive USB differential data signal.

Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

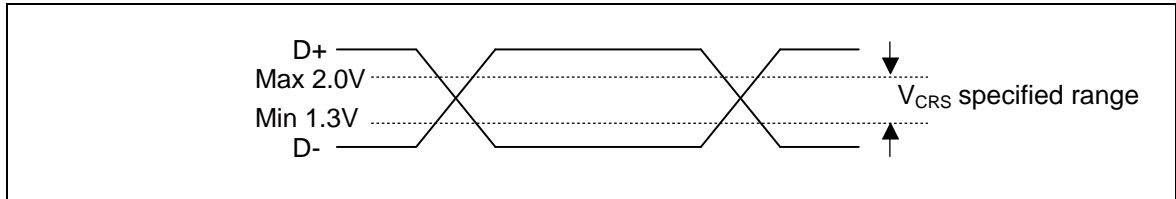
Above voltage range is the common mode input voltage range.



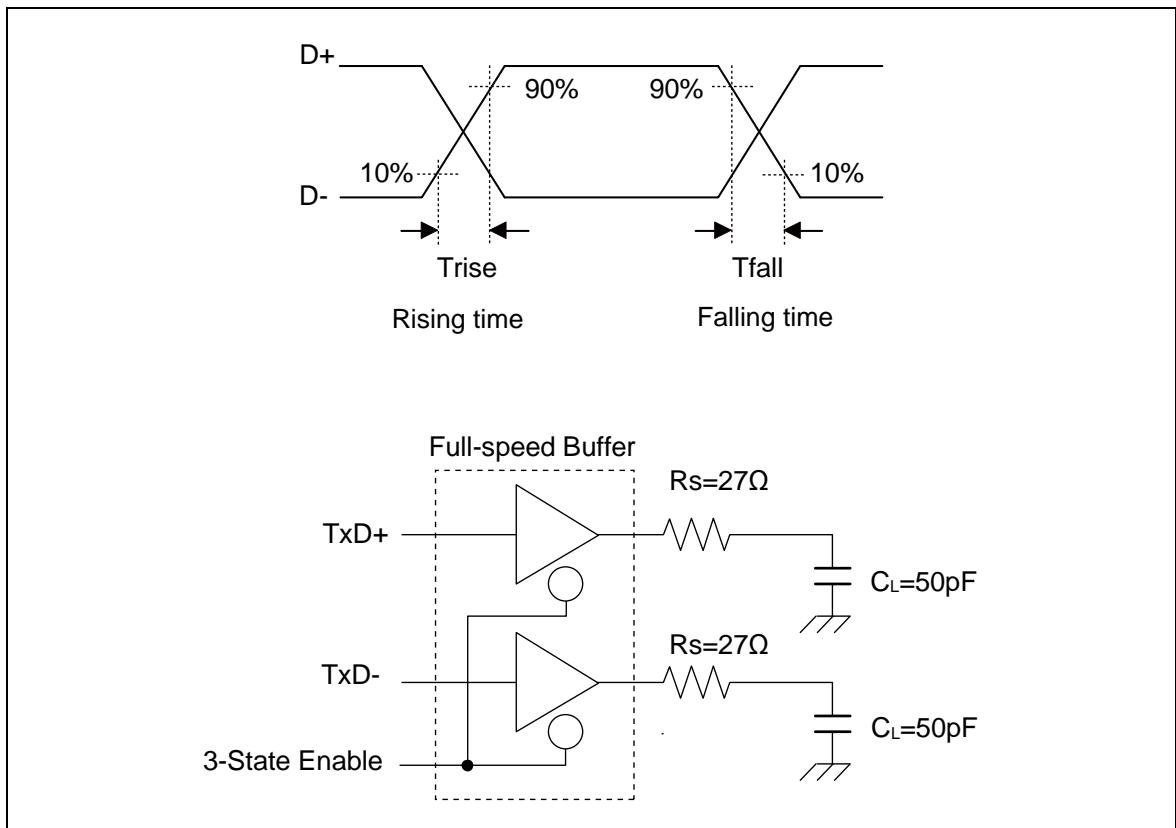
# MB9A310K Series

\*3 : The output drive capability of the driver is below 0.3 V at Low-State ( $V_{OL}$ ) (to 3.6 V and 1.5 k $\Omega$  load), and 2.8 V or above (to the VSS and 1.5 k $\Omega$  load) at High-State ( $V_{OH}$ ).

\*4 : The cross voltage of the external differential output signal (D + /D -) of USB I/O buffer is within 1.3 V to 2.0 V.



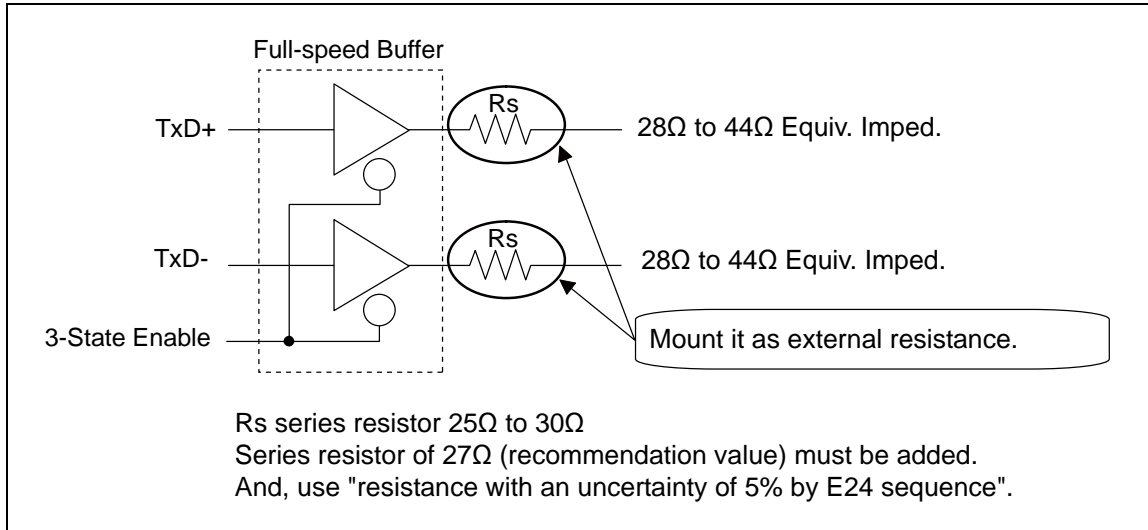
\*5 : They indicate rise time ( $T_{rise}$ ) and fall time ( $T_{fall}$ ) of the full-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage. For full-speed buffer,  $T_r/T_f$  ratio is regulated as within  $\pm 10\%$  to minimize RFI emission.



\*6 : USB Full-speed connection is performed via twist pair cable shield with  $90\Omega \pm 15\%$  characteristic impedance (Differential Mode).

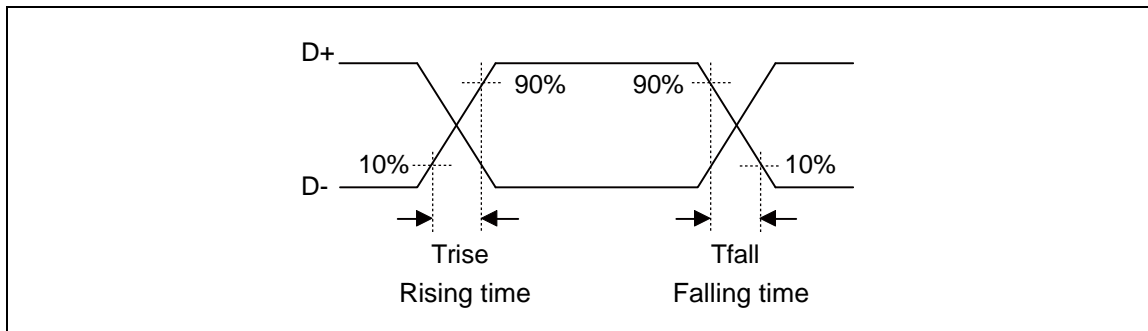
USB standard defines that output impedance of USB driver must be in range from  $28\Omega$  to  $44\Omega$ . So, discrete series resistor ( $R_s$ ) addition is defined in order to satisfy the above definition and keep balance.

When using this USB FLS I/O, use it with  $25\Omega$  to  $30\Omega$  (recommendation value  $27\Omega$ ) Series resistor  $R_s$ .



\*7 : They indicate rise time ( $T_{rise}$ ) and fall time ( $T_{fall}$ ) of the low-speed differential data signal.

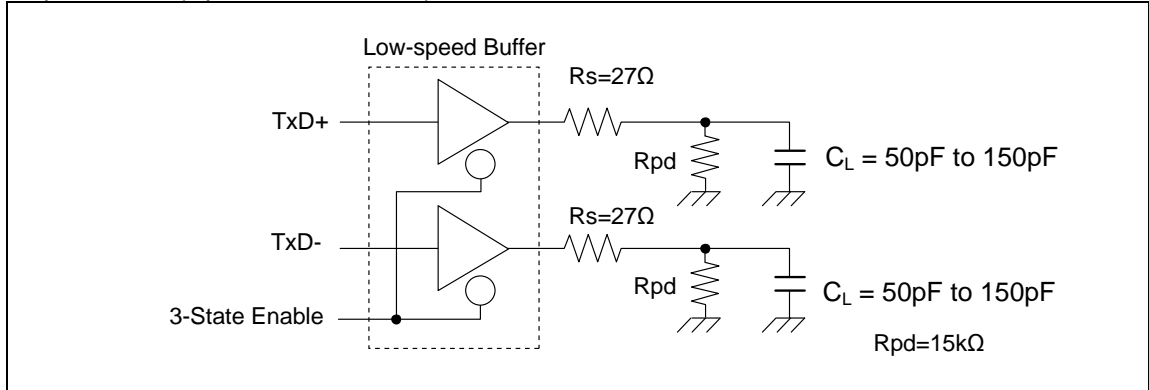
They are defined by the time between 10% and 90% of the output signal voltage.



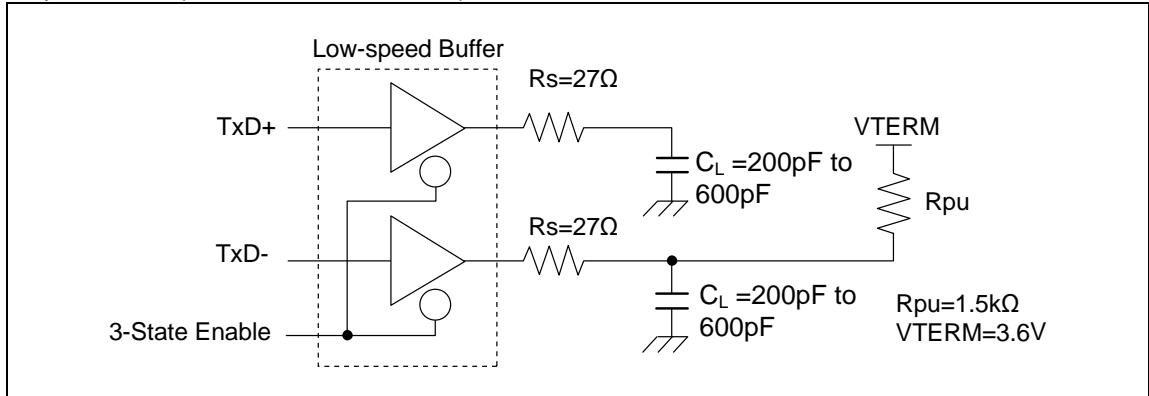
See Figure "• Low-Speed Load (Compliance Load)" for conditions of external load.

# MB9A310K Series

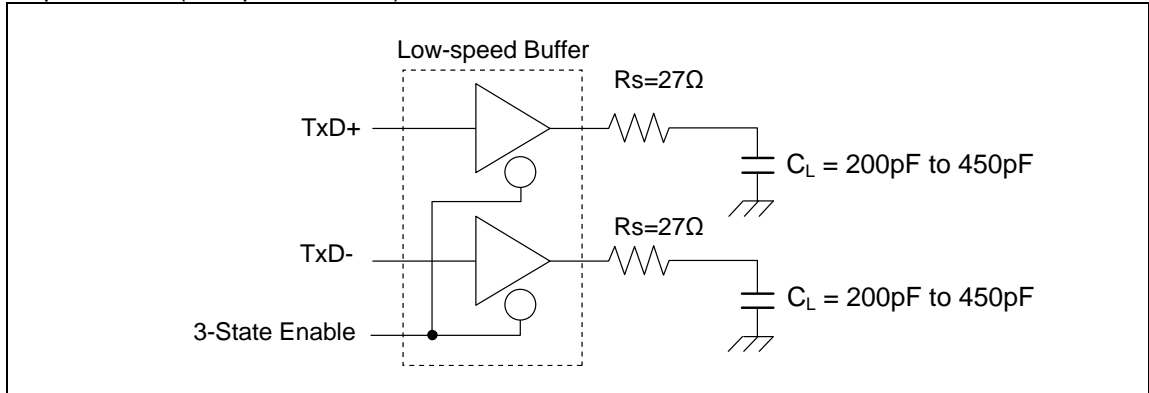
- Low-Speed Load (Upstream Port Load) - Reference 1



- Low-Speed Load (Downstream Port Load) - Reference 2



- Low-Speed Load (Compliance Load)





## 7. Low-voltage Detection Characteristics

### (1) Low-voltage Detection Reset

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

### (2) Interrupt of Low-voltage Detection

(Ta = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T <sub>LVDW</sub>	-	-	-	2240 × tcycp*	μs	

\*: tcycp indicates the APB2 bus clock cycle time.

# MB9A310K Series

## 8. MainFlash Memory Write/Erase Characteristics

(V<sub>CC</sub> = 2.7V to 5.5V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector		0.3	1.1		
Half word (16-bit) write time		-	12	384	μs	Not including system-level overhead time
Chip erase time		-	3.8	16.2	s	Includes write time prior to internal erase

Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)
1,000	20*
10,000	10*
100,000	5*

\*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

## 9. WorkFlash Memory Write/Erase Characteristics

(V<sub>CC</sub> = 2.7V to 5.5V, T<sub>a</sub> = - 40°C to + 105°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time		-	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time		-	20	384	μs	Not including system-level overhead time
Chip erase time		-	1.2	6	s	Includes write time prior to internal erase

Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)
1,000	20*
10,000	10*

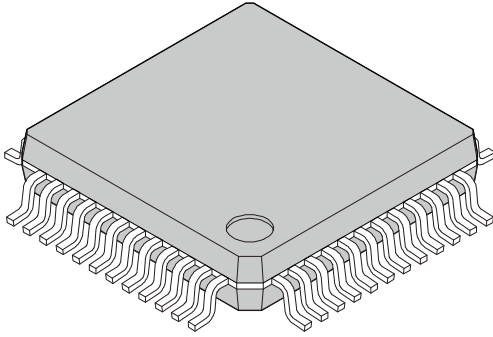
\*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

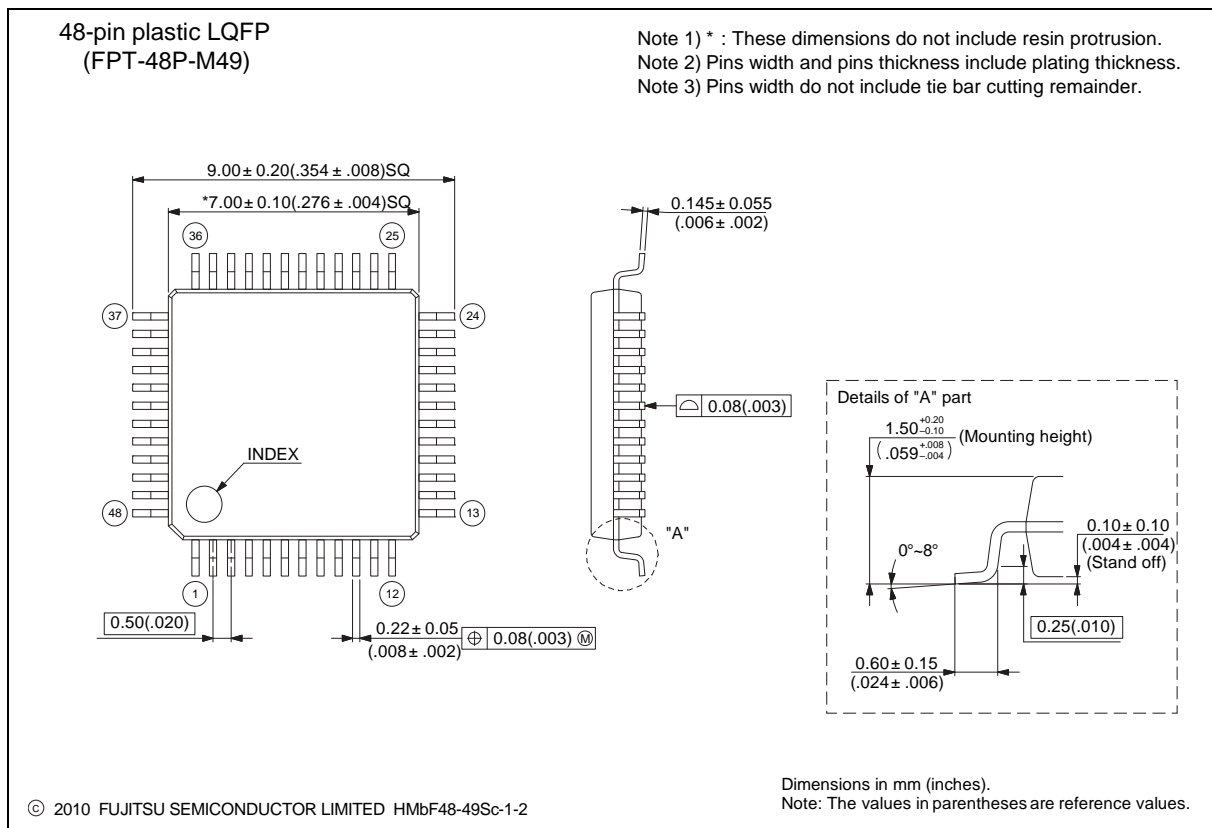
## ■ ORDERING INFORMATION

Part number	Package
MB9AF311KPMC	Plastic • LQFP 48-pin (0.5mm pitch), (FPT-48P-M49)
MB9AF312KPMC	
MB9AF311KPMC1	Plastic • LQFP 52-pin (0.65mm pitch), (FPT-52P-M02)
MB9AF312KPMC1	
MB9AF311KQN	Plastic • QFN 48-pin (0.5mm pitch), (LCC-48P-M73)
MB9AF312KQN	

# MB9A310K Series

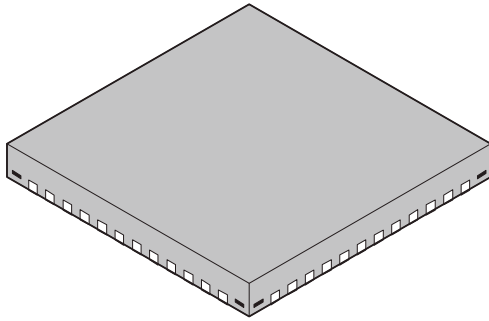
## ■ PACKAGE DIMENSIONS

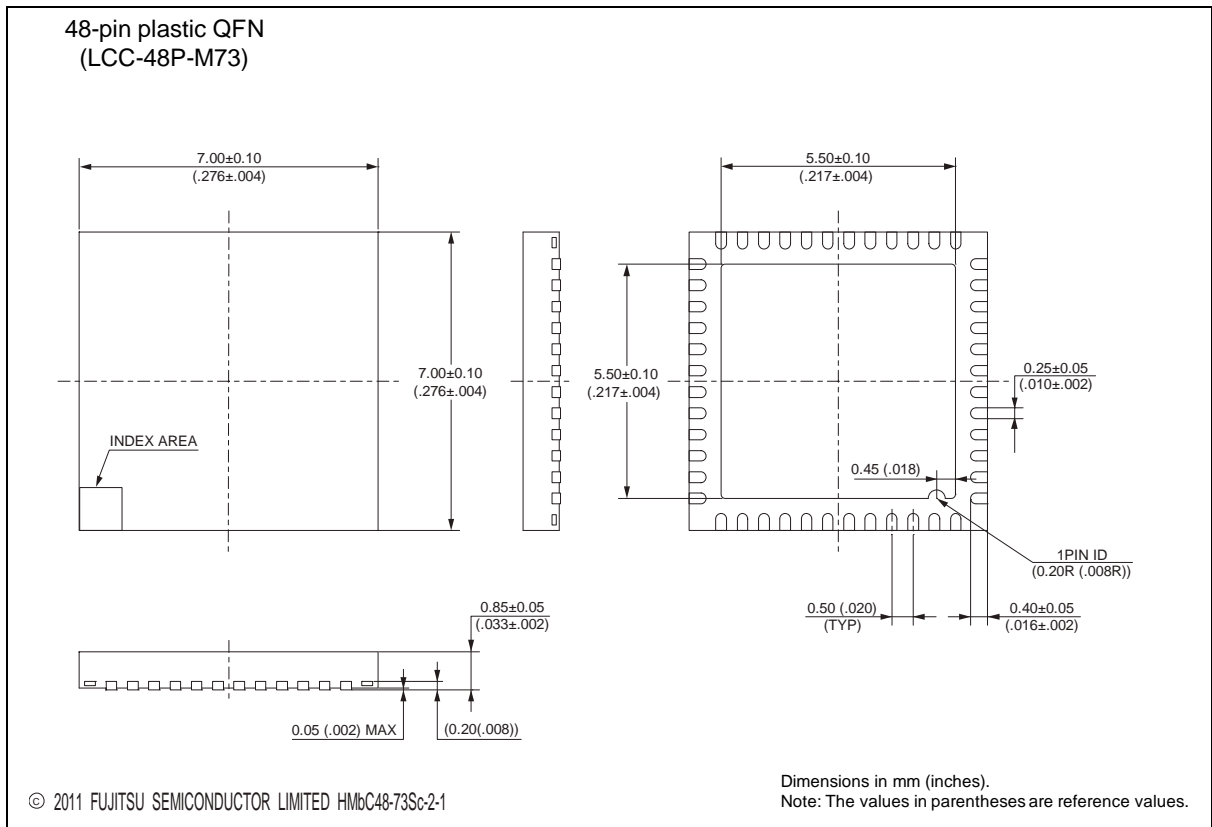
<p>48-pin plastic LQFP</p>  <p>(FPT-48P-M49)</p>	Lead pitch	0.50 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g



Please check the latest package dimension at the following URL.  
<http://edevic.fujitsu.com/package/en-search/>

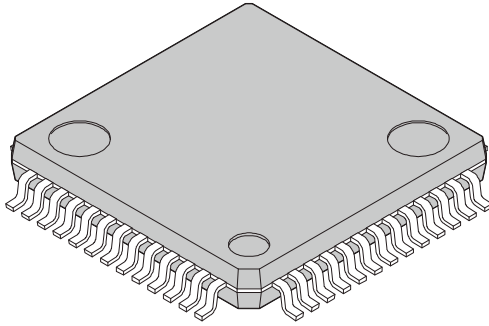
# MB9A310K Series

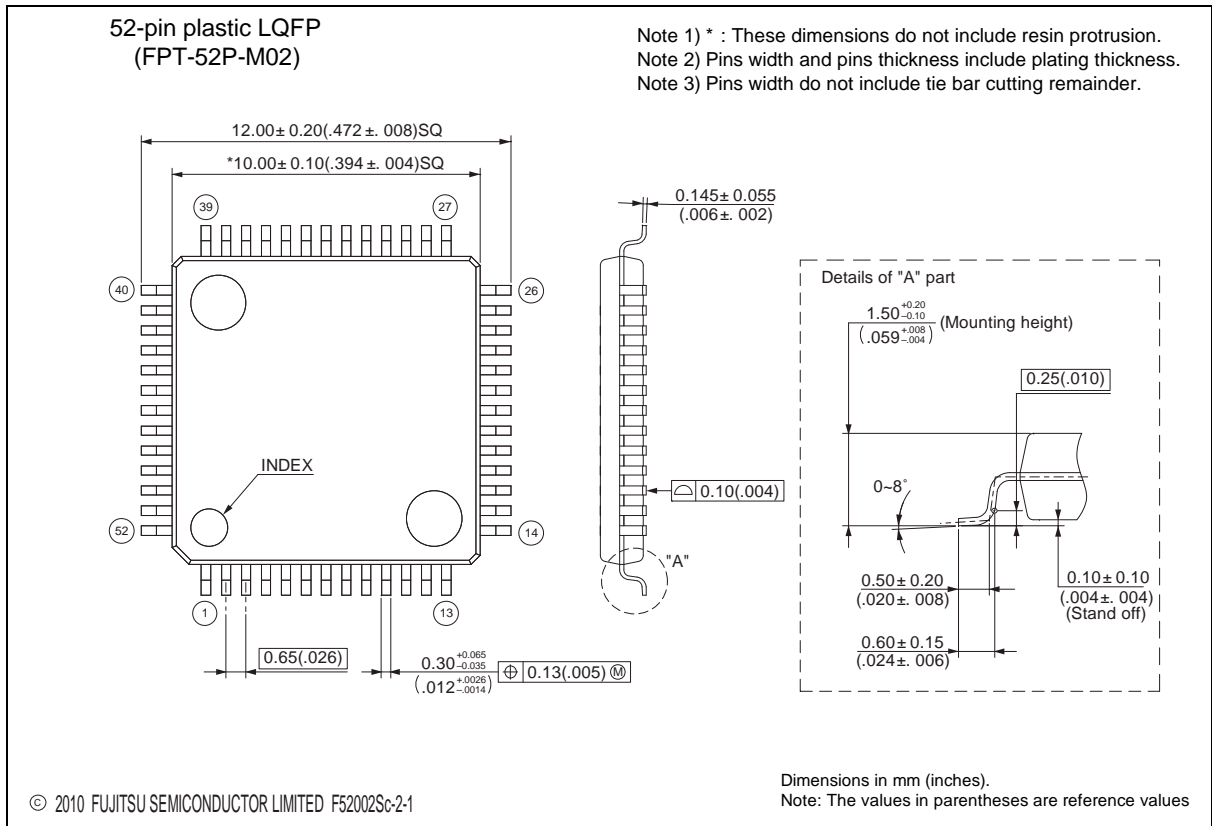
<p>48-pin plastic QFN</p>  <p>(LCC-48P-M73)</p>	Lead pitch	0.5 mm
	Package width × package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	—



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# MB9A310K Series

<p>52-pin plastic LQFP</p>  <p>(FPT-52P-M02)</p>	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP52-10×10-0.65



Please check the latest package dimension at the following URL.  
<http://edevice.fujitsu.com/package/en-search/>

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
-	-	PRELIMINARY → Data sheet
7	■PRODUCT LINEUP •Function	Added the pin count.
8	■PACKAGES	Revised from "Planning".
23	■I/O CIRCUIT TYPE	Corrected the following description to "TypeB". Digital output → Digital input
34	■BLOCK DIAGRAM	Corrected the following description. • AHB (Max 40MHz) → AHB (Max 42MHz) • APB0 (Max 40MHz) → APB0 (Max 42MHz) • APB1 (Max 40MHz) → APB1 (Max 42MHz) • APB2 (Max 40MHz) → APB2 (Max 42MHz)
45, 46	■ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current Rating	• Revised the value of "TBD". • Corrected the value. - "Power supply current (I <sub>CCR</sub> )" Typ: 60 → 50 - "Power supply current (I <sub>CCRD</sub> )" (RAM hold off) Typ: 45 → 30 - "Power supply current (I <sub>CCRD</sub> )" (RAM hold on) Typ: 48 → 33
61	(9) External Input Timing	Revised the value of "TBD".
66	5. 12-bit A/D Converter •Electrical characteristics for the A/D converter	• Deleted"(Preliminary value)". • Corrected the value of "Compare clock cycle". Max: 10000 → 2000
74	8. MainFlash Memory Write/Erase Characteristics Erase/write cycles and data hold time 9. WorkFlash Memory Write/Erase Characteristics Erase/write cycles and data hold time	Deleted"(targeted value)".

# MB9A310K Series

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