FUJITSU SEMICONDUCTOR
DATA SHEET

DS706-00042-3v0-E

32-bit ARM™ Cortex™-M3 based Microcontroller

FM3 MB9A130N Series

MB9AF131M/N, MB9AF132M/N

■ DESCRIPTION

The MB9A130N Series are highly integrated 32-bit microcontrollers that dedicated for embedded controllers with low-power consumption mode and competitive cost.
The MB9A130N Series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as Motor Control Timers, ADCs, DACs and Communication Interfaces (UART, CSIO, I^2C).

The products which are described in this data sheet are placed into TYPE7 product categories in " FM3 Family PERIPHERAL MANUAL ".

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ARM™

2013.3

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■ FEATURES

- 32-bit ARM Cortex-M3 Core
  - Processor version: r2p1
  - Up to 20MHz Operation Frequency
  - Integrated Nested Vectored Interrupt Controller (NVIC): 1 channel NMI (non-maskable interrupt) and 32 channels' peripheral interrupts and 8 priority levels
  - 24-bit System timer (Sys Tick): System timer for OS task management

- On-chip Memories

[Flash memory]

  - Up to 128 Kbytes
  - Read cycle: 0 wait-cycle
  - Security function for code protection

[SRAM]

This series contains a total of up to 16Kbyte on-chip SRAM memories. This is composed of two independent SRAM (SRAM0, SRAM1) . SRAM0 is connected to I-code bus or D-code bus of Cortex-M3 core. SRAM1 is connected to System bus of Cortex-M3 core.

  - SRAM0: None
  - SRAM1: Up to 16 Kbytes

- Multi-function Serial Interface (Max 8channels)

Operation mode is selectable from the followings for each channel.

  - UART
  - CSIO
  - I^2C

[UART]

  - Full duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

  - Full duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detection function available

[I^2C]

Standard mode (Max 100kbps) / High-speed mode (Max 400kbps) supported

- A/D Converter (Max 16channels)

[12-bit A/D Converter]

  - Successive Approximation type
  - Conversion time: Min 1.0µs
  - Priority conversion available (priority at 2levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

- D/A Converter (Max 2channels)
  - R-2R type
  - 10-bit resolution

- Base Timer (Max 8channels)

  Operation mode is selectable from the followings for each channel.

  - 16-bit PWM timer
  - 16-bit PPG timer
  - 16/32-bit reload timer
  - 16/32-bit PWC timer

- General-Purpose I/O Port

  This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

  - Capable of pull-up control per pin
  - Capable of reading pin level directly
  - Built-in the port relocate function
  - Up to 84 high-speed general-purpose I/O Ports@100pin Package
  - Some ports are 5V tolerant I/O

    See "■ LIST OF PIN FUNCTIONS" and "■ I/O CIRCUIT TYPE" to confirm the corresponding pins.

- Multi-function Timer

  The Multi-function timer is composed of the following blocks.

  - 16-bit free-run timer × 3ch.
  - Input capture × 4ch.
  - Output compare × 6ch.
  - A/D activating compare × 3ch.
  - Waveform generator × 3ch.
  - 16-bit PPG timer × 3ch.

    IGBT mode is contained

  The following function can be used to achieve the motor control.

  - PWM signal output function
  - DC chopper waveform output function
  - Dead time function
  - Input capture function
  - A/D convertor activate function
  - DTIF (Motor emergency stop) interrupt function

- HDMI-CEC/Remote Control Receiver (Up to 2channels)
  - HDMI- CEC receiver / Remote control receiver
    - Operating modes supporting the following standards can be selected
      - SIRCS
      - NEC/Association for Electric Home Appliances
      - HDMI-CEC
    - Capable of adjusting detection timings for start bit and data bit
    - Equipped with noise filter
  - HDMI-CEC transmitter
    - Header block automatic transmission by judging Signal free
    - Generating status interrupt by detecting Arbitration lost
    - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
    - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)

- Real-time clock (RTC)

  The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

  - The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
  - Timer interrupt function after set time or each set time.
  - Capable of rewriting the time with continuing the time count.
  - Leap year automatic count is available.

- External Interrupt Controller Unit
  - Up to 16 external interrupt input pins
  - Include one non-maskable interrupt (NMI) input pin

- Watchdog Timer (2channels)

  A watchdog timer can generate interrupts or a reset when a time-out value is reached.

  This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

  The "Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the "Hardware" watchdog is active in any low-power consumption mode except RTC, STOP, Deep standby RTC and Deep standby STOP modes.

- Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

- Main Clock : 4 MHz to 20MHz
- Sub Clock : 32.768kHz
- Built-in high-speed CR Clock : 4MHz
- Built-in low-speed CR Clock : 100kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power-on reset
- Software reset
- Watchdog timers reset
- Low-voltage detection reset
- Clock Super Visor reset

- Clock Super Visor (CSV)

  Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

  - If external clock failure (clock stop) is detected, reset is asserted.
  - If external frequency anomaly is detected, interrupt or reset is asserted.

- Low-Voltage Detector (LVD)

  This Series includes 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

  - LVD1: error reporting via interrupt
  - LVD2: auto-reset operation

- Low-Power Consumption Mode
  Six low-power consumption modes supported.

  - SLEEP
  - TIMER
  - RTC
  - STOP
  - Deep standby RTC
  - Deep standby STOP

  The back up register is 16bytes.

- Debug
  Serial Wire JTAG Debug Port (SWJ-DP)

- Power Supply
  Wide range voltage : VCC = 1.8V to 5.5V

■ PRODUCT LINEUP

• Memory size

Product name		MB9AF131M/N	MB9AF132M/N
On-chip Flash memory		64Kbytes	128Kbytes
On-chip SRAM	SRAM1	12Kbytes	16Kbytes

• Function

Product name			MB9AF131M MB9AF132M	MB9AF131N MB9AF132N
Pin count			80	100
CPU			Cortex-M3	
	Freq.		20MHz	
Power supply voltage range			1.8V to 5.5V	
Multi-function Serial Interface (UART/CSIO/I^{2}C)			8ch. (Max)	
Base Timer (PWC/ Reload timer/PWM/PPG)			8ch. (Max)	
MF-Timer	A/D activation compare	3ch.	1 unit (Max)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG (IGBT mode)	3ch.		
HDMI-CEC/ Remote Control Receiver			2ch. (Max)	
Real-time clock			1 unit	
Watchdog timer			1ch. (SW) + 1ch. (HW)	
External Interrupts			11pins (Max) + NMI × 1	16pins (Max) + NMI × 1
General-purpose I/O ports			67pins (Max)	84pins (Max)
12-bit A/D converter			12ch. (1 unit)	16ch. (1 unit)
10-bit D/A converter			2ch. (Max)	
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2ch.	
Built-in CR	High-speed		4MHz (± 2%)	
	Low-speed		100kHz (Typ)	
Debug Function			SWJ-DP	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.

■ PACKAGES

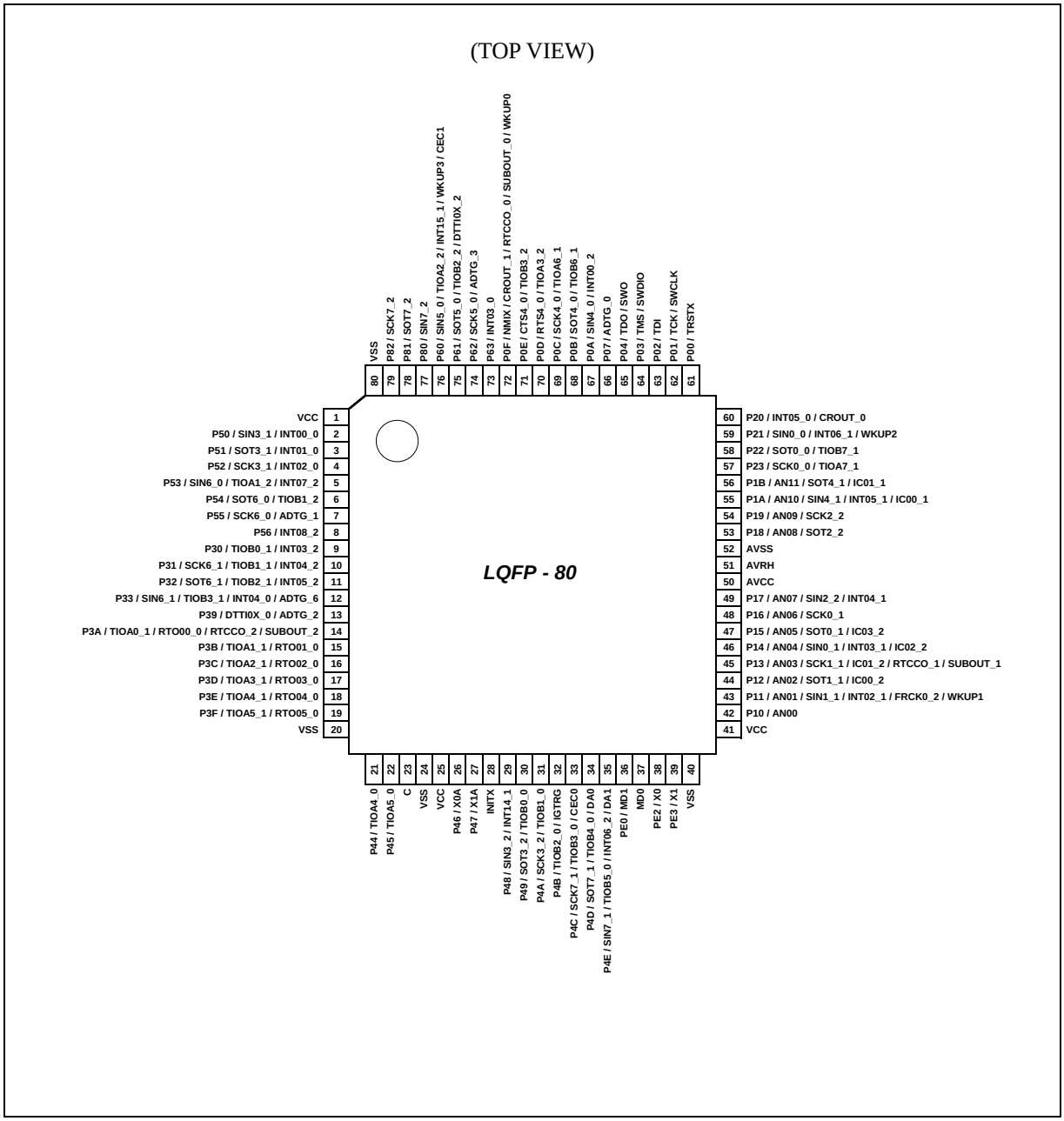
Package \ Product name	MB9AF131M MB9AF132M	MB9AF131N MB9AF132N
LQFP: FPT-80P-M37 (0.5mm pitch)	❍	-
LQFP: FPT-80P-M40 (0.65mm pitch)	❍	-
LQFP: FPT-100P-M23 (0.5mm pitch)	-	❍
QFP: FPT-100P-M06 (0.65mm pitch)	-	❍
BGA: BGA-112P-M04 (0.8mm pitch)	-	planning

❍ : Supported

Note : See "■PACKAGE DIMENSIONS" for detailed information on each package.

■ PIN ASSIGNMENT

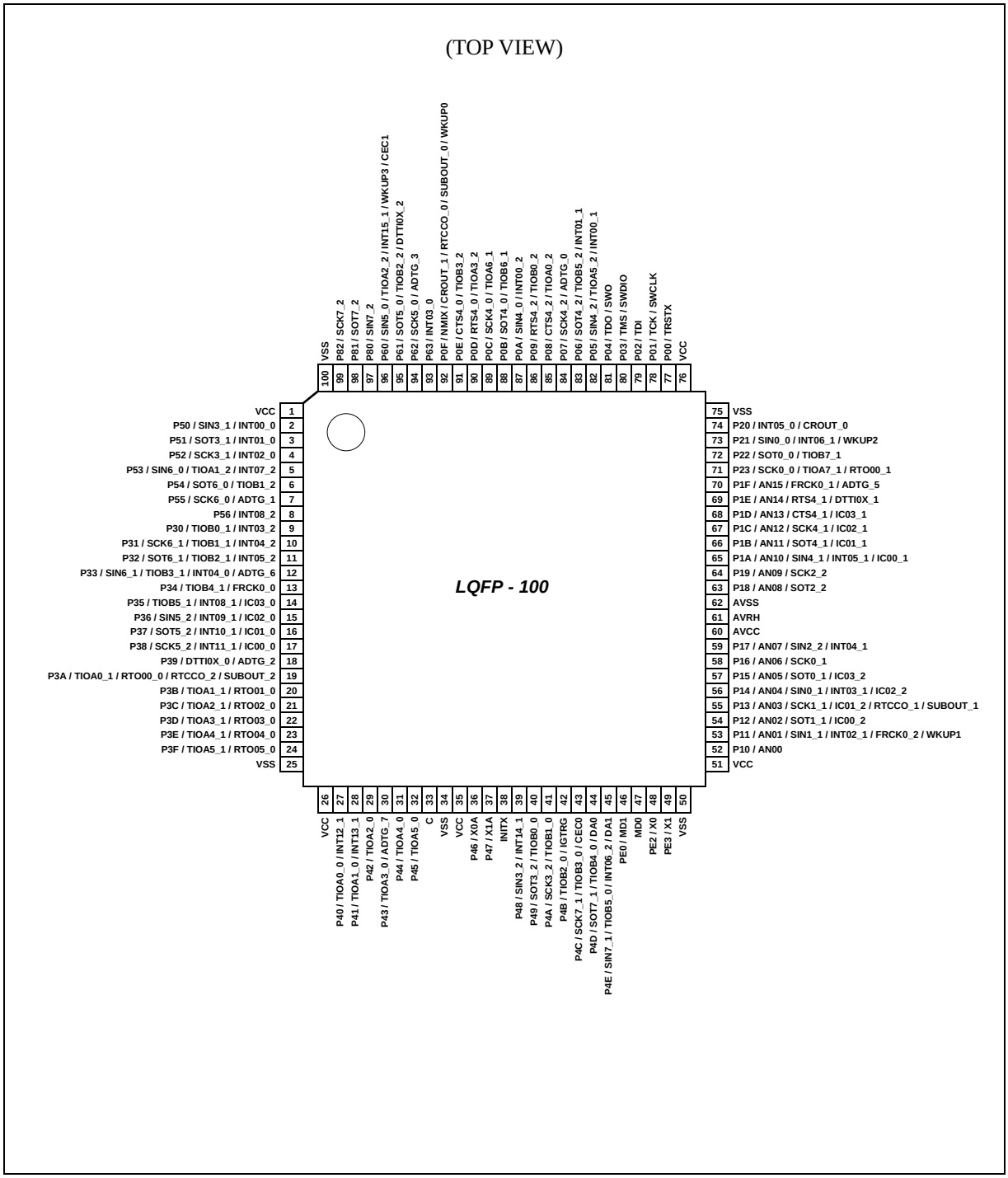
• FPT-80P-M37/M40



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

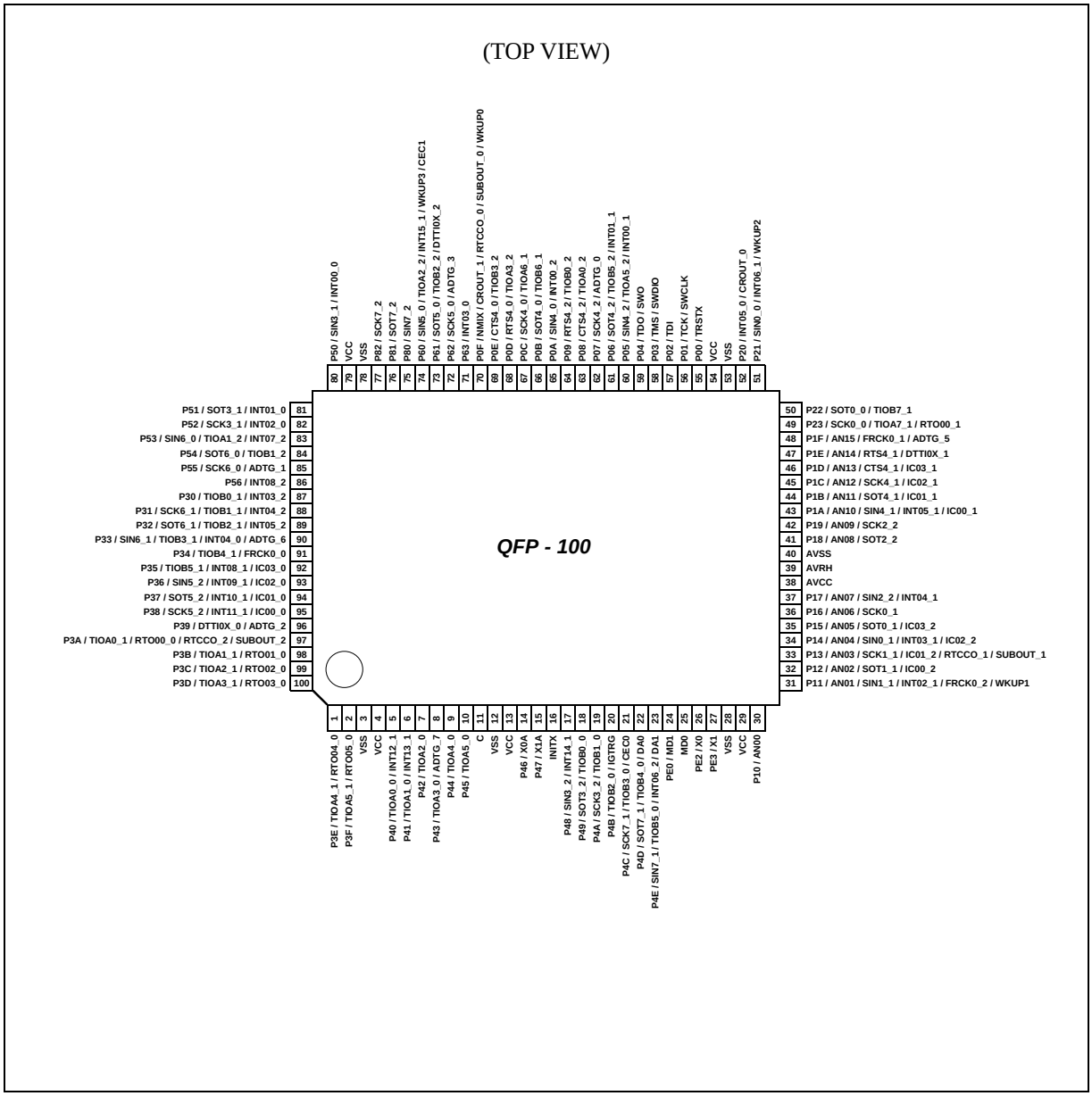
- FPT-100P-M23



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

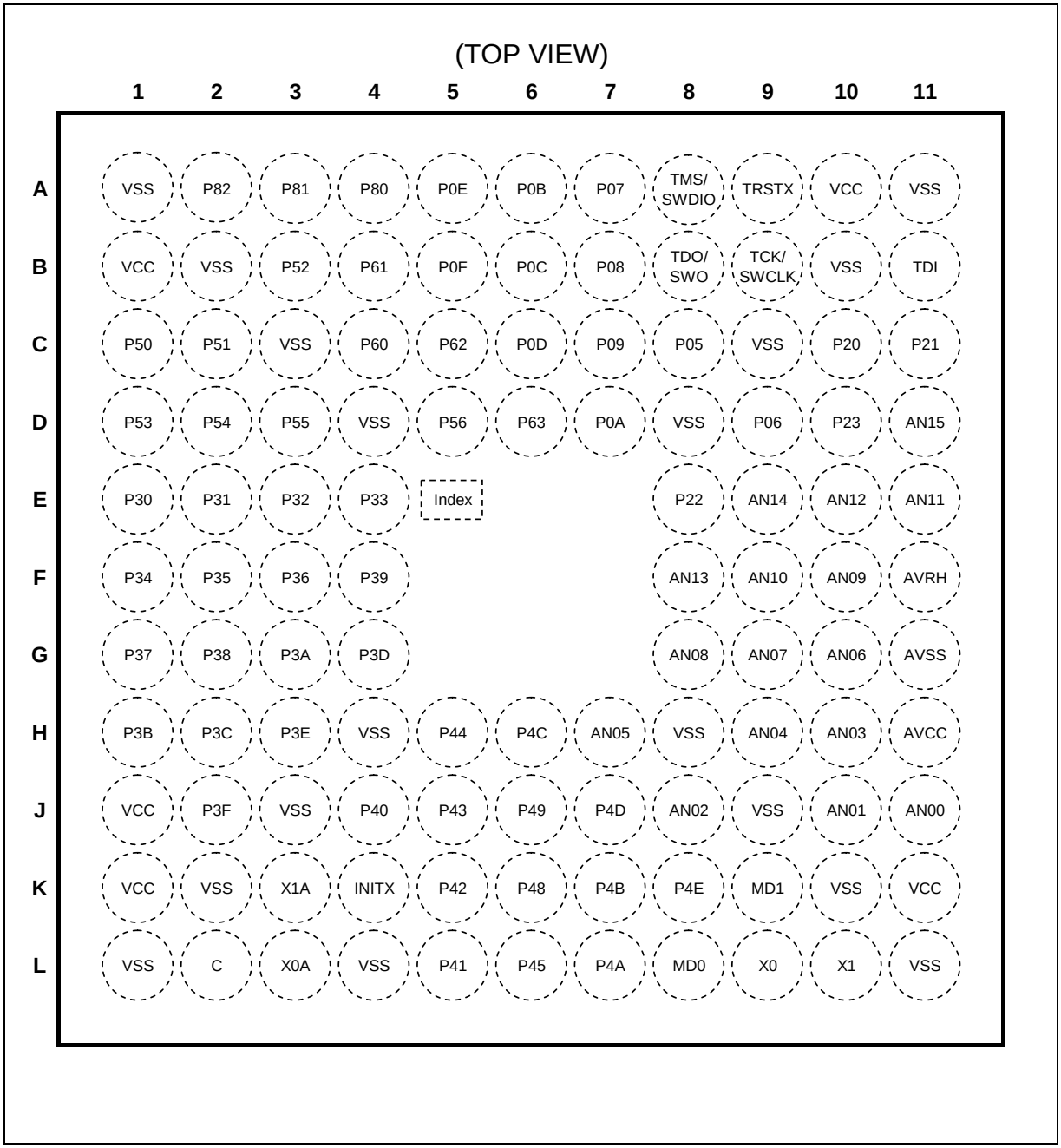
- FPT-100P-M06



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

• BGA-112P-M04



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ LIST OF PIN FUNCTIONS

- List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
1	1	79	B1	VCC	-	
2	2	80	C1	P50 INT00_0 SIN3_1	E	F
3	3	81	C2	P51 INT01_0 SOT3_1 (SDA3_1)	E	F
4	4	82	B3	P52 INT02_0 SCK3_1 (SCL3_1)	E	F
5	5	83	D1	P53 SIN6_0 TIOA1_2 INT07_2	E	F
6	6	84	D2	P54 SOT6_0 (SDA6_0) TIOB1_2	E	H
7	7	85	D3	P55 SCK6_0 (SCL6_0) ADTG_1	E	H
8	8	86	D5	P56 INT08_2	E	O
9	9	87	E1	P30 TIOB0_1 INT03_2	E	F
10	10	88	E2	P31 TIOB1_1 SCK6_1 (SCL6_1) INT04_2	E	F
11	11	89	E3	P32 TIOB2_1 SOT6_1 (SDA6_1) INT05_2	E	F

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
12	12	90	E4	P33 INT04_0 TIOB3_1 SIN6_1 ADTG_6	E	F
-	13	91	F1	P34 FRCK0_0 TIOB4_1	E	H
-	14	92	F2	P35 IC03_0 TIOB5_1 INT08_1	E	F
-	15	93	F3	P36 IC02_0 SIN5_2 INT09_1	E	F
-	16	94	G1	P37 IC01_0 SOT5_2 (SDA5_2) INT10_1	E	F
-	17	95	G2	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	F
13	18	96	F4	P39 DTTI0X_0 ADTG_2	E	H
14	19	97	G3	P3A RTO00_0 (PPG00_0) TIOA0_1 RTCCO_2 SUBOUT_2	E	H
15	20	98	H1	P3B RTO01_0 (PPG00_0) TIOA1_1	E	H
16	21	99	H2	P3C RTO02_0 (PPG02_0) TIOA2_1	E	H

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
17	22	100	G4	P3D RTO03_0 (PPG02_0) TIOA3_1	E	H
-	-	-	B2	VSS	-	
18	23	1	H3	P3E RTO04_0 (PPG04_0) TIOA4_1	E	H
19	24	2	J2	P3F RTO05_0 (PPG04_0) TIOA5_1	E	H
20	25	3	L1	VSS	-	
-	26	4	J1	VCC	-	
-	27	5	J4	P40 TIOA0_0 INT12_1	E	F
-	28	6	L5	P41 TIOA1_0 INT13_1	E	F
-	29	7	K5	P42 TIOA2_0	E	H
-	30	8	J5	P43 TIOA3_0 ADTG_7	E	H
21	31	9	H5	P44 TIOA4_0	E	H
22	32	10	L6	P45 TIOA5_0	E	H
-	-	-	K2	VSS	-	
-	-	-	J3	VSS	-	
-	-	-	H4	VSS	-	
23	33	11	L2	C	-	
24	34	12	L4	VSS	-	
25	35	13	K1	VCC	-	
26	36	14	L3	P46 X0A	D	M
27	37	15	K3	P47 X1A	D	N
28	38	16	K4	INITX	B	C
29	39	17	K6	P48 INT14_1 SIN3_2	E	F

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
30	40	18	J6	P49 TIOB0_0 SOT3_2 (SDA3_2)	E	H
31	41	19	L7	P4A TIOB1_0 SCK3_2 (SCL3_2)	E	H
32	42	20	K7	P4B TIOB2_0 IGTRG	E	H
33	43	21	H6	P4C TIOB3_0 SCK7_1 (SCL7_1) CEC0	G	Q
34	44	22	J7	P4D TIOB4_0 SOT7_1 (SDA7_1) DA0	J	T
35	45	23	K8	P4E TIOB5_0 INT06_2 SIN7_1 DA1	J	S
36	46	24	K9	PE0 MD1	C	P
37	47	25	L8	MD0	H	D
38	48	26	L9	PE2 X0	A	A
39	49	27	L10	PE3 X1	A	B
40	50	28	L11	VSS	-	
41	51	29	K11	VCC	-	
42	52	30	J11	P10 AN00	F	J
43	53	31	J10	P11 AN01 SIN1_1 INT02_1 FRCK0_2 WKUP1	F	L

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
44	54	32	J8	P12 AN02 SOT1_1 (SDA1_1) IC00_2	F	J
-	-	-	K10	VSS	-	
-	-	-	J9	VSS	-	
45	55	33	H10	P13 AN03 SCK1_1 (SCL1_1) IC01_2 RTCCO_1 SUBOUT_1	F	J
46	56	34	H9	P14 AN04 SIN0_1 INT03_1 IC02_2	F	K
47	57	35	H7	P15 AN05 SOT0_1 IC03_2	F	J
48	58	36	G10	P16 AN06 SCK0_1 (SCL0_1)	F	J
49	59	37	G9	P17 AN07 SIN2_2 INT04_1	F	K
50	60	38	H11	AVCC	-	
51	61	39	F11	AVRH	-	
52	62	40	G11	AVSS	-	
53	63	41	G8	P18 AN08 SOT2_2 (SDA2_2)	F	J
54	64	42	F10	P19 AN09 SCK2_2 (SCL2_2)	F	J
-	-	-	H8	VSS	-	

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
55	65	43	F9	P1A AN10 SIN4_1 INT05_1 IC00_1	F	K
56	66	44	E11	P1B AN11 SOT4_1 (SDA4_1) IC01_1	F	J
-	67	45	E10	P1C AN12 SCK4_1 (SCL4_1) IC02_1	F	J
-	68	46	F8	P1D AN13 CTS4_1 IC03_1	F	J
-	69	47	E9	P1E AN14 RTS4_1 DTTI0X_1	F	J
-	70	48	D11	P1F AN15 ADTG_5 FRCK0_1	F	J
-	-	-	B10	VSS	-	
-	-	-	C9	VSS	-	
57	71	49	D10	P23 SCK0_0 (SCL0_0) TIOA7_1	E	H
-				RTO00_1		
58	72	50	E8	P22 SOT0_0 (SDA0_0) TIOB7_1	E	H
59	73	51	C11	P21 SIN0_0 INT06_1 WKUP2	E	G
60	74	52	C10	P20 INT05_0 CROUT_0	E	F

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
-	75	53	A11	VSS	-	
-	76	54	A10	VCC	-	
61	77	55	A9	P00	E	E
				TRSTX		
62	78	56	B9	P01	E	E
				TCK		
				SWCLK		
63	79	57	B11	P02	E	E
				TDI		
64	80	58	A8	P03	E	E
				TMS		
				SWDIO		
65	81	59	B8	P04	E	E
				TDO		
				SWO		
-	82	60	C8	P05	E	F
				TIOA5_2		
				SIN4_2		
				INT00_1		
-	-	-	D8	VSS	-	
-	83	61	D9	P06	E	F
				TIOB5_2		
				SOT4_2 (SDA4_2)		
				INT01_1		
66	84	62	A7	P07	E	H
				ADTG_0		
-				SCK4_2 (SCL4_2)		
-	85	63	B7	P08	E	H
				TIOA0_2		
				CTS4_2		
-	86	64	C7	P09	E	H
				TIOB0_2		
				RTS4_2		
67	87	65	D7	P0A	G	F
				SIN4_0		
				INT00_2		
68	88	66	A6	P0B	G	H
				SOT4_0 (SDA4_0)		
				TIOB6_1		
69	89	67	B6	P0C	G	H
				SCK4_0 (SCL4_0)		
				TIOA6_1		

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-80	LQFP-100	QFP-100	BGA-112			
-	-	-	D4	VSS	-	
-	-	-	C3	VSS	-	
70	90	68	C6	P0D RTS4_0 TIOA3_2	E	H
71	91	69	A5	P0E CTS4_0 TIOB3_2	E	H
72	92	70	B5	P0F NMIX CROUT_1 RTCCO_0 SUBOUT_0 WKUP0	E	I
73	93	71	D6	P63 INT03_0	E	O
74	94	72	C5	P62 SCK5_0 (SCL5_0) ADTG_3	E	H
75	95	73	B4	P61 SOT5_0 (SDA5_0) TIOB2_2 DTTI0X_2	E	H
76	96	74	C4	P60 SIN5_0 TIOA2_2 INT15_1 WKUP3 CEC1	G	R
77	97	75	A4	P80 SIN7_2	G	H
78	98	76	A3	P81 SOT7_2	G	H
79	99	77	A2	P82 SCK7_2	G	H
80	100	78	A1	VSS	-	

- List of pin functions

  The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
ADC	ADTG_0	A/D converter external trigger input pin	66	84	62	A7
	ADTG_1		7	7	85	D3
	ADTG_2		13	18	96	F4
	ADTG_3		74	94	72	C5
	ADTG_4		-	-	-	-
	ADTG_5		-	70	48	D11
	ADTG_6		12	12	90	E4
	ADTG_7		-	30	8	J5
	ADTG_8		-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	42	52	30	J11
	AN01		43	53	31	J10
	AN02		44	54	32	J8
	AN03		45	55	33	H10
	AN04		46	56	34	H9
	AN05		47	57	35	H7
	AN06		48	58	36	G10
	AN07		49	59	37	G9
	AN08		53	63	41	G8
	AN09		54	64	42	F10
	AN10		55	65	43	F9
	AN11		56	66	44	E11
	AN12		-	67	45	E10
	AN13		-	68	46	F8
	AN14		-	69	47	E9
	AN15		-	70	48	D11

Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	-	27	5	J4
	TIOA0_1		14	19	97	G3
	TIOA0_2		-	85	63	B7
	TIOB0_0	Base timer ch.0 TIOB pin	30	40	18	J6
	TIOB0_1		9	9	87	E1
	TIOB0_2		-	86	64	C7
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	-	28	6	L5
	TIOA1_1		15	20	98	H1
	TIOA1_2		5	5	83	D1
	TIOB1_0	Base timer ch.1 TIOB pin	31	41	19	L7
	TIOB1_1		10	10	88	E2
	TIOB1_2		6	6	84	D2
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	-	29	7	K5
	TIOA2_1		16	21	99	H2
	TIOA2_2		76	96	74	C4
	TIOB2_0	Base timer ch.2 TIOB pin	32	42	20	K7
	TIOB2_1		11	11	89	E3
	TIOB2_2		75	95	73	B4
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	-	30	8	J5
	TIOA3_1		17	22	100	G4
	TIOA3_2		70	90	68	C6
	TIOB3_0	Base timer ch.3 TIOB pin	33	43	21	H6
	TIOB3_1		12	12	90	E4
	TIOB3_2		71	91	69	A5
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	21	31	9	H5
	TIOA4_1		18	23	1	H3
	TIOA4_2		-	-	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	34	44	22	J7
	TIOB4_1		-	13	91	F1
	TIOB4_2		-	-	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	22	32	10	L6
	TIOA5_1		19	24	2	J2
	TIOA5_2		-	82	60	C8
	TIOB5_0	Base timer ch.5 TIOB pin	35	45	23	K8
	TIOB5_1		-	14	92	F2
	TIOB5_2		-	83	61	D9
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	69	89	67	B6
	TIOB6_1	Base timer ch.6 TIOB pin	68	88	66	A6
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-	-	-
	TIOA7_1		57	71	49	D10
	TIOA7_2		-	-	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-	-	-
	TIOB7_1		58	72	50	E8
	TIOB7_2		-	-	-	-

Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
Debugger	SWCLK	Serial wire debug interface clock input pin	62	78	56	B9
	SWDIO	Serial wire debug interface data input / output pin	64	80	58	A8
	SWO	Serial wire viewer output pin	65	81	59	B8
	TRSTX	J-TAG reset input pin	61	77	55	A9
	TCK	J-TAG test clock input pin	62	78	56	B9
	TDI	J-TAG test data input pin	63	79	57	B11
	TMS	J-TAG test mode state input/output pin	64	80	58	A8
	TDO	J-TAG debug data output pin	65	81	59	B8
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	80	C1
	INT00_1		-	82	60	C8
	INT00_2		67	87	65	D7
	INT01_0	External interrupt request 01 input pin	3	3	81	C2
	INT01_1		-	83	61	D9
	INT02_0	External interrupt request 02 input pin	4	4	82	B3
	INT02_1		43	53	31	J10
	INT03_0	External interrupt request 03 input pin	73	93	71	D6
	INT03_1		46	56	34	H9
	INT03_2		9	9	87	E1
	INT04_0	External interrupt request 04 input pin	12	12	90	E4
	INT04_1		49	59	37	G9
	INT04_2		10	10	88	E2
	INT05_0	External interrupt request 05 input pin	60	74	52	C10
	INT05_1		55	65	43	F9
	INT05_2		11	11	89	E3
	INT06_1	External interrupt request 06 input pin	59	73	51	C11
	INT06_2		35	45	23	K8
	INT07_2	External interrupt request 07 input pin	5	5	83	D1
	INT08_1	External interrupt request 08 input pin	-	14	92	F2
	INT08_2		8	8	86	D5
	INT09_1	External interrupt request 09 input pin	-	15	93	F3
	INT10_1	External interrupt request 10 input pin	-	16	94	G1
	INT11_1	External interrupt request 11 input pin	-	17	95	G2
	INT12_1	External interrupt request 12 input pin	-	27	5	J4
	INT13_1	External interrupt request 13 input pin	-	28	6	L5
	INT14_1	External interrupt request 14 input pin	29	39	17	K6
	INT15_1	External interrupt request 15 input pin	76	96	74	C4
	NMIX	Non-Maskable Interrupt input pin	72	92	70	B5

Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
GPIO	P00	General-purpose I/O port 0	61	77	55	A9
	P01		62	78	56	B9
	P02		63	79	57	B11
	P03		64	80	58	A8
	P04		65	81	59	B8
	P05		-	82	60	C8
	P06		-	83	61	D9
	P07		66	84	62	A7
	P08		-	85	63	B7
	P09		-	86	64	C7
	P0A		67	87	65	D7
	P0B		68	88	66	A6
	P0C		69	89	67	B6
	P0D		70	90	68	C6
	P0E		71	91	69	A5
	P0F		72	92	70	B5
	P10	General-purpose I/O port 1	42	52	30	J11
	P11		43	53	31	J10
	P12		44	54	32	J8
	P13		45	55	33	H10
	P14		46	56	34	H9
	P15		47	57	35	H7
	P16		48	58	36	G10
	P17		49	59	37	G9
	P18		53	63	41	G8
	P19		54	64	42	F10
	P1A		55	65	43	F9
	P1B		56	66	44	E11
	P1C		-	67	45	E10
	P1D		-	68	46	F8
	P1E		-	69	47	E9
	P1F		-	70	48	D11
	P20	General-purpose I/O port 2	60	74	52	C10
	P21		59	73	51	C11
	P22		58	72	50	E8
	P23		57	71	49	D10

Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
GPIO	P30	General-purpose I/O port 3	9	9	87	E1
	P31		10	10	88	E2
	P32		11	11	89	E3
	P33		12	12	90	E4
	P34		-	13	91	F1
	P35		-	14	92	F2
	P36		-	15	93	F3
	P37		-	16	94	G1
	P38		-	17	95	G2
	P39		13	18	96	F4
	P3A		14	19	97	G3
	P3B		15	20	98	H1
	P3C		16	21	99	H2
	P3D		17	22	100	G4
	P3E		18	23	1	H3
	P3F		19	24	2	J2
	P40	General-purpose I/O port 4	-	27	5	J4
	P41		-	28	6	L5
	P42		-	29	7	K5
	P43		-	30	8	J5
	P44		21	31	9	H5
	P45		22	32	10	L6
	P46		26	36	14	L3
	P47		27	37	15	K3
	P48		29	39	17	K6
	P49		30	40	18	J6
	P4A		31	41	19	L7
	P4B		32	42	20	K7
	P4C		33	43	21	H6
	P4D		34	44	22	J7
	P4E		35	45	23	K8
	P50	General-purpose I/O port 5	2	2	80	C1
	P51		3	3	81	C2
	P52		4	4	82	B3
	P53		5	5	83	D1
	P54		6	6	84	D2
	P55		7	7	85	D3
	P56		8	8	86	D5
	P60	General-purpose I/O port 6	76	96	74	C4
	P61		75	95	73	B4
	P62		74	94	72	C5
	P63		73	93	71	D6
	P80	General-purpose I/O port 8	77	97	75	A4
	P81		78	98	76	A3
	P82		79	99	77	A2
	PE0	General-purpose I/O port E	36	46	24	K9
	PE2		38	48	26	L9
	PE3		39	49	27	L10

Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	59	73	51	C11
	SIN0_1		46	56	34	H9
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I^2C (operation mode 4).	58	72	50	E8
	SOT0_1 (SDA0_1)		47	57	35	H7
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I^2C (operation mode 4).	57	71	49	D10
	SCK0_1 (SCL0_1)		48	58	36	G10
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	43	53	31	J10
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I^2C (operation mode 4).	44	54	32	J8
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I^2C (operation mode 4).	45	55	33	H10
Multi-function Serial 2	SIN2_2	Multi-function serial interface ch.2 input pin	49	59	37	G9
	SOT2_2 (SDA2_2)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I^2C (operation mode 4).	53	63	41	G8
	SCK2_2 (SCL2_2)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	54	64	42	F10

Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	2	80	C1
	SIN3_2		29	39	17	K6
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I^2C (operation mode 4).	3	3	81	C2
	SOT3_2 (SDA3_2)		30	40	18	J6
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	4	82	B3
	SCK3_2 (SCL3_2)		31	41	19	L7
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	67	87	65	D7
	SIN4_1		55	65	43	F9
	SIN4_2		-	82	60	C8
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I^2C (operation mode 4).	68	88	66	A6
	SOT4_1 (SDA4_1)		56	66	44	E11
	SOT4_2 (SDA4_2)		-	83	61	D9
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	69	89	67	B6
	SCK4_1 (SCL4_1)		-	67	45	E10
	SCK4_2 (SCL4_2)		-	84	62	A7
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	70	90	68	C6
	RTS4_1		-	69	47	E9
	RTS4_2		-	86	64	C7
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	71	91	69	A5
	CTS4_1		-	68	46	F8
	CTS4_2		-	85	63	B7

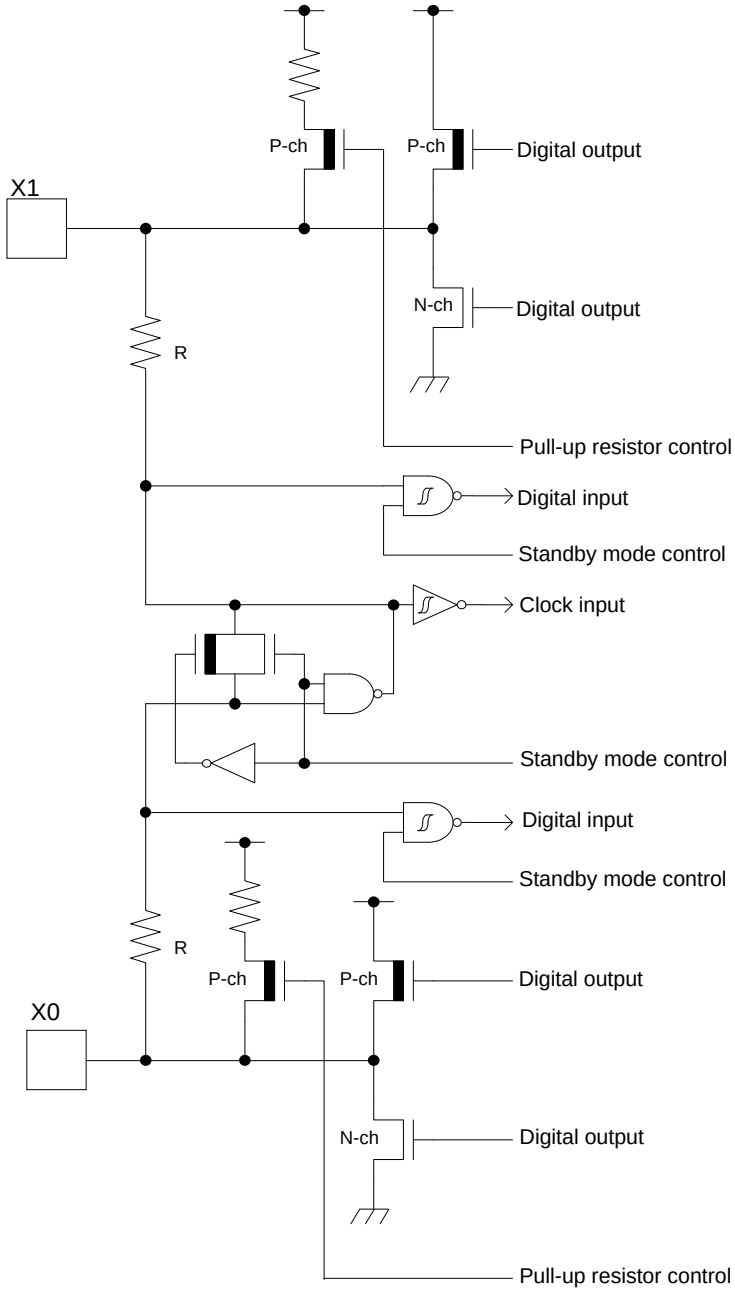
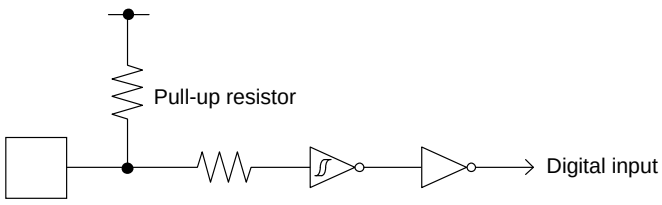
Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	76	96	74	C4
	SIN5_2		-	15	93	F3
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I^2C (operation mode 4).	75	95	73	B4
	SOT5_2 (SDA5_2)		-	16	94	G1
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I^2C (operation mode 4).	74	94	72	C5
	SCK5_2 (SCL5_2)		-	17	95	G2
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	5	5	83	D1
	SIN6_1		12	12	90	E4
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I^2C (operation mode 4).	6	6	84	D2
	SOT6_1 (SDA6_1)		11	11	89	E3
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	7	7	85	D3
	SCK6_1 (SCL6_1)		10	10	88	E2
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	35	45	23	K8
	SIN7_2		77	97	75	A4
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I^2C (operation mode 4).	34	44	22	J7
	SOT7_2 (SDA7_2)		78	98	76	A3
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	33	43	21	H6
	SCK7_2 (SCL7_2)		79	99	77	A2

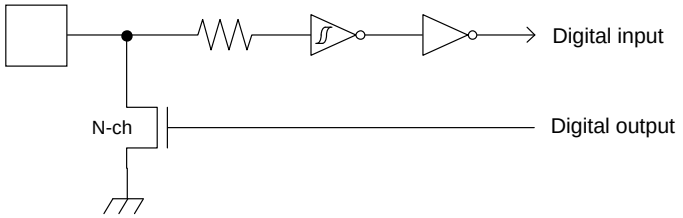
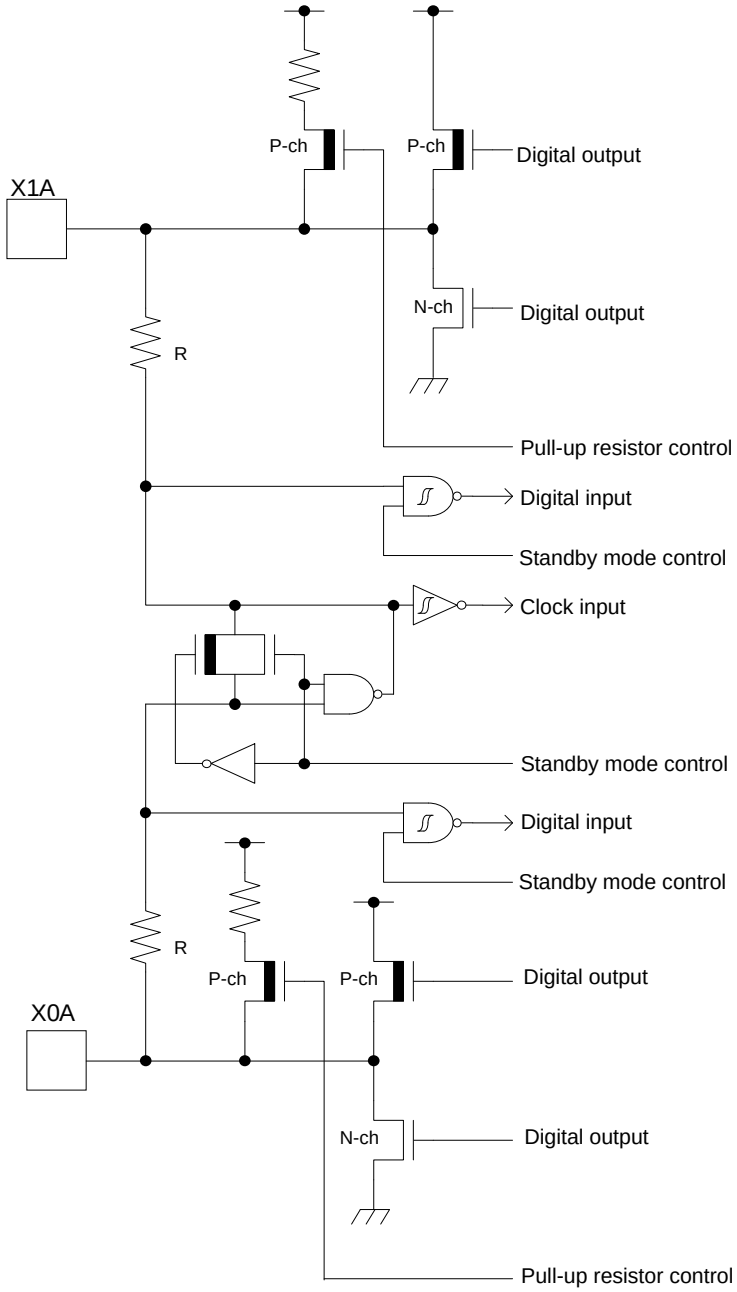
Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0	13	18	96	F4
	DTTI0X_1		-	69	47	E9
	DTTI0X_2		75	95	73	B4
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	-	13	91	F1
	FRCK0_1		-	70	48	D11
	FRCK0_2		43	53	31	J10
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes a channel number.	-	17	95	G2
	IC00_1		55	65	43	F9
	IC00_2		44	54	32	J8
	IC01_0		-	16	94	G1
	IC01_1		56	66	44	E11
	IC01_2		45	55	33	H10
	IC02_0		-	15	93	F3
	IC02_1		-	67	45	E10
	IC02_2		46	56	34	H9
	IC03_0		-	14	92	F2
	IC03_1		-	68	46	F8
	IC03_2		47	57	35	H7
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	14	19	97	G3
	RTO00_1 (PPG00_1)		-	71	49	D10
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	15	20	98	H1
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	16	21	99	H2
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	17	22	100	G4
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	18	23	1	H3
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	19	24	2	J2
	IGTRG	PPG IGBT mode external trigger input pin	32	42	20	K7

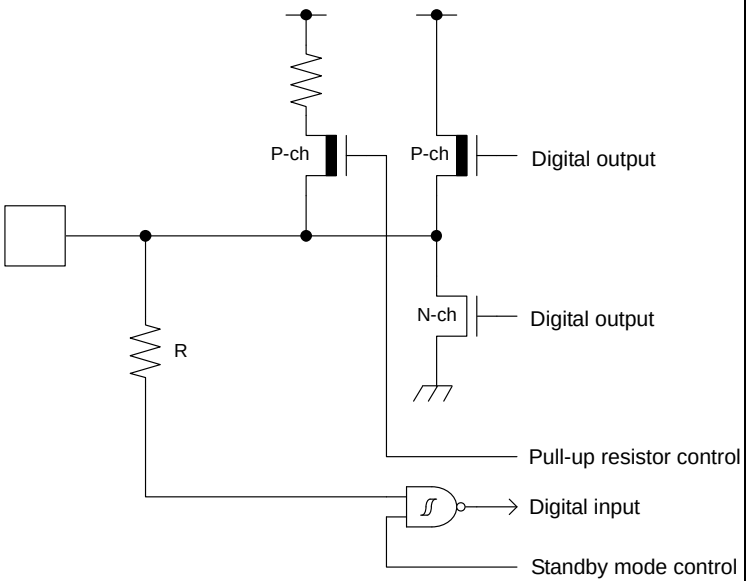
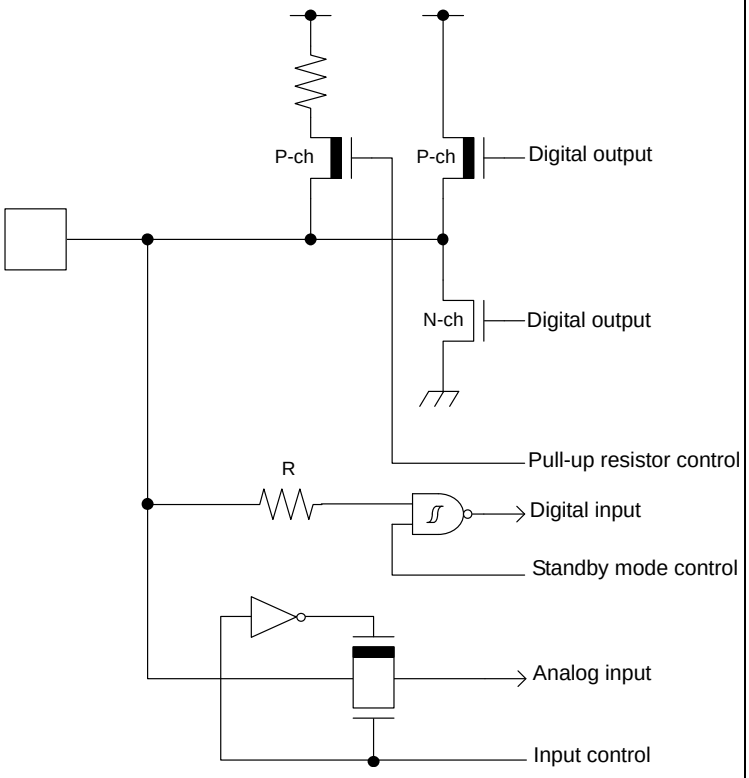
Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
Real-time clock	RTCCO_0	Pulse output pin of Real-time clock	72	92	70	B5
	RTCCO_1		45	55	33	H10
	RTCCO_2		14	19	97	G3
	SUBOUT_0	Sub clock output pin	72	92	70	B5
	SUBOUT_1		45	55	33	H10
	SUBOUT_2		14	19	97	G3
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	72	92	70	B5
	WKUP1	Deep standby mode return signal input pin 1	43	53	31	J10
	WKUP2	Deep standby mode return signal input pin 2	59	73	51	C11
	WKUP3	Deep standby mode return signal input pin 3	76	96	74	C4
DAC	DA0	D/A converter ch.0 analog output pin	34	44	22	J7
	DA1	D/A converter ch.1 analog output pin	35	45	23	K8
HDMI-CEC	CEC0	HDMI-CEC ch.0 pin	33	43	21	H6
	CEC1	HDMI-CEC ch.1 pin	76	96	74	C4

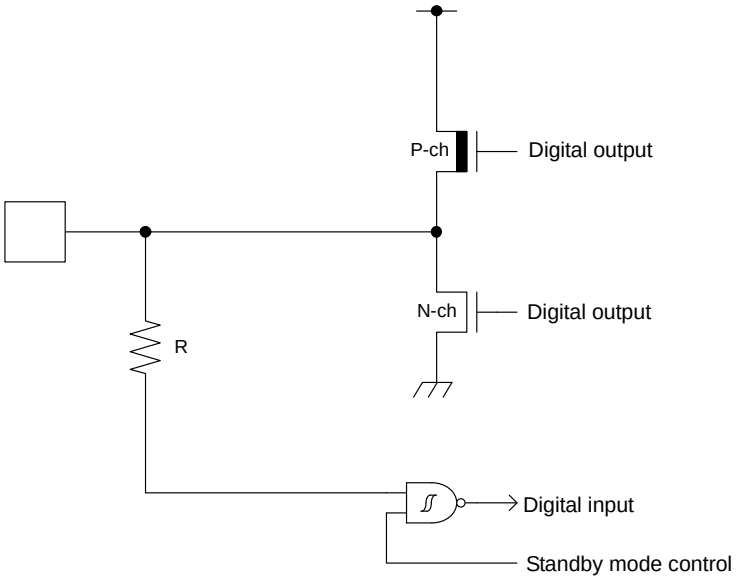
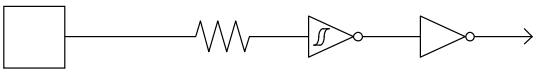
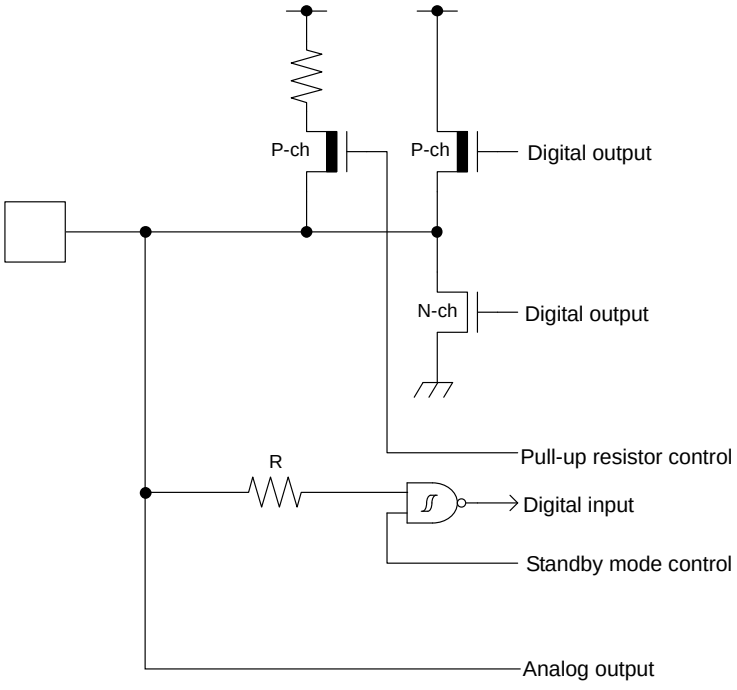
Pin function	Pin name	Function description	Pin No			
			LQFP-80	LQFP-100	QFP-100	BGA-112
RESET	INITX	External Reset Input Pin. A reset is valid when INITX = "L".	28	38	16	K4
Mode	MD0	Mode 0 pin. During normal operation, MD0 = "L" must be input. During serial programming to Flash memory, MD0 = "H" must be input.	37	47	25	L8
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	36	46	24	K9
POWER	VCC	Power supply pin	1	1	79	B1
			-	26	4	J1
			25	35	13	K1
			41	51	29	K11
			-	76	54	A10
GND	VSS	GND pin	-	-	-	B2
			20	25	3	L1
			-	-	-	K2
			-	-	-	J3
			-	-	-	H4
			24	34	12	L4
			40	50	28	L11
			-	-	-	K10
			-	-	-	J9
			-	-	-	H8
			-	-	-	B10
			-	-	-	C9
			-	75	53	A11
			-	-	-	D8
			-	-	-	D4
			-	-	-	C3
			80	100	78	A1
CLOCK	X0	Main clock (oscillation) input pin	38	48	26	L9
	X0A	Sub clock (oscillation) input pin	26	36	14	L3
	X1	Main clock (oscillation) I/O pin	39	49	27	L10
	X1A	Sub clock (oscillation) I/O pin	27	37	15	K3
	CROUT_0	Built-in high-speed CR-osc clock output port	60	74	52	C10
	CROUT_1		72	92	70	B5
Analog POWER	AVCC	A/D converter and D/A converter analog power supply pin	50	60	38	H11
	AVRH	A/D converter analog reference voltage input pin	51	61	39	F11
Analog GND	AVSS	A/D converter and D/A converter GND pin	52	62	40	G11
C pin	C	Power supply stabilization capacity pin	23	33	11	L2

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function. When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50kΩ

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 5MΩ • With standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With standby mode control • 5 V tolerant input • I_{OH} = -4mA, I_{OL} = 4mA • Available to control PZR registers. P0B, P0C, P4C, P60, P81, P82 only.
H		CMOS level hysteresis input
J		• CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

Code: DS00-00004-2Ea

- Observance of Safety Regulations and Standards

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

  FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- Lead-Free Packaging

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://edevice.fujitsu.com/fj/handling-e.pdf

■ HANDLING DEVICES

- Power supply pins

  In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

  Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pin and GND pin near this device.

- Crystal oscillator circuit

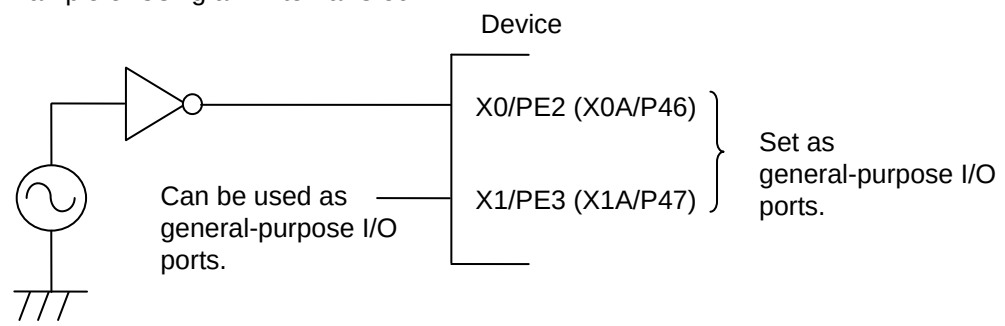
  Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

  It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

- Using an external clock

  To use the external clock, set general-purpose I/O ports to input the clock to X0/PE2 and X0A/P46 pin.

  • Example of Using an External Clock

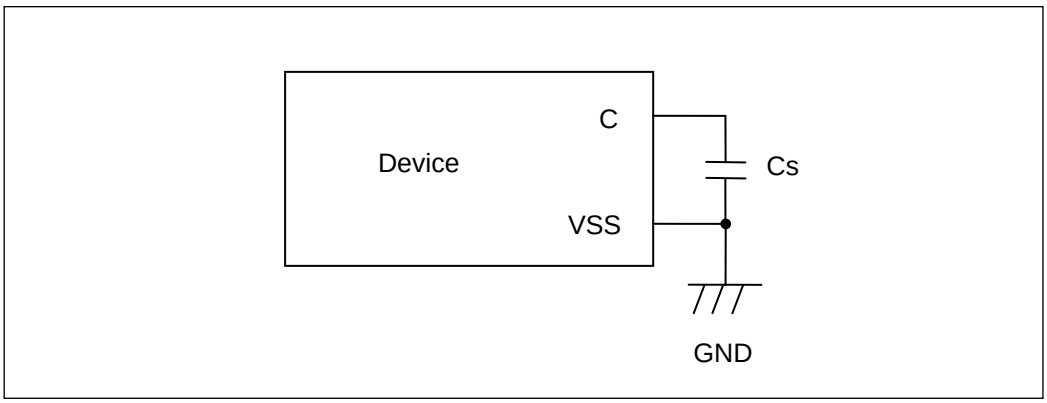


- Handling when using Multi-function serial pin as I^2C pin

  If it is using the multi-function serial pin as I^2C pins, P-ch transistor of digital output is always disabled. However, I^2C pins need to keep the electrical characteristic like other pins and not to connect to the external I^2C bus system with power OFF.

- C Pin

  This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
  However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
  A smoothing capacitor of about 4.7µF would be recommended for this series.



- Mode pins (MD0, MD1)

  Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on

  Turn power on/off in the following order or at the same time.
  If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

  Turning on : VCC → AVCC → AVRH

  Turning off : AVRH → AVCC → VCC

- Serial Communication

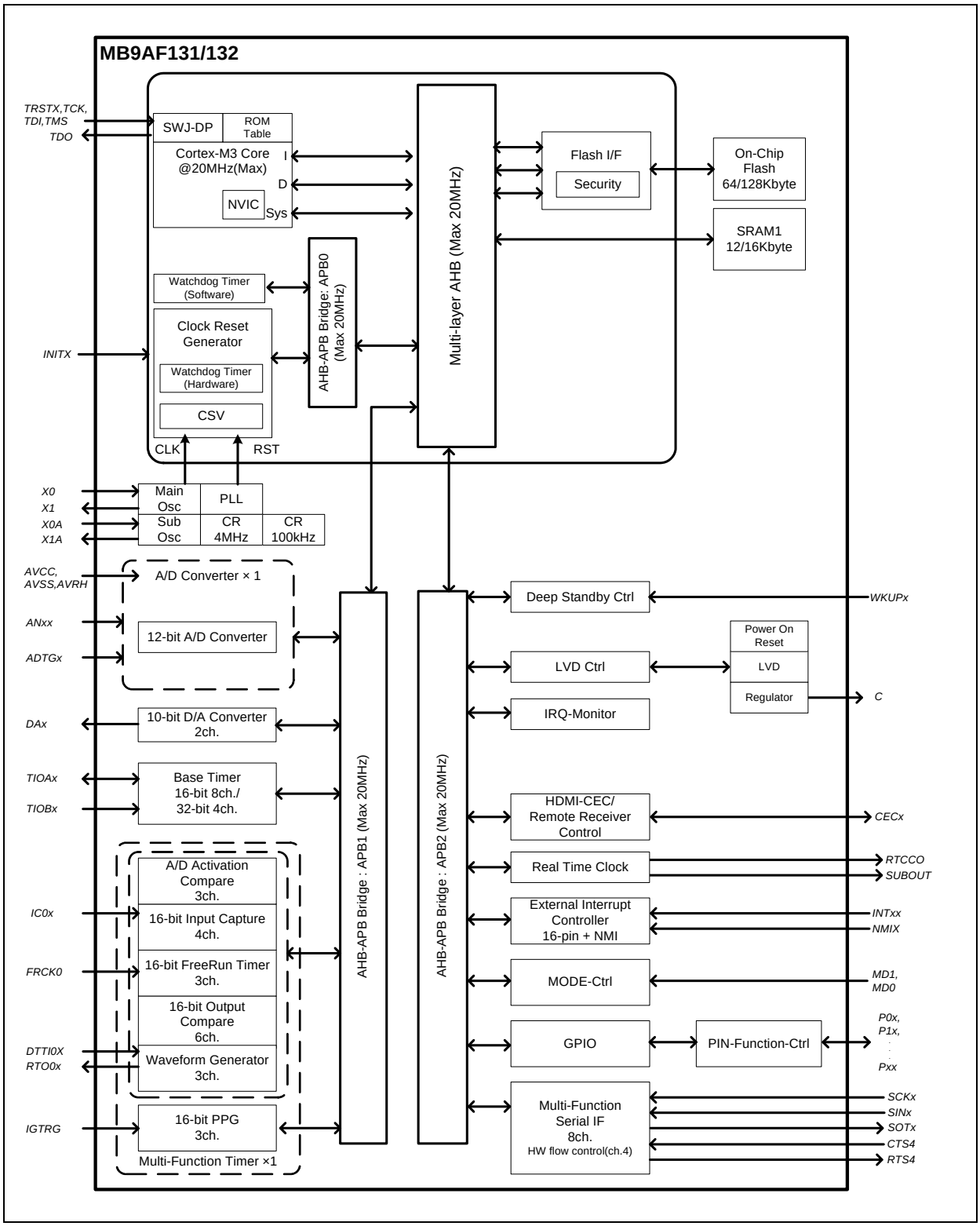
  There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
  Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

- Differences in features among the products with different memory sizes and between Flash memory products and MASK products

  The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

  If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

■ BLOCK DIAGRAM

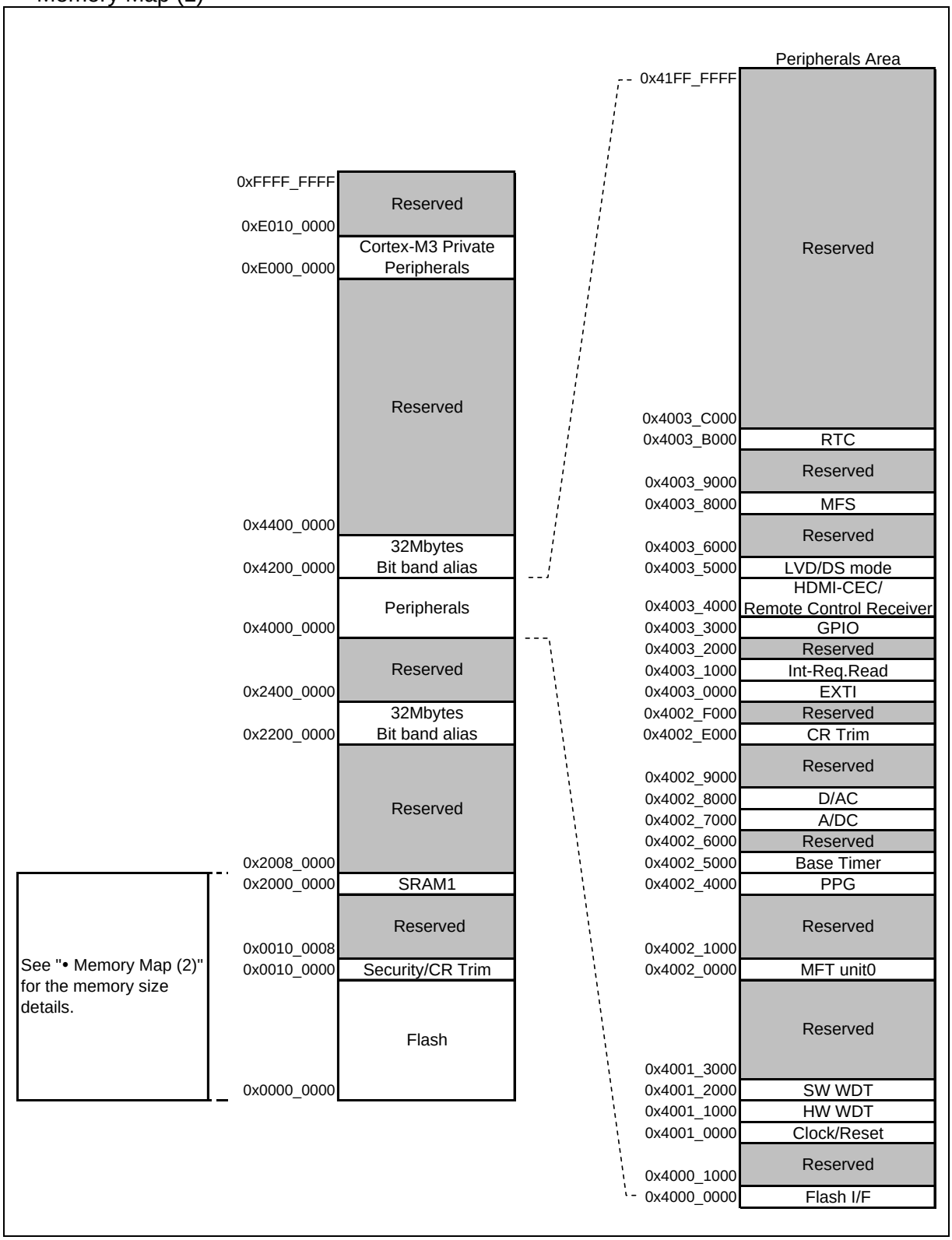


■ MEMORY SIZE

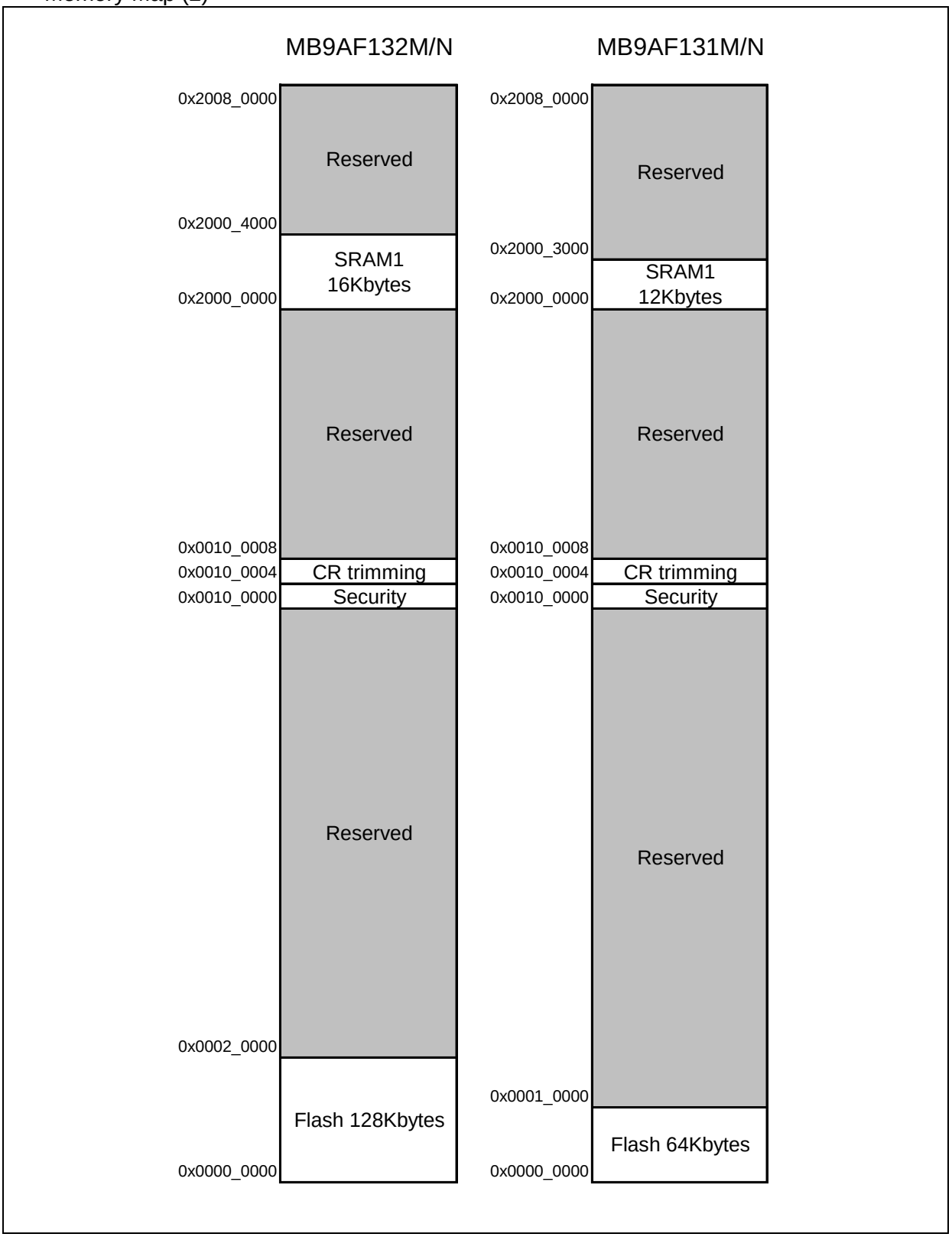
See " • Memory size" in "■PRODUCT LINEUP" to confirm the memory size.

■ MEMORY MAP

• Memory Map (1)



• Memory Map (2)


MB9AF132M/N
0x2008_0000
Reserved
0x2000_4000
SRAM1
16Kbytes
0x2000_0000
Reserved
0x0010_0008
0x0010_0004
CR trimming
0x0010_0000
Security
Reserved
0x0002_0000
Flash 128Kbytes
0x0000_0000
MB9AF131M/N
0x2008_0000
Reserved
0x2000_3000
SRAM1
12Kbytes
0x2000_0000
Reserved
0x0010_0008
0x0010_0004
CR trimming
0x0010_0000
Security
Reserved
0x0001_0000
Flash 64Kbytes
0x0000_0000

• Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Reserved
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Reserved
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_8FFF		D/A Converter
0x4002_9000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt
0x4003_1000	0x4003_1FFF		Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		HDMI-CEC/ Remote Control Receiver
0x4003_5000	0x4003_50FF		Low-Voltage Detector
0x4003_5100	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Reserved
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		Reserved
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x41FF_FFFF		Reserved

■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- INITX = 0
  This is the period when the INITX pin is the "L" level.
- INITX = 1
  This is the period when the INITX pin is the "H" level.
- SPL = 0
  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".
- SPL = 1
  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".
- Input enabled
  Indicates that the input function can be used.
- Internal input fixed at "0"
  This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z
  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled
  Indicates that the setting is disabled.
- Maintain previous state
  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.
- Analog input is enabled
  Indicates that the analog input is enabled.
- Trace output
  Indicates that the trace function can be used.
- GPIO selected
  In Deep standby mode, pins switch to the general-purpose I/O port.

- List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stops*1, output maintains previous state / Internal input fixed at "0"	Hi-Z / Input enabled / When oscillation stops*1, Hi-Z / Internal input fixed at "0"	Output maintains previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintains previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Output maintains previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state
B	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at "0"
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Output maintains previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"		Hi-Z / Internal input fixed at "0"	
F	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state
G	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled			Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
H	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state
I	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									Maintain previous state
J	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected						Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
M	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stops*2, output maintains previous state / Internal input fixed at "0"	Hi-Z / Input enabled / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, output maintains previous state / Internal input fixed at "0"	Hi-Z / Input enabled / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When Return from Deep Standby STOP mode, GPIO is selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintains previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Output maintains previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state
N	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Output maintains previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
O	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"	Output maintains previous state / Internal input fixed at "0"		Maintain previous state
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / input enabled	Maintain previous state	Hi-Z / input enabled	Maintain previous state
Q	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
R	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected						Maintain previous state	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state
S	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled		Maintain previous state	Maintain previous state			
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or SLEEP mode state	Timer mode, RTC mode, or STOP mode state		Deep standby RTC mode or Deep standby STOP mode state		Return from Deep standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
T	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Maintain previous state	Hi-Z / Internal input fixed at "0"			
	GPIO selected							Output maintains previous state / Internal input fixed at "0"		Maintain previous state

*1 : Oscillation is stopped at Sub run mode, Low-speed CR run mode, Sub SLEEP mode, Low-speed CR SLEEP mode, Sub timer mode, Low-speed CR timer mode, RTC mode, STOP mode, Deep standby RTC mode, and Deep standby STOP mode.

*2 : Oscillation is stopped at STOP mode and Deep standby STOP mode.

*3 : Maintain previous state at timer mode. GPIO selected Internal input fixed at "0" at RTC mode, STOP mode.

*4 : Maintain previous state at timer mode. Hi-Z/Internal input fixed at "0" at RTC mode, STOP mode.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1,*3	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1,*3	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
"L" level maximum output current*4	I_{OL}	-	10	mA	
"L" level average output current*5	I_{OLAV}	-	4	mA	
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current*6	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current*4	I_{OH}	-	- 10	mA	
"H" level average output current*5	I_{OHAV}	-	- 4	mA	
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current*6	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	400	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1 : These parameters are based on the condition that $V_{SS} = AV_{SS} = 0V$.
*2 : V_{CC} must not drop below V_{SS} - 0.5V.
*3 : Be careful not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.
*4 : The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
*5 : The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.
*6 : The total average output current is defined as the average current value flowing through all of corresponding pins for a 100ms.

<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	1.8	5.5	V	
Analog power supply voltage		AV_{CC}	-	1.8	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage		AVRH	-	2.7	AV_{CC}	V	$AV_{CC} \geq 2.7V$
				AV_{CC}			AV_{CC} < 2.7V
Smoothing capacitor		C_S	-	1	10	µF	For Regulator *
Operating Temperature	FPT-80P-M37, FPT-80P-M40, FPT-100P-M23, FPT-100P-M06, BGA-112P-M04	Ta	-	- 40	+ 85	°C	

* : See "●C Pin" in "■HANDLING DEVICES" for the smoothing capacitor.

<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

3. DC Characteristics

(1) Current Rating

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ*4	Max		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	-	19	24	mA	CPU : 20MHz, Peripheral : 20MHz, Flash memory 0Wait, FRWTR.RWT = 00, FSYNDN.SD = 000 *1
				-	9.5	12.5	mA	CPU : 20MHz, Peripheral : clock stopped, NOP operation *1
			Normal operation (built-in high-speed CR)	-	4.5	5.5	mA	CPU / Peripheral : 4MHz*2, Flash memory 0Wait, FRWTR.RWT = 00, FSYNDN.SD = 000 *1
			Normal operation (sub oscillation)	-	0.25	0.55	mA	CPU / Peripheral : 32kHz, Flash memory 0Wait, FRWTR.RWT = 00, FSYNDN.SD = 000 *1
			Normal operation (built-in low-speed CR)	-	0.3	0.95	mA	CPU / Peripheral : 100kHz, Flash memory 0Wait, FRWTR.RWT = 00, FSYNDN.SD = 000 *1
	I_{CCS}		SLEEP operation (PLL)	-	8	10.5	mA	Peripheral : 20MHz *1
			SLEEP operation (built-in high-speed CR)	-	2	2.5	mA	Peripheral : 4MHz*2 *1
			SLEEP operation (sub oscillation)	-	0.2	0.45	mA	Peripheral : 32kHz *1
			SLEEP operation (built-in low-speed CR)	-	0.25	0.65	mA	Peripheral : 100kHz *1
	I_{CCT}		TIMER mode (sub oscillation)	-	7.5	60	µA	Ta = + 25°C, When LVD is off *1, *3
				-	16	150	µA	Ta = + 85°C, When LVD is off *1, *3

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ*4	Max		
Power supply current	I_{CCR}	VCC	RTC mode	-	1.5	6.5	µA	Ta = + 25°C, When LVD is off *1, *3
				-	6	89	µA	Ta = + 85°C, When LVD is off *1, *3
	I_{CCRD}		Deep standby RTC mode	-	1.3	4.5	µA	Ta = + 25°C, When LVD is off *1, *3
				-	3	32	µA	Ta = + 85°C, When LVD is off *1, *3
	I_{CCH}		STOP mode	-	0.6	5	µA	Ta = + 25°C, When LVD is off *1
				-	4.2	87	µA	Ta = + 85°C, When LVD is off *1
	I_{CCHD}		Deep standby STOP mode	-	0.4	3	µA	Ta = + 25°C, When LVD is off *1
				-	1.4	30	µA	Ta = + 85°C, When LVD is off *1
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}		For occurrence of reset or for occurrence of interrupt in normal mode operation	-	10	20	µA	When not detected
			For occurrence of reset and for occurrence of interrupt in normal mode operation	-	14	30	µA	
			For occurrence of interrupt in low power mode operation	-	0.3	2	µA	

*1: When all ports are fixed.
*2: When setting it to 4MHz by trimming.
*3: When using sub crystal oscillator.
*4: When V_{CC}=3.3V

(2) Pin Characteristics

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	MD0, MD1, PE0, PE2, PE3, P46, P47, P3A, P3B, P3C, P3D, P3E, P3F, INITX	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
		P0A, P0B, P0C, P4C, P60, P80, P81, P82	-	V_{CC} × 0.7	-	V_{SS} + 5.5	V	5V tolerant
		CMOS hysteresis input pins other than the above	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	
"L" level input voltage (hysteresis input)	V_{ILS}	MD0, MD1, PE0, PE2, PE3, P46, P47, INITX	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
		CMOS hysteresis input pins other than the above	-	V_{SS} - 0.3	-	V_{CC} × 0.3	V	
"H" level output voltage	V_{OH}	Pxx	$V_{CC} \geq 4.5$ V, I_{OH} = - 4mA	V_{CC} - 0.5	-	V_{CC}	V	
			$V_{CC} < 4.5$ V, I_{OH} = - 1mA					
"L" level output voltage	V_{OL}	Pxx	$V_{CC} \geq 4.5$ V, I_{OL} = 4mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2mA					
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	40	100	400		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

4. AC Characteristics

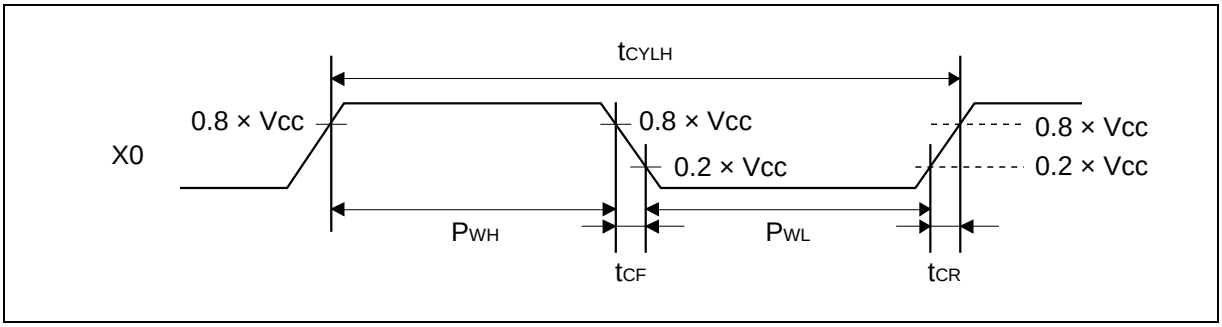
(1) Main Clock Input Characteristics

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	$V_{CC} \geq 2.0V$	4	20	MHz	When crystal oscillator is connected
			$V_{CC} < 2.0V$	4	4	MHz	
			$V_{CC} \geq 4.5V$	4	20	MHz	When using external clock
			$V_{CC} < 4.5V$	4	16	MHz	
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5V$	50	250	ns	When using external clock
			$V_{CC} < 4.5V$	62.5	250	ns	
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	20	MHz	Master clock
	F_{CC}	-	-	-	20	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	20	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	20	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	20	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	50	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	50	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	50	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	50	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "Chapter: Clock" in " FM3 Family PERIPHERAL MANUAL ".

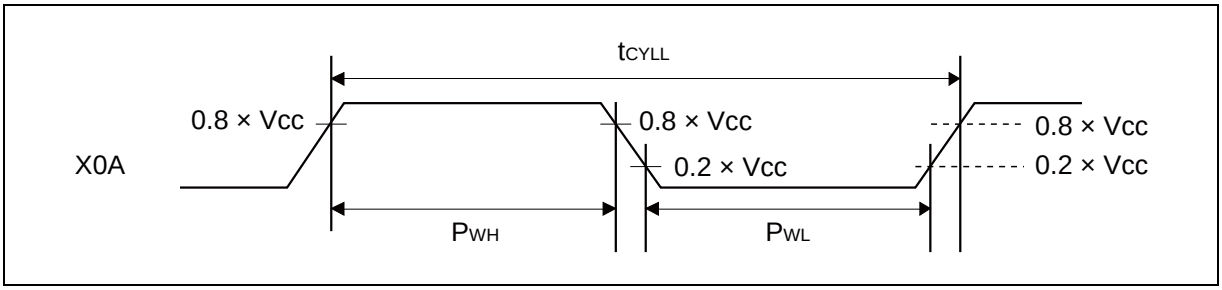
*2: For about each APB bus which each peripheral is connected to, see "■BLOCK DIAGRAM" in this data sheet.



(2) Sub Clock Input Characteristics

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



(3) Built-in CR Oscillation Characteristics

- Built-in high-speed CR

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions		Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CRH}	$V_{CC} \geq$ 2.2 V	Ta = + 25°C	3.92	4	4.08	MHz	When trimming*
			Ta = - 40°C to + 85°C	3.8	4	4.2		
			Ta = - 40°C to + 85°C	2.3	-	7.03		When not trimming
		V_{CC} < 2.2 V	Ta = + 25°C	3.4	4	4.6	MHz	When trimming*
			Ta = - 40°C to + 85°C	3.16	4	4.84		
			Ta = - 40°C to + 85°C	2.3	-	7.03		When not trimming

*: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

- Built-in low-speed CR

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

(4-1) Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	20	MHz	
PLL multiplication rate	-	1	-	5	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	10	-	20	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	20	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

(4-2) Operating Conditions of Main PLL (In the case of using the built-in high-speed CR for the input clock of the main PLL)

(V_{CC} = 2.2V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	3	-	4	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	11.4	-	16.8	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	16.8	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

Note: Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency has been trimmed.

(5) Reset Input Characteristics

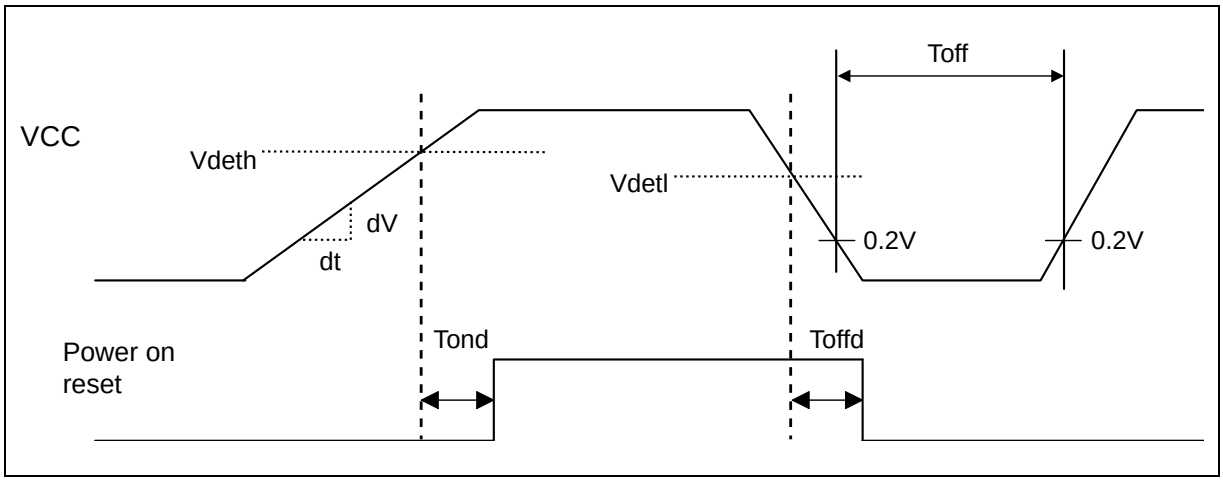
(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	
				1.5	-	ms	During RTC mode or STOP mode
				1.5	-	ms	During deep standby mode

(6) Power-on Reset Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	VCC	0.1	-	-	V/ms	
Power supply shut down time	Toff		1	-	-	ms	
Reset release voltage	Vdeth		1.44	1.60	1.76	V	When voltage rises
Reset detection voltage	Vdetl		1.39	1.55	1.71	V	When voltage drops
Reset release delay time	Tond		-	-	10	ms	dV/dt ≥ 0.1mV/µs
Reset detection delay time	Toffd		-	-	0.4	ms	dV/dt ≥ -0.04mV/µs

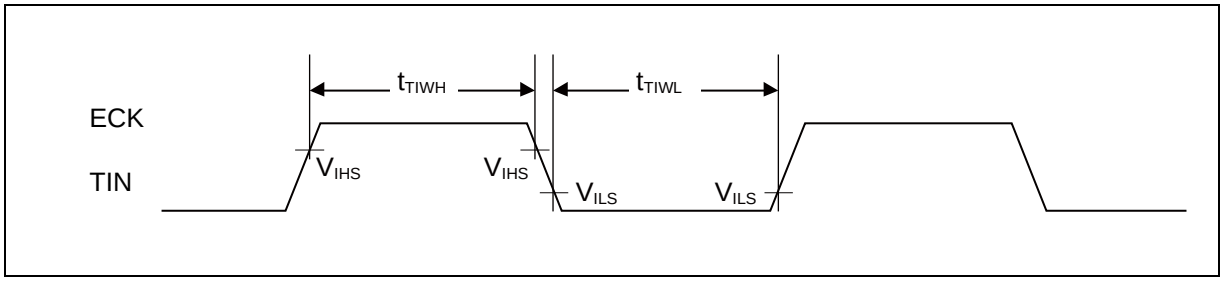


(7) Base Timer Input Timing

• Timer input timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

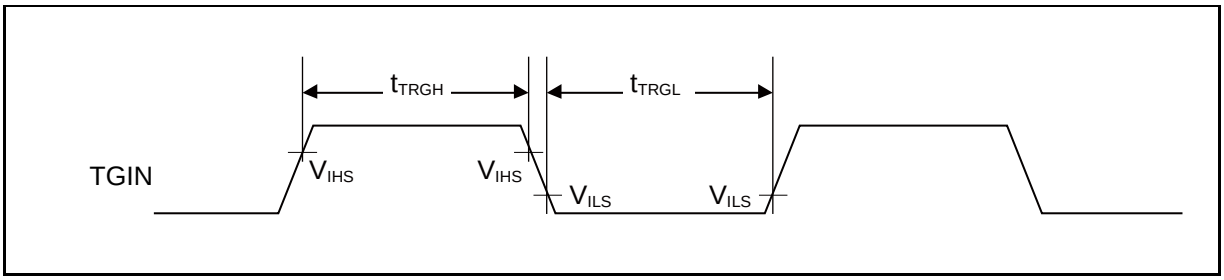
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



• Trigger input timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note: t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which the base timer is connected to, see "■BLOCK DIAGRAM" in this data sheet.

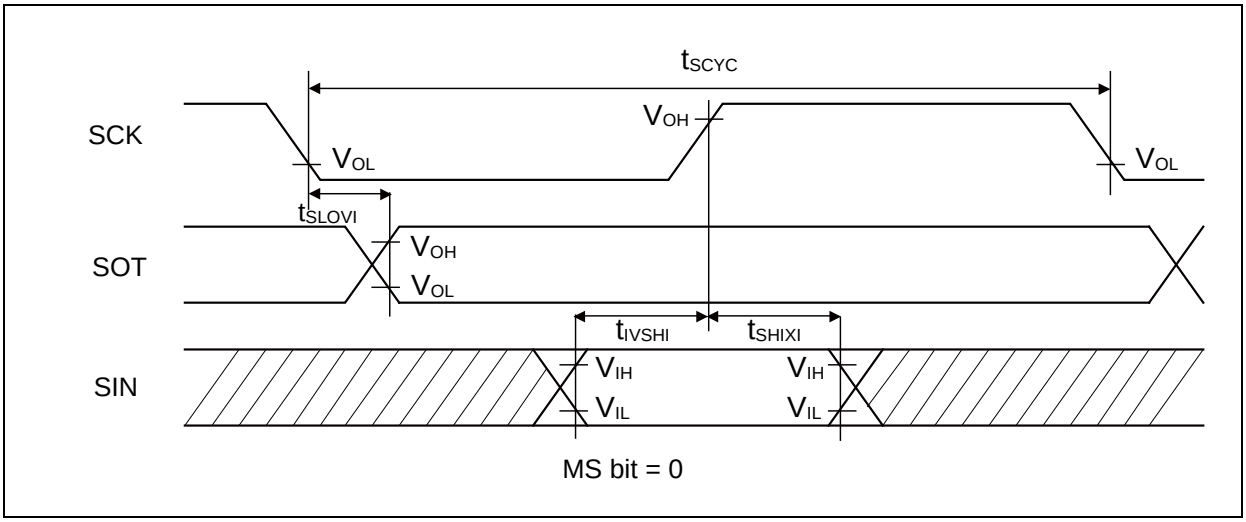
(8) UART Timing

- Synchronous serial (SPI = 0, SCINV = 0)

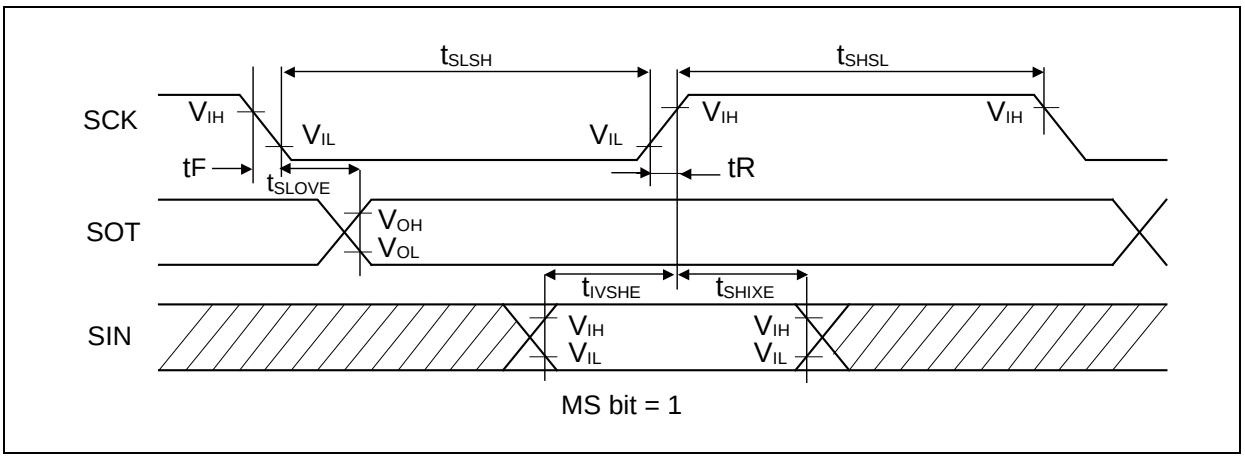
(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		2.7V ≤ V_{CC}< 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	-	5	ns

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 50pF.



MS bit = 0



MS bit = 1

• Synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

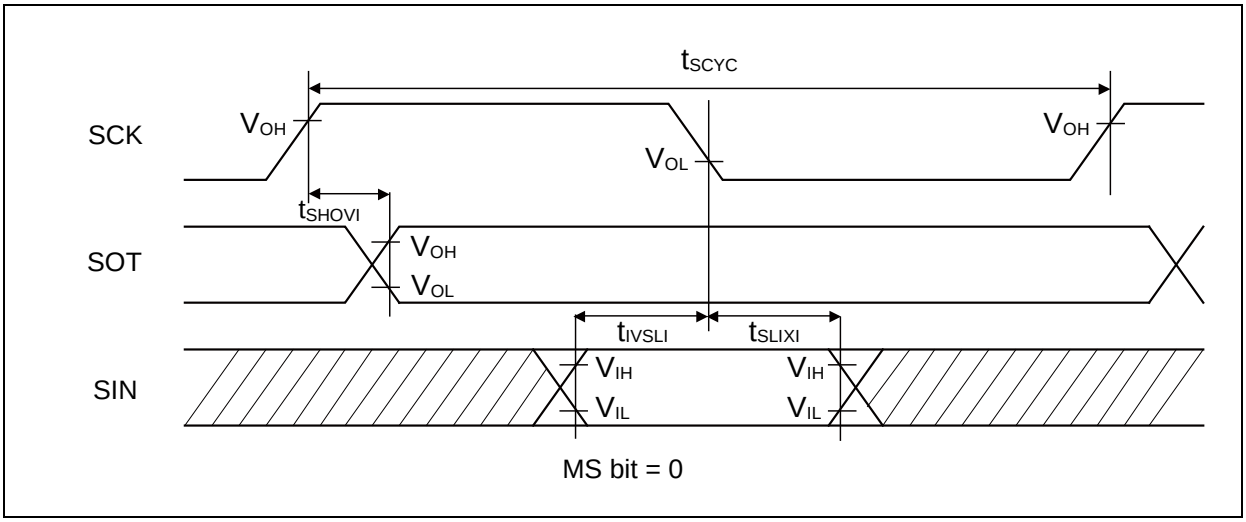
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		2.7V ≤ V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	-	5	ns

Notes: • The above characteristics apply to CLK synchronous mode.

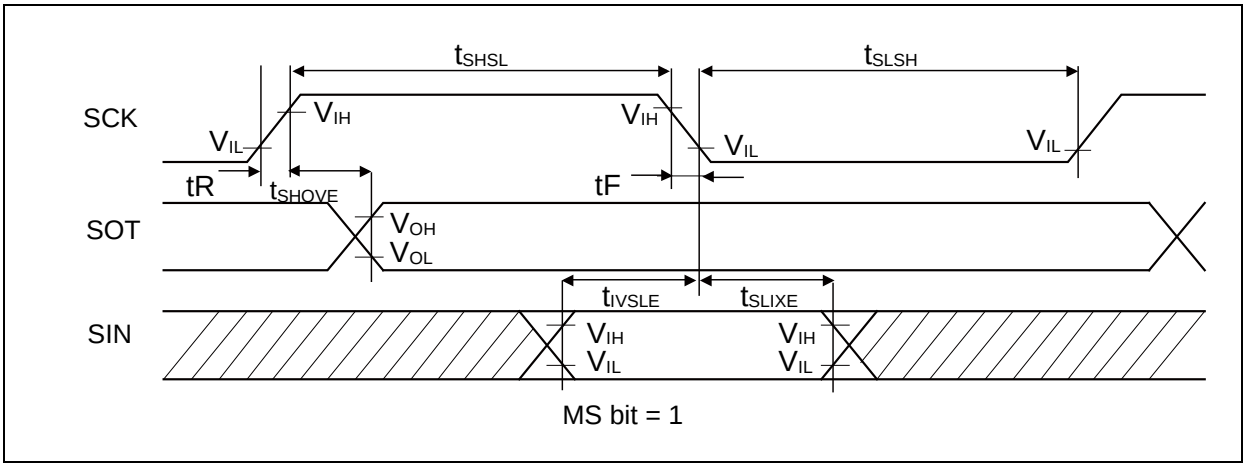
• t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.

• These characteristics only guarantee the same relocate port number.
For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.

• When the external load capacitance C_L = 50pF.



MS bit = 0



MS bit = 1

• Synchronous serial (SPI = 1, SCINV = 0)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

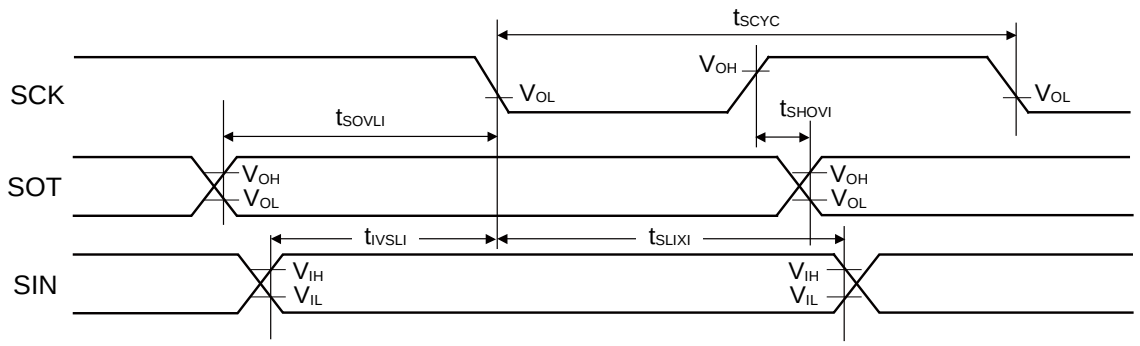
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		2.7V ≤ V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	-	5	ns

Notes: • The above characteristics apply to CLK synchronous mode.

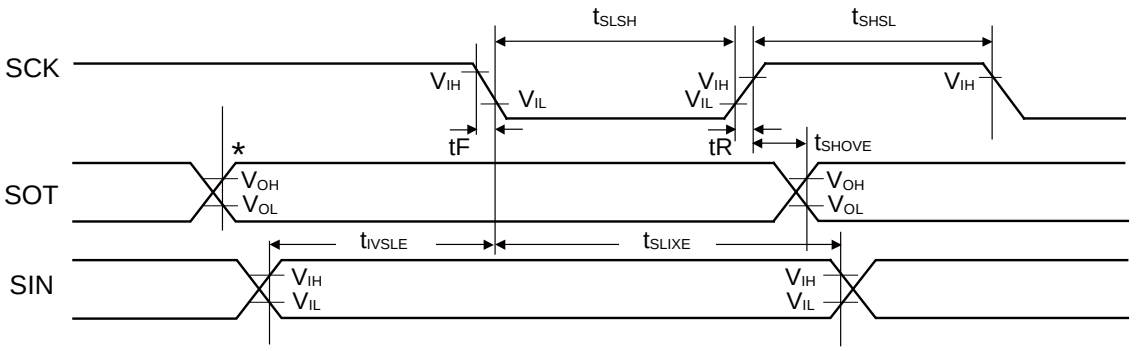
• t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.

• These characteristics only guarantee the same relocate port number.
For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.

• When the external load capacitance C_L = 50pF.



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

• Synchronous serial (SPI = 1, SCINV = 1)

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

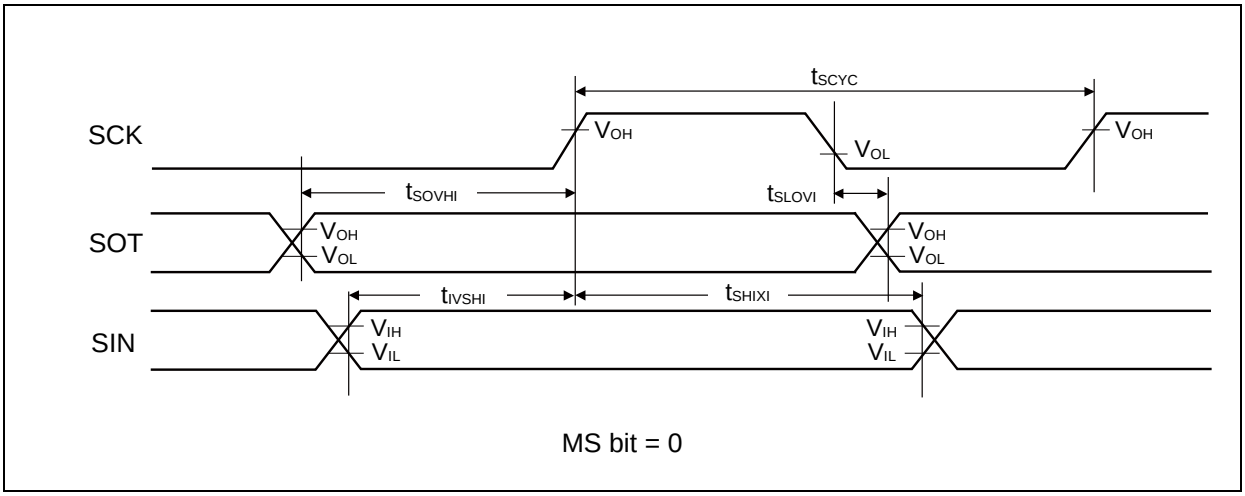
Parameter	Symbol	Pin name	Conditions	V_{CC} < 2.7V		2.7V ≤ V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	-	5	ns

Notes: • The above characteristics apply to CLK synchronous mode.

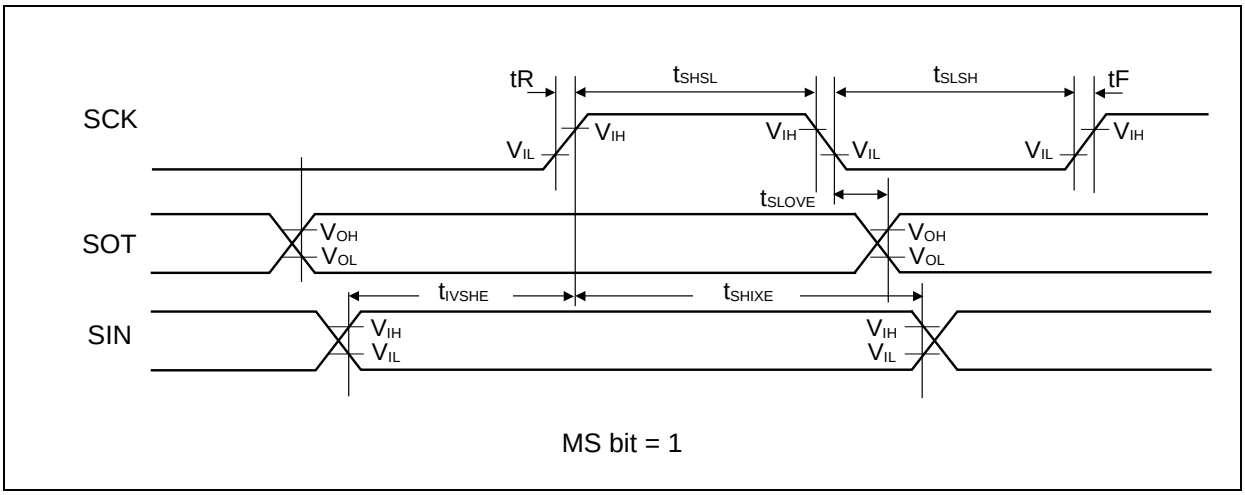
• t_{CYCP} indicates the APB bus clock cycle time.
About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.

• These characteristics only guarantee the same relocate port number.
For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.

• When the external load capacitance C_L = 50pF.



MS bit = 0

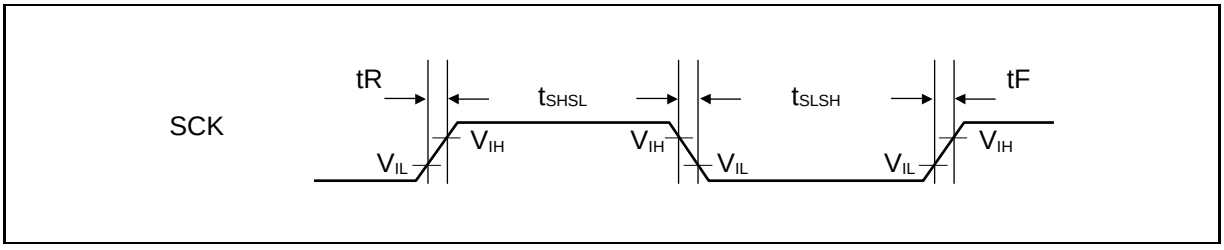


MS bit = 1

- External clock (EXT = 1) : asynchronous only

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 50pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	



(9) External Input Timing

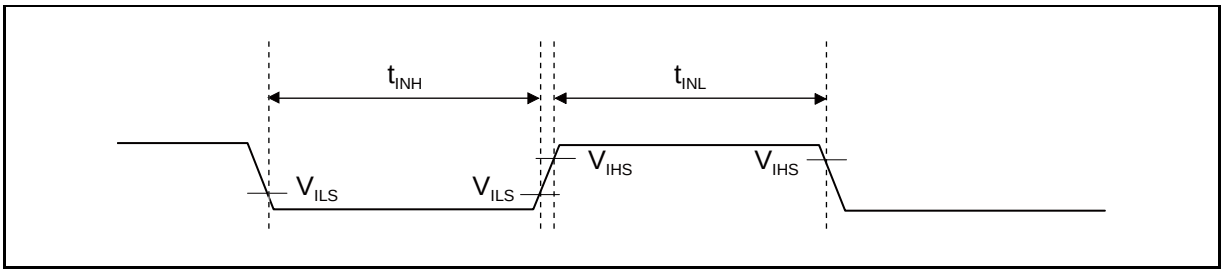
(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		IGTRG	-	$2t_{CYCP}$*1	-	ns	PPG IGBT mode
		INT00 to INT15, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

*1 : t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode, etc.
About the APB bus number which the A/D converter, Multi-function Timer, PPG, External interrupt, Deep standby mode Controller are connected to, see "■BLOCK DIAGRAM" in this data sheet.

*2 : When in stop mode, in timer mode.

*3 : When in deep standby STOP mode, in deep standby RTC mode.



(10) I^2C Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

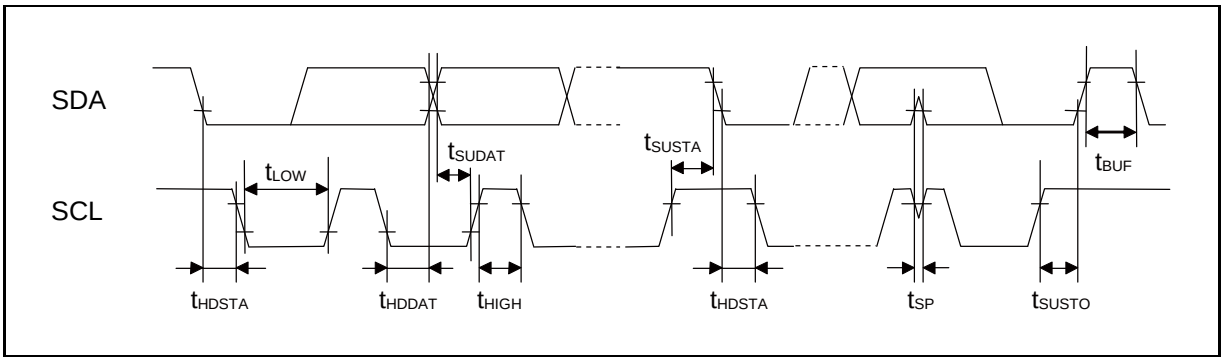
Parameter	Symbol	Conditions	Typical mode		High-speed mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 50pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1 : R and C_L represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4 : t_{CYCP} is the APB bus clock cycle time. About the APB bus number which I^2C is connected to, see "■BLOCK DIAGRAM" in this data sheet. To use I^2C, set the peripheral bus clock at 8 MHz or more.

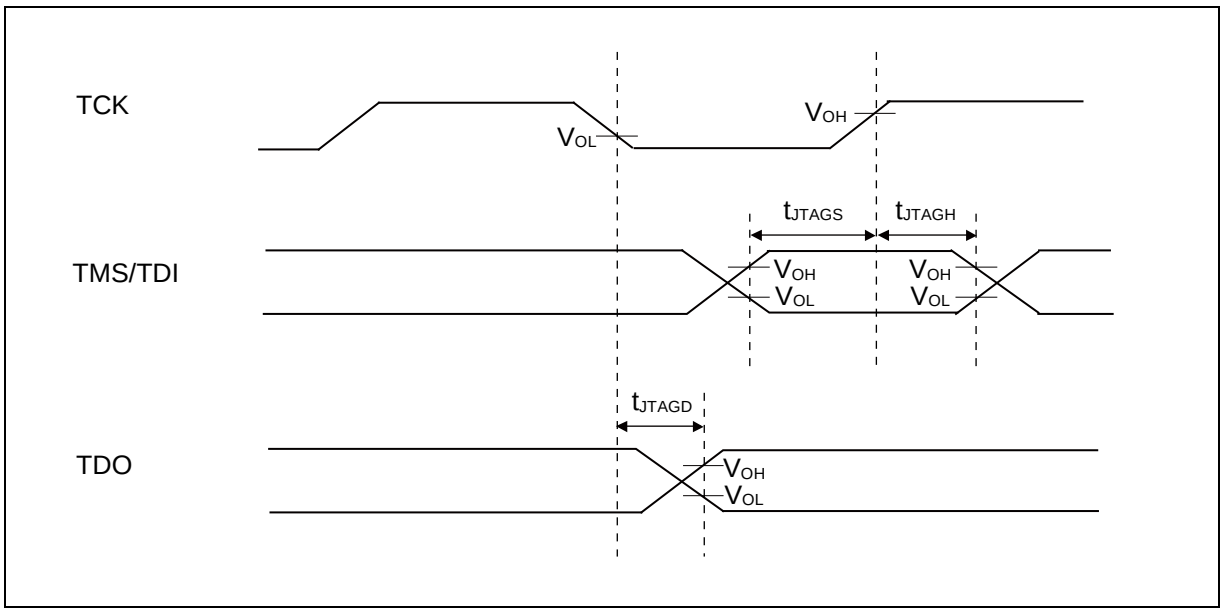


(11) JTAG Timing

(V_{CC} = 1.8V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t_{JTAGS}	TCK, TMS,TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TMS,TDI hold time	t_{JTAGH}	TCK, TMS,TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5V$	-	30	ns	
			$2.7V \leq V_{CC} < 4.5V$	-	45		
			$V_{CC} < 2.7V$	-	60		

Note: When the external load capacitance C_L = 50pF.



5. 12-bit A/D Converter

- Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

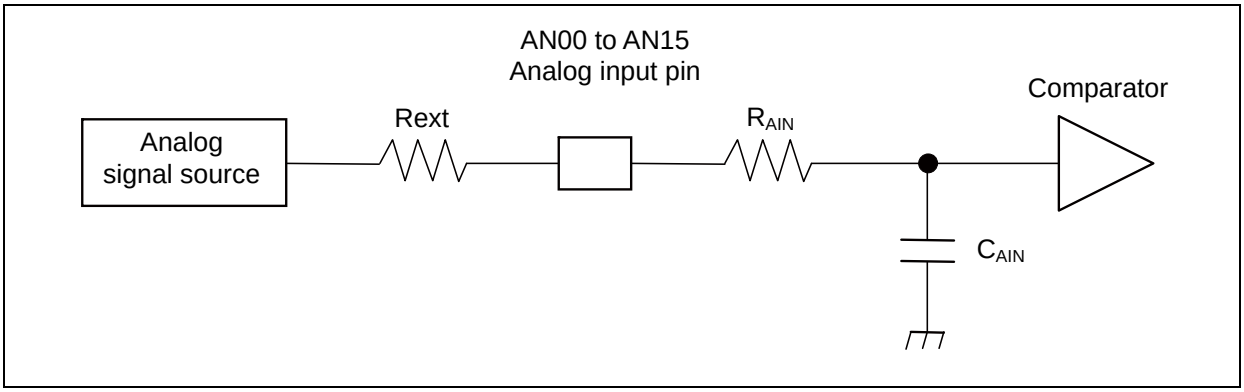
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Non linearity error	-	-	- 3.0	-	+ 3.0	LSB	$AV_{CC} \geq 2.7V$
			- 4.0	-	+ 4.0	LSB	$AV_{CC} < 2.7V$
Differential linearity error	-	-	- 1.9	-	+ 1.9	LSB	$AV_{CC} \geq 2.7V$
			- 2.9	-	+ 2.9	LSB	$AV_{CC} < 2.7V$
Zero transition voltage	V_{0T}	AN00 to AN15	- 20	-	+ 20	mV	
Full-scale transition voltage	V_{FST}	AN00 to AN15	AVRH-20	-	AVRH+20	mV	
Conversion time	-	-	1.0*1	-	-	µs	$AV_{CC} \geq 2.7V$
Sampling time	Ts	-	*2	-	10	µs	
Compare clock cycle*3	Tcck	-	50	-	1000	ns	$AV_{CC} \geq 2.7V$
			200				$AV_{CC} < 2.7V$
Period of operation enable state transitions	Tstt	-	1.0	-	-	µs	
Power supply current (analog + digital)	-	AVCC	-	1.4	2.5	mA	A/D operation
			-	0.1	0.35	µA	A/D stop
Reference power supply current (between AVRH and AVSS)	-	AVRH	-	0.5	1.5	mA	A/D operation AVRH=5.5V
			-	0.1	0.3	µA	A/D stop
Analog input capacity	C_{AIN}	-	-	-	15	pF	
Analog input resistor	R_{AIN}	-	-	-	0.9	kΩ	$AV_{CC} \geq 4.5V$
					1.6		$2.7V \leq AV_{CC} < 4.5V$
					4.0		$AV_{CC} < 2.7V$
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	AN00 to AN15	-	-	0.3	µA	
Analog input voltage	-	AN00 to AN15	AVSS	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AVCC	V	$AV_{CC} \geq 2.7V$
			AVCC				$AV_{CC} < 2.7V$

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is, the value of sampling time: 300ns, the value of compare time: 700ns ($AV_{CC} \geq 2.7V$).
Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).
For setting*4 of the sampling time and compare clock cycle, see "Chapter: A/D Converter" in " FM3 Family PERIPHERAL MANUAL Analog Macro Part ".

*2: A necessary sampling time changes by external impedance.
Ensure to set the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).

*4: The A/D Converter register is set at the peripheral clock timing.
The sampling clock and compare clock are set with the base clock (HCLK).
About the APB bus number which the A/D Converter is connected to, see "■BLOCK DIAGRAM" in this data sheet.



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

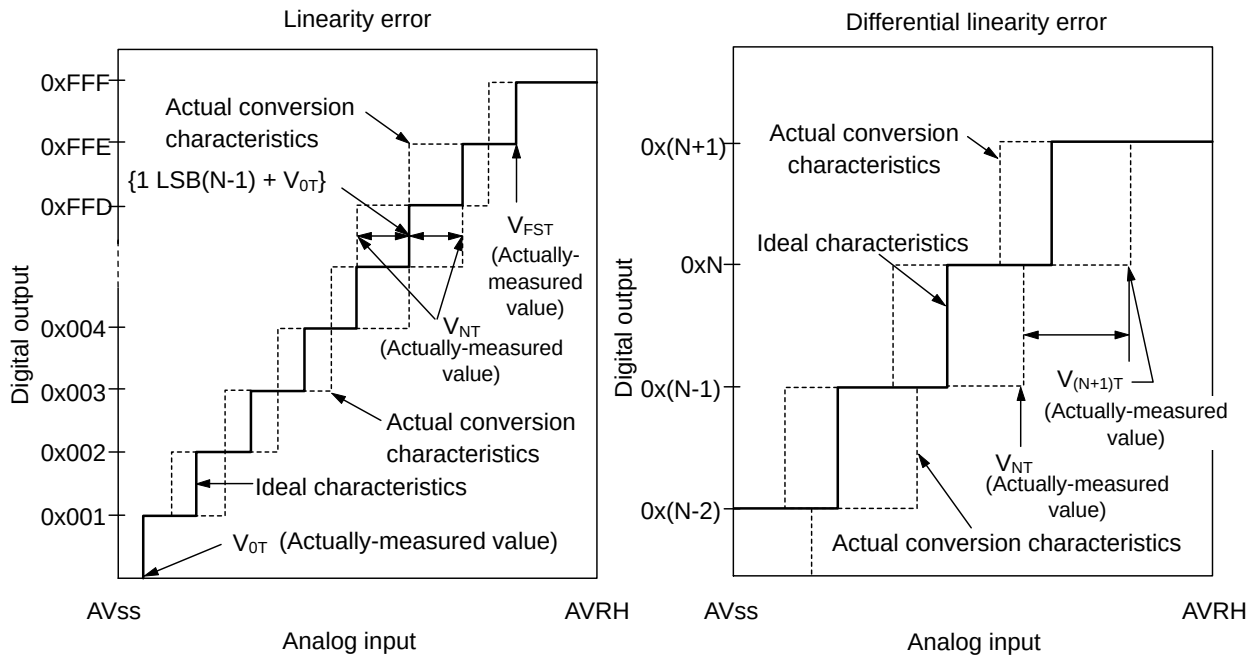
Ts : Sampling time
R_{AIN} : input resistor of A/D = 0.9kΩ at 4.5 ≤ AVCC ≤ 5.5
input resistor of A/D = 1.6kΩ at 2.7 ≤ AVCC < 4.5
input resistor of A/D = 4.0kΩ at 1.8 ≤ AVCC < 2.7
C_{AIN} : input capacity of A/D = 15pF at 1.8 ≤ AVCC ≤ 5.5
Rext : Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc : Compare time
Tcck : Compare clock cycle

- Definition of 12-bit A/D Converter Terms

  - Resolution : Analog variation that is recognized by an A/D converter.
  - Linearity error : Deviation of the line between the zero-transition point (0b000000000000←→0b000000000001) and the full-scale transition point (0b111111111110←→0b111111111111) from the actual conversion characteristics.
  - Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{0T}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{0T}}{4094}$$

N : A/D converter digital output value.
V_{0T} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

6. 10-bit D/A Converter

- Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 1.8V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	10	bit	
Conversion time	tc20		0.37	0.53	0.69	µs	Load 20pF
	tc100		1.87	2.67	3.47	µs	Load 100pF
Linearity error*1	INL		-4.0	-	+4.0	LSB	
Differential linearity error *1,*2	DNL		-0.9	-	+0.9	LSB	
Output Voltage offset	V_{OFF}		-	-	10.0	mV	Code is 0x000
			-50.0	-	+5.5	mV	Code is 0x3FF
Analog output impedance	R_O		2.45	3.50	4.55	kΩ	D/A operation
			5.0	9.0	-	MΩ	D/A stop
Output undefined period	t_R		-	-	250	ns	
Power supply current*1	IDDA*2	AVCC	190	314	440	µA	D/A 1ch. operation AV_{CC}=3.3V
			285	476	670	µA	D/A 1ch. operation AV_{CC}=5.0V
	IDSA		-	-	1.0	µA	D/A stop

*1: No-load

*2: Generates the max current by the CODE about 0x200

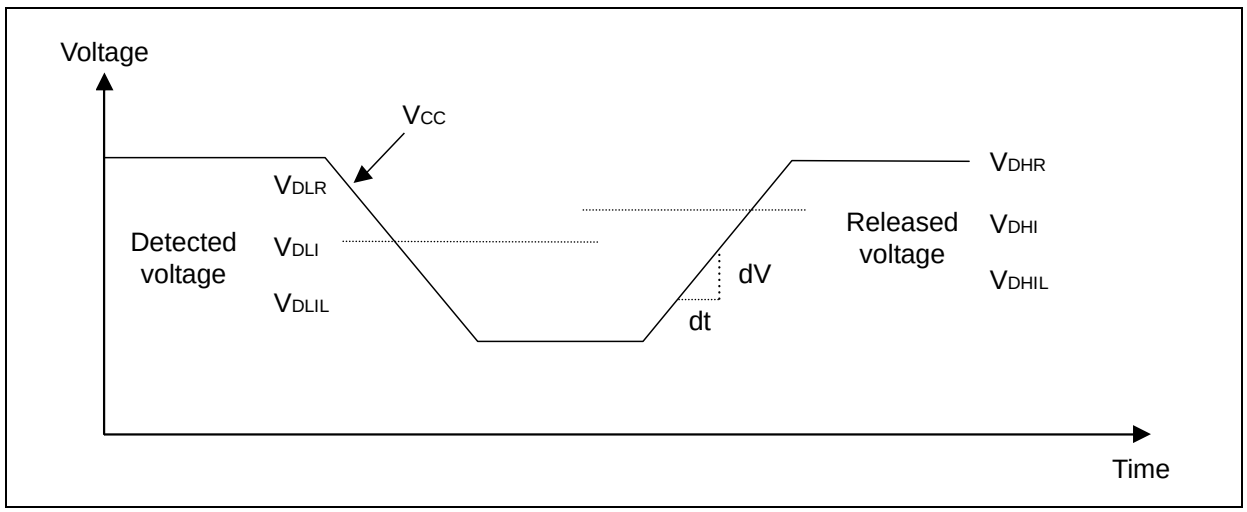
7. Low-Voltage Detection Characteristics

(1) Low-Voltage Detection Reset

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLR}	SVHR = 0001	1.43	1.53	1.63	V	When voltage drops
Released voltage	V_{DHR}		1.53	1.63	1.73	V	When voltage rises
Detected voltage	V_{DLR}	SVHR = 0100	1.80	1.93	2.06	V	When voltage drops
Released voltage	V_{DHR}		1.90	2.03	2.16	V	When voltage rises
LVD stabilization wait time	T_{LVDRW}	-	-	-	633 × t_{CYCP}*	µs	
Detection delay time	T_{LVDRD}	dV/dt ≥ -4mV/µs	-	-	60	µs	

* : t_{CYCP} indicates the APB2 bus clock cycle time.



(2) Interrupt of Low-Voltage Detection

- Normal mode

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLI}	SVHI = 0000	1.87	2.00	2.13	V	When voltage drops
Released voltage	V_{DHI}		1.97	2.10	2.23	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0001	1.96	2.10	2.24	V	When voltage drops
Released voltage	V_{DHI}		2.06	2.20	2.34	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0010	2.05	2.20	2.35	V	When voltage drops
Released voltage	V_{DHI}		2.15	2.30	2.45	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0011	2.15	2.30	2.45	V	When voltage drops
Released voltage	V_{DHI}		2.25	2.40	2.55	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0100	2.24	2.40	2.56	V	When voltage drops
Released voltage	V_{DHI}		2.34	2.50	2.66	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0101	2.33	2.50	2.67	V	When voltage drops
Released voltage	V_{DHI}		2.43	2.60	2.77	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0110	2.43	2.60	2.77	V	When voltage drops
Released voltage	V_{DHI}		2.53	2.70	2.87	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0111	2.61	2.80	2.99	V	When voltage drops
Released voltage	V_{DHI}		2.71	2.90	3.09	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1000	2.80	3.00	3.20	V	When voltage drops
Released voltage	V_{DHI}		2.90	3.10	3.30	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1001	2.99	3.20	3.41	V	When voltage drops
Released voltage	V_{DHI}		3.09	3.30	3.51	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1010	3.36	3.60	3.84	V	When voltage drops
Released voltage	V_{DHI}		3.46	3.70	3.94	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1011	3.45	3.70	3.95	V	When voltage drops
Released voltage	V_{DHI}		3.55	3.80	4.05	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1100	3.73	4.00	4.27	V	When voltage drops
Released voltage	V_{DHI}		3.83	4.10	4.37	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1101	3.83	4.10	4.37	V	When voltage drops
Released voltage	V_{DHI}		3.93	4.20	4.47	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1110	3.92	4.20	4.48	V	When voltage drops
Released voltage	V_{DHI}		4.02	4.30	4.58	V	When voltage rises
LVD stabilization wait time	T_{LVDIW}	-	-	-	633 × t_{CYCP}*	µs	
Detection delay time	T_{LVDID}	dV/dt ≥ - 4mV/µs	-	-	60	µs	

* : t_{CYCP} indicates the APB2 bus clock cycle time.

• Low power mode

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLIL}	SVHI = 0000	1.80	2.00	2.20	V	When voltage drops
Released voltage	V_{DHIL}		1.90	2.10	2.30	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0001	1.89	2.10	2.31	V	When voltage drops
Released voltage	V_{DHIL}		1.99	2.20	2.41	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0010	1.98	2.20	2.42	V	When voltage drops
Released voltage	V_{DHIL}		2.08	2.30	2.52	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0011	2.07	2.30	2.53	V	When voltage drops
Released voltage	V_{DHIL}		2.17	2.40	2.63	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0100	2.16	2.40	2.64	V	When voltage drops
Released voltage	V_{DHIL}		2.26	2.50	2.74	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0101	2.25	2.50	2.75	V	When voltage drops
Released voltage	V_{DHIL}		2.35	2.60	2.85	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0110	2.34	2.60	2.86	V	When voltage drops
Released voltage	V_{DHIL}		2.44	2.70	2.96	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0111	2.52	2.80	3.08	V	When voltage drops
Released voltage	V_{DHIL}		2.62	2.90	3.18	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1000	2.70	3.00	3.30	V	When voltage drops
Released voltage	V_{DHIL}		2.80	3.10	3.40	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1001	2.88	3.20	3.52	V	When voltage drops
Released voltage	V_{DHIL}		2.98	3.30	3.62	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1010	3.24	3.60	3.96	V	When voltage drops
Released voltage	V_{DHIL}		3.34	3.70	4.06	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1011	3.33	3.70	4.07	V	When voltage drops
Released voltage	V_{DHIL}		3.43	3.80	4.17	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1100	3.60	4.00	4.40	V	When voltage drops
Released voltage	V_{DHIL}		3.70	4.10	4.50	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1101	3.69	4.10	4.51	V	When voltage drops
Released voltage	V_{DHIL}		3.79	4.20	4.61	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1110	3.78	4.20	4.62	V	When voltage drops
Released voltage	V_{DHIL}		3.88	4.30	4.72	V	When voltage rises
LVD stabilization wait time	T_{LVDILW}	-	-	-	8039 × t_{CYCP}*	µs	
Detection/Release delay time	T_{LVDILD}	dV/dt ≥ - 0.4mV/µs	-	-	800	µs	

* : t_{CYCP} indicates the APB2 bus clock cycle time.

8. Flash Memory Write/Erase Characteristics

(V_{CC} = 2.0V to 5.5V, Ta = - 40°C to + 85°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.6	3.1	s	Excludes write time prior to internal erase
	Small Sector		0.3	1.6		
Half word (16-bit) write time		-	25	400	µs	Not including system-level overhead time.
Chip erase time		-	1.8	9.4	s	Excludes write time prior to internal erase

Write cycles and data hold time

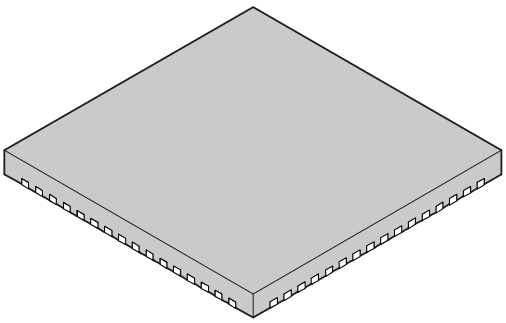
Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	
100,000	5*	

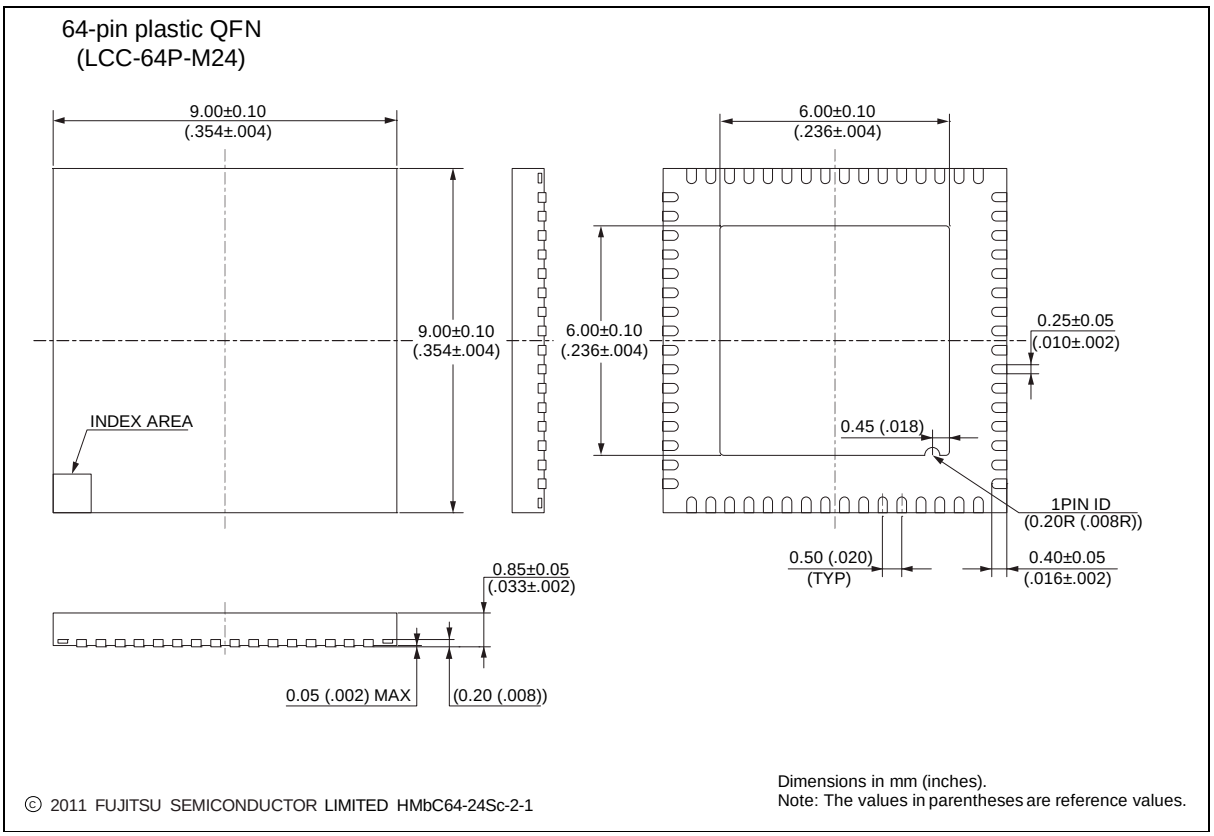
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

■ ORDERING INFORMATION

Part number	Package
MB9AF131MPMC	Plastic・LQFP(0.5mm pitch), 80-pin (FPT-80P-M37)
MB9AF132MPMC	
MB9AF131MPMC1	Plastic・LQFP(0.65mm pitch), 80-pin (FPT-80P-M40)
MB9AF132MPMC1	
MB9AF131NPMC	Plastic・LQFP(0.5mm pitch), 100-pin (FPT-100P-M23)
MB9AF132NPMC	
MB9AF131NPF	Plastic・QFP(0.65mm pitch), 100-pin (FPT-100P-M06)
MB9AF132NPF	
MB9AF131NBGL	Plastic・PFBGA(0.8mm pitch), 112-pin (BGA-112P-M04)
MB9AF132NBGL	

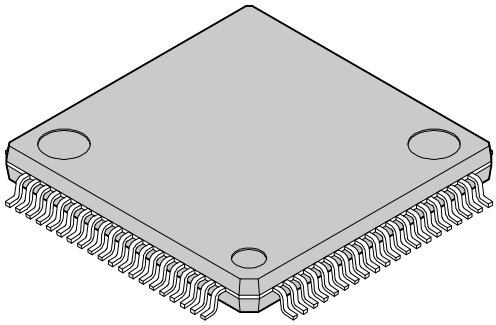
■ PACKAGE DIMENSIONS

64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	-
(LCC-64P-M24)		



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

80-pin plastic LQFP

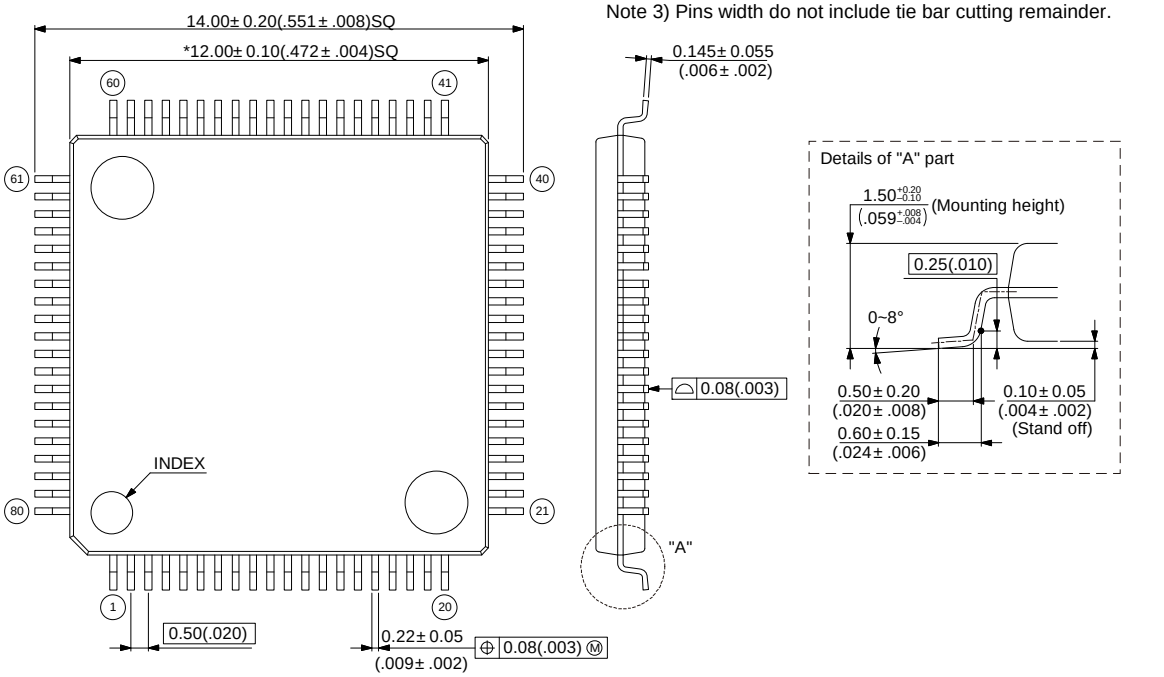


(FPT-80P-M37)

Lead pitch	0.50 mm
Package width × package length	12.00 mm × 12.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.47 g

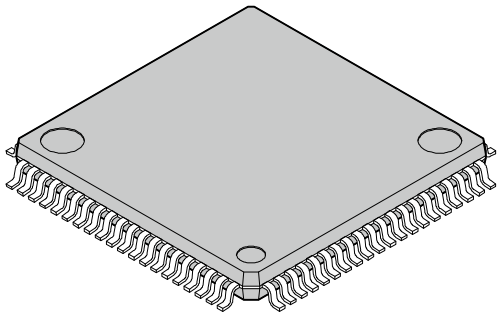
80-pin plastic LQFP
(FPT-80P-M37)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



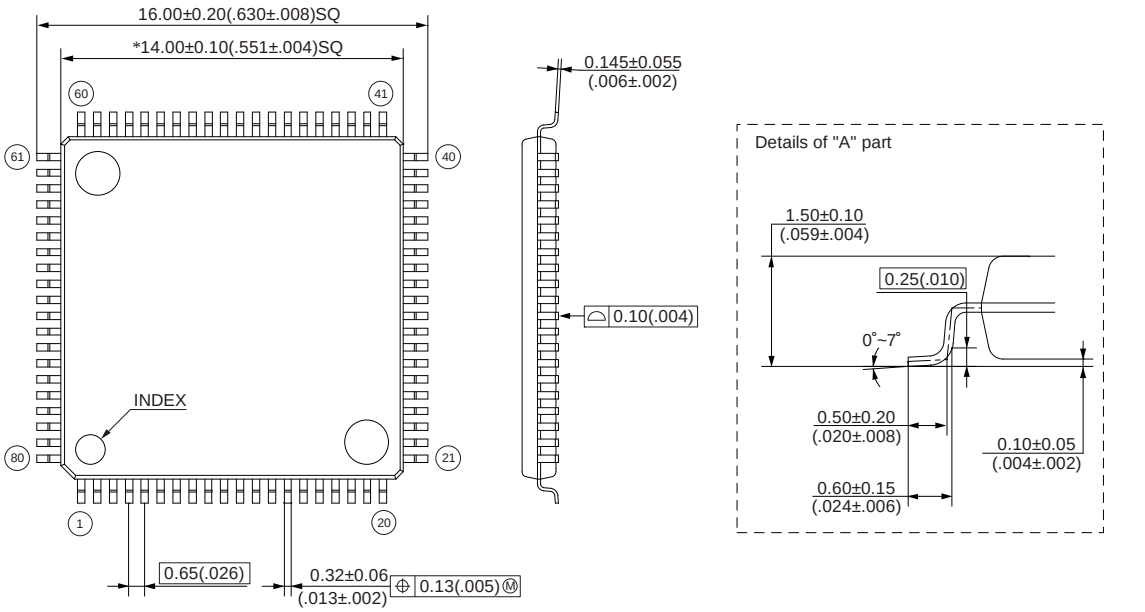
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

80-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 mm × 14.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.60 mm Max.
	Code (Reference)	P-LQFP80-14 × 14-0.65
(FPT-80P-M40)		

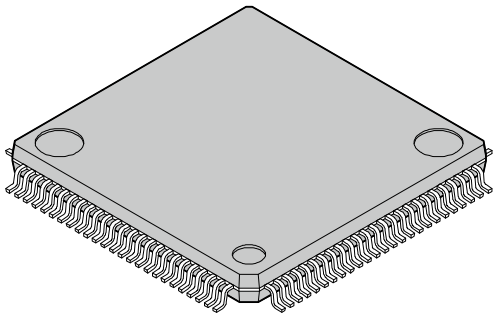
80-pin plastic LQFP
(FPT-80P-M40)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include



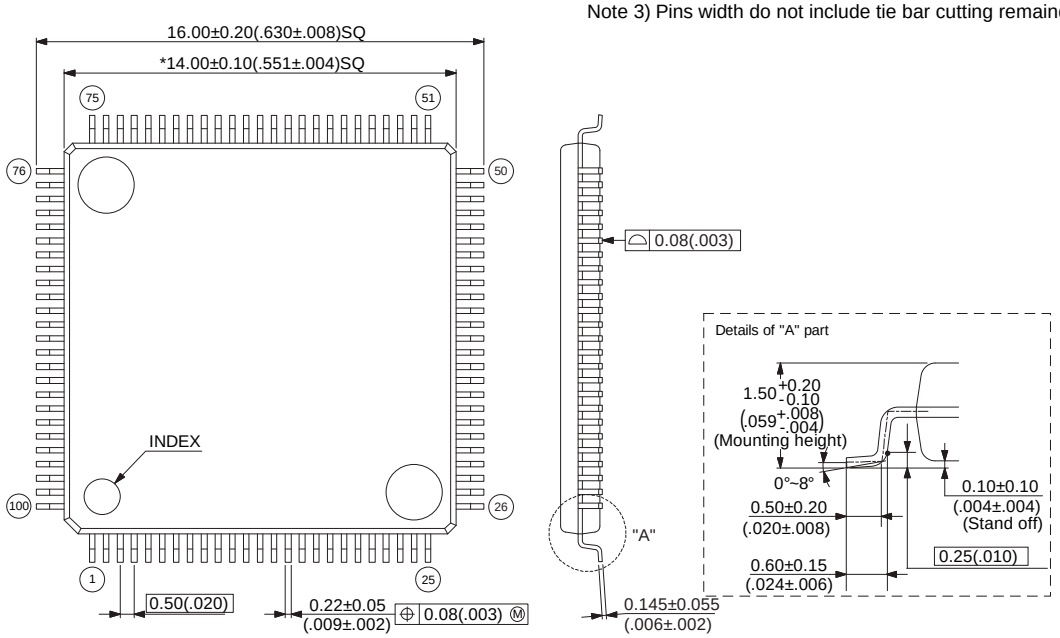
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.00 mm × 14.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
(FPT-100P-M23)	Weight	0.65 g

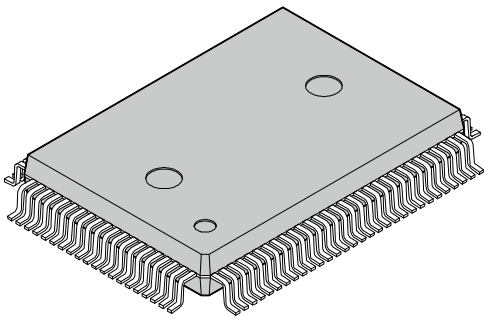
100-pin plastic LQFP
(FPT-100P-M23)

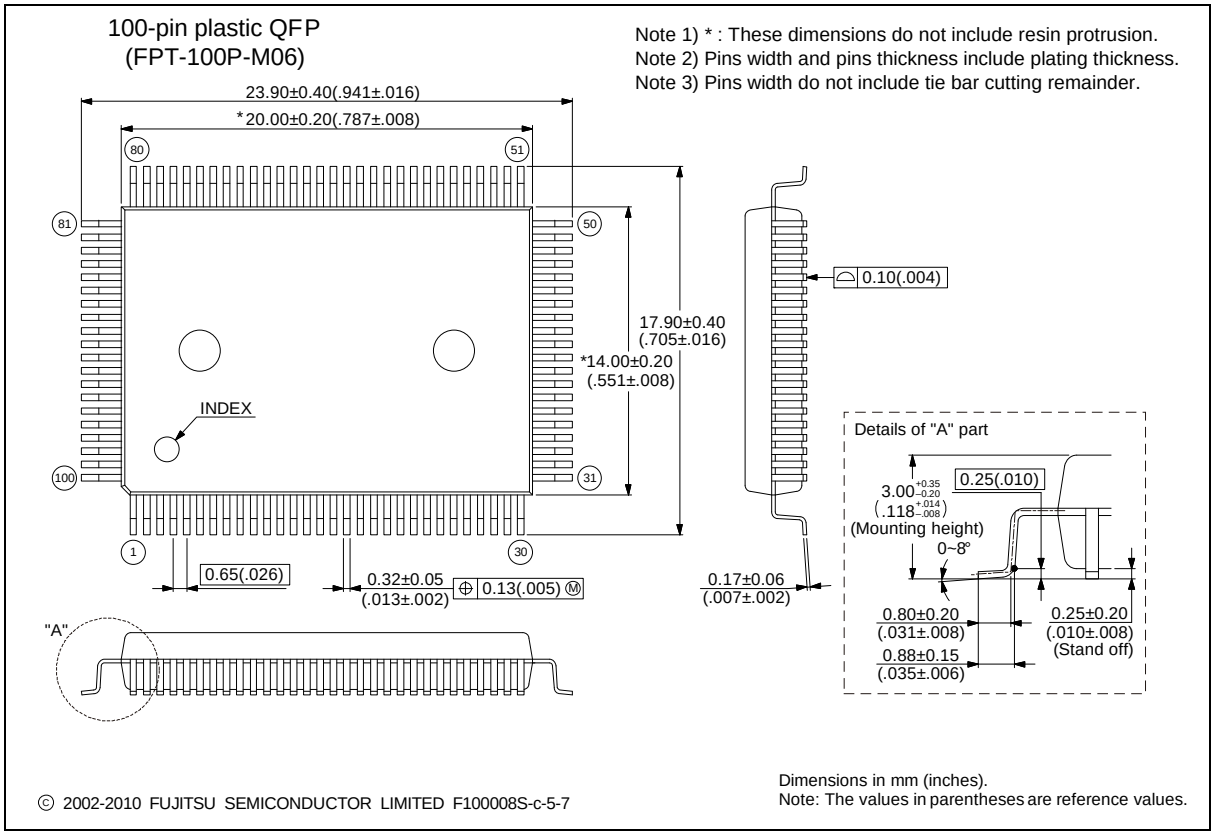
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



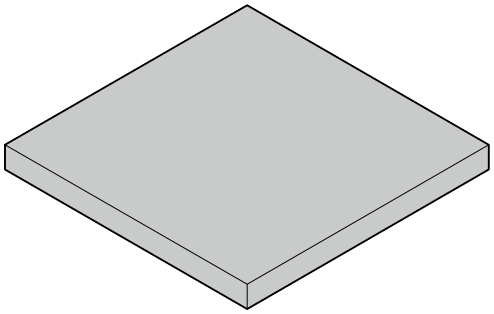
Dimensions in mm (inches).
Note:The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

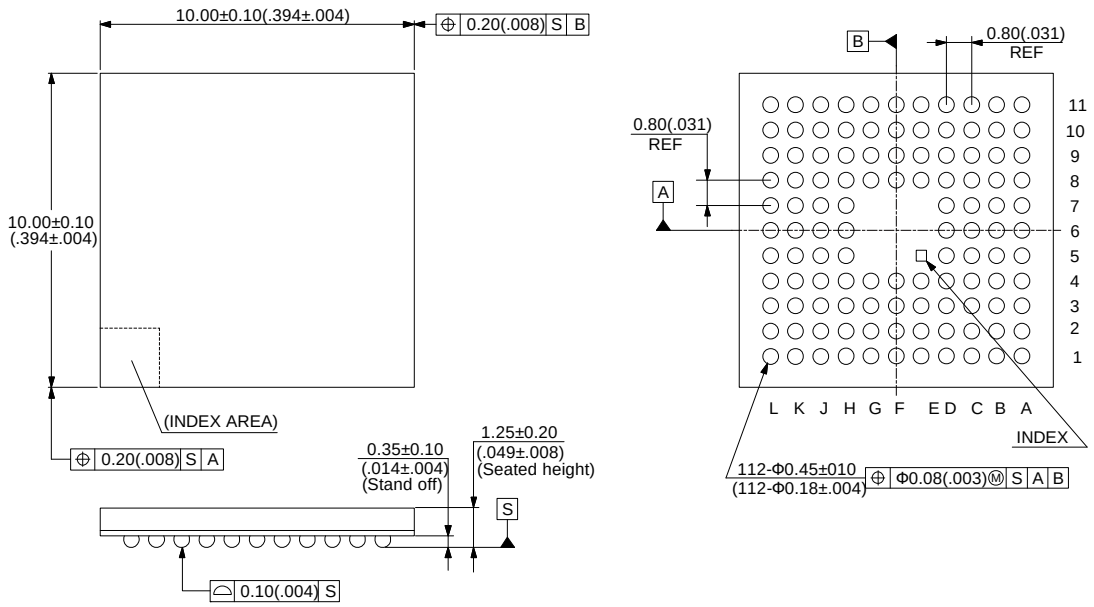
100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

112-ball plastic PFBGA		
	Ball pitch	0.80 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Φ 0.45 mm
	Mounting height	1.45 mm Max.
(BGA-112P-M04)	Weight	0.22 g

112-ball plastic PFBGA
(BGA-112P-M04)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
15	■LIST OF PIN FUNCTIONS • List of pin numbers	Revised the Pin state type.
22	• List of pin functions	Revised the pin name of "External Interrupt". INIT15_1 → INT15_1
41	■BLOCK DIAGRAM	Revised the description of "Multi-Function Serial IF".
52, 53	■PIN STATUS IN EACH CPU STATE • List of pin status	• Added "S" and "T" type to the Pin status type. • Added the footnote.

MEMO

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