

Double UART 8-bit CMOS Microcontroller, 0-60 MHz

1. Description

TEMIC TS80C51U2 is high performance CMOS ROM, OTP and EPROM versions of the 80C51 CMOS single chip 8-bit microcontroller.

The TS80C51U2 retains all features of the TEMIC 80C51 with extended ROM/EPROM capacity (16 Kbytes), 256 bytes of internal RAM, a 7-source, 4-level interrupt system, an on-chip oscillator and three timer/counters.

In addition, the TS80C51U2 has a second UART, enhanced functions on both UART, enhanced timer 2, a hardware watchdog timer, a dual data pointer, a baud rate generator and a X2 speed improvement mechanism.

The fully static design of the TS80C51U2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TS80C51U2 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

2. Features

- 80C52 Compatible
 - 8051 pin and instruction compatible
 - Four 8-bit I/O ports
 - Three 16-bit timer/counters
 - 256 bytes scratchpad RAM
- High-Speed Architecture
 - 40 MHz @ 5V, 30MHz @ 3V
 - X2 Speed Improvement capability (6 clocks/machine cycle)
30 MHz @ 5V, 20 MHz @ 3V (Equivalent to 60 MHz @ 5V, 40 MHz @ 3V)
- **second UART**
- **Baud Rate Generator**
- Dual Data Pointer
- On-chip ROM/EPROM (16K-bytes)
- Programmable Clock Out and Up/Down Timer/Counter 2
- Hardware Watchdog Timer (One-time enabled with Reset-Out)
- Asynchronous port reset
- Interrupt Structure with
 - 7 Interrupt sources
 - 4 level priority interrupt system
- Full duplex Enhanced UARTs
 - Framing error detection
 - Automatic address recognition
- Low EMI (inhibit ALE)
- Power Control modes
 - Idle mode
 - Power-down mode
 - Power-off Flag
- Once mode (On-chip Emulation)
- Power supply: 4.5-5.5V, 2.7-5.5V
- Temperature ranges: Commercial (0 to 70°C) and Industrial (-40 to 85°C)
- Packages: PDIL40, PLCC44, VQFP44 1.4, CQPJ44 (window), CDIL40 (window)

3. The second UART

In this document, UART_0 will make reference to the first UART (present in all TEMIC Semiconductors C51 derivatives) and UART_1 will make reference to the second UART, only present in the TS80C51U2 part.

The second UART (UART_1) can be seen as an alternate function of Port 1 (P1.2 or P1.6 for RXD1 and P1.3 or P1.7 for TXD1) or can be connected to (pin6 or pin12)

and (pin28 or pin34) of 44-pin package (see Pin configuration). UART_1 is fully compliant with the first one allowing an internal baud rate generator to be the clock source. This common internal baud rate generator can be used independently by each UART or both as clock source allowing to program various speeds.

The TS80C51U2 provides 7 sources of interrupt with four priority levels. UART_1 has a lower priority than Timer 2. The Serial Ports are full duplex meaning they can transmit and receive simultaneously. They are also receive buffered, meaning they can start reception of a second byte before a previously received byte has been read from the receive register. The Serial Port receive and transmit registers of UART_1 are both accessed at Special Function Register SBUF_1. Writing to SBUF_1 loads the transmit register and reading SBUF_1 accesses a physical separate receive register.

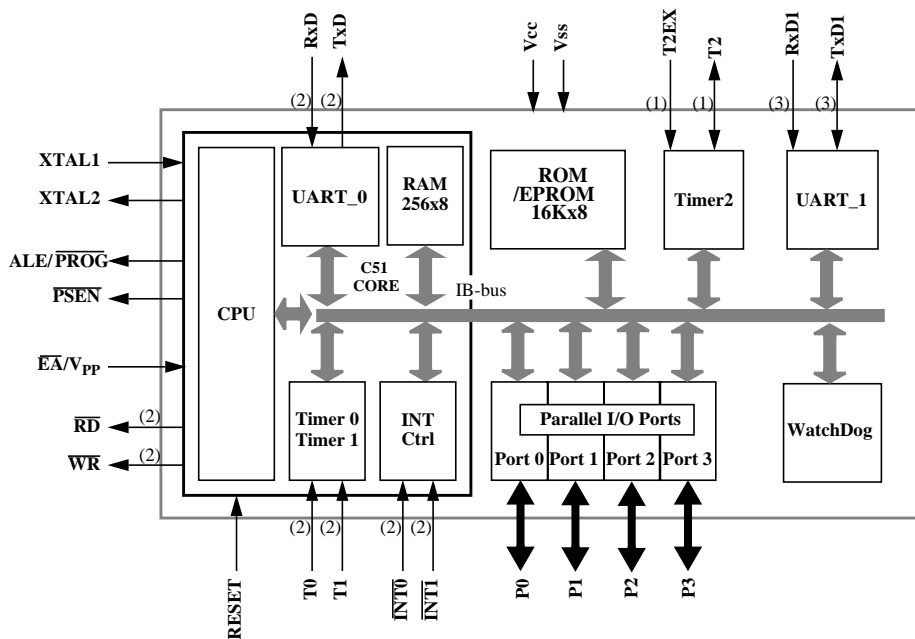
The UART_1 port control and status is the Special Function Register SCON_1. This register contains not only the mode selection bit but also the 9th bit for transmit and receive (TB8_1 and RB8_1) and the serial port interrupt bits (TI_1 and RI_1). The automatic address recognition feature is enabled when multiprocessor communication is enabled. Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the Serial Port to examine address of each incoming frame and provides filtering capability.

The UART_1 also comes with Frame error detection, similar to the UART_0.

Table 1. Memory size

PDIL40 PLCC44 VQFP44 1.4	ROM (bytes)	EPROM (bytes)
TS80C51U2	0	0
TS83C51U2	16k	0
TS87C51U2	0	16k

4. Block Diagram



- (1): Alternate function of Port 1
- (2): Alternate function of Port 3
- (3): See pin description

5. SFR Mapping

The Special Function Registers (SFRs) of the TS80C51U2 fall into the following categories:

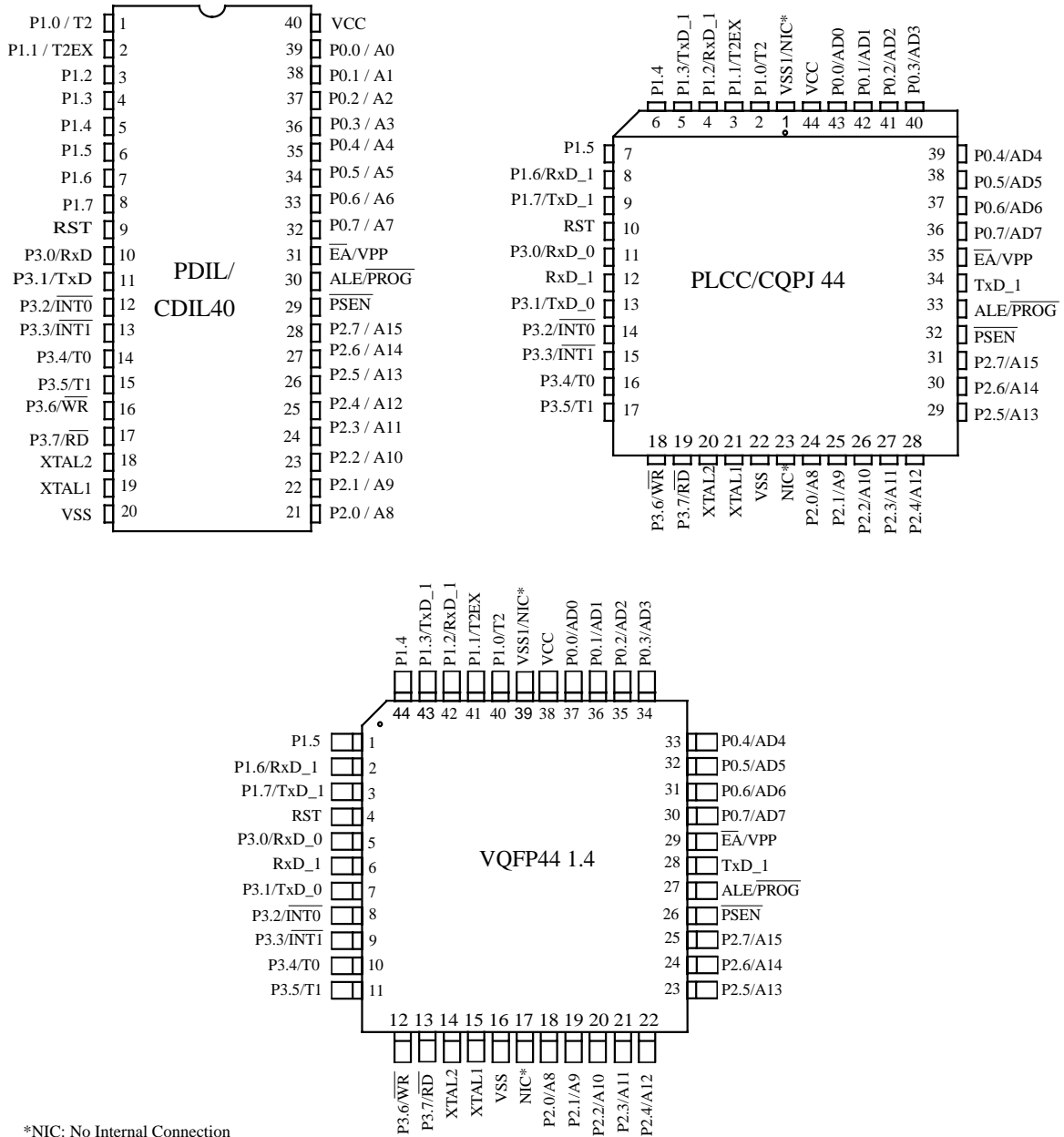
- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers for UART_0: SADDR_0, SADEN_0, SBUF_0, SCON_0
- Serial I/O port registers for UART_1: SADDR_1, SADEN_1, SBUF_1, SCON_1
- Baud Rate Generator registers: BRL, BDRCON, BDRCON_1
- Power and clock control registers: PCON
- HDW Watchdog Timer Reset: WDTRST, WDTPRG
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

Table 2. All SFRs with their address and their reset value

	Bit addressable	Non Bit addressable								
		0/8	1/9	2/A	3/B	4/C	5/D	6/E		7/F
F8h										FFh
F0h	B 0000 0000									F7h
E8h										EFh
E0h	ACC 0000 0000									E7h
D8h										DFh
D0h	PSW 0000 0000									D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000				CFh
C0h	SCON_1 0000 0000	SBUF_1 XXXX XXXX								C7h
B8h	IP X000 0000	SADEN_0 0000 0000	SADEN_1 0000 0000							BFh
B0h	P3 1111 1111								IPH X000 0000	B7h
A8h	IE 0X00 0000	SADDR_0 0000 0000	SADDR_1 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0					WDTRST XXXX XXXX	WDTPRG XXXX X000	A7h
98h	SCON_0 0000 0000	SBUF_0 XXXX XXXX	BRL 0000 0000	BDRCON 0XXX 0000	BDRCON_1 0X00 00XX					9Fh
90h	P1 1111 1111									97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR 00XX XXX0	CKCON XXXX XXX0		8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000					PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F		

reserved

6. Pin Configuration



Refer to paragraph 6.6 for accurate RxD_1 and TxD_1 pin location, depending on AUXR register configuration.

Table 3. Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIL	LCC	VQFP 1.4		
V _{SS}	20	22	16	I	Ground: 0V reference
V _{SS1}		1	39	I	Optional Ground: Contact the Sales Office for ground connection.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V _{CC} or V _{SS} in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification. Alternate functions for TSC8x54/58 Port 1 include:
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control Depending on values of (M1UA_1, M0UA_1) bits located into AUXR register, the UART_1 pins are alternate functions of P1 with two possible locations. First location: P1.2: RxD_1, serial input port for UART_1 P1.3: TxD_1, serial output port for UART_1 Second location: P1.6: RxD_1, serial input port for UART_1 P1.7: TxD_1, serial output port for UART_1 Refer to paragraph 6.6
P2.0-P2.7	21-28	24-31	18-25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.5
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	RxD_0 (P3.0): Serial input port for UART_0
	11	13	7	O	TxD_0 (P3.1): Serial output port for UART_0
	12	14	8	I	INT0 (P3.2): External interrupt 0
	13	15	9	I	INT1 (P3.3): External interrupt 1
	14	16	10	I	T0 (P3.4): Timer 0 external input
	15	17	11	I	T1 (P3.5): Timer 1 external input
	16	18	12	O	WR (P3.6): External data memory write strobe
	17	19	13	O	RD (P3.7): External data memory read strobe

Table 3. Pin Description for 40/44 pin packages

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	DIL	LCC	VQFP 1.4		
Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} . If the hardware watchdog reaches its time-out, the reset pin becomes an output during the time the internal reset is activated.
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
$\overline{\text{PSEN}}$	29	32	26	O	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{PP}$	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier
RxD_1	-	12	6	I	Serial Input for UART_1. For 44-pin package only.
TxD_1	-	34	28	O	Serial Output for UART_1. This pin is pulled up by a 100K resistor when not selected. For 44-pin package only.

7. TS80C51U2 Enhanced Features

In comparison to the original 80C52, the TS80C51U2 implements some new features, which are:

- The X2 option.
- The second full duplex enhanced UART.
- The Baud Rate generator.
- The Dual Data Pointer.
- The Watchdog.
- The 4 level interrupt priority system.
- The power-off flag.
- The ONCE mode.
- The ALE disabling.
- Some enhanced features are also located in the UARTs and the timer 2.

7.1 X2 Feature

The TS80C51U2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power.
- Save power consumption while keeping same CPU power (oscillator power saving).
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes.
- Increase CPU power by 2 while keeping same crystal frequency.

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

7.1.1 Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1+2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2. shows the mode switching waveforms.

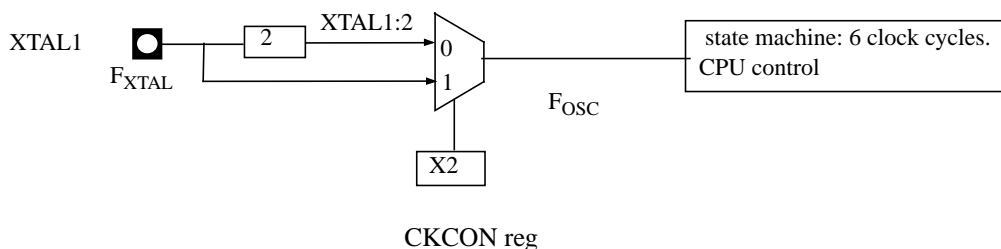


Figure 1. Clock Generation Diagram

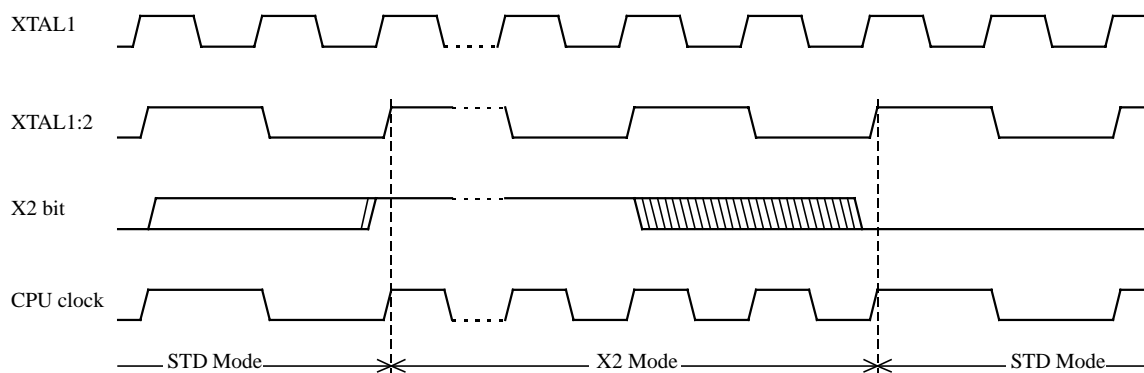


Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 4.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

CAUTION

In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UARTs, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 4. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
0	X2	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).					

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (<http://www.temic-semi.com>)

7.2 Dual Data Pointer Register Ddptr

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

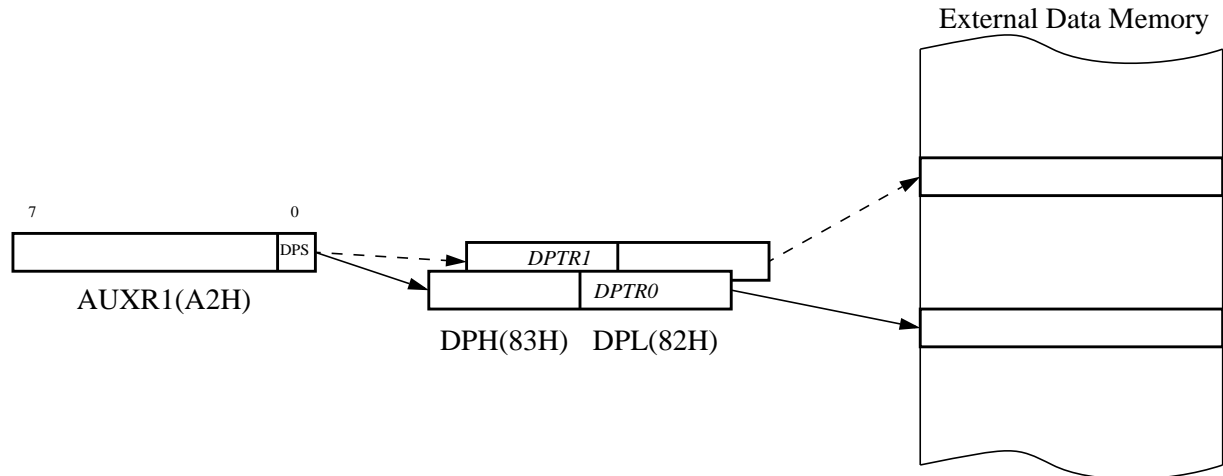


Figure 3. Use of Dual Pointer

Table 5. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	DPS
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
0	DPS	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.					

User software should not write 1s to reserved bits. These bits may be used in future 8051 family products to invoke new feature. In that case, the reset value of the new bit will be 0, and its active value will be 1. The value read from a reserved bit is indeterminate.

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2      AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE      ; address of SOURCE
0003 05A2  INC  AUXR1            ; switch data pointers
0005 90A000MOV DPTR,#DEST       ; address of DEST
0008      LOOP:
0008 05A2  INC  AUXR1            ; switch data pointers
000A E0    MOVX A,@DPTR          ; get a byte from SOURCE
000B A3    INC  DPTR             ; increment SOURCE address
000C 05A2  INC  AUXR1            ; switch data pointers
000E F0    MOVX @DPTR,A         ; write the byte to DEST
000F A3    INC  DPTR             ; increment DEST address
0010 70F6  JNZ  LOOP            ; check for 0 terminator
0012 05A2  INC  AUXR1            ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

7.3 Timer 2

The timer 2 in the TS80C51U2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 6) and T2MOD register (See Table 7). Timer 2 operation is similar to Timer 0 and Timer 1. $C/\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and $CP/\overline{RL2}$ (T2CON), as described in the TEMIC 8-bit Microcontroller Hardware description.

Refer to the TEMIC 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C51U2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

7.3.1 Auto-Reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the TEMIC 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

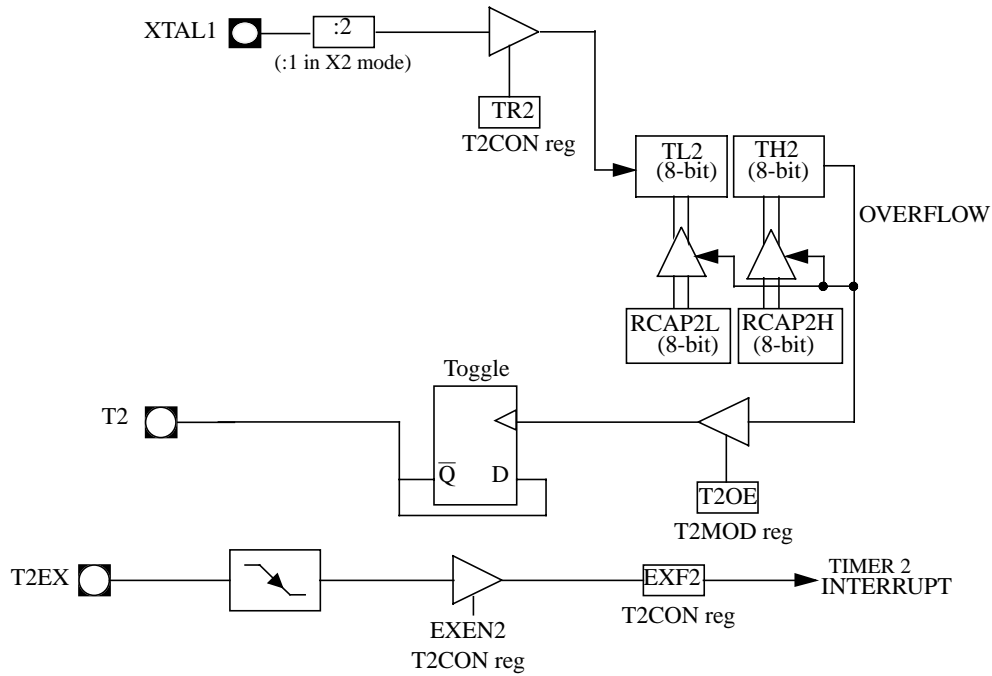


Figure 5. Clock-Out Mode $C/\overline{T2} = 0$

Table 6. T2CON Register

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
Bit Number	Bit Mnemonic	Description					
7	TF2	Timer 2 overflow Flag Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.					
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK_0	Receive Clock bit for UART_0 Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK_0	Transmit Clock bit for UART_0 Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{Osc}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.					

Reset Value = 0000 0000b

Bit addressable

Table 7. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
1	T2OE	Timer 2 Output Enable bit Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.					
0	DCEN	Down Counter Enable bit Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.					

Reset Value = XXXX XX00b

Not bit addressable

7.4 TS80C51U2 Serial I/O Ports enhancements

The serial I/O ports in the TS80C51U2 are compatible with the serial I/O port in the 80C52.

They provide both synchronous and asynchronous communication modes. They operate as Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

Serial I/O ports include the following enhancements:

- Framing error detection
- Automatic address recognition

As these improvements apply to both UART, most of the time in the following lines, there won't be any reference to UART_0 or UART_1, but only to UART, generally speaking. Idem for the bits in registers.

7.4.1 Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

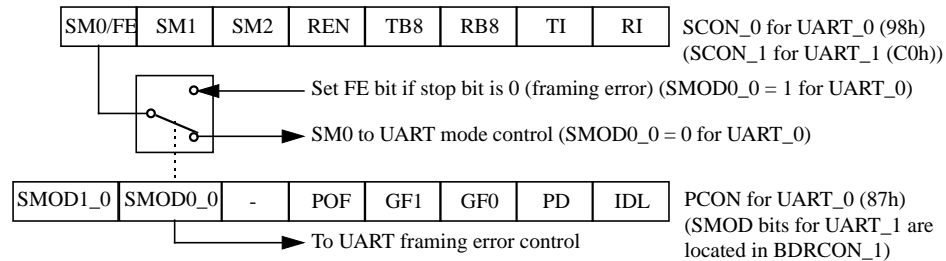


Figure 6. Framing Error Block Diagram

When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 8.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

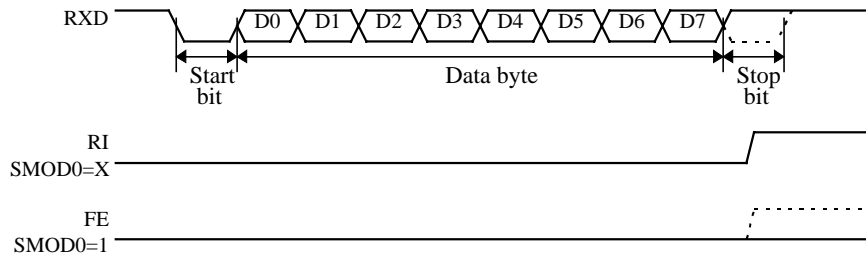


Figure 7. UART Timings in Mode 1

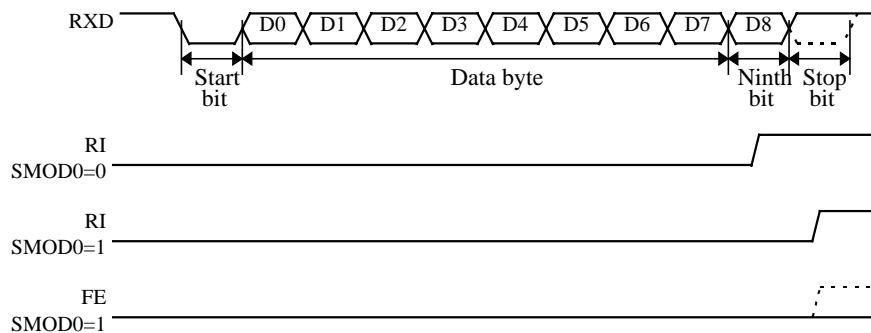


Figure 8. UART Timings in Modes 2 and 3

7.4.2 Automatic Address Recognition

The automatic address recognition feature is enabled for each UART when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

NOTE: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

7.4.3 Given Address

Each UART has an individual address that is specified in SADDR_0 or SADDR_1 register; the SADEN_0 or SADEN_1 register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example

illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be 1111 1111b.

For example:

SADDR	0101 0110b
<u>SADEN</u>	<u>1111 1100b</u>
Given	0101 01XXb

The following is an example of how to use given addresses to address different slaves:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Given	1111 0X0Xb

Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Given	1111 0XX1b

Slave C:	SADDR	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Given	1111 00X1b

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g. 1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

7.4.4 Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

	SADDR	0101 0110b
	<u>SADEN</u>	<u>1111 1100b</u>
Broadcast =SADDR OR SADEN		1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:	SADDR	1111 0001b
	<u>SADEN</u>	<u>1111 1010b</u>
	Broadcast	1111 1X11b,

Slave B:	SADDR	1111 0011b
	<u>SADEN</u>	<u>1111 1001b</u>
	Broadcast	1111 1X11B,

Slave C:	SADDR=	1111 0010b
	<u>SADEN</u>	<u>1111 1101b</u>
	Broadcast	1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

7.4.5 Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

7.4.6 Baud Rate Selection for UART0_0 for mode 1 and 3

The Baud Rate Generator for transmit and receive clocks can be selected separately via the T2CON and BDRCON registers.

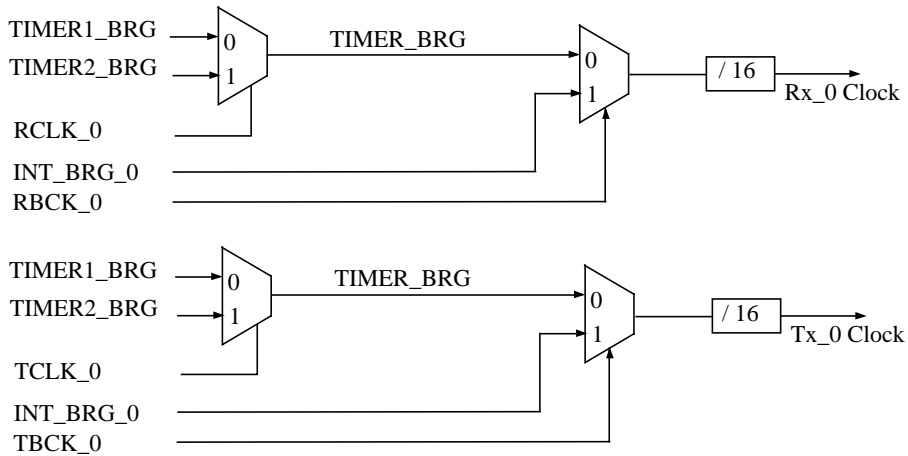


Figure 9. Baud Rate selection

7.4.7 Baud Rate Selection for UART1_1 for mode 1 and 3

The Baud Rate Generator for transmit and receive clocks can be selected separately via the BDRCON_1 register.

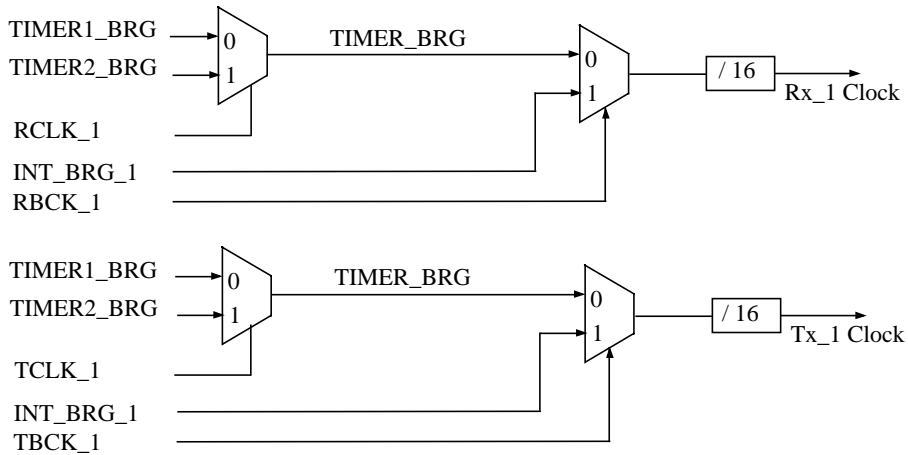


Figure 10. Baud Rate selection

7.4.8 Baud Rate selection table for UART_0

TCLK_0	RCLK_0	TBCK_0	RBCK_0	Clock Source for UART_0 Tx	Clock Source UART_0 Rx
0	0	0	0	Timer 1	Timer 1
1	0	0	0	Timer 2	Timer 1
0	1	0	0	Timer 1	Timer 2
1	1	0	0	Timer 2	Timer 2
X	0	1	0	INT_BRG_0	Timer 1
X	1	1	0	INT_BRG_0	Timer 2
0	X	0	1	Timer 1	INT_BRG_0
1	X	0	1	Timer 2	INT_BRG_0
X	X	1	1	INT_BRG_0	INT_BRG_0

7.4.9 Baud Rate selection table for UART_1

TCLK_1	RCLK_1	TBCK_1	RBCK_1	Clock Source for UART_1 Tx	Clock Source UART_1 Rx
0	0	0	0	Timer 1	Timer 1
1	0	0	0	Timer 2	Timer 1
0	1	0	0	Timer 1	Timer 2
1	1	0	0	Timer 2	Timer 2
X	0	1	0	INT_BRG_1	Timer 1
X	1	1	0	INT_BRG_1	Timer 2
0	X	0	1	Timer 1	INT_BRG_1
1	X	0	1	Timer 2	INT_BRG_1
X	X	1	1	INT_BRG_1	INT_BRG_1

7.4.10 Internal Baud Rate Generator (BRG)

When the internal Baud Rate Generator is used, the Baud Rates are determined by the BRG overflow depending on the BRL reload value, the X2 bit in CKON register, the value of SPD bit (Speed Mode) in BDRCON register and the value of the SMOD1_0 bit in PCON register (for UART_0) or SMOD1_1 in BDRCON_1 register (for UART_1). The Internal Baud Rate Generator is common to both UARTs:

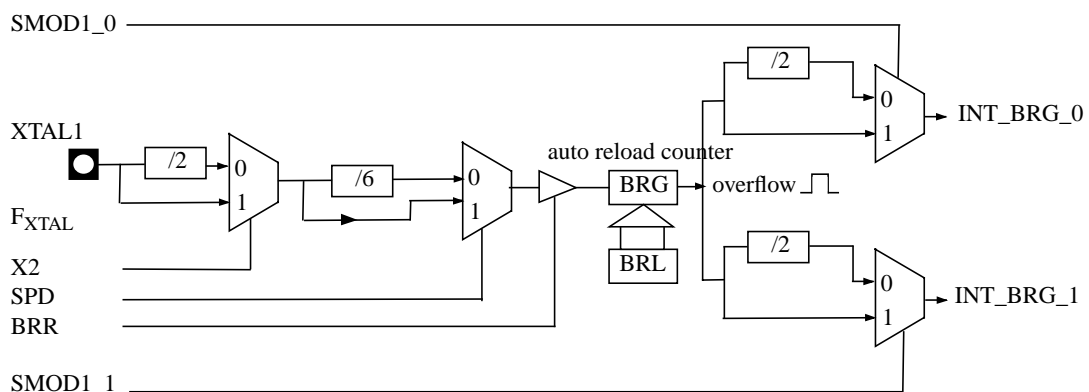


Figure 11. Internal Baud Rate

- for UART_1

$$\text{Baud_Rate} = \frac{2^{\text{SMOD1}_1} \times 2^{\text{X2}} \times \text{F}_{\text{XTAL}}}{2 \times 2 \times 6^{(1-\text{SPD})} \times 16 \times [256 - (\text{BRL})]}$$

$$(\text{BRL}) = 256 - \frac{2^{\text{SMOD1}_1} \times 2^{\text{X2}} \times \text{F}_{\text{XTAL}}}{2 \times 2 \times 6^{(1-\text{SPD})} \times 16 \times \text{Baud_Rate}}$$

- for UART_0

$$\text{Baud_Rate} = \frac{2^{\text{SMOD1}_0} \times 2^{\text{X2}} \times \text{F}_{\text{XTAL}}}{2 \times 2 \times 6^{(1-\text{SPD})} \times 16 \times [256 - (\text{BRL})]}$$

$$(\text{BRL}) = 256 - \frac{2^{\text{SMOD1}_0} \times 2^{\text{X2}} \times \text{F}_{\text{XTAL}}}{2 \times 2 \times 6^{(1-\text{SPD})} \times 16 \times \text{Baud_Rate}}$$

Example of computed value when X2=1, SMOD1=1, SPD=1

Baud Rates	F _{XTAL} = 16.384 MHz		F _{XTAL} = 24MHz	
	BRL	Error (%)	BRL	Error (%)
115200	247	1.23	243	0.16
57600	238	1.23	230	0.16
38400	229	1.23	217	0.16
28800	220	1.23	204	0.16
19200	203	0.63	178	0.16
9600	149	0.31	100	0.16
4800	43	1.23	-	-

Example of computed value when X2=0, SMOD1=0, SPD=0

Baud Rates	F _{OSC} = 16.384 MHz		F _{OSC} = 24MHz	
	BRL	Error (%)	BRL	Error (%)
4800	247	1.23	243	0.16
2400	238	1.23	230	0.16
1200	220	1.23	202	3.55
600	185	0.16	152	0.16

The baud rate generator can be used for mode 1 or 3 (refer to figures 9 and 10), but also for mode 0 for both UARTs, thanks to the bit SRC located in BDRCON register (Table 12)

7.5 UARTs registers

SADEN_0 - Slave Address Mask Register for UART_0 (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

SADEN_1 - Slave Address Mask Register for UART_1 (BAh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

SADDR_0 - Slave Address Register for UART_0 (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

SADDR_1 - Slave Address Register for UART_1 (AAh)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

SBUF_0 - Serial Buffer Register for UART_0 (99h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb

SBUF_1 - Serial Buffer Register for UART_1 (C1h)

7	6	5	4	3	2	1	0

Reset Value = XXXX XXXXb

BRL - Baud Rate Reload Register for the internal baud rate generator, UART_0 and UART_1 (9Ah)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Table 8. SCON Register

SCON_0 - Serial Control Register for UART_0 (98h)

7	6	5	4	3	2	1	0
FE_0/ SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0

Bit Number	Bit Mnemonic	Description																									
7	FE_0	Framing Error bit (SMOD0_0=1) for UART_0 Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0_0 must be set to enable access to the FE bit																									
	SM0_0	Serial port Mode bit 0 (SMOD0_0=0) for UART_0 Refer to SM1 for serial port mode selection. SMOD0_0 must be cleared to enable access to the SM0_0 bit																									
6	SM1_0	Serial port Mode bit 1 for UART_0 <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;"><u>SM1_0</u></th> <th style="width: 10%;"><u>SM0_0</u></th> <th style="width: 10%;"><u>Mode</u></th> <th style="width: 20%;"><u>Description</u></th> <th style="width: 40%;"><u>Baud Rate</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Shift Register</td> <td>$F_{XTAL}/12$ ($F_{XTAL}/6$ X2 mode)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8-bit UART</td> <td>Variable</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> <td>9-bit UART</td> <td>$F_{XTAL}/64$ or $F_{XTAL}/32$ ($F_{XTAL}/32$ or $F_{XTAL}/16$ X2 mode)</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> <td>9-bit UART</td> <td>Variable</td> </tr> </tbody> </table>	<u>SM1_0</u>	<u>SM0_0</u>	<u>Mode</u>	<u>Description</u>	<u>Baud Rate</u>	0	0	0	Shift Register	$F_{XTAL}/12$ ($F_{XTAL}/6$ X2 mode)	0	1	1	8-bit UART	Variable	1	0	2	9-bit UART	$F_{XTAL}/64$ or $F_{XTAL}/32$ ($F_{XTAL}/32$ or $F_{XTAL}/16$ X2 mode)	1	1	3	9-bit UART	Variable
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1	1	3	9-bit UART	Variable																							
5	SM2_0	Serial port Mode 2 bit / Multiprocessor Communication Enable bit for UART_0 Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																									
4	REN_0	Reception Enable bit for UART_0 Clear to disable serial reception. Set to enable serial reception.																									
3	TB8_0	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3 for UART_0. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																									
2	RB8_0	Receiver Bit 8 / Ninth bit received in modes 2 and 3 for UART_0 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																									
1	TI_0	Transmit Interrupt flag for UART_0 Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																									
0	RI_0	Receive Interrupt flag for UART_0 Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 7. and Figure 8. in the other modes.																									

Reset Value = 0000 0000b

Bit addressable

Table 9. SCON Register

SCON_1 - Serial Control Register for UART_1 (C0h)

7	6	5	4	3	2	1	0																									
FE_1/ SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1																									
Bit Number	Bit Mnemonic	Description																														
7	FE_1	Framing Error bit (SMOD0_1=1) for UART_1 Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0_1 must be set to enable access to the FE bit																														
	SM0_1	Serial port Mode bit 0 (SMOD0_1=0) for UART_1 Refer to SM1 for serial port mode selection. SMOD0_1 must be cleared to enable access to the SM0_1 bit																														
6	SM1_1	Serial port Mode bit 1 for UART_1 <table border="1"> <thead> <tr> <th>SM1_1</th> <th>SM0_1</th> <th>Mode</th> <th>Description</th> <th>Baud Rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Shift Register</td> <td>$F_{XTAL}/12$ ($F_{XTAL}/6$ X2 mode)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>8-bit UART</td> <td>Variable</td> </tr> <tr> <td>1</td> <td>0</td> <td>2</td> <td>9-bit UART</td> <td>$F_{XTAL}/64$ or $F_{XTAL}/32$ ($F_{XTAL}/32$ or $F_{XTAL}/16$ X2 mode)</td> </tr> <tr> <td>1</td> <td>1</td> <td>3</td> <td>9-bit UART</td> <td>Variable</td> </tr> </tbody> </table>						SM1_1	SM0_1	Mode	Description	Baud Rate	0	0	0	Shift Register	$F_{XTAL}/12$ ($F_{XTAL}/6$ X2 mode)	0	1	1	8-bit UART	Variable	1	0	2	9-bit UART	$F_{XTAL}/64$ or $F_{XTAL}/32$ ($F_{XTAL}/32$ or $F_{XTAL}/16$ X2 mode)	1	1	3	9-bit UART	Variable
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4	REN_1	Reception Enable bit for UART_1 Clear to disable serial reception. Set to enable serial reception.																														
3	TB8_1	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3 for UART_1. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																														
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1	TI_1	Transmit Interrupt flag for UART_1 Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																														
0	RI_1	Receive Interrupt flag for UART_1 Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 7. and Figure 8. in the other modes.																														

Reset Value = 0000 0000b

Bit addressable

Table 10. T2CON Register

T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
Bit Number	Bit Mnemonic	Description					
7	TF2	Timer 2 overflow Flag Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.					
6	EXF2	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK_0	Receive Clock bit for UART_0 Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK_0	Transmit Clock bit for UART_0 Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to auto-reload on timer 2 overflow. Clear to auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.					

Reset Value = 0000 0000b

Bit addressable

Table 11. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1_0	SMOD0_0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1_0	Serial port Mode bit 1 for UART_0 Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0_0	Serial port Mode bit 0 for UART_0 Clear to select SM0_0 bit in SCON_0 register. Set to to select FE_0 bit in SCON_0 register.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

Table 12. BDRCON Register

BDRCON - Baud Rate Control Register (9Bh)

7	6	5	4	3	2	1	0
-	-	-	BRR	TBCK_0	RBCK_0	SPD	SRC
Bit Number	Bit Mne- monic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit					
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	BRR	Baud Rate Run Control bit Clear to stop the internal Baud Rate Generator. Set to start the internal Baud Rate Generator.					
3	TBCK_0	Transmission Baud rate Generator Selection bit for UART_0 Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.					
2	RBCK_0	Reception Baud Rate Generator Selection bit for UART_0 Clear to select Timer 1 or Timer 2 for the Baud Rate Generator. Set to select internal Baud Rate Generator.					
1	SPD	Baud Rate Speed Control bit for UART_0 Clear to select the SLOW Baud Rate Generator. Set to select the FAST Baud Rate Generator.					
0	SRC	Baud Rate Source select bit in Mode 0 for UART_0 and UART_1 Clear to select $F_{OSC}/12$ as the Baud Rate Generator ($F_{OSC}/6$ in X2 mode). Set to select the internal Baud Rate Generator for UARTs in mode 0..					

Reset Value = XXX0 0000b

Table 13. BDRCON_1 Register

BDRCON_1 - Baud Rate Control Register for UART_1 (9Ch)

7	6	5	4	3	2	1	0
SMOD1_1	SMOD0_1	RCLK_1	TCLK_1	TBCK_1	RBCK_1	-	-
Bit Number	Bit Mnemonic	Description					
7	SMOD1_1	Serial port Mode bit 1 for UART_1 Set to select double baud rate, in mode 1, 2 and 3.					
6	SMOD0_1	SCON Select bit for UART_1 Clear to select SM0_1 bit in SCON_1 register. Set to to select FE_1 bit in SCON_1 register.					
5	RCLK_1	Receive Clock bit for UART_1 Clear to select Timer 1 as Receive Baud Rate Generator for the UART_1 Set to Select Timer 2 as the Receive Baud Rate Generator for the UART_1					
4	TCLK_1	Transmit Clock bit for UART_1 Clear to select Timer 1 as Transmit Baud Rate Generator for the UART_1 Set to Select Timer 2 as the Transmit Baud Rate Generator for the UART_1.					
3	TBCK_1	Transmission Baud rate Generator Selection bit for UART_1 Clear to select Timer 1 or Timer 2 for the Baud Rate Generator, for Tx. Set to select internal Baud Rate Generator for Tx.					
2	RBCK_1	Reception Baud Rate Generator Selection bit for UART_1 Clear to select Timer 1 or Timer 2 for the Baud Rate Generator for Rx. Set to select internal Baud Rate Generator for Rx.					
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
0	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					

Reset Value = 0000 00XXb

7.6 Alternate function on Port 1

The M1UA_1 and M0UA_1 bits located into AUXR register at bit location 7 and 6 permit to validate alternate functions located on Port 1. Following the combination of these two bits, the TxD_1 output and RxD_1 input of UART_1 take place on Port 1 pins (two different locations are possible) and the other locations of TxD_1 and RxD_1 available only for 44-pin package are no more valid.

Table 14. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
M1UA_1	M0UA_1	-	-	-	-	-	AO

Bit Number	Bit Mne-monic	Description
7	M1UA_1	Multiplex I/Os of UART_1 bit 1 This bit is used in conjunction with M0UA_1 bit to specify where are multiplexed UART_1 pins.
6	M0UA_1	Multiplex I/Os of UART_1 bit 0 This bit is used in conjunction with M1UA_1 bit to specify where are multiplexed UART_1 pins. <u>M1UA_1 M0UA_1 Result</u> 0 0 UART_1 pins are disabled. 0 1 UART_1 pins are located on pins (6, 28) or (12, 34) for 44-package only. 1 0 UART_1 pins are alternate functions of P1 located at P1.2 and P1.3. 1 1 UART_1 pins are alternate functions of P1 located at P1.6 and P1.7.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = 00XX XXX0b

Not bit addressable

7.7 Interrupt System

The TS80C51U2 has a total of 7 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2) and the two serial port interrupts. These interrupts are shown in Figure 12.

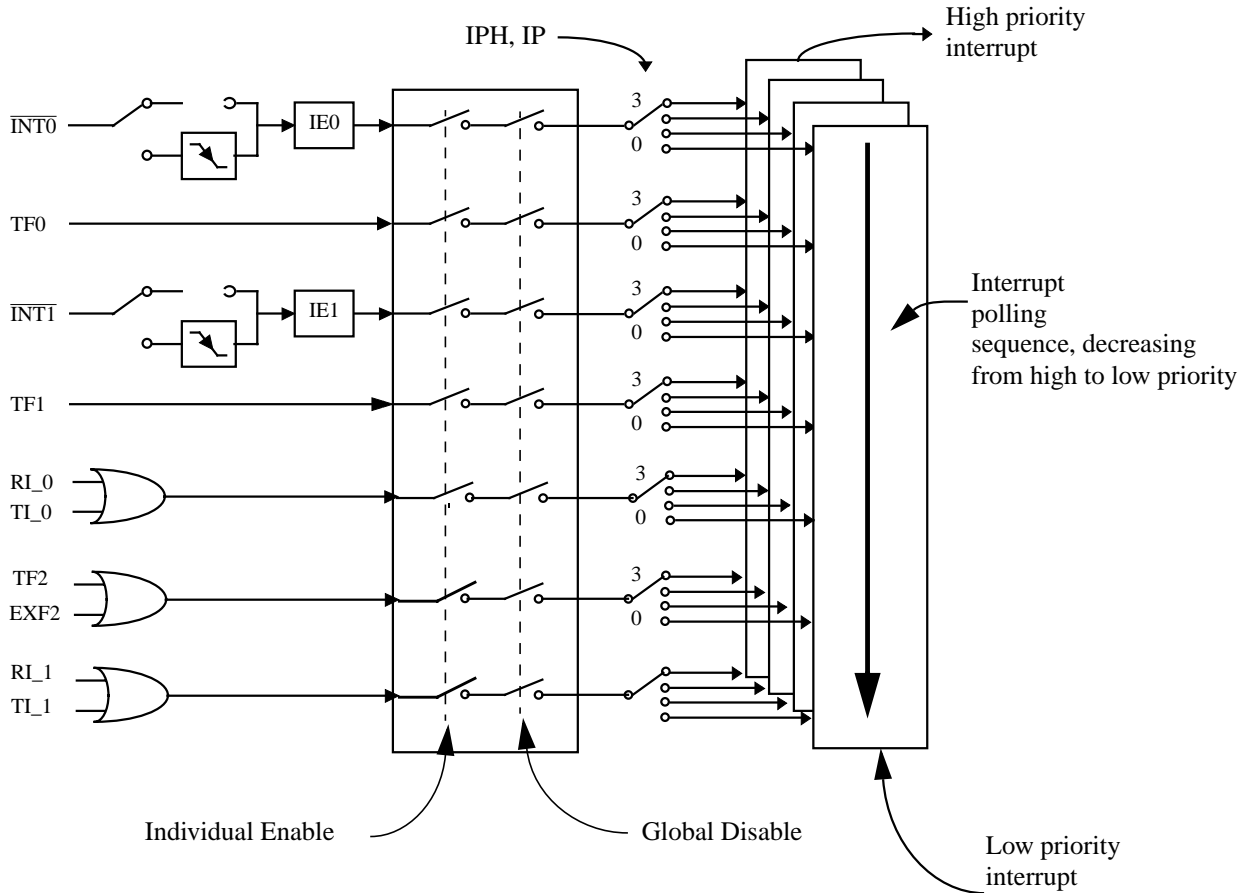


Figure 12. Interrupt Control System

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 16.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 17.) and in the Interrupt Priority High register (See Table 18.). shows the bit values and priority levels associated with each combination.

The second UART interrupt vector is located at address 0033H. All other vector addresses are the same as standard C52 devices.

Table 15. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 16. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	ES_1	ET2	ES_0	ET1	EX1	ET0	EX0
Bit Number	Bit Mnemonic	Description					
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.					
6	ES_1	Serial port Enable bit for UART_1 Clear to disable serial port interrupt. Set to enable serial port interrupt.					
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.					
4	ES_0	Serial port Enable bit for UART_0 Clear to disable serial port interrupt. Set to enable serial port interrupt.					
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.					
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.					
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.					
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.					

Reset Value = 0000 0000b

Bit addressable

Table 17. IP Register

IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	PS_1	PT2	PS_0	PT1	PX1	PT0	PX0
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
6	PS_1	Serial port Priority bit for UART_1 Refer to PSH for priority level.					
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.					
4	PS_0	Serial port Priority bit for UART_0 Refer to PSH for priority level.					
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.					
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.					
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.					
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.					

Reset Value = X000 0000b

Bit addressable

Table 18. IPH Register

IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0															
-	PSH_1	PT2H	PSH_0	PT1H	PX1H	PT0H	PX0H															
Bit Number	Bit Mnemonic	Description																				
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.																				
6	PSH_1	Serial port Priority High bit for UART_1 <table border="0"> <tr> <td><u>PSH_1</u></td> <td><u>PS_1</u></td> <td><u>Priority Level</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </table>						<u>PSH_1</u>	<u>PS_1</u>	<u>Priority Level</u>	0	0	Lowest	0	1		1	0		1	1	Highest
<u>PSH_1</u>	<u>PS_1</u>	<u>Priority Level</u>																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
5	PT2H	Timer 2 overflow interrupt Priority High bit <table border="0"> <tr> <td><u>PT2H</u></td> <td><u>PT2</u></td> <td><u>Priority Level</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </table>						<u>PT2H</u>	<u>PT2</u>	<u>Priority Level</u>	0	0	Lowest	0	1		1	0		1	1	Highest
<u>PT2H</u>	<u>PT2</u>	<u>Priority Level</u>																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
4	PSH_0	Serial port Priority High bit for UART_0 <table border="0"> <tr> <td><u>PSH_0</u></td> <td><u>PS_0</u></td> <td><u>Priority Level</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </table>						<u>PSH_0</u>	<u>PS_0</u>	<u>Priority Level</u>	0	0	Lowest	0	1		1	0		1	1	Highest
<u>PSH_0</u>	<u>PS_0</u>	<u>Priority Level</u>																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
3	PT1H	Timer 1 overflow interrupt Priority High bit <table border="0"> <tr> <td><u>PT1H</u></td> <td><u>PT1</u></td> <td><u>Priority Level</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </table>						<u>PT1H</u>	<u>PT1</u>	<u>Priority Level</u>	0	0	Lowest	0	1		1	0		1	1	Highest
<u>PT1H</u>	<u>PT1</u>	<u>Priority Level</u>																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
2	PX1H	External interrupt 1 Priority High bit <table border="0"> <tr> <td><u>PX1H</u></td> <td><u>PX1</u></td> <td><u>Priority Level</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </table>						<u>PX1H</u>	<u>PX1</u>	<u>Priority Level</u>	0	0	Lowest	0	1		1	0		1	1	Highest
<u>PX1H</u>	<u>PX1</u>	<u>Priority Level</u>																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
1	PT0H	Timer 0 overflow interrupt Priority High bit <table border="0"> <tr> <td><u>PT0H</u></td> <td><u>PT0</u></td> <td><u>Priority Level</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </table>						<u>PT0H</u>	<u>PT0</u>	<u>Priority Level</u>	0	0	Lowest	0	1		1	0		1	1	Highest
<u>PT0H</u>	<u>PT0</u>	<u>Priority Level</u>																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
0	PX0H	External interrupt 0 Priority High bit <table border="0"> <tr> <td><u>PX0H</u></td> <td><u>PX0</u></td> <td><u>Priority Level</u></td> </tr> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </table>						<u>PX0H</u>	<u>PX0</u>	<u>Priority Level</u>	0	0	Lowest	0	1		1	0		1	1	Highest
<u>PX0H</u>	<u>PX0</u>	<u>Priority Level</u>																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				

Reset Value = X000 0000b

Not bit addressable

7.8 Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

7.9 Power-Down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to 7.4.6, PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 13. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C51U2 into power-down mode.

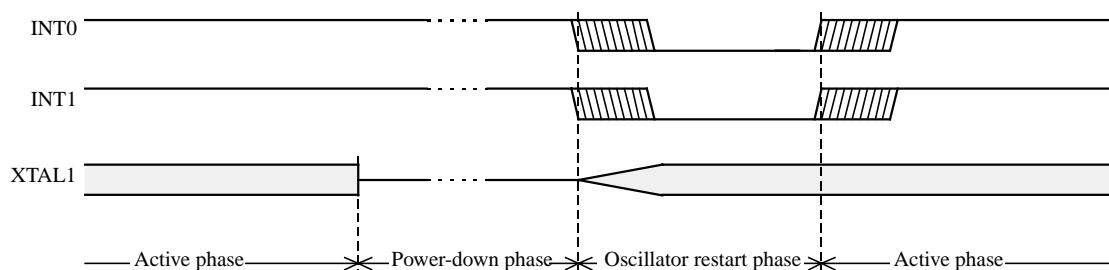


Figure 13. Power-Down Exit Waveform

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

NOTE: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 19. The state of ports during idle and power-down modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data*	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data*	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

* Port 0 can force a "zero" level. A "one" Level will leave port floating.

7.10 Hardware Watchdog Timer

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upset. The WDT consists of a 14-bit counter and the WatchDog Timer ReSeT (WDTRST) SFR. The WDT is by default disabled from exiting reset. To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, it will increment every machine cycle while the oscillator is running and there is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST-pin.

7.10.1 Using the WDT

To enable the WDT, user must write 01EH and 0E1H in sequence to the WDTRST, SFR location 0A6H. When WDT is enabled, the user needs to service it by writing to 01EH and 0E1H to WDTRST to avoid WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH) and this will reset the device. When WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycle. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST-pin. The RESET pulse duration is $96 \times T_{OSC}$, where $T_{OSC} = 1/F_{OSC}$. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

To have a more powerful WDT, a 2^7 counter has been added to extend the Time-out capability, ranking from 16ms to 2s @ $F_{OSC} = 12\text{MHz}$. To manage this feature, refer to WDTPRG register description, Table 21. (SFR0A7h).

Table 20. WDTRST Register

WDTRST Address (0A6h)

	7	6	5	4	3	2	1
Reset value	X	X	X	X	X	X	X

Write only, this SFR is used to reset/enable the WDT by writing 01EH then 0E1H in sequence.

Table 21. WDTPRG Register

WDTPRG Address (0A7h)

7	6	5	4	3	2	1	0
T4	T3	T2	T1	T0	S2	S1	S0
Bit Number	Bit Mnemonic	Description					
7	T4	Reserved Do not try to set or clear this bit.					
6	T3						
5	T2						
4	T1						
3	T0						
2	S2	WDT Time-out select bit 2					
1	S1	WDT Time-out select bit 1					
0	S0	WDT Time-out select bit 0					
		<u>S2</u>	<u>S1</u>	<u>S0</u>	<u>Selected Time-out</u>		
		0	0	0	(2 ¹⁴ - 1) machine cycles, 16.3 ms @ 12 MHz		
		0	0	1	(2 ¹⁵ - 1) machine cycles, 32.7 ms @ 12 MHz		
		0	1	0	(2 ¹⁶ - 1) machine cycles, 65.5 ms @ 12 MHz		
		0	1	1	(2 ¹⁷ - 1) machine cycles, 131 ms @ 12 MHz		
		1	0	0	(2 ¹⁸ - 1) machine cycles, 262 ms @ 12 MHz		
		1	0	1	(2 ¹⁹ - 1) machine cycles, 542 ms @ 12 MHz		
		1	1	0	(2 ²⁰ - 1) machine cycles, 1.05 s @ 12 MHz		
		1	1	1	(2 ²¹ - 1) machine cycles, 2.09 s @ 12 MHz		

Reset value XXXX X000

7.10.2 WDT during Power Down and Idle

In Power Down mode the oscillator stops, which means the WDT also stops. While in Power Down mode the user does not need to service the WDT. There are 2 methods of exiting Power Down mode: by a hardware reset or via a level activated external interrupt which is enabled prior to entering Power Down mode. When Power Down is exited with hardware reset, servicing the WDT should occur as it normally should whenever the TS80C51U2 is reset. Exiting Power Down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service routine.

To ensure that the WDT does not overflow within a few states of exiting of powerdown, it is best to reset the WDT just before entering powerdown.

In the Idle mode, the oscillator continues to run. To prevent the WDT from resetting the TS80C51U2 while in Idle mode, the user should always set up a timer that will periodically exit Idle, service the WDT, and re-enter Idle mode.

7.11 ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C51U2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C51U2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C51U2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26 shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 22. External Pin Status during ONCE Mode

ALE	$\overline{\text{PSEN}}$	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

7.12 Power-Off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 23.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a V_{cc} range from 4.5V to 5.5V. For lower V_{cc} value, reading POF bit will return indeterminate value.

Table 23. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1_0	SMOD0_0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1_0	Serial port Mode bit 1 for UART_0 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0_0	Serial port Mode bit 0 for UART_0 Clear to select SM0_0 bit in SCON_0 register. Set to to select FE_0 bit in SCON_0 register.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-Off Flag Clear to recognize next reset type. Set by hardware when V _{CC} rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	Power-Down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Reset Value = 00X1 0000b

Not bit addressable

7.13 Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 24. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
M1UA_1	M0UA_1	-	-	-	-	-	AO
Bit Number	Bit Mne- monic	Description					
7	M1UA_1	Multiplex I/Os of UART_1 bit 1 This bit is used in conjunction with M0UA_1 bit to specify where are multiplexed UART_1 pins.					
6	M0UA_1	Multiplex I/Os of UART_1 bit 0 This bit is used in conjunction with M1UA_1 bit to specify where are multiplexed UART_1 pins. M1UA_1M0UA_1Result 0 0 UART_1 pins are disabled. 0 1 UART_1 pins are located on pins (6, 28) or (12, 34) for 44-package only. 1 0 UART_1 pins are alternate functions of P1 located at P1.2 and P1.3. 1 1 UART_1 pins are alternate functions of P1 located at P1.6 and P1.7.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.					

Reset Value = 00XX XXX0b
Not bit addressable

8. TS80C51U2 ROM

8.1 ROM Structure

The TS83C51U2 ROM memory is divided in three different arrays:

- the code array: 16 Kbytes.
- the encryption array: 64 bytes.
- the signature array: 4 bytes.

8.2 ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

8.2.1 Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

8.2.2 Program Lock Bits

The lock bits when programmed according to Table 25. will provide different level of protection for the on-chip code and data.

Table 25. Program Lock bits

Program Lock Bits				Protection description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset.

U: unprogrammed
 P: programmed

8.2.3 Signature bytes

The TS83C51U2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 10.

8.2.4 Verify Algorithm

Refer to 9.3.4

9. TS87C51U2 EPROM

9.1 EPROM Structure

The TS87C51U2 EPROM is divided in two different arrays:

- the code array: 16 Kbytes.
- the encryption array: 64 bytes.

In addition a third non programmable array is implemented:

- the signature array: 4 bytes.

9.2 EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

9.2.1 Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

9.2.2 Program Lock Bits

The three lock bits, when programmed according to Table 26., will provide different level of protection for the on-chip code and data.

Table 26. Program Lock bits

Program Lock Bits				Protection description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed,
P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

9.2.3 Signature bytes

The TS87C51U2 contains 4 factory programmed signature bytes. To read these bytes, perform the process described in section 10.

9.3 EPROM Programming

9.3.1 Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C51U2 is placed in specific set-up modes (See Figure 14.).

Control and program signals must be held at the levels indicated in Table 27.

9.3.2 Definition of terms








Address Lines:P1.0-P1.7, P2.0-P2.5 respectively for A0-A13.

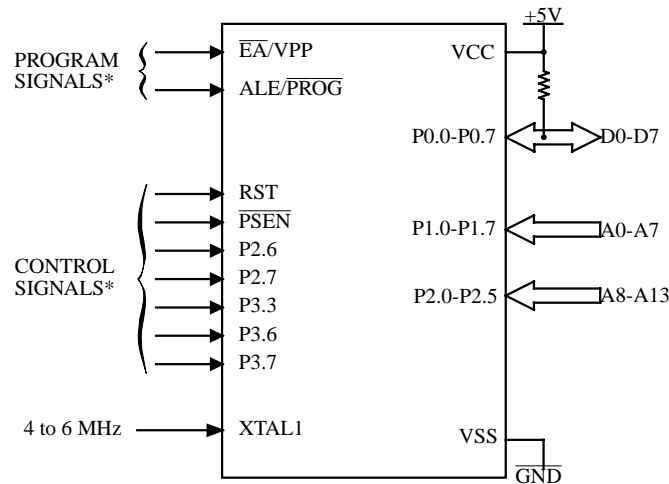
Data Lines:P0.0-P0.7 for D0-D7

Control Signals:RST, $\overline{\text{PSEN}}$, P2.6, P2.7, P3.3, P3.6, P3.7.

Program Signals:ALE/ $\overline{\text{PROG}}$, $\overline{\text{EA}}$ /VPP.

Table 27. EPROM Set-Up Modes

Mode	RST	$\overline{\text{PSEN}}$	ALE/ $\overline{\text{PROG}}$	$\overline{\text{EA}}$ / VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75V	1	1	1	1	1
Program Lock bit 2	1	0		12.75V	1	1	1	0	0
Program Lock bit 3	1	0		12.75V	1	0	1	1	0



* See Table 31. for proper value on these inputs

Figure 14. Set-Up Modes Configuration

9.3.3 Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C51U2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise \overline{EA}/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/\overline{PROG} once.
- Step 6: Lower \overline{EA}/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 15.).

9.3.4 Verify algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C51U2.

P 2.7 is used to enable data output.

To verify the TS87C51U2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 15.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

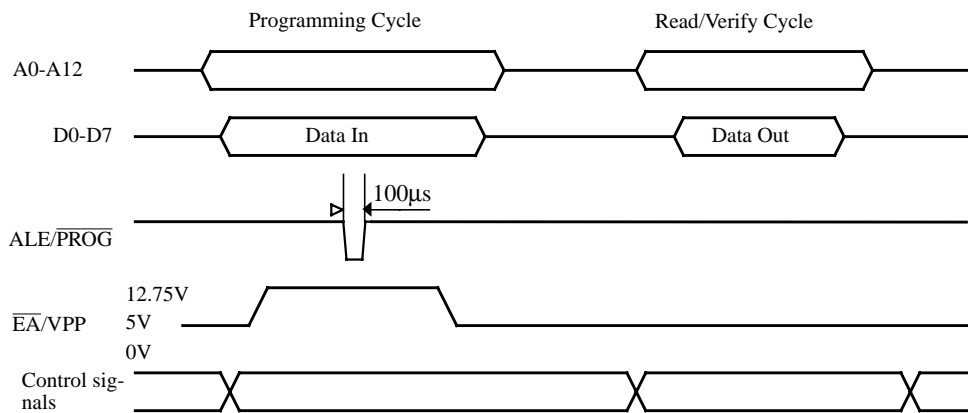


Figure 15. Programming and Verification Signal's Waveform

9.4 EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

9.4.1 Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm² rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

10. Signature Bytes

The TS83/87C51U2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 27. for Read Signature Bytes. Table 28. shows the content of the signature byte for the TS83/87C51U2.

Table 28. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: TEMIC
31h	57h	Family Code: C51 X2
60h	2Bh	Product name: TS83C51U2
60h	ABh	Product name: TS87C51U2
61h	FFh	Product revision number

11. Electrical Characteristics

11.1 Absolute Maximum Ratings ⁽¹⁾

Ambiant Temperature Under Bias:

C = commercial	0°C to 70°C
I = industrial	-40°C to 85°C
Storage Temperature	-65°C to + 150°C
Voltage on V _{CC} to V _{SS}	-0.5 V to + 7 V
Voltage on V _{PP} to V _{SS}	-0.5 V to + 13 V
Voltage on Any Pin to V _{SS}	-0.5 V to V _{CC} + 0.5 V
Power Dissipation	1 W ⁽²⁾

NOTES

1. Stresses at or above those listed under “ Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

11.2 Power consumption measurement

Since the introduction of the first C51 devices, every manufacturer made operating I_{cc} measurements under reset, which made sense for the designs were the CPU was running under reset. In TEMIC new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That’s why, while keeping measurements under Reset, TEMIC presents a new way to measure the operating I_{cc}:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = V_{cc}, RST = V_{ss}, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating I_{cc}.

11.3 DC Parameters for Standard Voltage

TA = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

TA = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5 V ± 10%; F = 0 to 40 MHz.

Table 29. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	0.2 V _{CC} + 0.9		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.3 0.45 1.0	V V V	I _{OL} = 100 μA ⁽⁴⁾ I _{OL} = 1.6 mA ⁽⁴⁾ I _{OL} = 3.5 mA ⁽⁴⁾
V _{OL1}	Output Low Voltage, port 0 ⁽⁶⁾			0.3 0.45 1.0	V V V	I _{OL} = 200 μA ⁽⁴⁾ I _{OL} = 3.2 mA ⁽⁴⁾ I _{OL} = 7.0 mA ⁽⁴⁾
V _{OL2}	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	I _{OL} = 100 μA ⁽⁴⁾ I _{OL} = 1.6 mA ⁽⁴⁾ I _{OL} = 3.5 mA ⁽⁴⁾
V _{OH}	Output High Voltage, ports 1, 2, 3	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	I _{OH} = -10 μA I _{OH} = -30 μA I _{OH} = -60 μA V _{CC} = 5 V ± 10%
V _{OH1}	Output High Voltage, port 0	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	I _{OH} = -200 μA I _{OH} = -3.2 mA I _{OH} = -7.0 mA V _{CC} = 5 V ± 10%
V _{OH2}	Output High Voltage, ALE, PSEN	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	I _{OH} = -100 μA I _{OH} = -1.6 mA I _{OH} = -3.5 mA V _{CC} = 5 V ± 10%
R _{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	kΩ	
I _{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	μA	V _{in} = 0.45 V
I _{LI}	Input Leakage Current			±10	μA	0.45 V < V _{in} < V _{CC}
I _{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μA	V _{in} = 2.0 V
C _{IO}	Capacitance of I/O Buffer			10	pF	F _c = 1 MHz T _A = 25°C
I _{PD}	Power Down Current		20 ⁽⁵⁾	50	μA	2.0 V < V _{CC} < 5.5 V ⁽³⁾
I _{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.4 Freq (MHz) @12MHz 5.8 @16MHz 7.4	mA	V _{CC} = 5.5 V ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			3 + 0.6 Freq (MHz) @12MHz 10.2 @16MHz 12.6	mA	$V_{CC} = 5.5 \text{ V}^{(8)}$
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.25+0.3 Freq (MHz) @12MHz 3.9 @16MHz 5.1	mA	$V_{CC} = 5.5 \text{ V}^{(2)}$

11.4 DC Parameters for Low Voltage

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{SS} = 0 \text{ V}$; $V_{CC} = 2.7 \text{ V}$ to $5.5 \text{ V} \pm 10\%$; $F = 0$ to 30 MHz .

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{SS} = 0 \text{ V}$; $V_{CC} = 2.7 \text{ V}$ to $5.5 \text{ V} \pm 10\%$; $F = 0$ to 30 MHz .

Table 30. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		$0.2 V_{CC} - 0.1$	V	
V_{IH}	Input High Voltage except XTAL1, RST	$0.2 V_{CC} + 0.9$		$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage, XTAL1, RST	$0.7 V_{CC}$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.45	V	$I_{OL} = 0.8 \text{ mA}^{(4)}$
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ ⁽⁶⁾			0.45	V	$I_{OL} = 1.6 \text{ mA}^{(4)}$
V_{OH}	Output High Voltage, ports 1, 2, 3	$0.9 V_{CC}$			V	$I_{OH} = -10 \mu\text{A}$
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	$0.9 V_{CC}$			V	$I_{OH} = -40 \mu\text{A}$
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	μA	$V_{in} = 0.45 \text{ V}$
I_{LI}	Input Leakage Current			± 10	μA	$0.45 \text{ V} < V_{in} < V_{CC}$
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μA	$V_{in} = 2.0 \text{ V}$
R_{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	k Ω	
CIO	Capacitance of I/O Buffer			10	pF	$F_c = 1 \text{ MHz}$ $T_A = 25^\circ\text{C}$
I_{PD}	Power Down Current		20 ⁽⁵⁾ 10 ⁽⁵⁾	50 30	μA	$V_{CC} = 2.0 \text{ V}$ to $5.5 \text{ V}^{(3)}$ $V_{CC} = 2.0 \text{ V}$ to $3.3 \text{ V}^{(3)}$
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.2 Freq (MHz) @12MHz 3.4 @16MHz 4.2	mA	$V_{CC} = 3.3 \text{ V}^{(1)}$
I_{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.3 Freq (MHz) @12MHz 4.6 @16MHz 5.8	mA	$V_{CC} = 3.3 \text{ V}^{(8)}$

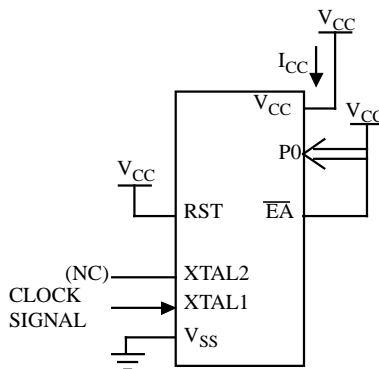
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{CC} idle	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			0.15 Freq (MHz) + 0.2 @ 12MHz 2 @ 16MHz 2.6	mA	$V_{CC} = 3.3 \text{ V}^{(2)}$

NOTES

- I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$ (see Figure 20.), $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; $\overline{EA} = RST = \text{Port } 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used.
- Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$, $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; Port 0 = V_{CC} ; $\overline{EA} = RST = V_{SS}$ (see Figure 18.).
- Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{SS}$; PORT 0 = V_{CC} ; XTAL2 N.C.; RST = V_{SS} (see Figure 19.).
- Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.
- Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
- Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port:
Port 0: 26 mA
Ports 1, 2 and 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5 \text{ ns}$ (see Figure 20.), $V_{IL} = V_{SS} + 0.5 \text{ V}$, $V_{IH} = V_{CC} - 0.5 \text{ V}$; XTAL2 N.C.; $\overline{EA} = \text{Port } 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.



All other pins are disconnected.

Figure 16. I_{CC} Test Condition, under reset

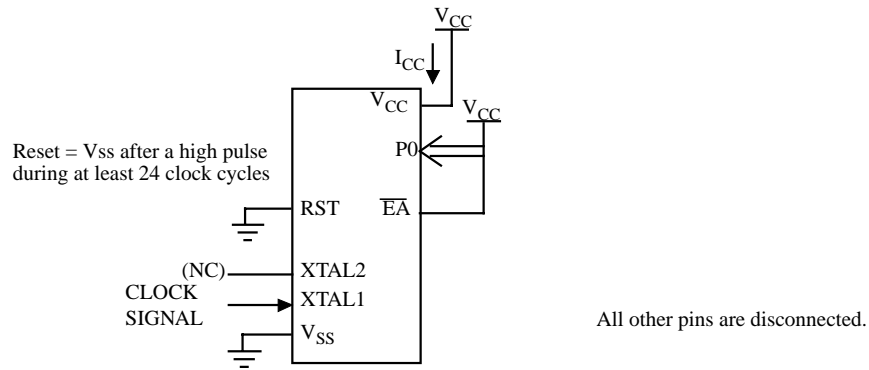


Figure 17. Operating I_{CC} Test Condition

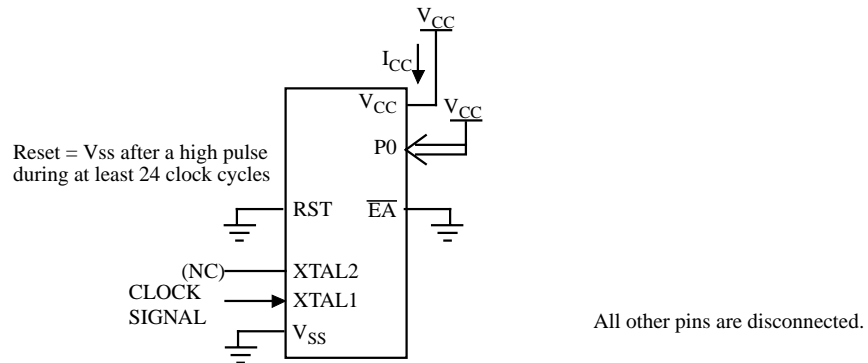


Figure 18. I_{CC} Test Condition, Idle Mode

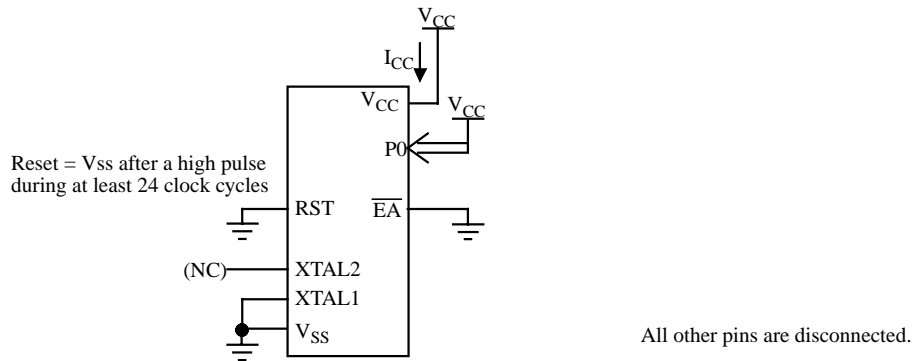


Figure 19. I_{CC} Test Condition, Power-Down Mode

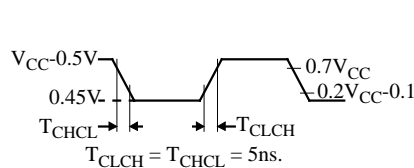


Figure 20. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes

11.5 AC Parameters

11.5.1 Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.

T_{LLPL} = Time for ALE Low to \overline{PSEN} Low.

$T_A = 0$ to $+70^\circ\text{C}$ (commercial temperature range); $V_{SS} = 0$ V; $V_{CC} = 5$ V \pm 10%; -M and -V ranges.

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (industrial temperature range); $V_{SS} = 0$ V; $V_{CC} = 5$ V \pm 10%; -M and -V ranges.

$T_A = 0$ to $+70^\circ\text{C}$ (commercial temperature range); $V_{SS} = 0$ V; 2.7 V $< V_{CC} < 5.5$ V; -L range.

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (industrial temperature range); $V_{SS} = 0$ V; 2.7 V $< V_{CC} < 5.5$ V; -L range.

Table 31. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and \overline{PSEN} signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 31. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / \overline{PSEN}	100	30	100

Table 33., Table 36. and Table 39. give the description of each AC symbols.

Table 34., Table 37. and Table 40. give for each range the AC parameter.

Table 35., Table 38. and Table 41. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 32. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz ($T = 1/20^{E6} = 50$ ns):

x = 25 (Table 35.)

T = 50ns

$T_{LLIV} = 2T - x = 2 \times 50 - 25 = 75$ ns

11.5.2 External Program Memory Characteristics

Table 33. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T _{LHLL}	ALE pulse width
T _{AVLL}	Address Valid to ALE
T _{LLAX}	Address Hold After ALE
T _{LLIV}	ALE to Valid Instruction In
T _{LLPL}	ALE to $\overline{\text{PSEN}}$
T _{PLPH}	$\overline{\text{PSEN}}$ Pulse Width
T _{PLIV}	$\overline{\text{PSEN}}$ to Valid Instruction In
T _{PXIX}	Input Instruction Hold After $\overline{\text{PSEN}}$
T _{PXIZ}	Input Instruction Float After $\overline{\text{PSEN}}$
T _{PXAV}	$\overline{\text{PSEN}}$ to Address Valid
T _{AVIV}	Address to Valid Instruction In
T _{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float

Table 34. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

Table 35. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T_{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T_{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T_{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T_{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T_{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

11.5.3 External Program Memory Read Cycle

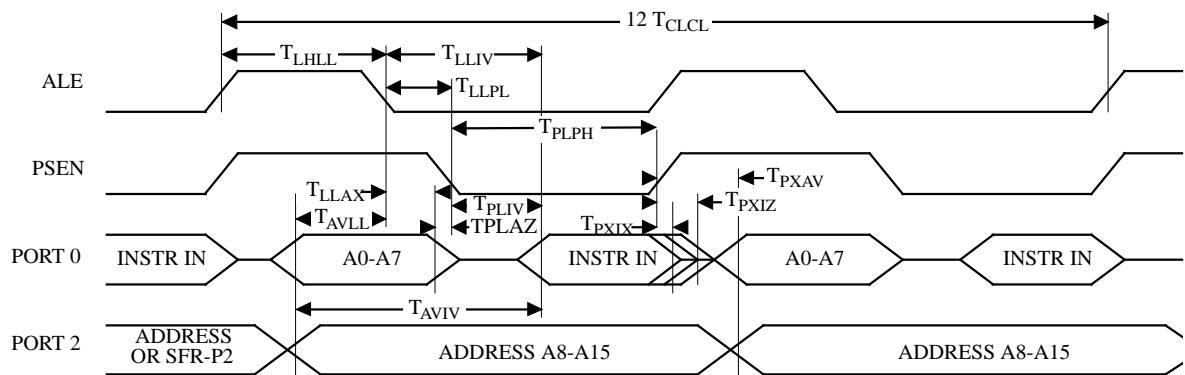


Figure 21. External Program Memory Read Cycle

11.5.4 External Data Memory Characteristics

Table 36. Symbol Description

Symbol	Parameter
T_{RLRH}	\overline{RD} Pulse Width
T_{WLWH}	\overline{WR} Pulse Width
T_{RLDV}	\overline{RD} to Valid Data In
T_{RHDX}	Data Hold After \overline{RD}
T_{RHDZ}	Data Float After \overline{RD}
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to \overline{WR} or \overline{RD}
T_{AVWL}	Address to \overline{WR} or \overline{RD}
T_{QVWX}	Data Valid to \overline{WR} Transition
T_{QVWH}	Data set-up to \overline{WR} High
T_{WHQX}	Data Hold After \overline{WR}
T_{RLAZ}	\overline{RD} Low to Address Float
T_{WHLH}	\overline{RD} or \overline{WR} High to ALE high

Table 37. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{RLRH}	130		85		135		125		175		ns
T _{WLWH}	130		85		135		125		175		ns
T _{RLDV}		100		60		102		95		137	ns
T _{RHDX}	0		0		0		0		0		ns
T _{RHDZ}		30		18		35		25		42	ns
T _{LLDV}		160		98		165		155		222	ns
T _{AVDV}		165		100		175		160		235	ns
T _{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T _{AVWL}	75		47		80		70		103		ns
T _{QVWX}	10		7		15		5		13		ns
T _{QVWH}	160		107		165		155		213		ns
T _{WHQX}	15		9		17		10		18		ns
T _{RLAZ}		0		0		0		0		0	ns
T _{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Table 38. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T_{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T_{RHDX}	Min	x	x	0	0	0	ns
T_{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T_{LLDV}	Max	8 T - x	4T - x	40	35	45	ns
T_{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T_{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T_{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T_{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T_{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T_{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T_{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T_{RLAZ}	Max	x	x	0	0	0	ns
T_{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T_{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

11.5.5 External Data Memory Write Cycle

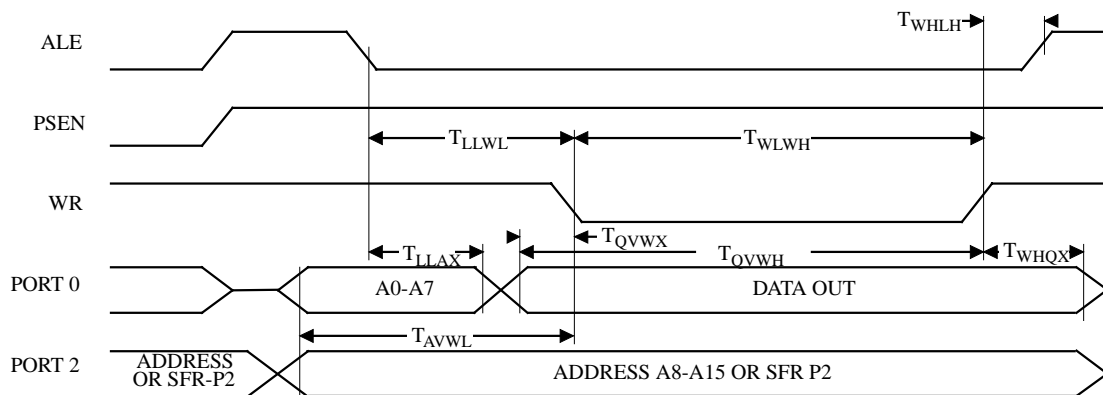


Figure 22. External Data Memory Write Cycle

11.5.6 External Data Memory Read Cycle

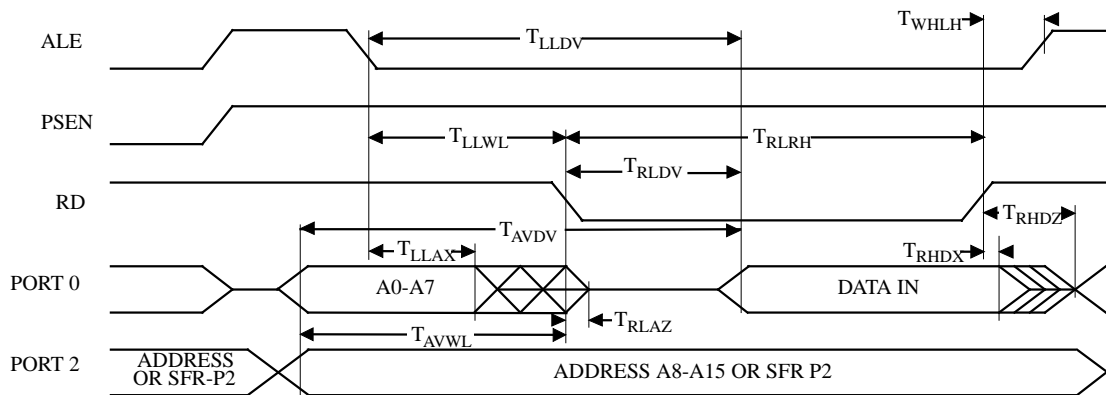


Figure 23. External Data Memory Read Cycle

11.5.7 Serial Port Timing - Shift Register Mode

Table 39. Symbol Description

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHdv}	Clock rising edge to input data valid

Table 40. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{XLXL}	300		200		300		300		400		ns
T_{QVHX}	200		117		200		200		283		ns
T_{XHQX}	30		13		30		30		47		ns
T_{XHDX}	0		0		0		0		0		ns
T_{XHdv}		117		34		117		117		200	ns

Table 41. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{XLXL}	Min	12 T	6 T				ns
T_{QVXH}	Min	10 T - x	5 T - x	50	50	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T_{XHDX}	Min	x	x	0	0	0	ns
T_{XHDTV}	Max	10 T - x	5 T - x	133	133	133	ns

11.5.8 Shift Register Timing Waveforms

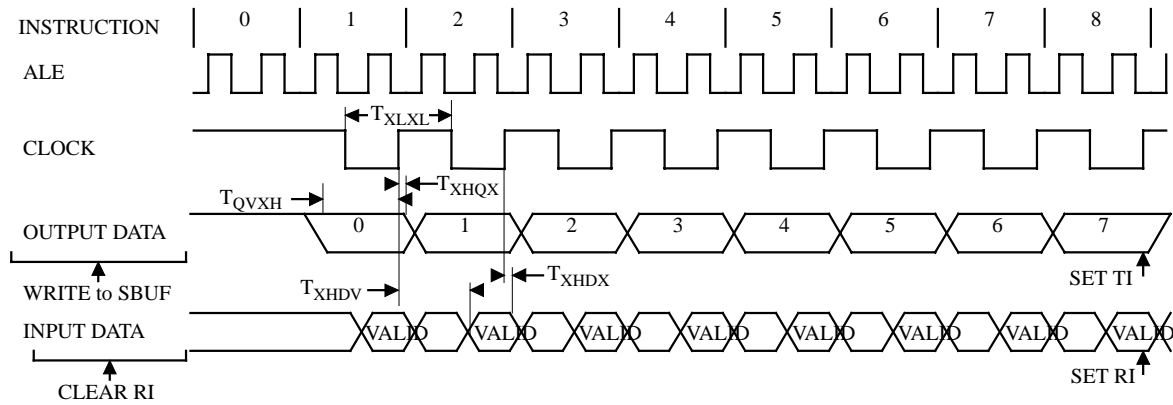


Figure 24. Shift Register Timing Waveforms

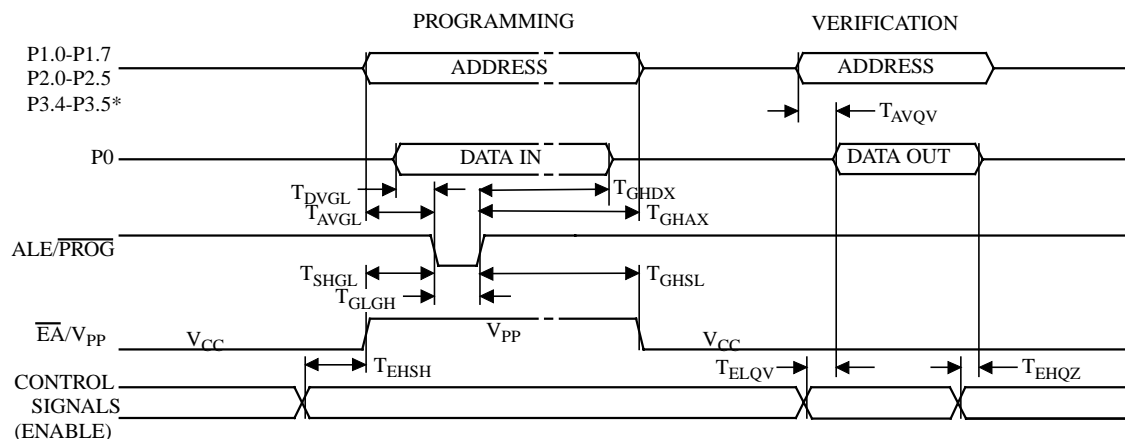
11.5.9 EPROM Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$ to 27°C ; $V_{SS} = 0\text{V}$; $V_{CC} = 5\text{V} \pm 10\%$ while programming. V_{CC} = operating range while verifying

Table 42. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHAX}	Address Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{DVGL}	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
T_{GHDX}	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
T_{EHS}	(Enable) High to V_{PP}	$48 T_{CLCL}$		
T_{SHGL}	V_{PP} Setup to $\overline{\text{PROG}}$ Low	10		μs
T_{GHSL}	V_{PP} Hold after $\overline{\text{PROG}}$	10		μs
T_{GLGH}	$\overline{\text{PROG}}$ Width	90	110	μs
T_{AVQV}	Address to Valid Data		$48 T_{CLCL}$	
T_{ELQV}	ENABLE Low to Data Valid		$48 T_{CLCL}$	
T_{EHQZ}	Data Float after ENABLE	0	$48 T_{CLCL}$	

11.5.10 EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Figure 25. EPROM Programming and Verification Waveforms

11.5.11 External Clock Drive Characteristics (XTAL1)

Table 43. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

11.5.12 External Clock Drive Waveforms

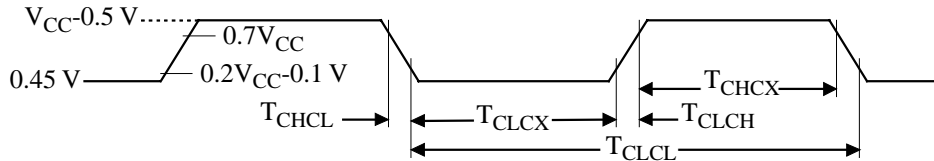


Figure 26. External Clock Drive Waveforms

11.5.13 AC Testing Input/Output Waveforms

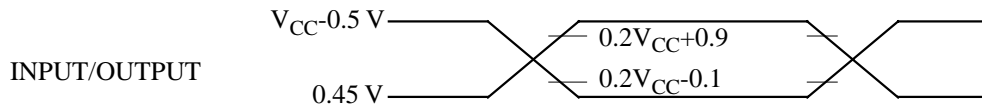


Figure 27. AC Testing Input/Output Waveforms

AC inputs during testing are driven at $V_{CC} - 0.5$ for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

11.5.14 Float Waveforms

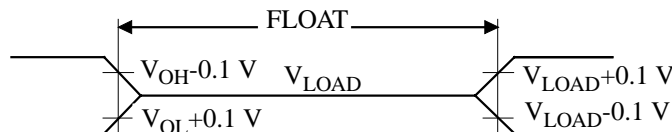


Figure 28. Float Waveforms

For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20mA$.

11.5.15 Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

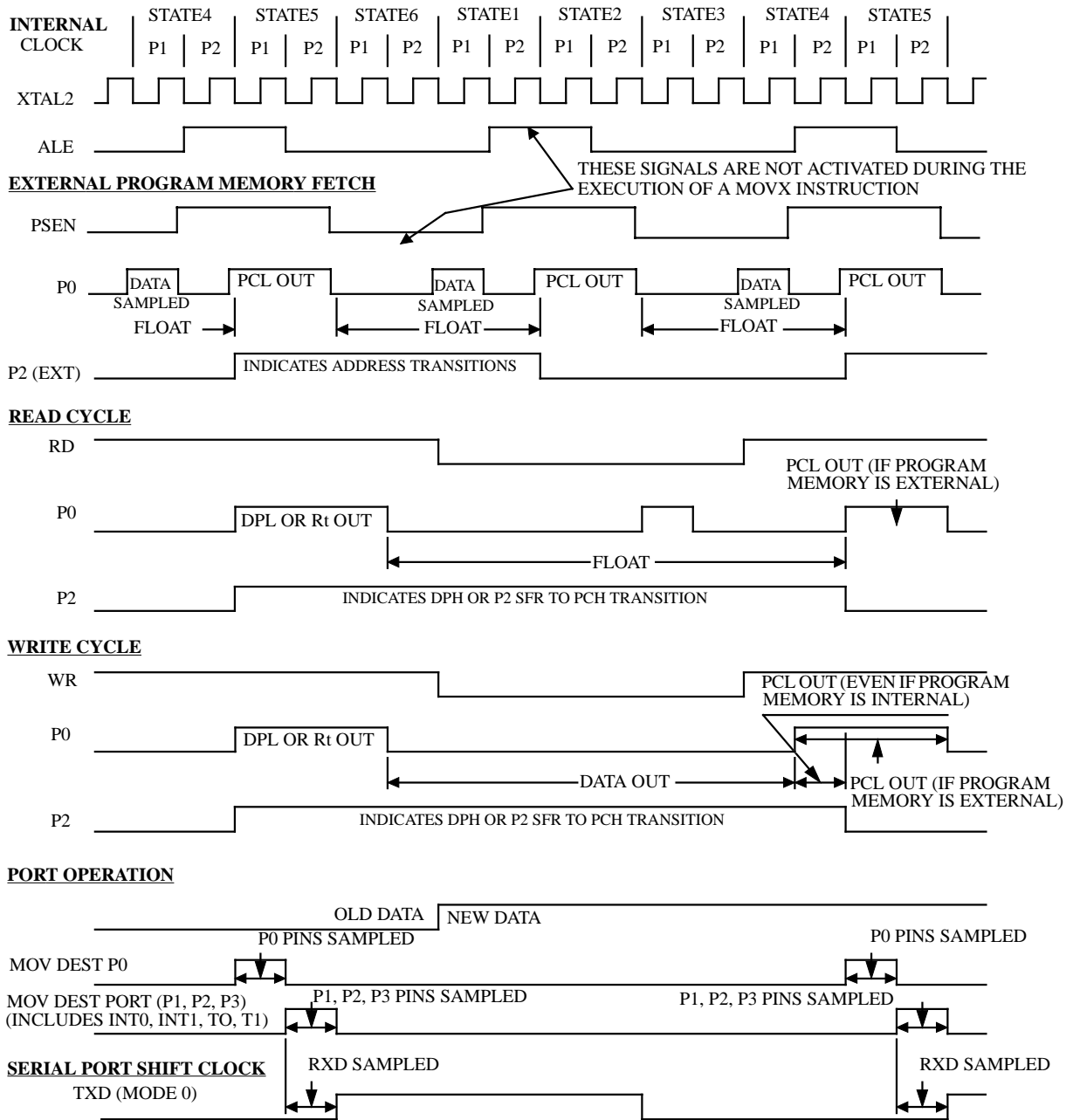
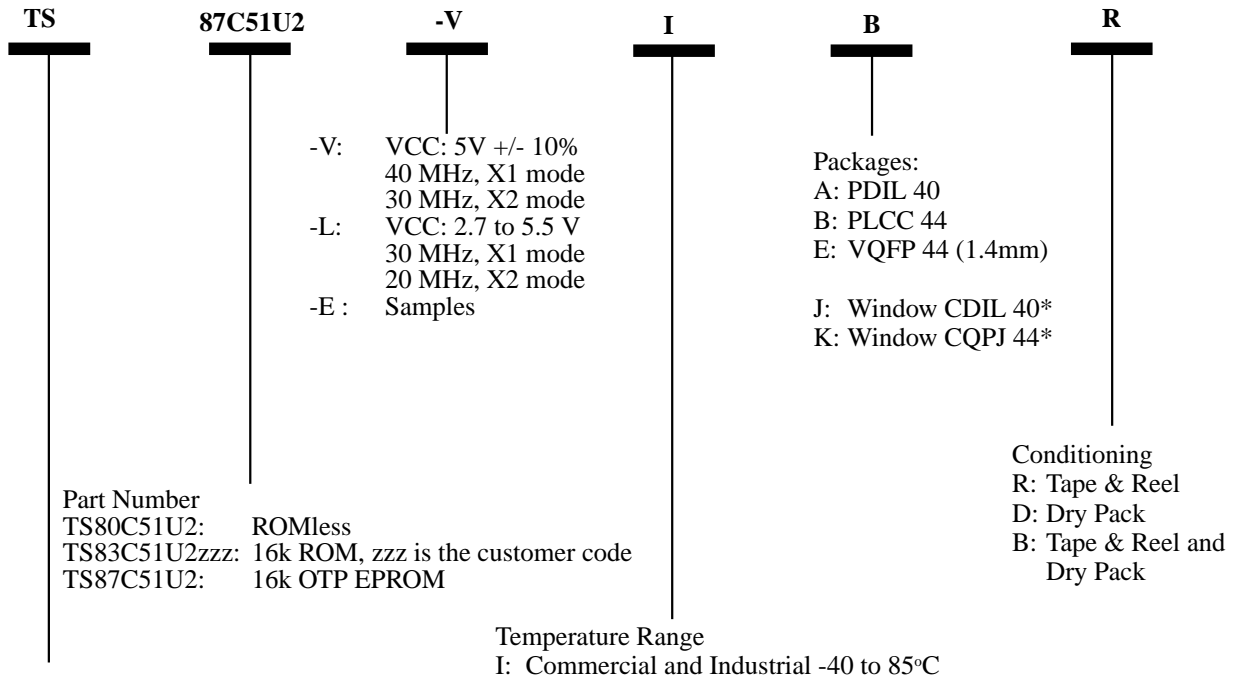


Figure 29. Clock Waveforms

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A=25^\circ C$ fully loaded) RD and WR propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

12. Ordering Information



(*) Check with TEMIC Sales Office for availability - Ceramic parts only for OTP (TS87C51U2)
 Ceramic packages (J, K) are available for prototyping, not for volume production.

Table 44. Maximum Clock Frequency

Code	-M	-V	-L	Unit
Standard Mode, oscillator frequency	40	40	30	MHz
Standard Mode, internal frequency	40	40	30	
X2 Mode, oscillator frequency	20	30	20	MHz
X2 Mode, internal equivalent frequency	40	60	40	

Table 45. Possible Ordering Entries

	TS80C51U2 ROMless	TS83C51U2zzz 16K ROM	TS87C51U2 16K OTP
-VIA	X	X	X
-VIB	X	X	X
-VIE	X	X	X
-LIA	X	X	X
-LIB	X	X	X
-LIE	X	X	X
-EA	X		X
-EB	X		X
-EE	X		X
-EJ			X
-EK			X

- -Ex for samples
- Tape and Reel available for B and E packages
- Dry pack mandatory for E packages