CMOS single-chip 8-bit MCU with 12-bit ADC and LDO

Main features

8-bit Microcontroller with high performance M8051 CPU

Basic MCU Function

- 6 Kbytes Flash Code Memory
- Code Area Protection
- 256 bytes SRAM Data Memory

Built-in Analog Function

- Power-On Reset and Low Voltage Indicator Reset
- Internal 32 MHz RC Oscillator

Peripheral features

- 12-bit Analog to Digital Converter with 2.5V LDO

I/O and packages

- Up to 18 programmable I/O lines with 20pin package
- Package types 20QFN, 20TSSOP, 16SOPN

Operating conditions

- -40°C to 85°C temperature range
- 2.2V to 5.5V wide operation range

Application

- Battery charge & discharge control
- Small home appliance

MC96F1206

Data Sheet

V 1.5

Revised 18 Sept, 2018

Revision history

Version	Date	Revision list
1.0	2016.01.18	Initial Release
1.1	2016.04.20	Delete 'ENBODST' in BODR register Update MCU stabilization time Update table format and contents in 7 Electrical Characteristics Add 7.11 Operating Voltage Range and 7.12 Typical Characteristics Change 'VREF2P3EN' to 'VREF2P3SEL' in LDOCR Change BOD to LVI (name change)
1.2	2016.06.29	Correct '24QFN' to '20QFN' in Figure 3.1 Correct PIN Number in Figure 3.3 Update 20QFN package diagram in Figure 4.1 Delete 20SOP package
1.3	2017.03.16	Correct symbol discrepancies in 7 Electrical characteristics. Correct WDT block diagram in Figure 10.2.
1.4	2017.04.25	Update 20TSSOP package diagram in Figure 4.2 Update 16SOPN package diagram in Figure 4.3 Correct ordering information in Table 1.1
1.5	2018.09.18	Revised this book. Added Nomenclature Figure 1.1 Update Figure 1.4 OCD Interface Circuit Added Chapter 1.3.3 OCD Port Operation. Updated Chapter 7.5 Power-On Reset VDD Voltage Rising Time. Added Chapter 7.13 Recommended Application Circuit. Updated POD (20-QFN_3x3)

Version 1.5

Published by AE team

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1 Overview

1.1. Description

The MC96F1206 is an advanced CMOS 8-bit microcontroller with 6 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 6 Kbytes of FLASH, 256 bytes of SRAM, 16-bit timer/counter/PWM, Watchdog timer with WDTOSC, 12-bit ADC with LDO, On-chip POR, LVI and LVR, Internal RC-Oscillator, Internal WDT-Oscillator and clock circuitry. The MC96F1206 also supports Power saving modes to reduce Power Consumption.

Device Name	FLASH	IRAM	XRAM	ADC	I/O PORT	Package
MC96F1206USBN	6 Kbytes	256 bytes	-	15 inputs	18	20-QFN
MC96F1206RBN	6 Kbytes	256 bytes	-	15 inputs	18	20-TSSOP
MC96F1206MBN	6 Kbytes	256 bytes	-	12 inputs	14	16-SOPN

Table 1.1 Ordering Information of MC96F1206

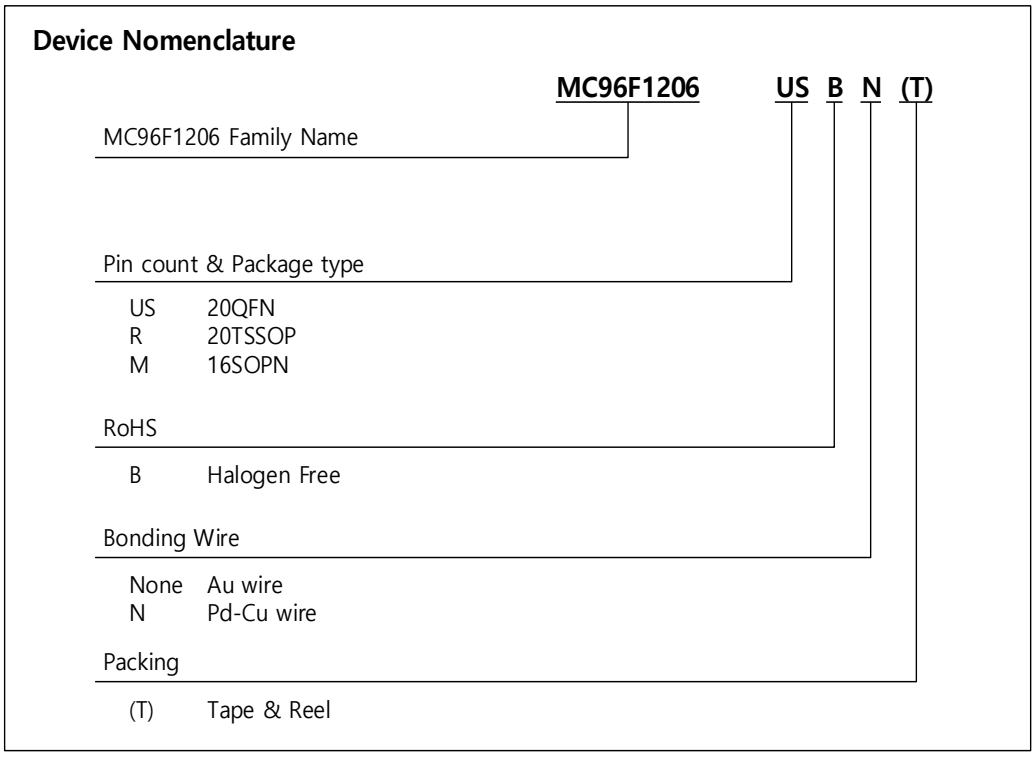


Figure 1.1 Device Nomenclature

1.2 Features

- **CPU**
  - M8051 (8051 Compatible, 2 clock per cycle)
- **6 Kbytes On-Chip FLASH**
  - Endurance : 10,000 times at room temperature
  - Retention : 10 years
  - Self-Writing (Code protect option)
- 256 bytes IRAM
- **Input Output Ports**
  - GPIO 18
- **Timer/Counter**
  - 16-bit × 2-ch (Timer0, Timer1)
  - Basic Interval Timer
- **PWM** (16-bit 2-ch, Using Timer0,1)
- **Watch Dog Timer**
- **12-bit A/D Converter**
  - 15-Input channels
  - Internal 2.5V LDO reference (option)
- **Interrupt Sources**
  - External Interrupts (3, with PCI)
  - Timer (2)
  - ADC (1)
  - BIT (1)
  - WDT (1)
  - LVI (1)
- **On-Chip RC-Oscillator**
  - 32MHz (±5%) Oscillator
- **On-Chip WDT-Oscillator**
  - 8kHz (±50%) Oscillator
- **Power On Reset**
  - 1.1 V
- **Low Voltage Reset**
  - 1-Level (1.75 V)
- **Low Voltage Indicator**
  - 3-Level (2.1 V, 2.5 V, 3.5 V)
- **Minimum Instruction Execution Time**
  - 125ns (@16MHz, NOP Instruction)
- **Power Down Mode**
  - IDLE, STOP1, STOP2 mode
- **Operating Frequency**
  - 16 MHz
- **Operating Voltage**
  - 2.2V~5.5V
- **Operating Temperature :** –40 ~ +85℃
- **Package Type**
  - 20 QFN/TSSOP, 16 SOPN
  - Pb free package

1.3 Development tools

1.3.1 Compiler

ABOV semiconductor does not provide any compiler for the MC96F1206. But the CPU core of MC96F1206 is M8051 core, you can use all kinds of third party's standard 8051 compiler like Keil C Compiler, Open Source SDCC (Small Device C Compiler). These compilers' output debug information can be integrated with our OCD2 emulator and debugger. Refer to OCD2 manual for more details.

1.3.2 OCD2 emulator and debugger

The OCD2 emulator supports ABOV Semiconductor’s 8051 series MCU emulation.

The OCD2 interface uses two wires interfacing between PC and MCU which is attached to user’s system. The OCD2 can read or change the value of MCU internal memory and I/O peripherals. And also the OCD2 controls MCU internal debugging logic, it means OCD2 controls emulation, step run, monitoring etc.

The OCD2 Debugger program works on Microsoft-Windows NT, 2000, XP, Vista (32-bit), 7, 8, 8.1 operating system.

If you want to see more details, please refer OCD2 debugger manual. You can download debugger S/W and manual from our web-site.

1.3.3 OCD Port Operation

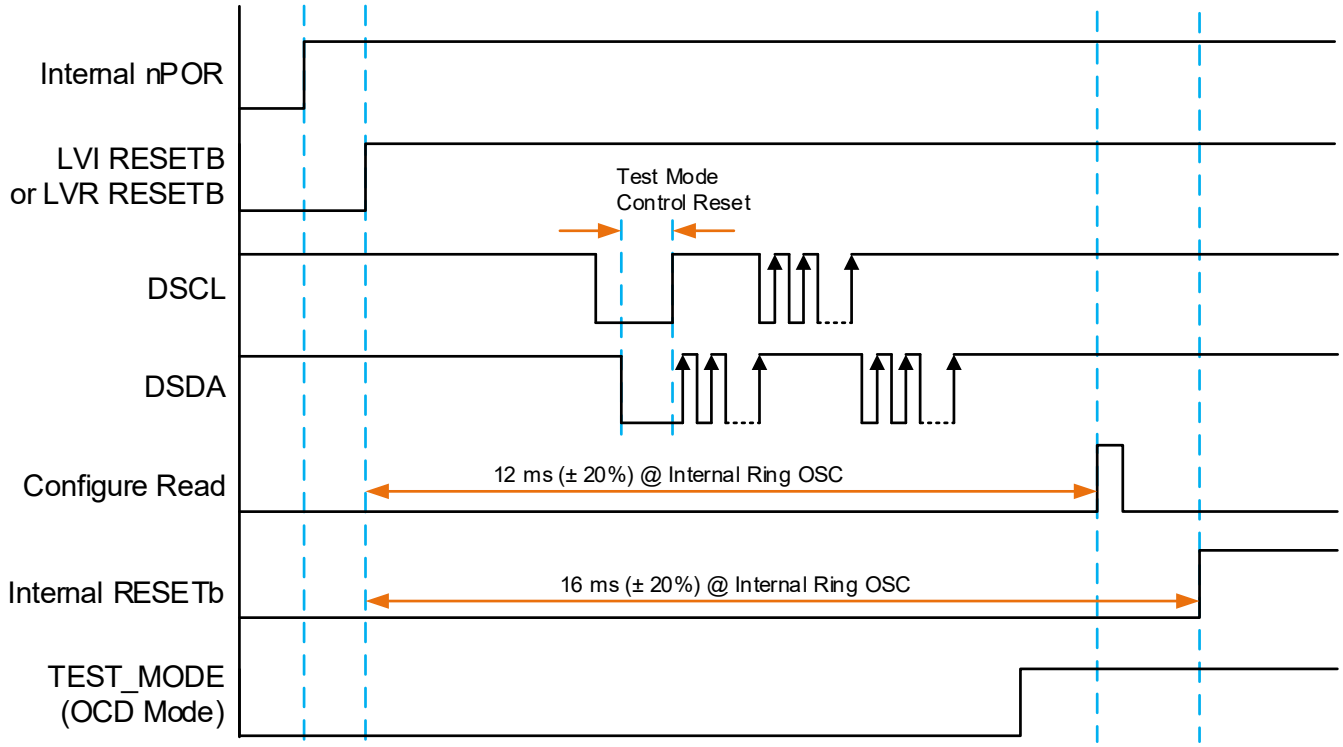


Figure 1.2 OCD Mode Sequence

The OCD port is used for flash program writing and device debugging. The device has a section that determines whether to use it in that mode of POR. This is done when the internal reset is cleared and waiting to clear Configure Read and Internal Reset. If the internal reset is cleared and DSCL and DSDA wait for a period of time from internal pull-up 'high' to 'low', the internal controller for entering test mode is initialized. Then, when DSCA and DSCA appointed communication, the test mode is entered.

As described above, OCD port is a port for special purpose. Even if it is used as Normal GPIO in User Program, it is necessary to limit the state to prevent malfunction during POR. Therefore, it is recommended to connect Pull-up Resistor to the outside of OCD Port and to fix OCD Port input to VDD / GND at POR. If it is difficult to apply pull-up on the circuit, install at least 0.1uf bypass capacitor to prevent Floating state at POR. However, if you install a bypass cap, you can not use on board writing and OCD Debugger.

There are OCD2 mode connection

- P01 (MC96F1206 DSCL pin)
- P00 (MC96F1206 DSDA pin)

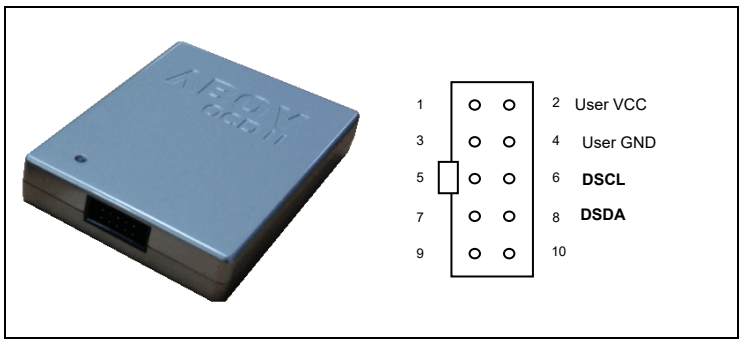


Figure 1.3 On Chip Debugger 2 and Pin description

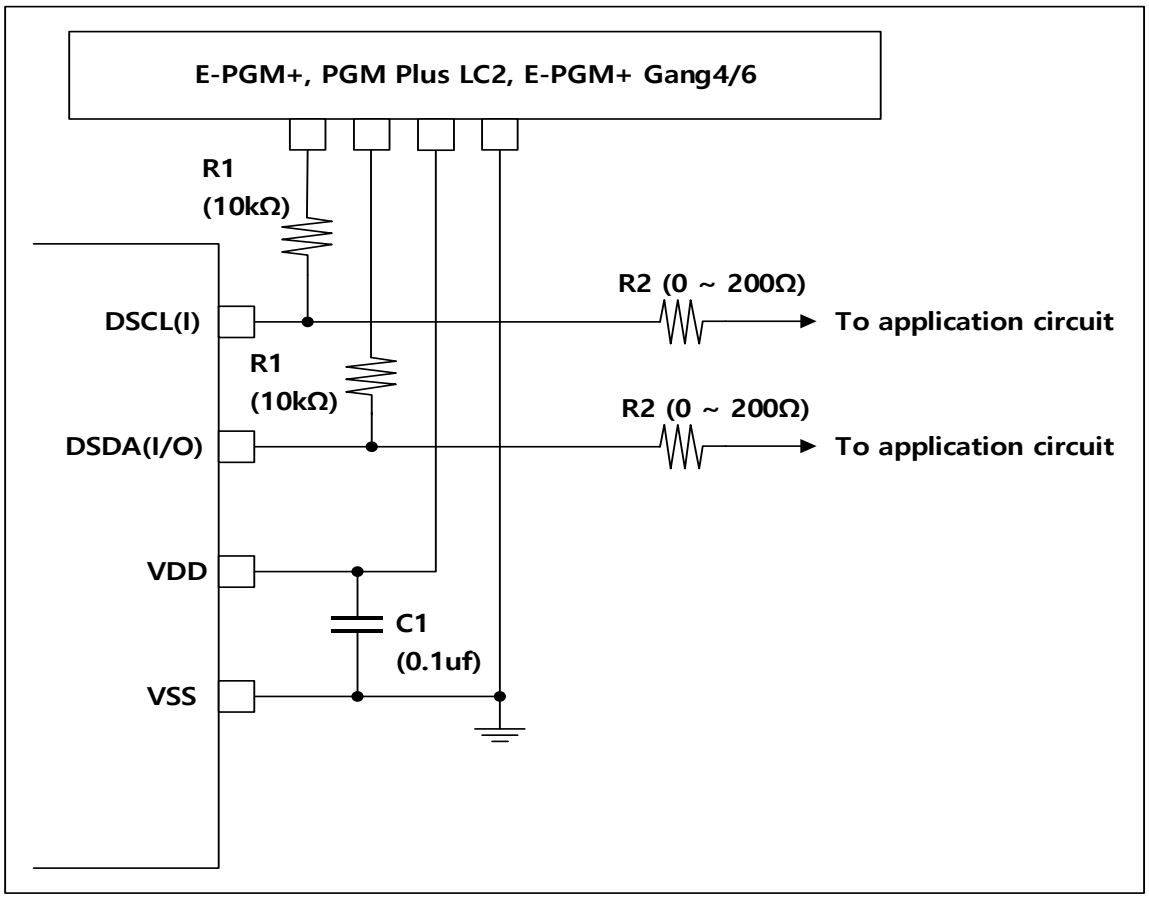


Figure 1.4 OCD Interface Circuit

NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1, R2 and C1 is recommended value. It varies with circuit of system.

OCD2 (On Chip Debug) Emulator

- MCU emulation control via 2pin or 3pin OCD interface.
- 2pin interface : OCD2 clock & data.
- 1pin option interface
  - Support device OCD2 mode entry during user S/W is running.
  - Support exact emulation time measurement.
- Higher interface speed than OCD dongle.
- Support newly added debugging specifications.
  - Data access break (1, 2, 4bytes),
  - internal OSC Frequency measurement and trimming, etc.
- Compact size.
- Cost effective emulator.
- Emulation & debugging on the target system directly.
- Real time emulation.
- PC interface : USB.

Debugger

- Operates with OCD2 emulator H/W.
- Integrated Development Environment (IDE).
  Support docking windows and menus.
- Support Free run, Step run, auto step run.
- Support Symbolic debugging.
- Support Source level debugging.

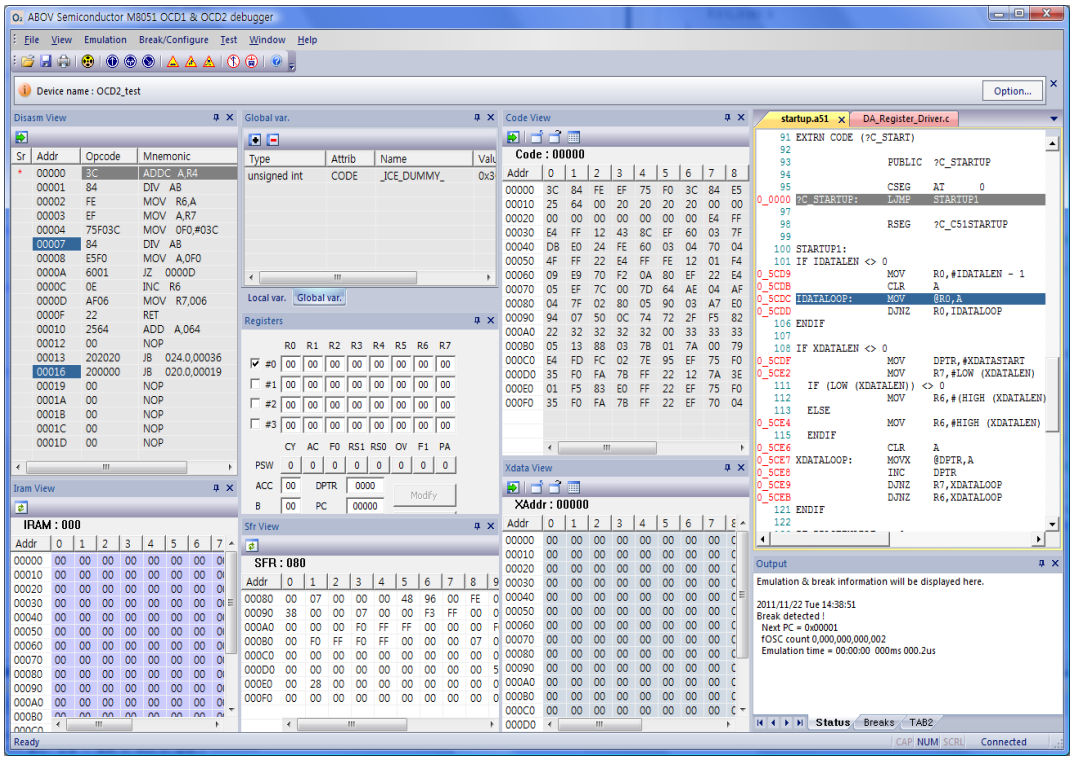


Figure 1.5 OCD Debugger

Support Devices

- MC95xxxx
- MC96xxxx
- MC97xxxx

1.3.4 Programmer

E-PGM +

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller : 32 bit MCU @ 72MHz
- Buffer memory : 1 MByte

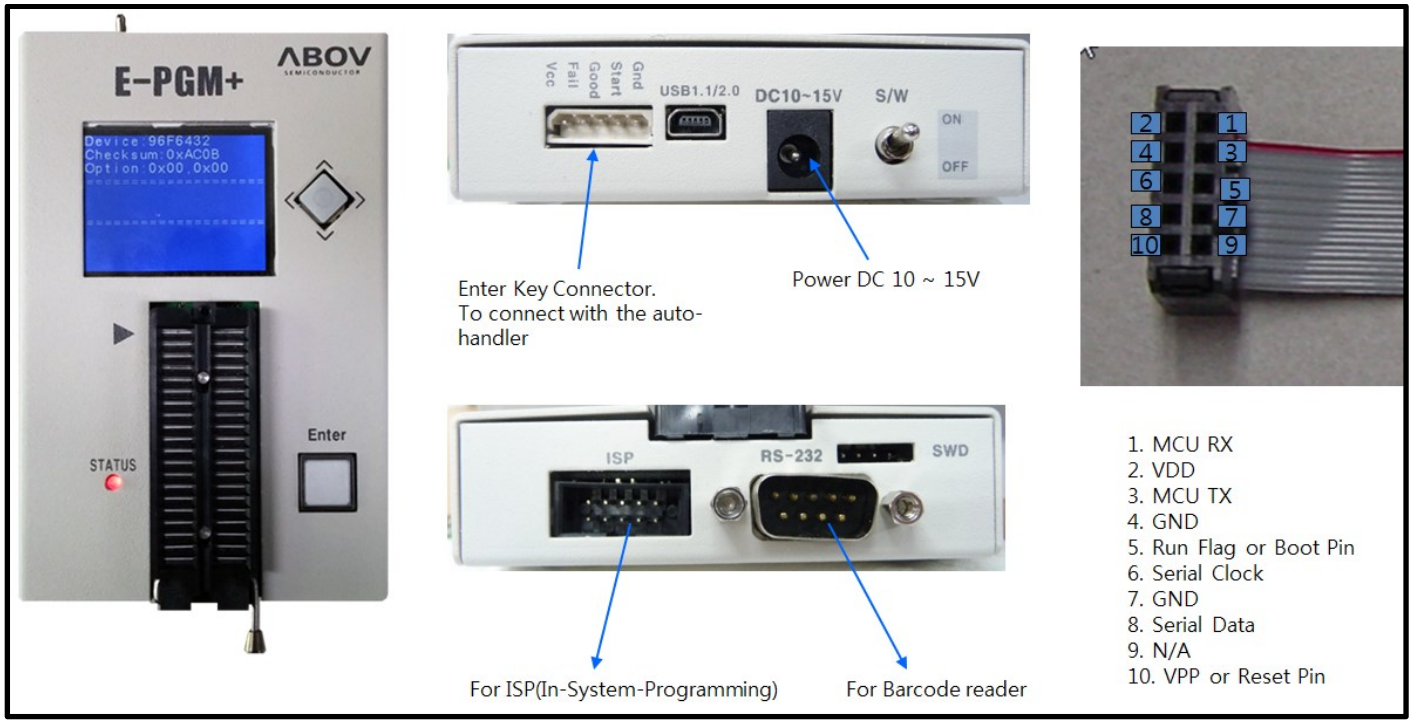


Figure 1.6 PGMplus USB

PGMPlusLC 2

Description

PGMPlusLC2 is for ISP (In System Programming). It is used to write into the MCU Which is already mounted on target board using 10pin cable.

Features

- PGMplusLC2 is low cost writing Tool.
- USB interface is supported.
- Not need USB driver installation.
- Connect the external power adaptor (5v@2A).
- Fast 32-bit Cortex-M3 MCU is used.
- Supported high voltage Max 18V.
- PGMplusLC2 is based on PC environment.
- PGMplusLC2 is faster than PGMplusLC.
- Transmission speed is 64Kbyte/s

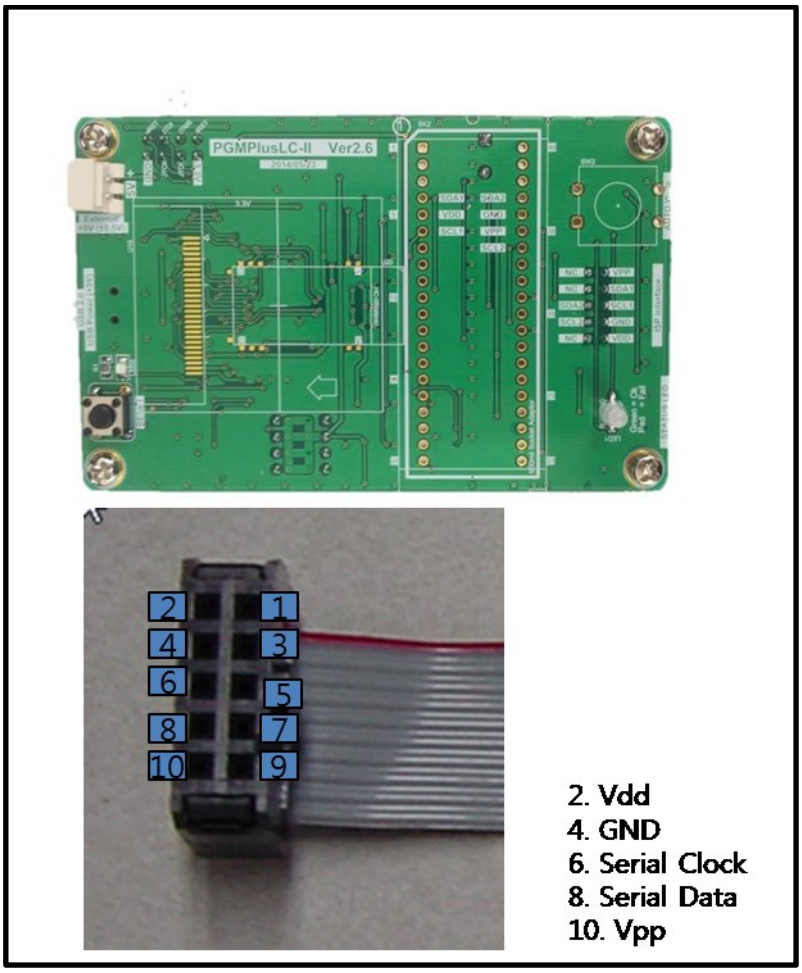


Figure 1.7 PGMplusLC Writer

E-PGM+ Gang4/6

- Product name : **E-PGM+ GANG 4**
- Dimension(x , y, h) : 33.5 x 22.5 x35mm
- Weight : 2.0kg
- Input Voltage : DC Adaptor 15V/2A
- Power Consumption :
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

- Product name : **E-PGM+ GANG 6**
- Dimension(x , y, h) : 148.2 x 22.5 x35mm
- Weight : 2.8kg

- Input Voltage : DC Adaptor 15V/2A
- Power Consumption :
- Operating Temp : -10 ~ 40℃
- Storage Temp : -30 ~ 80℃
- Water Proof : No

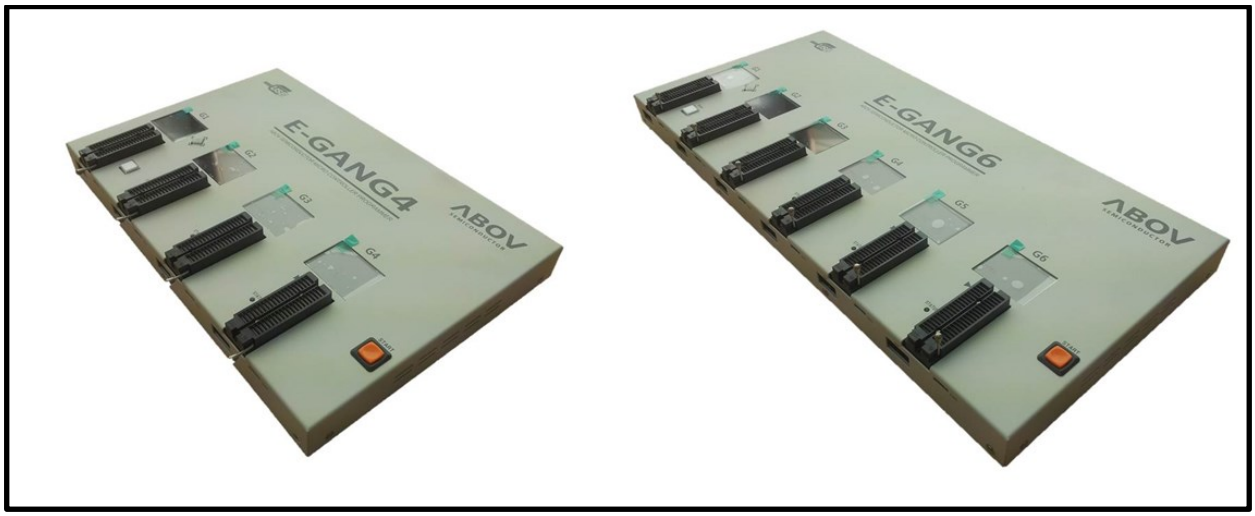


Figure 1.8 Gang Programmer

2 Block diagram

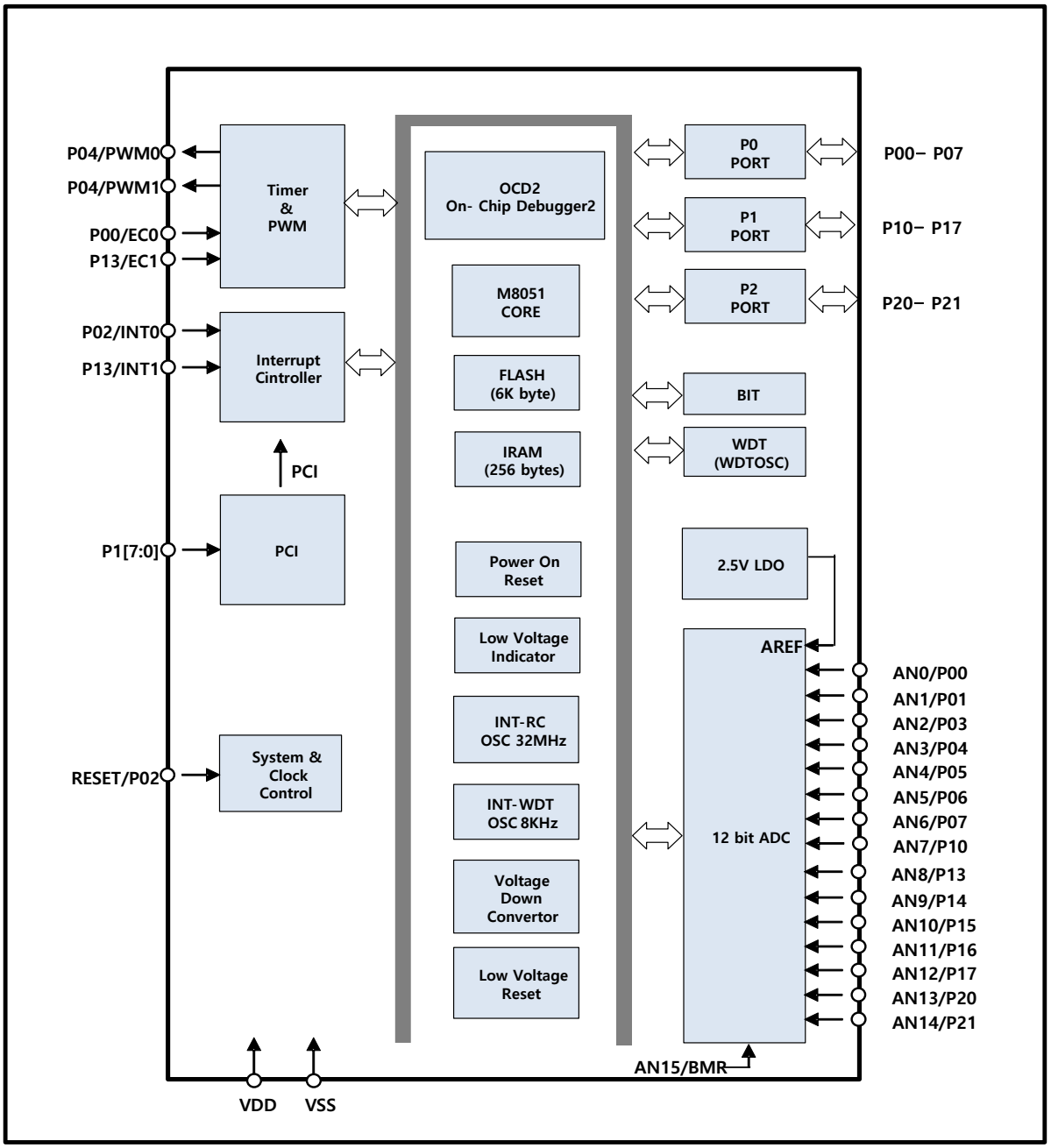


Figure 2.1 Block diagram of MC96F1206

3 Pin assignment

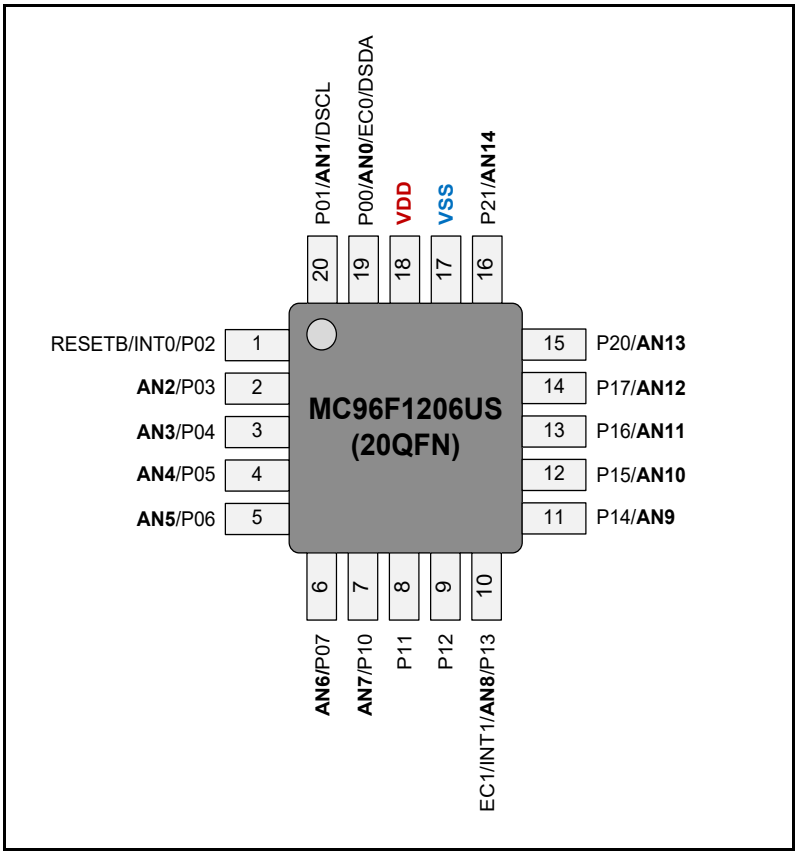


Figure 3.1 MC96F1206 20QFN assignment

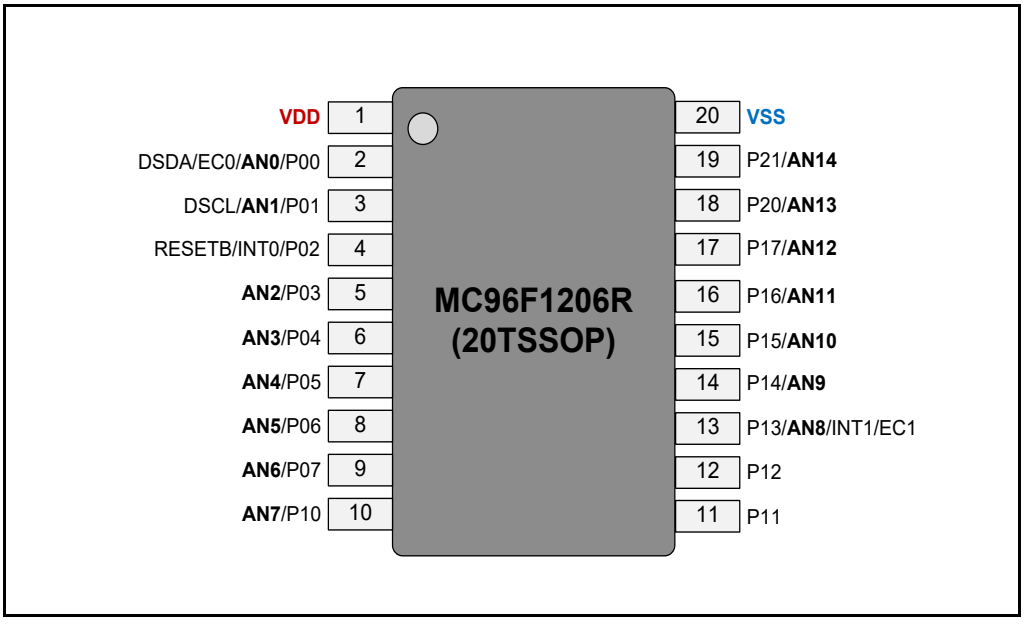


Figure 3.2 MC96F1206 20TSSOP assignment

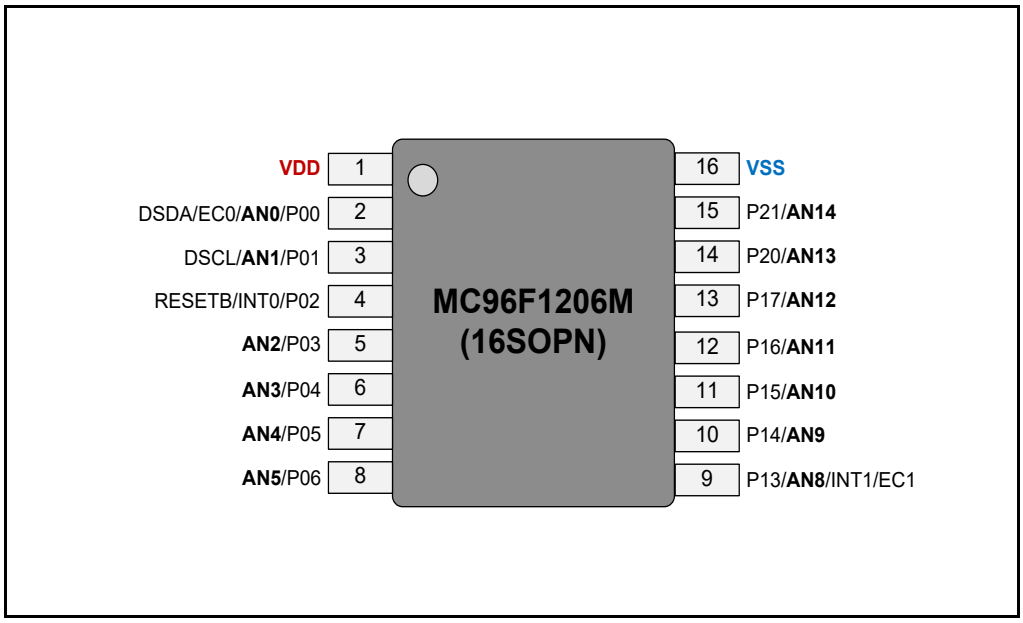


Figure 3.3 MC96F1206 16SOPN assignment

NOTE)

1. The P07, P10-P12 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16SOPN package is used.

4 Package Diagram

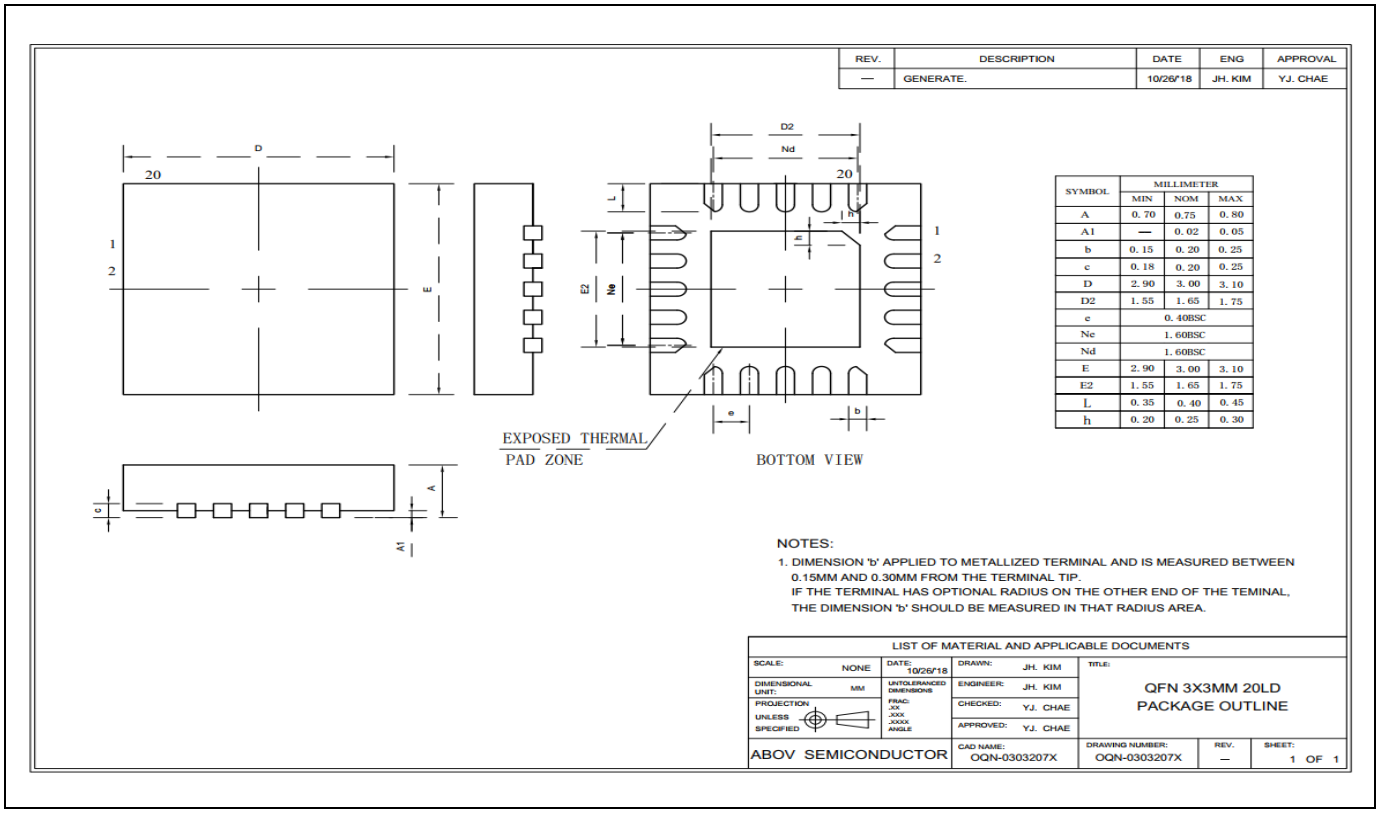


Figure 4.1 20 QFN Package

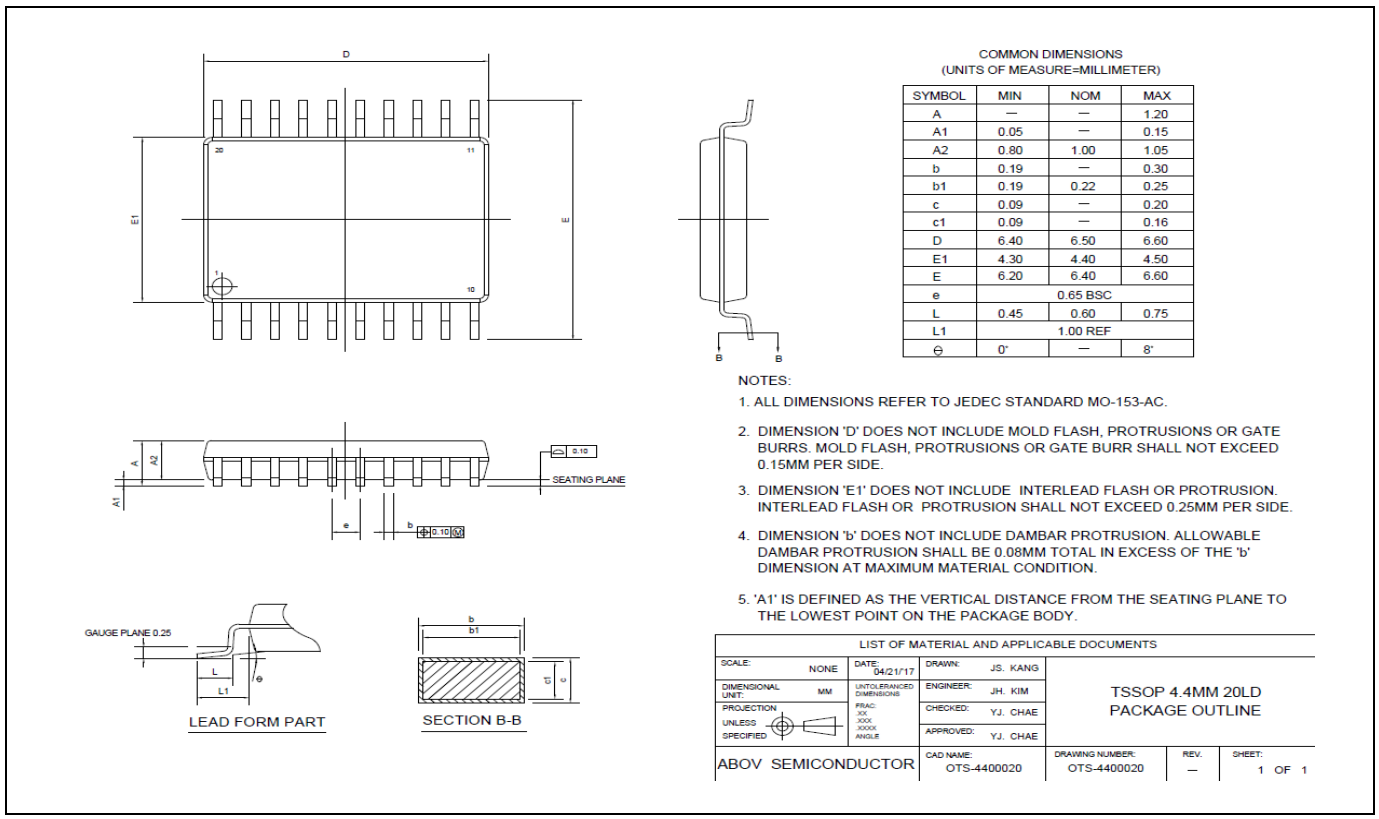
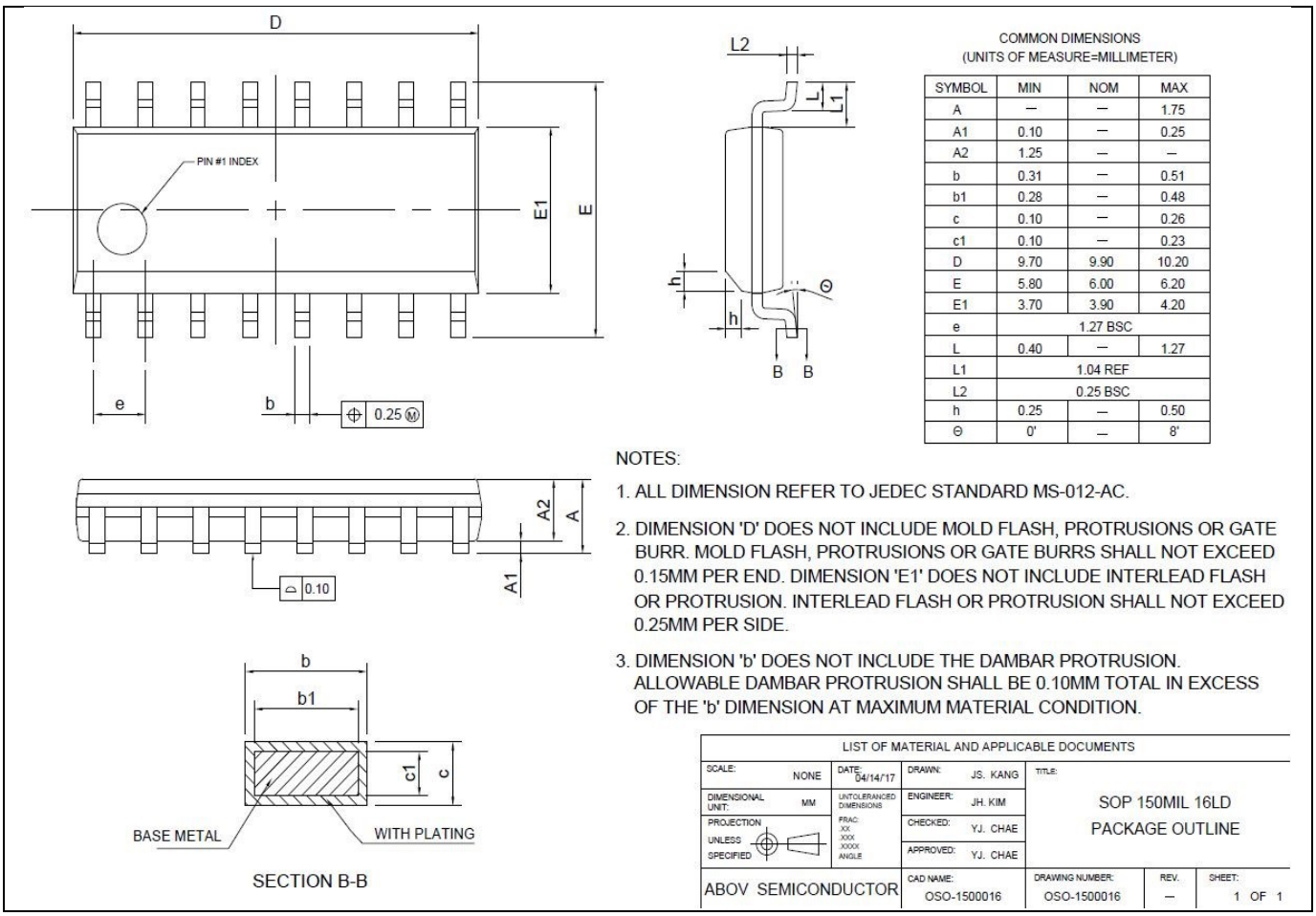


Figure 4.2 20 TSSOP Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
b1	0.28	—	0.48
c	0.10	—	0.26
c1	0.10	—	0.23
D	9.70	9.90	10.20
E	5.80	6.00	6.20
E1	3.70	3.90	4.20
e		1.27 BSC	
L	0.40	—	1.27
L1		1.04 REF	
L2		0.25 BSC	
h	0.25	—	0.50
Θ	0°	—	8°

NOTES:

1. ALL DIMENSION REFER TO JEDEC STANDARD MS-012-AC.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURR. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15MM PER END. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. DIMENSION 'b' DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/14/17	DRAWN: JS. KANG	TITLE: SOP 150MIL 16LD PACKAGE OUTLINE		
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS	ENGINEER: JH. KIM			
PROJECTION UNLESS SPECIFIED	FRAC: .XX .XXX .XXXX ANGLE	CHECKED: YJ. CHAE			
		APPROVED: YJ. CHAE			
ABOV SEMICONDUCTOR		CAD NAME: OSO-1500016	DRAWING NUMBER: OSO-1500016	REV. —	SHEET: 1 OF 1

Figure 4.3 16 SOPN Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port P0 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN0/ EC0/ DSDA
P01				AN1/ DSCL
P02				INT0/ RESETB
P03				AN2
P04				AN3/ PWM0/ PWM1
P05				AN4/ PWM0/ PWM1
P06				AN5/ PWM0/ PWM1
P07				AN6/ PWM0/ PWM1
P10	I/O	Port P1 8-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN7
P11				
P12				
P13				AN8/ INT1 / EC1
P14				AN9/ PWM0/ PWM1
P15				AN10/ PWM0/ PWM1
P16				AN11/ PWM0/ PWM1
P17				AN12/ PWM0/ PWM1
P20	I/O	Port P2 2-bit I/O Port Can be set in input or output mode in 1-bit units Internal pull-up register can be selected by software when this port is used as input port Open Drain enable register can be selected by software when this port is used as output port	Input	AN13
P21				AN14
VDD		Power Supply		
VSS		System Ground		

Table 5.1 Pin Description

NOTE) when using ports as PWM0 or PWM1 output port, set corresponding PSRPWM (PWM Port Selection Register. (0xDE)

6 Port Structure

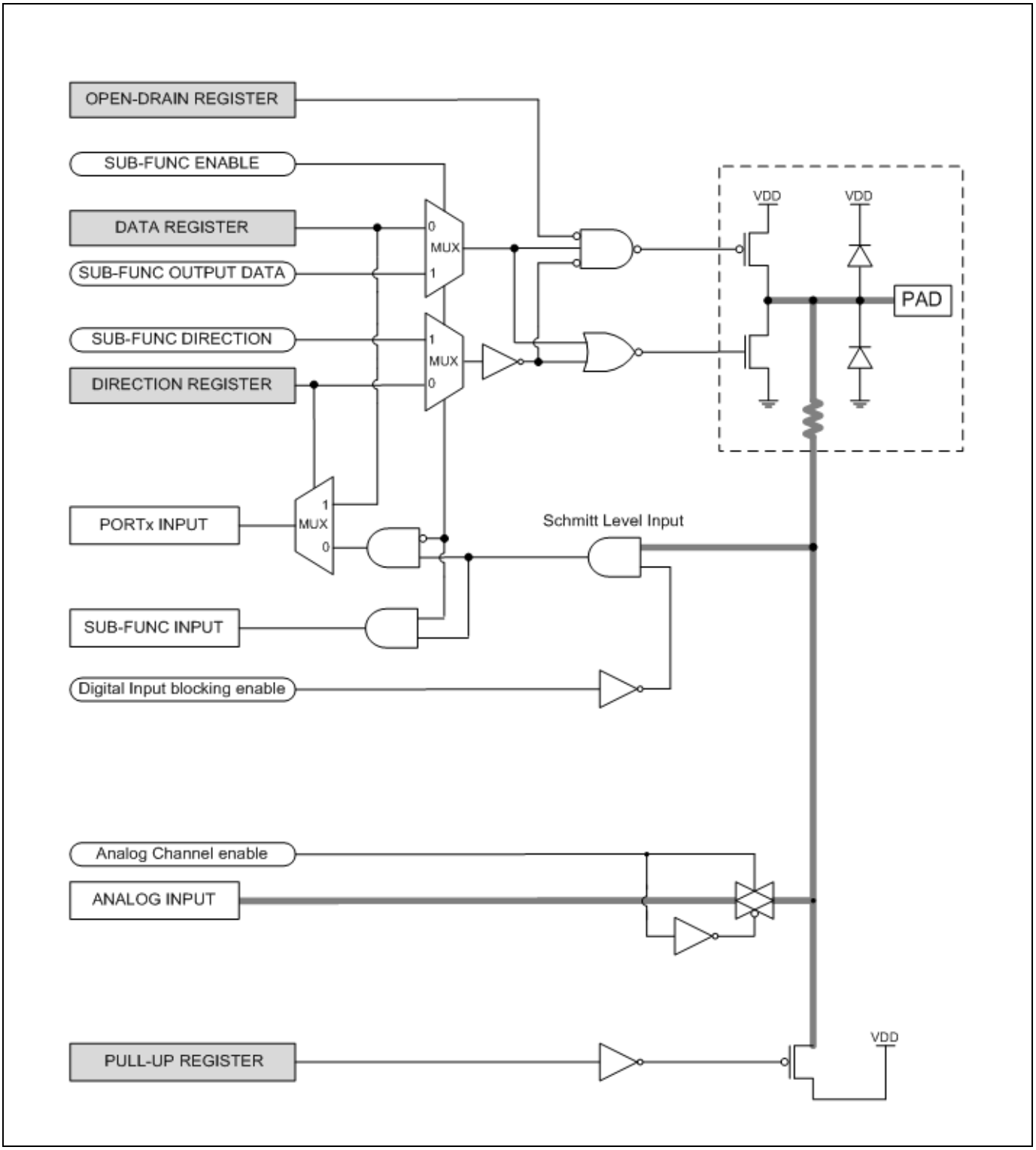


Figure 6.1 Second Function I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3~+6.5	V	–
Normal Voltage Pin	V_I	-0.3~VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3~VDD+0.3	V	
	I_{OH}	-15	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	30	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	160	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	400	mW	–
Storage Temperature	T_{STG}	-65~+150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 1, 4, 8, 16MHz	Internal RC	2.2	–	5.5	V
Operating Temperature	T_{OPR}	VDD=2.2~5.5V		-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(TA=-40℃ ~ +85℃, VDD= 2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–-	12	–	bit
Integral Non-Linearity	INL	Analog Reference Voltage = 2.5V ~ 5.5V fx= 8MHz		–	–	±4	LSB
Differential Non-Linearity	DNL			–	–	±1	
Zero Offset Error	ZOE			-3	–	+7	
Full Scale Error	FSE			–	–	±3	
Conversion Time	t_{CON}			–	60	–	Cycle
Analog Input Voltage	V_{AIN}	–		VSS	–	VDD	V
Analog Reference Voltage	VDDREF	NOTE		2.2	–	VDD	V
	LDOREF	–		-	2.5	-	
Analog Input Leakage Current	I_{AIN}	VDDREF=5.12V		–	–	2	uA
ADC Operating Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE) When Analog Reference Voltage is lower than 2.5V, the ADC resolution is worse.
ADC zero offset value (-3LSB ~ 7 LSB) is addressed at 0x1868 of option memory. (@ LDOREF)

7.4 Low Drop Out Characteristics

(T_A=-40°C ~ +85°C, VDD=2.7 ~ 5.5V, VSS=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Operating Current	I_{DD}	-	-	-	200	uA
Load Current	I_{LOAD}	-	-	1	-	mA
LDO Output Voltage	V_{LDO}	-40°C ~ 85°C	2.450	2.5	2.550	V
		25°C	2.475	2.5	2.525	V

Table 7.4 Low Drop Out Characteristics

7.5 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2 ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	0.9	1.1	1.3	V
VDD Voltage Rising Time	t_R	0V to 2.0V	0.05	–	5	V/ms
POR Current	I_{POR}	–	–	0.1	–	uA

Table 7.5 Power-On Reset Characteristics

7.6 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=5.0V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.80V		–	1.80	1.95	V
				1.6	2.1	2.6	
				2.0	2.5	3.0	
				3.0	3.5	4.0	
Hysteresis	△V	–		–	50	-	mV
Minimum Pulse Width	t_{LW}	–		-	500	–	us
LVR and LVI Current	I_{BL}	LVR 1.80V	VDD=5V	–	1	-	uA
		LVR/LVI except 1.80V		–	-	50	

Table 7.6 LVR and LVI Characteristics

NOTE) LVR 1.80V is always ON.

7.7 Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{IRC}	V_{DD} = 2.2 ~ 5.5V		–	32	–	MHz
Tolerance	–	T_A = 25°C	With 0.1uF Bypass capacitor	–	–	±2.0	%
		T_A = -40°C to +85°C		–	–	±5.0	
Stabilization Time	T_{HFS}	–		–	1	-	ms
IRC Current	I_{IRC}	Enable		–	0.4	–	mA
		Disable		–	–	0.1	uA

Table 7.7 Internal RC Oscillator Characteristics

NOTE) A 0.1uF bypass capacitor should be connected to VDD and VSS.

7.8 Internal WDT Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	4	8	12	kHz
Stabilization Time	t_{WDTS}	–	–	1	-	ms
WDTRC Current	I_{WDTRC}	Enable	–	5	–	uA
		Disable	–	–	0.1	

Table 7.8 Internal WDT Oscillator Characteristics

7.9 DC Characteristics

(T_A=-40°C ~ +85°C, VDD=2.2V ~ 5.5V, VSS=0V, f_X=8.0MHz)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage	V_{IH1}	P0, P1, P2	0.8VDD	–	VDD	V
Input Low Voltage	V_{IL1}	P0, P1, P2	–	–	0.2VDD	V
Output High Voltage	V_{OH1}	VDD=3.3V, I_{OH}=-5mA, All output ports	VDD-1.5	–	–	V
	V_{OH2}	VDD=5V, I_{OH}=-10mA, All output ports	VDD-1.5	–	–	V
Output Low Voltage	V_{OL}	I_{OL}= 20mA,All output ports	–	–	1.0	V
Input High Leakage Current	I_{IH}	All input ports	-1	–	1	uA
Input Low Leakage Current	I_{IL}	All input ports	-1	–	1	uA
Pull-Up Resistor	R_{PU1}	V_I=0V, T_A= 25°C All Input ports	25	50	100	kΩ
Supply Current	I_{DD1} (RUN)	Run Mode, f_X=8 MHz	-	3	5	mA
	I_{IDD2} (IDLE)	IDLE Mode, f_X=8 MHz	-	2	5	mA
	I_{DD3} (STOP1)	STOP1 Mode, WDTRC Enable	-	2	35	uA
	I_{DD4} (STOP2)	STOP2 Mode, WDTRC Disable	-	1.5	30	uA

Table 7.9 DC Characteristics

NOTE) STOP1: WDT only running, STOP2: All function disable.

7.10 AC Characteristics

(T_A= -40°C ~ +85°C, VDD=2.2V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	Input, VDD=5V	-	500	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD=5V	125	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	ECn, VDD=5V (n=0, 1)	125	–	–	ns
External Counter Transition Time	t_{REC}, t_{FEC}	ECn, VDD=5V (n=0, 1)	-	–	20	ns

Table 7.10 AC Characteristics

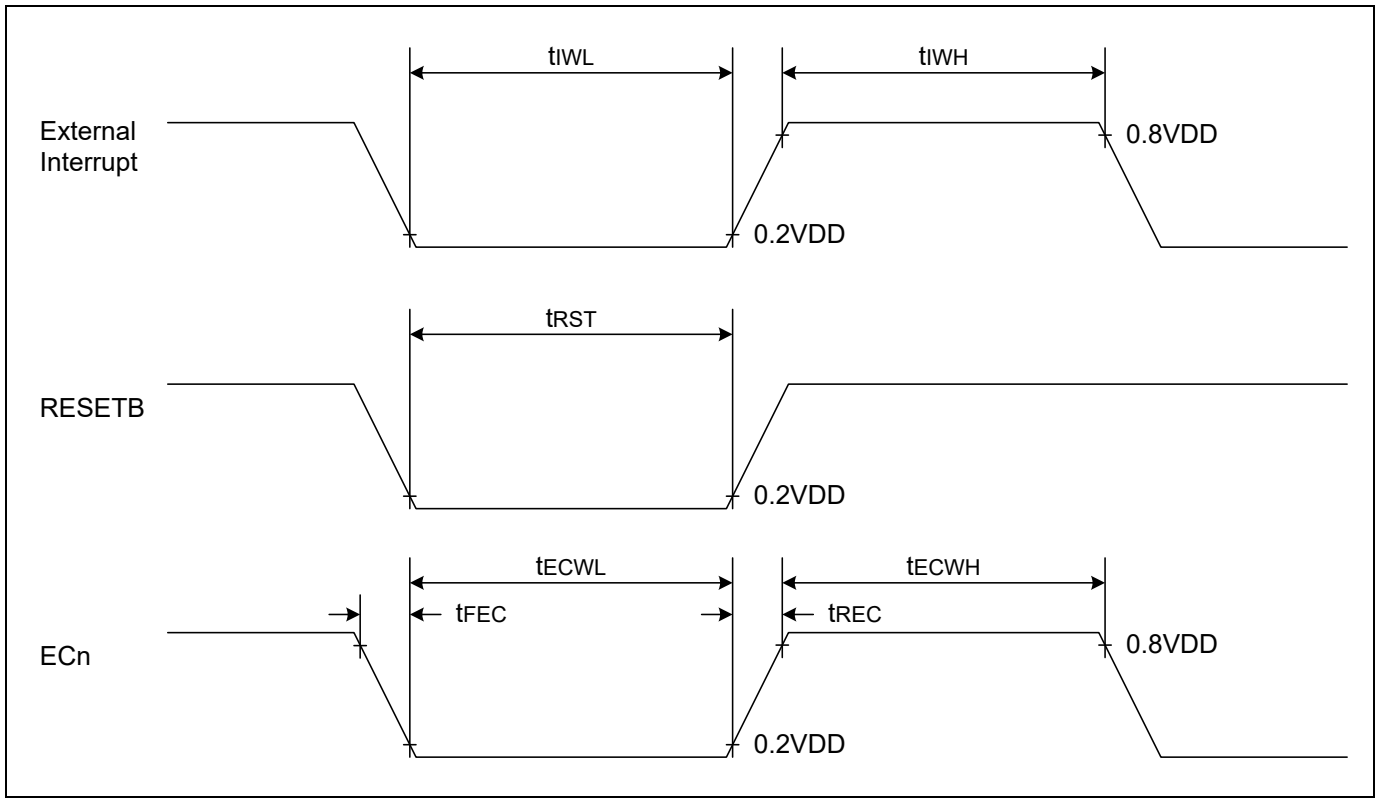


Figure 7.1 AC Timing

7.11 Operating Voltage Range

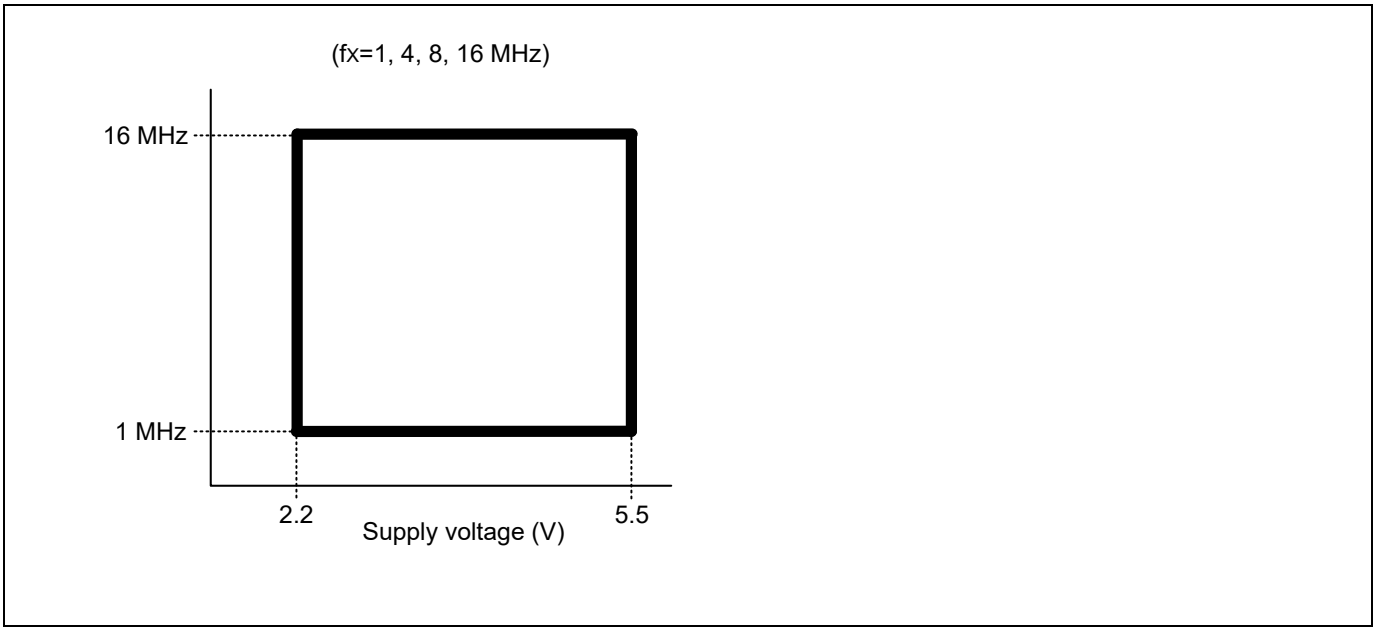


Figure 7.2 Operating Voltage Range

7.12 Typical Characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

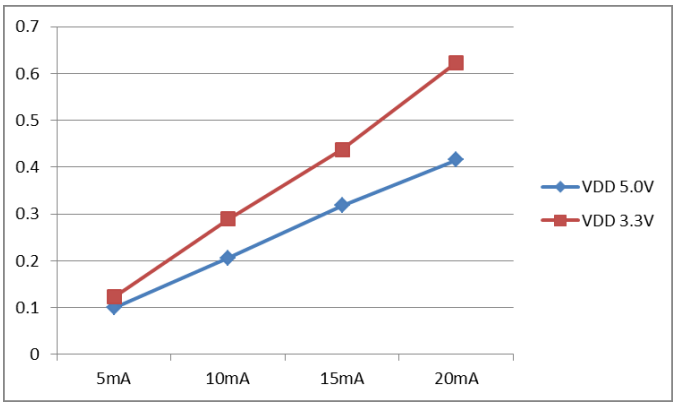


Figure 7.3 Output Low Voltage (V_{OL})

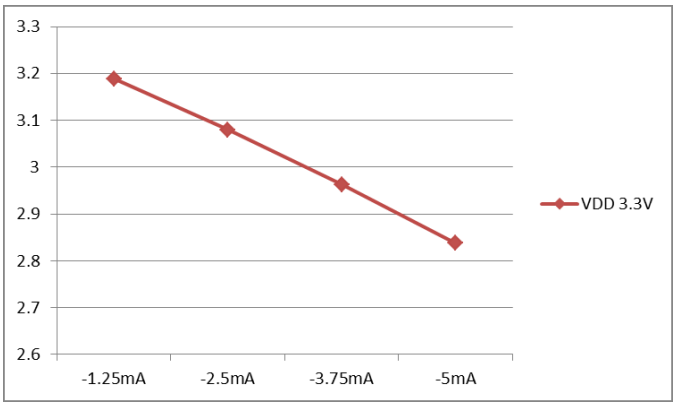


Figure 7.4 Output High Voltage (V_{OH1})

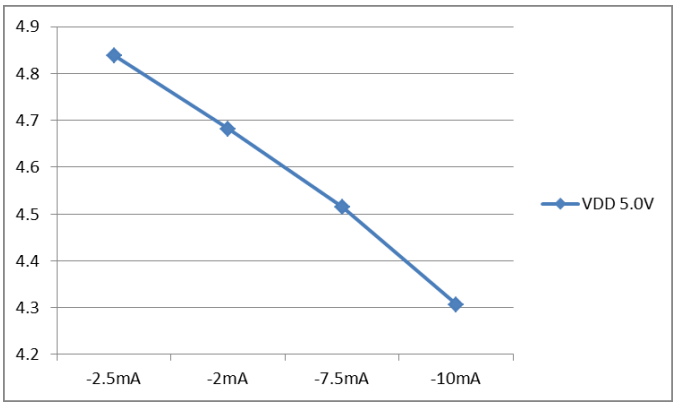


Figure 7.5 Output High Voltage (V_{OH2})

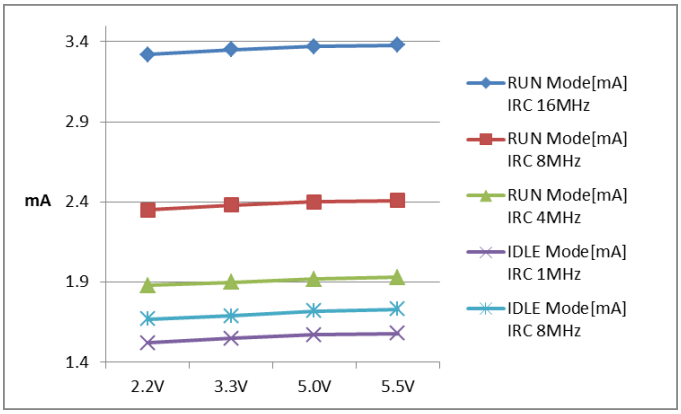


Figure 7.6 Power Supply Current (RUN, IDLE)

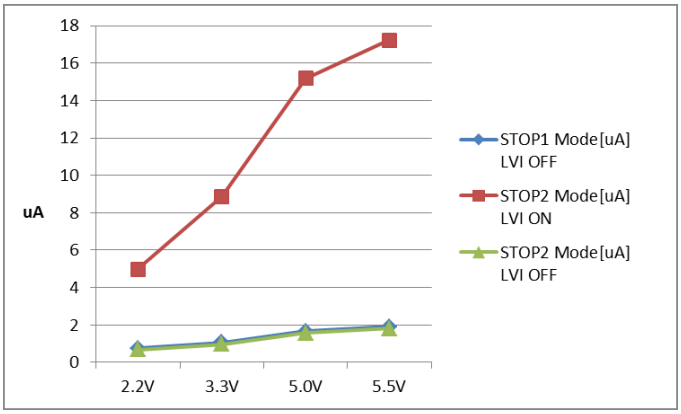


Figure 7.7 Power Supply Current (STOP1, STOP2)

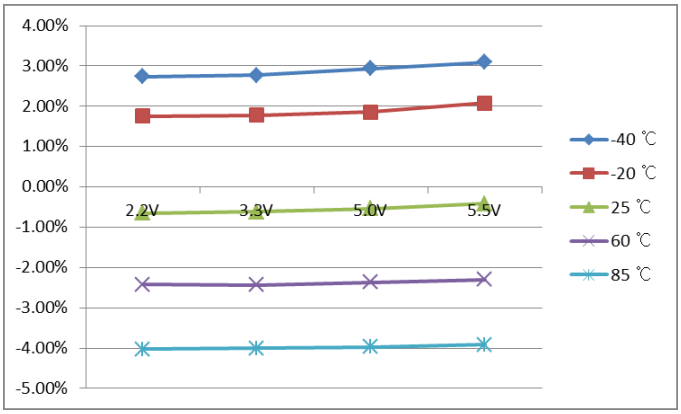


Figure 7.8 IRC Tolerance

7.13 Recommended Application Circuit

For the microprocessor and other devices in the system to function correctly, it is also necessary to monitor the supply voltage during operations. Voltage drops or glitches on the power supply lines, can cause unwanted changes in the internal registers, which can lead to instructions being incorrectly executed, incorrect output signals and errors in the operations results. If noise is applied to the VDD rising slope due to external factors during the POR, the microprocessor may malfunction because the microprocessor continues to operate and does not recognize that the voltage has fallen below the threshold due to the internal RC time constants. Therefore, VDD / GND requires a power capacitor for VDD drop and a decoupling capacitor for high frequency noise. Normally, electrolytic / tantalum capacitors of 10uf / 9V or more are recommended for power capacitors and multilayer ceramic capacitors of 0.1uF or more are recommended for decoupling capacitors. Decoupling capacitors should be placed as close as possible to the microprocessor.

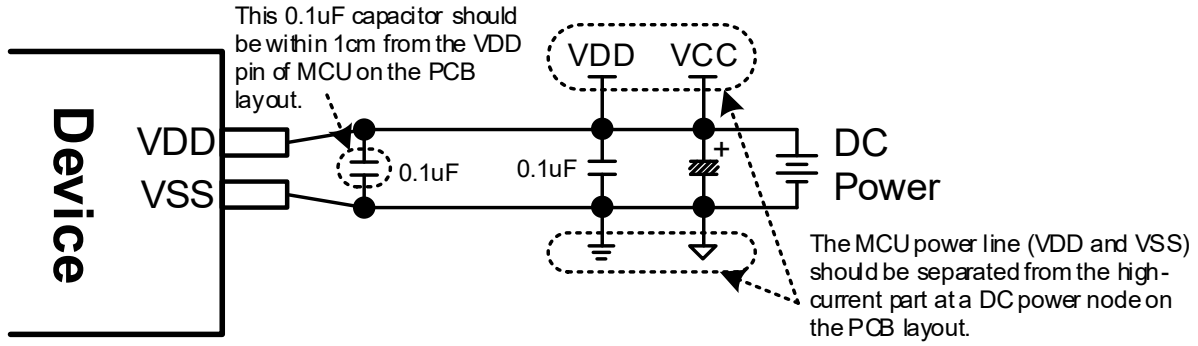


Figure 7.9 Recommended Power Circuit part when using DC Power.

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