STM32L552xx

Ultra-low-power Arm® Cortex®-M33 32-bit MCU+TrustZone®+FPU, 165 DMIPS, up to 512 KB Flash memory, 256 KB SRAM, SMPS

Data brief

Features

Ultra-low-power with FlexPowerControl

- 1.71 V to 3.6 V power supply
- -40 °C to 85/125 °C temperature range
- Batch acquisition mode (BAM)
- 225 nA in VBAT mode: supply for RTC and 32x32-bit backup registers
- 33 nA Shutdown mode (5 wakeup pins)
- 110 nA Standby mode (5 wakeup pins)
- 385 nA Standby mode with RTC
- 3.6 µA Stop 2 with RTC
- 96 µA/MHz Run mode (LDO mode)
- 60 µA/MHz Run mode @ 3 V (SMPS step down converter mode)
- 5 µs wakeup from Stop mode
- Brownout reset (BOR) in all modes except shutdown

Core

- Arm® 32-bit Cortex®-M33 CPU with TrustZone® and FPU

ART Accelerator™

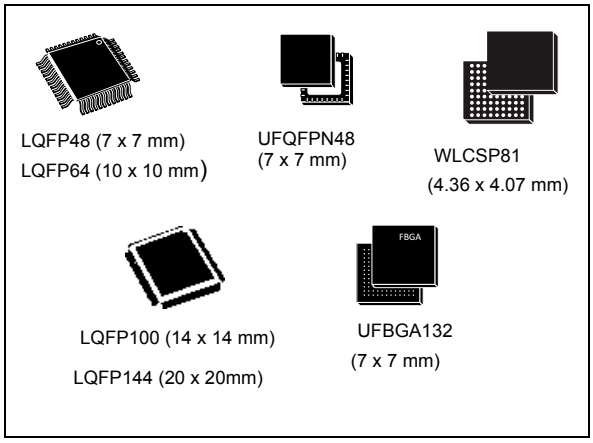
- 8 Kbytes instruction cache allowing 0-wait-state execution from Flash memory and external memories; frequency up to 110 MHz, MPU, 165 DMIPS and DSP instructions

Performance benckmark

- 1.5 DMIPS/MHz (Drystone 2.1)
- 442 Coremark® (4.02 Coremark®/MHz @ 110 MHz

Energy benchmark

- 402 ULPMark-CP® score
- 59.5 ULPMark-PP® score



- 27400 SecureMark-TLS® score

Memories

- Up to 512 Kbytes Flash, two banks read-while-write
- 256 Kbytes of SRAM including 64 Kbytes with hardware parity check
- External memory interface supporting SRAM, PSRAM, NOR, NAND and FRAM memories
- OCTOSPI memory interface

General-purpose input/outputs

- Up to 114 fast I/Os with interrupt capability most 5 V-tolerant and up to 14 I/Os with independent supply down to 1.08 V

Security

- Arm® TrustZone® with the ARMv8-M mainline security extension
- Up to 8 configurable SAU regions
- RDP, active tamper, secure firmware upgrade support, secure hide protection
- TrustZone aware and securable peripherals

Power management

- Embedded regulator (LDO) with three configurable range output to supply the digital circuitry
- SMPS step down converter
- External SMPS support

Clock management

- 4 to 48 MHz crystal oscillator
- 32 kHz crystal oscillator for RTC (LSE)
- Internal 16 MHz factory-trimmed RC (±1%)
- Internal low-power 32 kHz RC (±5%)
- Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (better than ±0.25% accuracy)
- Internal 48 MHz with clock recovery
- 3 PLLs for system clock, USB, audio, ADC

Up to 16 timers and 2 watchdogs

- 16x timers: 2 x 16-bit advanced motor-control, 2 x 32-bit and 5 x 16-bit general purpose, 2x 16-bit basic, 3x low-power 16-bit timers (available in Stop mode), 2x watchdogs, 2x SysTick timer
- RTC with HW calendar, alarms and calibration

Up to 19 communication peripherals

- 1x USB Type-C™/ USB power delivery controller
- 1x USB 2.0 full-speed crystal less solution, LPM and BCD
- 2x SAIs (serial audio interface)
- 4x I2C FM+(1 Mbit/s), SMBus/PMBus
- 6x USARTs (ISO 7816, LIN, IrDA, modem)
- 3x SPIs (7x SPIs with USART and OCTOSPI in SPI mode)
- 1x FDCAN controller
- 1x SDMMC interface

2 DMA controller

- 14 DMA channels

Up to 22 capacitive sensing channels:

- Support touch key, linear and rotary touch sensors

Rich analog peripherals (independent supply)

- 2x 12-bit ADC 5 Msps, up to 16-bit with hardware oversampling, 200 µA/Msps
- 2x 12-bit DAC, low-power sample and hold
- 2x operational amplifiers with built-in PGA
- 2x ultra-low-power comparators
- 4x digital filters for sigma delta modulator

True random number generator

CRC calculation unit

HASH (SHA-256) hardware accelerator

Debug

- Development support: serial wire debug (SWD), JTAG, Embedded Trace Macrocell (ETM)

96-bit unique ID

Table 1. Device summary

Reference	Part numbers
STM32L552xx	STM32L552CC, STM32L552CE, STM32L552ME, STM32L552QC, STM32L552QE, STM32L552RC, STM32L552RE, STM32L552VC, STM32L552VE, STM32L552ZC, STM32L552ZE

Contents

List of tables

List of figures

1 Introduction

This document provides the ordering information and mechanical device characteristics of the STM32L552xx microcontrollers.

This document should be read in conjunction with the STM32L552xx and STM32L562xx reference manual (RM0438).

For information on the Arm®(a) Cortex®-M33 core, please refer to the Cortex®-M33 Technical Reference Manual, available from the www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

The STM32L552xx devices are an ultra-low-power microcontrollers family (STM32L5 Series) based on the high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 110 MHz.

The Cortex-M33 core features a single-precision floating-point unit (FPU), which supports all the Arm® single-precision data-processing instructions and all the data types. The Cortex-M33 core also implements a full set of DSP (digital signal processing) instructions, TrustZone aware support and a memory protection unit (MPU) which enhances the application's security.

These devices embed high-speed memories (512 Kbytes of Flash memory and 256 Kbytes of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), an OctoSPI Flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L552xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, secure and hide protection areas.

These devices offer two fast 12-bit ADC (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM). In addition, up to 22 capacitive sensing channels are available.

They also feature standard and advanced communication interfaces such as:

- Four I2Cs
- Three SPIs
- Three USARTs, two UARTs and one low-power UART
- Two SAIs
- One SDMMC
- One FDCAN
- USB device FS
- USB Type-C / USB power delivery controller
- HASH (SHA-256) hardware accelerator

The devices operate in the -40 to +85 °C (+105 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported like an analog independent supply input for ADC, DAC, OPAMPs and comparators, a 3.3 V dedicated supply input for USB and up to 14 I/Os, which can be supplied independently down to 1.08 V. A VBAT input allows to backup the RTC and backup the registers.

The STM32L552xx devices offer seven packages from 48-pin to 144-pin.

Table 2. STM32L552xx features and peripheral counts

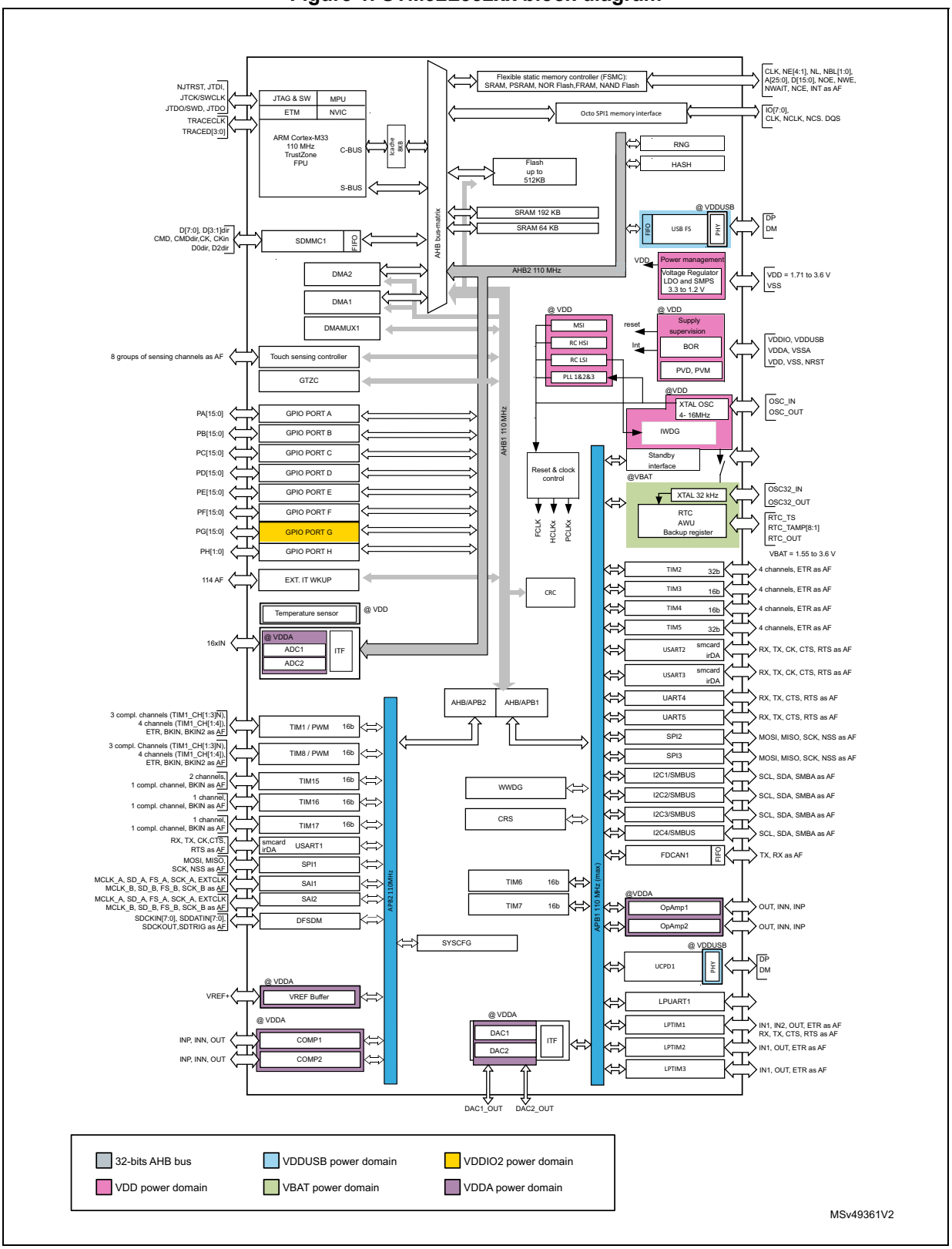
Peripherals		STM32L552CE, STM32L552CC/ STM32L552CExxP	STM32L552RE, STM32L552RC/ STM32L552RExxP/ STM32L552RExxQ	STM32L552MExxP/ STM32L552MExxQ	STM32L552VE/ STM32L552VExxQ, STM32L552VCxxQ	STM32L552QExxP/ STM32L552QExxQ, STM32L552QCxxQ	STM32L552ZE/ STM32L552ZExxQ, STM32L552ZCxxQ
Flash memory (Kbyte)		512/256					
SRAM	System (Kbyte)	256 (192+64)					
	Backup (byte)	128					
External memory controller for static memories (FSMC)		No			Yes		
OctoSPI		1					
Timers	Advancedcontrol	2 (16-bit)					
	General purpose	5 (16-bit) 2 (32-bit)					
	Basic	2 (16-bit)					
	Low power	3 (16-bit)					
	SysTick timer	1					
	Watchdog timers (independent, window)	2					
Communication interfaces	SPI	3					
	I2C	4					
	USART(1)/UART UART LPUART	3/2 (2) 2 1					
	SAI	2					
	FDCAN	1					
	USB FS	Yes					
	SDMMC	No	Yes/No/Yes	Yes			
Digital filters for sigma-delta modulators		Yes (4 filters)					
Number of channels		8					
Real time clock (RTC)		Yes					
Tamper pins		3	4/4/3	3	5/4	5	8/7
True random number generator		Yes					
HASH (SHA-256)		Yes					

Table 2. STM32L552xx features and peripheral counts (continued)

Peripherals		STM32L552CE, STM32L552CC/ STM32L552CExxP	STM32L552RE, STM32L552RC/ STM32L552RExxP/ STM32L552RExxQ	STM32L552MExxP/ STM32L552MExxQ	STM32L552VE/ STM32L552VExxQ, STM32L552VCxxQ	STM32L552QExxP/ STM32L552QExxQ, STM32L552QCxxQ	STM32L552ZE/ STM32L552ZExxQ, STM32L552ZCxxQ
GPIOs Wakeup pins Nb of I/Os down to 1.08 V		38/36 3 0	52/50/47 4/3/3 0	54/51 3 6	83/79 5/4 0	108/105 5 13/10	115 /111 5/4 14/13
Capacitive sensing Number of channels		5	10/10/9	10	19/18	22	22/21
ADC	12-bit ADC	2					
	Number of channels	9	16/16/15	16/15	16/14	16	16/14
DAC	12-bit DAC	2					
	Number of channels	2					
Internal voltage reference buffer		Yes					
Analog comparator		2					
Operational amplifiers		2					
Max. CPU frequency		110 MHz					
Operating voltage		1.71 to 3.6 V					
Operating temperature		Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C					
Package		LQFP48, UFQFN48	LQFP64	WLCSP81	LQFP100 (2)	UFBGA132	LQFP144

1. USART3 is not available on STM32L552CExxP devices.
2. For the LQFP100 package, only FSMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.

Figure 1. STM32L552xx block diagram



Note: AF: alternate function on I/O pins.

3 Functional overview

3.1 Arm® Cortex®-M33 core with TrustZone® and FPU

The Cortex-M33 with TrustZone and FPU is a highly energy efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. it features:

- Arm® TrustZone® technology, using the ARMv8-M main extension supporting secure and non-secure states
- Memory protection units (MPUs), supporting up to 16 regions for secure and non-secure applications
- Configurable secure attribute unit (SAU) supporting up to 8 memory regions as secure or non-secure
- Floating-point arithmetic functionality with support for single precision arithmetic

The processor supports a set of DSP instructions that allows an efficient signal processing and a complex algorithm execution.

The Cortex-M33 processor supports the following bus interfaces:

- System AHB bus:
  The System AHB (S-AHB) bus interface is used for any instruction fetch and data access to the memory-mapped SRAM, peripheral, external RAM and external device, or Vendor_SYS regions of the ARMv8-M memory map.
- Code AHB bus
  The Code AHB (C-AHB) bus interface is used for any instruction fetch and data access to the code region of the ARMv8-M memory map.

Figure 1 shows the general block diagram of the STM32L552xx family devices.

3.2 ART Accelerator™ (ICACHE)

The instruction cache (ICACHE) is introduced on C-AHB code bus of Cortex®-M33 processor to improve performance when fetching instruction (or data) from both internal and external memories.

ICACHE offers the following features:

- Multi-bus interface:
  - slave port receiving the memory requests from the Cortex®-M33 C-AHB code execution port
  - master1 port performing refill requests to internal memories (FLASH and SRAMs)
  - master2 port performing refill requests to external memories (external FLASH/RAMs through OctoSPI/FMC interfaces)
  - a second slave port dedicated to ICACHE registers access.
- Close to zero wait states instructions/data access performance:
  - 0 wait-state on cache hit
  - hit-under-miss capability, allowing to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - critical-word-first refill policy, minimizing processor stalls on cache miss
  - hit ratio improved by 2-ways set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - dual master ports allowing to decouple internal and external memory traffics, on Fast and Slow buses, respectively; also minimizing impact on interrupt latency
  - optimal cache line refill thanks to AHB burst transactions (of the cache line size).
  - performance monitoring by means of a hit counter and a miss counter.
- Extension of cacheable region beyond Code memory space, by means of address remapping logic that allows to define up to 4 cacheable external regions
- Power consumption reduced intrinsically (most accesses to cache memory rather to bigger main memories); even improved by configuring ICACHE as direct mapped (rather than the default 2-ways set-associative mode)
- TrustZone® security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to the memory and to prevent one task to accidentally corrupt the memory or the resources used by any other active task. This memory area is organized into up to 16 protected areas. The MPU regions and registers are banked across secure and non-secure states.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices feature 512 Kbytes of embedded Flash memory which is available for storing programs and data.

The Flash interface features:

- Single or dual bank operating modes
- Read-while-write (RWW) in dual bank mode

This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 128 pages of 2 or 4 Kbytes (depending on the read access width).

Flexible protections can be configured thanks to the option bytes:

- Readout protection (RDP) to protect the whole memory. Four levels of protection are available:
  - Level 0: no readout protection
  - Level 0.5: available only when TrustZone is enabled
    All read/write operations (if no write protection is set) from/to the non-secure Flash memory are possible. The Debug access to secure area is prohibited. Debug access to non-secure area remains possible.
  - Level 1: memory readout protection; the Flash memory cannot be read from or written to if either the debug features are connected or the boot in RAM or bootloader are selected. If TrustZone is enabled, the non-secure debug is possible and the boot in SRAM is not possible.
  - Level 2: chip readout protection; the debug features (Cortex-M33 JTAG and serial wire), the boot in RAM and the bootloader selection are disabled (JTAG fuse). This selection is irreversible.
- Write protection (WRP): the protected area is protected against erasing and programming:
  - In single bank mode, four areas can be selected with 4-Kbyte granularity.
  - In dual bank mode, two areas per bank can be selected with 2-Kbyte granularity.

The whole non-volatile memory embeds the error correction code (ECC) feature supporting:

- Single error detection and correction
- Double error detection
- The address of the ECC fail can be read in the ECC register.

TrustZone security

When the TrustZone security is enabled, the whole Flash is secure after reset and the following protections are available:

- Non-volatile watermark-based secure Flash area: the secure area can be accessed only in secure mode.
  - In single bank mode, four areas can be selected with a page granularity.
  - In dual bank mode, one area per bank can be selected with a page granularity.
- Secure hide protection area: it is part of the Flash secure area and it can be protected to deny an access to this area by any data read, write and instruction fetch. For

example, a software code in the secure Flash hide protection area can be executed only once and deny any further access to this area until next system reset.

- Volatile block-based secure Flash area. In a block-based secure area, each page can be programmed on-the-fly as secure or non-secure.

3.5 Embedded SRAM

The devices feature 256 Kbytes of embedded SRAM. This SRAM is split into three blocks:

- 192 Kbytes mapped at address 0x2000 0000 (SRAM1).
- 64 Kbytes located at address 0x0A03 0000 with hardware parity check (SRAM2). This memory is also mapped at address 0x2003 0000 offering a contiguous address space with the SRAM1.
  This block is accessed through the C-bus for maximum performance. Either 64 Kbytes or upper 4 Kbytes of SRAM2 can be retained in Standby mode.
  The SRAM2 can be write-protected with 1 Kbyte granularity.

The memory can be accessed in read/write at CPU clock speed with 0 wait states.

TrustZone security

When the TrustZone security is enabled, all SRAMs are secure after reset. The SRAM can be programmed as non-secure by block based using the MPCBB (memory protection controller block based) in GTZC controller. The granularity of SRAM secure block based is a page of 256 bytes.

3.6 Boot modes

At startup, a BOOT0 pin, nBOOT0 and NSBOOTADDx [24:0] / SECBOOTADD0 [24:0] option bytes are used to select the boot memory address which includes:

- Boot from any address in user Flash
- Boot from system memory bootloader
- Boot from any address in embedded SRAM
- Boot from Root Security service (RSS)

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, FDCAN or USB FS in device mode through the DFU (device firmware upgrade).

Refer to *Table 3* and *Table 4* for boot modes when TrustZone is disabled and enabled respectively.

Table 3. Boot modes when TrustZone is disabled (TZEN=0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0 [24:0]	Boot address defined by user option bytes NSBOOTADD0 [24:0]	Flash: 0x0800 0000
-	1	1	NSBOOTADD1 [24:0]	Boot address defined by user option bytes NSBOOTADD1 [24:0]	System bootloader: 0x0BF9 0000
1	-	0	NSBOOTADD0 [24:0]	Boot address defined by user option bytes NSBOOTADD0 [24:0]	Flash: 0x0800 0000
0	-	0	NSBOOTADD1 [24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

When TrustZone is enabled by setting the TZEN option bit, the boot space must be in secure area. The SECBOOTADD0 [24:0] option bytes are used to select the boot secure memory address.

A unique boot entry option can be selected by setting the BOOT_LOCK option bit, allowing to boot always at the address selected by SECBOOTADD0 [24:0] option bytes. All other boot options are ignored.

Table 4. Boot modes when TrustZone is enabled (TZEN=1)

BOOT_LOCK	nBOOT0 FLASH_OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR[26]	RSS command	Boot address option-bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0 [24:0]	Flash: 0x0C00 0000
	-	1	1	0	N/A	RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
	1	-	0	0	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0 [24:0]	Flash: 0x0C00 0000
	0	-	0	0	N/A	RSS: RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
	-	-	-	≠ 0	N/A	RSS: RSS: 0x0FF8 0000	RSS: 0x0FF8 0000
1	-	-	-	-	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0 [24:0]	Flash: 0x0C00 0000

The boot address option bytes enables the possibility to program any boot memory address. However, the allowed address space depends on Flash read protection RDP level.

If the programmed boot memory address is out of the allowed memory mapped area when RDP level is 0.5 or more, the default boot fetch address is forced either in secure Flash or non-secure Flash depending on TrustZone security option as described in *Table 5*.

Table 5. Boot space versus RDP protection

RDP	TZEN = 1	TZEN = 0
0	Any boot address	Any boot address
0.5	Boot address only in: – RSS – or secure Flash: 0x0C00 0000 - 0x0C07 FFFF Otherwise boot address forced is: 0x0C00 0000	N/A
1		Any boot address
2		Boot address only in Flash 0x0800 0000 - 0x0807 FFFF Otherwise boot address forced is: 0x0800 0000

3.7 Global TrustZone controller (GTZC)

The GTZC includes three different sub-blocks:

- **TZSC**: TrustZone® security controller
  This sub-block defines the secure/privilege state of slave/master peripherals. It also controls the non-secure area size for the watermark memory peripheral controller (MPCWM). The TZSC block informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.

1. **MPCBB**: block-based memory protection controller
   This sub-block controls secure states of all blocks (256-byte pages) of the associated SRAM.
2. **TZIC**: TrustZone illegal access controller
   This sub-block gathers all illegal access events in the system and generates a secure interrupt towards NVIC.

These sub-blocks are used to configure TrustZone and privileged attributes within the full system.

The GTZC main features are:

- 3 independent 32-bit AHB interface for TZSC, MPCBB and TZIC
- MPCBB and TZIC accessible only with secure transactions
- Secure and non-secure access supported for priv/non-priv part of TZSC
- Register set to define security settings:
  - Secure blocks for internal SRAM
  - Non-secure regions for external memories
  - Secure/privilege access mode for securable and TZ-aware peripherals
- Secure/privilege access mode for securable legacy masters.

3.8 TrustZone security architecture

The security architecture is based on Arm® TrustZone® with the ARMv8-M Main Extension.

The TrustZone security is activated by the TZEN option bit in the FLASH_OPTR register.

When the TrustZone is enabled, the SAU (security attribution unit) and IDAU (implementation defined attribution unit) defines the access permissions based on secure and non-secure state.

- SAU: Up to 8 SAU configurable regions are available for security attribution.
- IDAU: It provides a first memory partition as non-secure or non-secure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on IDAU security attribution, the Flash, system SRAMs and peripherals memory space is aliased twice for secure and non-secure state. However, the external memories space is not aliased.

Table 6 shows an example of typical SAU regions configuration based on IDAU regions. The user can split and choose the secure, non-secure or NSC regions for external memories as needed.

Table 6. Example of memory map security attribution vs SAU configuration regions(1) (2)

Region description	Address range	IDAU security attribution	SAU security attribution typical configuration	Final security attribution
Code - external memories	0x0000_0000 0x07FF_FFFF	Non-secure	Secure or non-secure or NSC	Secure or non-secure or NSC
Code - Flash and SRAM	0x0800_0000 0x0BFF_FFFF	Non-secure	Non-secure	Non-secure
	0x0C00_0000 0x0FFF_FFFF	NSC	Secure or NSC	Secure or NSC
Code - external memories	0x1000_0000 0x17FF_FFFF	Non-secure	Non-secure	
	0x1800_0000 0x1FFF_FFFF			
SRAM	0x2000_0000 0x2FFF_FFFFF	Non-secure		
	0x3000_0000 0x3FFF_FFFFF	NSC	Secure or NSC	Secure or NSC
Peripherals	0x4000_0000 0x4FFF_FFFFF	Non-secure	Non-secure	Non-secure
	0x5000_0000 0x5FFF_FFFFF	NSC	Secure or NSC	Secure or NSC
External memories	0x6000_0000 0xDFFF_FFFF	Non-secure	Secure or non-secure or NSC	Secure or non-secure or NSC

1. NSC = non-secure callable.
2. Different colors highlights the different configurations
   Pink: Non-secure
   Green: NSC (non-secure callable)
   Lighter green: Secure or non-secure or NSC

3.8.1 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either Securable or TrustZone-aware type as follows:

- Securable: a peripheral is protected by an AHB/APB firewall gate that is controlled from TZSC controller to define security properties.
- TrustZone-aware: a peripheral connected directly to AHB or APB bus and is implementing a specific TrustZone behavior such as a subset of registers being secure.

The tables below summarize the list of Securable and TrustZone aware peripherals within the system.

Table 7. Securable peripherals by TZSC

Bus	Peripheral
AHB3	OCTOSPI1 registers
	FMC registers
AHB 2	SDMMC1
	RNG
	ADC
AHB1	ICACHE registers
	TSC
	CRC
APB2	DFSDM1
	SAI2
	SAI1
	TIM17
	TIM16
	TIM15
	USART1
	TIM8
	SPI1
	TIM1
	COMP
	VREFBUF

Table 7. Securable peripherals by TZSC (continued)

Bus	Peripheral
APB1	UCPD1
	USB FS
	FDCAN1
	LPTIM3
	LPTIM2
	I2C4
	LPUART1
	LPTIM1
	OPAMP
	DAC1/DAC2
	CRS
	I2C3
	I2C2
	I2C1
	UART5
	UART4
	USART3
	USART2
	SPI3
	SPI2
	IWDG
	WWDG
	TIM7
	TIM6
	TIM5
	TIM4
	TIM3
	TIM2

Table 8. TrustZone-aware peripherals

Bus	Peripheral
AHB2	GPIOH
	GPIOG
	GPIOF
	GPIOE
	GPIOD
	GPIOC
	GPIOB
	GPIOA
AHB1	MPCBB2
	MPCBB1
	MPCWM2
	MPCWM1
	TZIC
	TZSC
	EXTI
	Flash memory
	RCC
	DMAMUX1
	DMA2
	DMA1
APB2	SYSCFG
APB1	PWR
	RTC

Default TrustZone security state

The default system security state is:

- CPU:
  - Cortex-M33 is in secure state after reset. The boot address must be in secure address.
- Memory map:
  - SAU: is fully secure after reset. Consequently, all memory map is fully secure. Up to 8 SAU configurable regions are available for security attribution.
- Flash:
  - Flash security area is defined by watermark user options.
  - Flash block based area is non-secure after reset.
- SRAMs:
  - All SRAMs are secure after reset. MPCBB (memory protection block based controller) is secure.
- External memories:
  - FSMC, OctoSPI banks are secure after reset. MPCWMx (memory protection watermark based controller) are secure
- Peripherals
  - Securable peripherals are non-secure after reset.
  - TrustZone-aware peripherals (except the GPIO) are non-secure after reset. Their secure configuration registers are secure.

Note: Refer to Table 7 and Table 8 for a list of Securable and TrustZone-aware peripherals.

- All GPIO are secure after reset.
- Interrupts:
  - NVIC: All interrupts are secure after reset. NVIC is banked for secure and non-secure state.
  - TZIC: All illegal access interrupts are disabled after reset.

3.9 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domains (VCORE)
  - VDD domain
  - Backup domain (VBAT)
  - Analog domain (VDDA)
  - VDDIO2 domain
  - VDDUB for USB transceiver
- System supply voltage regulation
  - SMPS step down converter
  - Voltage regulator (LDO)
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - PVD monitor
  - PVM monitor (VDDA, VDDUSB, VDDIO2)
  - Temperature thresholds monitor
  - Upper VDD voltage threshold monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- VBAT battery charging
- TrustZone security

3.9.1 Power supply schemes

The devices require a 1.71 V to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V

  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins.
- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) to 2.4 V (VREFBUF) to 3.6 V

  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage and should preferably be connected to V_{DD} when these peripherals are not used.

- VDDSMPS = 1.71 V to 3.6 V
  VDDSMPS is the external power supply for the SMPS step down converter. It is provided externally through VDDSMPS supply pin, and shall be connected to the same supply as VDD.
- VLXSMPS is the switched SMPS step down converter output.
- V15SMPS are the power supply for the system regulator. It is provided externally through the SMPS step down converter VLXSMPS output.

Note: The SMPS power supply pins are available only on a specific package with SMPS step down converter option.

- VDD12 = 1.05 to 1.32 V
  VDD12 is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. VDD12 does not require any external decoupling capacitance and cannot support any external load.
- VDDUSB = 3.0 V to 3.6 V
  VDDUSB is the external independent power supply for USB transceivers. The VDDUSB voltage level is independent from the VDD voltage and should preferably be connected to VDD when the USB is not used.
- VDDIO2 = 1.08 V to 3.6 V
- VDDIO2 is the external power supply for 14 I/Os (port G[15:2]). The VDDIO2 voltage level is independent from the VDD voltage and should preferably be connected to VDD when PG[15:2] are not used.
- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREFBUF_CSR register:

  – V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.
  – V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively.
  When the VREF+ is double-bonded with VDDA in a package, the internal voltage reference buffer is not available and must be kept disabled (refer to datasheet for packages pinout description).
  V_{REF-} must always be equal to V_{SSA}.

An embedded linear voltage-regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals, SRAM1 and SRAM2. The Flash is supplied by V_{CORE} and V_{DD}.

Figure 2. STM32L552xx power supply overview

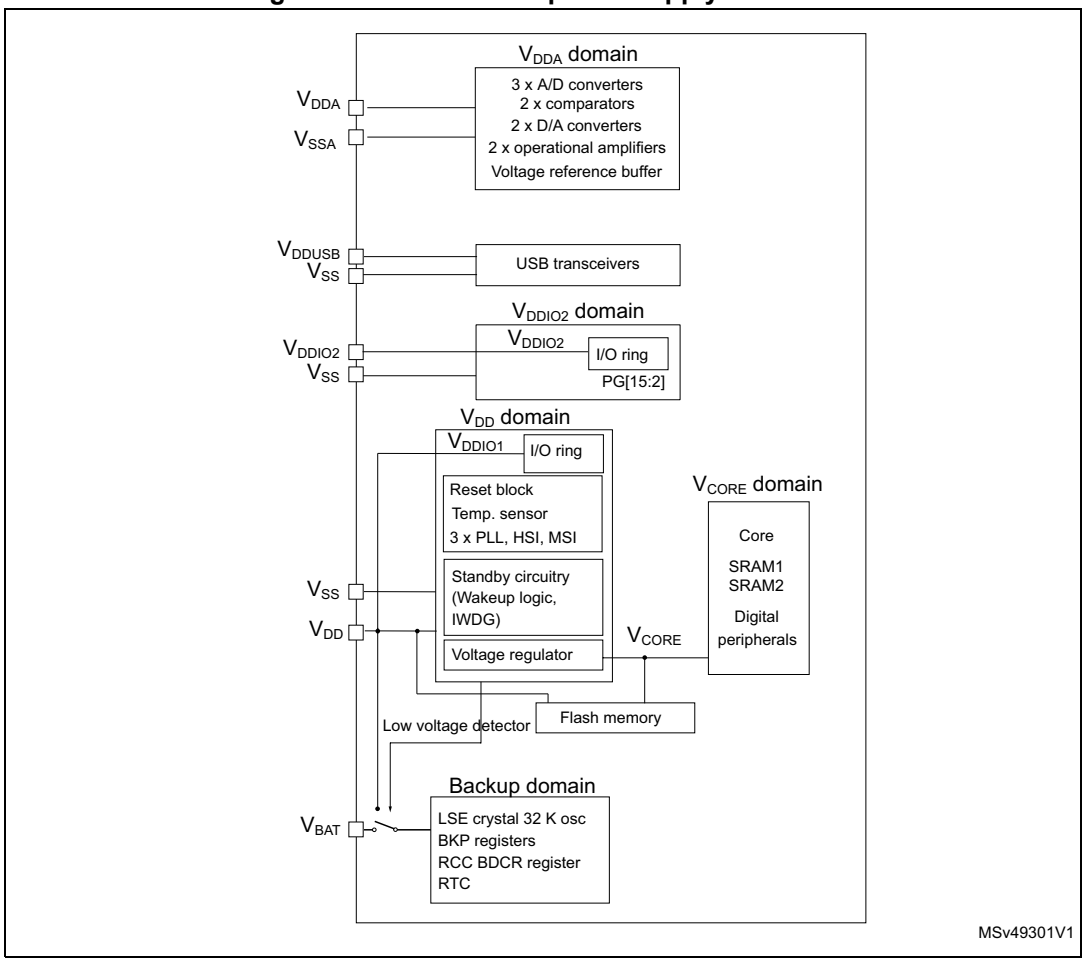


Figure 3. STM32L552xxxxP power supply overview

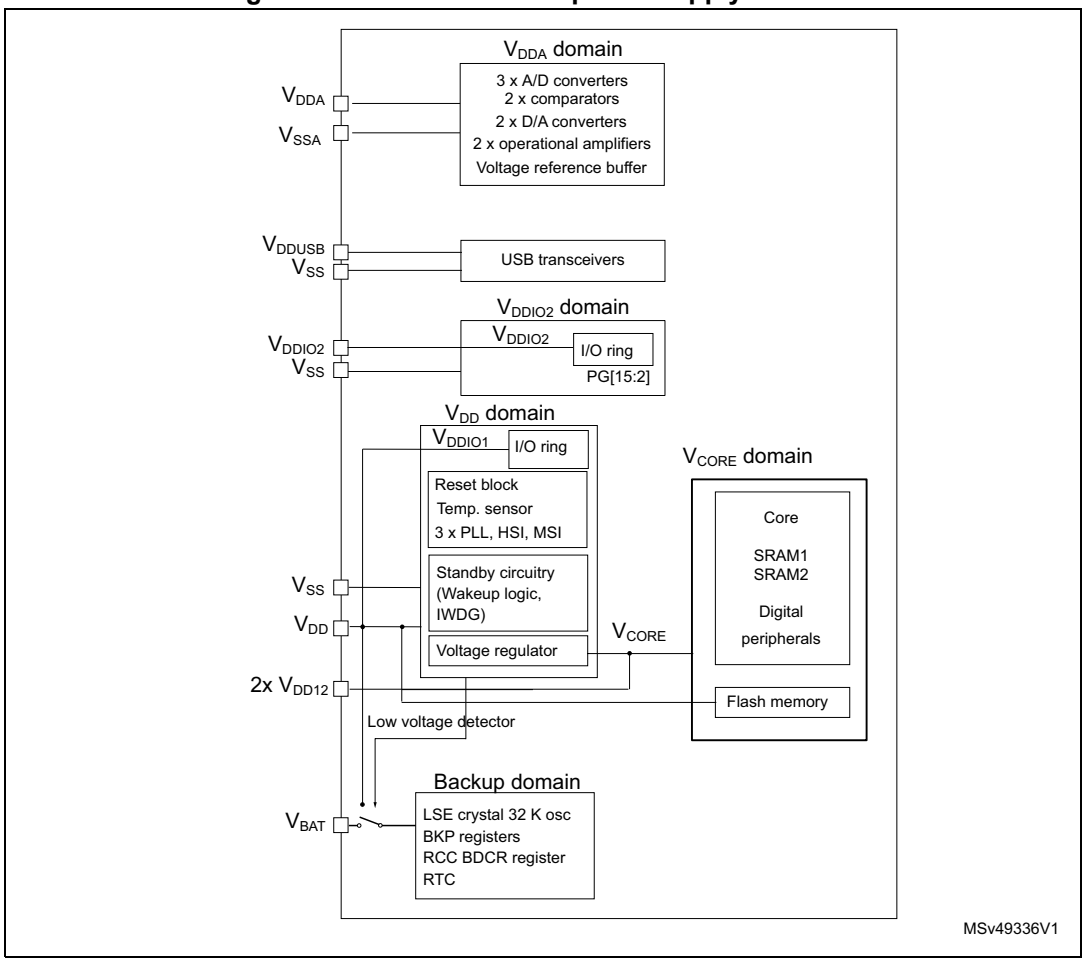
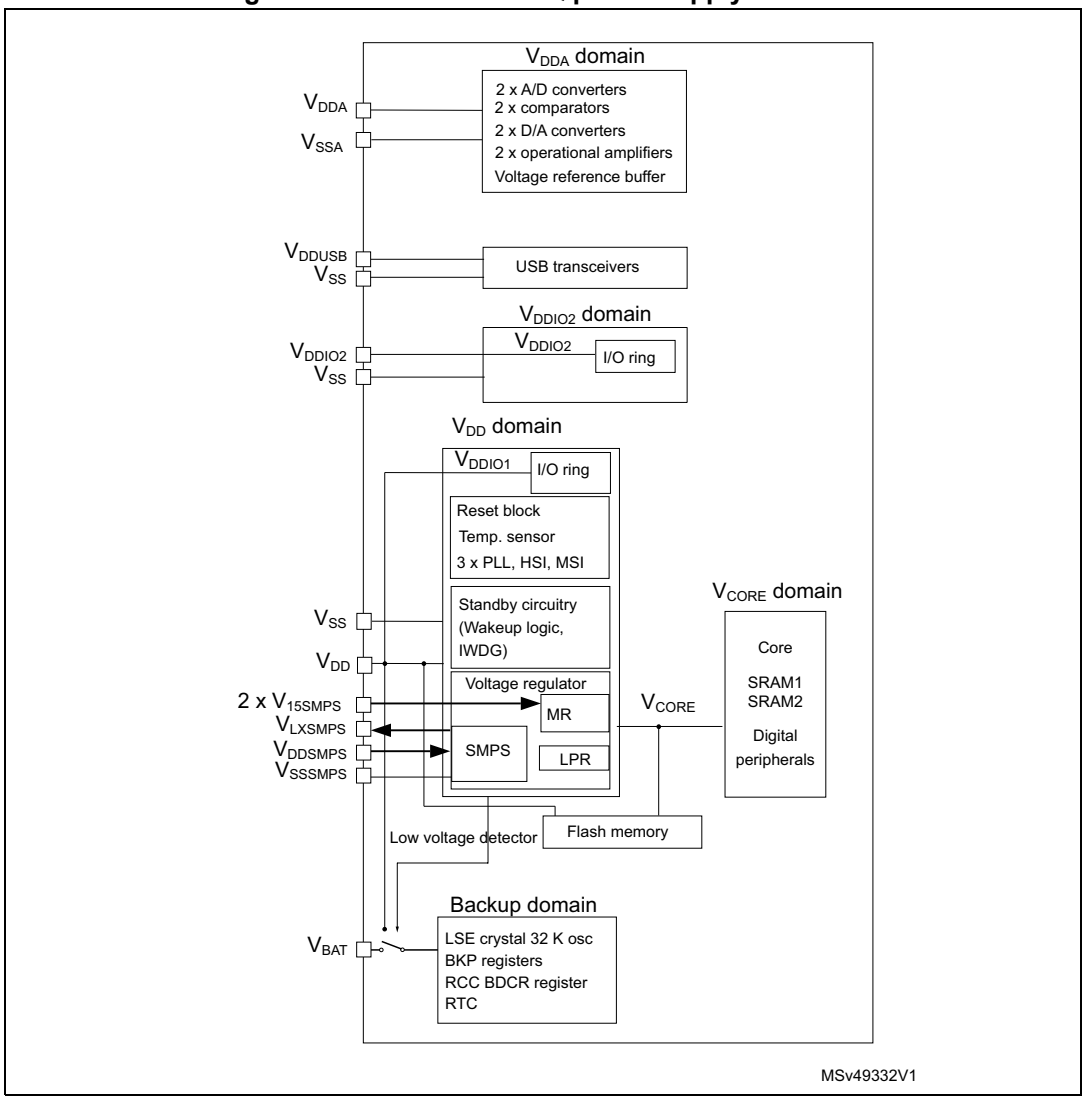


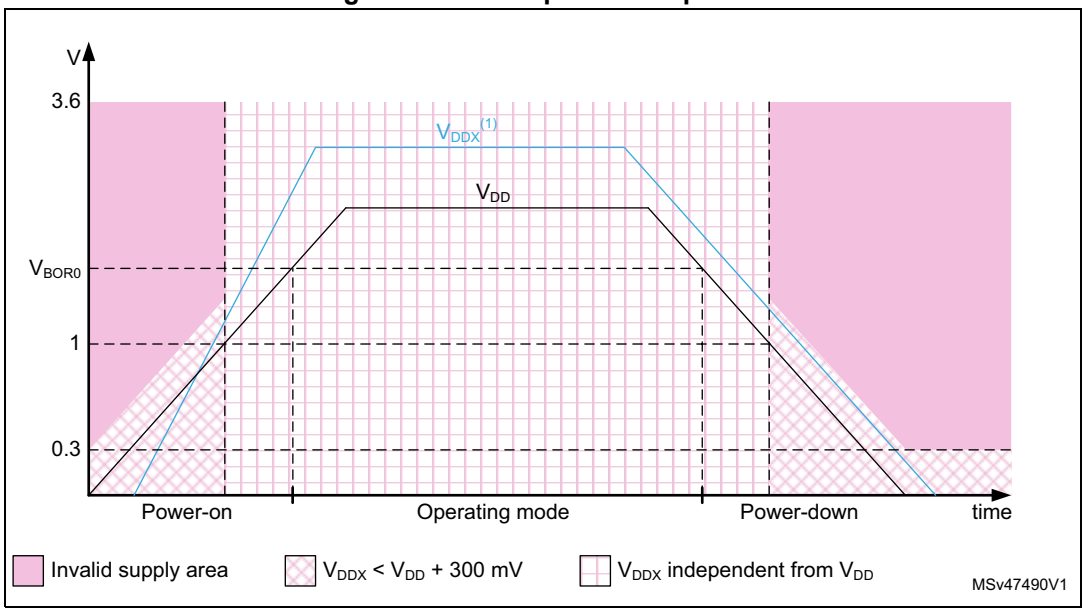
Figure 4. STM32L552xxxxQ power supply overview



During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2} and V_{DDUSB}) must remain below VDD +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 5. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2} and V_{DDUSB}.

3.9.2 Power supply supervisor

The devices have an integrated ultra-low-power Brownout reset (BOR) active in all modes (except for Shutdown mode). The BOR ensures proper operation of the devices after power-on and during power down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold.

An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a peripheral voltage monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.9.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-power run, Low-power sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbytes or only 4 Kbytes of SRAM2 in standby with SRAM2 retention.
- Both regulators are in power-down while they are in standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultra-low-power STM32L552xx devices support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the main regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 0 with the CPU running at up to 110 MHz.
- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by the HSI16.

3.9.4 SMPS step down converter

The built-in SMPS step down converter is a highly power-efficient DC/DC non-linear switching regulator that improves low-power performance when the VDD voltage is high enough. This SMPS step down converter automatically enters in bypass mode when the VDD voltage falls below 2 V in Range 0 and Range 1.

Note: There is no automatic SMPS bypass in Range 2.

The SMPS step down converter can be configured in:

- High-power mode (HPM): achieving a high efficiency at high current load. It is the default selected mode after POR reset.
- Low power mode achieving very high efficiency at low load
- Bypass mode

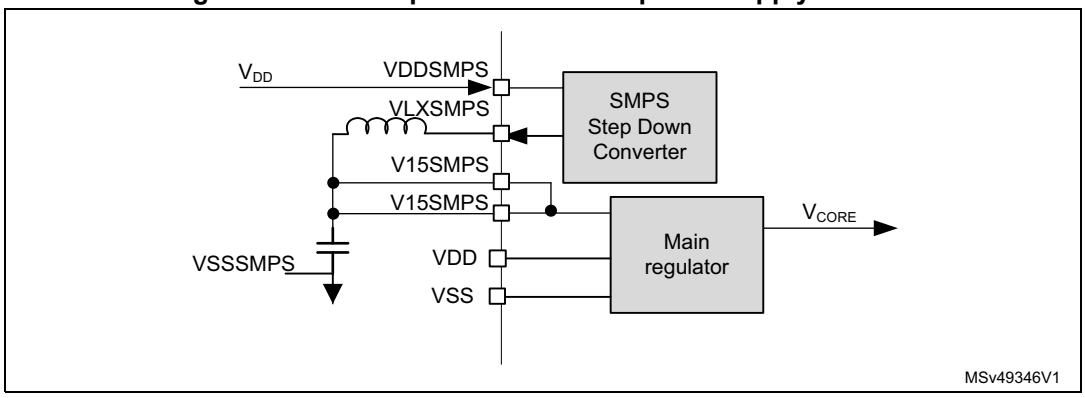
The SMPS step down converter can be switched in bypass mode at any time by the application software.

Note: The SMPS step down converter is available only on specific package.

SMPS step down converter power supply scheme

The SMPS step down converter requires an external coil with typical value of 4.7 µH to be connected between the dedicated V_{LXSMPS} pin to V_{SSSMPS} via a capacitor of 4.7µF. It can be switched OFF by selecting the Bypass mode by software. Thus, only main regulator is used by the application.

Figure 6. SMPS step down converter power supply scheme



If the selected package is with the SMPS step down converter option but it is never used by the application, it is recommend to set the SMPS power supply pins as follows:

- V_{DDSMPS} and V_{LXSMPS} connected to VSS
- V_{15SMPS} connected to VDD

SMPS step down converter fast startup

After POR reset, the SMPS step down converter starts in High-power mode and in Low startup mode. The low-startup feature is selected to limit the inrush current after power-on reset.

However, it is possible to configure a faster startup on the fly and it is applied for next startup either after a system reset or wakeup from low-power mode except Shutdown and VBAT modes. The fast startup is selected by setting the SMPSFSTEN bit in the PWR_CR4 register.

3.9.5 Low-power modes

The ultra-low-power STM32L552xx devices support seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wake-up sources. *Table 10* shows the related STM32L552xx modes overview.

Table 9. STM32L552xx modes overview

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Run	Range 1	Yes	ON[3]	ON	Any	All	N/A
	Range2					All except USB, UCPD, RNG	
LPRun	LPR	Yes	ON[3]	ON	Any except PLL	All except USB, UCPD, RNG	N/A
Sleep	Range 1	No	ON[3]	ON[4]	Any	All	Any interrupt or event
	Range 2					All except USB, UCPD, RNG	
LPSleep	LPR	No	ON[3]	ON[4]	Any except PLL	All except USB, UCPD, RNG	Any interrupt or event
Stop 0	Range 1	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) USB and UCPD[7]
	Range 2						

Table 9. STM32L552xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[5] LPUART1[5] I2Cx (x=1...4)[6] LPTIMx (x=1,2) OTG_FS[7]
Stop 2	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[6] LPUART1[5] LPTIM1 *** All other peripherals are frozen.	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) I2C3[6] LPUART1[5] LPTIM1
Standby	LPR	Powered Off	Off	64 KB or 4 KB of SRAM2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)[8] BOR, RTC, IWDG
	OFF			Powered Off			
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down[9]	Reset pin 5 I/Os (WKUPx)[8] RTC

1. LPR means that the main regulator is OFF and the low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1 and SRAM2 clocks can be gated on or off independently.
5. U(S)ART and LPUART reception is functional in Stop mode, and generates a wake-up interrupt on start, address match or received frame event.
6. I2C address detection is functional in Stop mode, and generates a wake-up interrupt in case of address match.
7. USB and UCPD wakeup by resume from suspend and attach detection protocol event.
8. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
9. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

By default, the microcontroller is in Run mode after a system or a power reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the Low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the Low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wake-up capability can enable the HSI16 RC during Stop mode to detect their wake-up condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop 1 or Stop 2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The Brownout reset (BOR) always remains active in Standby mode.

  The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, the full SRAM2 or 4 Kbytes can be retained in Standby mode, supplied by the low-power regulator (standby with RAM2 retention mode).

The BORL (brown out detector low) can be configured in ultra-low-power mode to further reduce power consumption during standby mode.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

The system clock after wakeup is MSI up to 8 MHz.

- **Shutdown** mode

  The Shutdown mode allows to achieve the lowest power consumption. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the HSI16, the MSI, the LSI and the HSE oscillators are also switched off.

  The RTC can remain active (Shutdown mode with RTC, Shutdown mode without RTC).

  The BOR is not available in Shutdown mode. No power voltage monitoring is possible in this mode, therefore the switch to Backup domain is not supported.

  SRAM1, SRAM2 and register contents are lost except for registers in the Backup domain.

  The device exits Shutdown mode when an external reset (NRST pin), a WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper).

  The system clock after wakeup is MSI at 4 MHz.

Table 10. Functionalities depending on the working mode(1)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (2 Mbytes)	O(2)	O(2)	O(2)	O(2)	-	-	-	-	-	-	-	-	-
SRAM1 (192 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	O(4)	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
OctoSPI	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable voltage detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral voltage monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system on LSE	O	O	O	O	O	O	O	O	O	O	-	-	-
RTC / Auto-wakeup	O	O	O	O	O	O	O	O	O	O	O	O	O

Table 10. Functionalities depending on the working mode[1] (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Number of RTC Tamper pins	8	8	8	8	8	O	8	O	8	O	8	O	3
USB, UCPD	O[8]	O[8]	-	-	-	O	-	-	-	-	-	-	-
USARTx (x=1,2,3,4,5)	O	O	O	O	O[6]	O[6]	-	-	-	-	-	-	-
Low-power UART (LPUART)	O	O	O	O	O[6]	O[6]	O[6]	O[6]	-	-	-	-	-
I2Cx (x=1,2,4)	O	O	O	O	O[7]	O[7]	-	-	-	-	-	-	-
I2C3	O	O	O	O	O[7]	O[7]	O[7]	O[7]	-	-	-	-	-
SPIx (x=1,2,3)	O	O	O	O	-	-	-	-	-	-	-	-	-
FDCAN1	O	O	O	O	-	-	-	-	-	-	-	-	-
SDMMC1	O	O	O	O	-	-	-	-	-	-	-	-	-
SAIx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DFSDM1	O	O	O	O	-	-	-	-	-	-	-	-	-
ADCx (x=1,2)	O	O	O	O	-	-	-	-	-	-	-	-	-
DACx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
VREFBUF	O	O	O	O	O	-	-	-	-	-	-	-	-
OPAMPx (x=1,2)	O	O	O	O	O	-	-	-	-	-	-	-	-
COMPx (x=1,2)	O	O	O	O	O	O	O	O	-	-	-	-	-
Temperature sensor	O	O	O	O	-	-	-	-	-	-	-	-	-
Timers (TIMx)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low-power timer 1, 3 (LPTIM1 and LPTIM3)	O	O	O	O	O	O	O	O	-	-	-	-	-
Low-power timer 2 (LPTIM2)	O	O	O	O	O	O	-	-	-	-	-	-	-
Independent watchdog (IWDG)	O	O	O	O	O	O	O	O	O	O	-	-	-
Window watchdog (WWDG)	O	O	O	O	-	-	-	-	-	-	-	-	-
SysTick timer	O	O	O	O	-	-	-	-	-	-	-	-	-
Touch sensing controller (TSC)	O	O	O	O	-	-	-	-	-	-	-	-	-

Table 10. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
Random number generator (RNG)	O(8)	O(8)	-	-	-	-	-	-	-	-	-	-	-
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = yes (enable). O = optional (disable by default, can be enabled by software). - = not available.

Gray cells highlight the wakeup capability in each mode.

2. The Flash can be configured in Power-down mode. By default, it is not in Power-down mode.
3. The SRAM clock can be gated on or off.
4. 4 Kbytes or full SRAM2 content is preserved depending on RRS[1:0] bits configuration in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from standby/shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.6 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.7 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.9.8 PWR TrustZone security

When the TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone security allows to secure the following configuration:

- Low-power mode
- Wake-up (WKUP) pins
- Voltage detection and monitoring
- VBAT mode

Other PWR configuration bits are secure when:

- The system clock selection is secure in RCC, the voltage scaling (VOS) configuration is secure
- A GPIO is configured as secure, it's corresponding bit for Pull-up/Pull-down in standby mode is secure
- The RTC is secure, the backup domain write protection bit in PWR is secure.

3.10 Peripheral interconnect matrix

Several peripherals have direct connections between them, which allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, Low-power run and Sleep, Stop 0, Stop 1 and Stop 2 modes. See *Table 11* for more details.

Table 11. STM32L552xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC DACx DFSDM1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-

Table 11. STM32L552xx peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-
USB	TIM2	Timer triggered by USB SOF	Y	Y	-	-	-	-
CSS CPU (hard fault) RAM (parity error) Flash memory (ECC error) COMPx PVD DFSDM1 (analog watchdog, short circuit detection)	TIM1,8 TIM15,16,17	Timer break	Y	Y	Y	Y	-	-
GPIO	TIMx	External trigger	Y	Y	Y	Y	-	-
	LPTIMERx	External trigger	Y	Y	Y	Y	Y	Y (1)
	ADC DACx DFSDM1	Conversion external trigger	Y	Y	Y	Y	-	-

1. LPTIM1 and LPTIM3 only.

3.11 Reset and clock controller (RCC)

The clock controller (see *Figure 7*) distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures the clock robustness. It features:

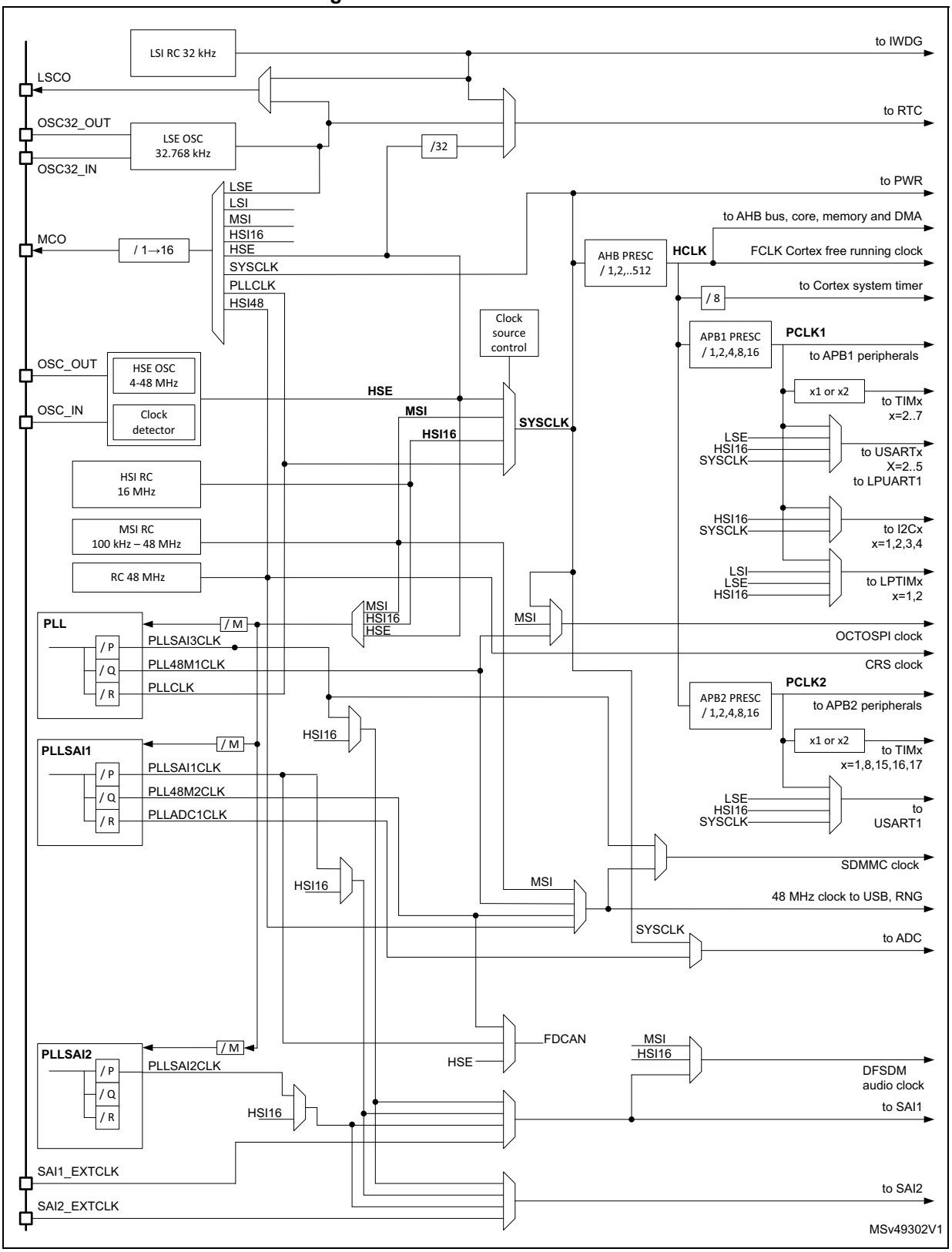
- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Clock security system:** clock sources can be changed safely on the fly in Run mode through a configuration register.
- **Clock management:** to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4 to 48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 110 MHz.
- **RC48 with clock recovery system (HSI48):** internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **UCPD kernel clock**: it is derived from HSI16 clock. The HSI16 RC oscillator must be enabled prior to the UCPD kernel clock use.
- **Auxiliary clock source:** two ultra-low-power clock sources that can be used to drive the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy. The LSI clock can be divided by 128 to output a 250 Hz as source clock.
- **Peripheral clock sources:** several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

interrupt is generated if enabled. LSE failure can also be detected and generated an interrupt.

- Clock-out capability:
  - **MCO (microcontroller clock output):** it outputs one of the internal clocks for external use by the application
  - **LSCO (low-speed clock output):** it outputs LSI or LSE in all low-power modes (except VBAT).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 110 MHz.

Figure 7. STM32L552xx clock tree



TrustZone security

When the TrustZone security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone security allows to secure some RCC system configuration and peripheral configuration clock from being read or modified by non-secure accesses:

- RCC system security:
  - HSE, HSE-CSS, HSI, MSI, LSI, LSE, LSE-CSS, HSI48 configuration and status bits
  - Main PLL, PLLSAI1, PLLSAI2, AHB prescaler configuration and status bits
  - System clock SYSCLK and HSI48 source clock selection and status bits
  - MCO clock output configuration and STOPWUCK bit
  - Reset flag RMVF configuration bit
- RCC peripheral security:
  - When a peripheral is secure, the related peripheral clock, reset, clock source selection and clock enable during low power modes control bits are secure.
- A peripheral is in secure state when:
  - For securable peripherals, when it's corresponding SEC security bit is set in the TZSC (TrustZone security controller)
  - For TrustZone-aware peripherals, a security feature of this peripheral is enabled through its dedicated bits.

3.12 Clock recovery system (CRS)

The devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in Analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

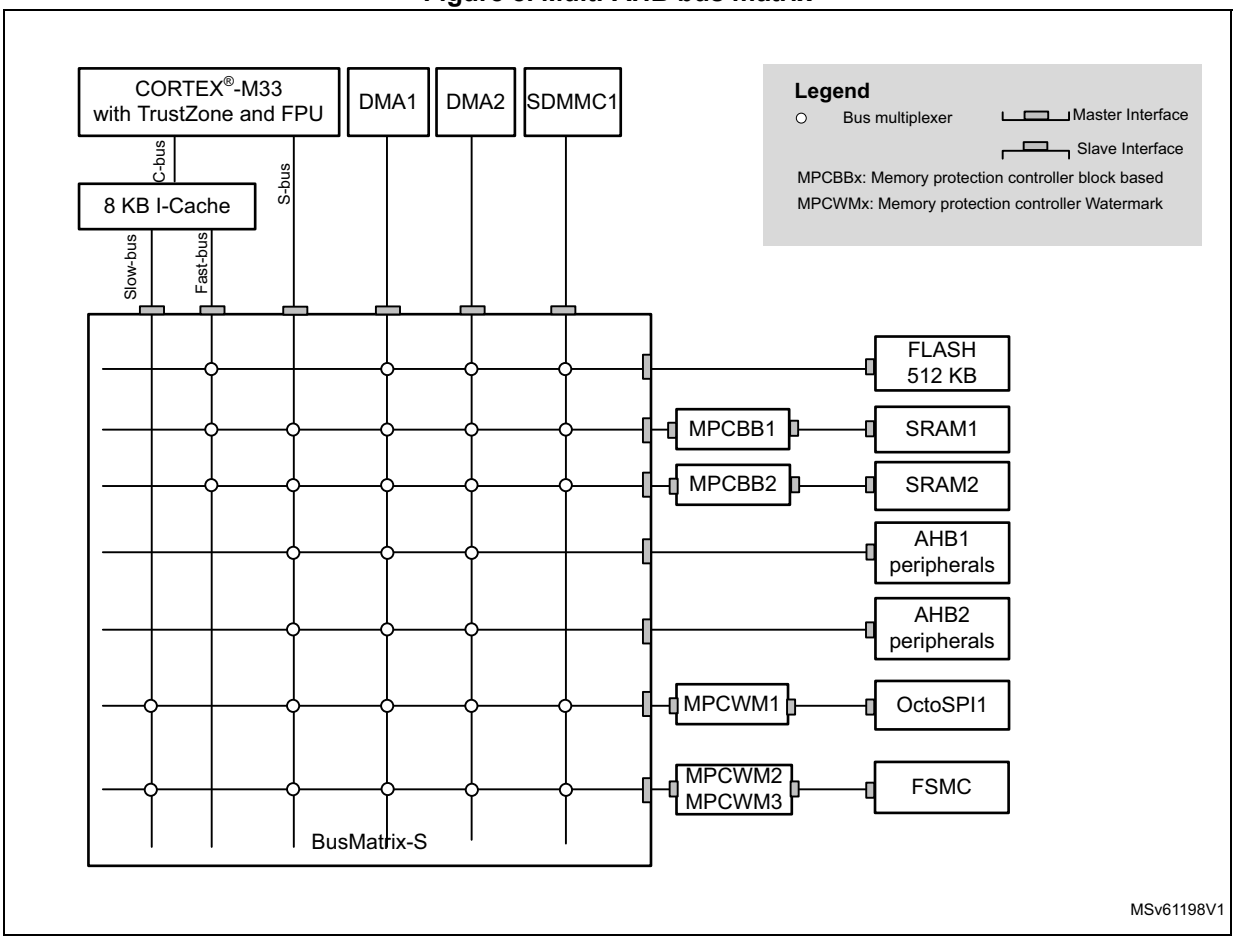
GPIO TrustZone security

Each I/O pin of GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against a non-secure access. The associated registers bit access is restricted to a secure software only. After reset, all GPIO ports are secure.

3.14 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, SDMMC1) and the slaves (Flash memory, RAM, FMC, OctoSPI, AHB and APB peripherals). It also ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 8. Multi-AHB bus matrix



3.15 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 12: DMA1 and DMA2 implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

The two DMA controllers have 16 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports 8 channels for each DMA1 and DMA2, independently configurable:

- Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
- Priority between the requests is programmable by software (4 levels per channel: very high, high, medium, low) or by hardware in case of equality (such as request 1 has priority over request 2).
- Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
- Support of transfers from/to peripherals to/from memory with circular buffer management.
- Programmable number of data to be transferred: 0 to 2^{18} - 1.
- Generation of an interrupt request per channel. Each interrupt request is caused from any of the three DMA events: transfer complete, half transfer, or transfer error.
- TrustZone support:
  - Support for AHB secure and non-secure DMA transfers, independently at a first channel level, and independently at a source and destination sub-level
  - TrustZone-aware AHB slave port, protecting any secure resource (register, register field) from a non-secure software access
- Privileged / unprivileged support:
  - Support for AHB privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port.

Table 12. DMA1 and DMA2 implementation

Feature	DMA1	DMA2
Number of DMA channels	8	8
TrustZone	1 (supported)	1 (supported)

3.16 DMA request router (DMAMUX)

When a peripheral indicates a request for DMA transfer by setting its DMA request line, the DMA request is pending until it is served and the corresponding DMA request line is reset. The DMA request router allows to route the DMA control lines between the peripherals and the DMA controllers of the product.

An embedded multi-channel DMA request generator can be considered as one of such peripherals. The routing function is ensured by a multi-channel DMA request line multiplexer. Each channel selects a unique set of DMA control lines, unconditionally or synchronously with events on synchronization inputs.

DMAMUX main features

- 16-channel programmable DMA request line multiplexer output
- 4-channel DMA request generator
- 23 trigger inputs to DMA request generator
- 23 synchronization inputs
- Per DMA request generator channel:
  - DMA request trigger input selector
  - DMA request counter
  - Event overrun flag for selected DMA request trigger input
- Per DMA request line multiplexer channel output:
  - 90 input DMA request lines from peripherals
  - One DMA request line output
  - Synchronization input selector
  - DMA request counter
  - Event overrun flag for selected synchronization input
  - One event output, for DMA request chaining
- TrustZone support:
  - Support for AHB secure and non-secure DMA transfers, independently at a channel level.
  - TrustZone-aware AHB slave port, protecting any secure resource (register, register field) from a non-secure software access, with configurable interrupt event.
  - Two secure and non-secure interrupt requests, resulting from any of the respectively secure and non-secure channels. Each channel event being caused from any of the two DMAMUX input events: trigger or synchronization overrun, associated with a respectively secure and non-secure channels.
- Privileged / Unprivileged support:
  - Support for AHB privileged and unprivileged DMA transfers, independently, at a channel level.
  - Privileged-aware AHB slave port.

3.17 Interrupts and events

3.17.1 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and to handle up to 109 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M33.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone support. The NVIC registers are banked across secure and non-secure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.17.2 Extended interrupt/event controller (EXTI)

The Extended interrupts and event controller (EXTI) manages the individual CPU and system wakeup through configurable and direct event inputs. It provides wakeup requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU an additional Event Generation block (EVG) is needed to generate the CPU event signal.

The EXTI wakeup requests allow the system to be woken up from STOP modes.

The interrupt request and event request generation can also be used in RUN modes. The EXTI also includes the EXTI mux IOport selection.

The EXTI main features are the following:

The EXTI main features are the following:

- 43 input events supported
- All event inputs allow to wake up the system.
- Events which do not have an associated wakeup flag in the peripheral, have a flag in the EXTI and generate an interrupt to the CPU from the EXTI.

The asynchronous event inputs are classified in 2 groups:

- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Configurable events have the following features:
    Selectable active trigger edge
    Interrupt pending status register bit independent for the rising and falling edge.
    Individual interrupt and event generation mask, used for conditioning the CPU wakeup, interrupt and event generation.
    SW trigger possibility
- Direct events (interrupt and wakeup sources from peripherals having an associated flag which requiring to be cleared in the peripheral)
  - Direct events have the following features:
    Fixed rising edge active trigger
    No interrupt pending status register bit in the EXTI. (The interrupt pending status flag is provided by the peripheral generating the event.)
    Individual interrupt and event generation mask, used for conditioning the CPU wakeup and event generation.
    No SW trigger possibility
- TrustZone secure events
  - The access to control and configuration bits of secure input events can be made secure.
- EXTI IO port selection

3.18 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

3.19 Flexible static memory controller (FSMC)

The flexible static memory controller (FSMC) includes two memory controllers:

- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named flexible memory controller (FMC).

The main features of the FSMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (four memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
  - Ferroelectric RAM (FRAM)
- 8-,16- bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

TrustZone security

When the TrustZone security is enabled, the whole FSMC banks are secure after reset. Non-secure area can be configured using the TZSC MPCWMx controller.

- The FSMC NOR/PSRAM bank:
  - Up to two non-secure area can be configured thought the TZSC MPCWM2 controller with a granularity of 64 Kbytes.
- The FSMC NAND bank:
  - Can be either configured as fully secure or fully non-secure using the TZSC MPCWM3 controller.

The FSMC registers can be configured as secure through the TZSC controller.

3.20 OctoSPI interface (OCTOSPI)

The OCTOSPI is a specialized communication interface targetting single, dual, quad or octal SPI memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the OCTOSPI registers
- Status polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and is seen by the system as if it were an internal memory supporting read and write operation

The OctoSPI supports two frame formats:

- Classical frame format with command, address, alternate byte, dummy cycles and data phase over 1, 2, 4 or 8 data pins
- Hyperbus™ frame format

The OCTOSPI offers the following features:

- Three functional modes: indirect, status-polling, and memory-mapped
- Read and write support in memory-mapped mode
- Supports for single, dual, quad and octal communication
- Dual-quad mode, where 8 bits can be sent/received simultaneously by accessing two quad memories in parallel.
- SDR and DTR support
- Data strobe support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the five following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Hyperbus™ support
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

TrustZone security

When the TrustZone security is enabled, the whole OCTOSPI bank is secure after reset.

Up to two non-secure area can be configured thought the TZSC MPCWM1 controller with a granularity of 64 Kbytes.

The OCTOSPI registers can be configured as secure through the TZSC controller.

3.21 Analog-to-digital converter (ADC)

The device embeds two successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into a data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.21.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 13. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 05A8 - 0x0BFA 05A9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 05CA- 0x0BFA 05CB

3.21.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and the comparators. The VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 14. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x0BFA 05AA - 0x0BFA 05AB

3.21.3 V_{BAT} battery voltage monitoring

This embedded hardware enables the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18. As the V_{BAT} voltage may be higher than the VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third of the V_{BAT} voltage.

3.22 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.23 Voltage reference buffer (VREFBUF)

The devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

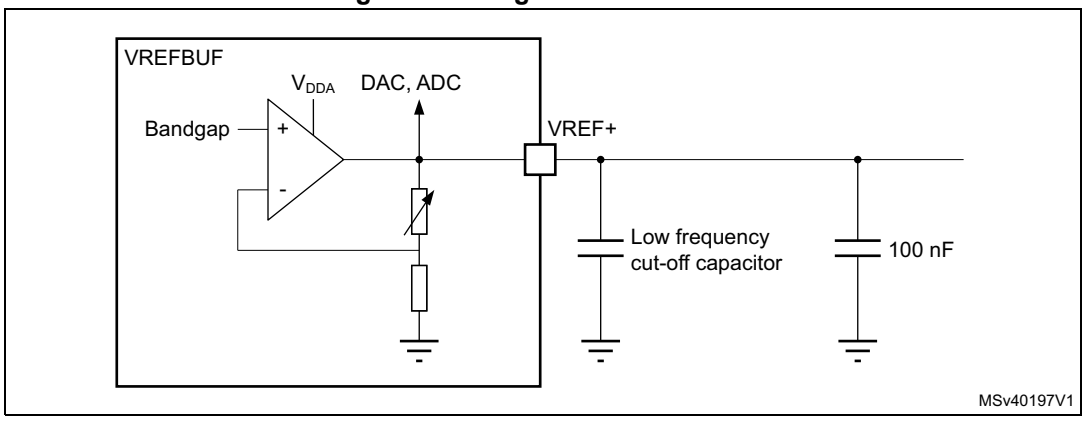
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 9. Voltage reference buffer



3.24 Comparators (COMP)

The devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

3.25 Operational amplifier (OPAMP)

The devices embed two operational amplifiers with external or internal follower routing and PGA capability.

The operational amplifier features:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.26 Digital filter for sigma-delta modulators (DFSDM)

The devices embed one DFSDM with four digital filters modules and eight external input serial channels (transceivers) or alternately eight internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to the microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs).

The DFSDM can also interface the PDM (pulse density modulation) microphones and perform PDM to PCM conversion and filtering in hardware. The DFSDM features optional parallel data stream inputs from microcontrollers memory (through DMA/CPU transfers into DFSDM).

The DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators) and the DFSDM digital filter modules perform digital processing according to the user's selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- Up to 4 multiplexed input digital serial channels:
  - Configurable SPI interface to connect various ΣΔ modulators
  - Configurable Manchester coded 1 wire interface support
  - Clock output for ΣΔ modulator(s)
- Alternative inputs from up to 4 internal digital parallel channels:
  - Inputs with up to 16 bit resolution
  - Internal sources: ADCs data or memory (CPU/DMA write) data streams
- Adjustable digital signal processing:
  - Sincx filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - Integrator: oversampling ratio (1..256)
- Up to 24-bit output data resolution:
  - Right bit-shifter on final data (0..31 bits)
- Signed output data format
- Automatic data offset correction (offset stored in register by user)
- Continuous or single conversion
- Start-of-conversion synchronization with:
  - Software trigger
  - Internal timers
  - External events
  - Start-of-conversion synchronously with first DFSDM filter (DFSDM_FLT0)
- Analog watchdog feature:
  - Low value and high value data threshold registers
  - Own configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - Input from output data register or from one or more input digital serial channels
  - Continuous monitoring independently from standard conversion
- Short-circuit detector to detect saturated analog input values (bottom and top ranges):
  - Up to 8-bit counter to detect 1..256 consecutive 0's or 1's on input data stream
  - Mnitoring continuously each channel (4 serial channel transceiver outputs)
- Break generation on analog watchdog event or short-circuit detector event
- Extremes detector:
  - Store minimum and maximum values of output data values
  - Refreshed by software
- DMA may be used to read the conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short-circuit, channel clock absence
- "Regular" or "injected" conversions:
  - "Regular" conversions can be requested at any time or even in continuous mode without having any impact on the timing of "injected" conversions.

3.27 Touch sensing controller (TSC)

The touch sensing controller provides a simple solution to add capacitive sensing functionality to any application. A capacitive sensing technology is able to detect finger presence near an electrode that is protected from direct touch by a dielectric (glass, plastic or other). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

The main features of the touch sensing controller are the following:

- Proven and robust surface charge transfer acquisition principle
- Supports up to 22 capacitive sensing channels
- Up to 3 capacitive sensing channels can be acquired in parallel offering a very good response time
- Spread spectrum feature to improve system robustness in noisy environments
- Full hardware management of the charge transfer acquisition sequence
- Programmable charge transfer frequency
- Programmable sampling capacitor I/O pin
- Programmable channel I/O pin
- Programmable max count value to avoid long acquisition when a channel is faulty
- Dedicated end of acquisition and max count error flags with interrupt capability
- One sampling capacitor for up to 3 capacitive sensing channels to reduce the system components
- Compatible with proximity, touchkey, linear and rotary touch sensor implementation
- Designed to operate with STMTouch touch sensing firmware library

Note: The number of capacitive sensing channels is dependent on the size of the packages and subject to I/O availability.

3.28 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.29 HASH hardware accelerator (HASH)

The hash processor is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-224, SHA-256), the MD5 (message-digest algorithm 5) hash algorithm and the HMAC (keyed-hash message authentication code) algorithm suitable for a variety of applications.

It computes a message digest (160 bits for the SHA-1 algorithm, 256 bits for the SHA-256 algorithm and 224 bits for the SHA-224 algorithm,128 bits for the MD5 algorithm) for messages of up to (264 - 1) bits, while the HMAC algorithms provide a way of authenticating

messages by means of hash functions. The HMAC algorithms consist in calling the SHA-1, SHA-224, SHA-256 or MD5 hash function twice.

3.30 Timers and watchdogs

The devices include two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer.

The *Table 15* below compares the features of the advanced control, general-purpose and basic timers.

Table 15. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.30.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.30.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

3.30.2 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM15, TIM16, TIM17)

There are up to seven synchronizable general-purpose timers embedded in the STM32L552xx devices (see *Table 15* for differences).
Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, TIM3, TIM4 and TIM5

  They are full-featured general-purpose timers:

  – TIM2 and TIM5 have a 32-bit auto-reload up/downcounter and 32-bit prescaler

  – TIM3 and TIM4 have 16-bit auto-reload up/downcounter and 16-bit prescaler.

  These timers feature four independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  They are general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has two channels and one complementary channel

  – TIM16 and TIM17 have one channel and one complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.30.3 Basic timers (TIM6 and TIM7)

The basic timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit timebases.

3.30.4 Low-power timer (LPTIM1, LPTIM2 and LPTIM3)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by LSE, LSI or an external clock. They are able to wakeup the system from Stop mode.

LPTIM1 and LPTIM3 are active in Stop 0, Stop 1 and Stop 2 modes.

LPTIM2 is active in Stop 0 and Stop 1 mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by pulse counter application).
- Programmable digital glitch filter
- Encoder mode (LPTIM1 only).

3.30.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and an 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI) and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.30.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.30.7 SysTick timer

The Cortex-M33 with TrustZone embeds two SysTick timers.

When TrustZone is activated, two SysTick timer are available:

- SysTick, Secure instance.
- SysTick, Non-secure instance.

When TrustZone is disabled, only one SysTick timer is available.

This timer (secure or non-secure) is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.31 Real-time clock (RTC)

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wakeup Timer and timestamp individual secure or non-secure configuration

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the V_{BAT} pin.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE), divided by a prescaler in the RCC.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp) can generate an interrupt and wakeup the device from the low-power modes.

3.32 Tamper and backup registers (TAMP)

32 32-bit backup registers are retained in all low-power modes and also in VBAT mode. They can be used to store sensitive data as their content is protected by an tamper detection circuit. 8 tamper pins and 7 internal tampers are available for anti-tamper detection.

The external tamper pins can be configured for edge detection, or level detection with or without filtering, or active tamper which increases the security level by auto checking that the tamper pins are not externally opened or shorted.

TAMP main features:

- 32 backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the RTC domain that remains powered-on by VBAT when the VDD power is switched off
- 8 external tamper detection events
  - Each external event can be configured to be active or passive
  - External passive tampers with configurable filter and internal pull-up
- 5 internal tamper events
- Any tamper detection can generate a RTC timestamp event
- Any tamper detection can erase the backup registers
- TrustZone support:
  - Tamper secure or non-secure configuration.
  - Backup registers configuration in 3 configurable-size areas:
    1 read/write secure area
    1 write secure/read non-secure area
    1 read/write non-secure area
- Monotonic counter.

3.33 Inter-integrated circuit interface (I2C)

The device embeds four I2C. Refer to *Table 16: I2C implementation* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to *Figure 7: STM32L552xx clock tree*
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 16. I2C implementation

I2C features(1)	I2C1	I2C2	I2C3	I2C4
Standard-mode (up to 100 kbit/s)	X	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X	X	X
Programmable analog and digital noise filters	X	X	X	X
SMBus/PMBus hardware support	X	X	X	X
Independent clock	X	X	X	X
Wakeup from Stop 0, Stop 1 mode on address match	X	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X	-

1. X: supported

3.34 Universal synchronous/asynchronous receiver transmitter (USART)

The devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4, UART5).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN master/slave capability. They provide hardware management of the CTS and RTS signals, and RS485 driver enable. They are able to communicate at speeds of up to 10 Mbit/s.

The USART1, USART2 and USART3 also provide a Smartcard mode (ISO 7816 compliant) and an SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3,4,5) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 17. USART/UART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	UART4	UART5	LPUART1
Hardware flow control for modem	X	X	X	X	X	X
Continuous communication using DMA	X	X	X	X	X	X
Multiprocessor communication	X	X	X	X	X	X
Synchronous mode	X	X	X	-	-	-
Smartcard mode	X	X	X	-	-	-
Single-wire half-duplex communication	X	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X	-
LIN mode	X	X	X	X	X	-
Dual clock domain	X	X	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	-	-	X
Receiver timeout interrupt	X	X	X	X	X	-
Modbus communication	X	X	X	X	X	-
Auto baud rate detection	X (4 modes)					-
Driver enable	X	X	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits					

1. X = supported.

3.35 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode using baudrates up to 220 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

3.36 Serial peripheral interface (SPI)

Three SPI interfaces allow communication up to slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives eight master mode frequencies and the frame size is configurable from 4 bits to 16 bits. The SPI interfaces support NSS pulse mode, TI mode and hardware CRC calculation.

All SPI interfaces can be served by the DMA controller.

3.37 Serial audio interfaces (SAI)

The devices embed two SAI. Refer to *Table 18: SAI implementation* for the features implementation. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

The SAI peripheral supports:

- Two independent audio sub-blocks which can be transmitters or receivers with their respective FIFO.
- 8-word integrated FIFOs for each audio sub-block.
- Synchronous or asynchronous mode between the audio sub-blocks.
- Master or slave configuration independent for both audio sub-blocks.
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode.
- Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit.
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 and SPDIF out.

- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame.
- Number of bits by frame may be configurable.
- Frame synchronization active level configurable (offset, bit length, level).
- First active bit position in the slot is configurable.
- LSB first or MSB first for data transfer.
- Mute mode.
- Stereo/Mono audio frame capability.
- Communication clock strobing edge configurable (SCK).
- Error flags with associated interrupts if enabled respectively.
  - Overrun and underrun detection.
  - Anticipated frame synchronization signal detection in slave mode.
  - Late frame synchronization signal detection in slave mode.
  - Codec not ready for the AC'97 mode in reception.
- Interruption sources when enabled:
  - Errors.
  - FIFO requests.
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio sub-block.

Table 18. SAI implementation

SAI features(1)	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO size	X (8 Word)	X (8 Word)
SPDIF	X	X
PDM	X	-

1. X: supported

3.38 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The SD/SDIO, MultiMediaCard (MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD Memory Card Specifications Version 4.1. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Full compliance with SDIO Card Specification Version 4.0: card support for two different databus modes: 1-bit (default) and 4-bit. (SDR104 SDMMC_CK speed limited to maximum allowed IO speed, SPI mode and UHS-II mode not supported)
- Data transfer up to 104 Mbyte/s for the 8-bit mode (depending maximum allowed IO speed)
- Data and command output enable signals to control external bidirectional drivers.

3.39 Controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN modules and message RAM memory.

The CAN module (FDCAN) is compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

A 1 Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers.

3.40 Universal serial bus (USB FS)

The devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and battery charging detection according to Battery Charging Specification Revision 1.2.

The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 link power management. It has software-configurable endpoint setting with packet memory up-to 1 Kbyte and suspend/resume support.

This interface requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator (HSI48) in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

3.41 USB Type-C™ / USB Power Delivery controller (UCPD)

The device embeds one controller (UCPD) compliant with USB Type-C Rev. 1.2 and USB Power Delivery Rev. 3.0 specifications.

The controller uses specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- “Dead battery” support
- USB Power Delivery message transmission and reception
- FRS (fast role swap) support

The digital controller handles notably:

- USB Type-C level detection with debounce, generating interrupts
- FRS detection, generating an interrupt
- Byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode
- Ordered sets (with a programmable ordered set mask at receive)
- Frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages and FRS signaling.

3.42 Development support

3.42.1 Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins could be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

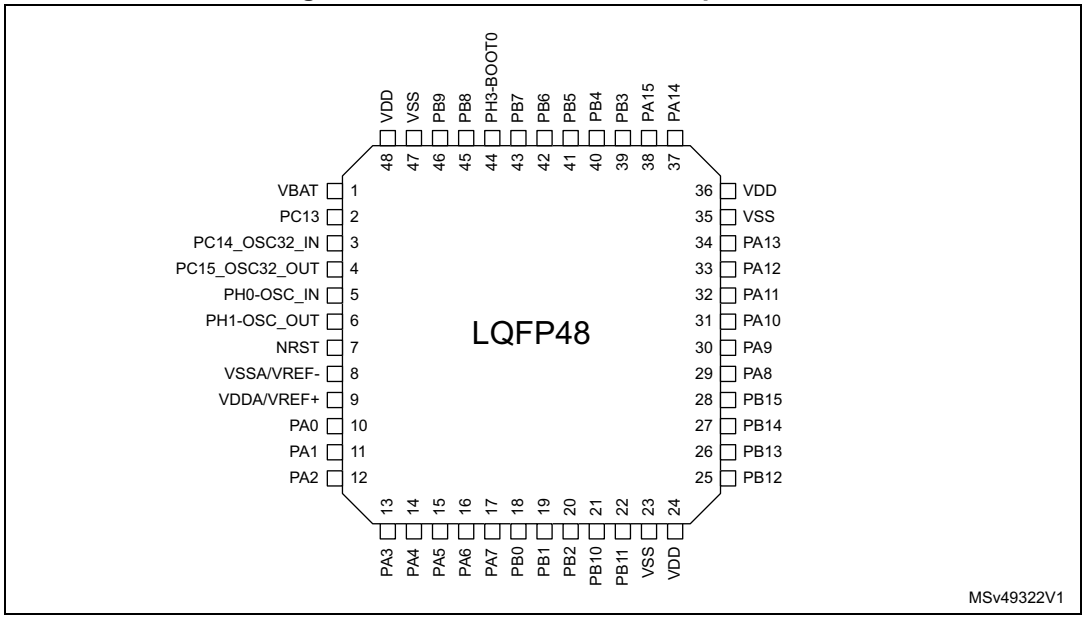
3.42.2 Embedded Trace Macrocell™

The Arm® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. Real-time instruction and data flow activity be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

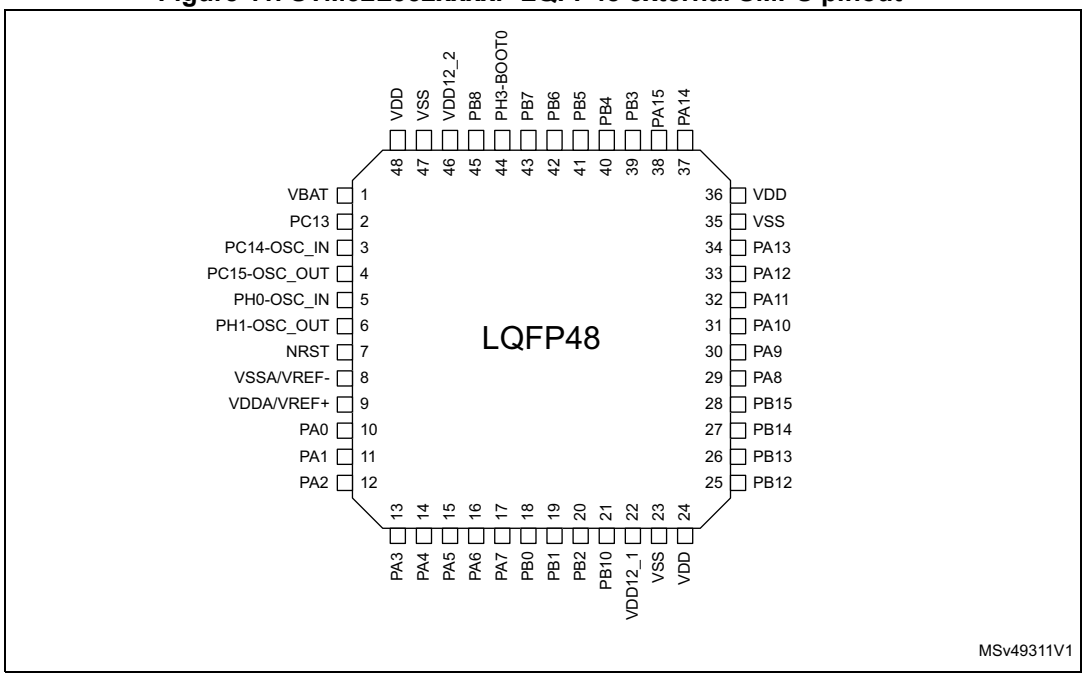
4 Pinouts and pin description

Figure 10. STM32L552xx LQFP48 pinout(1)



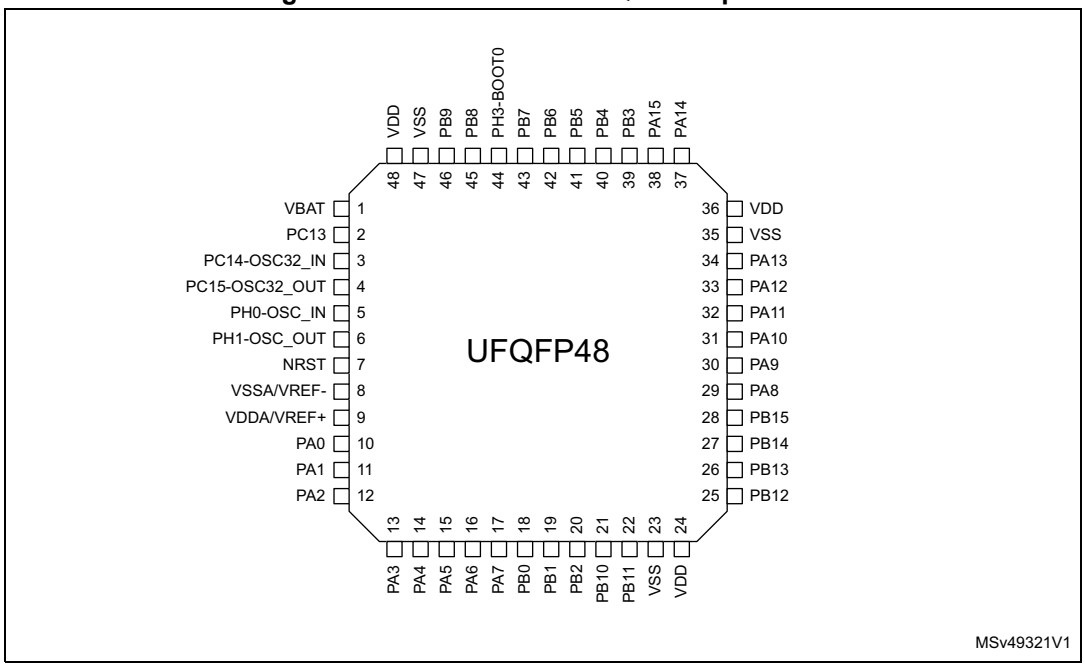
1. The above figure shows the package top view.

Figure 11. STM32L552xxxxP LQFP48 external SMPS pinout(1)



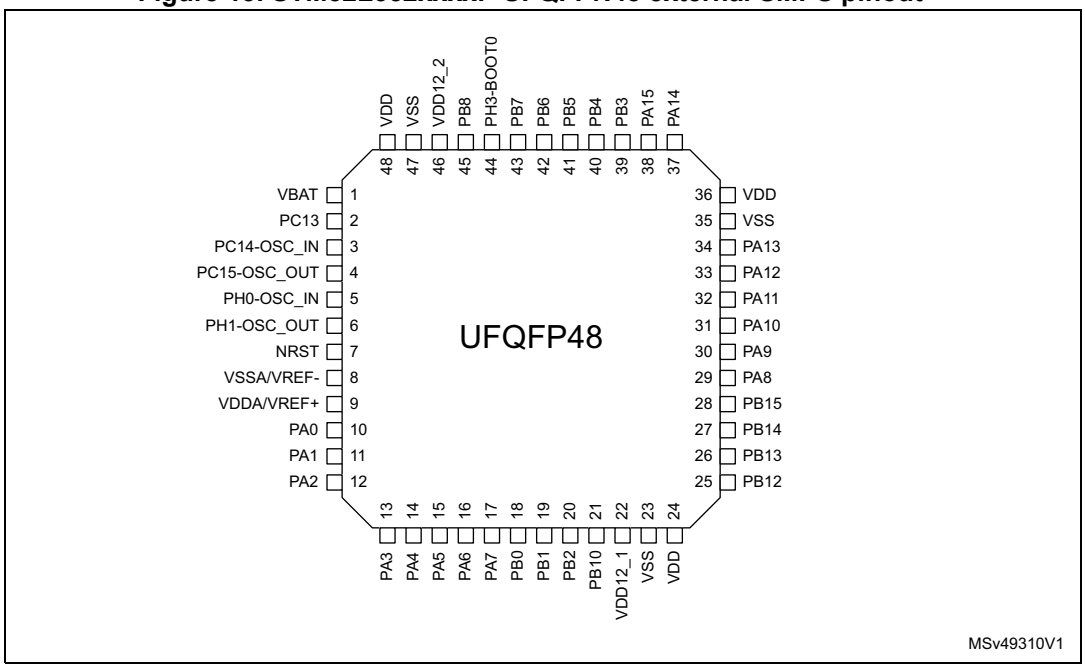
1. The above figure shows the package top view.

Figure 12. STM32L552xx UFQFPN48 pinout(1)



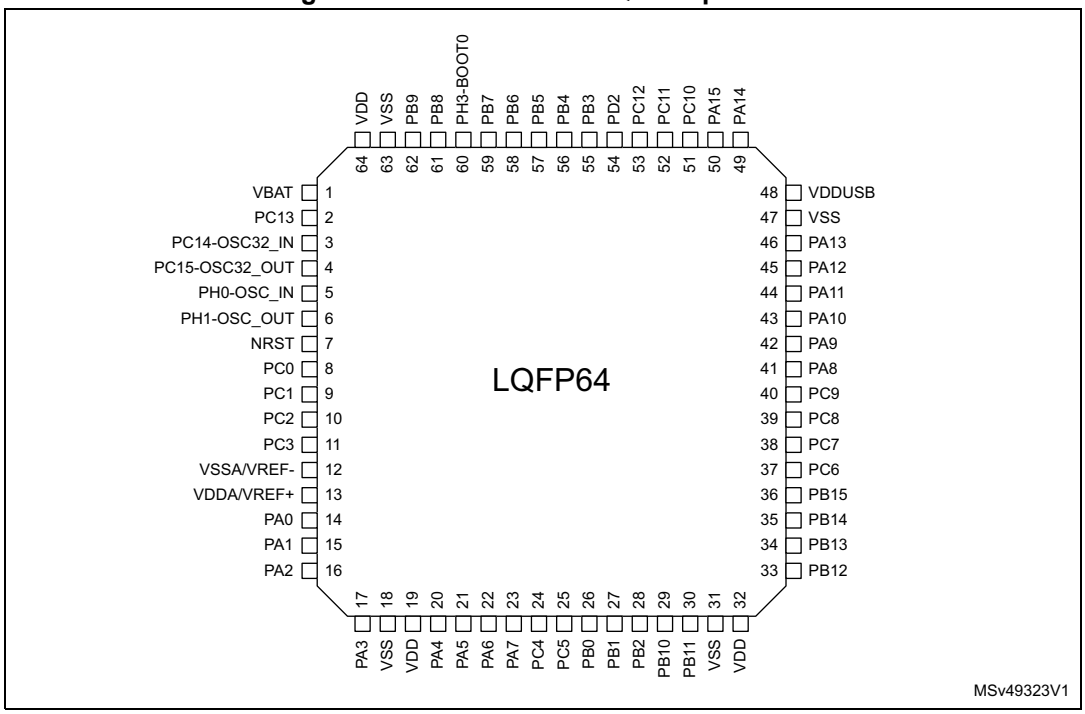
1. The above figure shows the package top view.

Figure 13. STM32L552xxxxP UFQFPN48 external SMPS pinout(1)



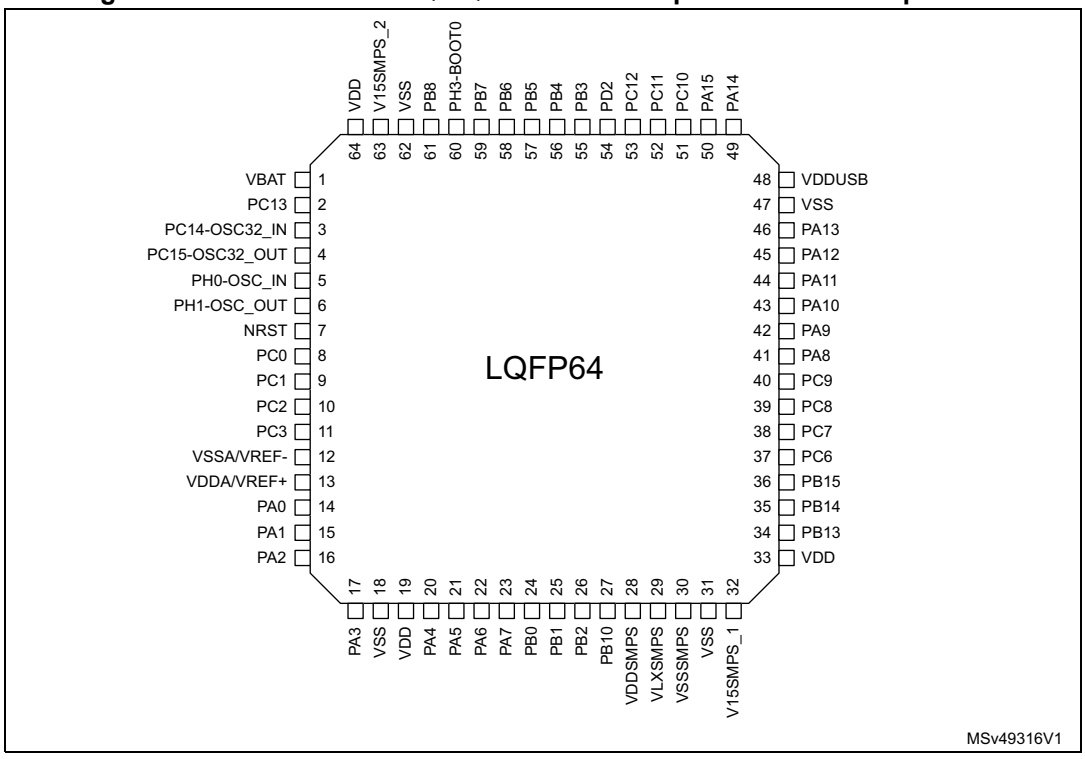
1. The above figure shows the package top view.

Figure 14. STM32L552xx LQFP64 pinout(1)



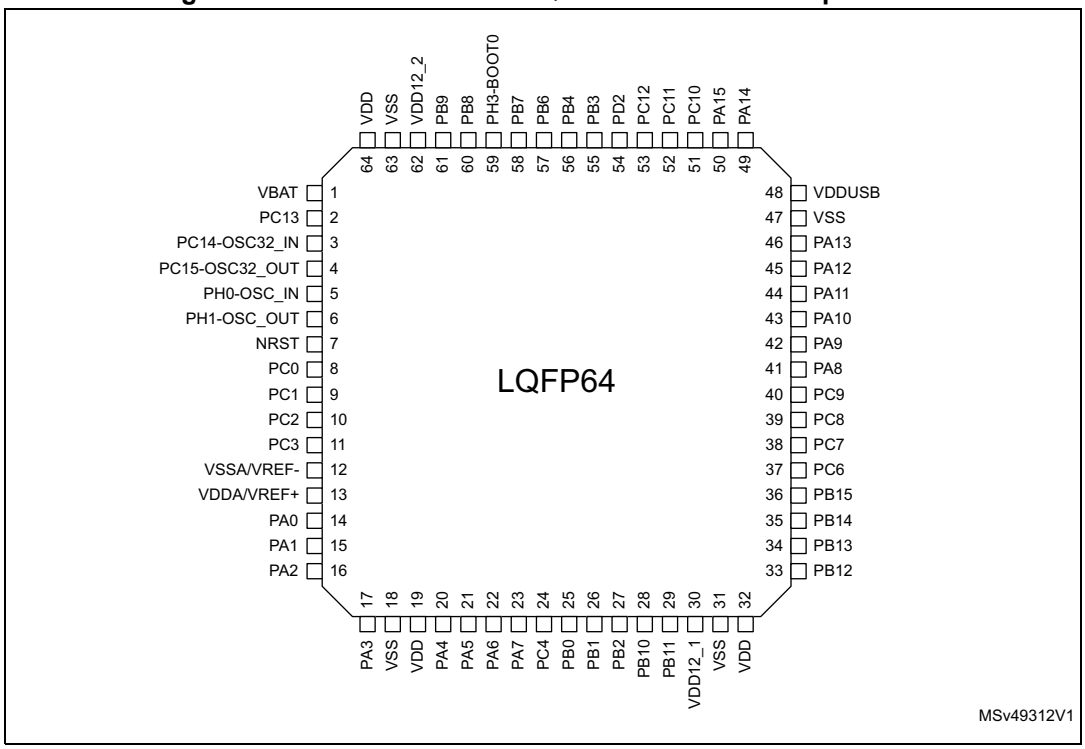
1. The above figure shows the package top view.

Figure 15. STM32L552xxxxQ LQFP64 SMPS step down converter pinout(1)



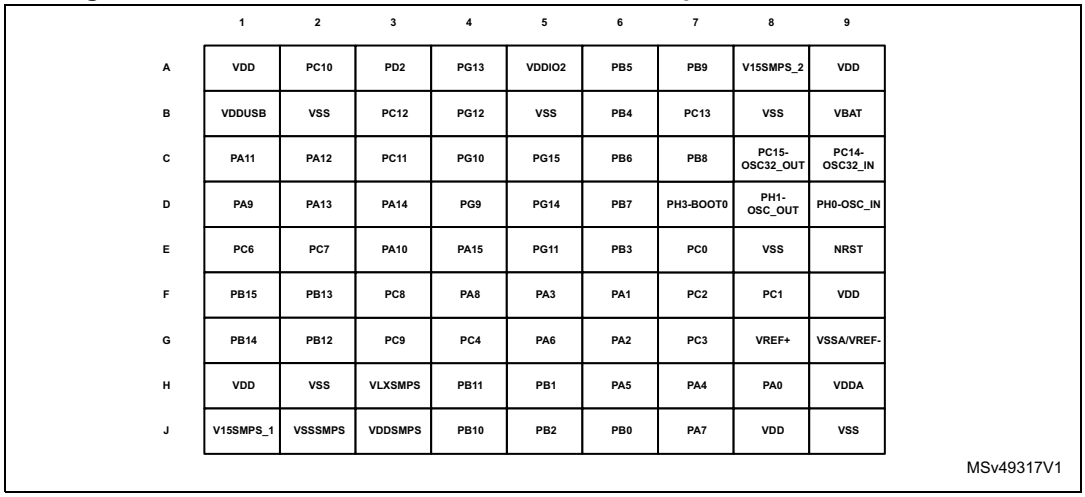
1. The above figure shows the package top view.

Figure 16. STM32L552xxxxP LQFP64 external SMPS pinout(1)



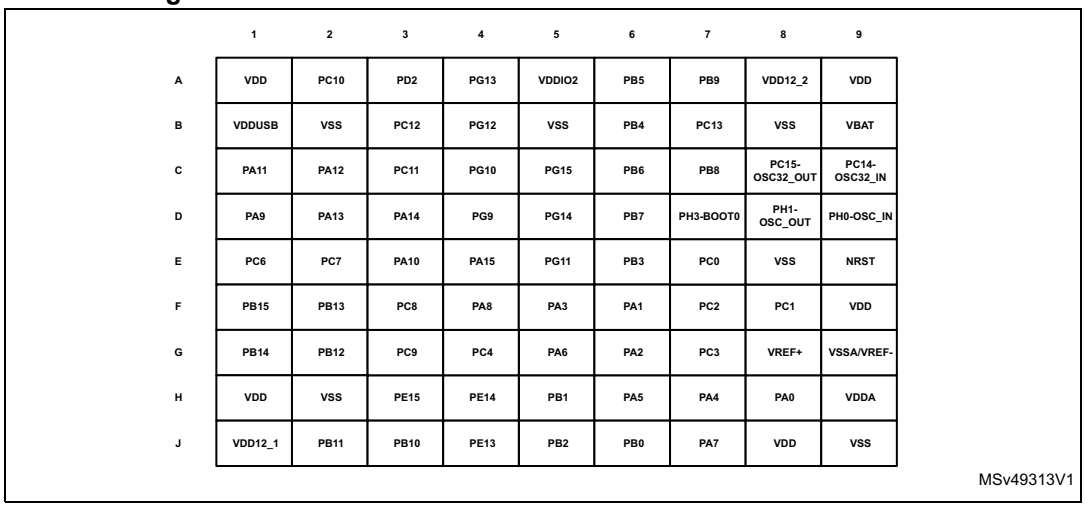
1. The above figure shows the package top view.

Figure 17. STM32L552xxxxQ WLCSP81 SMPS step down converter ballout(1)



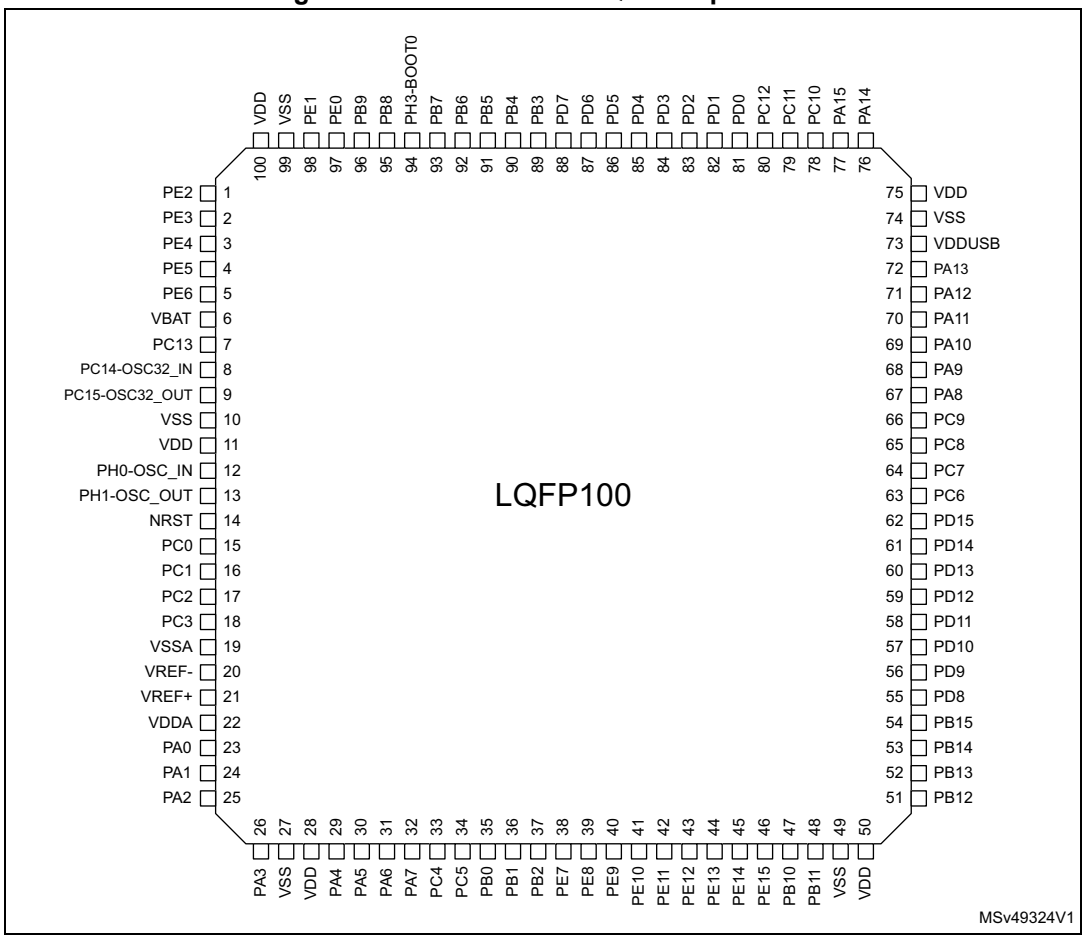
1. The above figure shows the package top view.

Figure 18. STM32L552xxxxP WLCSP81 external SMPS ballout(1)



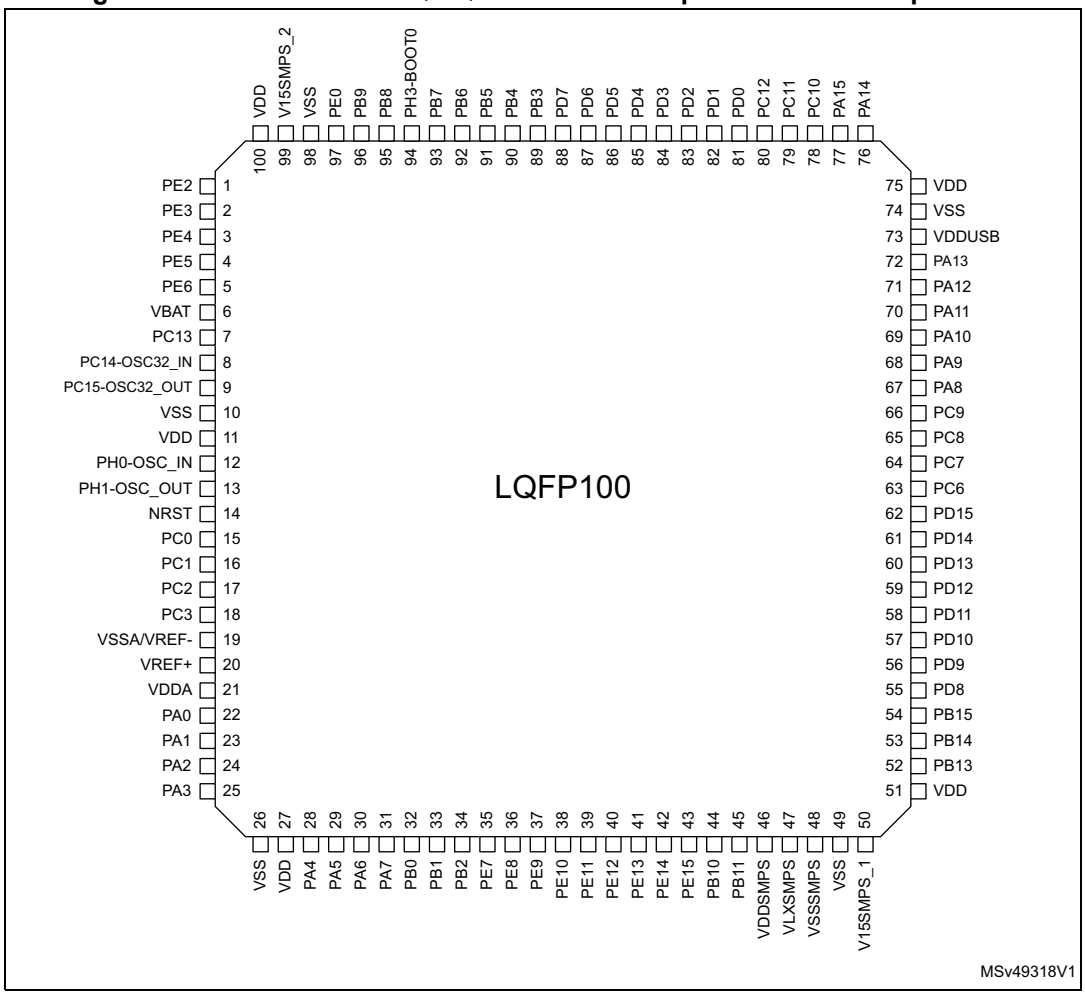
1. The above figure shows the package top view.

Figure 19. STM32L552xx LQFP100 pinout(1)



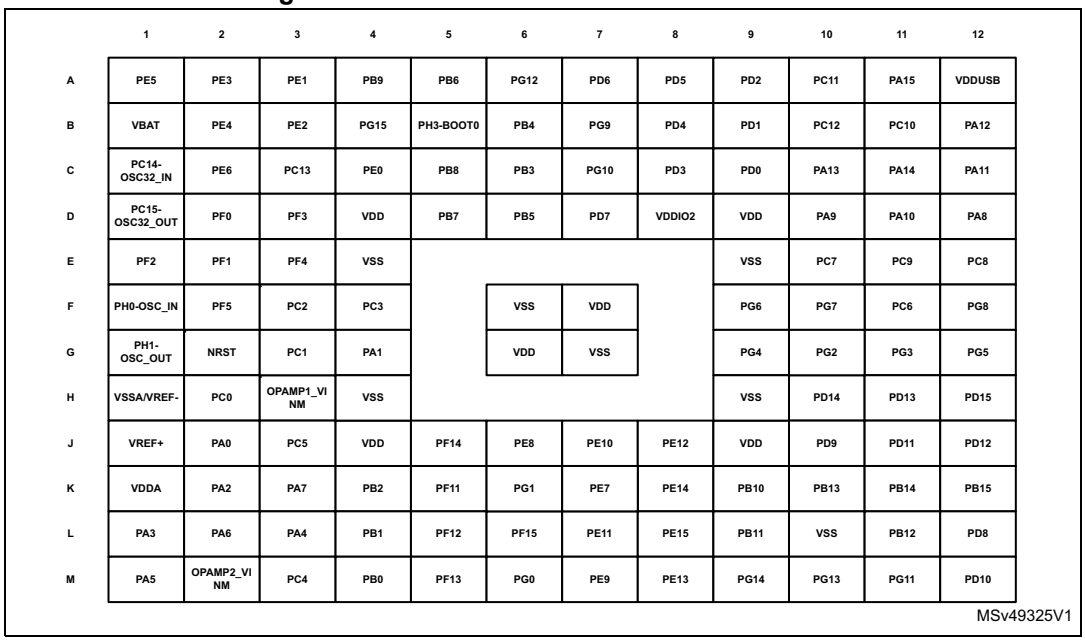
1. The above figure shows the package top view.

Figure 20. STM32L552xxxxQ LQFP100 SMPS step down converter pinout(1)



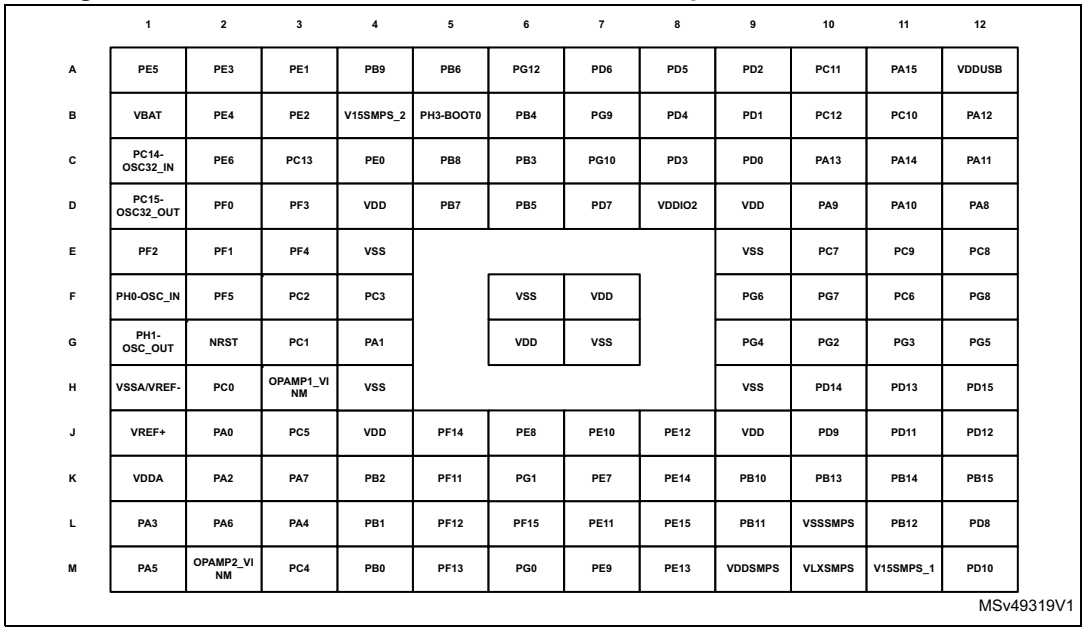
1. The above figure shows the package top view.

Figure 21. STM32L552xx UFBGA132 ballout(1)



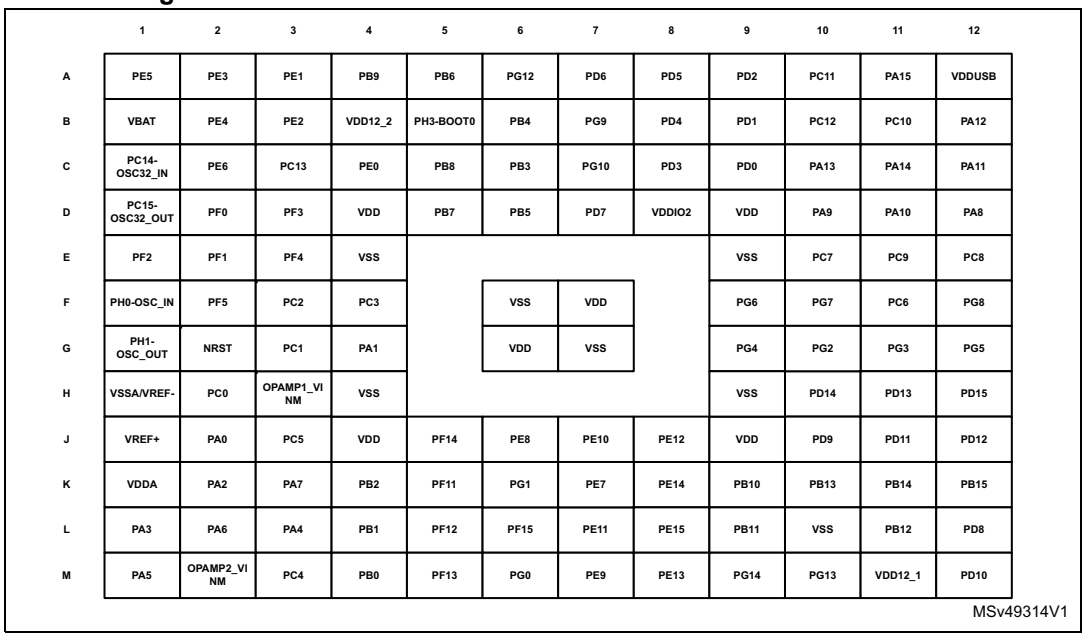
1. The above figure shows the package top view.

Figure 22. STM32L552xxxxQ UFBGA132 SMPS step down converter ballout(1)



1. The above figure shows the package top view.

Figure 23. STM32L552xxxxP UFBGA132 external SMPS ballout(1)

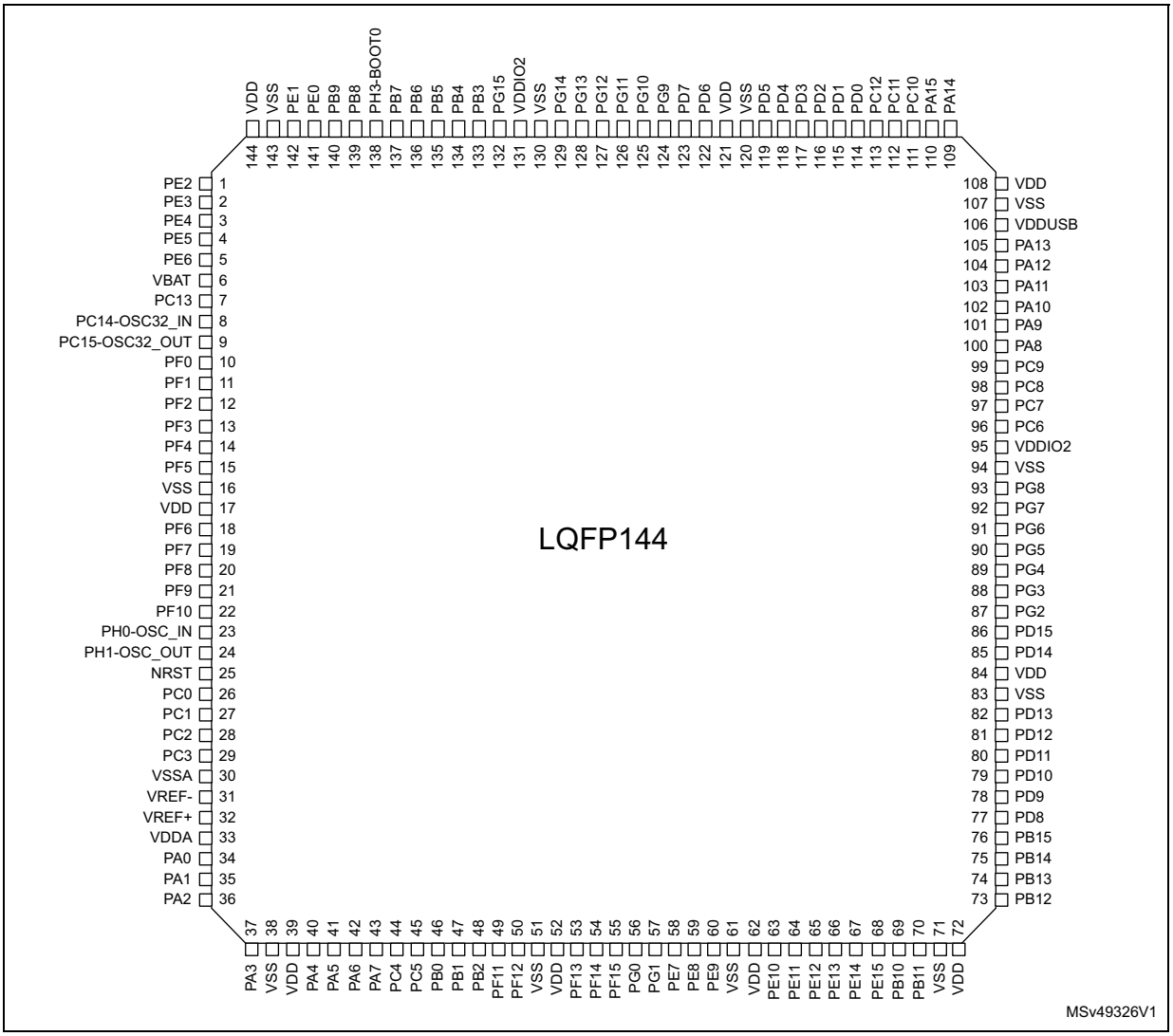


	1	2	3	4	5	6	7	8	9	10	11	12
A	PE5	PE3	PE1	PB9	PB6	PG12	PD6	PD5	PD2	PC11	PA15	VDDUSB
B	VBAT	PE4	PE2	VDD12_2	PH3-BOOT0	PB4	PG9	PD4	PD1	PC12	PC10	PA12
C	PC14-OSC32_IN	PE6	PC13	PE0	PB8	PB3	PG10	PD3	PD0	PA13	PA14	PA11
D	PC15-OSC32_OUT	PF0	PF3	VDD	PB7	PB5	PD7	VDDIO2	VDD	PA9	PA10	PA8
E	PF2	PF1	PF4	VSS					VSS	PC7	PC9	PC8
F	PH0-OSC_IN	PF5	PC2	PC3		VSS	VDD		PG6	PG7	PC6	PG8
G	PH1-OSC_OUT	NRST	PC1	PA1		VDD	VSS		PG4	PG2	PG3	PG5
H	VSSA/VREF-	PC0	OPAMP1_VINM	VSS					VSS	PD14	PD13	PD15
J	VREF+	PA0	PC5	VDD	PF14	PE8	PE10	PE12	VDD	PD9	PD11	PD12
K	VDDA	PA2	PA7	PB2	PF11	PG1	PE7	PE14	PB10	PB13	PB14	PB15
L	PA3	PA6	PA4	PB1	PF12	PF15	PE11	PE15	PB11	VSS	PB12	PD8
M	PA5	OPAMP2_VINM	PC4	PB0	PF13	PG0	PE9	PE13	PG14	PG13	VDD12_1	PD10

MSv49314V1

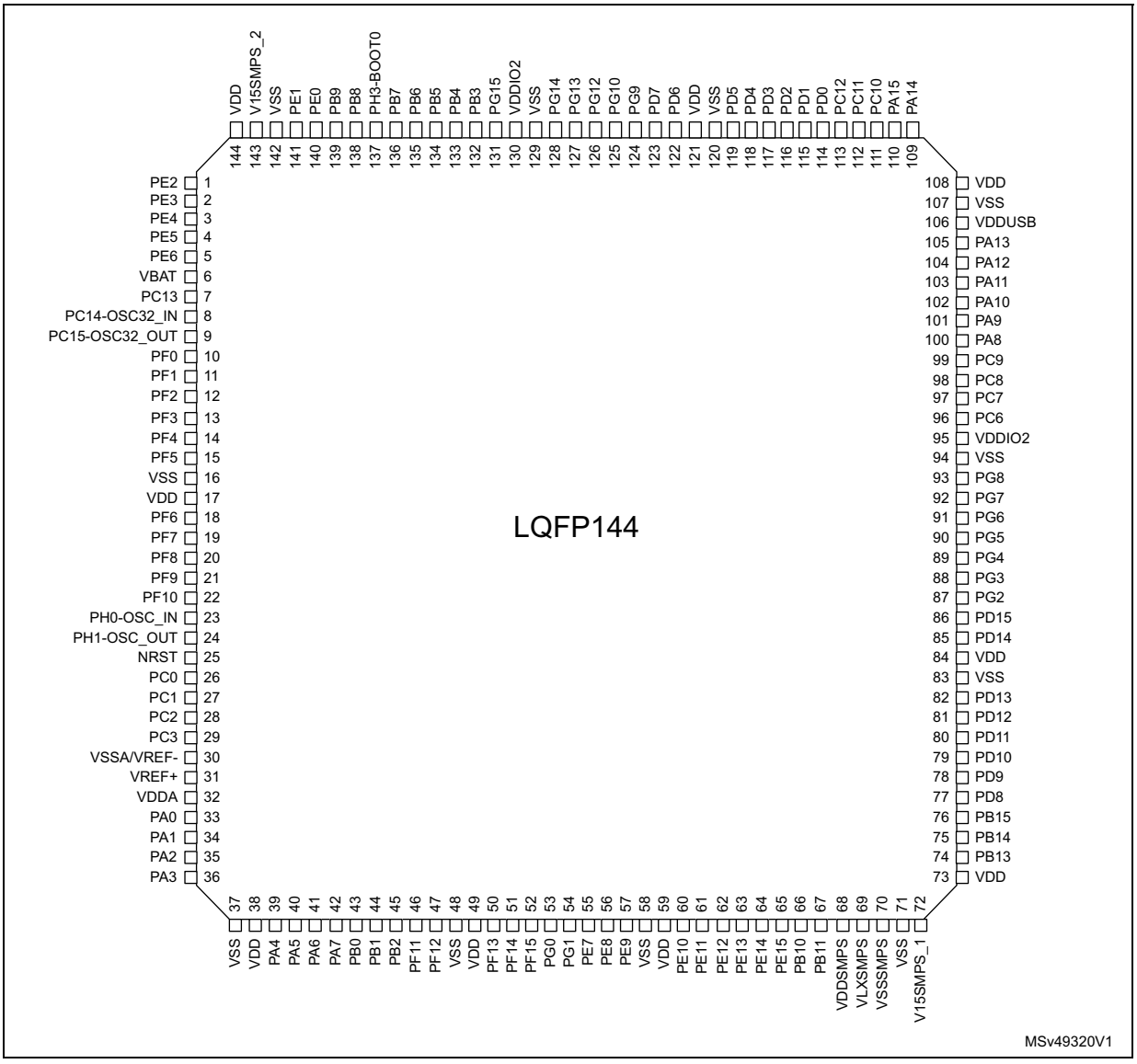
1. The above figure shows the package top view.

Figure 24. STM32L552xx LQFP144 pinout(1)



1. The above figure shows the package top view.

Figure 25. STM32L552xxxxQ LQFP144 SMPS step down converter pinout(1)



1. The above figure shows the package top view.

Table 19. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Option for TT or FT I/Os	
		_f (1)	I/O, Fm+ capable
		_u (2)	I/O, with USB function supplied by V_{DDUSB}
		_a (3)	I/O, with Analog switch function supplied by V_{DDA}
		_s (4)	I/O supplied only by V_{DDIO2}
		_c	I/O, USB Type-C PD capable
		_d	I/O, USB Type-C PD dead battery function
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 20* are: FT_f, FT_fa.
2. The related I/O structures in *Table 20* are: FT_u, FT_lu.
3. The related I/O structures in *Table 20* are: FT_a, FT_fa, TT_a.
4. The related I/O structures in *Table 20* are: FT_s, FT_fs.

Table 20. STM32L552xx pin definitions

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	B3	-	-	1	B3	1	-	-	-	1	B3	1	PE2	I/O	FT	-	TRACECK, TIM3_ETR, SAI1_CK1, TSC_G7_IO1, FMC_A23, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	A2	-	-	2	A2	2	-	-	-	2	A2	2	PE3	I/O	FT	-	TRACED0, TIM3_CH1, OCTOSPI1_DQS, TSC_G7_IO2, FMC_A19, SAI1_SD_B, EVENTOUT	-
-	-	-	-	B2	-	-	3	B2	3	-	-	-	3	B2	3	PE4	I/O	FT	-	TRACED1, TIM3_CH2, SAI1_D2, DFSDM1_DATIN3, TSC_G7_IO3, FMC_A20, SAI1_FS_A, EVENTOUT	-
-	-	-	-	A1	-	-	4	A1	4	-	-	-	4	A1	4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, SAI1_CK2, DFSDM1_CKIN3, TSC_G7_IO4, FMC_A21, SAI1_SCK_A, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	C2	-	-	5	C2	5	-	-	-	5	C2	5	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_D1, FMC_A22, SAI1_SD_A, EVENTOUT	WKUP3, TAMP_IN3/TAMP_OUT6
1	1	1	B9	B1	1	B9	6	B1	6	1	1	1	6	B1	6	VBAT	S	-	-	-	-
2	2	2	B7	C3	2	B7	7	C3	7	2	2	2	7	C3	7	PC13	I/O	FT	(1) (2)	EVENTOUT	WKUP2, RTC_TS/RTC_OUT1, TAMP_IN1/TAMP_OUT2
3	3	3	C9	C1	3	C9	8	C1	8	3	3	3	8	C1	8	PC14-OSC32_IN (PC14)	I/O	FT	(1) (2)	EVENTOUT	OSC32_IN
4	4	4	C8	D1	4	C8	9	D1	9	4	4	4	9	D1	9	PC15-OSC32_OUT (PC15)	I/O	FT	(1) (2)	EVENTOUT	OSC32_OUT
-	-	-	-	D2	-	-	-	D2	10	-	-	-	-	D2	10	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	E2	-	-	-	E2	11	-	-	-	-	E2	11	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	-	-	E1	-	-	-	E1	12	-	-	-	-	E1	12	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	D3	-	-	-	D3	13	-	-	-	-	D3	13	PF3	I/O	FT_a	-	LPTIM3_IN1, FMC_A3, EVENTOUT	-
-	-	-	-	E3	-	-	-	E3	14	-	-	-	-	E3	14	PF4	I/O	FT_a	-	LPTIM3_ETR, FMC_A4, EVENTOUT	-
-	-	-	-	F2	-	-	-	F2	15	-	-	-	-	F2	15	PF5	I/O	FT_a	-	LPTIM3_OUT, FMC_A5, EVENTOUT	-
-	-	-	-	F6	-	-	10	F6	16	-	-	-	10	F6	16	VSS	S	-	-	-	-
-	-	-	-	F7	-	-	11	F7	17	-	-	-	11	F7	17	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	18	-	-	-	-	-	18	PF6	I/O	FT_a	-	TIM5_ETR, TIM5_CH1, OCTOSPI1_IO3, SAI1_SD_B, EVENTOUT	-
-	-	-	-	-	-	-	-	-	19	-	-	-	-	-	19	PF7	I/O	FT_a	-	TIM5_CH2, OCTOSPI1_IO2, SAI1_MCLK_B, EVENTOUT	TAMP_IN6/TAMP_OUT3

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	-	-	-	-	-	20	-	-	-	-	-	20	PF8	I/O	FT_a	-	TIM5_CH3, OCTOSPI1_IO0, SAI1_SCK_B, EVENTOUT	TAMP_IN7/TAMP_OUT8
-	-	-	-	-	-	-	-	-	21	-	-	-	-	-	21	PF9	I/O	FT_a	-	TIM5_CH4, OCTOSPI1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	TAMP_IN8/TAMP_OUT7
-	-	-	-	-	-	-	-	-	22	-	-	-	-	-	22	PF10	I/O	FT_a	-	OCTOSPI1_CLK, DFSDM1_CKOUT, SAI1_D3, TIM15_CH2, EVENTOUT	-
5	5	5	D9	F1	5	D9	12	F1	23	5	5	5	12	F1	23	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	6	6	D8	G1	6	D8	13	G1	24	6	6	6	13	G1	24	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	7	7	E9	G2	7	E9	14	G2	25	7	7	7	14	G2	25	NRST	I-O	RST	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	8	E7	H2	8	E7	15	H2	26	-	-	8	15	H2	26	PC0	I/O	FT_fa	-	LPTIM1_IN1, OCTOSPI1_IO7, I2C3_SCL, LPUART1_RX, SDMMC1_D5, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	ADC12_IN1
-	-	9	F8	G3	9	F8	16	G3	27	-	-	9	16	G3	27	PC1	I/O	FT_fa	-	TRACED0, LPTIM1_OUT, SPI2_MOSI, I2C3_SDA, LPUART1_TX, OCTOSPI1_IO4, SAI1_SD_A, EVENTOUT	ADC12_IN2
-	-	10	F7	F3	10	F7	17	F3	28	-	-	10	17	F3	28	PC2	I/O	FT_a	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, OCTOSPI1_IO5, EVENTOUT	ADC12_IN3

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	11	G7	F4	11	G7	18	F4	29	-	-	11	18	F4	29	PC3	I/O	FT_a	-	LPTIM1_ETR, LPTIM3_OUT, SAI1_D1, SPI2_MOSI, OCTOSPI1_IO6, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC12_IN4
-	-	-	-	-	-	-	-	-	-	-	-	-	19	-	30	VSSA	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	20	-	31	VREF-	S	-	-	-	-
8	8	12	G9	H1	12	G9	19	H1	30	8	8	12	-	H1	-	VSSA/VREF-	S	-	-	-	-
-	-	-	G8	J1	-	G8	20	J1	31	-	-	-	21	J1	32	VREF+	S	-	-	-	VREFBUF_OUT
-	-	-	H9	K1	-	H9	21	K1	32	-	-	-	22	K1	33	VDDA	S	-	-	-	-
9	9	13	-	-	13	-	-	-	-	9	9	13	-	-	-	VDDA/VREF+	S	-	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
10	10	14	H8	J2	14	H8	22	J2	33	10	10	14	23	J2	34	PA0	I/O	FT_a	-	TIM2_CH1, TIM5_CH1, TIM8_ETR, USART2_CTS/USART2_NSS, UART4_TX, SAI1_EXTCLK, TIM2_ETR, EVENTOUT	OPAMP1_VINP, ADC12_IN5, WKUP1, TAMP_IN2/TAMP_OUT1
-	-	-	-	H3	-	-	-	H3	-	-	-	-	-	H3	-	OPAMP1_VINM	I	TT	-	-	-
11	11	15	F6	G4	15	F6	23	G4	34	11	11	15	24	G4	35	PA1	I/O	FT_a	-	TIM2_CH2, TIM5_CH2, I2C1_SMBA, SPI1_SCK, USART2_RTS/USART2_DE, UART4_RX, OCTOSPI1_DQS, TIM15_CH1N, EVENTOUT	OPAMP1_VINM, ADC12_IN6, TAMP_IN5/TAMP_OUT4

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
12	12	16	G6	K2	16	G6	24	K2	35	12	12	16	25	K2	36	PA2	I/O	FT_a	-	TIM2_CH3, TIM5_CH3, USART2_TX, LPUART1_TX, OCTOSPI1_NCS, UCPD1_FRSCC1, SAI2_EXTCLK, TIM15_CH1, EVENTOUT	ADC12_IN7, WKUP4/LSCO, COMP1_INP
13	13	17	F5	L1	17	F5	25	L1	36	13	13	17	26	L1	37	PA3	I/O	TT_a	-	TIM2_CH4, TIM5_CH4, SAI1_CK1, USART2_RX, LPUART1_RX, OCTOSPI1_CLK, SAI1_MCLK_A, TIM15_CH2, EVENTOUT	OPAMP1_VOUT, ADC12_IN8
-	-	18	H2	G7	18	H2	26	G7	37	-	-	18	27	G7	38	VSS	S	-	-	-	-
-	-	19	-	G6	19	-	27	G6	38	-	-	19	28	G6	39	VDD	S	-	-	-	-
14	14	20	H7	L3	20	H7	28	L3	39	14	14	20	29	L3	40	PA4	I/O	TT_a	-	OCTOSPI1_NCS, SPI1_NSS, SPI3_NSS, USART2_CK, SAI1_FS_B, LPTIM2_OUT, EVENTOUT	ADC12_IN9, DAC1_OUT1

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
15	15	21	H6	M1	21	H6	29	M1	40	15	15	21	30	M1	41	PA5	I/O	TT_a	-	TIM2_CH1, TIM2_ETR, TIM8_CH1N, SPI1_SCK, LPTIM2_ETR, EVENTOUT	ADC12_IN10, DAC1_OUT2
16	16	22	G5	L2	22	G5	30	L2	41	16	16	22	31	L2	42	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, USART3_CTS/USART3_NSS, LPUART1_CTS, OCTOSPI1_IO3, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC12_IN11
-	-	-	-	M2	-	-	-	M2	-	-	-	-	-	M2	-	OPAMP2_VINM	I	TT	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
17	17	23	J7	K3	23	J7	31	K3	42	17	17	23	32	K3	43	PA7	I/O	FT_fa	-	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, OCTOSPI1_IO2, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC12_IN12
-	-	24	G4	M3	-	G4	-	M3	-	-	-	24	33	M3	44	PC4	I/O	FT_a	-	USART3_TX, OCTOSPI1_IO7, EVENTOUT	COMP1_INM, ADC12_IN13
-	-	-	-	J3	-	-	-	J3	-	-	-	25	34	J3	45	PC5	I/O	FT_a	-	SAI1_D3, USART3_RX, EVENTOUT	ADC12_IN14, WKUP5, TAMP_IN4/TAMP_OUT5, COMP1_INP
18	18	25	J6	M4	24	J6	32	M4	43	18	18	26	35	M4	46	PB0	I/O	TT_a	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, OCTOSPI1_IO1, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC12_IN15

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
19	19	26	H5	L4	25	H5	33	L4	44	19	19	27	36	L4	47	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS/USART3_DE, LPUART1_RTS/LPUART1_DE, OCTOSPI1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
20	20	27	J5	K4	26	J5	34	K4	45	20	20	28	37	K4	48	PB2	I/O	FT	-	LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, OCTOSPI1_DQS, UCPD1_FRSCC1, EVENTOUT	RTC_OUT2, COMP1_INP
-	-	-	-	K5	-	-	-	K5	46	-	-	-	-	K5	49	PF11	I/O	FT	-	OCTOSPI1_NCLK, EVENTOUT	-
-	-	-	-	L5	-	-	-	L5	47	-	-	-	-	L5	50	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	-	J9	-	-	J9	-	-	48	-	-	-	-	-	51	VSS	S	-	-	-	-
-	-	-	J8	-	-	J8	-	-	49	-	-	-	-	-	52	VDD	S	-	-	-	-
-	-	-	-	M5	-	-	-	M5	50	-	-	-	-	M5	53	PF13	I/O	FT	-	I2C4_SMBA, FMC_A7, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	J5	-	-	-	J5	51	-	-	-	-	J5	54	PF14	I/O	FT_f	-	I2C4_SCL, TSC_G8_IO1, FMC_A8, EVENTOUT	-
-	-	-	-	L6	-	-	-	L6	52	-	-	-	-	L6	55	PF15	I/O	FT_f	-	I2C4_SDA, TSC_G8_IO2, FMC_A9, EVENTOUT	-
-	-	-	-	M6	-	-	-	M6	53	-	-	-	-	M6	56	PG0	I/O	FT	-	TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	-	-	-	K6	-	-	-	K6	54	-	-	-	-	K6	57	PG1	I/O	FT	-	TSC_G8_IO4, FMC_A11, EVENTOUT	-
-	-	-	-	K7	-	-	35	K7	55	-	-	-	38	K7	58	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT	-
-	-	-	-	J6	-	-	36	J6	56	-	-	-	39	J6	59	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT	-
-	-	-	-	M7	-	-	37	M7	57	-	-	-	40	M7	60	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, OCTOSPI1_NCLK, FMC_D6, SAI1_FS_B, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	L10	-	-	-	-	58	-	-	-	-	L10	61	VSS	S	-	-	-	-
-	-	-	H1	J4	-	H1	-	J4	59	-	-	-	-	J4	62	VDD	S	-	-	-	-
-	-	-	-	J7	-	-	38	J7	60	-	-	-	41	J7	63	PE10	I/O	FT	-	TIM1_CH2N, TSC_G5_IO1, OCTOSPI1_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	-	-	-	L7	-	-	39	L7	61	-	-	-	42	L7	64	PE11	I/O	FT	-	TIM1_CH2, TSC_G5_IO2, OCTOSPI1_NCS, FMC_D8, EVENTOUT	-
-	-	-	-	J8	-	-	40	J8	62	-	-	-	43	J8	65	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, TSC_G5_IO3, OCTOSPI1_IO0, FMC_D9, EVENTOUT	-
-	-	-	J4	M8	-	-	41	M8	63	-	-	-	44	M8	66	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, TSC_G5_IO4, OCTOSPI1_IO1, FMC_D10, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	H4	K8	-	-	42	K8	64	-	-	-	45	K8	67	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, OCTOSPI1_IO2, FMC_D11, EVENTOUT	-
-	-	-	H3	L8	-	-	43	L8	65	-	-	-	46	L8	68	PE15	I/O	FT	-	TIM1_BKIN, SPI1_MOSI, OCTOSPI1_IO3, FMC_D12, EVENTOUT	-
21	21	28	J3	K9	27	J4	44	K9	66	21	21	29	47	K9	69	PB10	I/O	FT_f	-	TIM2_CH3, LPTIM3_OUT, I2C4_SCL, I2C2_SCL, SPI2_SCK, USART3_TX, LPUART1_RX, TSC_SYNC, OCTOSPI1_CLK, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	29	J2	L9	-	H4	45	L9	67	22	22	30	48	L9	70	PB11	I/O	FT_f	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, USART3_RX, LPUART1_TX, OCTOSPI1_NCS, COMP2_OUT, EVENTOUT	-
-	-	-	-	-	28	J3	46	M9	68	-	-	-	-	-	-	VDDSMPS	S	-	-	-	-
-	-	-	-	-	29	H3	47	M10	69	-	-	-	-	-	-	VLXSMPS	S	-	-	-	-
-	-	-	-	-	30	J2	48	L10	70	-	-	-	-	-	-	VSSSMPS	S	-	-	-	-
22	22	30	J1	M11	-	-	-	-	-	-	-	-	-	-	-	VDD12_1	S	-	-	-	-
23	23	31	B2	E9	31	B2	49	E9	71	23	23	31	49	E9	71	VSS	S	-	-	-	-
-	-	-	-	-	32	J1	50	M11	72	-	-	-	-	-	-	V15SMPS_1	S	-	-	-	-
24	24	32	A1	D4	33	A1	51	D4	73	24	24	32	50	D4	72	VDD	S	-	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
25	25	33	G2	L11	-	G2	-	L11	-	25	25	33	51	L11	73	PB12	I/O	FT	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS, DFSDM1_DATIN1, USART3_CK, LPUART1_RTS/LPUART1_DE, TSC_G1_IO1, OCTOSPI1_NCLK, SAI2_FS_A, TIM15_BKIN, EVENTOUT	-
26	26	34	F2	K10	34	F2	52	K10	74	26	26	34	52	K10	74	PB13	I/O	FT_f	-	TIM1_CH1N, LPTIM3_IN1, I2C2_SCL, SPI2_SCK, DFSDM1_CKIN1, USART3_CTS/USART3_NSS, LPUART1_CTS, TSC_G1_IO2, UCPD1_FRSCC2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
27	27	35	G1	K11	35	G1	53	K11	75	27	27	35	53	K11	75	PB14	I/O	FT_fd	-	TIM1_CH2N, LPTIM3_ETR, TIM8_CH2N, I2C2_SDA, SPI2_MISO, DFSDM1_DATIN2, USART3_RTS/USART3_DE, TSC_G1_IO3, SAI2_MCLK_A, TIM15_CH1, EVENTOUT	UCPD1_DB2
28	28	36	F1	K12	36	F1	54	K12	76	28	28	36	54	K12	76	PB15	I/O	FT_c	-	RTC_REFIN, TIM1_CH3N, TIM8_CH3N, SPI2_MOSI, DFSDM1_CKIN2, SAI2_SD_A, TIM15_CH2, EVENTOUT	UCPD1_CC2
-	-	-	-	L12	-	-	55	L12	77	-	-	-	55	L12	77	PD8	I/O	FT	-	USART3_TX, FMC_D13, EVENTOUT	-
-	-	-	-	J10	-	-	56	J10	78	-	-	-	56	J10	78	PD9	I/O	FT	-	USART3_RX, FMC_D14, SAI2_MCLK_A, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	M12	-	-	57	M12	79	-	-	-	57	M12	79	PD10	I/O	FT	-	USART3_CK, TSC_G6_IO1, FMC_D15, SAI2_SCK_A, EVENTOUT	-
-	-	-	-	J11	-	-	58	J11	80	-	-	-	58	J11	80	PD11	I/O	FT	-	I2C4_SMBA, USART3_CTS/USART3_NSS, TSC_G6_IO2, FMC_A16, SAI2_SD_A, LPTIM2_ETR, EVENTOUT	-
-	-	-	-	J12	-	-	59	J12	81	-	-	-	59	J12	81	PD12	I/O	FT_f	-	TIM4_CH1, I2C4_SCL, USART3_RTS/USART3_DE, TSC_G6_IO3, FMC_A17, SAI2_FS_A, LPTIM2_IN1, EVENTOUT	-
-	-	-	-	H11	-	-	60	H11	82	-	-	-	60	H11	82	PD13	I/O	FT_f	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	-	-	-	-	83	-	-	-	-	-	83	VSS	S	-	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	-	-	-	-	-	84	-	-	-	-	-	84	VDD	S	-	-	-	-
-	-	-	-	H10	-	-	61	H10	85	-	-	-	61	H10	85	PD14	I/O	FT	-	TIM4_CH3, FMC_D0, EVENTOUT	-
-	-	-	-	H12	-	-	62	H12	86	-	-	-	62	H12	86	PD15	I/O	FT	-	TIM4_CH4, FMC_D1, EVENTOUT	-
-	-	-	-	G10	-	-	-	G10	87	-	-	-	-	G10	87	PG2	I/O	FT_s	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	-	-	-	G11	-	-	-	G11	88	-	-	-	-	G11	88	PG3	I/O	FT_s	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	-	-	-	G9	-	-	-	G9	89	-	-	-	-	G9	89	PG4	I/O	FT_s	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	G12	-	-	-	G12	90	-	-	-	-	G12	90	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	F9	-	-	-	F9	91	-	-	-	-	F9	91	PG6	I/O	FT_s	-	OCTOSPI1_DQS, I2C3_SMBA, LPUART1_RTS/LPUART1_DE, UCPD1_FRSCC1, EVENTOUT	-
-	-	-	-	F10	-	-	-	F10	92	-	-	-	-	F10	92	PG7	I/O	FT_fs	-	SAI1_CK1, I2C3_SCL, DFSDM1_CKOUT, LPUART1_TX, UCPD1_FRSCC2, FMC_INT, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	F12	-	-	-	F12	93	-	-	-	-	F12	93	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	94	-	-	-	-	-	94	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	95	-	-	-	-	-	95	VDDIO2	S	-	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	37	E1	F11	37	E1	63	F11	96	-	-	37	63	F11	96	PC6	I/O	FT	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, SDMMC1_D0DIR, TSC_G4_IO1, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
-	-	38	E2	E10	38	E2	64	E10	97	-	-	38	64	E10	97	PC7	I/O	FT	-	TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, SDMMC1_D123DIR, TSC_G4_IO2, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
-	-	39	F3	E12	39	F3	65	E12	98	-	-	39	65	E12	98	PC8	I/O	FT	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, SDMMC1_D0, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	40	G3	E11	40	G3	66	E11	99	-	-	40	66	E11	99	PC9	I/O	FT_f	-	TRACED0, TIM8_BKIN2, TIM3_CH4, TIM8_CH4, TSC_G4_IO4, USB_NOE, SDMMC1_D1, SAI2_EXTCLK, EVENTOUT	-
29	29	41	F4	D12	41	F4	67	D12	100	29	29	41	67	D12	100	PA8	I/O	FT_f	-	MCO, TIM1_CH1, SAI1_CK2, USART1_CK, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
30	30	42	D1	D10	42	D1	68	D10	101	30	30	42	68	D10	101	PA9	I/O	FT_fu	-	TIM1_CH2, SPI2_SCK, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
31	31	43	E3	D11	43	E3	69	D11	102	31	31	43	69	D11	102	PA10	I/O	FT_fu	-	TIM1_CH3, SAI1_D1, USART1_RX, CRS_SYNC, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
32	32	44	C1	C12	44	C1	70	C12	103	32	32	44	70	C12	103	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS/USART1_NSS, FDCAN1_RX, USB_DM, EVENTOUT	-
33	33	45	C2	B12	45	C2	71	B12	104	33	33	45	71	B12	104	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS/USART1_DE, FDCAN1_TX, USB_DP, EVENTOUT	-
34	34	46	D2	C10	46	D2	72	C10	105	34	34	46	72	C10	105	PA13 (JTMS/SWDIO)	I/O	FT	(3)	JTMS/SWDIO, IR_OUT, USB_NOE, SAI1_SD_B, EVENTOUT	-
-	-	47	-	-	47	-	-	-	-	-	-	47	-	-	-	VSS	S	-	-	-	-
-	-	48	B1	A12	48	B1	73	A12	106	-	-	48	73	A12	106	VDDUSB	S	-	-	-	-
35	35	-	B5	H4	-	B5	74	H4	107	35	35	-	74	H4	107	VSS	S	-	-	-	-
36	36	-	A9	D9	-	A9	75	D9	108	36	36	-	75	D9	108	VDD	S	-	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
37	37	49	D3	C11	49	D3	76	C11	109	37	37	49	76	C11	109	PA14 (JTCK /SWC LK)	I/O	FT	(3)	JTCK/SWCLK, LPTIM1_OUT, I2C1_SMBA, I2C4_SMBA, SAI1_FS_B, EVENTOUT	-
38	38	50	E4	A11	50	E4	77	A11	110	38	38	50	77	A11	110	PA15 (JTDI)	I/O	FT _c	(3)	JTDI, TIM2_CH1, TIM2_ETR, USART2_RX, SPI1_NSS, SPI3_NSS, USART3_RTS/USART 3_DE, UART4_RTS/UART4_ DE, SAI2_FS_B, EVENTOUT	UCPD1_CC1
-	-	51	A2	B11	51	A2	78	B11	111	-	-	51	78	B11	111	PC10	I/O	FT	-	TRACED1, LPTIM3_ETR, SPI3_SCK, USART3_TX, UART4_TX, TSC_G3_IO2, SDMMC1_D2, SAI2_SCK_B, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	52	C3	A10	52	C3	79	A10	112	-	-	52	79	A10	112	PC11	I/O	FT	-	LPTIM3_IN1, OCTOSPI1_NCS, SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, UCPD1_FRSCC2, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
-	-	53	B3	B10	53	B3	80	B10	113	-	-	53	80	B10	113	PC12	I/O	FT	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
-	-	-	-	C9	-	-	81	C9	114	-	-	-	81	C9	114	PD0	I/O	FT	-	SPI2_NSS, FDCAN1_RX, FMC_D2, EVENTOUT	-
-	-	-	-	B9	-	-	82	B9	115	-	-	-	82	B9	115	PD1	I/O	FT	-	SPI2_SCK, FDCAN1_TX, FMC_D3, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	A3	A9	54	A3	83	A9	116	-	-	54	83	A9	116	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS/USART3_DE, UART5_RX, TSC_SYNC, SDMMC1_CMD, EVENTOUT	-
-	-	-	-	C8	-	-	84	C8	117	-	-	-	84	C8	117	PD3	I/O	FT	-	SPI2_SCK, SPI2_MISO, DFSDM1_DATIN0, USART2_CTS/USART2_NSS, FMC_CLK, EVENTOUT	-
-	-	-	-	B8	-	-	85	B8	118	-	-	-	85	B8	118	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS/USART2_DE, OCTOSPI1_IO4, FMC_NOE, EVENTOUT	-
-	-	-	-	A8	-	-	86	A8	119	-	-	-	86	A8	119	PD5	I/O	FT	-	USART2_TX, OCTOSPI1_IO5, FMC_NWE, EVENTOUT	-
-	-	-	-	-	-	-	-	-	120	-	-	-	-	-	120	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	121	-	-	-	-	-	121	VDD	S	-	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	-	A7	-	-	87	A7	122	-	-	-	87	A7	122	PD6	I/O	FT	-	SAI1_D1, SPI3_MOSI, DFSDM1_DATIN1, USART2_RX, OCTOSPI1_IO6, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
-	-	-	-	D7	-	-	88	D7	123	-	-	-	88	D7	123	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, OCTOSPI1_IO7, FMC_NCE/FMC_NE1, EVENTOUT	-
-	-	-	D4	B7	-	D4	-	B7	124	-	-	-	-	B7	124	PG9	I/O	FT_s	-	SPI3_SCK, USART1_TX, FMC_NCE/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
-	-	-	C4	C7	-	C4	-	C7	125	-	-	-	-	C7	125	PG10	I/O	FT_s	-	LPTIM1_IN1, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	E5	-	-	E5	-	-	-	-	-	-	-	M11	126	PG11	I/O	FT_s	-	LPTIM1_IN2, OCTOSPI1_IO5, SPI3_MOSI, USART1_CTS/USART1_NSS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	-	-	B4	A6	-	B4	-	A6	126	-	-	-	-	A6	127	PG12	I/O	FT_s	-	LPTIM1_ETR, SPI3_NSS, USART1_RTS/USART1_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	-	-	A4	M10	-	A4	-	-	127	-	-	-	-	M10	128	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, FMC_A24, EVENTOUT	-
-	-	-	D5	M9	-	D5	-	-	128	-	-	-	-	M9	129	PG14	I/O	FT_fs	-	I2C1_SCL, FMC_A25, EVENTOUT	-
-	-	-	B8	H9	-	B8	-	H9	129	-	-	-	-	H9	130	VSS	S	-	-	-	-
-	-	-	A5	D8	-	A5	-	D8	130	-	-	-	-	D8	131	VDDIO2	S	-	-	-	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	-	C5	-	-	C5	-	-	131	-	-	-	-	B4	132	PG15	I/O	FT_s	-	LPTIM1_OUT, I2C1_SMBA, EVENTOUT	-
39	39	54	E6	C6	55	E6	89	C6	132	39	39	55	89	C6	133	PB3 (JTDO/TRACESWO)	I/O	FT_a	-	JTDO/TRACESWO, TIM2_CH2, SPI1_SCK, SPI3_SCK, USART1_RTS/USART1_DE, CRS_SYNC, SAI1_SCK_B, EVENTOUT	COMP2_INM
40	40	55	B6	B6	56	B6	90	B6	133	40	40	56	90	B6	134	PB4 (NJTRST)	I/O	FT_fa	(3)	NJTRST, TIM3_CH1, I2C3_SDA, SPI1_MISO, SPI3_MISO, USART1_CTS/USART1_NSS, UART5_RTS/UART5_DE, TSC_G2_IO1, SAI1_MCLK_B, TIM17_BKIN, EVENTOUT	COMP2_INP

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
41	41	56	A6	D6	57	A6	91	D6	134	41	41	57	91	D6	135	PB5	I/O	FT_d	-	LPTIM1_IN1, TIM3_CH2, OCTOSPI1_NCLK, I2C1_SMBA, SPI1_MOSI, SPI3_MOSI, USART1_CK, UART5_CTS/UART5_NSS, TSC_G2_IO2, COMP2_OUT, SAI1_SD_B, TIM16_BKIN, EVENTOUT	UCPD1_DB1
42	42	57	C6	A5	58	C6	92	A5	135	42	42	58	92	A5	136	PB6	I/O	FT_fa	-	LPTIM1_ETR, TIM4_CH1, TIM8_BKIN2, I2C1_SCL, I2C4_SCL, USART1_TX, TSC_G2_IO3, SAI1_FS_B, TIM16_CH1N, EVENTOUT	COMP2_INP

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
43	43	58	D6	D5	59	D6	93	D5	136	43	43	59	93	D5	137	PB7	I/O	FT_fa	-	LPTIM1_IN2, TIM4_CH2, TIM8_BKIN, I2C1_SDA, I2C4_SDA, USART1_RX, UART4_CTS, TSC_G2_IO4, FMC_NL, TIM17_CH1N, EVENTOUT	COMP2_INM, PVD_IN
44	44	59	D7	B5	60	D7	94	B5	137	44	44	60	94	B5	138	PH3-BOOT0	I/O	FT	-	EVENTOUT	-
45	45	60	C7	C5	61	C7	95	C5	138	45	45	61	95	C5	139	PB8	I/O	FT_f	-	TIM4_CH3, SAI1_CK1, I2C1_SCL, DFSDM1_CKOUT, SDMMC1_CKIN, FDCAN1_RX, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-

Table 20. STM32L552xx pin definitions (continued)

Pin Number																Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L552xxxxP					STM32L552xxxxQ					STM32L552xx											
UFQFPN48_Ext-SMPS	LQFP48_Ext-SMPS	LQFP64_Ext-SMPS	WLCSP81_Ext-SMPS	UFBGA132_ExtSMPS	LQFP64_SMPS	WLCSP81_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144						
-	-	61	A7	A4	-	A7	96	A4	139	46	46	62	96	A4	140	PB9	I/O	FT_f	-	IR_OUT, TIM4_CH4, SAI1_D2, I2C1_SDA, SPI2_NSS, SDMMC1_CDIR, FDCAN1_TX, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	-	-	-	C4	-	-	97	C4	140	-	-	-	97	C4	141	PE0	I/O	FT	-	TIM4_ETR, FMC_NBL0, TIM16_CH1, EVENTOUT	-
-	-	-	-	A3	-	-	-	A3	141	-	-	-	98	A3	142	PE1	I/O	FT	-	FMC_NBL1, TIM17_CH1, EVENTOUT	-
46	46	62	A8	B4	-	-	-	-	-	-	-	-	-	-	-	VDD12_2	S	-	-	-	-
47	47	63	E8	E4	62	E8	98	E4	142	47	47	63	99	E4	143	VSS	S	-	-	-	-
-	-	-	-	-	63	A8	99	B4	143	-	-	-	-	-	-	V15SMPS_2	S	-	-	-	-
48	48	64	F9	J9	64	F9	100	J9	144	48	48	64	100	J9	144	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0438 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 21. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS_NSS
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	SAI1_CK1	-	-	-	USART2_RX
	PA4	-	-	-	OCTOSPI1_NCS	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	USART3_CTS_NSS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	SAI1_CK2	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	-	-	-	USART1_TX
	PA10	-	TIM1_CH3	-	SAI1_D1	-	-	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS_NSS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_DE

Table 21. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	SPI1_NSS	-	USART3_CK
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	DFSDM1_DATIN0	USART3_RTS_DE
	PB2	-	LPTIM1_OUT	-	-	I2C3_SMBA	-	DFSDM1_CKIN0	-
	PB3	JTDO/TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	USART1_RTS_DE
	PB4	NJTRST	-	TIM3_CH1	-	I2C3_SDA	SPI1_MISO	SPI3_MISO	USART1_CTS_NSS
	PB5	-	LPTIM1_IN1	TIM3_CH2	OCTOSPI1_NCLK	I2C1_SMBA	SPI1_MOSI	SPI3_MOSI	USART1_CK
	PB6	-	LPTIM1_ETR	TIM4_CH1	TIM8_BKIN2	I2C1_SCL	I2C4_SCL	-	USART1_TX
	PB7	-	LPTIM1_IN2	TIM4_CH2	TIM8_BKIN	I2C1_SDA	I2C4_SDA	-	USART1_RX
	PB8	-	-	TIM4_CH3	SAI1_CK1	I2C1_SCL	DFSDM1_CKOUT	-	-
	PB9	-	IR_OUT	TIM4_CH4	SAI1_D2	I2C1_SDA	SPI2_NSS	-	-
	PB10	-	TIM2_CH3	LPTIM3_OUT	I2C4_SCL	I2C2_SCL	SPI2_SCK	-	USART3_TX
	PB11	-	TIM2_CH4	-	I2C4_SDA	I2C2_SDA	-	-	USART3_RX
	PB12	-	TIM1_BKIN	-	TIM1_BKIN	I2C2_SMBA	SPI2_NSS	DFSDM1_DATIN1	USART3_CK
	PB13	-	TIM1_CH1N	LPTIM3_IN1	-	I2C2_SCL	SPI2_SCK	DFSDM1_CKIN1	USART3_CTS_NSS
	PB14	-	TIM1_CH2N	LPTIM3_ETR	TIM8_CH2N	I2C2_SDA	SPI2_MISO	DFSDM1_DATIN2	USART3_RTS_DE
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	-	SPI2_MOSI	DFSDM1_CKIN2	-

Table 21. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port C	PC0	-	LPTIM1_IN1	-	OCTOSPI1_IO7	I2C3_SCL	-	-	-
	PC1	TRACED0	LPTIM1_OUT	-	SPI2_MOSI	I2C3_SDA	-	-	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_CKOUT	-
	PC3	-	LPTIM1_ETR	LPTIM3_OUT	SAI1_D1	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	SAI1_D3	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	TRACED0	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	-	-	-	-
	PC10	TRACED1	-	LPTIM3_ETR	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	LPTIM3_IN1	-	-	OCTOSPI1_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 21. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port D	PD0	-	-	-	-	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_RTS_DE
	PD3	-	-	-	SPI2_SCK	-	SPI2_MISO	DFSDM1_DATIN0	USART2_CTS_NSS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM1_CKIN0	USART2_RTS_DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	SAI1_D1	-	SPI3_MOSI	DFSDM1_DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM1_CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS_NSS
	PD12	-	-	TIM4_CH1	-	I2C4_SCL	-	-	USART3_RTS_DE
	PD13	-	-	TIM4_CH2	-	I2C4_SDA	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

Table 21. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	SAI1_CK1	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	OCTOSPI1_DQS	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	SAI1_D2	-	-	DFSDM1_DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	SAI1_CK2	-	-	DFSDM1_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	SAI1_D1	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	-	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN	-	SPI1_MOSI	-	-

Table 21. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	LPTIM3_IN1	-	-	-	-	-
	PF4	-	-	LPTIM3_ETR	-	-	-	-	-
	PF5	-	-	LPTIM3_OUT	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	OCTOSPI1_CLK	-	-	DFSDM1_CKOUT	-
	PF11	-	-	-	OCTOSPI1_NCLK	-	-	-	-
	PF12	-	-	-	-	-	-	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	-	-
	PF14	-	-	-	-	I2C4_SCL	-	-	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 21. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port G	PG0	-	-	-	-	-	-	-	-
	PG1	-	-	-	-	-	-	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPI1_DQS	I2C3_SMBA	-	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	-	DFSDM1_CKOUT	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	-	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	-	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPI1_IO5	-	-	SPI3_MOSI	USART1_CTS_NSS
	PG12	-	LPTIM1_ETR	-	-	-	-	SPI3_NSS	USART1_RTS_DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	-	-	-

Table 21. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5/LPTIM3	SPI2/SAI1/I2C4/USART2/TIM1/8/OCTOSPI1	I2C1/2/3/4	SPI1/2/3/I2C4/DFSDM1/OCTOSPI1	SPI3/I2C3/DFSDM1/COMP1/	USART1/2/3
Port H - -	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH3	-	-	-	-	-	-	-	-

1. Refer to *Table 22* for AF8 to AF15.

Table 22. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	OCTOSPI1_DQS	-	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	OCTOSPI1_NCS	UCPD1_FRSCC1	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	OCTOSPI1_CLK	-	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	-	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS_NSS	-	OCTOSPI1_IO3	-	TIM1_BKIN	TIM8_BKIN	TIM16_CH1	EVENTOUT
	PA7	-	-	OCTOSPI1_IO2	-	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	-	-	-	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	-	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	CRS_SYNC	-	-	SAI1_SD_A	TIM17_BKIN	EVENTOUT
	PA11	-	FDCAN1_RX	USB_DM	-	TIM1_BKIN2	-	-	EVENTOUT
	PA12	-	FDCAN1_TX	USB_DP	-	-	-	-	EVENTOUT
	PA13	-	-	USB_NOE	-	-	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	-	-	-	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_DE	-	-	-	-	SAI2_FS_B	-	EVENTOUT

Table 22. Alternate function AF8 to AF15[1]

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port B	PB0	-	-	OCTOSPI1_IO1	-	COMP1_OUT	SAI1_EXTCLK	-	EVENTOUT
	PB1	LPUART1_RTS_DE	-	OCTOSPI1_IO0	-	-	-	LPTIM2_IN1	EVENTOUT
	PB2	-	-	OCTOSPI1_DQS	UCPD1_FRSCC1	-	-	-	EVENTOUT
	PB3	-	-	CRS_SYNC	-	-	SAI1_SCK_B	-	EVENTOUT
	PB4	UART5_RTS_DE	TSC_G2_IO1	-	-	-	SAI1_MCLK_B	TIM17_BKIN	EVENTOUT
	PB5	UART5_CTS_NSS	TSC_G2_IO2	-	-	COMP2_OUT	SAI1_SD_B	TIM16_BKIN	EVENTOUT
	PB6	-	TSC_G2_IO3	-	-	TIM8_BKIN2	SAI1_FS_B	TIM16_CH1N	EVENTOUT
	PB7	UART4_CTS_NSS	TSC_G2_IO4	-	-	FMC_NL	TIM8_BKIN	TIM17_CH1N	EVENTOUT
	PB8	SDMMC1_CKIN	FDCAN1_RX	-	-	SDMMC1_D4	SAI1_MCLK_A	TIM16_CH1	EVENTOUT
	PB9	SDMMC1_CDIR	FDCAN1_TX	-	-	SDMMC1_D5	SAI1_FS_A	TIM17_CH1	EVENTOUT
	PB10	LPUART1_RX	TSC_SYNC	OCTOSPI1_CLK	-	COMP1_OUT	SAI1_SCK_A	-	EVENTOUT
	PB11	LPUART1_TX	-	OCTOSPI1_NCS	-	COMP2_OUT	-	-	EVENTOUT
	PB12	LPUART1_RTS_DE	TSC_G1_IO1	OCTOSPI1_NCLK	-	-	SAI2_FS_A	TIM15_BKIN	EVENTOUT
	PB13	LPUART1_CTS_NSS	TSC_G1_IO2	-	UCPD1_FRSCC2	-	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PB14	-	TSC_G1_IO3	-	-	-	SAI2_MCLK_A	TIM15_CH1	EVENTOUT
	PB15	-	-	-	-	-	SAI2_SD_A	TIM15_CH2	EVENTOUT

Table 22. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port C	PC0	LPUART1_RX	-	-	-	SDMMC1_D5	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PC1	LPUART1_TX	-	OCTOSPI1_IO4	-	-	SAI1_SD_A	-	EVENTOUT
	PC2	-	TSC_G3_IO1	OCTOSPI1_IO5	-	-	-	-	EVENTOUT
	PC3	-	TSC_G1_IO4	OCTOSPI1_IO6	-	-	SAI1_SD_A	LPTIM2_ETR	EVENTOUT
	PC4	-	-	OCTOSPI1_IO7	-	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	EVENTOUT
	PC6	SDMMC1_D0DIR	TSC_G4_IO1	-	-	SDMMC1_D6	SAI2_MCLK_A	-	EVENTOUT
	PC7	SDMMC1_D123DIR	TSC_G4_IO2	-	-	SDMMC1_D7	SAI2_MCLK_B	-	EVENTOUT
	PC8	-	TSC_G4_IO3	-	-	SDMMC1_D0	-	-	EVENTOUT
	PC9	-	TSC_G4_IO4	USB_NOE	-	SDMMC1_D1	SAI2_EXTCLK	TIM8_BKIN2	EVENTOUT
	PC10	UART4_TX	TSC_G3_IO2	-	-	SDMMC1_D2	SAI2_SCK_B	-	EVENTOUT
	PC11	UART4_RX	TSC_G3_IO3	-	UCPD1_FRSCC2	SDMMC1_D3	SAI2_MCLK_B	-	EVENTOUT
	PC12	UART5_TX	TSC_G3_IO4	-	-	SDMMC1_CK	SAI2_SD_B	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT

Table 22. Alternate function AF8 to AF15[1]

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port D	PD0	-	FDCAN1_RX	-	-	FMC_D2	-	-	EVENTOUT
	PD1	-	FDCAN1_TX	-	-	FMC_D3	-	-	EVENTOUT
	PD2	UART5_RX	TSC_SYNC	-	-	SDMMC1_CMD	-	-	EVENTOUT
	PD3	-	-	-	-	FMC_CLK	-	-	EVENTOUT
	PD4	-	-	OCTOSPI1_IO4	-	FMC_NOE	-	-	EVENTOUT
	PD5	-	-	OCTOSPI1_IO5	-	FMC_NWE	-	-	EVENTOUT
	PD6	-	-	OCTOSPI1_IO6	-	FMC_NWAIT	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	OCTOSPI1_IO7	-	FMC_NCE/FMC_NE1	-	-	EVENTOUT
	PD8	-	-	-	-	FMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	FMC_D14	SAI2_MCLK_A	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	-	FMC_D15	SAI2_SCK_A	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	-	FMC_A16	SAI2_SD_A	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	-	FMC_A17	SAI2_FS_A	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	-	FMC_A18	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	-	FMC_D0	-	-	EVENTOUT
	PD15	-	-	-	-	FMC_D1	-	-	EVENTOUT

Table 22. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port E	PE0	-	-	-	-	FMC_NBL0	-	TIM16_CH1	EVENTOUT
	PE1	-	-	-	-	FMC_NBL1	-	TIM17_CH1	EVENTOUT
	PE2	-	TSC_G7_IO1	-	-	FMC_A23	SAI1_MCLK_A	-	EVENTOUT
	PE3	-	TSC_G7_IO2	-	-	FMC_A19	SAI1_SD_B	-	EVENTOUT
	PE4	-	TSC_G7_IO3	-	-	FMC_A20	SAI1_FS_A	-	EVENTOUT
	PE5	-	TSC_G7_IO4	-	-	FMC_A21	SAI1_SCK_A	-	EVENTOUT
	PE6	-	-	-	-	FMC_A22	SAI1_SD_A	-	EVENTOUT
	PE7	-	-	-	-	FMC_D4	SAI1_SD_B	-	EVENTOUT
	PE8	-	-	-	-	FMC_D5	SAI1_SCK_B	-	EVENTOUT
	PE9	-	-	OCTOSPI1_NCLK	-	FMC_D6	SAI1_FS_B	-	EVENTOUT
	PE10	-	TSC_G5_IO1	OCTOSPI1_CLK	-	FMC_D7	SAI1_MCLK_B	-	EVENTOUT
	PE11	-	TSC_G5_IO2	OCTOSPI1_NCS	-	FMC_D8	-	-	EVENTOUT
	PE12	-	TSC_G5_IO3	OCTOSPI1_IO0	-	FMC_D9	-	-	EVENTOUT
	PE13	-	TSC_G5_IO4	OCTOSPI1_IO1	-	FMC_D10	-	-	EVENTOUT
	PE14	-	-	OCTOSPI1_IO2	-	FMC_D11	-	-	EVENTOUT
	PE15	-	-	OCTOSPI1_IO3	-	FMC_D12	-	-	EVENTOUT

Table 22. Alternate function AF8 to AF15[1]

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	OCTOSPI1_IO3	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	OCTOSPI1_IO2	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	OCTOSPI1_IO0	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	OCTOSPI1_IO1	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	-	-	-	SAI1_D3	TIM15_CH2	EVENTOUT
	PF11	-	-	-	-	-	-	-	EVENTOUT
	PF12	-	-	-	-	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	-	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	-	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	-	FMC_A9	-	-	EVENTOUT

Table 22. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_CTS_NSS	-	-	-	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_RTS_DE	-	-	UCPD1_FRSCC1	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	UCPD1_FRSCC2	FMC_INT	SAI1_MCLK_A	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	FMC_NCE/FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	-	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	-	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	-	FMC_A25	-	-	EVENTOUT
	PG15	-	-	-	-	-	-	-	EVENTOUT

Table 22. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/LPUART1/SDMMC1	FDCAN1/TSC	USB/OCTOSPI1	UCPD1	SDMMC1/COMP1/2/TIM1/8/FMC	SAI1/2/TIM8	TIM2/8/15/16/17/LPTIM2	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT

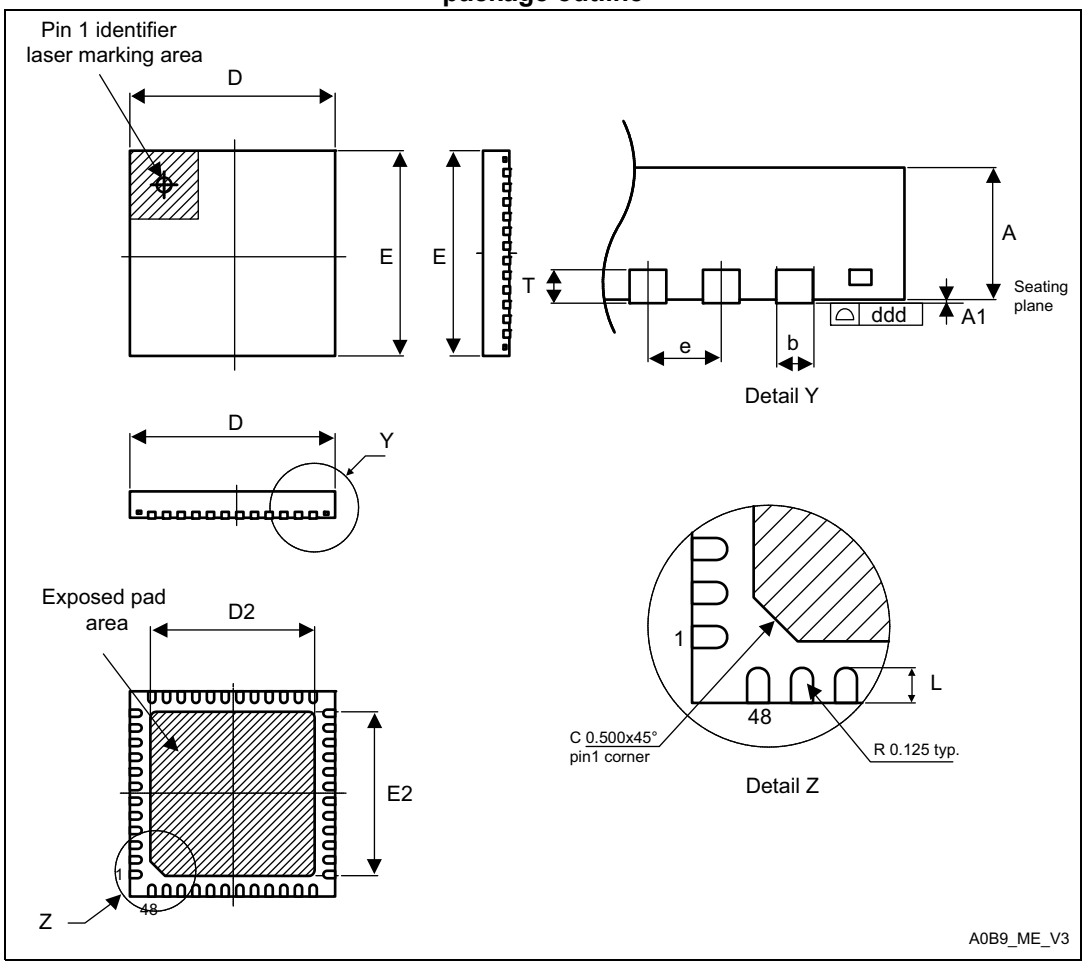
1. Refer to *Table 21* for AF0 to AF7.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 UFQFPN48 package information

Figure 26. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



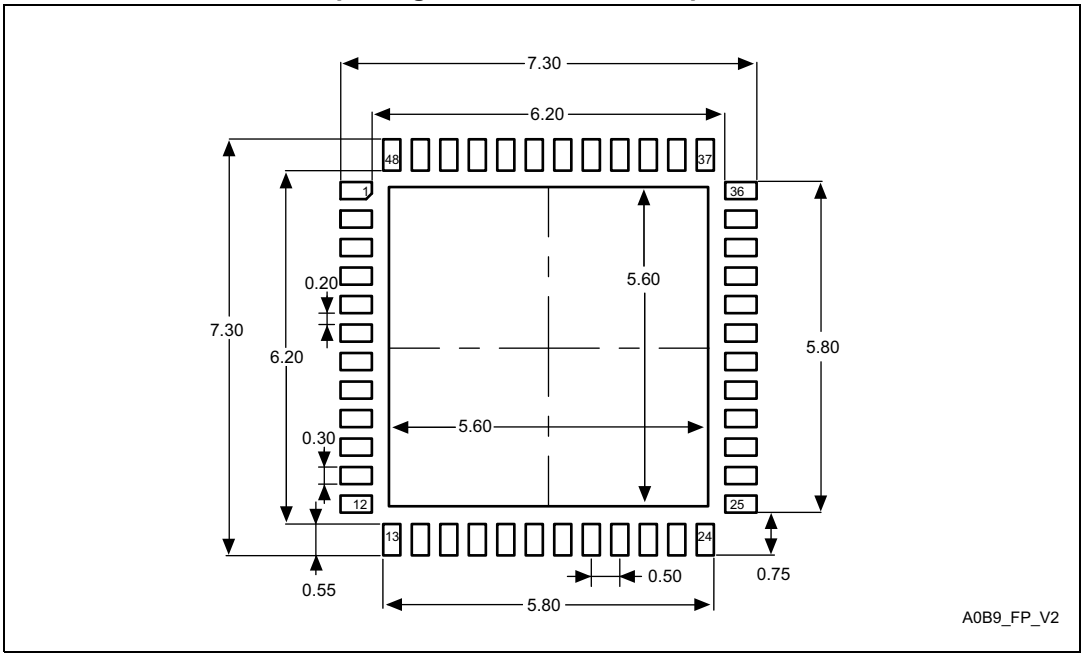
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 23. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 27. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

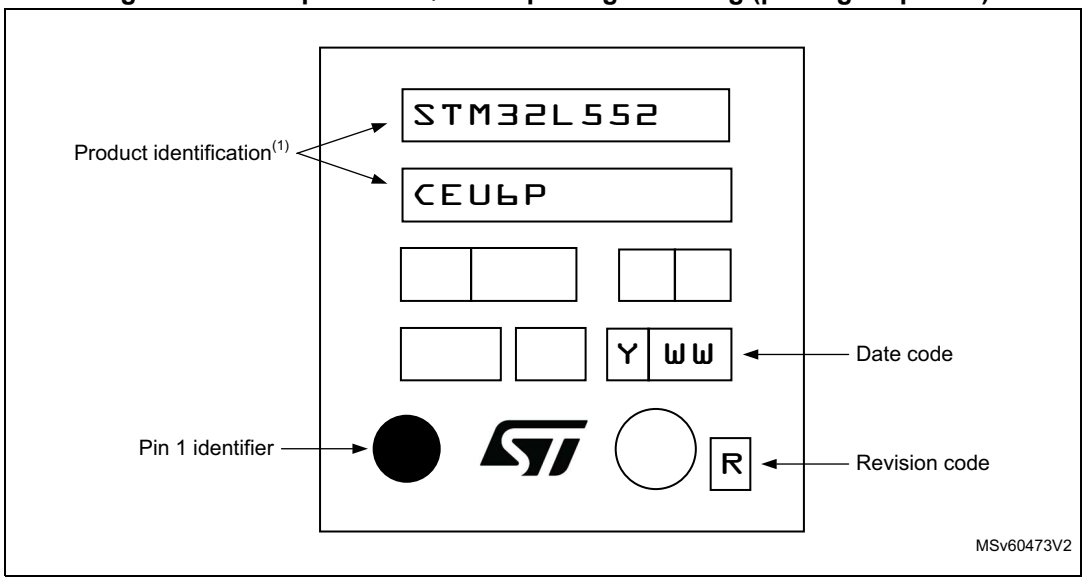
Device marking for UFQFPN48 (7 x 7)

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

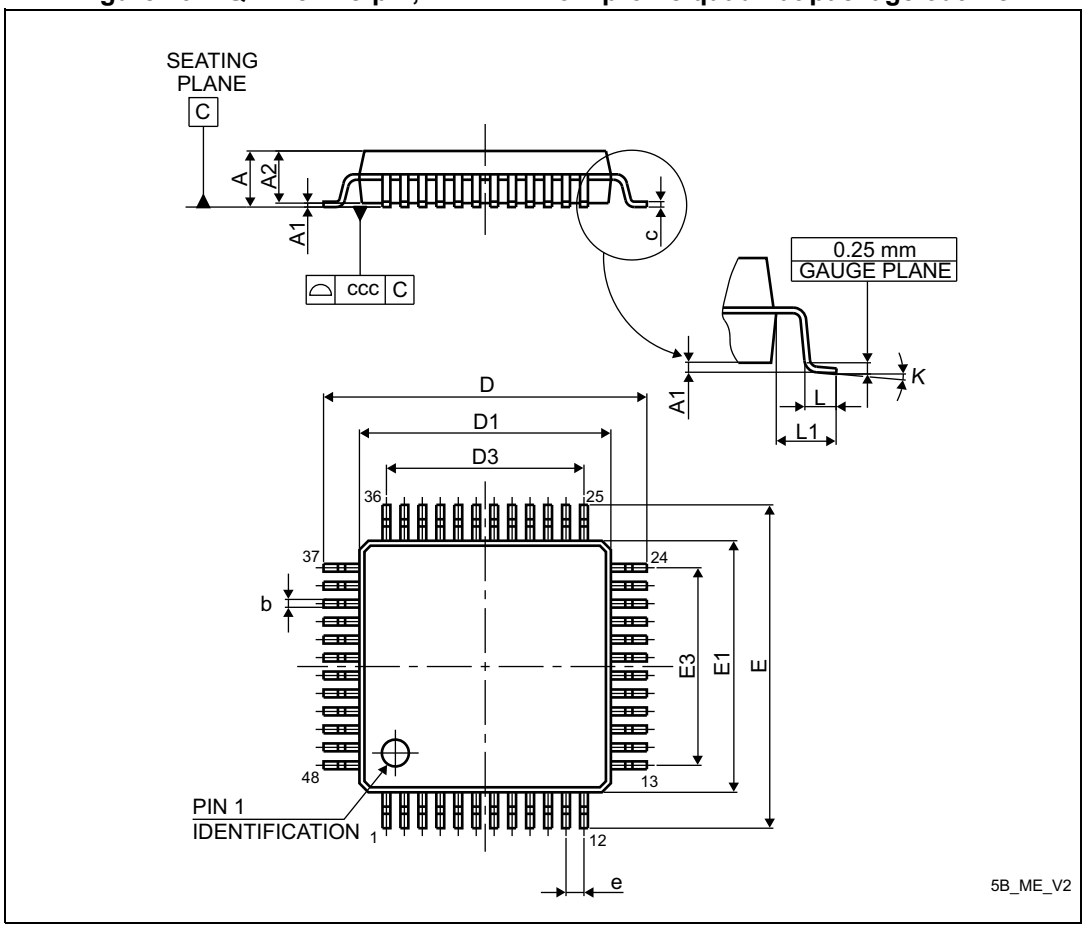
Figure 28. Example of UFQFPN48 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

5.2 LQFP48 package information

Figure 29. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 24. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

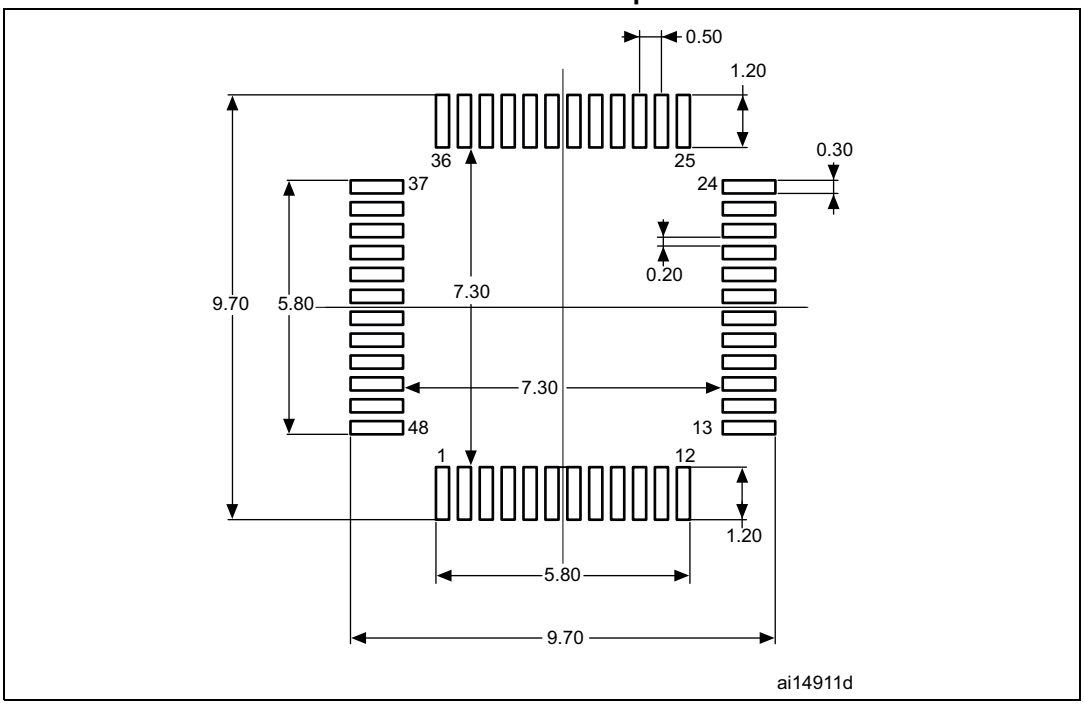
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622

Table 24. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 30. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

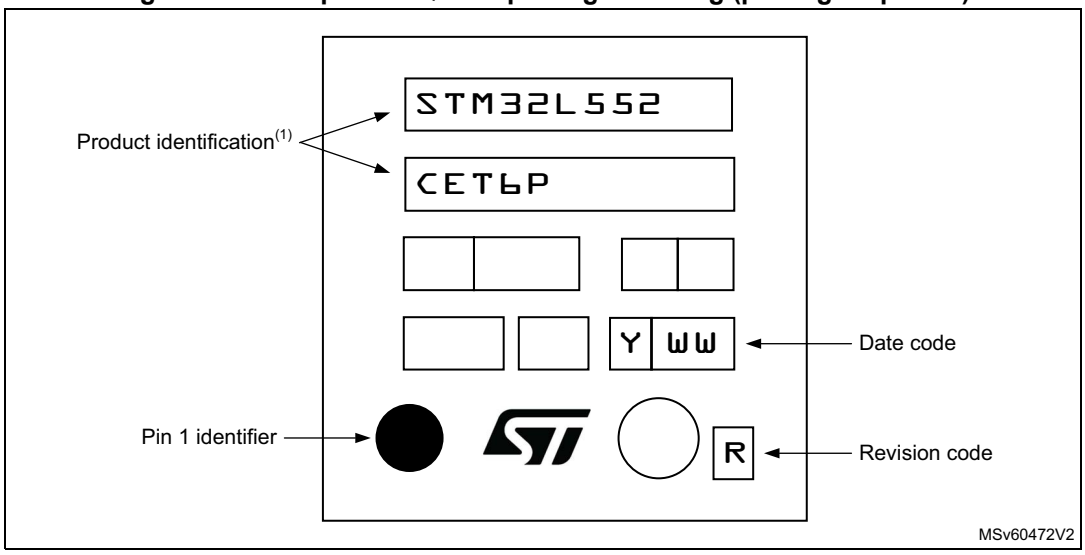
Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

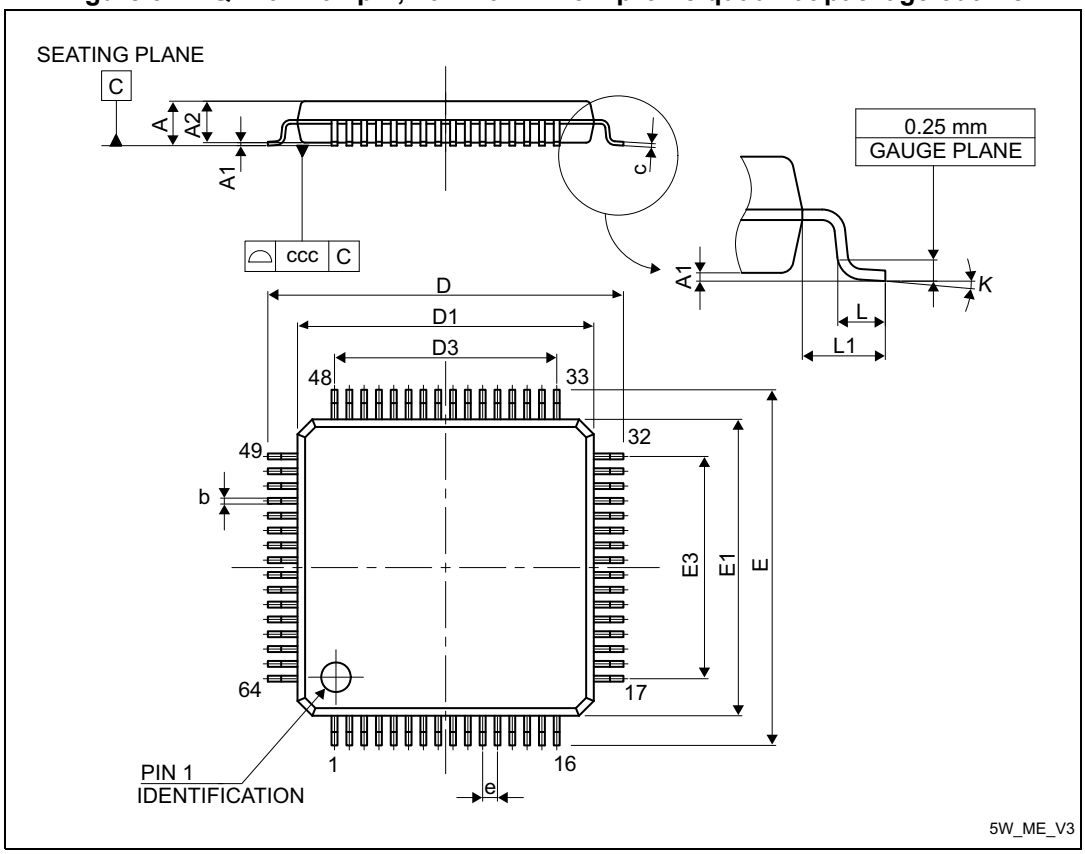
Figure 31. Example of LQFP48 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

5.3 LQFP64 package information

Figure 32. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 25. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

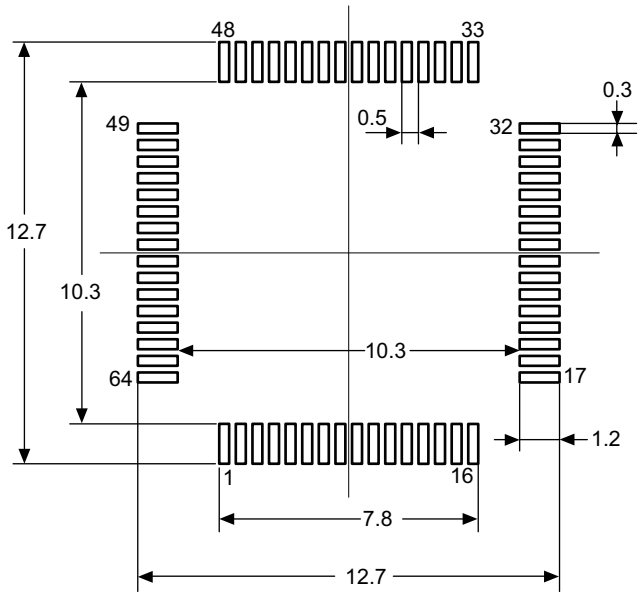
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 25. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

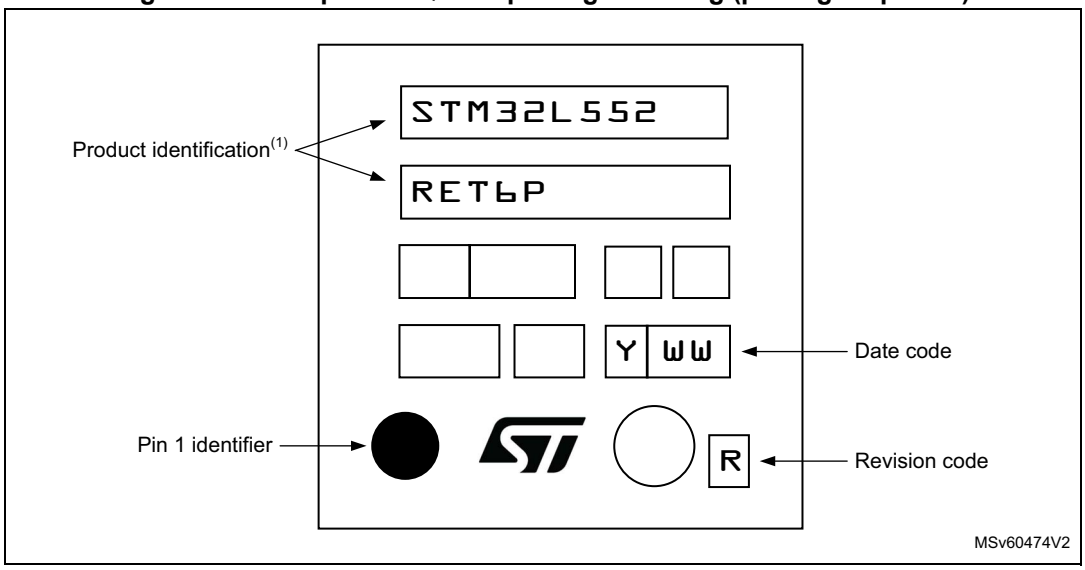
Device marking for LQFP64 (10 x 10)

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

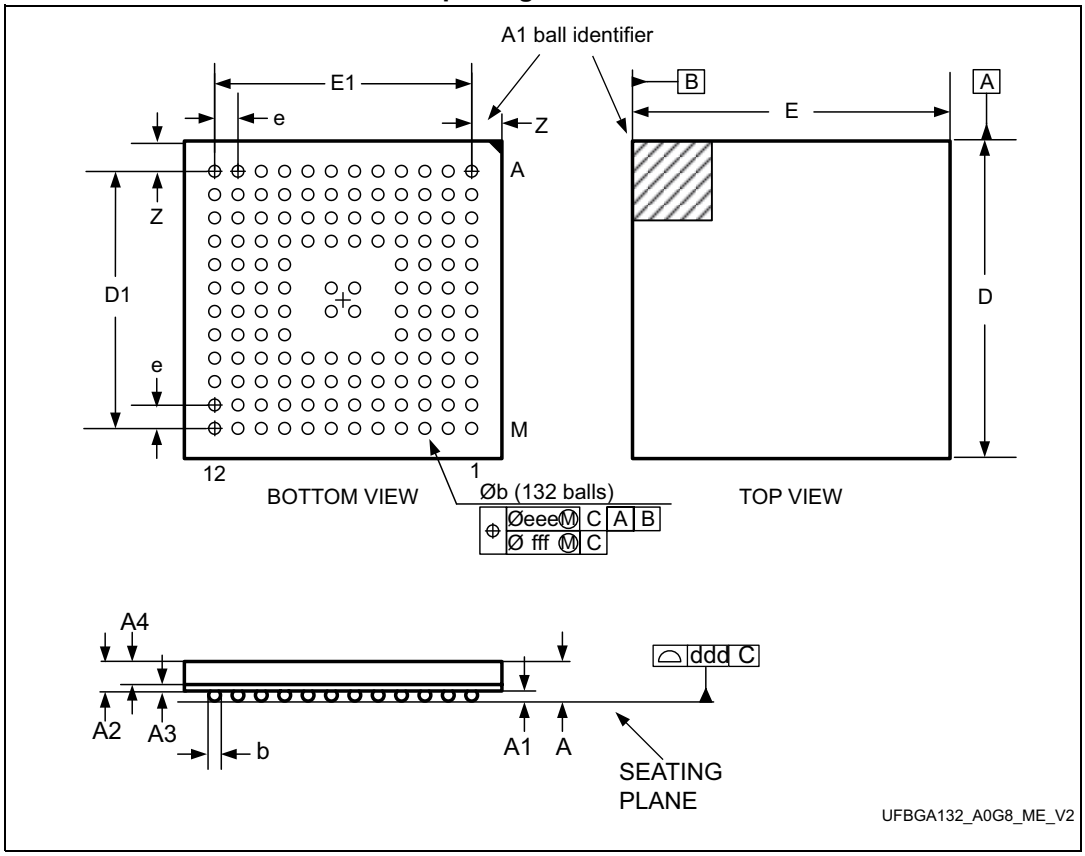
Figure 34. Example of LQFP64 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

5.4 UFBGA132 package information

Figure 35. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 26. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815

Table 26. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-
ddd	-	0.080	-	-	0.0031	-
eee	-	0.150	-	-	0.0059	-
fff	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package recommended footprint

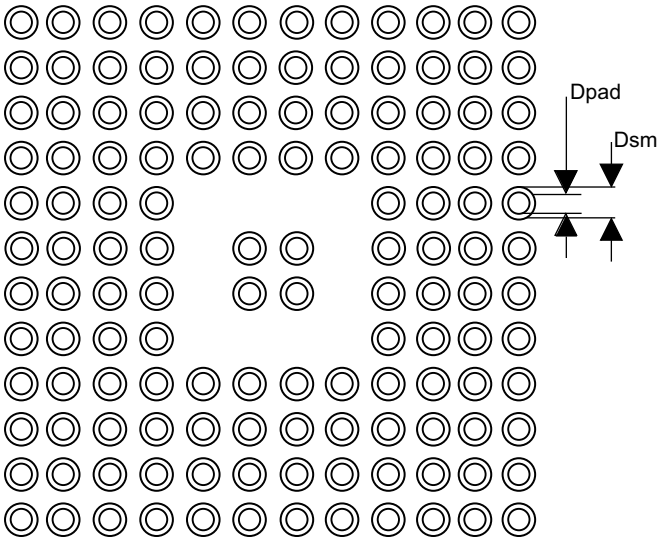


Table 27. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Table 27. UFBGA132 recommended PCB design rules (0.5 mm pitch BGA) (continued)

Dimension	Recommended values
Pad trace width	0.100 mm
Ball diameter	0.280 mm

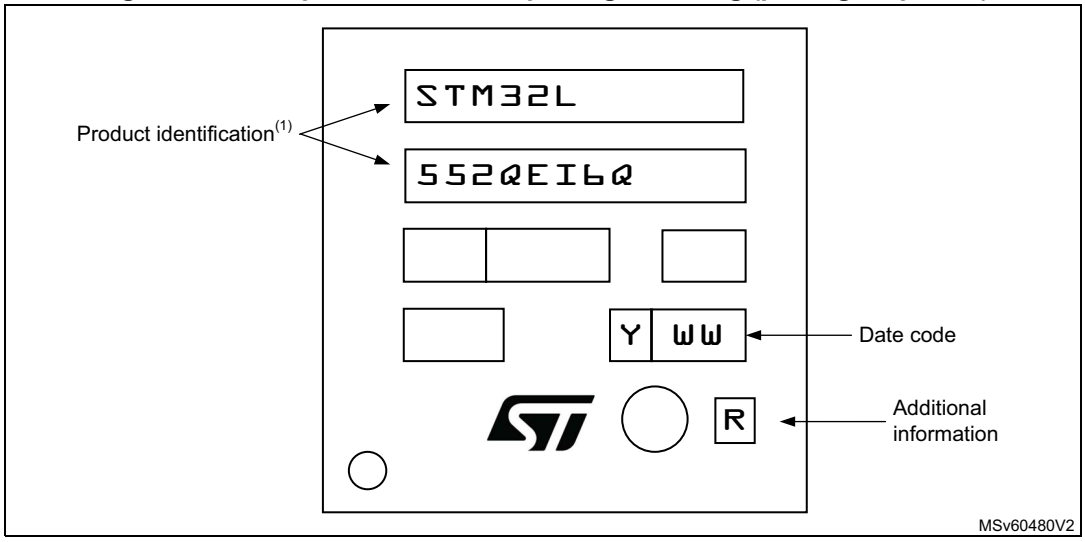
Device marking for UFBGA132 (7 x 7)

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

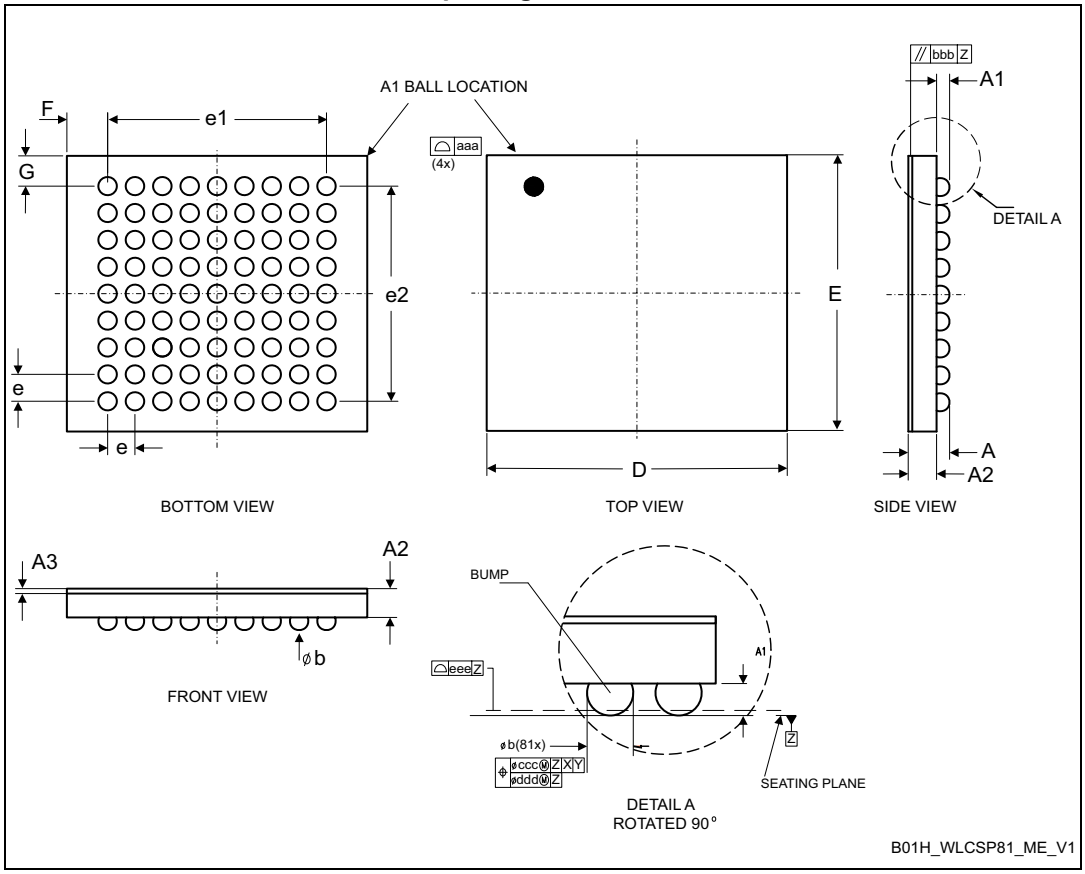
Figure 37. Example of UFBGA132 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

5.5 WLCSP81 package information

Figure 38. WLCSP - 81 balls, 4.36 x 4.07 mm, 0.4 mm pitch, wafer level chip scale package outline



1. Drawing is not to scale.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 28. WLCSP - 81 balls, 4.36 x 4.07 mm, 0.4 mm pitch, wafer level chip scale mechanical data

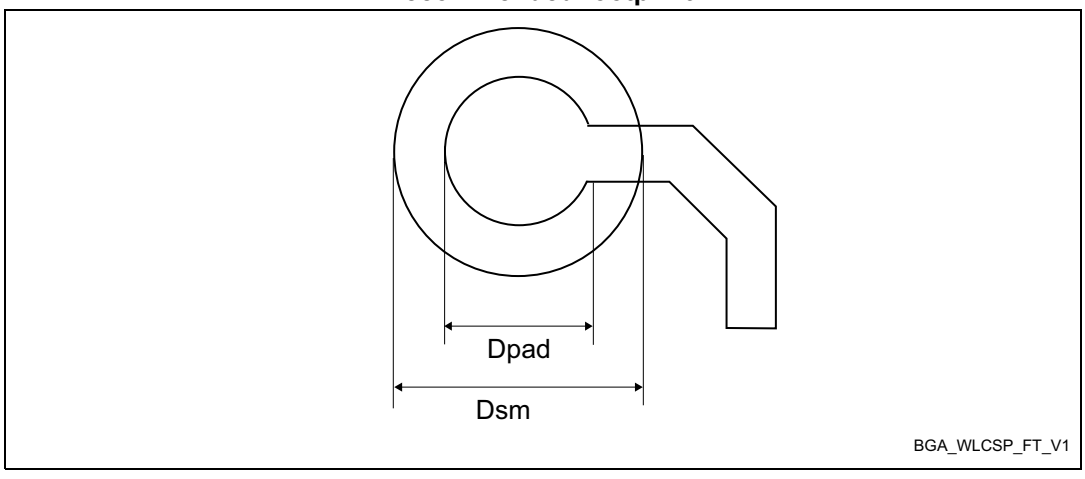
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3(3)	-	0.025	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	4.33	4.36	4.39	0.170	0.172	0.173
E	4.05	4.07	4.09	0.159	0.160	0.161

Table 28. WLCSP - 81 balls, 4.36 x 4.07 mm, 0.4 mm pitch, wafer level chip scale mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.40	-	-	0.016	-
e1	-	3.20	-	-	0.126	-
e2	-	3.20	-	-	0.126	-
F[4]	-	0.580	-	-	0.023	-
G[4]	-	0.435	-	-	0.017	-
aaa	-	0.10	-	-	0.004	-
bbb	-	0.10	-	-	0.004	-
ccc	-	0.10	-	-	0.004	-
ddd	-	0.05	-	-	0.002	-
eee	-	0.05	-	-	0.002	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The maximum total package height is calculated by the RSS method (Root Sum Square) using nominal and tolerances values of A1 and A2.
3. Back side coating. Nominal dimension is rounded to the 3rd decimal place resulting from process capability.
4. Calculated dimensions are rounded to the 3rd decimal place.

Figure 39. WLCSP - 81 balls, 4.36 x 4.07 mm, 0.4 mm pitch, wafer level chip scale recommended footprint



1. Dimensions are expressed in millimeters.

Table 29. WLCSP81 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0,225 mm

Table 29. WLCSP81 recommended PCB design rules

Dimension	Recommended values
Dsm	0.290 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

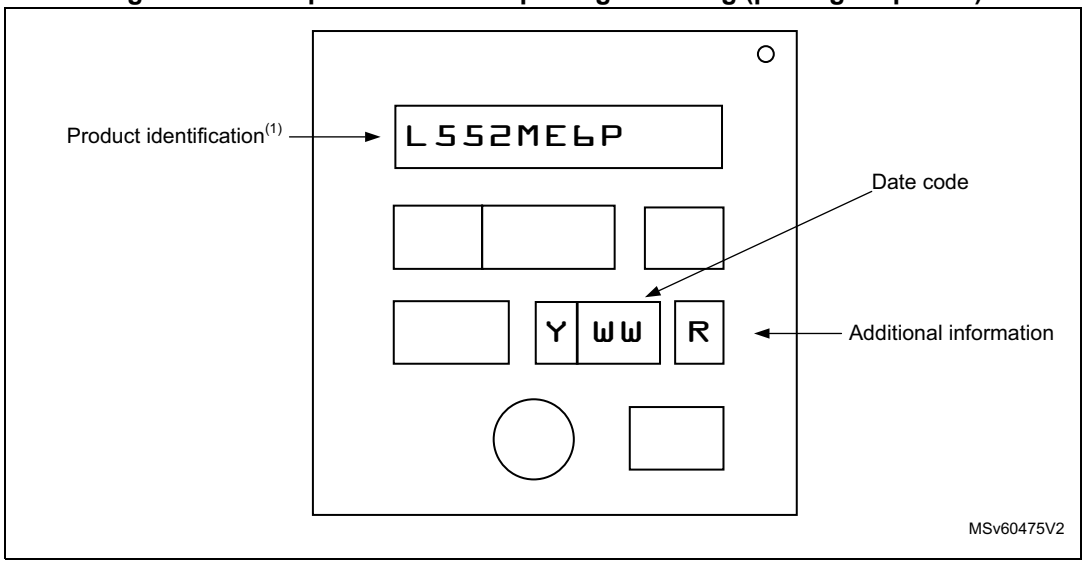
Device marking for WLCSP81

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

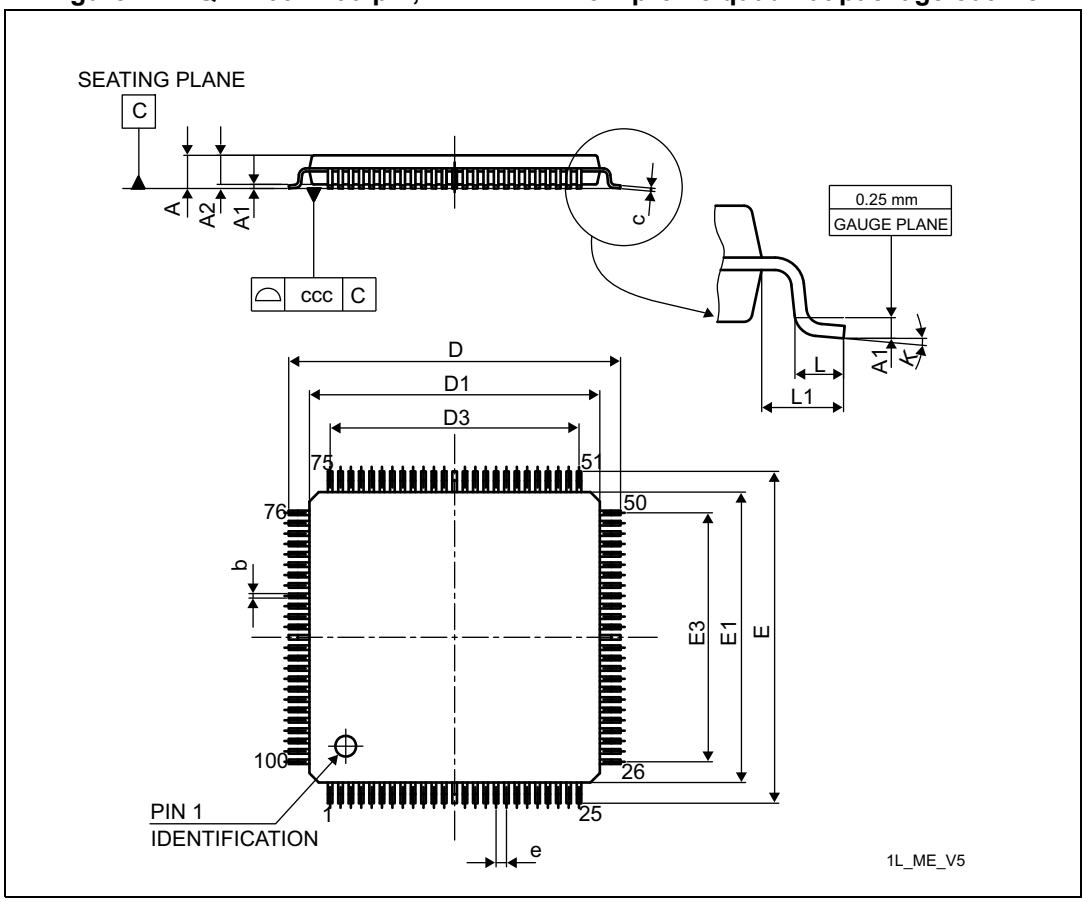
Figure 40. Example of WLCSP81 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

5.6 LQFP100 package information

Figure 41. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 30. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

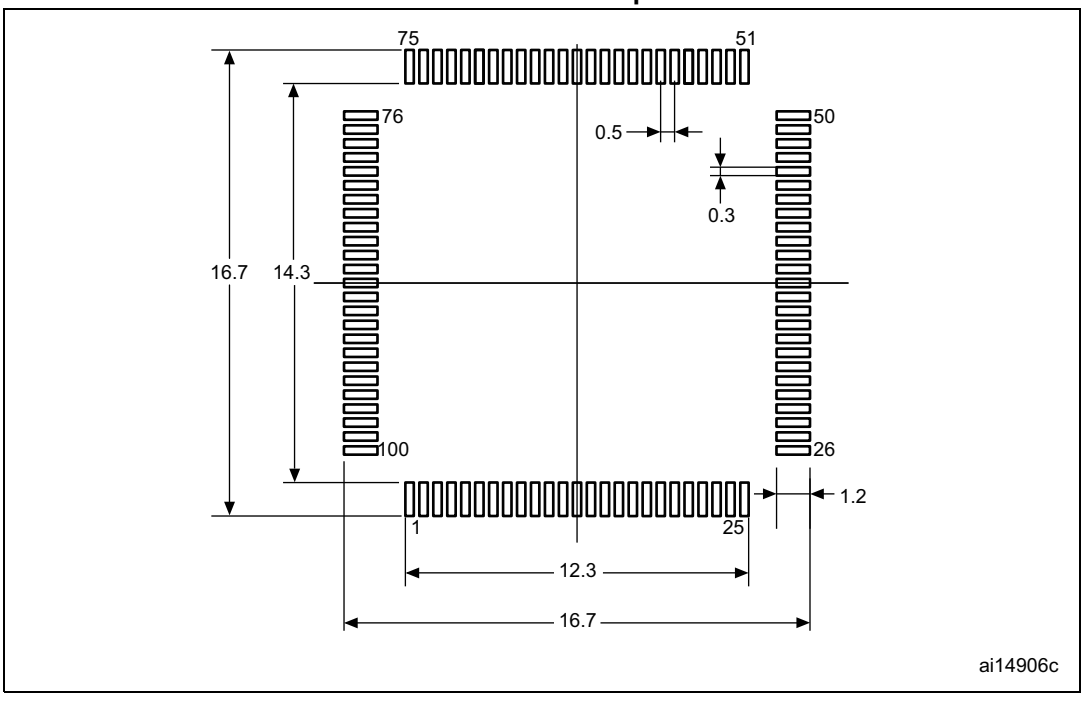
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 30. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 42. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

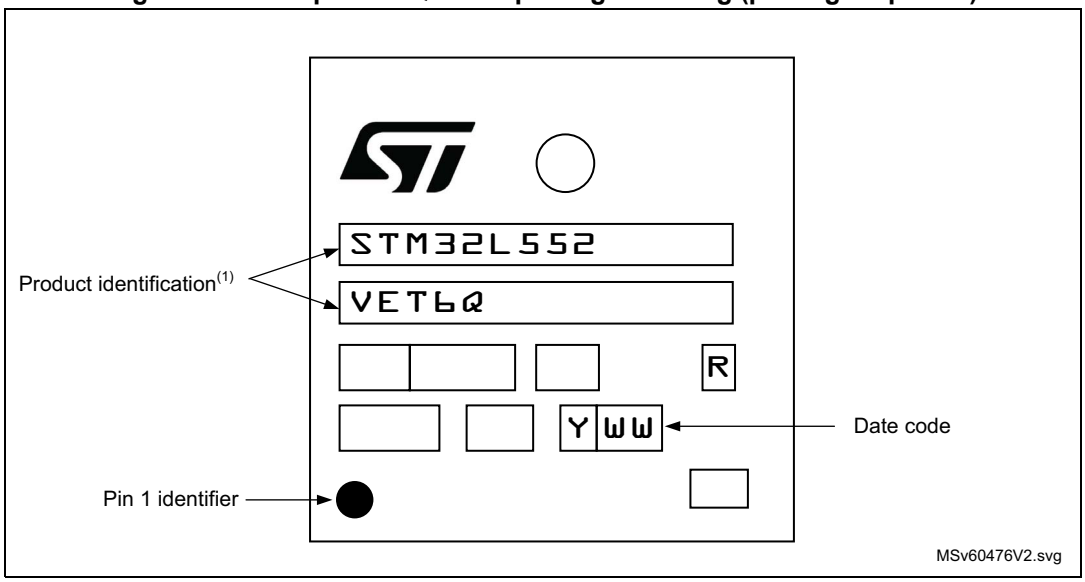
Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

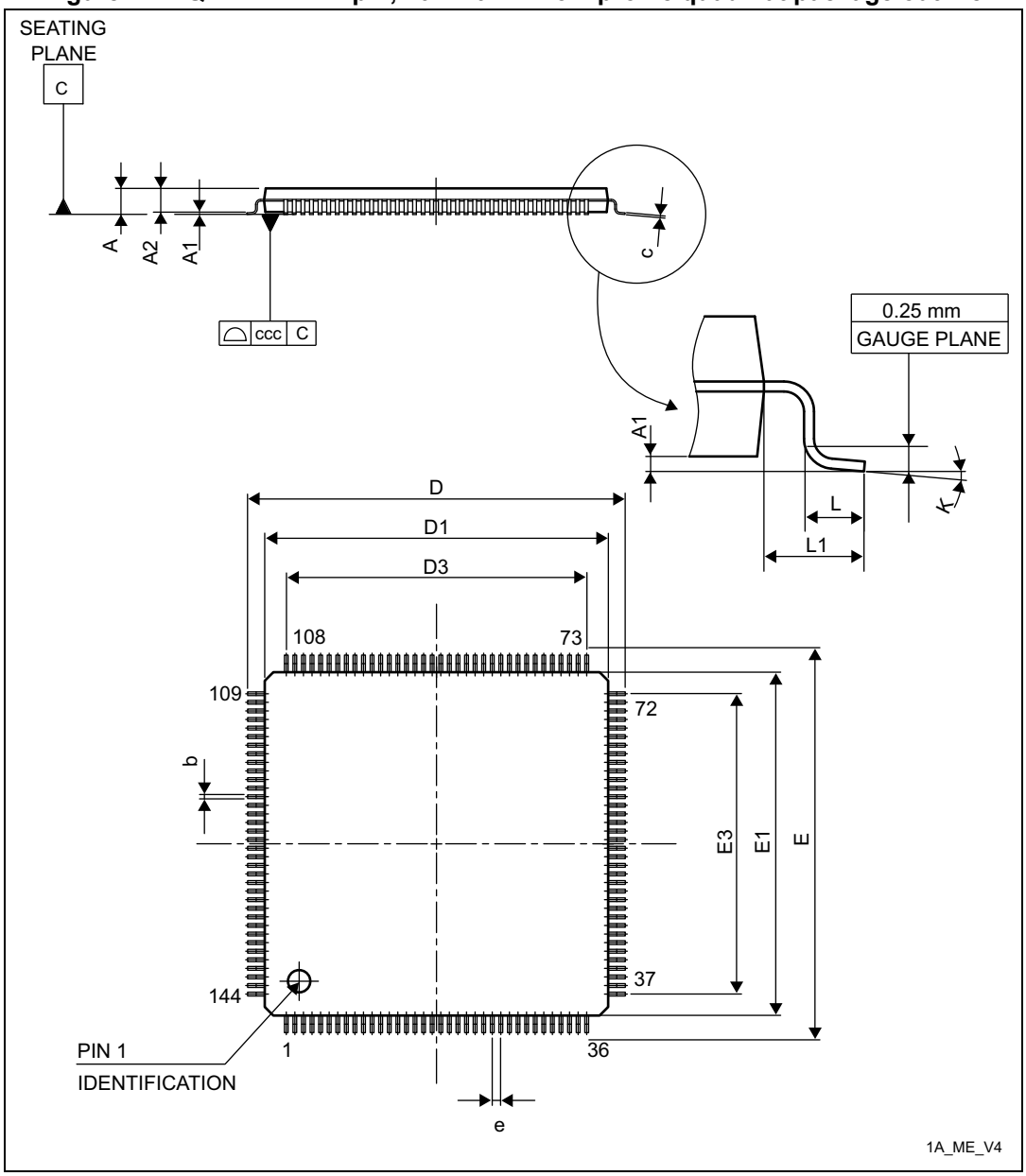
Figure 43. Example of LQFP100 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

5.7 LQFP144 package information

Figure 44. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 31. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

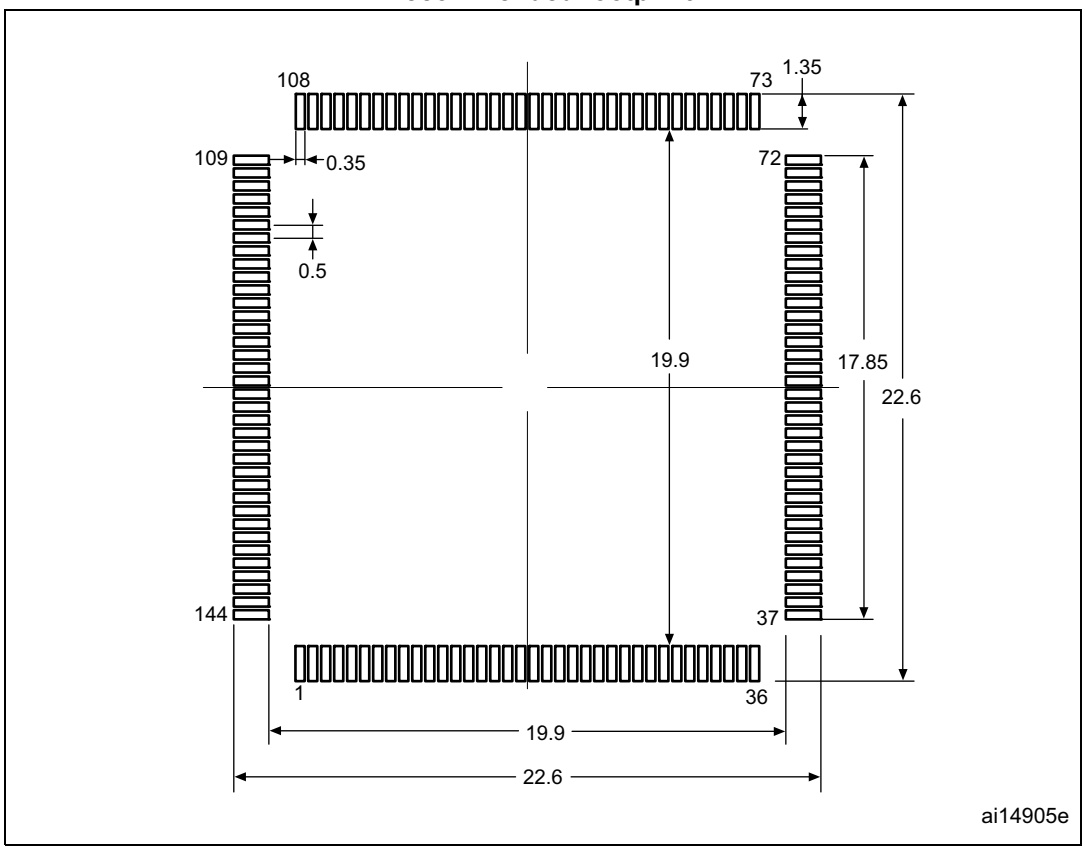
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059

Table 31. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

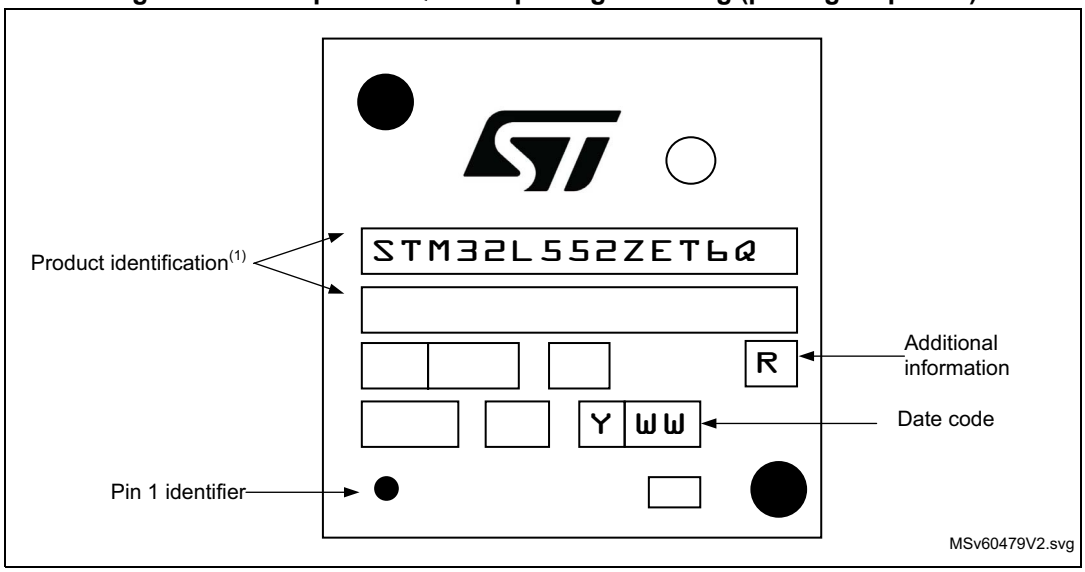
Device marking for LQFP144

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which also depend on supply chain operations, are not indicated below.

Figure 46. Example of LQFP144 package marking (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

6 Ordering information

Example: STM32 L 55x V E T 6 Q

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

L = ultra-low-power

Device subfamily

552 = STM32L552xx

Pin count

C = 48 pins
R = 64 pins
M = 81 pins
V = 100 pins
Q = 132 balls
Z = 144 pins/balls

Flash memory size

E = 512 Kbytes of Flash memory
C= 256 Kbytes of Flash memory

Package

T = LQFP
I = UFBGA
U = UFQFPN
Y = WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C (105 °C junction)
3 = Industrial temperature range, -40 to 125 °C (130°C junction)

Dedicated pinout

Q = Dedicated pinout supporting SMPS step down converter
P = Dedicated pinout supporting external SMPS

Packing

TR = tape and reel
xxx = programmed parts

1. All packages are ECOPACK2 (RoHS compliant and free of brominated, chlorinated and antimony-oxide flame retardants).
2. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

7 Revision history

Table 32. Document revision history

Date	Revision	Changes
12-Oct-2018	1	Initial release
16-Oct-2018	2	Updated: – *Features* on cover page – *Section 2: Description*
15-Mar-2019	3	Updated: – *Features* on cover page – *Section 3.4: Embedded Flash memory* – *Section 3.5: Embedded SRAM* – *Table 6: Example of memory map security attribution vs SAU configuration regions* – *Table 7: Securable peripherals by TZSC* – *Table 8: TrustZone-aware peripherals* – *Default TrustZone security state on page 25* – *Section 3.9: Power supply management* – *Section 3.9.1: Power supply schemes* – *Figure 5: Power-up/down sequence* footnote – *Table 10: Functionalities depending on the working mode* – *Table 11: STM32L552xx peripherals interconnect matrix* – *Section 3.14: Multi-AHB bus matrix* – *Figure 8: Multi-AHB bus matrix* – *Section 3.15: Direct memory access controller (DMA)* – *Section 3.30.4: Low-power timer (LPTIM1, LPTIM2 and LPTIM3)* – *Table 19: Legend/abbreviations used in the pinout table* – *Table 20: STM32L552xx pin definitions* Deleted: – Table *Access status versus readout protection level and execution modes when TZEN=0.*

Table 32. Document revision history

Date	Revision	Changes
15-May-2019	4	Updated: – *Features* and package silhouettes in cover page – *Section 2: Description* – *Table 2: STM32L552xx features and peripheral counts* – *Figure 1: STM32L552xx block diagram* – *Section 3.4: Embedded Flash memory* – *Section 3.6: Boot modes* – *Table 3: Boot modes when TrustZone is disabled (TZEN=0)* – *Table 4: Boot modes when TrustZone is enabled (TZEN=1)* – *Section 3.9.3: Voltage regulator* – *Section 3.9.4: SMPS step down converter* including *Section : SMPS step down converter power supply scheme* – *Table 13: Temperature sensor calibration values* – *Table 14: Internal voltage reference calibration values* – *Section 3.27: Touch sensing controller (TSC)* – *Table 19: Legend/abbreviations used in the pinout table* – *Table 20: STM32L552xx pin definitions*
17-Jun-2019	5	Updated: – *Features* in cover page – *Table 20: STM32L552xx pin definitions* – *Figure 40: Example of WLCSP81 package marking (package top view)*
25-Jun-2019	6	Updated: – *Features* in cover page – All figures for device marking examples on *Section 5: Package information*