# STM32F398VE

ARM® Cortex®-M4 32b MCU+FPU, up to 512KB Flash, 80KB SRAM, FMC, 4 ADCs, 2 DAC ch., 7 comp, 4 Op-Amp, 1.8 V

Datasheet - preliminary data

Features

- Core: ARM® Cortex®-M4 32-bit CPU with 72 MHz FPU, single-cycle multiplication and HW division, DSP instruction and MPU (memory protection unit)
- Memories
  - Up to 512 Kbytes of Flash memory
  - 64 Kbytes of SRAM, with HW parity check implemented on the first 32 Kbytes.
  - Routine booster: 16 Kbytes of SRAM on instruction and data bus, with HW parity check (CCM)
  - Flexible memory controller (FMC) for static memories, with four Chip Select
- CRC calculation unit
- Reset and supply management
  - Low power modes: Sleep and Stop
  - Supply: VDD = 1.8 V ± 8%
    V_{DDA} voltage range = 1.65 V to 3.6 V
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x 16 PLL option
  - Internal 40 kHz oscillator
- Up to 114 fast I/Os
  - All mappable on external interrupt vectors
  - Several 5 V-tolerant
- Interconnect matrix
- 12-channel DMA controller
- Four ADCs 0.20 µs (up to 39 channels) with selectable resolution of 12/10/8/6 bits, 0 to 3.6 V conversion range, separate analog supply from 1.8 to 3.6 V
- Two 12-bit DAC channels with analog supply from 2.4 to 3.6 V
- Seven ultra-fast rail-to-rail analog comparators with analog supply from 1.8 to 3.6 V
- Four operational amplifiers that can be used in PGA mode, all terminals accessible with analog supply from 2.4 to 3.6 V
- Up to 24 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- Up to 14 timers

LQFP100
(14 mm × 14 mm)
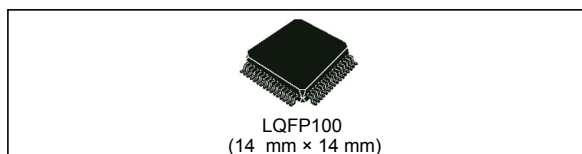
- One 32-bit timer and two 16-bit timers with up to four IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - Three 16-bit 6-channel advanced-control timers, with up to six PWM channels, deadtime generation and emergency stop
  - One 16-bit timer with two IC/OCs, one OCN/PWM, deadtime generation and emergency stop
  - Two 16-bit timers with IC/OC/OCN/PWM, deadtime generation and emergency stop
  - Two watchdog timers (independent, window)
  - One SysTick timer: 24-bit downcounter
  - Two 16-bit basic timers to drive the DAC
- Calendar RTC with Alarm, periodic wakeup from Stop/Standby
- Communication interfaces
  - CAN interface (2.0B Active)
  - Three I²C Fast mode plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, wakeup from STOP
  - Up to five USART/UARTs (ISO 7816 interface, LIN, IrDA, modem control)
  - Up to four SPIs, 4 to 16 programmable bit frames, two with multiplexed half/full duplex I2S interface
  - Infrared transmitter
- SWD, Cortex®-M4 with FPU ETM, JTAG
- 96-bit unique ID

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1   Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F398VE microcontroller.

This STM32F398VE datasheet should be read in conjunction with the reference manual of STM32F303xB/C/D/E, STM32F358xC and STM32F328x4/6/8 devices (RM0316) available on STMicroelectronics website at *www.st.com*.

For information on the Cortex®-M4 core with FPU, please refer to the following documents:

- Cortex®-M4 with FPU Technical Reference Manual, available from ARM website at www.arm.com
- STM32F3xxx and STM32F4xxx Cortex-M4 programming manual (PM0214) available on STMicroelectronics website at *www.st.com*.

2 Description

The STM32F398VE is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (512 Kbytes of Flash memory, 80 Kbytes of SRAM), a flexible memory controller (FMC) for static memories (SRAM, PSRAM, NOR and NAND), and an extensive range of enhanced I/Os and peripherals connected to an AHB and two APB buses.

The device offers four fast 12-bit ADCs (5 Msps), seven comparators, four operational amplifiers, two DAC channel, a low-power RTC, up to five general-purpose 16-bit timers, one general-purpose 32-bit timer, and three timers dedicated to motor control. They also feature standard and advanced communication interfaces: up to three I^{2}Cs, up to four SPIs (two SPIs are with multiplexed full-duplex I2Ss), three USARTs, up to two UARTs and CAN. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL.

The STM32F398VE operates in the -40 to +85°C and -40 to +105°C temperature ranges at 1.8 V ± 8% power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F398VE offers devices in LQFP100 package.

The set of included peripherals changes with the device chosen.

Table 1. STM32F398VE device features and peripheral counts

Peripheral		STM32F3398VE
Flash (Kbytes)		512
SRAM (Kbytes) on data bus		64
CCM (Core Coupled Memory) RAM (Kbytes)		16
FMC (flexible memory controller)		YES
Timers	Advanced control	3 (16-bit)
	General purpose	5 (16-bit) 1 (32-bit)
	Basic	2 (16-bit)
	PWM channels (all) [1]	40
	PWM channels (except complementary)	28
Communication interfaces	SPI (I2S)[2]	4(2)
	I^2C	3
	USART	3
	UART	2
	CAN	1
GPIOs	Normal I/Os (TC, TTa)	43
	5-volt tolerant I/Os (FT, FTf)	42
DMA channels		12
Capacitive sensing channels		24
12-bit ADCs		4 38 channels
12-bit DAC channels		2
Analog comparator		7
Operational amplifiers		4
CPU frequency		72 MHz
Operating voltage		V_{DD} = 1.8 V ± 8%, V_{DDA} voltage range = 1.65 V to 3.6 V
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C
Packages		LQFP100

1. This total number considers also the PWMs generated on the complementary output channels.

2. The SPI interfaces can work in an exclusive way in either the SPI mode or the I^2S audio mode.

Figure 1. STM32F398VE block diagram
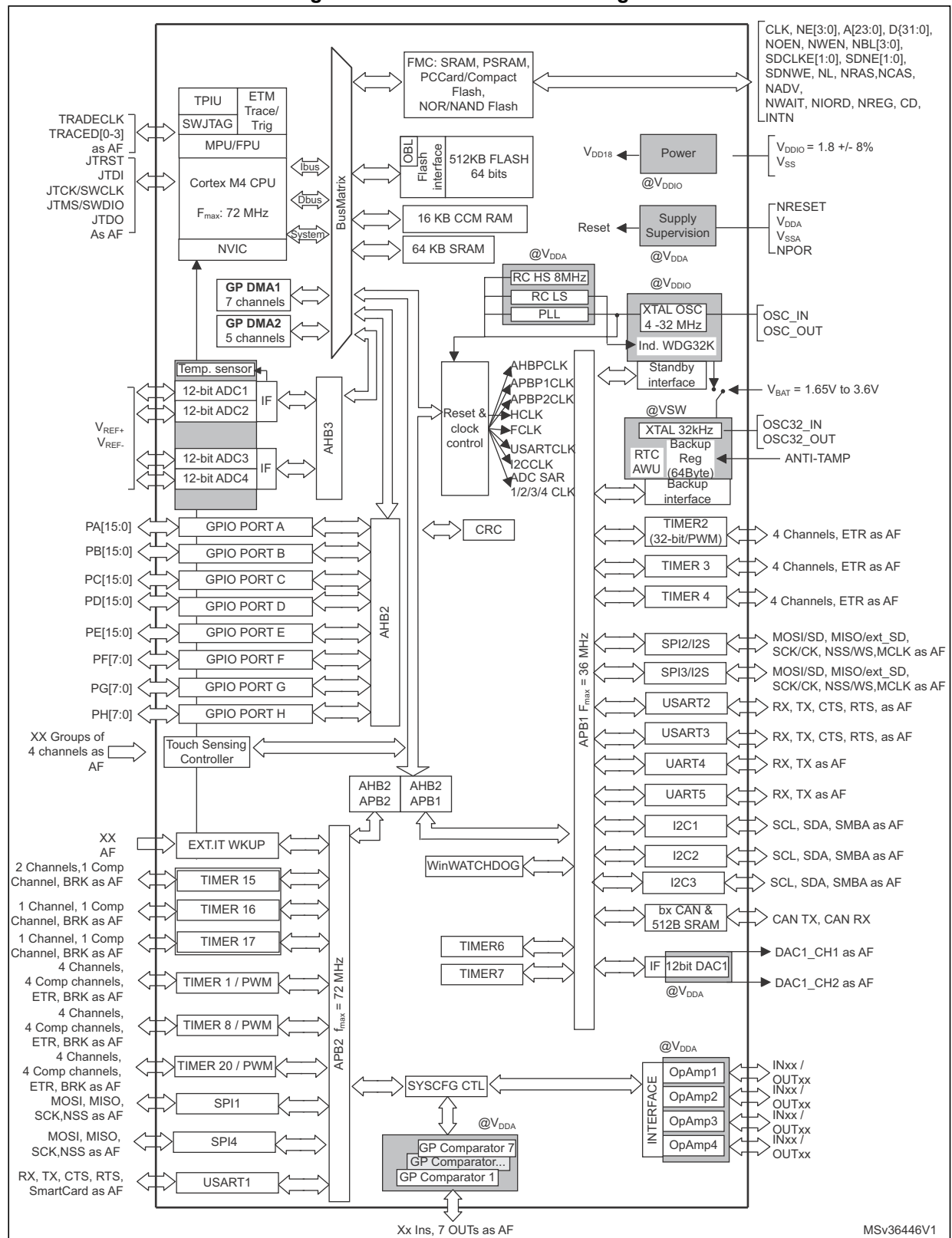
1. AF: alternate function on I/O pins.

3   Functional overview

3.1   ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F398VE is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F398VE.

3.2   Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3   Embedded Flash memory

All STM32F398VE features 384/512 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Embedded SRAM

STM32F398VE features 80 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states, allowing the CPU to achieve 90 Dhrystone MIPS at 72 MHz (when running code from the CCM (Core Coupled Memory) RAM).

- 16 Kbytes of CCM RAM mapped on both instruction and data bus, used to execute critical routines or to access data (parity check on all of CCM RAM).
- 64 Kbytes of SRAM mapped on the data bus (parity check on first 32 Kbytes of SRAM).

3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10) or USART2 (PA2/PA3) or I2C1 (PB6/PB7) or I2C3 (PA8/PB5).

3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.7 Power management

3.7.1 Power supply schemes

- V_{SS}, V_{DD} = 1.8 V ± 8% V: external power supply for I/Os and the internal regulator. It is provided externally through VDD pins.

- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supply for ADC, DAC, comparators, operational amplifier, reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} differs from one analog peripheral to another. *Table 2* provides the summary of the V_{DDA} ranges for analog peripherals. The V_{DDA} voltage level must always be greater than or equal to the V_{DD} voltage level and must be provided first.

Table 2. External analog supply values for analog peripherals

Analog peripheral	Minimum V_{DDA} supply	Maximum V_{DDA} supply
ADC/COMP	1.8 V	3.6 V
DAC/OPAMP	2.4 V	3.6 V

- V_{BAT} = 1.65 to 3.6 V: power supply for RT C, external clock 32 kHz oscillator and backup registers (through power switch which is guaranteed in the full range of V_{DD}) when V_{DD} is not present.

3.7.2 Power supply supervisor

The device power-on reset (POR) is controlled through the external NPOR pin. The device remains in reset state when NPOR pin is held low.

To guarantee a proper power-on reset, the NPOR pin must be held low when V_{DDA} is applied. Then, when V_{DD} is stable, the reset state can be exited through one of the following ways:

- by putting the NPOR pin in high impedance, NPOR pin has an internal pull up,

or

- by forcing the pin to high level by connecting it to VDDA.

3.7.3 Low-power modes

The STM32F398VE supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

Note: *The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

3.8   Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 3. STM32F398VE peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADCx DAC1	Conversion triggers
	DMA	Memory to memory transfer trigger
	Compx	Comparator output blanking
COMPx	TIMx	Timer input: OCREF_CLR input, input capture
ADCx	TIMx	Timer triggered by analog watchdog
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx GPIO	TIM1, TIM8, TIM20 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: *For more details about the interconnect actions, please refer to the corresponding sections in the STM32F398VEreference manual (RM0316).*

3.9   Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

Figure 2. STM32F398VE clock tree
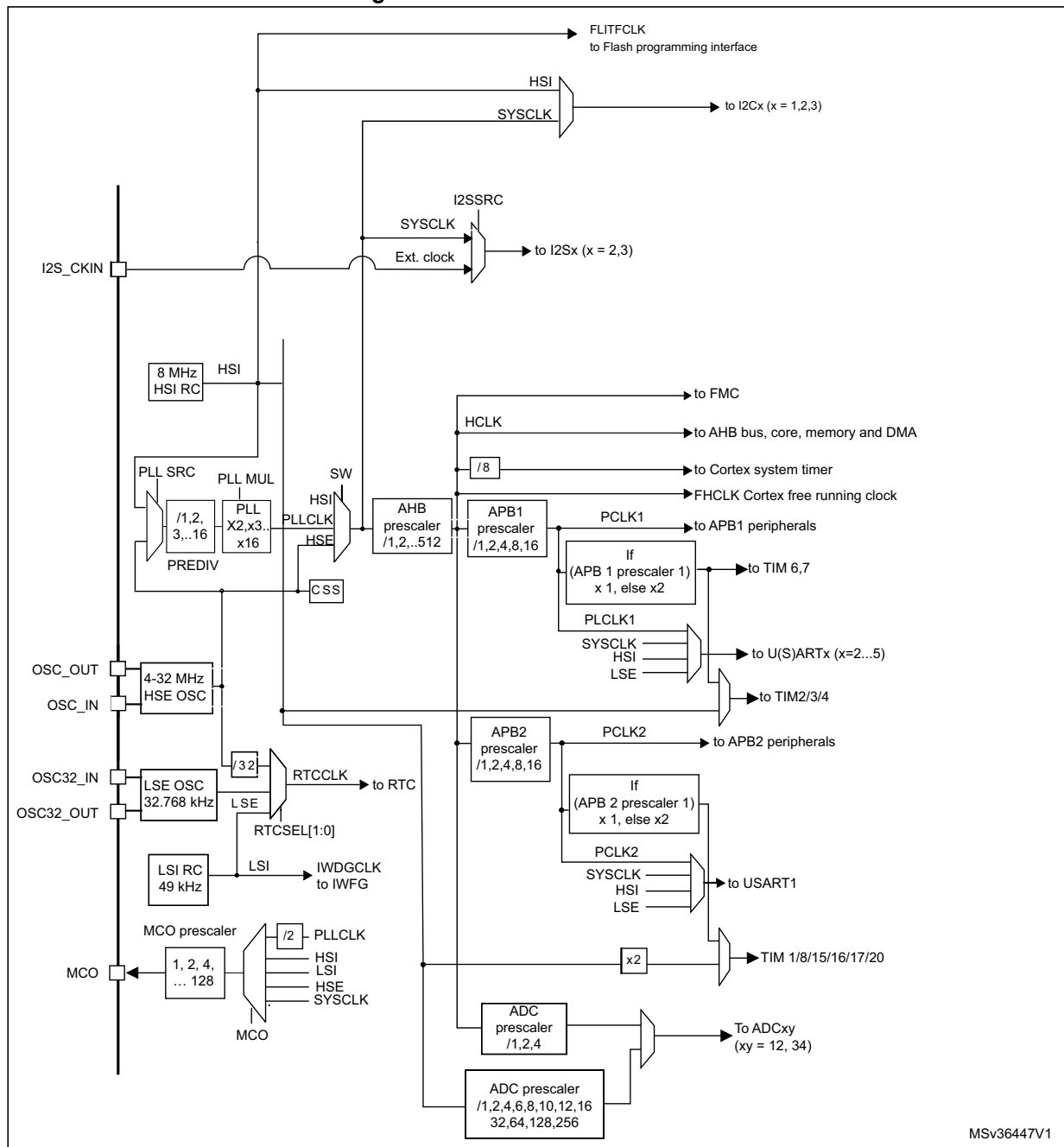
3.10   General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allows I/O toggling up to 36 MHz.

3.11   Direct memory access (DMA)

The flexible general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each of the 12 DMA channels is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^{2}C, USART, general-purpose timers, DAC and ADC.

3.12   Flexible memory controller (FMC)

The Flexible memory controller (FMC) includes two memory controllers:
- The NOR/PSRAM memory controller,
- The NAND/PC Card memory controller.

The main features of the FMC controller are the following:
- Interface with static-memory mapped devices including:
  – Static random access memory (SRAM),
  – NOR Flash memory/OneNAND Flash memory,
  – PSRAM (four memory banks),
  – NAND Flash memory with ECC hardware to check up to 8 Kbyte of data,
  – 16-bit PC Card compatible devices.
- 8-,16-bit data bus width,
- Independent Chip Select control for each memory bank,
- Independent configuration for each memory bank,
- Write FIFO,
- LCD parallel interface.

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.13 Interrupts and events

3.13.1 Nested vectored interrupt controller (NVIC)

The STM32F398VE embeds a nested vectored interrupt controller (NVIC) able to handle up to 73 maskable interrupt channels and 16 priority levels.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.14 Fast analog-to-digital converter (ADC)

Four fast analog-to-digital converters 5 MSPS, with selectable resolution between 12 and 6 bit, are embedded in the STM32F398VE. The ADCs have up to 39 external channels. Some of the external channels are shared between ADC1&2 and between ADC3&4. The ADCs can perform conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADCs have also internal channels: Temperature sensor connected to ADC1 channel 16, VBAT/2 connected to ADC1 channel 17, Voltage reference VREFINT connected to the 4 ADCs channel 18, VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17, VREFOPAMP3 connected to ADC3 channel 17 and VREFOPAMP4 connected to ADC4 channel 17.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single-shunt phase current reading techniques.

The ADC can be served by the DMA controller.

Three analog watchdogs are available per ADC.

The analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers and the advanced-control timer (TIM1, TIM8 and TIM20) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.14.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

3.14.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADCx_IN18, x=1...4 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.14.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN17. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.14.4 OPAMP reference voltage (VREFOPAMP)

Every OPAMP reference voltage can be measured using a corresponding ADC internal channel: VREFOPAMP1 connected to ADC1 channel 15, VREFOPAMP2 connected to ADC2 channel 17, VREFOPAMP3 connected to ADC3 channel 17 and VREFOPAMP4 connected to ADC4 channel 17.

3.15 Digital-to-analog converter (DAC)

Two 12-bit buffered DAC channel can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Two DAC output channel
- 8-bit or 10-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability (for each channel)
- External triggers for conversion
- Input voltage reference VREF+

3.16 Operational amplifier (OPAMP)

The STM32F398VE embeds four operational amplifiers with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain can be programmed to be 2, 4, 8 or 16.

3.17 Ultra-fast comparators (COMP)

The STM32F398VE embeds seven ultra-fast rail-to-rail comparators with programmable reference voltage (internal or external) and selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 20: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers. and can be also combined per pair into a window comparator.

3.18   Timers and watchdogs

The STM32F398VE includes three advanced control timer, up to six general-purpose timers, two basic timers, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced	TIM1, TIM8, TIM20	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Note: *TIM1/8/20/2/3/4/15/16/17 can have PLL as clock source, and therefore can be clocked at 144 MHz.*

3.18.1 Advanced timers (TIM1, TIM8, TIM20)

The advanced-control timers (TIM1, TIM8, TIM20) can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timers (described in *Section 3.18.2* using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.18.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F398VE (see *Table 4* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, and TIM4

  These are full-featured general-purpose timers:

  – TIM2 has a 32-bit auto-reload up/downcounter and 32-bit prescaler
  – TIM3 and 4 have 16-bit auto-reload up/downcounters and 16-bit prescalers.

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM15, 16 and 17

  These three timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM15 has 2 channels and 1 complementary channel
  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.18.3 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

3.18.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.18.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.18.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.19 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.20 Inter-integrated circuit interface (I2C)

Up to three I2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

All I2C bus interfaces support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 5. Comparison of I2C analog and digital filters

	Analog filter	**Digital filter**
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2,3) to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 6* for the features available in I2C1, I2C2 and I2C3.

Table 6. STM32F398VE I2C implementation

I2C features[1]	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Independent clock	X	X	X
SMBus	X	X	X
Wakeup from STOP	X	X	X

1.   X = supported.

3.21 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F398VE has three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

3.22 Universal asynchronous receiver transmitter (UART)

The STM32F398VE has 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART4 interface can be served by the DMA controller.

Refer to *Table 7* for the features available in all U(S)ART interfaces.

Table 7. USART features

USART modes/features[1]	USART1	USART2	USART3	UART4	UART5
Hardware flow control for modem	X	X	X	-	-
Continuous communication using DMA	X	X	X	X	-
Multiprocessor communication	X	X	X	X	X
Synchronous mode	X	X	X	-	-
Smartcard mode	X	X	X	-	-
Single-wire half-duplex communication	X	X	X	X	X
IrDA SIR ENDEC block	X	X	X	X	X
LIN mode	X	X	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X	X	X
Receiver timeout interrupt	X	X	X	X	X
Modbus communication	X	X	X	X	X
Auto baud rate detection	X	X	X	-	-
Driver Enable	X	X	X	-	-

1. X = supported.

3.23 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I2S)

Up to four SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 8* for the features available in SPI1, SPI2, SPI3 and SPI4.

Table 8. STM32F398VE SPI/I2S implementation

SPI features[1]	SPI1	SPI2	SPI3	SPI4
Hardware CRC calculation	X	X	X	X
Rx/Tx FIFO	X	X	X	X
NSS pulse mode	X	X	X	X
I2S mode	-	X	X	-
TI mode	X	X	X	X

1. X = supported.

3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.25 Infrared Transmitter

The STM32F398VE provides an infrared transmitter solution. The solution is based on internal connections between TIM16 and TIM17 as shown in the figure below.

TIM17 is used to provide the carrier frequency and TIM16 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate the infrared remote control signals, TIM16 channel 1 and TIM17 channel 1 must be properly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming the two timers output compare channels.

Figure 3. Infrared transmitter
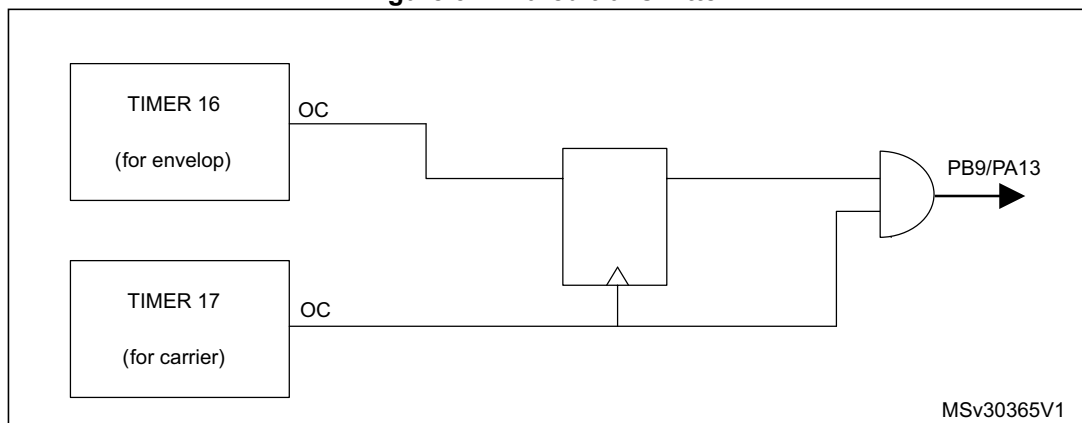
3.26 Touch sensing controller (TSC)

The STM32F398VE provides a simple solution for adding capacitive sensing functionality to any application. The device offers up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, etc.). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 9. Capacitive sensing GPIOs available on STM32F398VE

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	-	-		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 10. Number of capacitive sensing channels available on STM32F398VE

Analog I/O group	Number of capacitive sensing channels	
	STM32F398VE/ZE	STM32F398RE
G1	3	3
G2	3	3
G3	3	3
G4	3	3
G5	3	3
G6	3	3
G7	3	0
G8	3	0
Number of capacitive sensing channels	24	18

3.27 Development support

3.27.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.27.2 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F398VE through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using a high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

4 Pinouts and pin description

Figure 4. STM32F398VE LQFP100 pinout

MS36449V1
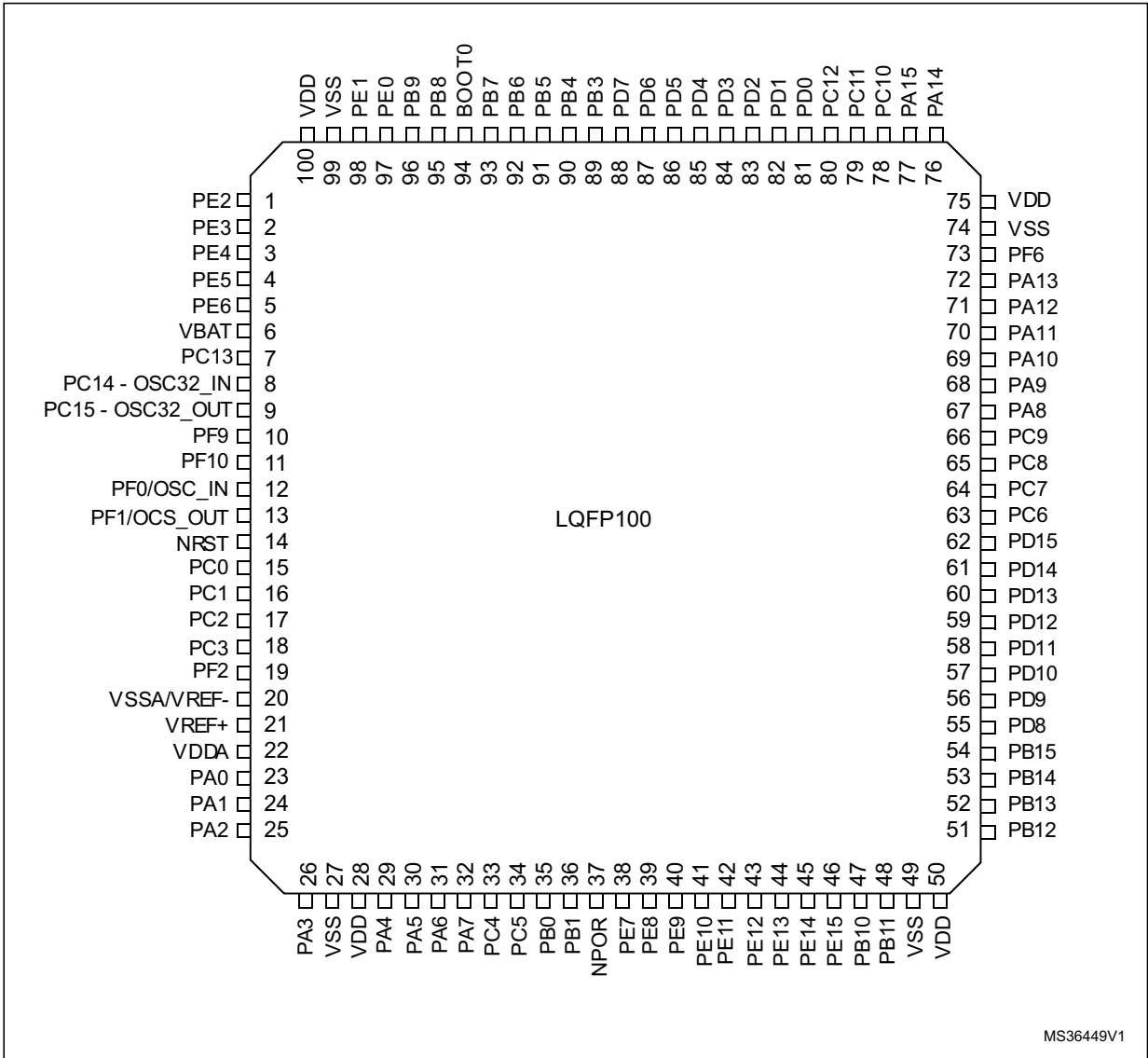
Table 11. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name			Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, I2C FM+ option
		TTa	3.3 V tolerant I/O
		TC	Standard 3.3V I/O
		POR	Dedicated to NPOR pin
		B	Dedicated to BOOT0 pin
		RST	Bi-directional reset pin with embedded weak pull-up resistor
Notes			Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset
Pin functions	Alternate functions		Functions selected through GPIOx_AFR registers
	Additional functions		Functions directly selected/enabled through peripheral registers

Table 12. STM32F398VE pin definitions

Pin number LQFP100	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
1	PE2	I/O	FT	(1)	TRACECK, EVENTOUT, TIM3_CH1, TSC_G7_IO1, SPI4_SCK, TIM20_CH1, FMC_A23	-
2	PE3	I/O	FT	(1)	TRACED0, EVENTOUT, TIM3_CH2, TSC_G7_IO2, SPI4_NSS, TIM20_CH2, FMC_A19	-
3	PE4	I/O	FT	(1)	TRACED1, EVENTOUT, TIM3_CH3, TSC_G7_IO3, SPI4_NSS, TIM20_CH1N, FMC_A20	-
4	PE5	I/O	FT	(1)	TRACED2, EVENTOUT, TIM3_CH4, TSC_G7_IO4, SPI4_MISO, TIM20_CH2N, FMC_A21	-
5	PE6	I/O	FT	(1)	TRACED3, EVENTOUT, SPI4_MOSI, TIM20_CH3N, FMC_A22	WKUP3, RTC_TAMP3
6	VBAT	S	-	-	-	-

Table 12. STM32F398VE pin definitions (continued)

Pin number	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100						
7	PC13[2]	I/O	TC	-	EVENTOUT, TIM1_CH1N	WKUP2,RTC_TAMP1, RTC_TS, RTC_OUT
8	PC14 - OSC32_IN [2]	I/O	TC	-	EVENTOUT	OSC32_IN
9	PC15 - OSC32_OUT [2]	I/O	TC	-	EVENTOUT	OSC32_OUT
-	PH0	I/O	FT	[1]	EVENTOUT, TIM20_CH1, FMC_A0	-
-	PH1	I/O	FT	[1]	EVENTOUT, TIM20_CH2, FMC_A1	-
19	PF2	I/O	TTa	[1]	EVENTOUT, TIM20_CH3, FMC_A2	ADC12_IN10
-	PF3	I/O	FT	[1]	EVENTOUT, TIM20_CH4, FMC_A3	-
-	PF4	I/O	TTa	[1]	EVENTOUT, COMP1_OUT, TIM20_CH1N, FMC_A4	ADC1_IN5
-	PF5	I/O	FT	[1]	EVENTOUT, TIM20_CH2N, FMC_A5	-
-	VSS	S		[1]	-	-
-	VDD	S		[1]	-	-
73	PF6	I/O	FTf	[1]	EVENTOUT, TIM4_CH4, I2C2_SCL, USART3_RTS, FMC_NIORD	-
-	PF7	I/O	FT	[1]	EVENTOUT, TIM20_BKIN, FMC_NREG	-
-	PF8	I/O	FT	[1]	EVENTOUT, TIM20_BKIN2, FMC_NIOWR	-
10	PF9	I/O	FT	[1]	EVENTOUT, TIM20_BKIN, TIM15_CH1, SPI2_SCK, FMC_CD	-
11	PF10	I/O	FT	[1]	EVENTOUT, TIM20_BKIN2, TIM15_CH2, SPI2_SCK, FMC_INTR	-
12	PF0-OSC_IN	I	FTf	-	EVENTOUT, I2C2_SDA, SPI2_NSS/I2S2_WS, TIM1_CH3N	OSC_IN
13	PF1- OSC_OUT	O	FTf	-	EVENTOUT, I2C2_SCL, SPI2_SCK/I2S2_CK	OSC_OUT
14	NRST	I-O	RST	-	Device reset input/internal reset output (active low)	

Table 12. STM32F398VE pin definitions (continued)

Pin number LQFP100	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
15	PC0	I/O	TTa	-	EVENTOUT, TIM1_CH1	ADC12_IN6, COMP7_INM
16	PC1	I/O	TTa	-	EVENTOUT, TIM1_CH2	ADC12_IN7, COMP7_INP
17	PC2	I/O	TTa	-	EVENTOUT, TIM1_CH3, COMP7_OUT	ADC12_IN8
18	PC3	I/O	TTa	-	EVENTOUT, TIM1_CH4, TIM1_BKIN2	ADC12_IN9
20	VSSA	S	-	(1)	-	-
-	VREF-	S	-	(1)	-	-
21	VREF+	S	-	-	-	-
22	VDDA	S	-	-	-	-
23	PA0	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TSC_G1_IO1, USART2_CTS, COMP1_OUT, TIM8_BKIN, TIM8_ETR, EVENTOUT	ADC1_IN1, COMP1_INM, RTC_TAMP2, WKUP1
24	PA1	I/O	TTa	-	RTC_REFIN, TIM2_CH2, TSC_G1_IO2, USART2_RTS, TIM15_CH1N, EVENTOUT	ADC1_IN2, COMP1_INP, OPAMP1_VINP, OPAMP3_VINP
25	PA2	I/O	TTa	(3)	TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3, COMP2_INM, OPAMP1_VOUT
26	PA3	I/O	TTa	-	TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4, OPAMP1_VINM/OPAMP,1_VINP
27	VSS	S	-	-	-	-
28	VDD	S	-	(1)	-	-
29	PA4	I/O	TTa	(3)	TIM3_CH2, TSC_G2_IO1, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC2_IN1, DAC1_OUT1, COMP1_INM, COMP2_INM, COMP3_INM, COMP4_INM, COMP5_INM, COMP6_INM, COMP7_INM, OPAMP4_VINP
30	PA5	I/O	TTa	(3)	TIM2_CH1/TIM2_ETR, TSC_G2_IO2, SPI1_SCK, EVENTOUT	ADC2_IN2, DAC1_OUT2, COMP1_INM, COMP2_INM, COMP3_INM, COMP4_INM, COMP5_INM, COMP6_INM, COMP7_INM, OPAMP1_VINP, OPAMP2_VINM, OPAMP3_VINP
31	PA6	I/O	TTa	(3)	TIM16_CH1, TIM3_CH1, TSC_G2_IO3, TIM8_BKIN, SPI1_MISO, TIM1_BKIN, COMP1_OUT, EVENTOUT	ADC2_IN3, OPAMP2_VOUT

Table 12. STM32F398VE pin definitions (continued)

Pin number LQFP100	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
32	PA7	I/O	TTa	-	TIM17_CH1, TIM3_CH2, TSC_G2_IO4, TIM8_CH1N, SPI1_MOSI, TIM1_CH1N, EVENTOUT	ADC2_IN4, COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
33	PC4	I/O	TTa	-	EVENTOUT, TIM1_ETR, USART1_TX	ADC2_IN5
34	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM
35	PB0	I/O	TTa	-	TIM3_CH3, TSC_G3_IO2, TIM8_CH2N, TIM1_CH2N, EVENTOUT	ADC3_IN12, COMP4_INP, OPAMP2_VINP, OPAMP3_VINP
36	PB1	I/O	TTa	(3)	TIM3_CH4, TSC_G3_IO3, TIM8_CH3N, TIM1_CH3N, COMP4_OUT, EVENTOUT	ADC3_IN1, OPAMP3_VOUT
37	NPOR	I	POR	-	Device power on reset input	
-	PF11	I/O	FT	(1)	EVENTOUT, TIM20_ETR	-
-	PF12	I/O	FT	(1)	EVENTOUT, TIM20_CH1, FMC_A6	-
-	VSS	S	-	-	-	-
-	VDD	S	-	(1)	-	-
-	PF13	I/O	FT	(1)	EVENTOUT, TIM20_CH2, FMC_A7	-
-	PF14	I/O	FT	(1)	EVENTOUT, TIM20_CH3, FMC_A8	-
-	PF15	I/O	FT	(1)	EVENTOUT, TIM20_CH4, FMC_A9	-
-	PG0	I/O	FT	(1)	EVENTOUT, TIM20_CH1N, FMC_A10	-
-	PG1	I/O	FT	(1)	EVENTOUT, TIM20_CH2N, FMC_A11	-
38	PE7	I/O	TTa	(1)	EVENTOUT, TIM1_ETR, FMC_D4	ADC3_IN13
39	PE8	I/O	TTa	(1)	EVENTOUT, TIM1_CH1N, FMC_D5	ADC34_IN6, COMP4_INM
40	PE9	I/O	TTa	(1)	EVENTOUT, TIM1_CH1, FMC_D6	ADC3_IN2
41	PE10	I/O	TTa	(1)	EVENTOUT, TIM1_CH2N, FMC_D7	ADC3_IN14
42	PE11	I/O	TTa	(1)	EVENTOUT, TIM1_CH2, SPI4_NSS, FMC_D8	ADC3_IN15

Table 12. STM32F398VE pin definitions (continued)

Pin number	Pin name	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	(function after reset)					
43	PE12	I/O	TTa	(1)	EVENTOUT, TIM1_CH3N, SPI4_SCK, FMC_D9	ADC3_IN16
44	PE13	I/O	TTa	(1)	EVENTOUT, TIM1_CH3, SPI4_MISO, FMC_D10	ADC3_IN3
45	PE14	I/O	TTa	(1)	EVENTOUT, TIM1_CH4, SPI4_MOSI, TIM1_BKIN2, FMC_D11	ADC4_IN1
46	PE15	I/O	TTa	(1)	EVENTOUT, TIM1_BKIN, USART3_RX, FMC_D12	ADC4_IN2
47	PB10	I/O	TTa	-	TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	COMP5_INM, OPAMP3_VINM, OPAMP4_VINM
48	PB11	I/O	TTa	-	TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC12_IN14, COMP6_INP, OPAMP4_VINP
49	VSS	S	-	-	-	-
50	VDD	S	-	-	-	-
51	PB12	I/O	TTa	(3)	TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	ADC4_IN3, COMP3_INM, OPAMP4_VOUT
52	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	ADC3_IN5, COMP5_INP, OPAMP3_VINP, OPAMP4_VINP
53	PB14	I/O	TTa	-	TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS, EVENTOUT	ADC4_IN4, COMP3_INP, OPAMP2_VINP
54	PB15	I/O	TTa	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	ADC4_IN5, COMP6_INM
55	PD8	I/O	TTa	(1)	EVENTOUT, USART3_TX, FMC_D13	ADC4_IN12, OPAMP4_VINM
56	PD9	I/O	TTa	(1)	EVENTOUT, USART3_RX, FMC_D14	ADC4_IN13
57	PD10	I/O	TTa	(1)	EVENTOUT, USART3_CK, FMC_D15	ADC34_IN7, COMP6_INM
58	PD11	I/O	TTa	(1)	EVENTOUT, USART3_CTS, FMC_A16	ADC34_IN8, OPAMP4_VINP

Table 12. STM32F398VE pin definitions (continued)

Pin number LQFP100	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
59	PD12	I/O	TTa	(1)	EVENTOUT, TIM4_CH1, TSC_G8_IO1, USART3_RTS, FMC_A17	ADC34_IN9
60	PD13	I/O	TTa	(1)	EVENTOUT, TIM4_CH2, TSC_G8_IO2, FMC_A18	ADC34_IN10, COMP5_INM
61	PD14	I/O	TTa	(1)	EVENTOUT, TIM4_CH3, TSC_G8_IO3, FMC_D0	ADC34_IN11, OPAMP2_VINP
62	PD15	I/O	TTa	(1)	EVENTOUT, TIM4_CH4, TSC_G8_IO4, SPI2_NSS, FMC_D1	COMP3_INM
63	PC6	I/O	FT	-	EVENTOUT, TIM3_CH1, TIM8_CH1, I2S2_MCK, COMP6_OUT	-
64	PC7	I/O	FT	-	EVENTOUT, TIM3_CH2, TIM8_CH2, I2S3_MCK, COMP5_OUT	-
65	PC8	I/O	FT	-	EVENTOUT, TIM3_CH3, TIM8_CH3, COMP3_OUT	-
66	PC9	I/O	FTf	-	EVENTOUT, TIM3_CH4, I2C3_SDA, TIM8_CH4, I2SCKIN, TIM8_BKIN2	-
67	PA8	I/O	FTf	-	MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, COMP3_OUT, TIM4_ETR, EVENTOUT	-
68	PA9	I/O	FTf	-	I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, COMP5_OUT, TIM15_BKIN, TIM2_CH3, EVENTOUT	-
69	PA10	I/O	FTf	-	TIM17_BKIN, TSC_G4_IO2, I2C2_SDA, SPI2_MISO/I2S2ext_SD, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, TIM8_BKIN, EVENTOUT	-
70	PA11	I/O	FT	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, CAN_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, EVENTOUT	-

Table 12. STM32F398VE pin definitions (continued)

Pin number LQFP100	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
71	PA12	I/O	FT	-	TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS, COMP2_OUT, CAN_TX, TIM4_CH2, TIM1_ETR, EVENTOUT	-
72	PA13	I/O	FT	-	SWDIO-JTMS, TIM16_CH1N, TSC_G4_IO3, IR-OUT, USART3_CTS, TIM4_CH3, EVENTOUT	-
74	VSS	S	-	-	-	-
75	VDD	S	-	-	-	-
76	PA14	I/O	FTf	-	SWCLK-JTCK, TSC_G4_IO4, I2C1_SDA, TIM8_CH2, TIM1_BKIN, USART2_TX, EVENTOUT	-
77	PA15	I/O	FTf	-	JTDI, TIM2_CH1/TIM2_ETR, TIM8_CH1, TSC_SYNC, I2C1_SCL, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_RX, TIM1_BKIN, EVENTOUT	-
78	PC10	I/O	FT	-	EVENTOUT, TIM8_CH1N, UART4_TX, SPI3_SCK/I2S3_CK, USART3_TX	-
79	PC11	I/O	FT	-	EVENTOUT, TIM8_CH2N, UART4_RX, SPI3_MISO/I2S3ext_SD, USART3_RX	-
80	PC12	I/O	FT	-	EVENTOUT, TIM8_CH3N, UART5_TX, SPI3_MOSI/I2S3_SD, USART3_CK	-
81	PD0	I/O	FT	(1)	EVENTOUT, CAN_RX, FMC_D2	-
82	PD1	I/O	FT	(1)	EVENTOUT, TIM8_CH4, TIM8_BKIN2, CAN_TX, FMC_D3	-
83	PD2	I/O	FT	-	EVENTOUT, TIM3_ETR, TIM8_BKIN, UART5_RX	-
84	PD3	I/O	FT	(1)	EVENTOUT, TIM2_CH1/TIM2_ETR, USART2_CTS, FMC_CLK	-

Table 12. STM32F398VE pin definitions (continued)

Pin number LQFP100	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
85	PD4	I/O	FT	(1)	EVENTOUT, TIM2_CH2, USART2_RTS, FMC_NOE	-
86	PD5	I/O	FT	(1)	EVENTOUT, USART2_TX, FMC_NWE	-
87	PD6	I/O	FT	(1)	EVENTOUT, TIM2_CH4, USART2_RX, FMC_NWAIT	-
88	PD7	I/O	FT	(1)	EVENTOUT, TIM2_CH3, USART2_CK, FMC_NE1/FMC_NCE2	-
89	PB3	I/O	FT	-	JTDO-TRACESWO, TIM2_CH2, TIM4_ETR, TSC_G5_IO1, TIM8_CH1N, SPI1_SCK, SPI3_SCK/I2S3_CK, USART2_TX, TIM3_ETR, EVENTOUT	-
90	PB4	I/O	FT	-	JTRST, TIM16_CH1, TIM3_CH1, TSC_G5_IO2, TIM8_CH2N, SPI1_MISO, SPI3_MISO/I2S3ext_SD, USART2_RX, TIM17_BKIN, EVENTOUT	-
91	PB5	I/O	FTf	-	TIM16_BKIN, TIM3_CH2, TIM8_CH3N, I2C1_SMBAI, SPI1_MOSI, SPI3_MOSI/I2S3_SD, USART2_CK, I2C3_SDA, TIM17_CH1, EVENTOUT	-
92	PB6	I/O	FTf	-	TIM16_CH1N, TIM4_CH1, TSC_G5_IO3, I2C1_SCL, TIM8_CH1, TIM8_ETR, USART1_TX, TIM8_BKIN2, EVENTOUT	-
93	PB7	I/O	FTf	-	TIM17_CH1N, TIM4_CH2, TSC_G5_IO4, I2C1_SDA, TIM8_BKIN, USART1_RX, TIM3_CH4, FMC_NADV, EVENTOUT	-
94	BOOT0	I	-	-	-	-
95	PB8	I/O	FTf	-	TIM16_CH1, TIM4_CH3, TSC_SYNC, I2C1_SCL, USART3_RX, COMP1_OUT, CAN_RX, TIM8_CH2, TIM1_BKIN, EVENTOUT	-

Table 12. STM32F398VE pin definitions (continued)

Pin number	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100						
96	PB9	I/O	FTf	-	TIM17_CH1, TIM4_CH4, I2C1_SDA, IR-OUT, USART3_TX, COMP2_OUT, CAN_TX, TIM8_CH3, EVENTOUT	-
97	PE0	I/O	FT	(1)	EVENTOUT, TIM4_ETR, TIM16_CH1, TIM20_ETR, USART1_TX, FMC_NBL0	-
98	PE1	I/O	FT	(1)	EVENTOUT, TIM17_CH1, TIM20_CH4, USART1_RX, FMC_NBL1	-
99	VSS	S		-	-	-
100	VDD	S		-	-	-

1. Function availability depends on the chosen device.

2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF
 - These GPIOs must not be used as current sources (e.g. to drive an LED)

 After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0316 reference manual.

3. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 13. STM32F398VE alternate function mapping

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port A	PA0	-	TIM2_CH1/TIM2_ETR	-	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR	-	-	-	-	EVENT OUT
	PA1	RTC_REFIN	TIM2_CH2	-	TSC_G1_IO2	-	-	-	USART2_RTS	-	TIM15_CH1N	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	-	TSC_G1_IO3	-	-	-	USART2_TX	COMP2_OUT	TIM15_CH1	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	-	TSC_G1_IO4	-	-	-	USART2_RX	-	TIM15_CH2	-	-	-	-	-	EVENT OUT
	PA4	-		TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	-	-	-	-	-	EVENT OUT
	PA5	-	TIM2_CH1/TIM2_ETR	-	TSC_G2_IO2	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	TIM8_BKIN	SPI1_MISO	TIM1_BKIN	-	COMP1_OUT	-	-	-	-	-	-	EVENT OUT
	PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N	-	-	-	-	-	-	-	-	EVENT OUT
	PA8	MCO	-	-	I2C3_SCL	I2C2_SMBAL	I2S2_MCK	TIM1_CH1	USART1_CK	COMP3_OUT	-	TIM4_ETR	-	-	-	-	EVENT OUT
	PA9	-	-	I2C3_SMBAL	TSC_G4_IO1	I2C2_SCL	I2S3_MCK	TIM1_CH2	USART1_TX	COMP5_OUT	TIM15_BKIN	TIM2_CH3	-	-	-	-	EVENT OUT

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port A	PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	SPI2_MISO/I2S2ext_SD	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	TIM8_BKIN	-	-	-	EVENT OUT
	PA11	-	-	-	-	-	SPI2_MOSI/I2S2_SD	TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	-	-	EVENT OUT
	PA12	-	TIM16_CH1	-	-	-	I2SCKIN	TIM1_CH2N	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2	TIM1_ETR	-	-	-	EVENT OUT
	PA13	SWDIO-JTMS	TIM16_CH1N	-	TSC_G4_IO3	-	IR-OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	-	-	EVENT OUT
	PA14	SWCLK-JTCK	-	-	TSC_G4_IO4	I2C1_SDA	TIM8_CH2	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	TIM8_CH1	TSC_SYNC	I2C1_SCL	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_RX	-	TIM1_BKIN	-	-	-	-	-	EVENT OUT
Port B	PB0	-	-	TIM3_CH3	TSC_G3_IO2	TIM8_CH2N	-	TIM1_CH2N	-	-	-	-	-	-	-	-	EVENT OUT
	PB1	-	-	TIM3_CH4	TSC_G3_IO3	TIM8_CH3N	-	TIM1_CH3N	-	COMP4_OUT	-	-	-	-	-	-	EVENT OUT
	PB3	JTDO-TRACESWO	TIM2_CH2	TIM4_ETR	TSC_G5_IO1	TIM8_CH1N	SPI1_SCK	SPI3_SCK/I2S3_CK	USART2_TX	-	-	TIM3_ETR	-	-	-	-	EVENT OUT

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/TIM8/20/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port B	PB4	JTRST	TIM16_CH1	TIM3_CH1	TSC_G5_IO2	TIM8_CH2N	SPI1_MISO	SPI3_MISO/I2S3ext_SD	USART2_RX	-	-	TIM17_BKIN	-	-	-	-	EVENTOUT
	PB5	-	TIM16_BKIN	TIM3_CH2	TIM8_CH3N	I2C1_SMBAl	SPI1_MOSI	SPI3_MOSI/I2S3_SD	USART2_CK	I2C3_SDA	-	TIM17_CH1	-	-	-	-	EVENTOUT
	PB6	-	TIM16_CH1N	TIM4_CH1	TSC_G5_IO3	I2C1_SCL	TIM8_CH1	TIM8_ETR	USART1_TX	-	-	TIM8_BKIN2	-	-	-	-	EVENTOUT
	PB7	-	TIM17_CH1N	TIM4_CH2	TSC_G5_IO4	I2C1_SDA	TIM8_BKIN	-	USART1_RX	-	-	TIM3_CH4	-	FMC_NADV	-	-	EVENTOUT
	PB8	-	TIM16_CH1	TIM4_CH3	TSC_SYNC	I2C1_SCL	-	-	USART3_RX	COMP1_OUT	CAN_RX	TIM8_CH2	-	TIM1_BKIN	-	-	EVENTOUT
	PB9	-	TIM17_CH1	TIM4_CH4	-	I2C1_SDA	-	IR-OUT	USART3_TX	COMP2_OUT	CAN_TX	TIM8_CH3	-	-	-	-	EVENTOUT
	PB10	-	TIM2_CH3	-	TSC_SYNC	-	-	-	USART3_TX	-	-	-	-	-	-	-	EVENTOUT
	PB11	-	TIM2_CH4	-	TSC_G6_IO1	-	-	-	USART3_RX	-	-	-	-	-	-	-	EVENTOUT
	PB12	-	-	-	TSC_G6_IO2	I2C2_SMBAL	SPI2_NSS/I2S2_WS	TIM1_BKIN	USART3_CK	-	-	-	-	-	-	-	EVENTOUT
	PB13	-	-	-	TSC_G6_IO3	-	SPI2_SCK/I2S2_CK	TIM1_CH1N	USART3_CTS	-	-	-	-	-	-	-	EVENTOUT

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port B	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	SPI2_MISO/I2S2ext_SD	TIM1_CH2N	USART3_RTS	-	-	-	-	-	-	-	EVENT OUT
	PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT
Port C	PC0	-	EVENT OUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC1	-	EVENT OUT	TIM1_CH2	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC2	-	EVENT OUT	TIM1_CH3	COMP7_OUT	-	-	-	-	-	-	-	-	-	-	-	-
	PC3	-	EVENT OUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
	PC4	-	EVENT OUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
	PC5	-	EVENT OUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
	PC6	-	EVENT OUT	TIM3_CH1	-	TIM8_CH1	-	I2S2_MCK	COMP6_OUT	-	-	-	-	-	-	-	-
	PC7	-	EVENT OUT	TIM3_CH2	-	TIM8_CH2	-	I2S3_MCK	COMP5_OUT	-	-	-	-	-	-	-	-
	PC8	-	EVENT OUT	TIM3_CH3	-	TIM8_CH3	-	-	COMP3_OUT	-	-	-	-	-	-	-	-
	PC9	-	EVENT OUT	TIM3_CH4	I2C3_SDA	TIM8_CH4	I2SCKIN	TIM8_BKIN2	-	-	-	-	-	-	-	-	-

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port C	PC10	-	EVENT OUT	-	-	TIM8_CH1N	UART4_TX	SPI3_SCK/I2S3_CK	USART3_TX	-	-	-	-	-	-	-	-
	PC11	-	EVENT OUT	-	-	TIM8_CH2N	UART4_RX	SPI3_MISO/I2S3ext_SD	USART3_RX	-	-	-	-	-	-	-	-
	PC12	-	EVENT OUT	-	-	TIM8_CH3N	UART5_TX	SPI3_MOSI/I2S3_SD	USART3_CK	-	-	-	-	-	-	-	-
	PC13	-	EVENT OUT	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port D	PD0	-	EVENT OUT	-	-	-	-	-	CAN_RX	-	-	-	-	FMC_D2	-	-	-
	PD1	-	EVENT OUT	-	-	TIM8_CH4	-	TIM8_BKIN2	CAN_TX	-	-	-	-	FMC_D3	-	-	-
	PD2	-	EVENT OUT	TIM3_ETR	-	TIM8_BKIN	UART5_RX	-	-	-	-	-	-	-	-	-	-
	PD3	-	EVENT OUT	TIM2_CH1/TIM2_ETR	-	-	-	-	USART2_CTS	-	-	-	-	FMC_CLK	-	-	-
	PD4	-	EVENT OUT	TIM2_CH2	-	-	-	-	USART2_RTS	-	-	-	-	FMC_NOE	-	-	-

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port D	PD5	-	EVENT OUT	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	-
	PD6	-	EVENT OUT	TIM2_CH4	-	-	-	-	USART2_RX	-	-	-	-	FMC_NWAIT	-	-	-
	PD7	-	EVENT OUT	TIM2_CH3	-	-	-	-	USART2_CK	-	-	-	-	FMC_NE1/FMC_NCE2	-	-	-
	PD8	-	EVENT OUT	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	-
	PD9	-	EVENT OUT	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	-
	PD10	-	EVENT OUT	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	-	-
	PD11	-	EVENT OUT	-	-	-	-	-	USART3_CTS	-	-	-	-	FMC_A16	-	-	-
	PD12	-	EVENT OUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS	-	-	-	-	FMC_A17	-	-	-
	PD13	-	EVENT OUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-	-	-	-	-	FMC_A18	-	-	-
	PD14	-	EVENT OUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-	-	-	-	-	FMC_D0	-	-	-
	PD15	-	EVENT OUT	TIM4_CH4	TSC_G8_IO4	-	-	SPI2_NSS	-	-	-	-	-	FMC_D1	-	-	-

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port E	PE0	-	EVENT OUT	TIM4_ETR	-	TIM16_CH1	-	TIM20_ETR	USART1_TX	-	-	-	-	FMC_NBL0	-	-	-
	PE1	-	EVENT OUT	-	-	TIM17_CH1	-	TIM20_CH4	USART1_RX	-	-	-	-	FMC_NBL1	-	-	-
	PE2	TRACECK	EVENT OUT	TIM3_CH1	TSC_G7_IO1	-	SPI4_SCK	TIM20_CH1	-	-	-	-	-	FMC_A23	-	-	-
	PE3	TRACED0	EVENT OUT	TIM3_CH2	TSC_G7_IO2	-	SPI4_NSS	TIM20_CH2	-	-	-	-	-	FMC_A19	-	-	-
	PE4	TRACED1	EVENT OUT	TIM3_CH3	TSC_G7_IO3	-	SPI4_NSS	TIM20_CH1N	-	-	-	-	-	FMC_A20	-	-	-
	PE5	TRACED2	EVENT OUT	TIM3_CH4	TSC_G7_IO4	-	SPI4_MISO	TIM20_CH2N	-	-	-	-	-	FMC_A21	-	-	-
	PE6	TRACED3	EVENT OUT	-	-	-	SPI4_MOSI	TIM20_CH3N	-	-	-	-	-	FMC_A22	-	-	-
	PE7	-	EVENT OUT	TIM1_ETR	-	-	-	-	-	-	-	-	-	FMC_D4	-	-	-
	PE8	-	EVENT OUT	TIM1_CH1N	-	-	-	-	-	-	-	-	-	FMC_D5	-	-	-
	PE9	-	EVENT OUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	FMC_D6	-	-	-
	PE10	-	EVENT OUT	TIM1_CH2N	-	-	-	-	-	-	-	-	-	FMC_D7	-	-	-
	PE11	-	EVENT OUT	TIM1_CH2	-	-	SPI4_NSS	-	-	-	-	-	-	FMC_D8	-	-	-

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port E	PE12	-	EVENT OUT	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	-	-
	PE13	-	EVENT OUT	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	-	-
	PE14	-	EVENT OUT	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	-	-	FMC_D11	-	-	-
	PE15	-	EVENT OUT	TIM1_BKIN	-	-	-	-	USART3_RX	-	-	-	-	FMC_D12	-	-	-
Port F	PF0	-	EVENT OUT	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	EVENT OUT	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	-
	PF2	-	EVENT OUT	TIM20_CH3	-	-	-	-	-	-	-	-	-	FMC_A2	-	-	-
	PF3	-	EVENT OUT	TIM20_CH4	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	-
	PF4	-	EVENT OUT	COMP1_OUT	TIM20_CH1N	-	-	-	-	-	-	-	-	FMC_A4	-	-	-
	PF5	-	EVENT OUT	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	-
	PF6	-	EVENT OUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS	-	-	-	-	FMC_NIORD	-	-	-
	PF7	-	EVENT OUT	TIM20_BKIN	-	-	-	-	-	-	-	-	-	FMC_NREG	-	-	-

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port F	PF8	-	EVENT OUT	TIM20_BKIN2	-	-	-	-	-	-	-	-	-	FMC_NIOWR	-	-	-
	PF9	-	EVENT OUT	TIM20_BKIN	TIM15_CH1	-	SPI2_SCK	-	-	-	-	-	-	FMC_CD	-	-	-
	PF10	-	EVENT OUT	TIM20_BKIN2	TIM15_CH2	-	SPI2_SCK	-	-	-	-	-	-	FMC_INTR	-	-	-
	PF11	-	EVENT OUT	TIM20_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-
	PF12	-	EVENT OUT	TIM20_CH1	-	-	-	-	-	-	-	-	-	FMC_A6	-	-	-
	PF13	-	EVENT OUT	TIM20_CH2	-	-	-	-	-	-	-	-	-	FMC_A7	-	-	-
	PF14	-	EVENT OUT	TIM20_CH3	-	-	-	-	-	-	-	-	-	FMC_A8	-	-	-
	PF15	-	EVENT OUT	TIM20_CH4	-	-	-	-	-	-	-	-	-	FMC_A9	-	-	-
Port G	PG0	-	EVENT OUT	TIM20_CH1N	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	-
	PG1	-	EVENT OUT	TIM20_CH2N	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	-
	PG2	-	EVENT OUT	TIM20_CH3N	-	-	-	-	-	-	-	-	-	FMC_A12	-	-	-
	PG3	-	EVENT OUT	TIM20_BKIN	-	-	-	-	-	-	-	-	-	FMC_A13	-	-	-
	PG4	-	EVENT OUT	TIM20_BKIN2	-	-	-	-	-	-	-	-	-	FMC_A14	-	-	-

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port G	PG5	-	EVENT OUT	TIM20_ETR	-	-	-	-	-	-	-	-	-	-	FMC_A15	-	-	-
	PG6	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_INT2	-	-	-
	PG7	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_INT3	-	-	-
	PG8	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PG9	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_NE2/FMC_NCE3	-	-	-
	PG10	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_1/FMC_NE3	-	-	-
	PG11	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_2	-	-	-
	PG12	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_NE4	-	-	-
	PG13	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_A24	-	-	-
	PG14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	FMC_A25	-	-	-
	PG15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 13. STM32F398VE alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3/TIM8/20/15/GPCOMP7/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/TIM8/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP3/5/6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	SDIO/FMC/TIM1	-	-	EVENT
Port H	PH0	-	EVENT OUT	TIM20_CH1	-	-	-	-	-	-	-	-	-	FMC_A0	-	-	-
	PH1	-	EVENT OUT	TIM20_CH2	-	-	-	-	-	-	-	-	-	FMC_A1	-	-	-
	PH2	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-

5   Memory mapping

Figure 5. STM32F398VE memory map

MSv35523V1
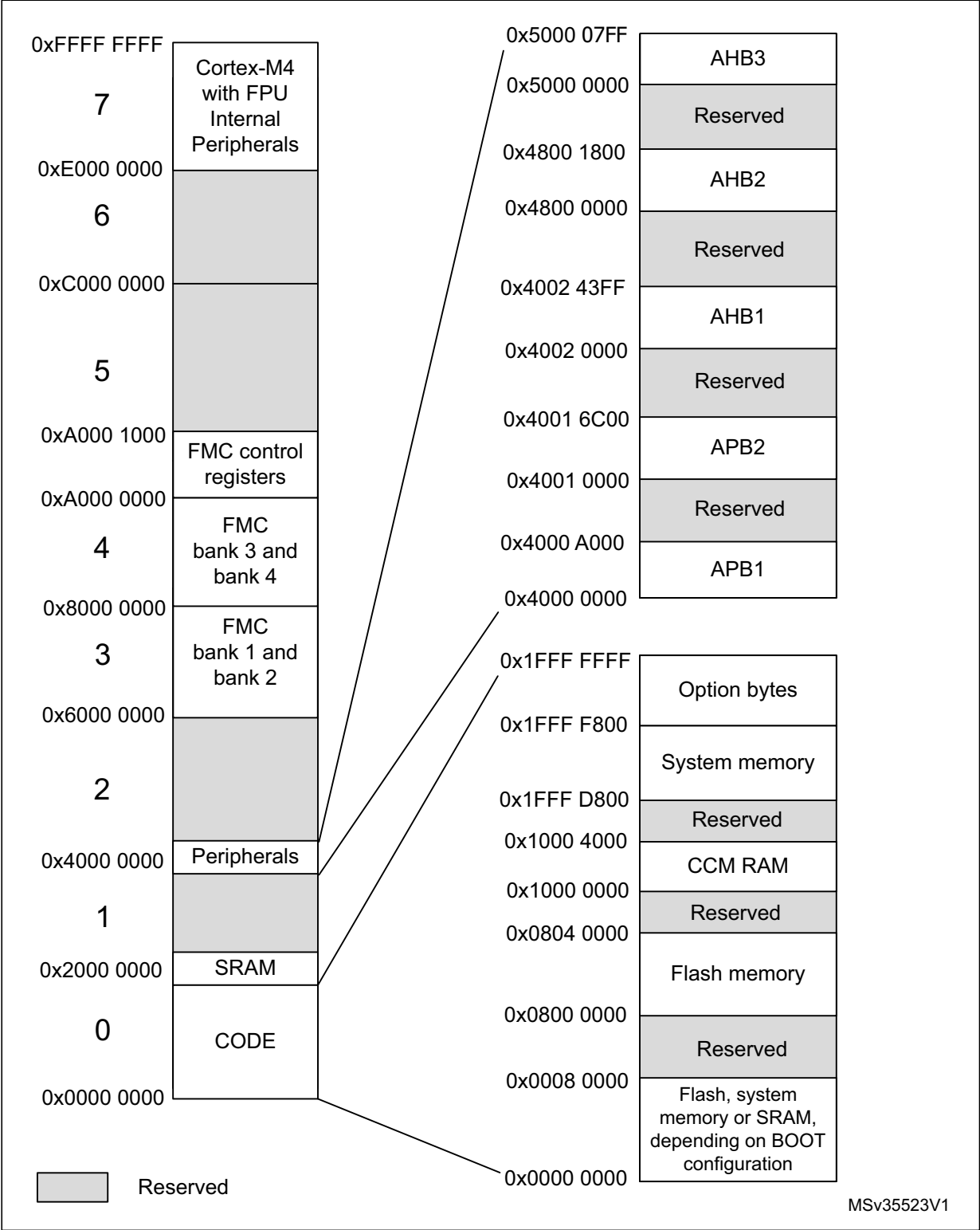
Table 14. Memory map, peripheral register boundary addresses

Bus	Boundary address	Size (bytes)	Peripheral
AHB4	0xA000 0000 - 0xA000 0FFF	4 K	FMC control registers
	0x8000 0000 - 0x9FFF FFFF	512 M	FMC Banks 3 and 4
	0x6000 0000 - 0x7FFF FFFF	512 M	FMC Banks 1 and 2
	0x5000 0800 - 0x5FFF FFFF	384 M	Reserved
AHB3	0x5000 0400 - 0x5000 07FF	1 K	ADC3 - ADC4
	0x5000 0000 - 0x5000 03FF	1 K	ADC1 - ADC2
	0x4800 2000 - 0x4FFF FFFF	~132 M	Reserved
AHB2	0x4800 1C00 - 0x4800 1FFF	1 K	GPIOH
	0x4800 1800 - 0x4800 1BFF	1 K	GPIOG
	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 M	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 K	TSC
	0x4002 3400 - 0x4002 3FFF	3 K	Reserved
	0x4002 3000 - 0x4002 33FF	1 K	CRC
	0x4002 2400 - 0x4002 2FFF	3 K	Reserved
	0x4002 2000 - 0x4002 23FF	1 K	Flash interface
	0x4002 1400 - 0x4002 1FFF	3 K	Reserved
	0x4002 1000 - 0x4002 13FF	1 K	RCC
	0x4002 0800 - 0x4002 0FFF	2 K	Reserved
	0x4002 0400 - 0x4002 07FF	1 K	DMA2
	0x4002 0000 - 0x4002 03FF	1 K	DMA1

Table 14. Memory map, peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
	0x4001 8000 - 0x4001 FFFF	32 K	Reserved
	0x4001 5400 - 0x4001 7FFF	11 K	Reserved
	0x4001 5000 - 0x4001 53FF	1 K	TIM20
	0x4001 4C00 - 0x4001 4FFF	1 K	Reserved
	0x4001 4800 - 0x4001 4BFF	1 K	TIM17
	0x4001 4400 - 0x4001 47FF	1 K	TIM16
	0x4001 4000 - 0x4001 43FF	1 K	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 K	SPI4
	0x4001 3800 - 0x4001 3BFF	1 K	USART1
	0x4001 3400 - 0x4001 37FF	1 K	TIM8
	0x4001 3000 - 0x4001 33FF	1 K	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
	0x4000 7C00 - 0x4000 FFFF	32 K	Reserved

Table 14. Memory map, peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 7800 - 0x4000 7BFF	1 K	I2C3
	0x4000 7400 - 0x4000 77FF	1 K	DAC
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	CAN SRAM
	0x4000 5C00 - 0x4000 5FFF	1 K	Reserved
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1400 - 0x4000 17FF	1 K	TIM7
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V, V_{DDA} = 3.3 VV. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves
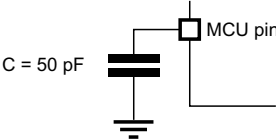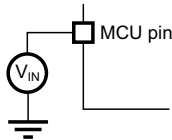
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions	Figure 7. Pin input voltage

6.1.6 Power supply scheme

Figure 8. Power supply scheme
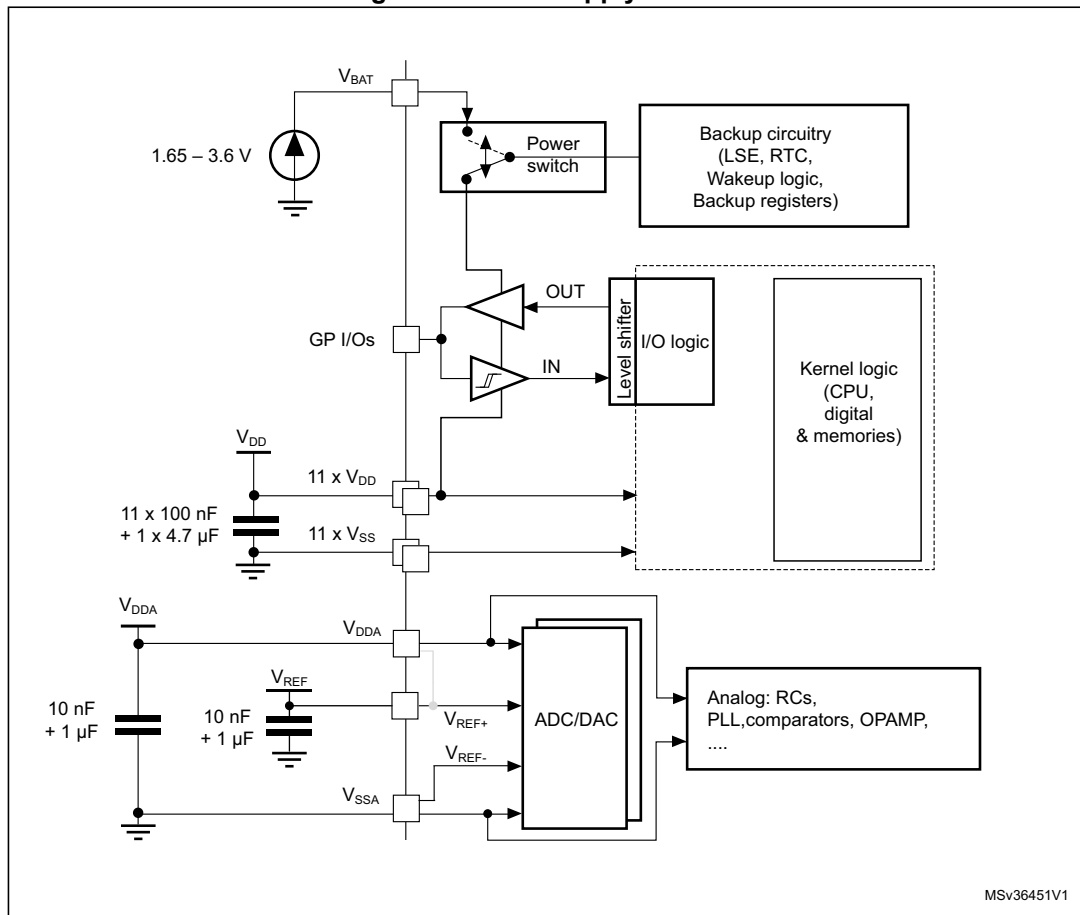
1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme

MS31435V1
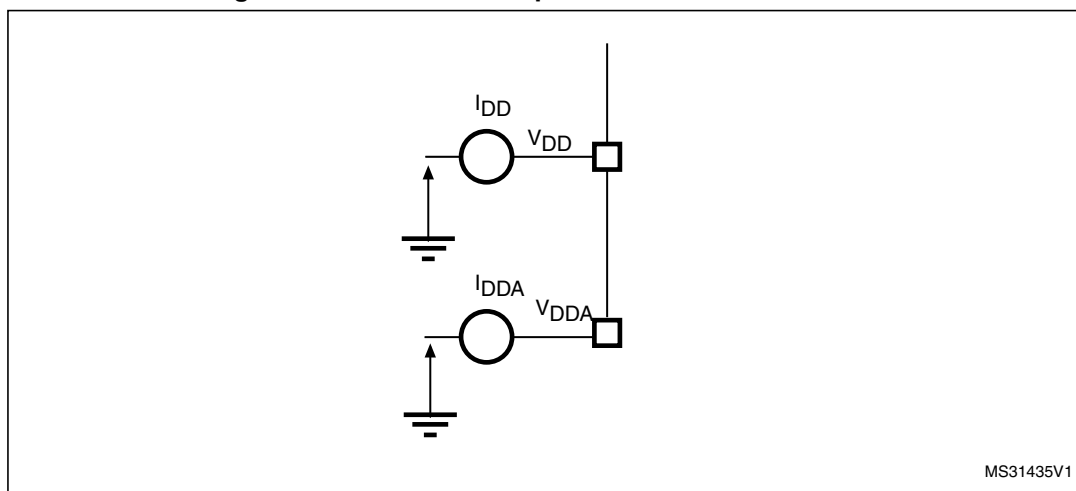
6.2   Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics*, and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 15. Voltage characteristics[1]

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including $V_{DDA,}$ V_{BAT} and V_{DD})	-0.3	1.95	V
V_{DDA}–V_{SS}	External main supply voltage	-0.3	4.0	
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	
V_{REF+}–V_{DDA}[2]	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	
V_{IN}[3]	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DD} + 4.0$	V
	Input voltage on TTa and TT pins	$V_{SS} - 0.3$	4.0	
	Input voltage on POR pin	$V_{SS} - 0.3$	$V_{DDA} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
	Input voltage on Boot0 pin	0	9	
$|\Delta V_{DDx}|$	Variations between different V_{DD} power pins	-	50	mV
$|V_{SSX} - V_{SS}|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range. The following relationship must be respected between V_{DDA} and V_{DD}:
    V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence.
    V_{DDA} must be greater than or equal to V_{DD}.

2. V_{REF+} must be always lower or equal than V_{DDA} ($V_{REF+} \leq V_{DDA}$). If unused then it must be connected to V_{DDA}.

3. V_{IN} maximum must always be respected. Refer to *Table 16: Current characteristics* for the maximum allowed injected current values.

Table 16. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	160	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	-160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)[1]	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)[1]	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins[2]	80	
	Total output current sourced by sum of all IOs and control pins[2]	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf, and B pins[3]	-5/+0	
	Injected current on TC and RST pin[4]	±5	
	Injected current on TTa pins[5]	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)[6]	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.

4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15: Voltage characteristics* for the maximum allowed input voltage values.

5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 15: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note [2] below *Table 76*.

6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 18. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	1.65	1.95	V
V_{DDA}	Analog operating voltage (OPAMP and DAC not used)	Must have a potential equal to or higher than V_{DD}	1.65	3.6	V
	Analog operating voltage (OPAMP and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC I/O	-0.3	V_{DD}+0.3	V
		TT I/O[1]	-0.3	3.6	
		TTa I/O pins and POR pin	-0.3	V_{DDA}+0.3	
		FT and FTf I/O[1]	-0.3	5.2	
		BOOT0	0	5.2	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7[2]	LQFP100	-	476	mW
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	85	°C
		Low power dissipation[3]	-40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	105	°C
		Low power dissipation[3]	-40	125	
T_J	Junction temperature range	6 suffix version	-40	105	°C
		7 suffix version	-40	125	

1. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.

2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics*).

3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.2: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 19* are derived from tests performed under the ambient temperature condition summarized in *Table 18*.

Table 19. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reference voltage

The parameters given in *Table 20* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 20. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24[1]	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	2.2	-	-	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10[2]	mV
T_{Coeff}	Temperature coefficient	-	-	-	100[2]	ppm/°C

1. Data based on characterization results, not tested in production.

2. Guaranteed by design, not tested in production.

Table 21. Internal reference voltage calibration values

Calibration value name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: *The total current consumption is the sum of I_{DD} and I_{DDA}.*

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When $f_{HCLK} > 8$ MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 22* to *Table 26* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18*.

Table 22. Typical and maximum current consumption from V$_{DD}$ supply at V$_{DD}$ = 1.8 V

Symbol	Parameter	Conditions	f$_{HCLK}$	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T$_A$[1]			Typ	Max @ T$_A$[1]			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I$_{DD}$	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	61.5	68.9	69.3	69.7	28.4	31.2	31.7	32.3	mA
			64 MHz	55.0	60.0	61.1	62.5	25.5	27.9	28.3	28.5	
			48 MHz	41.9	46.6	47.2	47.9	19.5	21.1	21.5	21.8	
			32 MHz	28.5	31.1	31.6	32.0	13.3	14.4	14.7	15.0	
			24 MHz	21.9	23.7	24.3	24.6	10.4	11.3	11.5	11.7	
			8 MHz	7.8	8.2	8.4	8.9	3.95	4.33	4.43	4.60	
			1 MHz	1.82	2.16	2.27	2.40	1.31	1.66	1.69	1.79	
		Internal clock (HSI)	64 MHz	51.9	56.5	56.9	57.2	25.6	28.0	28.2	28.4	
			48 MHz	39.3	42.9	43.4	43.6	19.4	21.1	21.3	21.4	
			32 MHz	26.9	29.3	29.7	29.9	13.4	14.6	14.7	14.9	
			24 MHz	20.9	21.6	21.9	22.2	10.7	11.1	11.2	11.3	
			8 MHz	7.8	8.3	8.4	8.5	4.22	4.82	4.96	5.30	
I$_{DD}$	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	61.3	68.8	69.2	69.6	28.3	31.1	31.6	32.2	
			64 MHz	54.8	59.9	61.0	62.4	25.3	27.8	28.2	28.4	
			48 MHz	41.7	46.5	47.1	47.7	19.2	21.0	21.4	21.6	
			32 MHz	28.2	30.9	31.4	31.8	13.0	14.3	14.6	14.7	
			24 MHz	21.4	23.5	23.8	24.2	9.9	11.0	11.1	11.2	
			8 MHz	7.45	7.92	7.97	8.17	3.57	3.96	4.08	4.19	
			1 MHz	1.29	1.59	1.72	1.91	0.89	1.21	1.26	1.40	
		Internal clock (HSI)	64 MHz	51.4	56.3	56.8	57.0	25.2	27.8	28.0	28.1	
			48 MHz	39.1	42.8	43.3	43.5	19.1	21.0	21.2	21.3	
			32 MHz	26.5	29.2	29.4	29.6	13.0	13.6	13.7	13.8	
			24 MHz	20.3	21.0	21.2	21.5	10.0	10.4	10.5	10.6	
			8 MHz	7.29	7.76	7.86	7.98	3.65	4.02	4.09	4.16	

Table 22. Typical and maximum current consumption from V$_{DD}$ supply at V$_{DD}$ = 1.8 V (continued)

Symbol	Parameter	Conditions	f$_{HCLK}$	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T$_A$[1]			Typ	Max @ T$_A$[1]			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I$_{DD}$	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	72 MHz	43.6	47.4	48.6	49.0	7.0	7.6	7.90	8.20	mA
			64 MHz	38.9	42.3	43.5	43.8	6.30	6.90	7.20	7.40	
			48 MHz	29.5	32.1	33.1	34.1	4.80	5.30	5.50	5.90	
			32 MHz	20.0	21.8	22.5	22.7	3.40	3.70	4.00	4.30	
			24 MHz	15.2	16.7	17.1	17.3	2.60	3.00	3.10	3.60	
			8 MHz	5.36	5.71	5.81	6.03	1.16	1.54	1.65	1.80	
			1 MHz	1.11	1.47	1.51	1.66	0.59	0.97	1.06	1.15	
		Internal clock (HSI)	64 MHz	35.3	38.5	39.1	39.4	6.10	6.70	6.80	7.10	
			48 MHz	26.8	29.2	29.8	30.0	4.60	5.10	5.20	5.60	
			32 MHz	18.2	20.0	20.2	20.4	3.20	3.70	3.80	4.10	
			24 MHz	14.0	14.6	14.7	15.1	2.68	3.11	3.16	3.27	
			8 MHz	5.18	5.57	5.70	5.82	1.21	1.54	1.61	1.67	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 23. Typical and maximum current consumption from the V$_{DDA}$ supply

Symbol	Parameter	Conditions [1]	f$_{HCLK}$	V$_{DDA}$ = 2.4 V				V$_{DDA}$ = 3.6 V				Unit
				Typ	Max @ T$_A$[2]			Typ	Max @ T$_A$[2]			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I$_{DDA}$	Supply current in Run mode, code executing from Flash or RAM	HSE bypass	72 MHz	240	263	279	286	219	242	254	259	µA
			64 MHz	211	232	246	252	193	214	225	230	
			48 MHz	156	174	186	191	144	162	171	175	
			32 MHz	107	122	129	132	99	115	120	123	
			24 MHz	83	96	101	103	77	91	95	96	
			8 MHz	1.2	2.4	2.9	4.1	0.8	2.0	2.5	3.3	
			1 MHz	1.2	2.4	2.9	4.1	0.8	2.0	2.5	3.3	
		HSI clock	64 MHz	294	319	334	339	265	289	300	305	
			48 MHz	239	260	273	278	215	236	245	249	
			32 MHz	189	207	216	220	169	187	194	197	
			24 MHz	165	181	188	191	147	163	169	171	
			8 MHz	83	91	94	95	69	77	80	81	

1. Current consumption from the V$_{DDA}$ supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I$_{DDA}$ is independent from the frequency.

2. Data based on characterization results, not tested in production.

Table 24. Typical and maximum V$_{DD}$ consumption in Stop mode

Symbol	Parameter	Conditions	Typ @V$_{DD}$ (V$_{DD}$= 1.8 V, V$_{DDA}$ = 3.3 V)	Max			Unit
			1.8 V	T$_A$ = 25 °C	T$_A$ = 85 °C	T$_A$ = 105 °C	
I$_{DD}$	Supply current in Stop mode	All oscillators OFF	8.6	22.4	418	927	µA

Table 25. Typical and maximum V$_{DDA}$ consumption in Stop mode

Symbol	Parameter	Conditions	Typ @V$_{DD}$ (V$_{DD}$ = 1.8 V)							Max			Unit
			1.8 V	2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T$_A$ = 25 °C	T$_A$ = 85 °C	T$_A$ = 105 °C	
I$_{DDA}$	Supply current in Stop mode	All oscillators OFF	0.72	0.73	0.75	0.78	0.83	0.90	0.98	9.3	9.6	10.6	µA

Table 26. Typical and maximum current consumption from V$_{BAT}$ supply

Symbol	Parameter	Conditions [1]	Typ @V$_{BAT}$								Max @V$_{BAT}$ = 3.6 V[2]			Unit
			1.65V	1.8V	2V	2.4V	2.7V	3V	3.3V	3.6V	T$_A$ = 25°C	T$_A$ = 85°C	T$_A$ = 105°C	
I$_{DD\_VBAT}$	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.48	0.50	0.52	0.58	0.65	0.72	0.80	0.90	1.1	1.5	2.0	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.83	0.86	0.90	0.98	1.03	1.10	1.20	1.30	1.5	2.2	2.9	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a CL of 6 pF for typical values.

2. Data based on characterization results, not tested in production.

Figure 10. Typical V$_{BAT}$ current consumption (LSE and RTC ON/LSEDRV[1:0] 00')
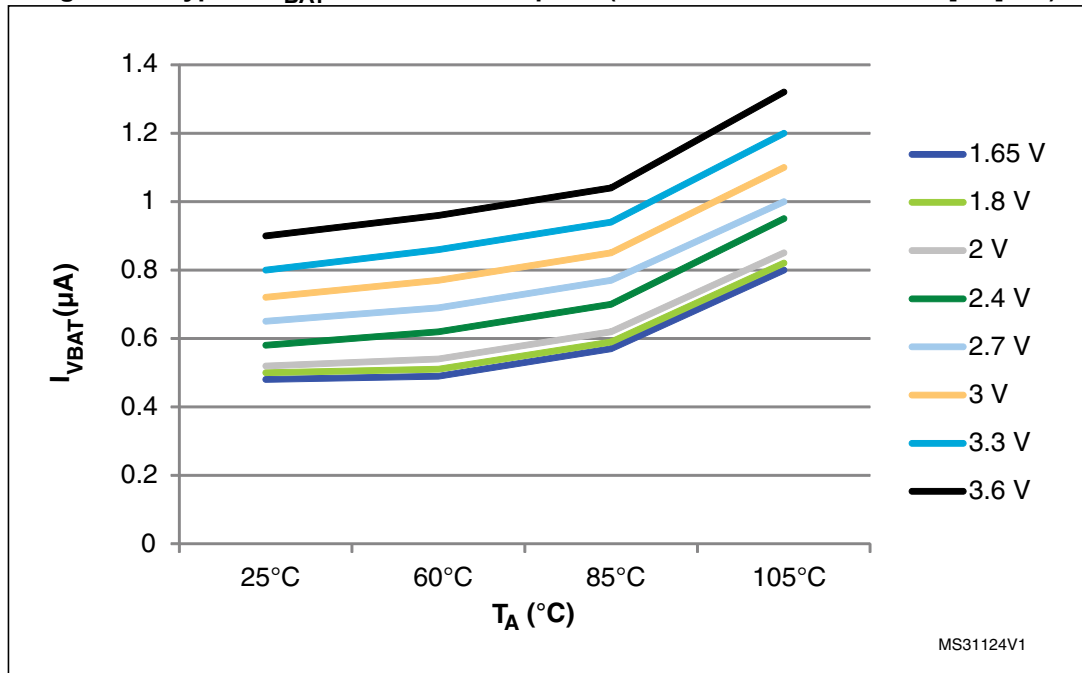
Typical current consumption

The MCU is placed under the following conditions:

- V$_{DD}$ = 1.8 V, V$_{DDA}$ = 3.3 V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f$_{HCLK}$ frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, f$_{APB1}$ = f$_{AHB/2}$, f$_{APB2}$ = f$_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 27. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	**Peripherals disabled**	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	72 MHz	60.6	27.2	mA
			64 MHz	54.3	24.4	
			48 MHz	42.3	19.0	
			32 MHz	28.6	13.1	
			24 MHz	22.0	10.3	
			16 MHz	14.6	7.10	
			8 MHz	7.42	3.67	
			4 MHz	4.27	2.15	
			2 MHz	2.46	1.33	
			1 MHz	1.55	0.92	
			500 kHz	1.10	0.71	
			125 kHz	0.75	0.56	
I_{DDA} [1]	Supply current in Run mode from V_{DDA} supply		72 MHz	241.0		µA
			64 MHz	211.7		
			48 MHz	156.8		
			32 MHz	106.5		
			24 MHz	82.6		
			16 MHz	58.6		
			8 MHz	0.9		
			4 MHz	0.9		
			2 MHz	0.9		
			1 MHz	0.9		
			500 kHz	0.9		
			125 kHz	0.9		

1. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.

Table 28. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	72 MHz	43.2	6.8	mA
			64 MHz	38.3	6.1	
			48 MHz	29.0	4.6	
			32 MHz	19.6	3.1	
			24 MHz	14.8	2.41	
			16 MHz	9.88	1.68	
			8 MHz	4.83	0.74	
			4 MHz	2.94	0.64	
			2 MHz	1.79	0.56	
			1 MHz	1.22	0.52	
			500 kHz	0.93	0.50	
			125 kHz	0.72	0.48	
I_{DDA}[1]	Supply current in Sleep mode from V_{DDA} supply		72 MHz	241.0		μA
			64 MHz	211.7		
			48 MHz	156.8		
			32 MHz	106.5		
			24 MHz	82.6		
			16 MHz	58.6		
			8 MHz	0.90		
			4 MHz	0.90		
			2 MHz	0.90		
			1 MHz	0.90		
			500 kHz	0.90		
			125 kHz	0.90		

1. When peripherals are enabled, the power consumption of the analog part of peripherals such as ADC, DAC, Comparators, OpAmp etc. is not included. Refer to the tables of characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 62: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 30: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: C = C_{INT}+ C_{EXT}+C_S

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 29. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and V_{DD} = 1.8 V, V_{DDA} = 3.3 VV_{DD} = V_{DDA} = 3.3 V.

Table 30. Peripheral current consumption

Peripheral	Typical consumption[1]	Unit
	I_{DD}	
BusMatrix [2]	8.3	µA/MHz
DMA1	7.0	
DMA2	5.4	
FMC	35.0	
CRC	1.5	
GPIOH	1.3	
GPIOA	5.4	
GPIOB	5.3	
GPIOC	5.4	
GPIOD	5.0	
GPIOE	5.4	
GPIOF	5.2	
GPIOG	5.0	
TSC	5.2	
ADC1&2	15.4	
ADC3&4	16.2	
APB2-Bridge [3]	3.1	
SYSCFG	4.0	
TIM1	26.0	
SPI1	6.2	
TIM8	26.4	
USART1	17.7	
SPI4	6.2	
TIM15	11.9	
TIM16	8.0	
TIM17	8.5	
TIM20	25.3	

Table 30. Peripheral current consumption (continued)

Peripheral	Typical consumption[1]	Unit
	I_{DD}	
APB1-Bridge [3]	6.7	µA/MHz
TIM2	39.2	
TIM3	30.8	
TIM4	31.3	
TIM6	4.3	
TIM7	4.3	
WWDG	1.3	
SPI2	33.6	
SPI3	33.9	
USART2	39.3	
USART3	39.3	
UART4	29.8	
UART5	27.0	
I2C1	6.7	
I2C2	6.4	
CAN	25.6	
PWR	3.7	
DAC	22.1	
I2C3	6.8	

1. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC, DAC, Comparators, OpAmp is not included. Refer to the tables of characteristics in the subsequent sections.

2. BusMatrix is automatically active when at least one master is ON (CPU, DMA1 or DMA2).

3. The APBx bridge is automatically active when at least one peripheral is ON on the same bus.

6.3.5 Wakeup time from low-power mode

The wakeup times given in *Table 31* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep mode: the wakeup event is WFE.
- WKUP1 (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 31. Low-power mode wakeup timings

Symbol	Parameter	Typ @V_{DD} = 1.8 V, V_{DDA} = 3.3V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode	4.98	5.7	µs
$t_{WUSLEEP}$	Wakeup from sleep mode	6.0	-	CPU clock cycle
t_{WUPOR}	Wakeup from power-off mode	91	139	µs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 11*.

Table 32. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency[1]		1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time[1]		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time[1]		-	-	20	

1. Guaranteed by design, not tested in production.

Figure 11. High-speed external clock source AC timing diagram

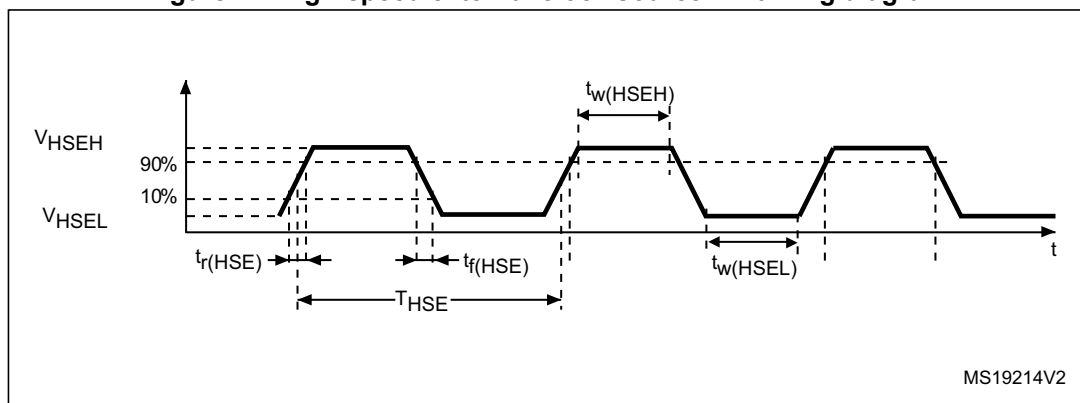### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12*

Table 33. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency[1]		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time[1]		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time[1]		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 12. Low-speed external clock source AC timing diagram

MS19215V2
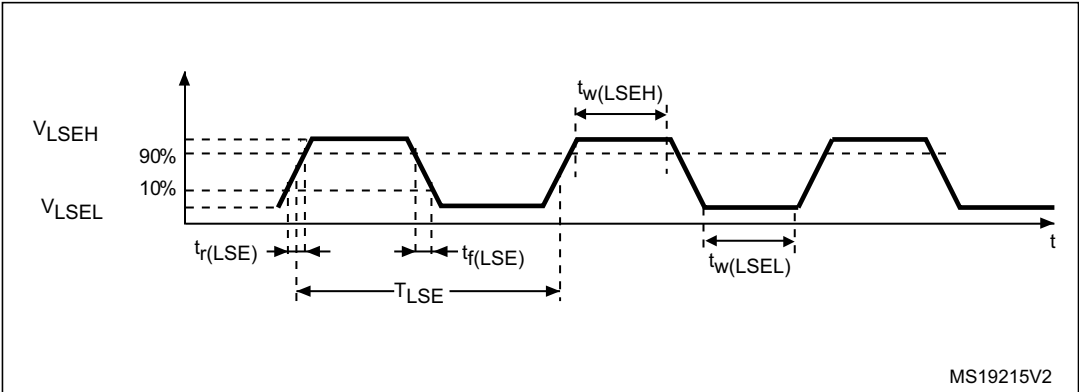
High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 34*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 34. HSE oscillator characteristics

Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200		$k\Omega$
I_{DD}	HSE current consumption	During startup[3]	-	-	8.5	mA
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}= 3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by design, not tested in production.

3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.

4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 13*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: *For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

Figure 13. Typical application with an 8 MHz crystal
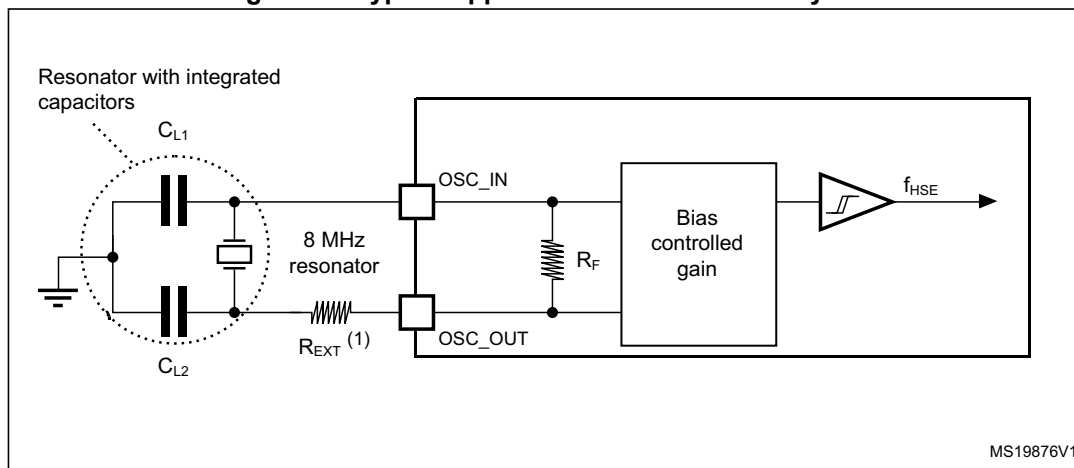
1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 35*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	μA
		LSEDRV[1:0]=01 medium low driving capability	-	-	1	
		LSEDRV[1:0]=10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	μA/V
		LSEDRV[1:0]=01 medium low driving capability	8	-	-	
		LSEDRV[1:0]=10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$[3]	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".

2. Guaranteed by design, not tested in production.

3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

Note: *For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

Figure 14. Typical application with a 32.768 kHz crystal
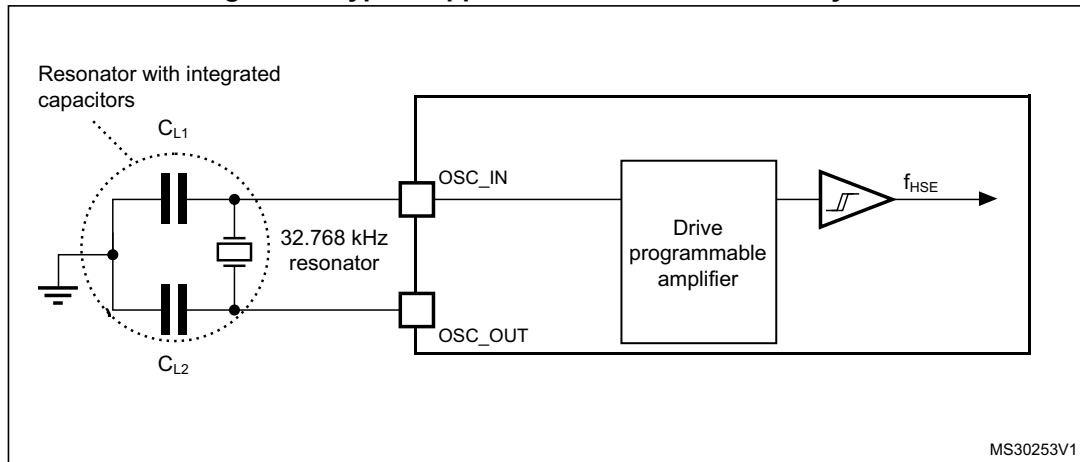
Note: *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

6.3.7 Internal clock source characteristics

The parameters given in *Table 36* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18*.

High-speed internal (HSI) RC oscillator

Table 36. HSI oscillator characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1[2]	%
$DuCy_{(HSI)}$	Duty cycle	-	45[2]	-	55[2]	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8[3]	-	3.8[3]	%
		T_A = -10 to 85°C	-1.9[3]	-	2.3[3]	
		T_A = 0 to 85°C	-1.9[3]	-	2[3]	
		T_A = 0 to 70°C	-1.3[3]	-	2[3]	
		T_A = 0 to 55°C	-1[3]	-	2[3]	
		T_A = 25°C[4]	-1	-	1	
$t_{SU(HSI)}$	HSI oscillator startup time	-	1[2]	-	2[2]	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-		80	100[2]	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 15. HSI oscillator accuracy characterization results for soldered parts

Low-speed internal (LSI) RC oscillator

Table 37. LSI oscillator characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$[2]	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$[2]	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

6.3.8 PLL characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18*.
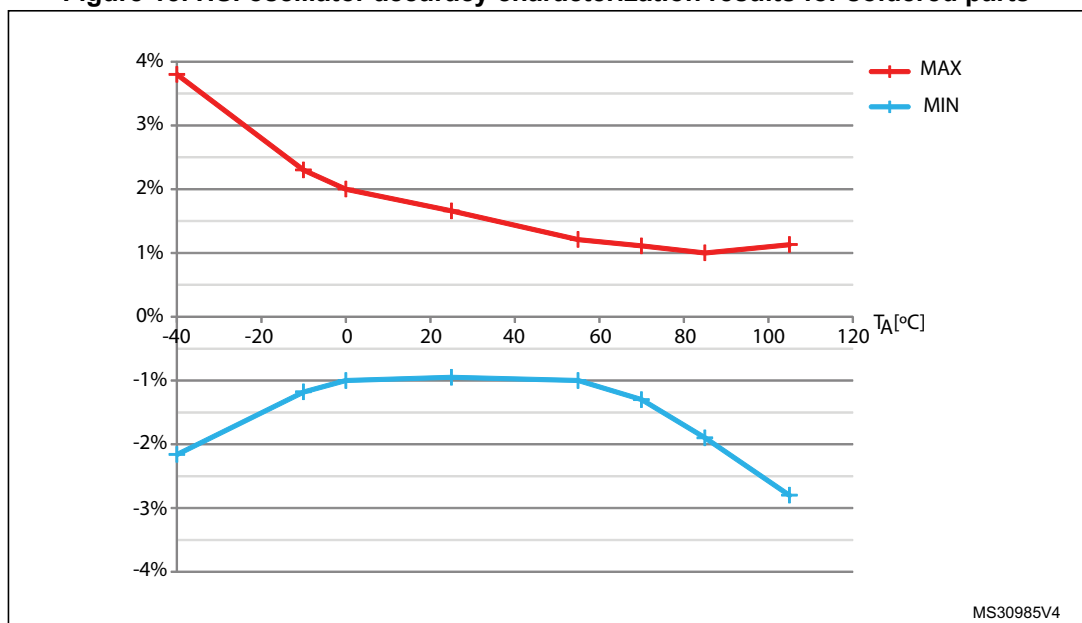
Table 38. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock[1]	1[2]	-	24[2]	MHz
	PLL input clock duty cycle	40[2]	-	60[2]	%
f_{PLL_OUT}	PLL multiplier output clock	16[2]	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200[2]	µs
Jitter	Cycle-to-cycle jitter	-	-	300[2]	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

2. Guaranteed by design, not tested in production.

6.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 39. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 40. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value Min[1]	Unit
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	10	
		10 kcycle[2] at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.10 FMC characteristics

Unless otherwise specified, the parameters given in *Table 41* to *Table 56* for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in *Table 18* with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5VDD

Refer to *Section 6.3.14: I/O port characteristics*: for more details on the input/output characteristics.

Asynchronous waveforms and timings

Figure 16 to *Figure 19* represent asynchronous waveforms and *Table 41* to *Table 48* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x4
- AddressHoldTime = 0x1
- DataSetupTime = 0x4 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- NOR NWAIT pulse width= 1THCLK

In all the timing tables, the T_{HCLK} is the HCLK clock period.

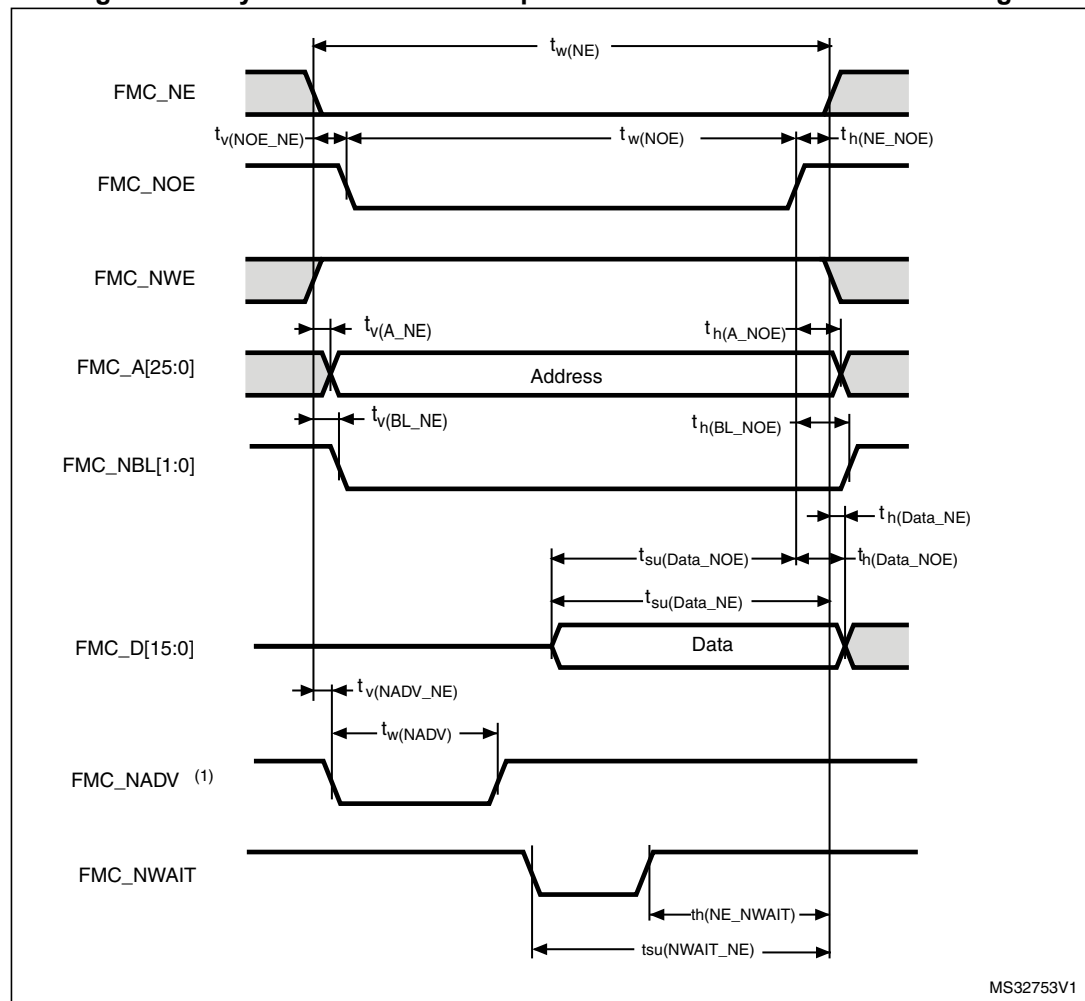### Figure 16. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

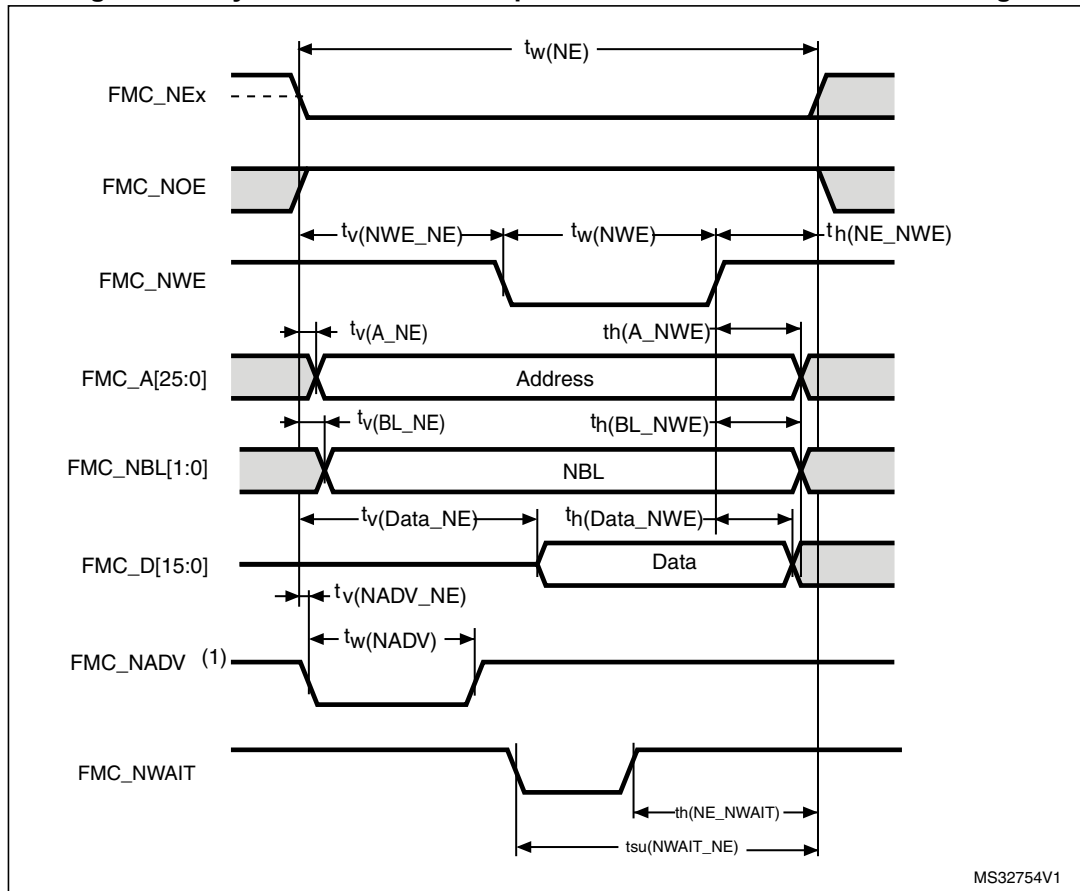**Table 41. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings[1]**

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8THCLK– 1	8THCLK+1	
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	0	1	
$t_{w(NOE)}$	FMC_NOE low time	8THCLK	8THCLK+ 1.5	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2 (NA)	ns
$t_{h(BL\_NOE)}$	FMC_BL hold time after FMC_NOE high	0	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	THCLK + 6	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOEx high setup time	THCLK +7	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	2	
$t_{w(NADV)}$	FMC_NADV low time	-	4THCLK +1.5	

1. Based on characterization, not tested in production

Table 42. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	10THCLK +0.5	10THCLK+ 1	
$t_{w(NOE)}$	FMC_NWE low time	6THCLK -1.5	6THCLK +2	ns
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	4THCLK +15	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK-3	-	

1. Based on characterization, not tested in production

Figure 17. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 43. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9THCLK-1	9THCLK+2	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK+0.5	THCLK+1	
$t_{w(NWE)}$	FMC_NWE low time	4THCLK-2	4THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	THCLK+ 3	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK+0.5	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	2.5	
$t_{w(NADV)}$	FMC_NADV low time	-	4THCLK+2	

1. Based on characterization, not tested in production

Table 44. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	11THCLK+1	11THCLK+2	
$t_{w(NWE)}$	FMC_NWE low time	6THCLK-1	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK-0.5	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK+2	-	

1. Based on characterization, not tested in production

Table 45. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	11THCLK+2	11THCLK+2	
$t_{w(NOE)}$	FMC_NWE low time	6THCLK-1	6THCLK+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	4THCLK+14	-	ns
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK-4	-	

1. Based on characterization, not tested in production
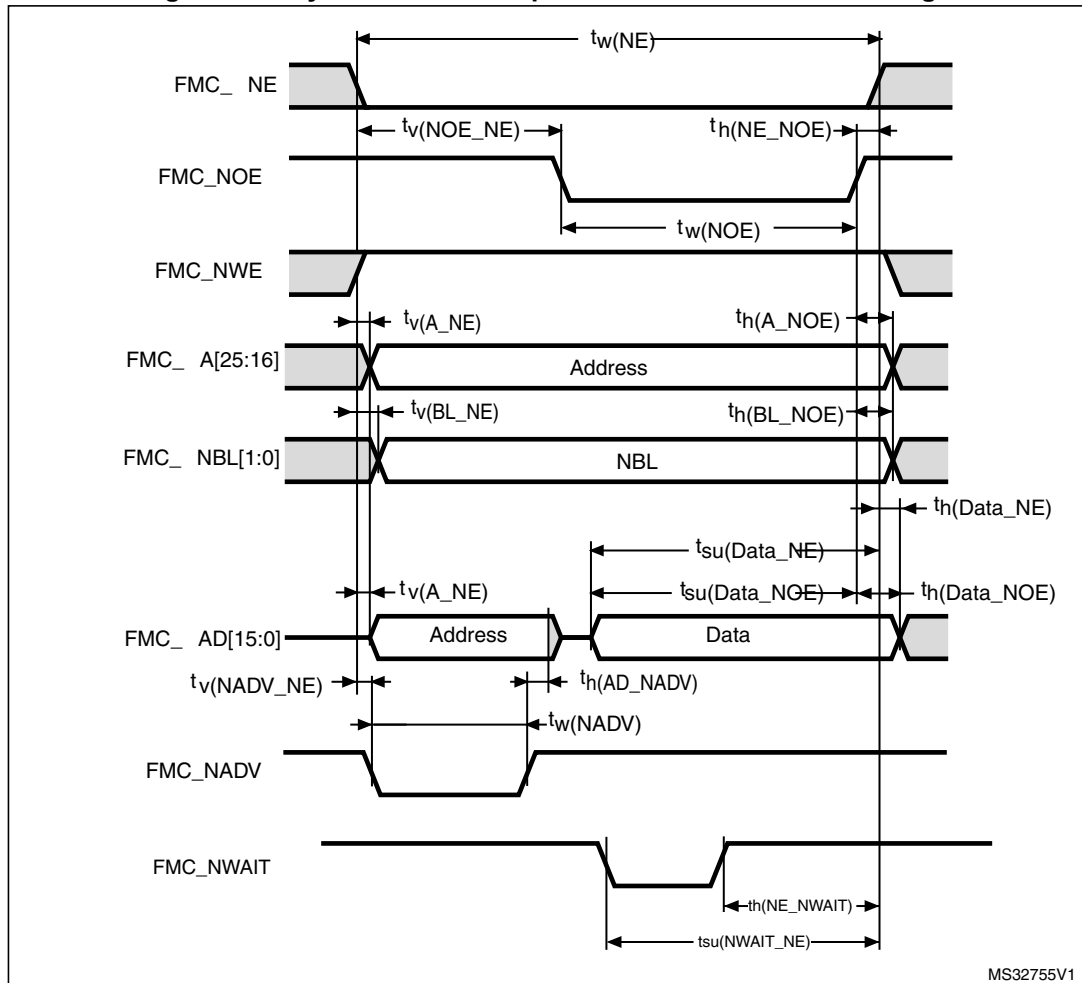
Figure 18. Asynchronous multiplexed PSRAM/NOR read timings

Table 46. Asynchronous multiplexed PSRAM/NOR read timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9THCLK-0.5	9THCLK+1	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	5THCLK	5THCLK+1	
$t_{w(NOE)}$	FMC_NOE low time	4THCLK-2	4THCLK+2	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	1.5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	2	
$t_{w(NADV)}$	FMC_NADV low time	4THCLK-2	4THCLK+2	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	0	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	THCLK-0.5	-	
$t_{h(BL\_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	THCLK	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	THCLK+1	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Based on characterization, not tested in production
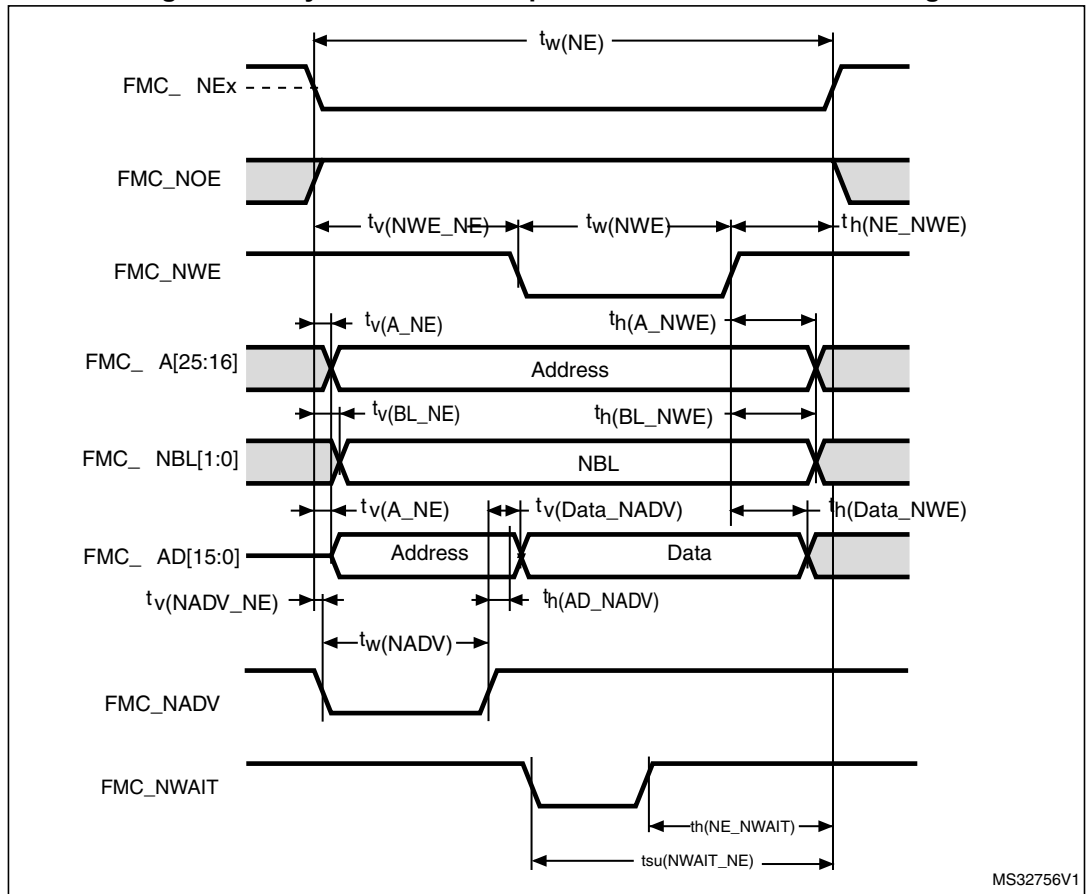
Figure 19. Asynchronous multiplexed PSRAM/NOR write timings

Table 47. Asynchronous multiplexed PSRAM/NOR write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	10THCLK-1	10THCLK+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK	THCLK+0.5	
$t_{w(NWE)}$	FMC_NWE low time	5THCLK-0.5	5THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	1	2.5	
$t_{w(NADV)}$	FMC_NADV low time	4THCLK-2	4THCLK+2	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	THCLK-2	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	THCLK +3.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK +0.5	-	

1. Based on characterization, not tested in production

Table 48. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	12THCLK	12THCLK+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	6THCLK	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK+6	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	5THCLK-5	-	

1. Based on characterization, not tested in production

Synchronous waveforms and timings

Figure 20 and *Figure 23* present the synchronous waveforms and *Table 49* to *Table 52* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 4;
- DataLatency = 2 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the THCLK is the HCLK clock period (with maximum FMC_CLK = 18 MHz).

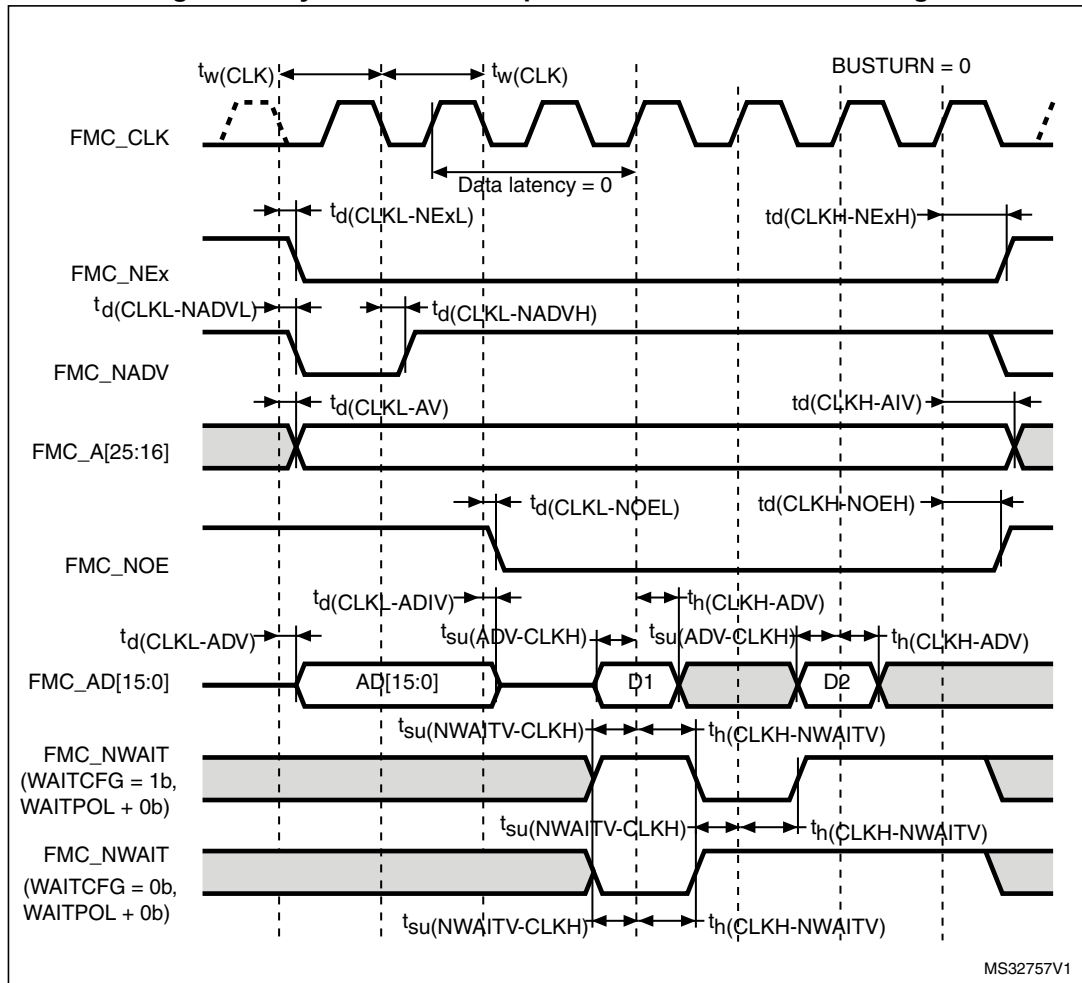**Figure 20. Synchronous multiplexed NOR/PSRAM read timings**

Table 49. Synchronous multiplexed NOR/PSRAM read timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	4THCLK	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	4	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	6	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production
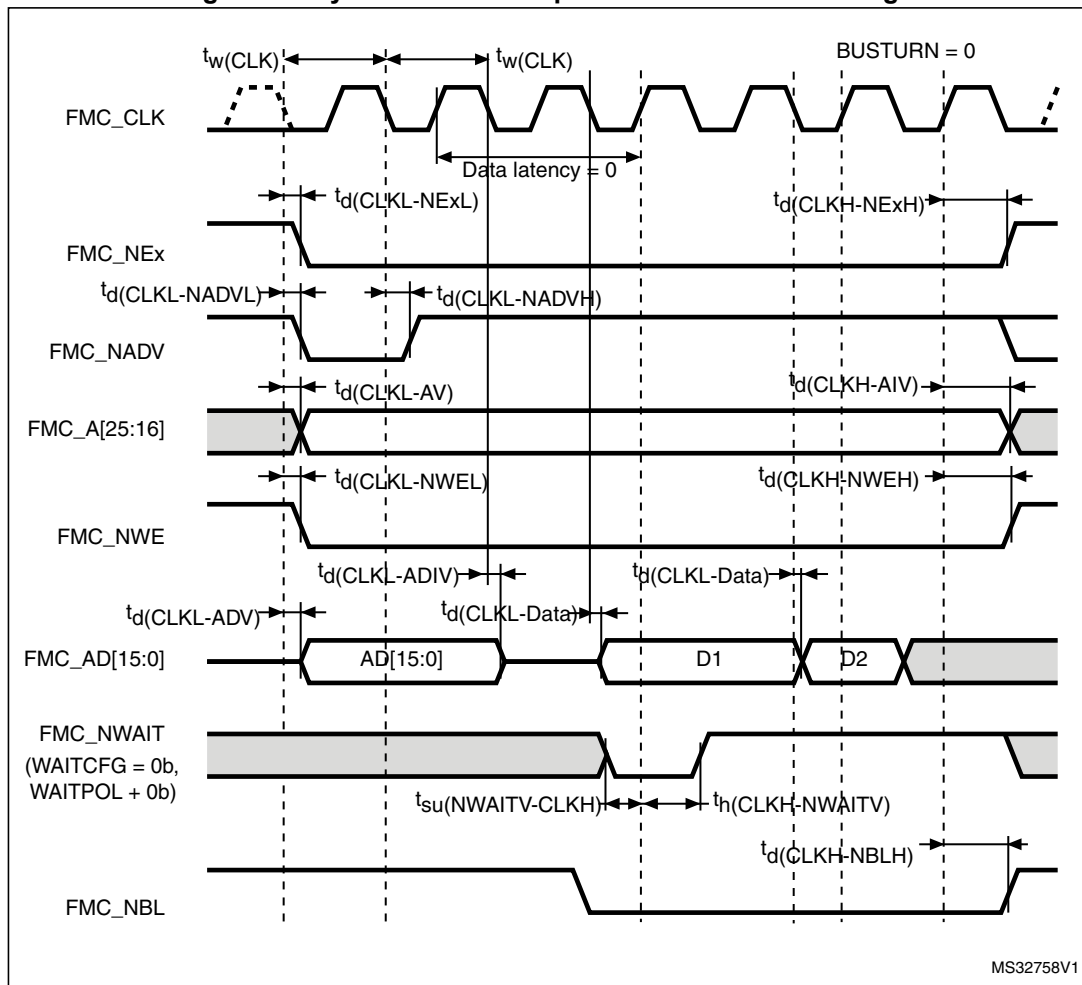
Figure 21. Synchronous multiplexed PSRAM write timings

Table 50. Synchronous multiplexed PSRAM write timings[1] [2]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, VDD range= 2.7 to 3.6 V	4THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	5.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	7.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	8	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	6	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	5	-	

1. Based on characterization, not tested in production

2. C_L = 30 pF.

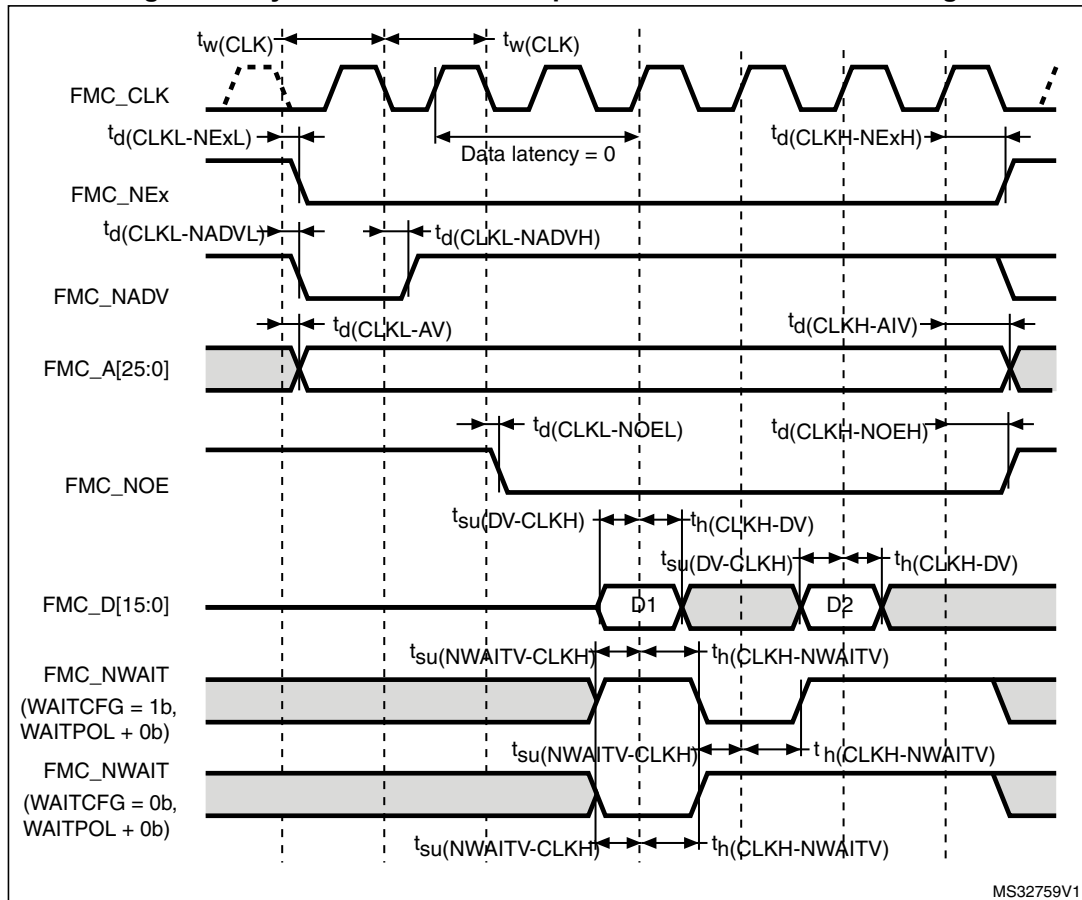**Figure 22. Synchronous non-multiplexed NOR/PSRAM read timings**

Table 51. Synchronous non-multiplexed NOR/PSRAM read timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	4THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	7	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	THCLK	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2		
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4		

1. Based on characterization, not tested in production

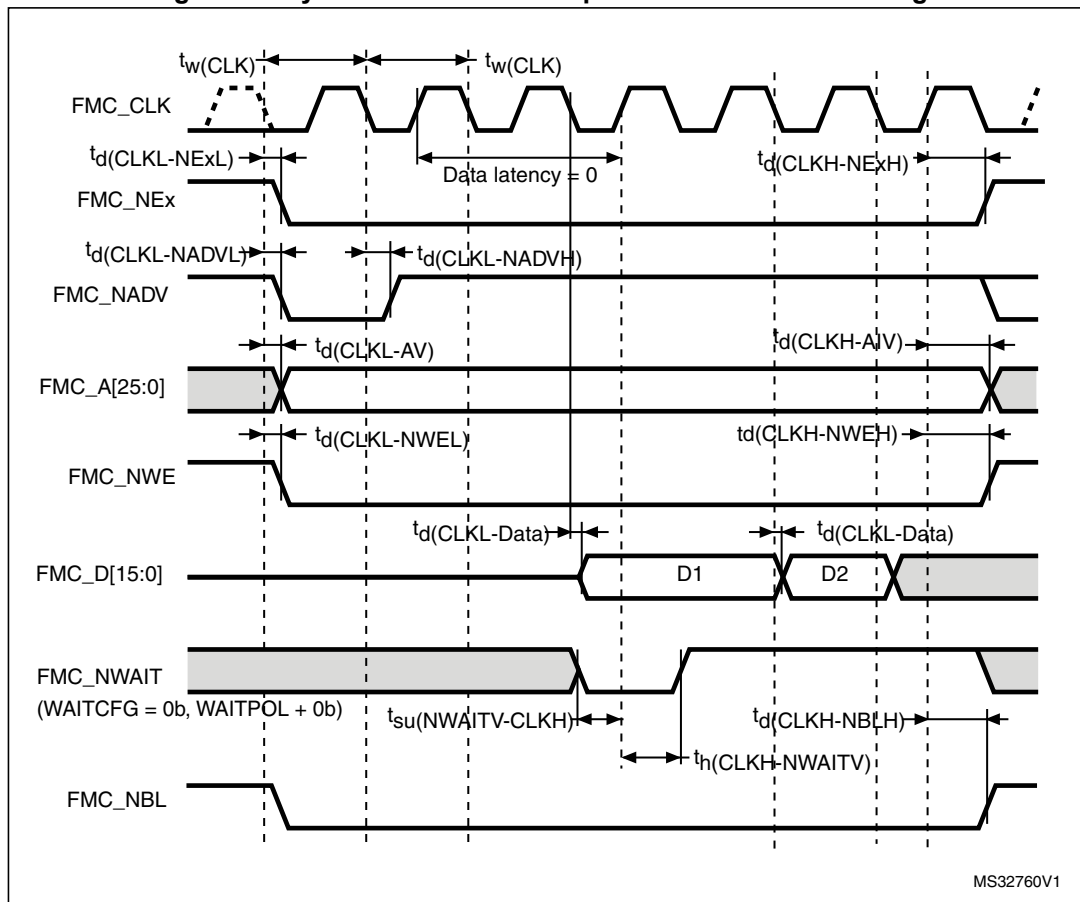**Figure 23. Synchronous non-multiplexed PSRAM write timings**

MS32760V1

Table 52. Synchronous non-multiplexed PSRAM write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	4THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	6	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	6.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	0	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+2	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	7.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	7	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production

PC Card/CompactFlash controller waveforms and timings

Figure 24 to *Figure 29* present the PC Card/Compact Flash controller waveforms, and *Table 53* to *Table 54* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x04;
- COM.FMC_WaitSetupTime = 0x07;
- COM.FMC_HoldSetupTime = 0x04;
- COM.FMC_HiZSetupTime = 0x05;
- ATT.FMC_SetupTime = 0x04;
- ATT.FMC_WaitSetupTime = 0x07;
- ATT.FMC_HoldSetupTime = 0x04;
- ATT.FMC_HiZSetupTime = 0x05;
- IO.FMC_SetupTime = 0x04;
- IO.FMC_WaitSetupTime = 0x07;
- IO.FMC_HoldSetupTime = 0x04;
- IO.FMC_HiZSetupTime = 0x05;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the THCLK is the HCLK clock period.

Table 53. Switching characteristics for PC Card/CF read and write cycles in attribute/common space[1]

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FMC_Ncex low to FMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FMC_NCEx high to FMC_Ax invalid	2.5	-	
$t_{d(NREG-NCEx)}$	FMC_NCEx low to FMC_NREG valid	-	2	
$t_{h(NCEx-NREG)}$	FMC_NCEx high to FMC_NREG invalid	0	-	
$t_{d(NCEx-NWE)}$	FMC_NCEx low to FMC_NWE low	-	5THCLK+2	
$t_{w(NWE)}$	FMC_NWE low width	8THCLK	8THCLK+0.5	
$t_{d(NWE\_NCEx)}$	FMC_NWE high to FMC_NCEx high	5THCLK-1	-	
$t_{v\ (NWE-D)}$	FMC_NWE low to FMC_D[15:0] valid	-	5	
$t_{h\ (NWE-D)}$	FMC_NWE high to FMC_D[15:0] invalid	4THCLK-1	-	
$t_{d\ (D-NWE)}$	FMC_D[15:0] valid before FMC_NWE high	13THCLK-3	-	
$t_{d(NCEx-NOE)}$	FMC_NCEx low to FMC_NOE low		5THCLK+2	
$t_{w(NOE)}$	FMC_NOE low width	8THCLK-1	8THCLK+2	
$t_{d(NOE\_NCEx)}$	FMC_NOE high to FMC_NCEx high	5THCLK-1	-	
$t_{su\ (D-NOE)}$	FMC_D[15:0] valid data before FMC_NOE high	THCLK+2	-	
$t_{h(NOE-D)}$	FMC_N0E high to FMC_D[15:0] invalid	0	-	

1. Based on characterization, not tested in production

Figure 24. PC Card/CompactFlash controller waveforms for common memory read access
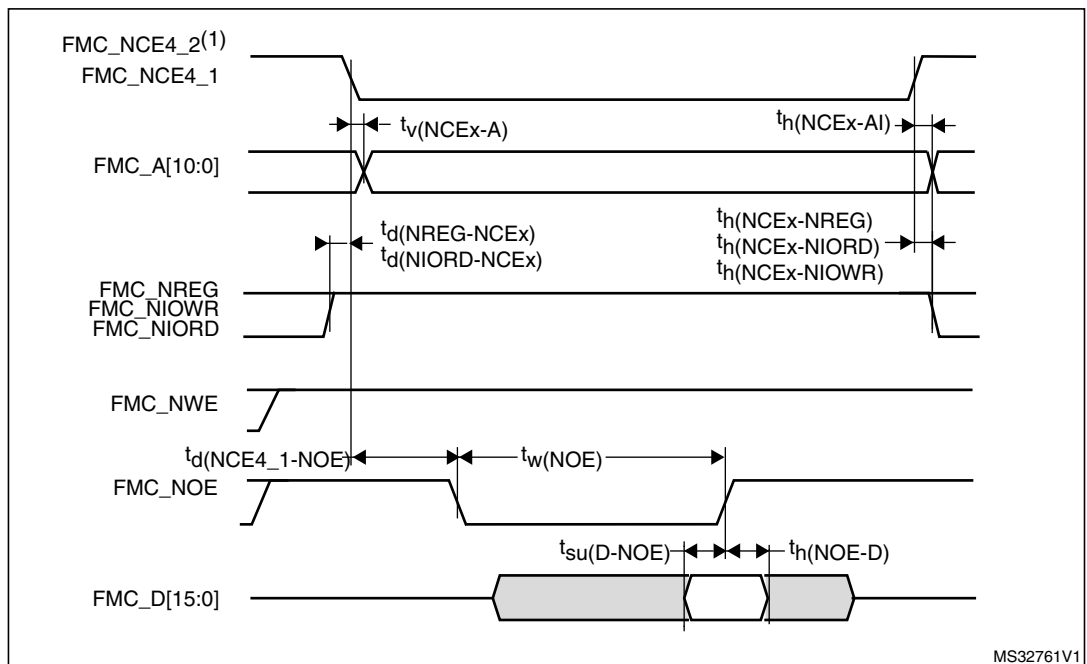
1. FMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 25. PC Card/CompactFlash controller waveforms for common memory write access
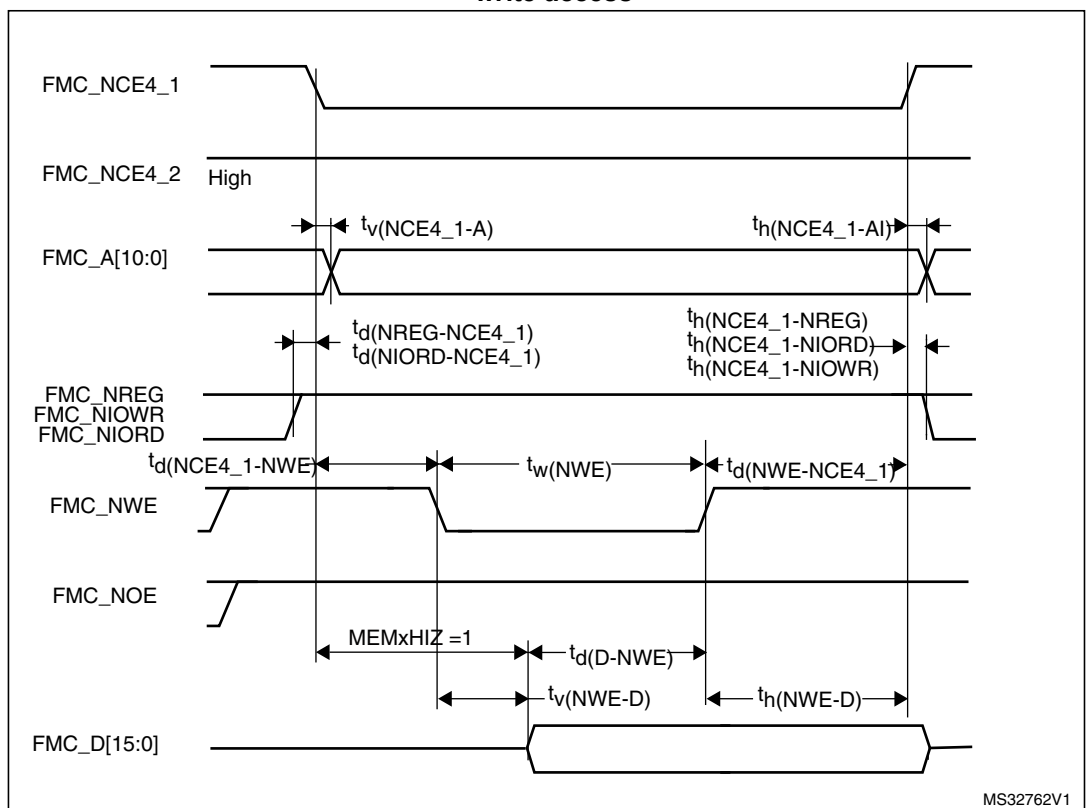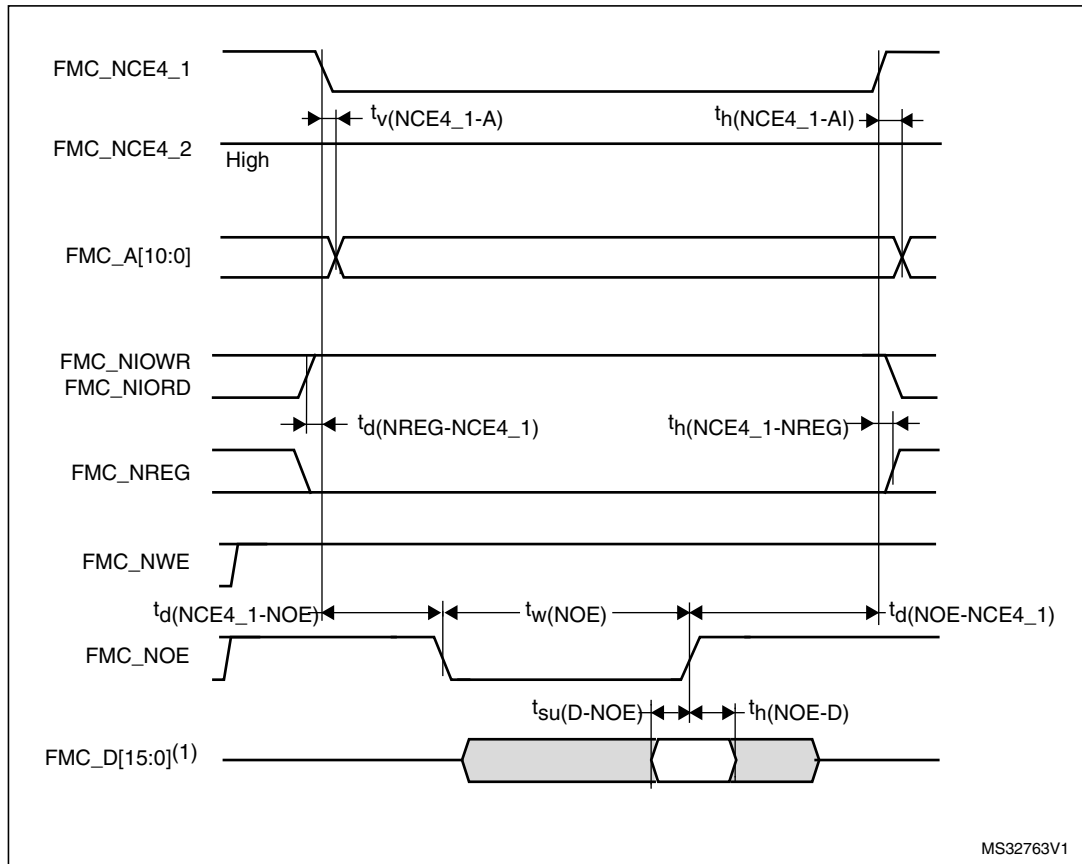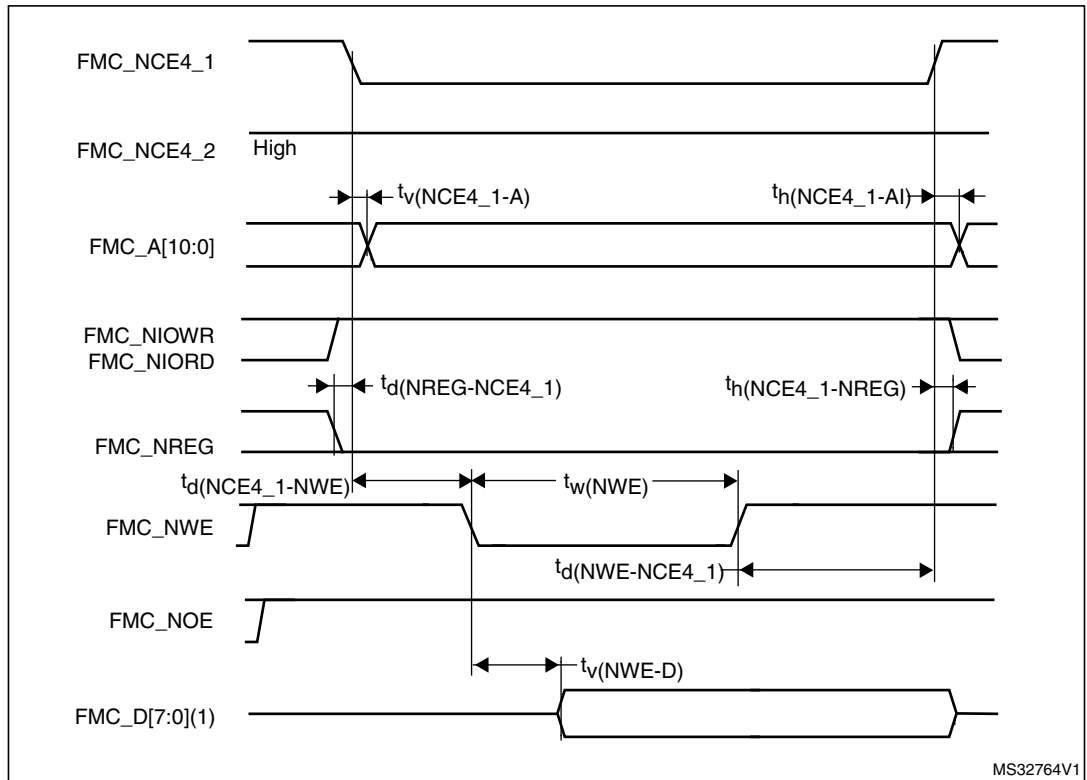
Figure 26. PC Card/CompactFlash controller waveforms for attribute memory read access

1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 27. PC Card/CompactFlash controller waveforms for attribute memory write access

1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Table 54. Switching characteristics for PC Card/CF read and write cycles in I/O space[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FMC_NIOWR low width	8THCLK-0.5		
$t_{v(NIOWR-D)}$	FMC_NIOWR low to FMC_D[15:0] valid	-	5.5	
$t_{h(NIOWR-D)}$	FMC_NIOWR high to FMC_D[15:0] invalid	4THCLK-0.5	-	
$t_{d(NCE4\_1-NIOWR)}$	FMC_NCE4_1 low to FMC_NIOWR valid	-	5THCLK+1	
$t_{h(NCEx-NIOWR)}$	FMC_NCEx high to FMC_NIOWR invalid	4THCLK+0.5	-	
$t_{d(NIORD-NCEx)}$	FMC_NCEx low to FMC_NIORD valid	-	5THCLK	ns
$t_{h(NCEx-NIORD)}$	FMC_NCEx high to FMC_NIORD) valid	6THCLK+2	-	
$t_{w(NIORD)}$	FMC_NIORD low width	8THCLK-1	8THCLK+1	
$t_{su(D-NIORD)}$	FMC_D[15:0] valid before FMC_NIORD high	THCLK+2	-	
$t_{d(NIORD-D)}$	FMC_D[15:0] valid after FMC_NIORD high	0	-	

1. Based on characterization, not tested in production

Figure 28. PC Card/CompactFlash controller waveforms for I/O space read access
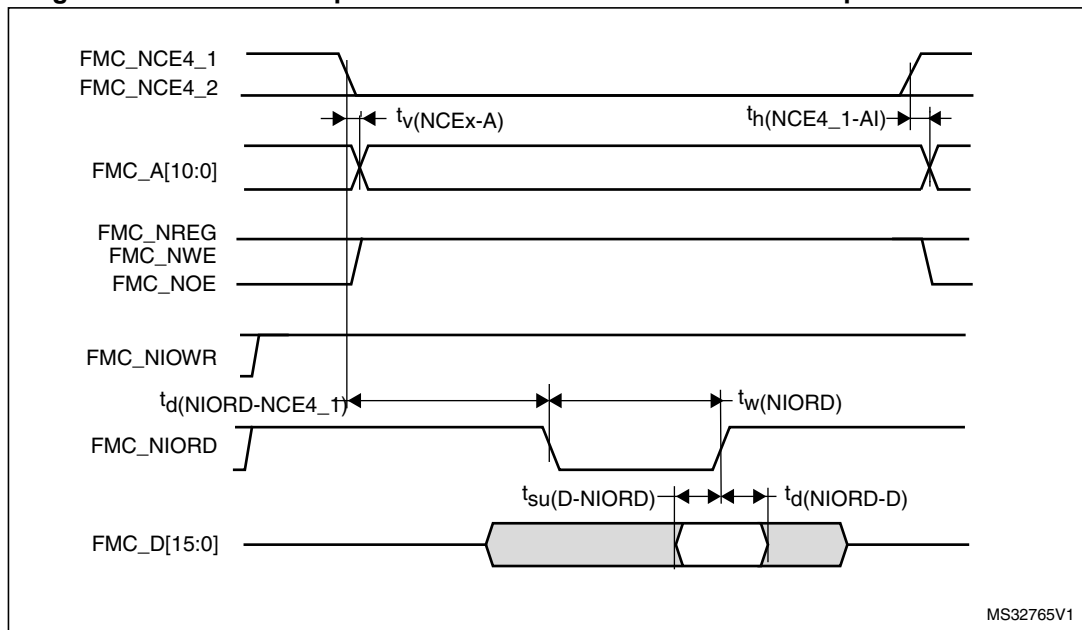
Figure 29. PC Card/CompactFlash controller waveforms for I/O space write access
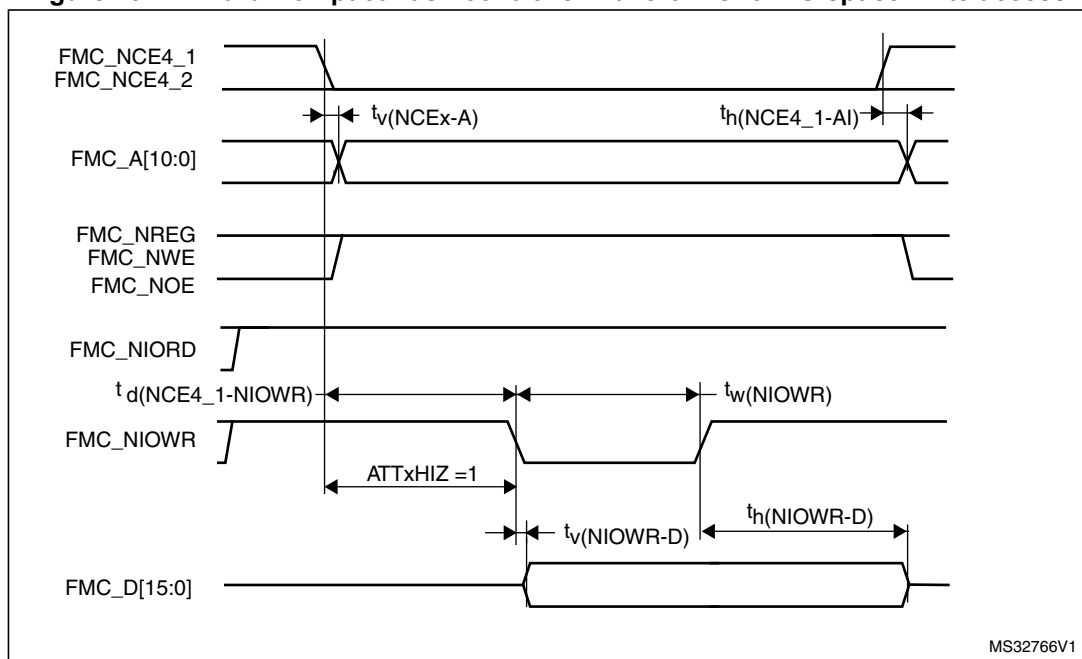
NAND controller waveforms and timings

Figure 30 and *Figure 31* present the NAND controller synchronous waveforms, and *Table 55* and *Table 56* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x03;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x03;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the THCLK is the HCLK clock period.

Figure 30. NAND controller read timings
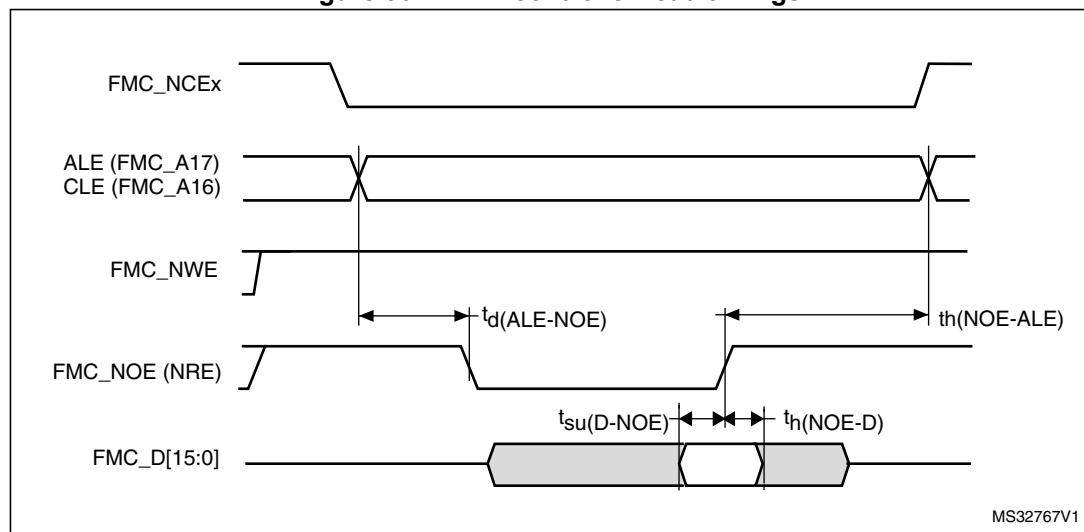
Table 55. Switching characteristics for NAND Flash read cycles[1] [2]

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	6THCLK	6THCLK + 2	
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	THCLK+5	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	ns
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	6THCLK -0.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	6THCLK-1	-	

1. Based on characterization, not tested in production

2. CL = 30 pF

Figure 31. NAND controller write timings
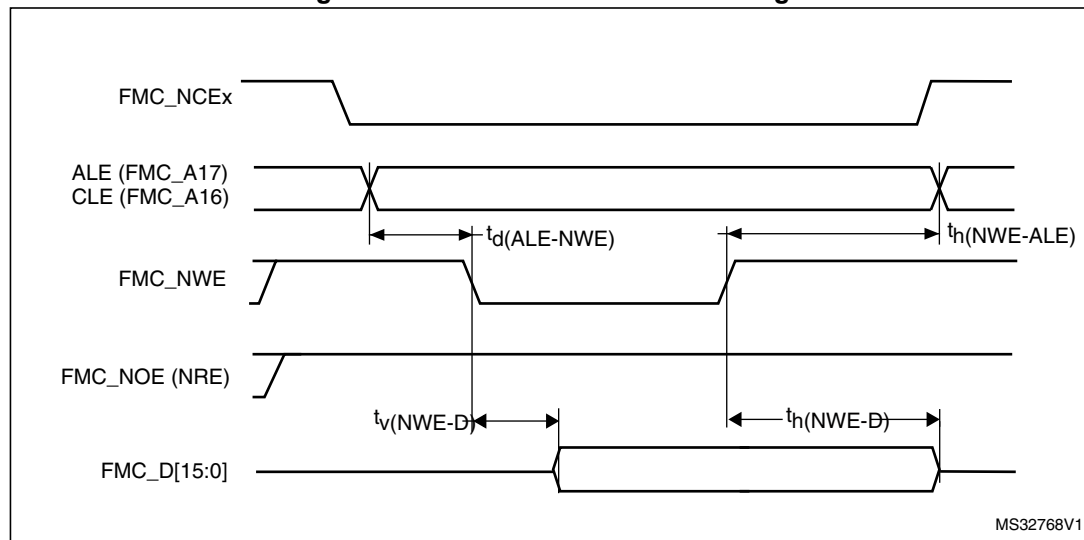
Table 56. Switching characteristics for NAND Flash write cycles[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	4THCLK-0.5	4THCLK + 1.5	
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	-	3.5	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	3THCLK -1.5	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	5THCLK – 3	-	ns
$t_{d(ALE\_NWE)}$	FMC_ALE valid before FMC_NWE low	-	4THCLK+2	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	2THCLK-1	-	

1. Based on characterization, not tested in production

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 57*. They are based on the EMS levels and classes defined in application note AN1709.

Table 57. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	TBD
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	TBD

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Pre qualification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 58. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}] 8/72 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 1.8 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	TBD	dBµV
			30 to 130 MHz	TBD	
			130 MHz to 1GHz	TBD	
			SAE EMI Level	TBD	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 59. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 60. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	TBD

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 61*.

Table 61. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PF3, PC1, PC2, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PB0, PB1, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 pins with induced leakage current on adjacent pins less than -50 µA or more than +400 µA	-5	+5	
	Injected current on PF2, PF4, PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PC4, PC5, PB2, PB11 with induced leakage current on other pins from this group less than -50 µA or more than +400 µA	-5	+5	
	Injected current on PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, P15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than -50 µA or more than +400 µA	-5	+5	
	Injected current on any other FT, FTf and NPOR pins	-5	NA	
	Injected current on any other pins	-5	+5	

Note: *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

6.3.14   I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 62* are derived from tests performed under the conditions summarized in *Table 18*. All I/Os are CMOS and TTL compliant.

Table 62. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DD}+0.07$ [1]	V
		FT and FTf I/O	-	-	$0.475\ V_{DD}-0.2$ [1]	
		BOOT0	-	-	$0.3\ V_{DD}-0.3$ [1]	
		All I/Os except BOOT0	-	-	$0.3\ V_{DD}$ [2]	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DD}+0.398$ [1]	-	-	V
		FT and FTf I/O	$0.5\ V_{DD}+0.2$ [1]	-	-	
		NPOR I/O input high-level voltage	$0.2\ V_{DDA}+0.2$	-	-	
		BOOT0	$0.2\ V_{DD}+0.95$ [1]	-	-	
		All I/Os except BOOT0	$0.7\ V_{DD}$ [2]	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200 [1]	-	mV
		FT, FTf I/O and NPOR pin	-	100 [1]	-	
		BOOT0	-	300 [1]	-	
I_{lkg}	Input leakage current [3]	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O[4] $V_{DD} \le V_{IN} \le 5\ V$	-	-	10	
		POR $V_{DDA} \le V_{IN} \le 5\ V$	-	-	10	
R_{PU}	Weak pull-up equivalent resistor[5]	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor[5]	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.

2. Tested in production.

3. Leakage could be higher than the maximum value. if negative current is injected on adjacent pins. Refer to *Table 61: I/O current injection susceptibility*.

4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.

5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 32* for standard I/Os.
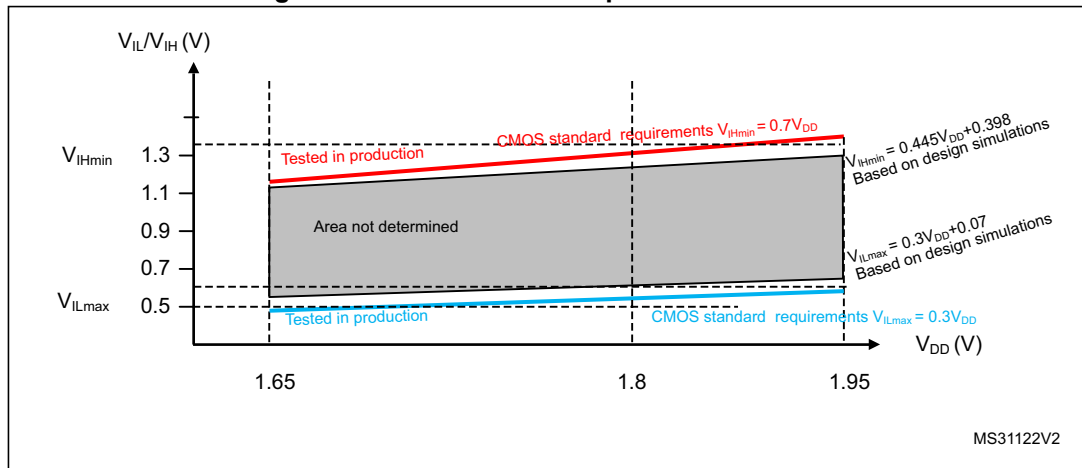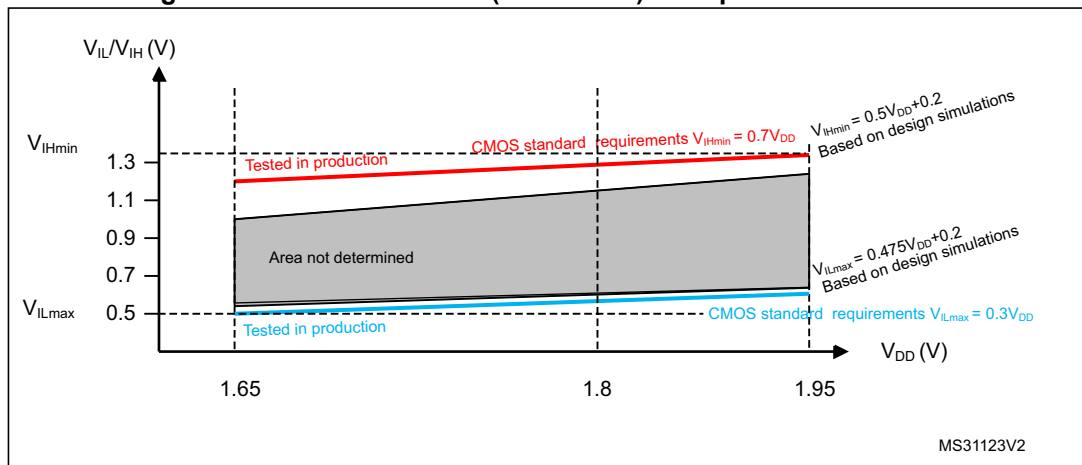
Figure 32. TC and TTA I/O input characteristics

MS31122V2

Figure 33. Five volt tolerant (FT and FTf) I/O input characteristics

MS31123V2

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 16*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 16*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 63. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}[1]	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V < V_{DD} < 1.95 V	-	0.4	
V_{OH}[2]	Output high level voltage for an I/O pin	I_{IO} = -4 mA 1.65 V < V_{DD} < 1.95 V	V_{DD}–0.4	-	V
V_{OLFM+}[1][3]	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +10 mA 1.65 V < V_{DD} < 1.95 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.

2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.

3. Data based on design simulation.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 34* and *Table 64*, respectively.
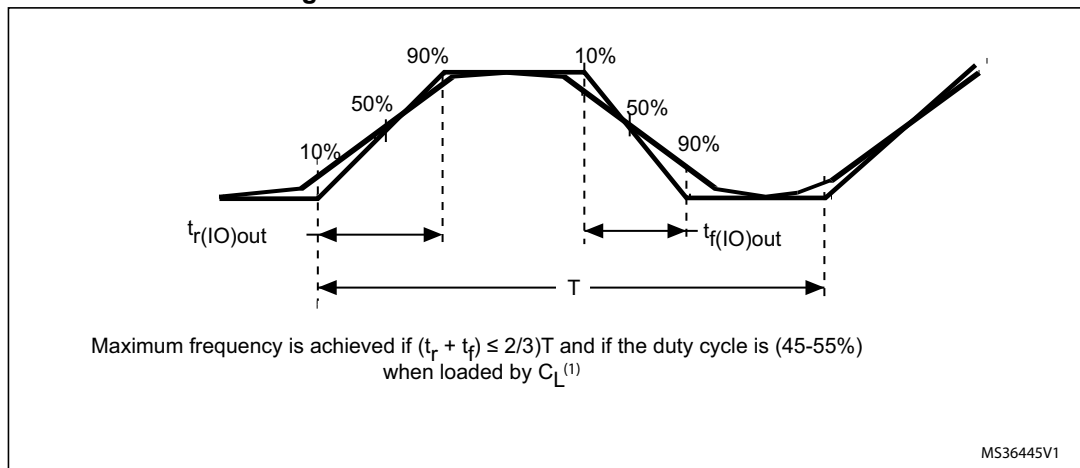
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 64. I/O AC characteristics[1]

OSPEEDRy [1:0] value[1]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	1[3]	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	125[3]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125[3]	
01	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	4[3]	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	62.5[3]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25[3]	
11	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	10[3]	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25[3]	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25[3]	
FM+ configuration[4]	$f_{max(IO)out}$	Maximum frequency[2]	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	0.5[3][4]	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	16[4]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	44[3][4]	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10[3]	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0316 reference manual for a description of GPIO Port configuration register.

2. The maximum frequency is defined in *Figure 34*.

3. Guaranteed by design, not tested in production.

4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the reference manual RM0316 for a description of FM+ I/O mode configuration.

Figure 34. I/O AC characteristics definition

1. See *Table 64: I/O AC characteristics*.

6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 62*).

Unless otherwise specified, the parameters given in *Table 65* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 65. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$[1]	NRST Input low level voltage	-	-	-	$0.3V_{DD}+$ 0.07[1]	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage	-	$0.445V_{DD}+$ 0.398[1]	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor[2]	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$[1]	NRST Input filtered pulse	-	-	-	100[1]	ns
$V_{NF(NRST)}$[1]	NRST Input not filtered pulse	-	700[1]	-	-	ns

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 35. Recommended NRST pin protection
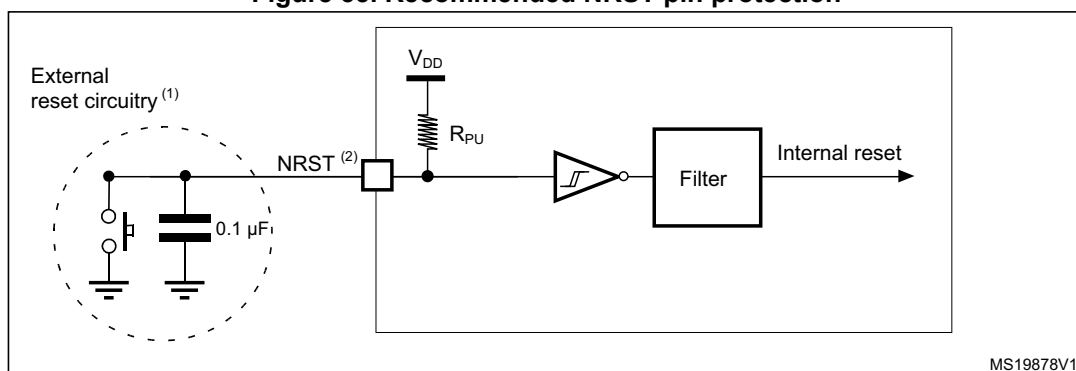
1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 65*. Otherwise the reset will not be taken into account by the device.

6.3.16 NPOR pin characteristics

The NPOR pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 66*) connected to V_{DDA} supply.

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under ambient temperature and V_{DDA} supply voltage conditions summarized in *Table 18*.

Table 66. NPOR pin characteristics

Symbol[1]	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}$	NPOR Input low level voltage	-	-	-	$0.475V_{DDA}$ - 0.2	V
$V_{IH(NPOR)}$	NPOR Input high level voltage	-	$0.5V_{DDA}$ + 0.2	-	-	
$V_{hys(NPOR)}$	NPOR Schmitt trigger voltage hysteresis	-	-	100	-	mV
R_{PU}	Weak pull-up equivalent resistor[2]	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.17 Timer characteristics

The parameters given in *Table 67* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 67. TIMx[1][2] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIMxCLK}$ = 144 MHz	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIMxCLK}$ = 144 MHz	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIMxCLK}$ = 144 MHz	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM8, TIM15, TIM16 TIM17 and TIM20 timers.

2. Guaranteed by design, not tested in production.

Table 68. IWDG min/max timeout period at 40 kHz (LSI) [1]

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 69. WWDG min-max timeout value @72 MHz (PCLK)[1]

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.18 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev.03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbits/s

The I^2C timings requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics*.

All I^2C I/Os embed an analog filter. refer to the *Table 71: I2C analog filter characteristics*.

Table 70. I2C timings specification (see I2C specification, rev.03, June 2007)[1]

Symbol	Parameter	Standard mode		Fast mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4		0.6		0.26	-	µs
t_r	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
t_f	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45[2]	-	0.9[2]	-	0.45[2]	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45[2]	-	0.9[2]	-	0.45[2]	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD:STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26		µs
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF
t_{SP}	Pulse width of spikes that are suppressed by the analog filter for Standard and Fast mode	0	50[3]	0	50[3]	-	-	ns

1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to the RM0316 reference manual). These characteristics are not tested in production.

2. The maximum $t_{HD; DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.

3. The minimum width of the spikes filtered by the analog filter is above t_{SP}(max).

Table 71. I2C analog filter characteristics[1]

Symbol	Parameter	Min	Max	Unit
t_{AF}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 36. I²C bus AC waveforms and measurement circuit
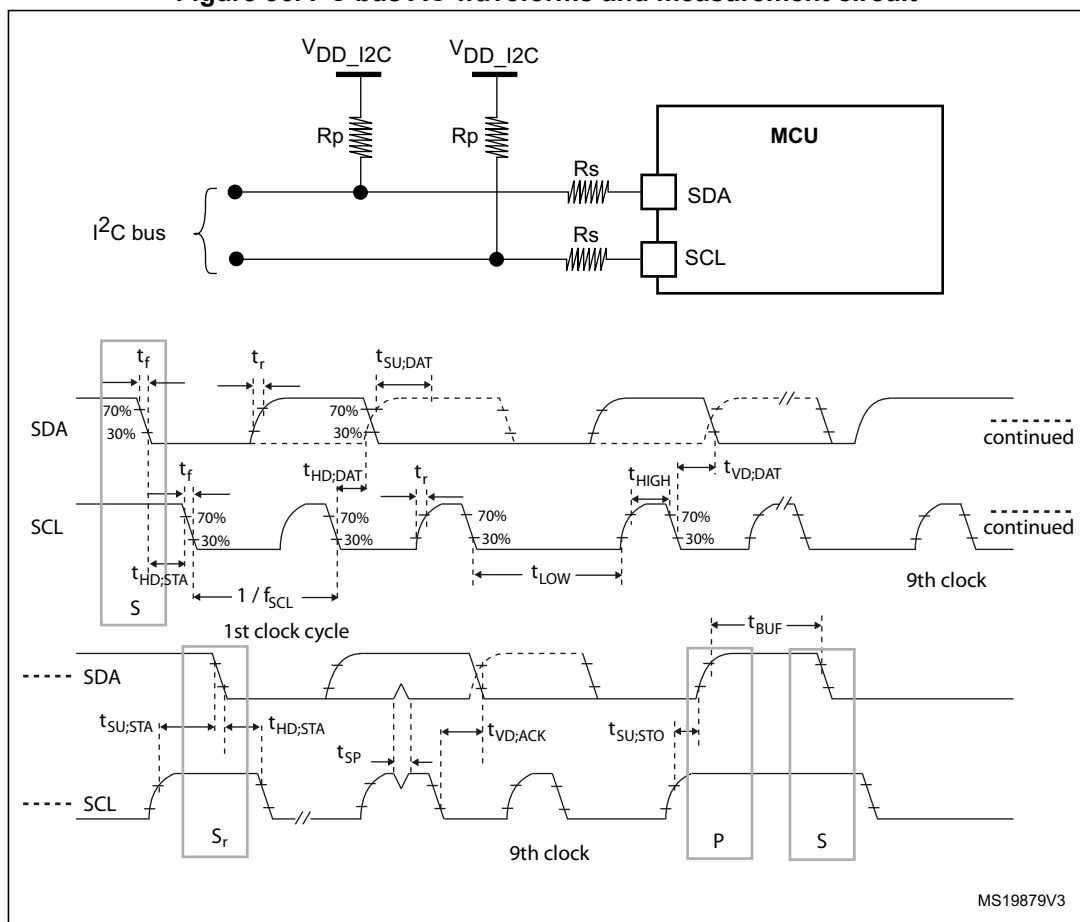
1. Rs: Series protection resistors, Rp: Pull-up resistors, VDD_I2C: I2C bus supply.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 72* for SPI or in *Table 73* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 18*.

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 72. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, SPI1/2/3/4	-	-	18	MHz
		Slave mode, SPI1/2/3/4	-	-	18	
		Slave mode transmitter/full duplex, 1.65 V<V_{DD}<1.95 V, SPI1/2/3/4	-	-	12.5[2]	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	10	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	17	
$t_{v(SO)}$	Data output valid time	Slave mode	-	22	39	
$t_{v(MO)}$		Master mode	-	1.5	5	
$t_{h(SO)}$	Data output hold time	Slave mode	11	-	-	
$t_{h(MO)}$		Master mode	0	-	-	

1. Data based on characterization results, not tested in production.

2. The maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 37. SPI timing diagram - slave mode and CPHA = 0
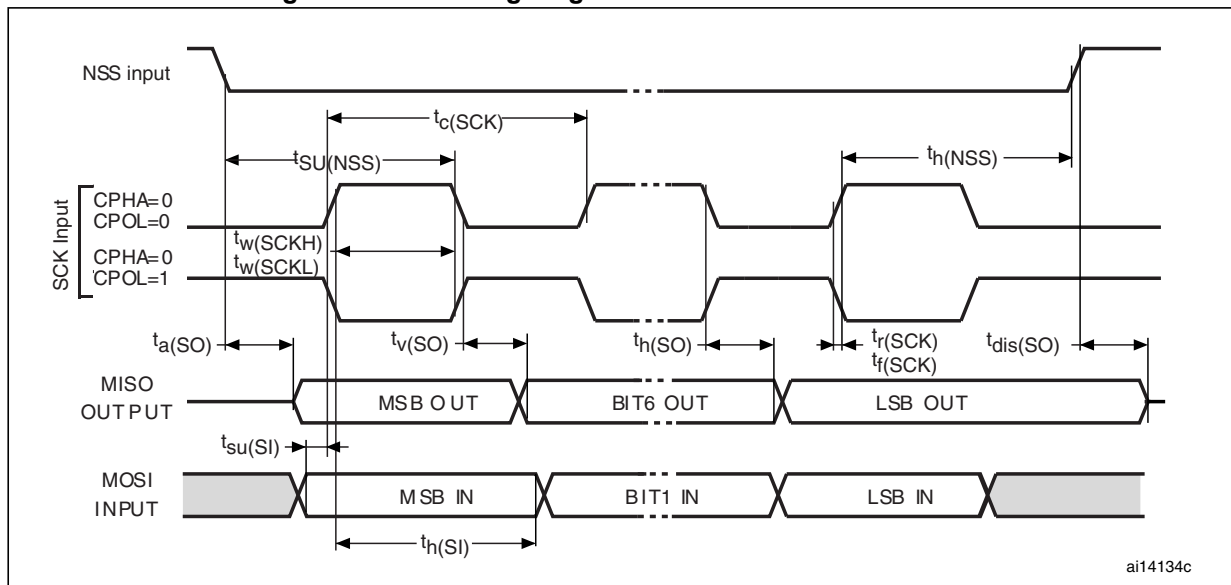
Figure 38. SPI timing diagram - slave mode and CPHA = 1[1]
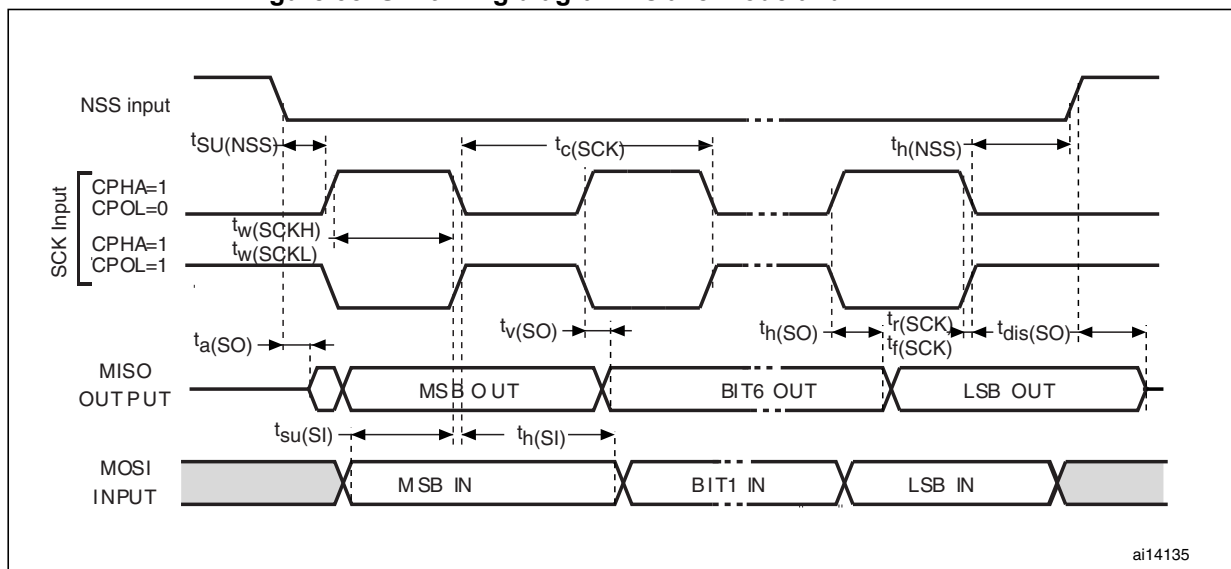
1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Figure 39. SPI timing diagram - master mode[1]
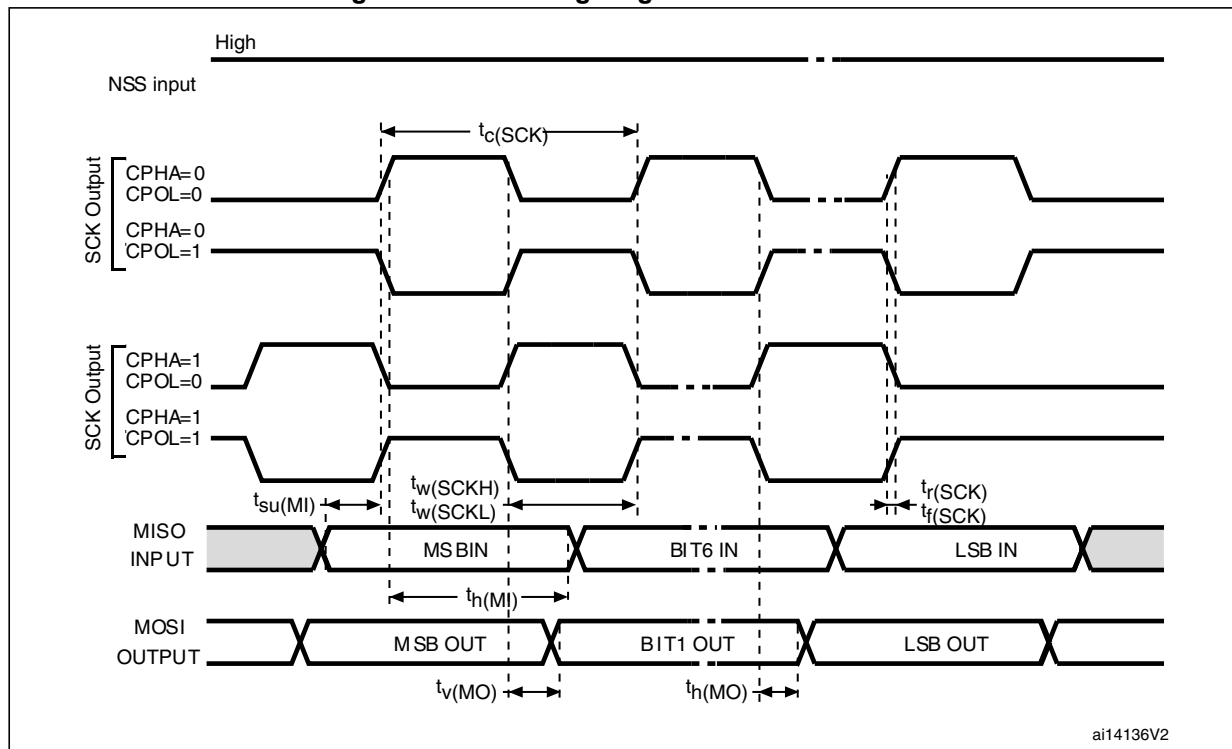
1. Measurement points are done at $0.5V_{DD}$ and with external C_L = 30 pF.

Table 73. I²S characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs [2]	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%

Table 73. I^{2}S characteristics$^{(1)}$ (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(WS)}$	WS valid time	Master mode	-	20	ns
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	0	-	
$t_{h(WS)}$	WS hold time	Slave mode	4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	8	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	50	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	22	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1	-	

1. Data based on characterization results, not tested in production.

2. 256xFs maximum is 36 MHz (APB1 Maximum frequency)

Note: *Refer to theI2S section in RM0316 Reference Manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK}, DCK values reflect only the digital peripheral behavior, source clock precision might slightly change the values DCK depends mainly on ODD bit value. Digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max (I2SDIV+ODD)/(2*I2SDIV+ODD) and Fs max supported for each mode/condition.*

Figure 40. I²S slave timing diagram (Philips protocol)[1]
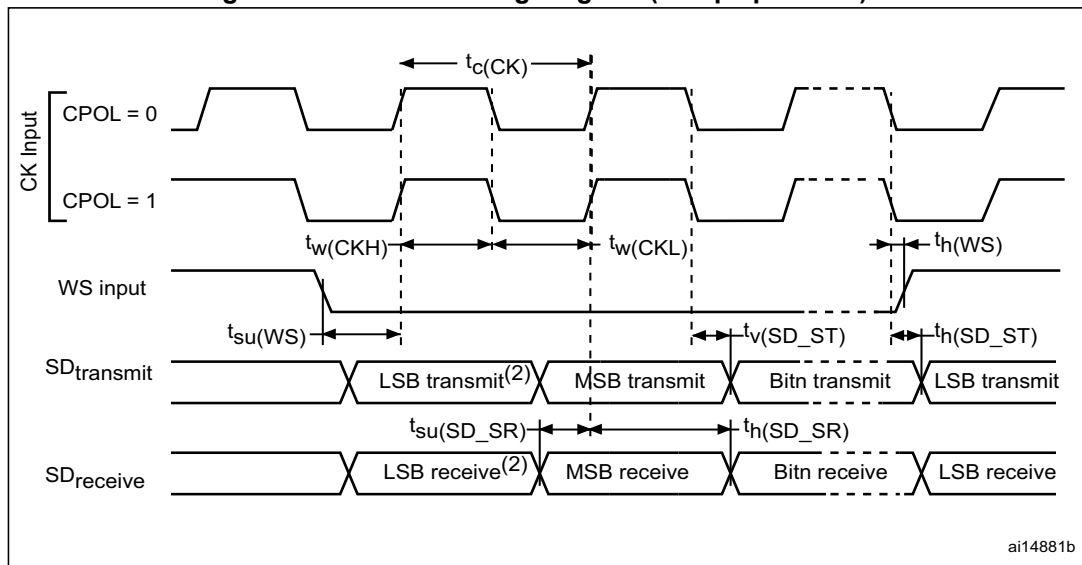
1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.

2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 41. I²S master timing diagram (Philips protocol)[1]
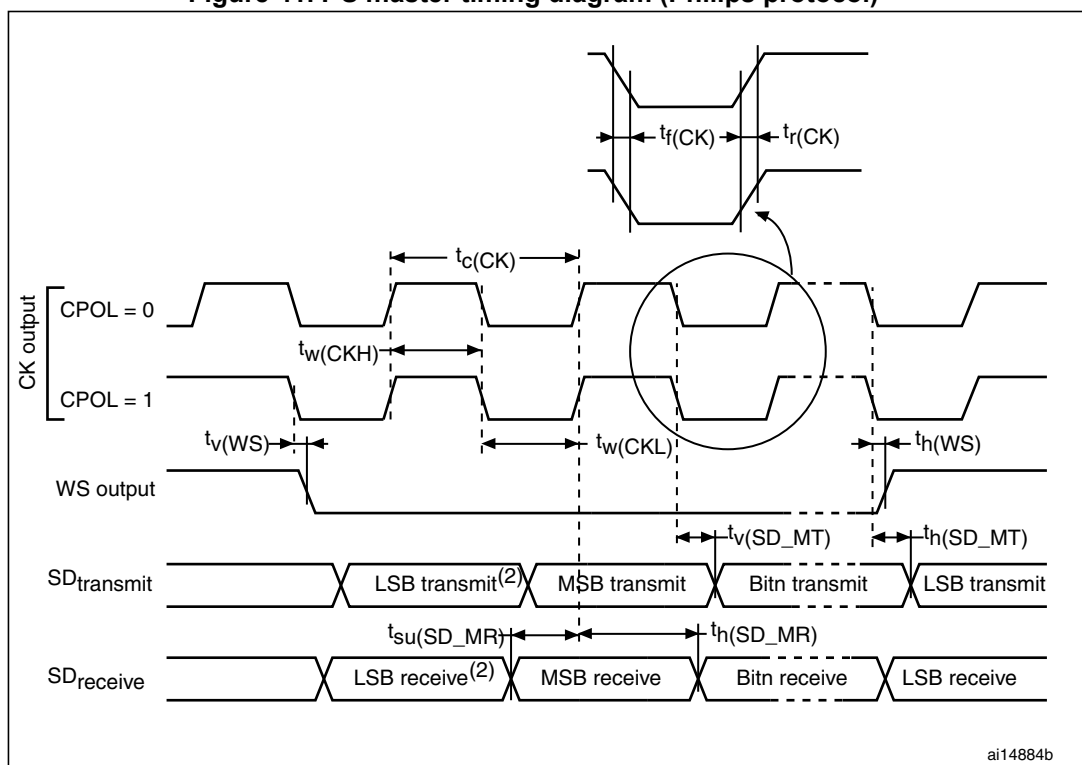
1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.

2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.19   ADC characteristics

Unless otherwise specified, the parameters given in *Table 74* to *Table 77* are guaranteed by design, with conditions summarized in *Table 18*.

Table 74. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	1.8	-	3.6	V
I_{DDA}	Current on VDDA pin (see *Figure 42*)	Single-ended mode, 5 MSPS	-	907	1033	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	
I_{REF}	Current on VREF+ pin (see *Figure 43*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz

Table 74. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S[1]	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}[1]	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range[2]	-	0	-	V_{REF+}	V
R_{AIN}[1]	External input impedance	-	-	-	100	kΩ
C_{ADC}[1]	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}[1]	Power-up time	-	0	0	1	µs
t_{CAL}[1]	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr}[1]	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$[1]	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$
t_S[1]	Sampling time	f_{ADC} = 72 MHz	0.021	-	8.35	µs
		-	1.5	-	601.5	$1/f_{ADC}$
$T_{ADCVREG\_STUP}$[1]	ADC Voltage Regulator Start-up time	-	-	-	10	µs
t_{CONV}[1]	Total conversion time (including sampling time)	f_{ADC} = 72 MHz Resolution = 12 bits	0.19	-	8.52	µs
		Resolution = 12 bits	14 to 614 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

1. Data guaranteed by design, not tested in Production.

2. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.
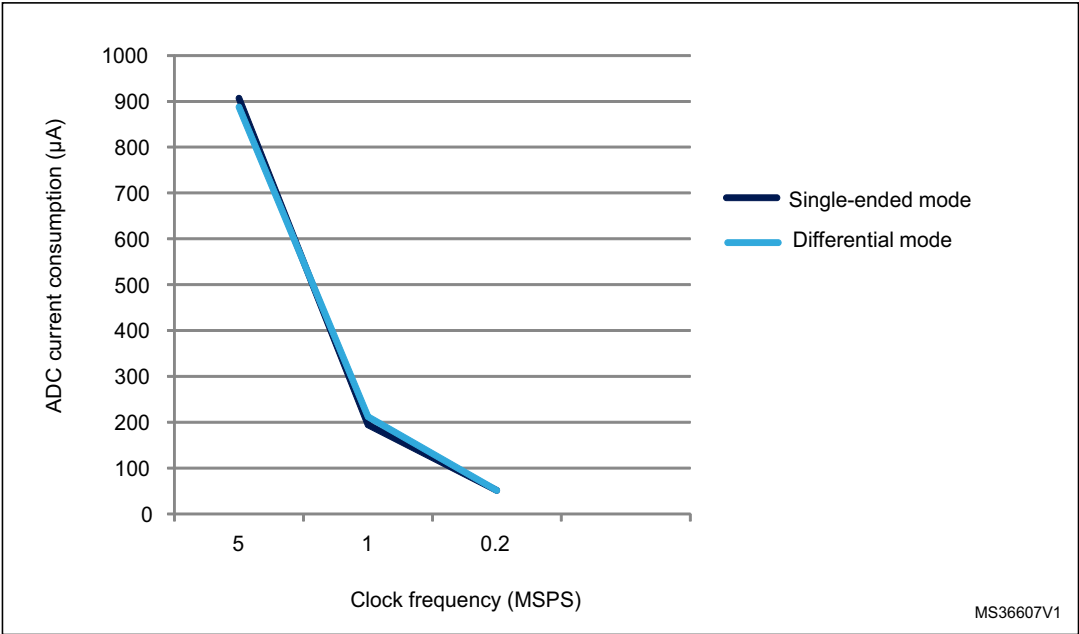
Figure 42. ADC typical current consumption on VDDA pin

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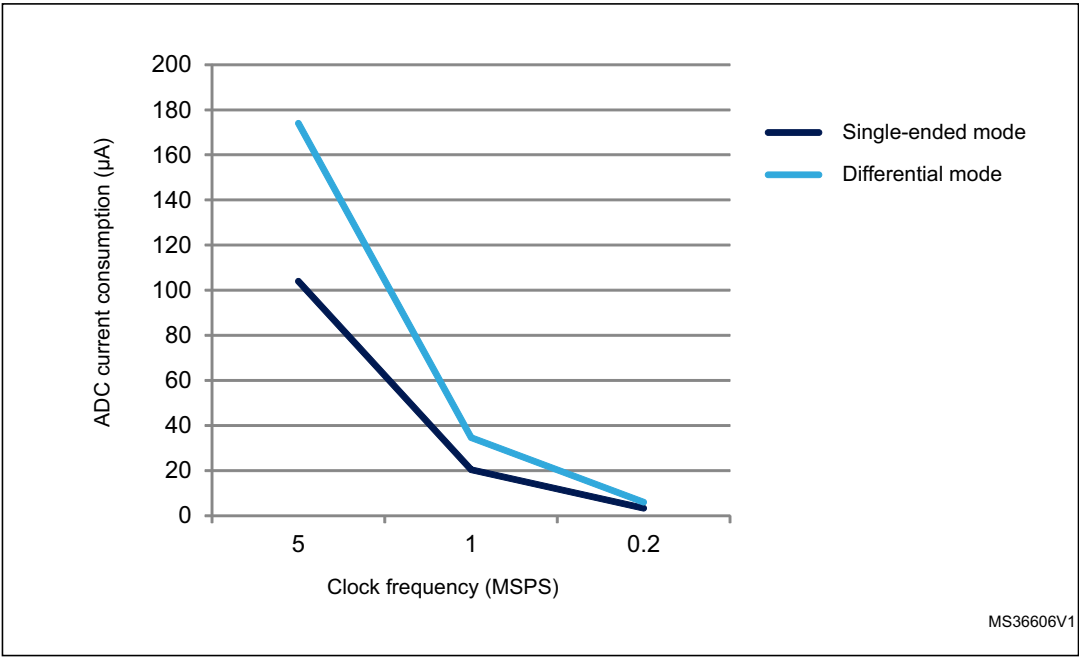**Figure 43. ADC typical current consumption on VREF+ pin**

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Table 75. Maximum ADC R$_{AIN}$ [1]

Resolution	Sampling cycle @ 72 MHz	Sampling time [ns] @ 72 MHz	R$_{AIN}$ max (kΩ)		
			Fast channels[2]	Slow channels	Other channels[3]
12 bits	1.5	20.83	0.018	NA	NA
	2.5	34.72	0.150	NA	0.022
	4.5	62.50	0.470	0.220	0.180
	7.5	104.17	0.820	0.560	0.470
	19.5	270.83	2.70	1.80	1.50
	61.5	854.17	8.20	6.80	4.70
	181.5	2520.83	22.0	18.0	15.0
	601.5	8354.17	82.0	68.0	47.0
10 bits	1.5	20.83	0.082	NA	NA
	2.5	34.72	0.270	0.082	0.100
	4.5	62.50	0.560	0.390	0.330
	7.5	104.17	1.20	0.82	0.68
	19.5	270.83	3.30	2.70	2.20
	61.5	854.17	10.0	8.2	6.8
	181.5	2520.83	33.0	27.0	22.0
	601.5	8354.17	100.0	82.0	68.0
8 bits	1.5	20.83	0.150	NA	0.039
	2.5	34.72	0.390	0.180	0.180
	4.5	62.50	0.820	0.560	0.470
	7.5	104.17	1.50	1.20	1.00
	19.5	270.83	3.90	3.30	2.70
	61.5	854.17	12.00	12.00	8.20
	181.5	2520.83	39.00	33.00	27.00
	601.5	8354.17	100.00	100.00	82.00
6 bits	1.5	20.83	0.270	0.100	0.150
	2.5	34.72	0.560	0.390	0.330
	4.5	62.50	1.200	0.820	0.820
	7.5	104.17	2.20	1.80	1.50
	19.5	270.83	5.60	4.70	3.90
	61.5	854.17	18.0	15.0	12.0
	181.5	2520.83	56.0	47.0	39.0
	601.5	8354.17	100.00	100.0	100.0

1. Data based on characterization results, not tested in production.

2. All fast channels, expect channels on PA2, PA6, PB1, PB12.

3.   Fast channels available on PA2, PA6, PB1, PB12.

Table 76. ADC accuracy - limited test conditions, 100-pin packages [1][2]

Symbol	Parameter	Conditions			Min [3]	Typ	Max [3]	Unit
ET	Total unadjusted error	ADC clock freq. $\leq$ 72 MHz Sampling freq. $\leq$ 5 Msps $V_{DDA} = V_{REF+} = 3.3$ V 25°C 100-pin package	Single ended	Fast channel 5.1 Ms	-	±3.5	±4.5	LSB
				Slow channel 4.8 Ms	-	±4	±4.5	
			Differential	Fast channel 5.1 Ms	-	±3	±3	
				Slow channel 4.8 Ms	-	±3	±3	
EO	Offset error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±2.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
EG	Gain error		Single ended	Fast channel 5.1 Ms	-	±3	±4	
				Slow channel 4.8 Ms	-	±3.5	±4	
			Differential	Fast channel 5.1 Ms	-	±1.5	±2.5	
				Slow channel 4.8 Ms	-	±2	±2.5	
ED	Differential linearity error		Single ended	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1	±1	
				Slow channel 4.8 Ms	-	±1	±1	
EL	Integral linearity error		Single ended	Fast channel 5.1 Ms	-	±1.5	±2	
				Slow channel 4.8 Ms	-	±1.5	±3	
			Differential	Fast channel 5.1 Ms	-	±1	±1.5	
				Slow channel 4.8 Ms	-	±1	±1.5	
ENOB [4]	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.7	10.8	-	bits
				Slow channel 4.8 Ms	10.7	10.8	-	
			Differential	Fast channel 5.1 Ms	11.2	11.3	-	
				Slow channel 4.8 Ms	11.1	11.3	-	
SINAD [4]	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	

Table 76. ADC accuracy - limited test conditions, 100-pin packages [1][2] (continued)

Symbol	Parameter	Conditions			Min [3]	Typ	Max [3]	Unit
SNR[4]	Signal-to-noise ratio	ADC clock freq. $\leq$ 72 MHz Sampling freq $\leq$ 5 Msps $V_{DDA} = V_{REF+}$ = 3.3 V 25°C 100-pin package	Single ended	Fast channel 5.1 Ms	66	67	-	dB
				Slow channel 4.8 Ms	66	67	-	
			Differential	Fast channel 5.1 Ms	69	70	-	
				Slow channel 4.8 Ms	69	70	-	
THD[4]	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-76	-76	
				Slow channel 4.8 Ms	-	-76	-76	
			Differential	Fast channel 5.1 Ms	-	-80	-80	
				Slow channel 4.8 Ms	-	-80	-80	

1. ADC DC accuracy values are measured after internal calibration.

2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.

3. Data based on characterization results, not tested in production.

4. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 77. ADC accuracy, 100-pin packages- limited test conditions [1][2][3]

Symbol	Parameter	Conditions			Min [4]	Max[4]	Unit
ET	Total unadjusted error	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps 1.8 V ≤ V$_{DDA}$, V$_{REF+}$ ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	-	±6.5	LSB
				Slow channel 4.8 Ms	-	±6.5	
			Differential	Fast channel 5.1 Ms	-	±4	
				Slow channel 4.8 Ms	-	±4	
EO	Offset error		Single Ended	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
EG	Gain error		Single Ended	Fast channel 5.1 Ms	-	±6	
				Slow channel 4.8 Ms	-	±6	
			Differential	Fast channel 5.1 Ms	-	±3	
				Slow channel 4.8 Ms	-	±3	
ED	Differential linearity error		Single Ended	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
			Differential	Fast channel 5.1 Ms	-	±1.5	
				Slow channel 4.8 Ms	-	±1.5	
EL	Integral linearity error		Single Ended	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±3	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2	
ENOB [5]	Effective number of bits		Single Ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.2	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	

Table 77. ADC accuracy, 100-pin packages- limited test conditions [1][2][3] (continued)

Symbol	Parameter	Conditions			Min [4]	Max[4]	Unit
SINAD [5]	Signal-to-noise and distortion ratio	ADC clock freq. ≤ 72 MHz, Sampling freq. ≤ 5 Msps, 1.8 V≤ V$_{DDA}$, V$_{REF+}$ ≤ 3.6 V 100-pin package	Single Ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR[5]	Signal-to-noise ratio		Single Ended	Fast channel 5.1 Ms	64	-	
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD[5]	Total harmonic distortion		Single Ended	Fast channel 5.1 Ms	-	74	
				Slow channel 4.8 Ms	-	-74	
			Differential	Fast channel 5.1 Ms	-	-78	
				Slow channel 4.8 Ms	-	-76	

1. ADC DC accuracy values are measured after internal calibration.

2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for I$_{INJ(PIN)}$ and ΣI$_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.

3. Better performance may be achieved in restricted V$_{DDA}$, frequency and temperature ranges.

4. Data based on characterization results, not tested in production.

5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 78. ADC accuracy at 1MSPS[1][2]

Symbol	Parameter	Test conditions		Typ	Max[3]	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V$_{DDA}$ = V$_{REF+}$ ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.

2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.14: I/O port characteristics* does not affect the ADC accuracy.

3. Data based on characterization results, not tested in production.

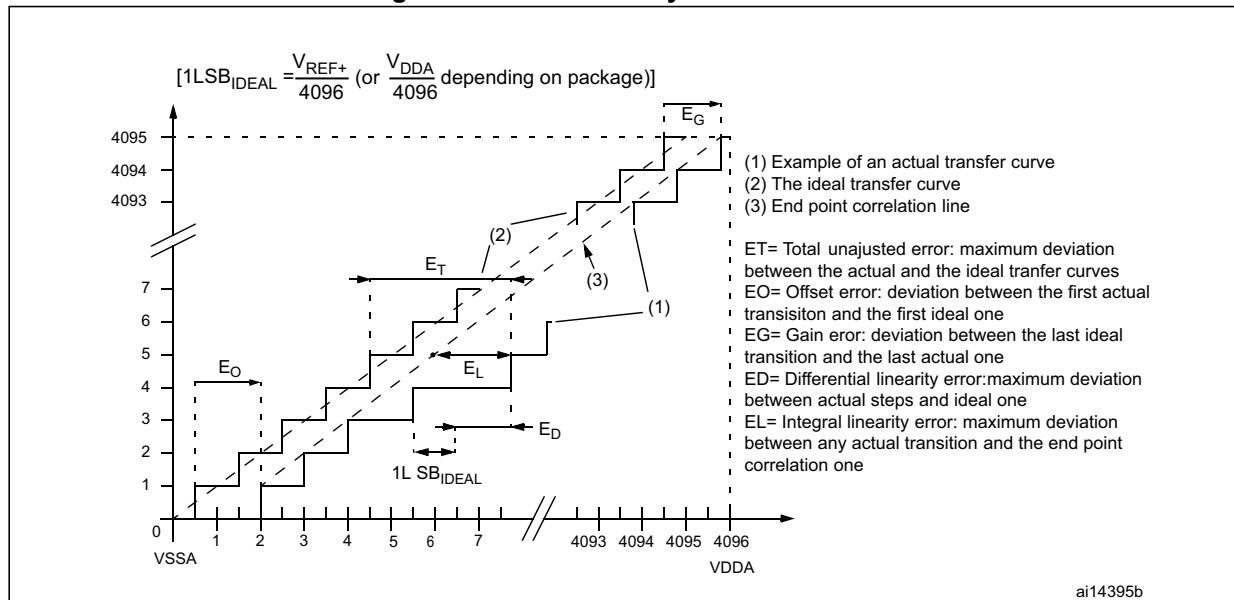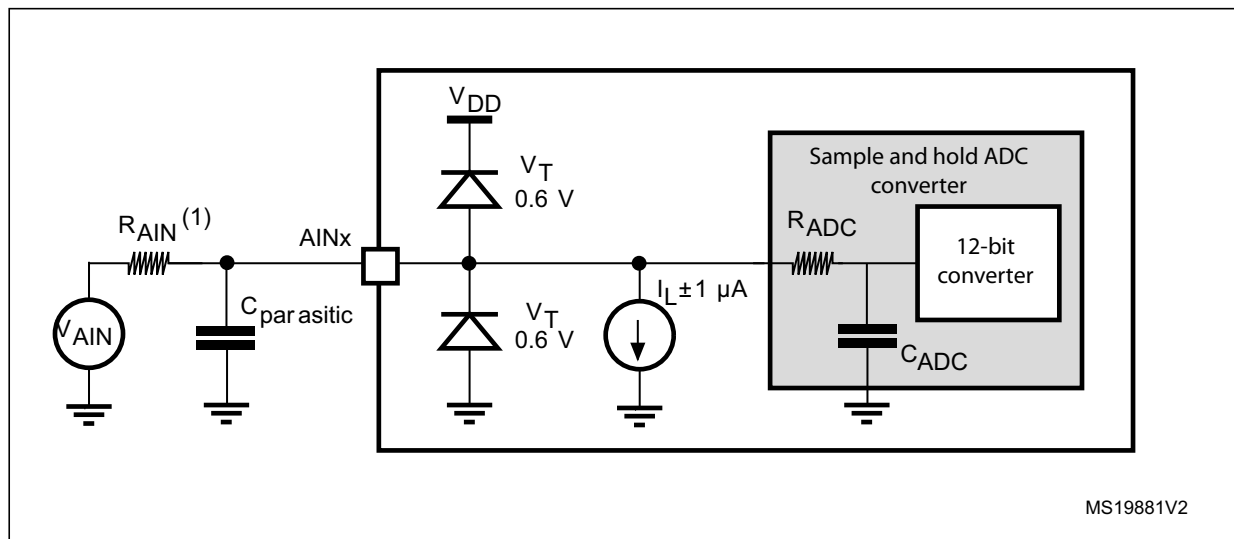### Figure 44. ADC accuracy characteristics

Figure 45. Typical connection diagram using the ADC

1. Refer to *Table 74* for the values of R_{AIN}.

2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 8*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.20 DAC electrical specifications
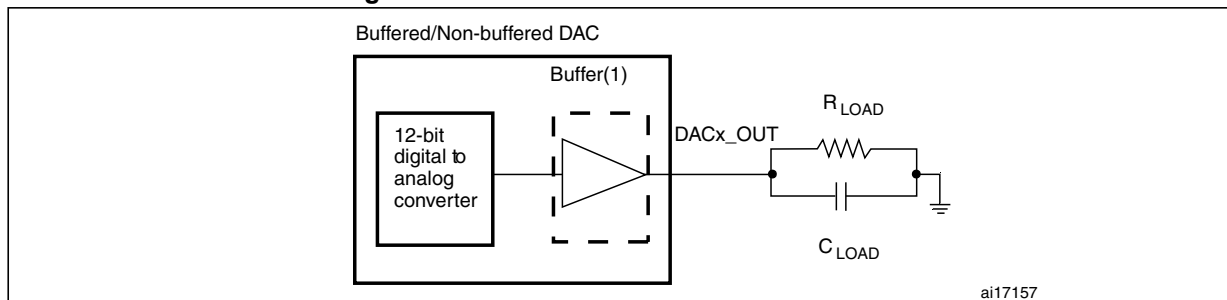
Table 79. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	DAC output buffer ON	2.4	-	3.6	V
R_{LOAD} [1]	Resistive load	DAC output buffer ON	5	-	-	kΩ
R_O [1]	Output impedance	DAC output buffer ON	-	-	15	kΩ
C_{LOAD} [1]	Capacitive load	DAC output buffer ON	-	-	50	pF
V_{DAC_OUT} [1]	Voltage on DAC_OUT output	Corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V DAC output buffer ON.	0.2	-	$V_{DDA} - 0.2$	V
		DAC output buffer OFF	-	0.5	V_{DDA} - 1LSB	mV
I_{REF}	DAC DC current consumption in quiescent mode	With no load, worst code (0xF1C) on the input	-	-	220	µA
I_{DDA} [3]	DAC DC current consumption in quiescent mode[2]	With no load, middle code (0x800) on the input.	-	-	380	µA
		With no load, worst code (0xF1C) on the input.	-	-	480	µA
DNL [3]	Differential non linearity Difference between two consecutive code-1LSB)	Given for a 10-bit input code	-	-	±0.5	LSB
		Given for a 12-bit input code	-	-	±2	LSB
INL [3]	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095)	Given for a 10-bit input code	-	-	±1	LSB
		Given for a 12-bit input code	-	-	±4	LSB
$Offset$ [3]	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)	-	-	-	±10	mV
		Given for a 10-bit input code at V_{DDA} = 3.6 V	-	-	±3	LSB
		Given for a 12-bit input code at V_{DDA} = 3.6 V	-	-	±12	LSB
Gain error [3]	Gain error	Given for a 12-bit input code	-	-	±0.5	%
$t_{SETTLING}$ [3]	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \le 50$ pF, $R_{LOAD} \ge 5$ kΩ	-	3	4	µs

Table 79. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Update rate[3]	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	1	MS/s
t_{WAKEUP}[3]	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	6.5	10	µs
PSRR+ [1]	Power supply rejection ratio (to V_{DDA}) (static DC measurement	$C_{LOAD} = 50$ pF, No $R_{LOAD} \geq 5$ kΩ,	-	−67	−40	dB

1. Guaranteed by design, not tested in production.

2. Quiescent mode refers to the state of the DAC a keeping steady value on the output, so no dynamic consumption is involved.

3. Data based on characterization results, not tested in production.

Figure 46. 12-bit buffered /non-buffered DAC

1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.21 Comparator characteristics

Table 80. Comparator characteristics[1]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
V_{BG}	Scaler input voltage	-	-	$V_{REFINIT}$	-	
V_{SC}	Scaler offset voltage	-	-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down	-	-	-	0.2	ms
t_{START}	Comparator startup time	$V_{DDA} \geq 2.7$ V	-	-	4	µs
		$V_{DDA} < 2.7$ V	-	-	10	

Table 80. Comparator characteristics[1] (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_D	Propagation delay for 200 mV step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	25	28	ns
		$V_{DDA} < 2.7$ V	-	28	30	
	Propagation delay for full range step with 100 mV overdrive	$V_{DDA} \geq 2.7$ V	-	32	35	
		$V_{DDA} < 2.7$ V	-	35	40	
V_{OFFSET}	Comparator offset error	$V_{DDA} \geq 2.7$ V	-	±5	±10	mV
		$V_{DDA} < 2.7$ V	-	-	±25	
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
I_{DDA}	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.

6.3.22 Operational amplifier characteristics

Table 81. Operational amplifier characteristics[1]

Symbol	Parameter		Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage		-	2.4	-	3.6	V
CMIR	Common mode input range		-	0	-	V_{DDA}	V
VI_{OFFSET}	Input offset voltage	Maximum calibration range	25°C, No Load on output.	-	-	4	mV
			All voltage/Temp.	-	-	6	
		After offset calibration	25°C, No Load on output.	-	-	1.6	
			All voltage/Temp.	-	-	3	
ΔVI_{OFFSET}	Input offset voltage drift		-	-	5	-	µV/°C
I_{LOAD}	Drive current		-	-	-	500	µA
I_{DDA}	OPAMP consumption		No load, quiescent mode	-	690	1450	µA
TS_OPAMP_VOUT	ADC sampling time when reading the OPAMP output.		-	400	-	-	ns
CMRR	Common mode rejection ratio		-	-	90	-	dB
PSRR	Power supply rejection ratio		DC	73	117	-	dB
GBW	Bandwidth		-	-	8.2	-	MHz
SR	Slew rate		-	-	4.7	-	V/µs
R_{LOAD}	Resistive load		-	4	-	-	kΩ
C_{LOAD}	Capacitive load		-	-	-	50	pF
VOH_{SAT}	High saturation voltage		R_{load} = min, Input at V_{DDA}.	-	-	100	mV
			R_{load} = 20K, Input at V_{DDA}.	-	-	20	
VOL_{SAT}	Low saturation voltage		Rload = min, input at 0V	-	-	100	
			Rload = 20K, input at 0V.	-	-	20	
φm	Phase margin		-	-	62	-	°
$t_{OFFTRIM}$	Offset trim time: during calibration, minimum time needed between two steps to have 1 mV accuracy		-	-	-	2	ms
t_{WAKEUP}	Wake up time from OFF state.		$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ, Follower configuration	-	2.8	5	µs

Table 81. Operational amplifier characteristics[1] (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
R$_{network}$	R2/R1 internal resistance values in PGA mode [2]	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error		-	-1%	-	1%	
I$_{bias}$	OPAMP input bias current	-	-	-	±0.2[3]	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\dfrac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design, not tested in production.

2. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1

3. Mostly TTa I/O leakage, when used in analog mode.

Figure 47. OPAMP voltage noise versus frequency
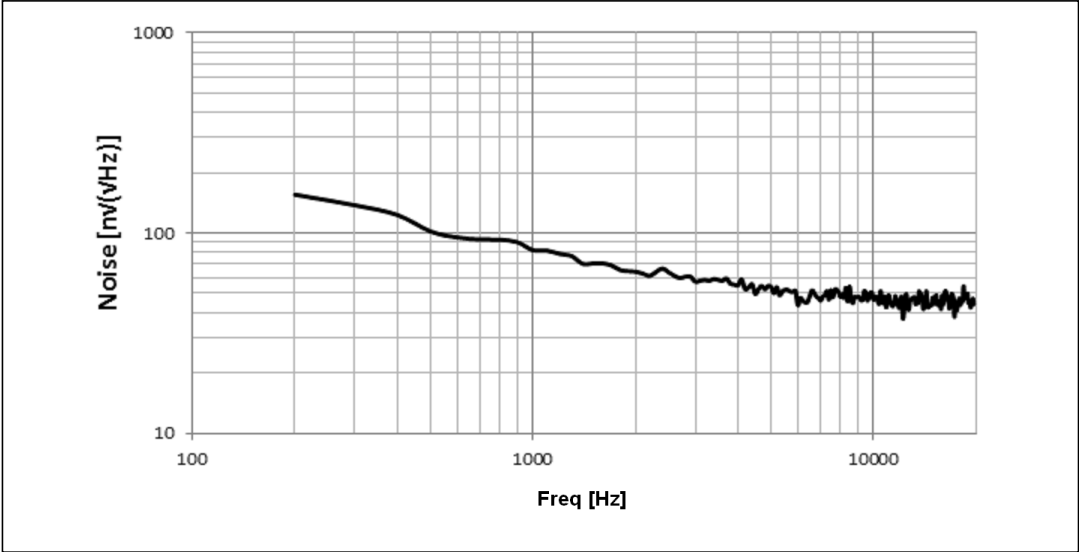
6.3.23 Temperature sensor characteristics

Table 82. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}[1]	Startup time	4	-	10	μs
T_{S_temp}[1][2]	ADC sampling time when reading the temperature	2.2	-	-	μs

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

Table 83. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

6.3.24 V_{BAT} monitoring characteristics

Table 84. V_{BAT} monitoring characteristics

| Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er[1]	Error on Q	-1	-	+1	%
T_{S_vbat}[1][2]	ADC sampling time when reading the V_{BAT} 1mV accuracy	2.2	-	-	μs

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

7 Package characteristics

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 48. LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline
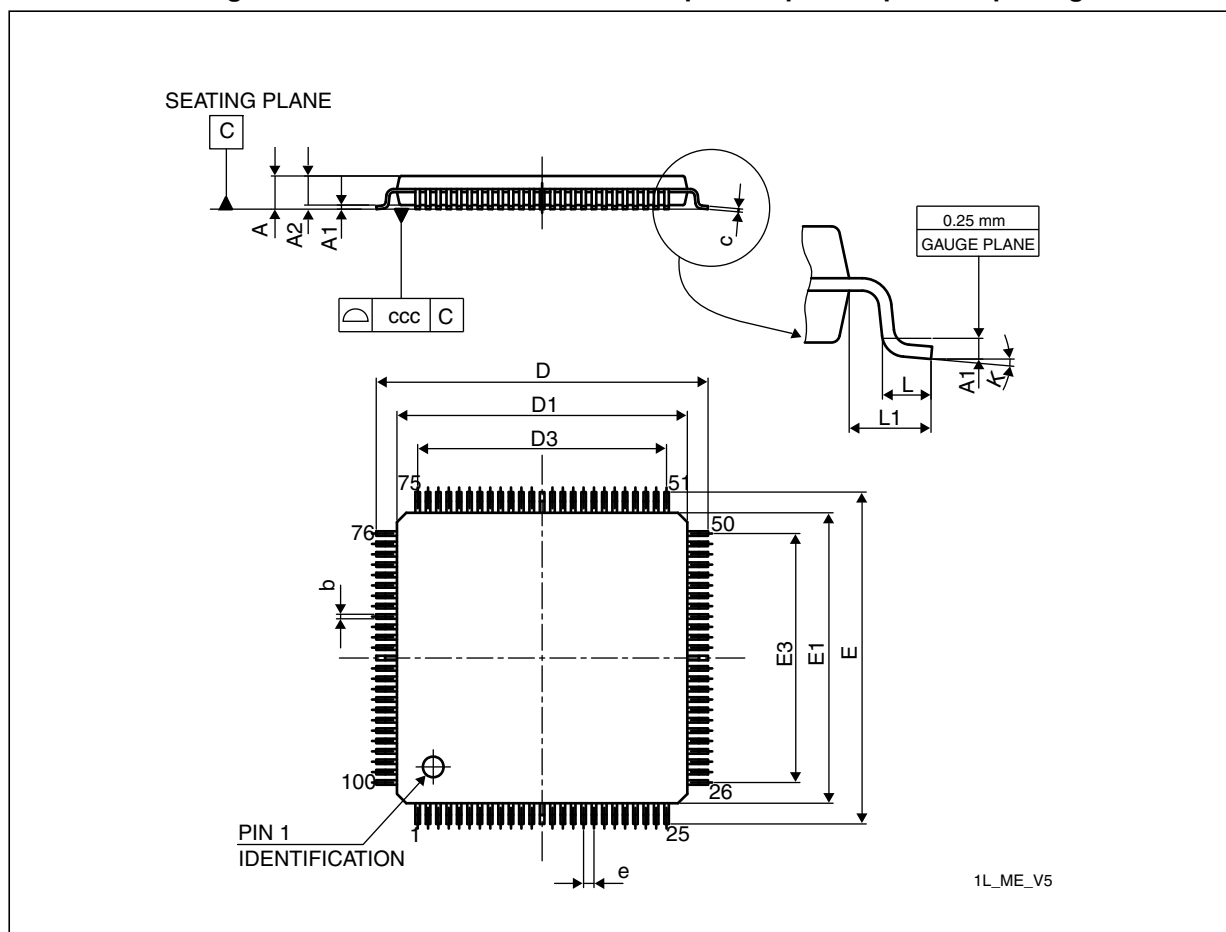
1. Drawing is not to scale.

Table 85. LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-

Table 85. LQFP100 – 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031
K	0°	3.5°	7°	0°	3.5°	7°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 49. LQFP100 recommended footprint
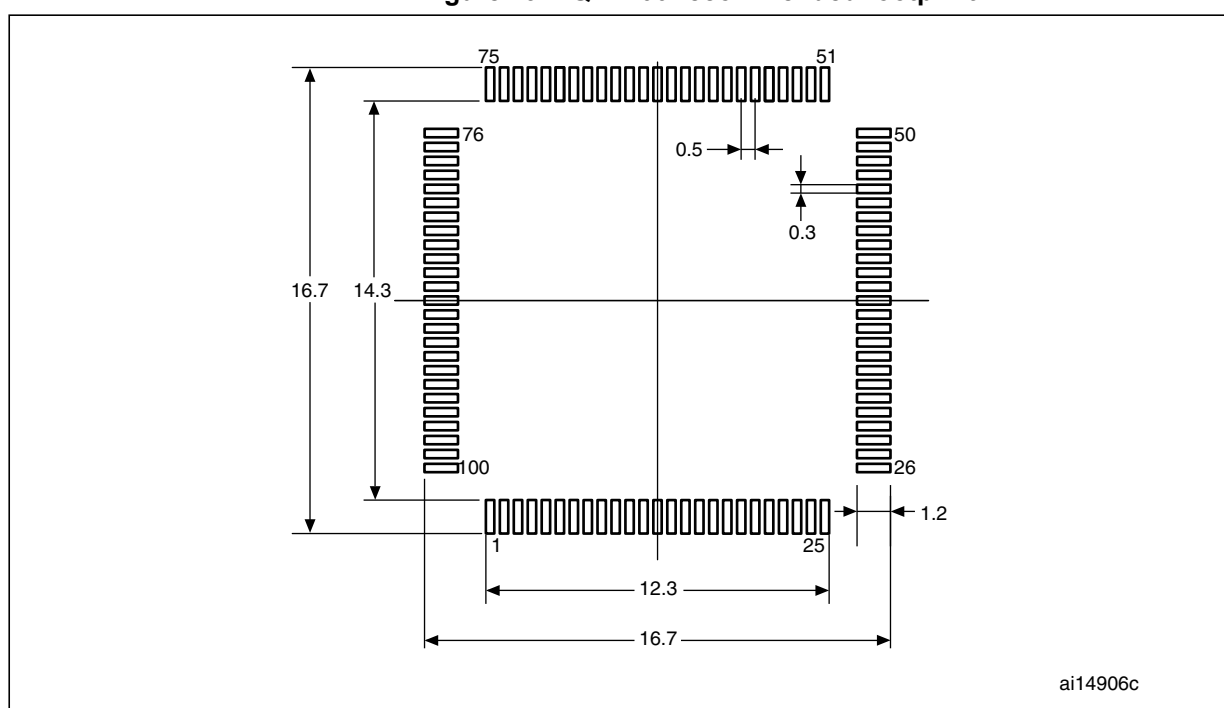
1. Dimensions are in millimeters.

Device marking for LQFP100

The following figure shows the device marking for the LQFP100 package.

Figure 50. LQFP100 marking example (package top view)
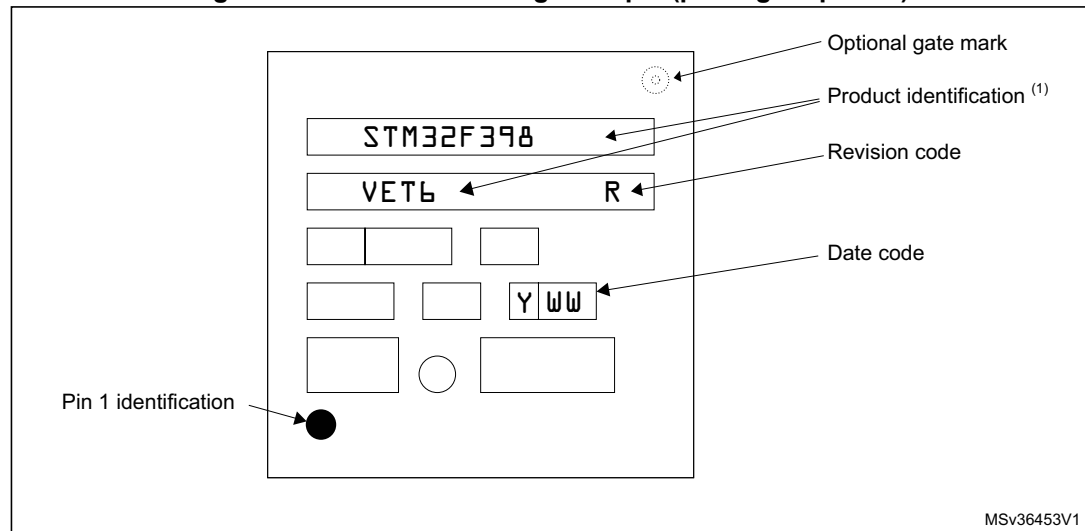
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 18: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum temperature in °C,
- Θ_{JA} is the package junction-to- thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ ($V_{OL} \times I_{OL}$) + Σ (($V_{DD} - V_{OH}$) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 86. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-** LQFP100 - 14 × 14 mm	42	°C/W

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use the STM32F078x at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 86* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Note: *With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).*

Suffix 6: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 7: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 125-18.774 = 106.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperature with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 86* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 51* to select the required temperature range (suffix 6 or 7) according to your temperature or power requirements.

Figure 51. LQFP100 P$_D$ max vs. T$_A$
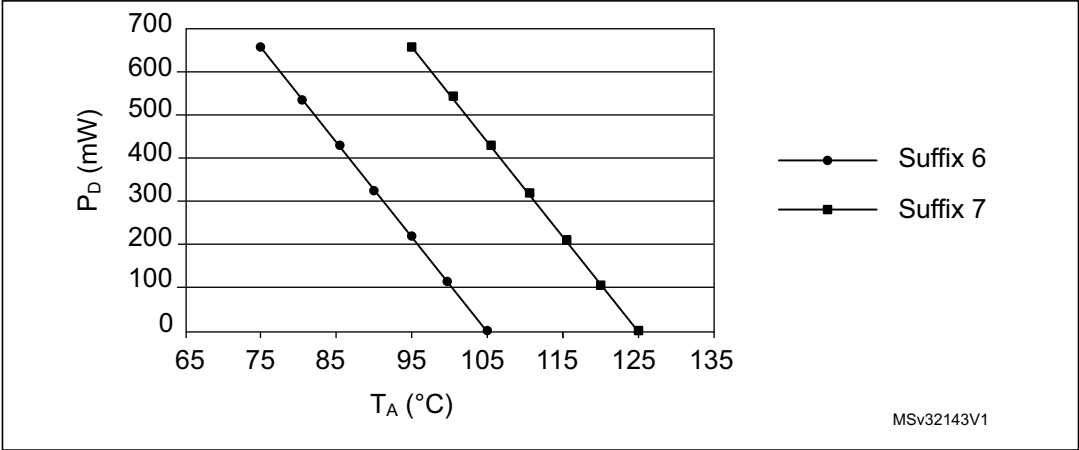
8   Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 87. Ordering information scheme

Example: STM32   F   398   V   E   T   6   x

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = General-purpose

Sub-family
398 = STM32F398xx

Pin count
V = 100 pins

Code size
E = 512 Kbytes of Flash memory

Package
T = LQFP

Temperature range
6 = –40 to 85 °C
7 = –40 to 105 °C

Options
xxx = programmed parts
TR = tape and reel

9 Revision history

Table 88. Document revision history

Date	Revision	Changes
27-Jan-2015	1	Initial release.

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