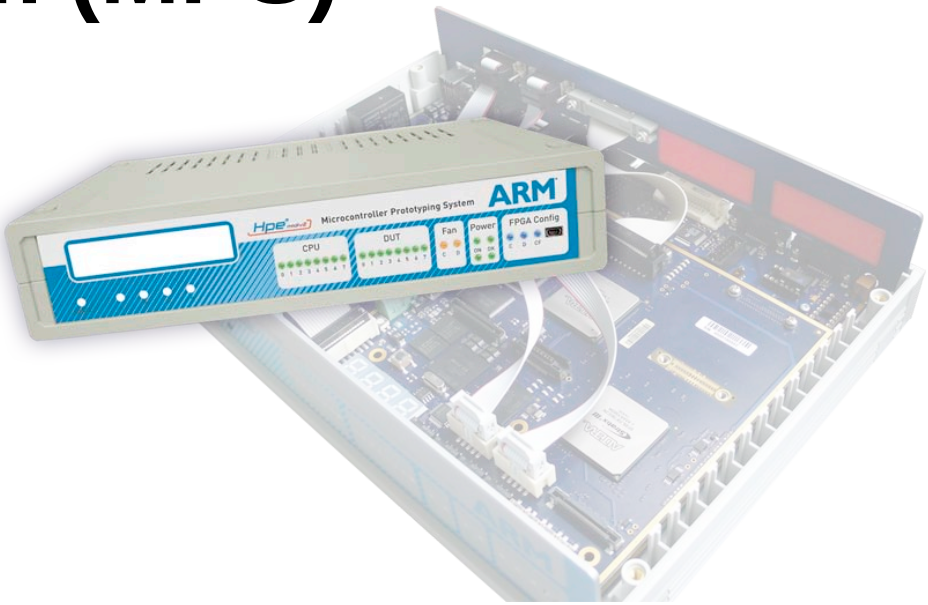
Microcontroller Prototyping System (MPS)



Imagine you would like to develop…

- A microcontroller system based on ARM Cortex-Mx class processor for:
  - Any application of your choice, such as:
    - Wireless sensor network
    - Motor control solutions
    - Industrial control and automation
    - White goods
    - Medical
    - …

- MPS allows you to achieve
  - Finalize requirements with prototype demonstrator
  - FPGA prototyping avoids design iterations at silicon stage
  - Develop and validate software before first silicon is available

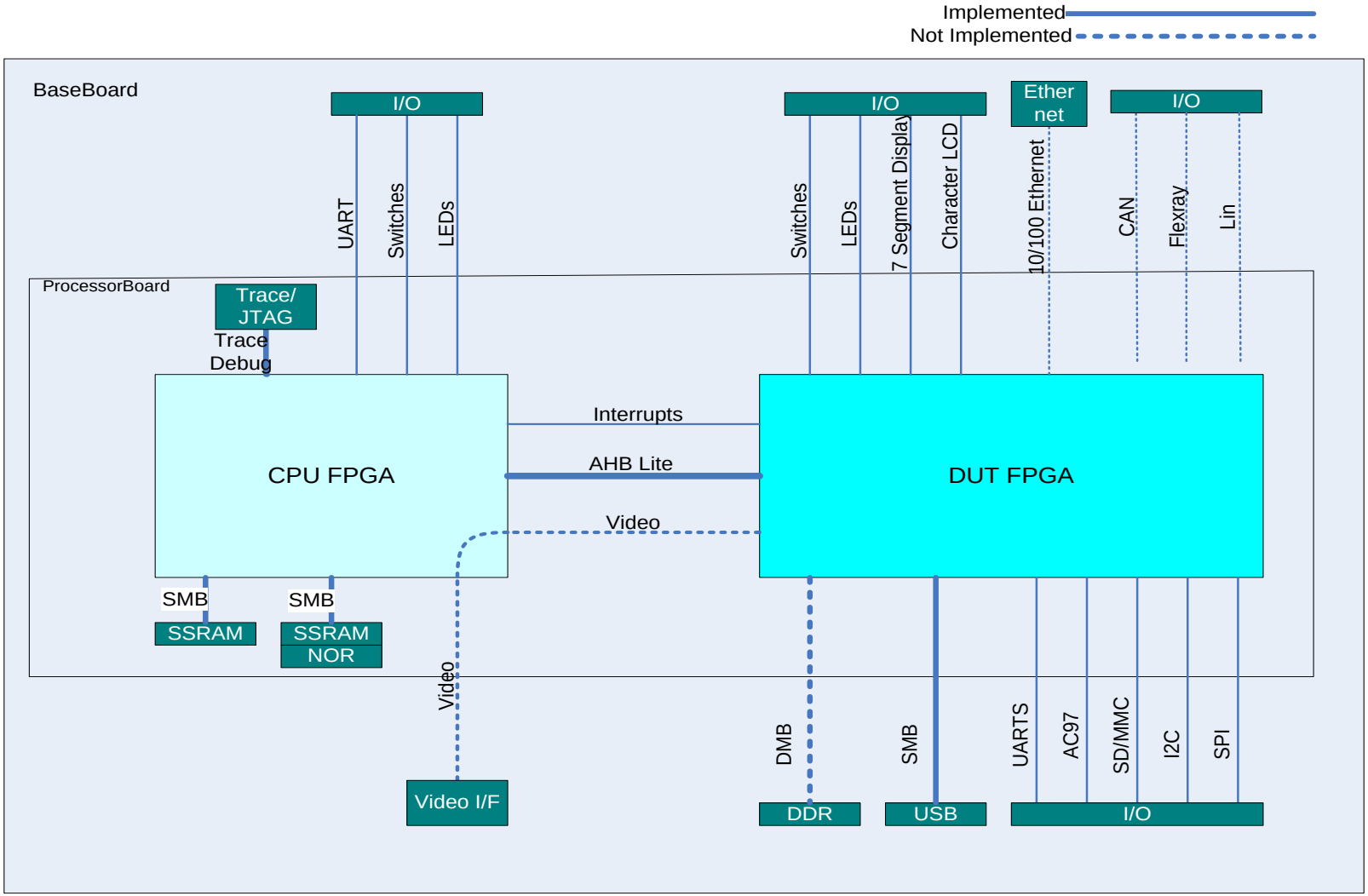
Microcontroller Prototyping System

- FPGA platform-based Cortex-M3/Cortex-M0 processors
  - Includes encrypted FPGA processor image for M0/M3 evaluation
  - Complete memory and peripheral interfaces
    - USB, Ethernet, DVI, SD/MMC, FlexRay, CAN
  - User expandable
    - Third-party IP and peripherals
  - Comprehensive Development Tools
    - Altera Quartus II (Web Edition)
    - Keil MDK-ARM (eval)
    - Keil ULINK2

MPS Deliverables

- MPS Hardware Platform
- FPGA Images
  - Encrypted Cortex-Mx class CPU FPGA images
  - Example DUT FPGA RTL, netlists, and images
- Development Tools
  - Keil MDK-ARM (evaluation version)
  - ULINK2 USB-JTAG adapter
  - Gleichmann HPE_desk™ configuration application
  - Altera Quartus II 8.1 Web Edition
- Utilities & Examples

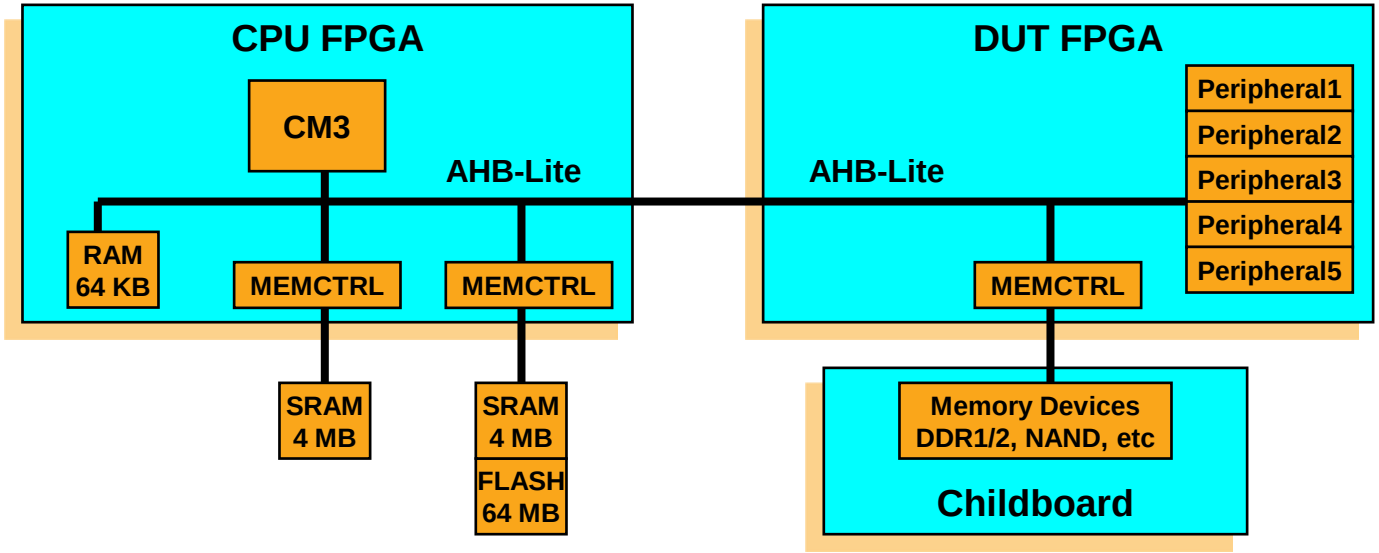
MPS Block Diagram



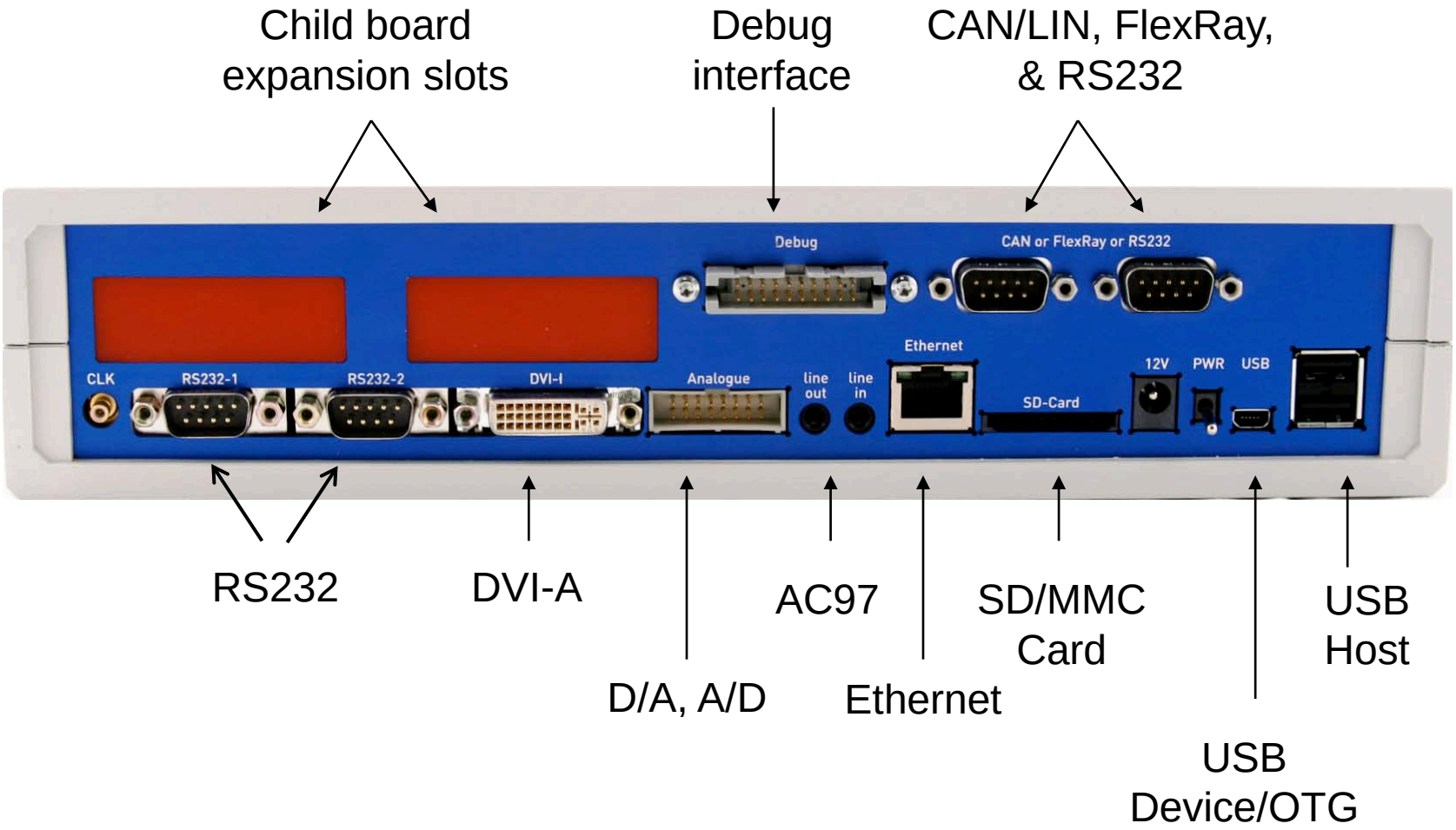
MPB-M3 Block Diagram I/O

MPS Memory System

- CPU Memory Interfaces
  - SRAM – 50MHz zero wait-state
    - 2x External (SMC0/SMC1) - 4MB 32-bit
    - Internal FPGA – 64KB 32-bit
  - NOR Flash
    - External SMC0 - 64MB 32-bit three AHB wait-states at 50MHz
- DUT Memory Interfaces
  - DDR1/2 SDRAM (via Childboard), 32-bit 100MHz



MPS I/O interfaces



IP supplied with MPS

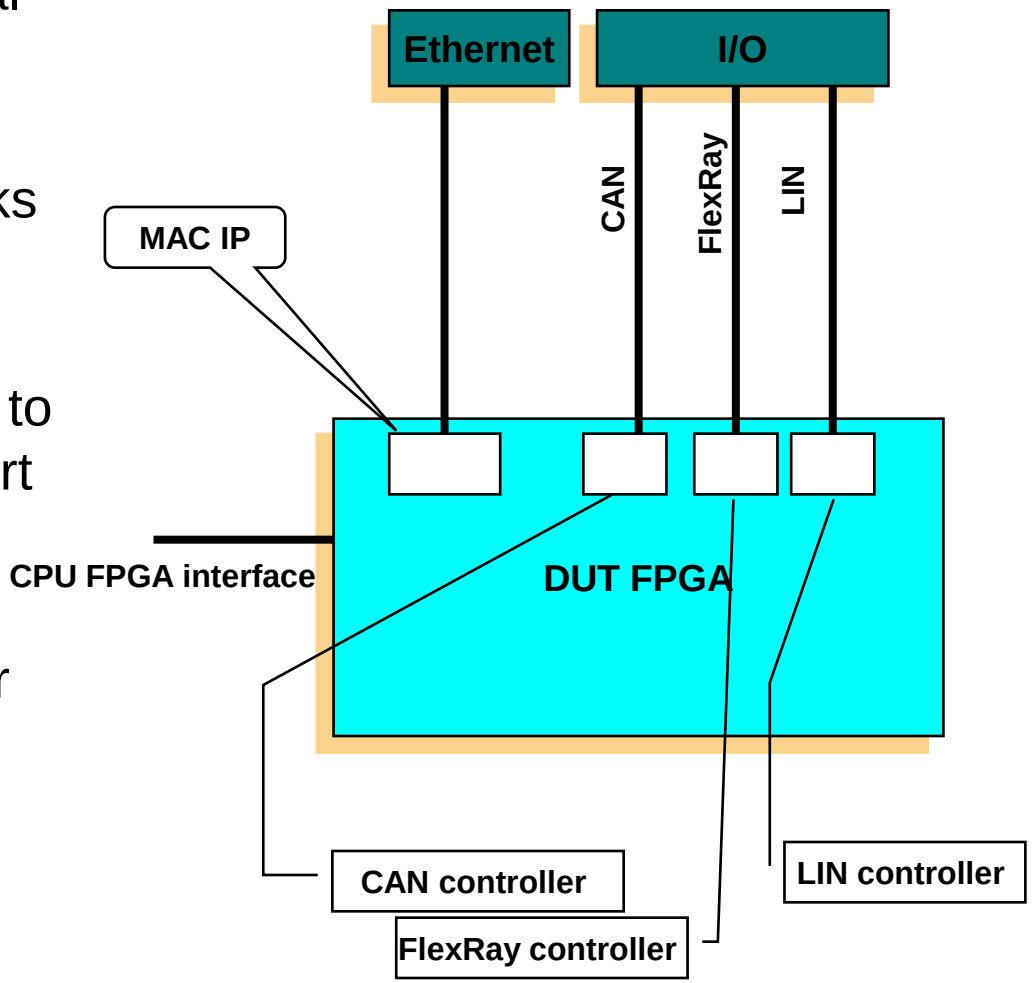
IP	Remarks
Cortex-Mx processors	Cortex-M3 (pre-loaded), Cortex-M0
Interrupt controller	Internal Interrupt controller
Static Memory Controller	SRAM, FLASH
UART	PL011; 4 * UART supplied
Character LCD controller	Verilog RTL supplied
Watchdog Timer	ARM SP804
Timer	ARM SP805
Real Time Clock	ARM PL031
SD/MMC Card Interface	ARM PL181
Advance Audio Codec Interface	ARM PL041
SSP Controller	ARM PL022
USB controller	External chip (ISP1761)

Supported Interfaces

- Integrated physical interfaces for
  - CAN
  - FlexRay
  - LIN
  - Video/LCD
  - Ethernet
  - Child board interface
    - Allows addition of any other i/o interface
- User should integrate controller IP

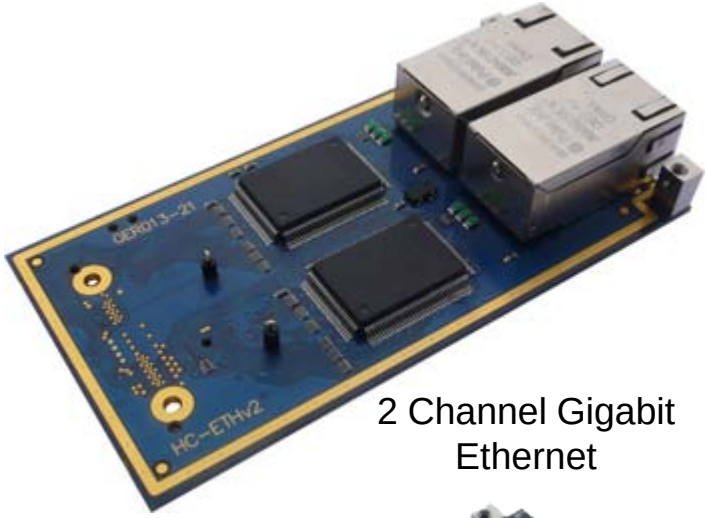
How to use Ethernet or CAN interface?

- MPS provides standard physical interfaces for Ethernet, CAN, FlexRay, & LIN
- The controller IP for these blocks are not provided with MPS
- In-house/third-party IP can be implemented in the DUT FPGA to build complete hardware support
- In-house/third party software drivers need to be developed in order to use these interfaces, or are supplied by the IP vendor.

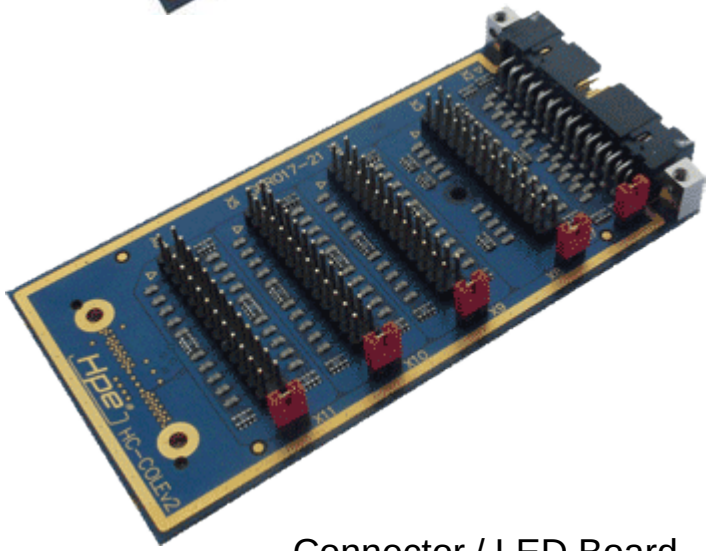


Expansion of I/O interfaces

- DUT “Childboard” interface can be used to expand the I/O features
- Off-the-shelf boards
  - Available from Gleichmann
    - USB Phy interface
    - 2 Channel Gigabit Ethernet
    - Connector LED board
    - SDRAM, DDR2
    - NAND
    - SSRAM and NOR Flash
- Custom I/O interface can be developed using this interface



2 Channel Gigabit Ethernet



Connector / LED Board (HC-COLEv2)

A Typical MPS Design Flow

H/W Design Entry
Customer preferred design entry tool

↓

H/W Synthesis, Place and Route
Altera Quartus II Web Edition

↓

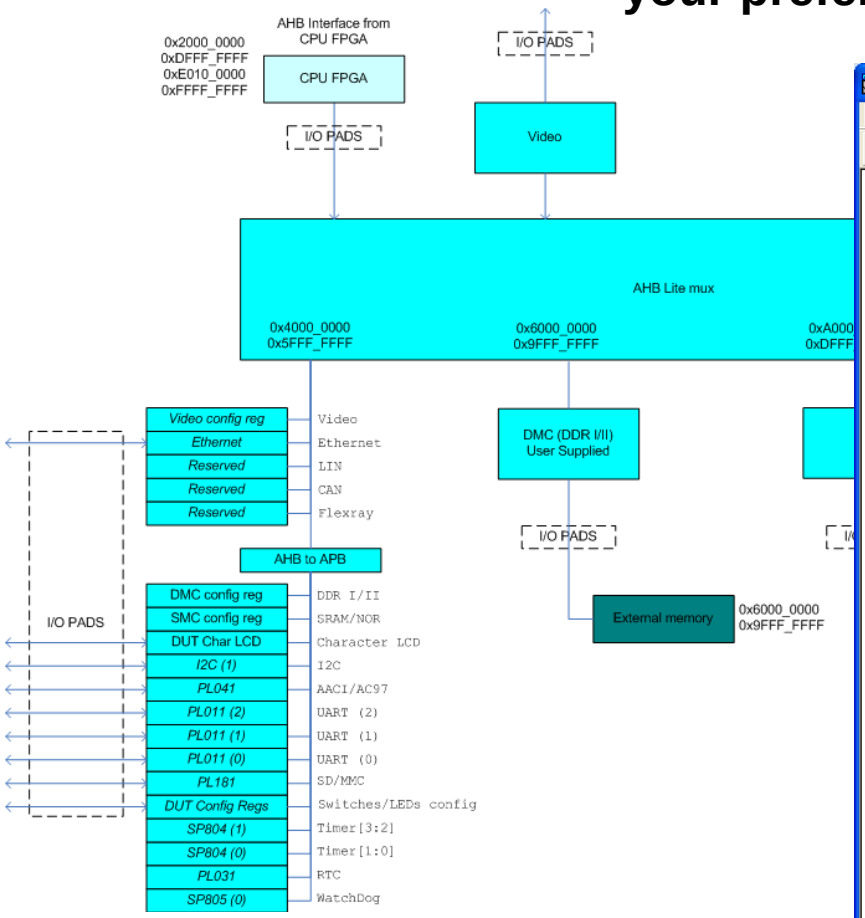
H/W Download to FPGA
Gleichmann HPE_Desk™

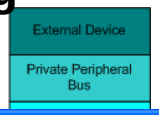
↓

S/W Development
Keil MDK and Ulink2
RVDS and RVI/RVT, 3rd party tools

H/W Design Entry

Create RTL design using your preferred tools





TextPad - [C:\work\Microcontroller_Prototyping_Board\fpga_dut\logical\verilog\dut_logic.v]

File Edit Search View Tools Macros Configure Window Help

```
    // Inputs
    .HADDR                  (HADDR),
    // Outputs
    .HSELAHBAPB             (HSELAHBAPB),
    .HSELCLCD               (HSELCLCD),
    .HSELDMC                (HSELDMC),
    .HSELUSB                (HSELUSB),
    .HSELDefault            (HSELDefault)
  );

  // AHB Slave return mux
  AHBMuxS2M_dut uAHBMuxS2M (
    // Inputs
    .HCLK                   (HCLK),
    .HRESETn                (HRESETn),
    .HSELAHBAPB             (HSELAHBAPB),
    .HREADYAHBAPB           (HREADYAHBAPB),
    .HRESPAHBAPB            (HRESPAHBAPB),
    .HRDATAAHBAPB           (HRDATAAHBAPB),
    .HSELCLCD               (HSELCLCD),
    .HREADYCLCD             (HREADYCLCD),
    .HRESPCLCD              (HRESPCLCD[0]),
    .HRDATACLCD             (HRDATACLCD),
    .HSELDMC                (HSELDMC),
    .HREADYDMC              (HREADYDMC),
    .HRESPDMC               (HRESPDMC),
    .HRDATADMC              (HRDATADMC),
    .HSELUSB                (HSELUSB),
    .HREADYUSB              (HREADYUSB),
    .HRESPUSB               (HRESPUSB),
    .HRDATAUSB              (HRDATAUSB),
    .HREADYDefault          (HREADYDefault),
    .HRESPDefault           (HRESPDefault),

    // Outputs
    .HREADYOut              (HREADYOut),
    .HRESP                  (HRESP),
    .HRDATA                 (HRDATA)
  );

  AHBDefaultSlave uAHBDefaultSlave (/*AUTOINST*/
    .HCLK                   (HCLK),
    .HRESETn                (HRESETn),
    .HTRANS                 (HTRANS),
    .HREADYIn               (HREADYOut),
    .HSELDefault            (HSELDefault),
    .HREADYOut              (HREADYDefault),
```

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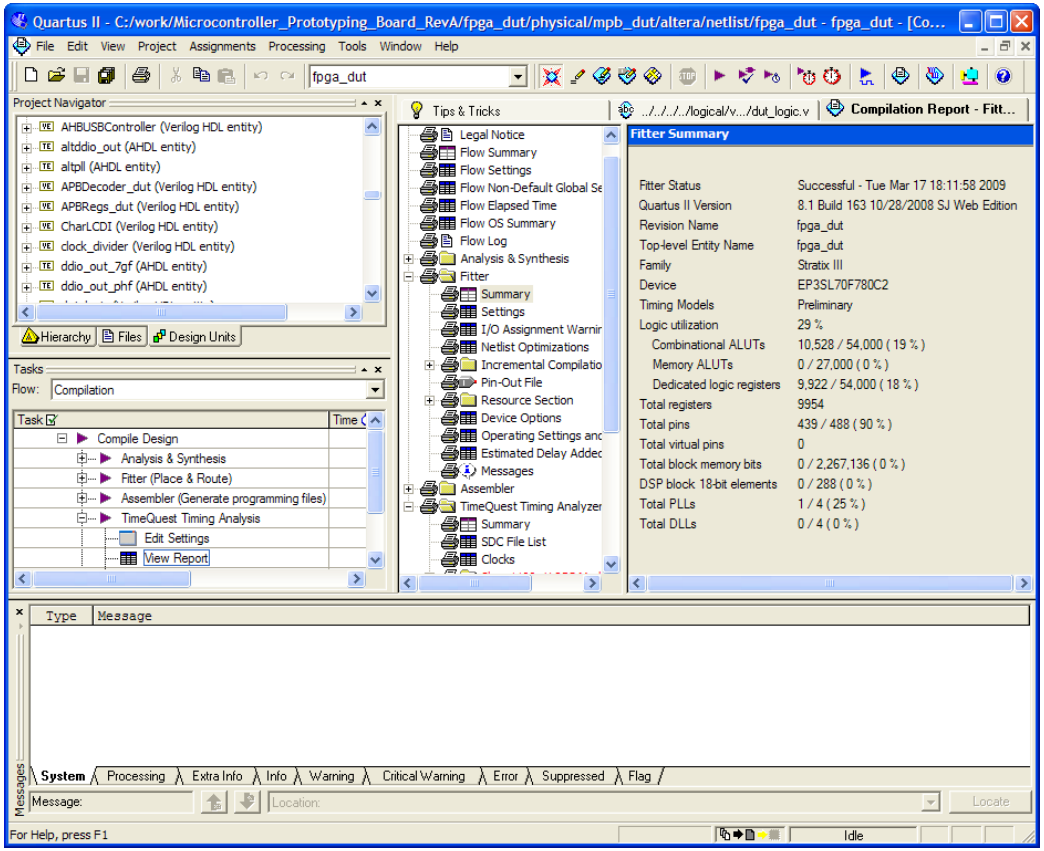
KEIL™ Tools by ARM

H/W Synthesis, Place and Route

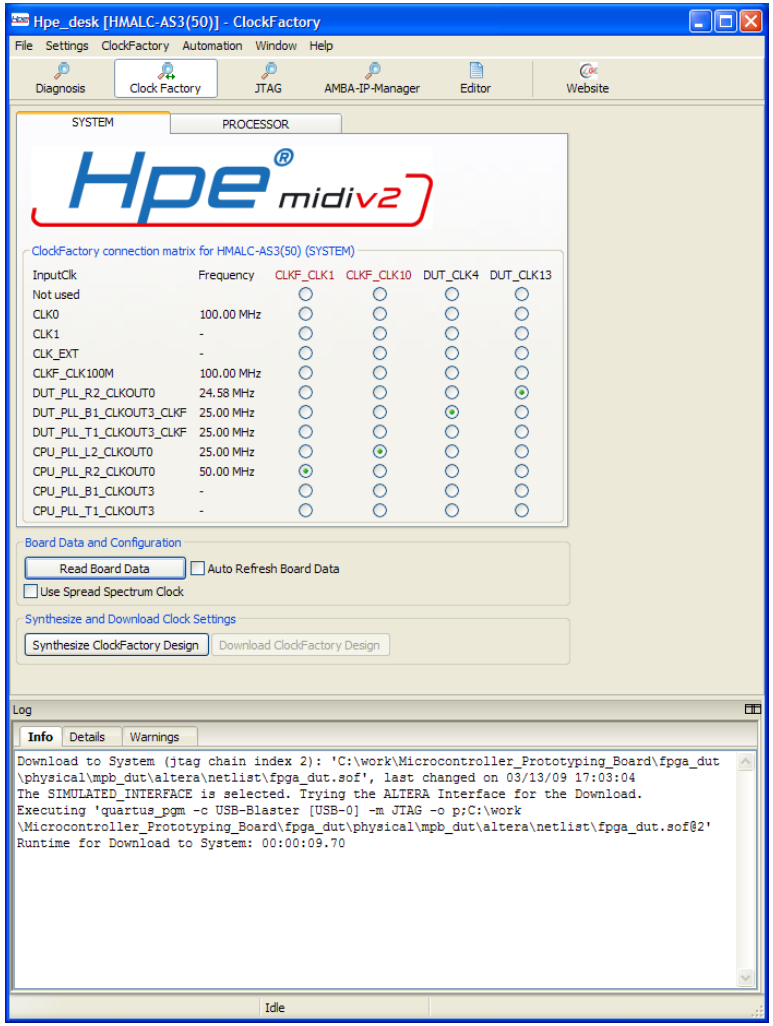
- Synthesize and Place & Route your design using Altera Quartus II software

- Quickly target the MPS using the supplied timing and placement files



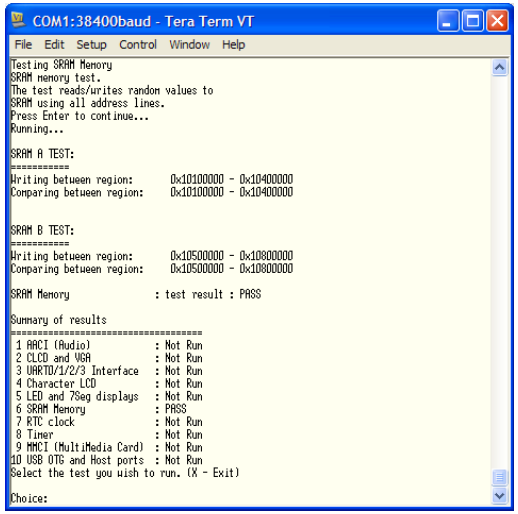
H/W Download to FPGA

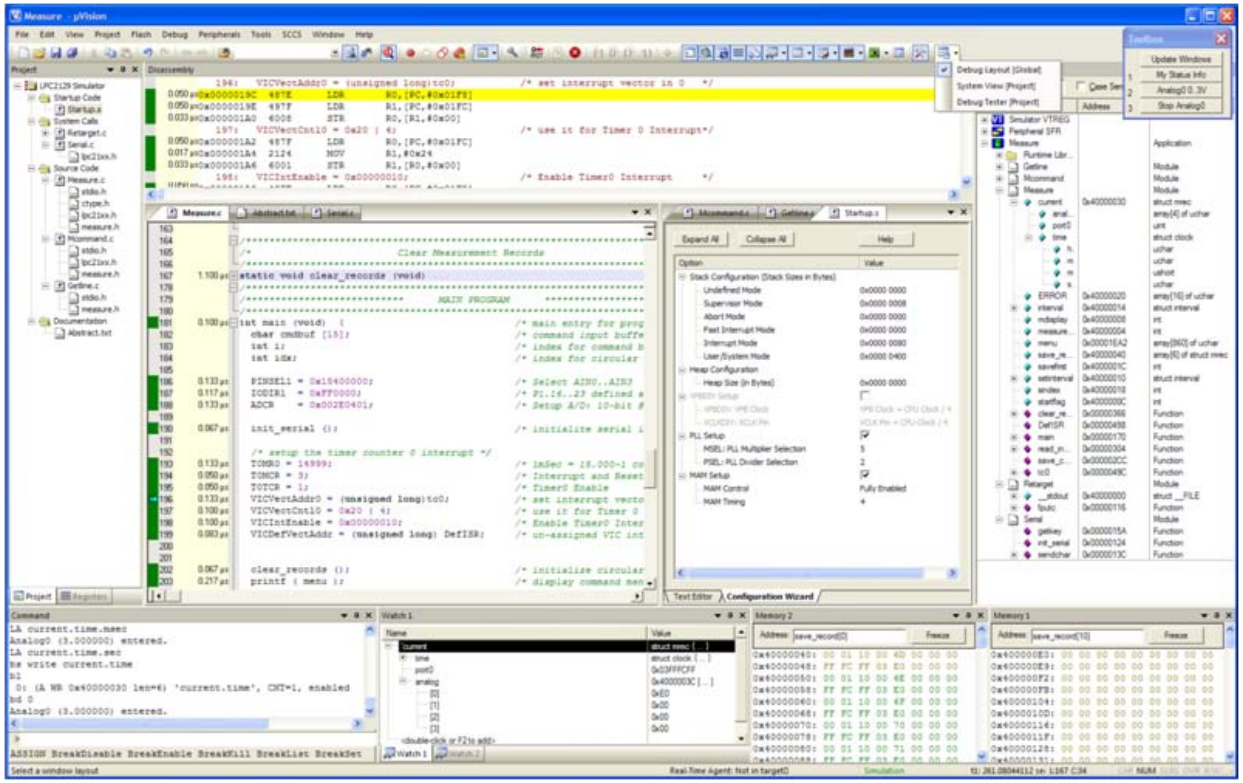
- Configure MPS using Gleichmann's HPE_desk tools
  - Download directly to FPGA to prove/debug hardware design
  - Program FPGA flash memory for stand-alone operation
  - Configure clock structure for system



S/W Development with MDK-ARM

- Use MDK and ULINK2 to develop and debug your Software
  - Download to SRAM
  - Debug Code
  - Program Flash
  - Example Code
  - Customer tests

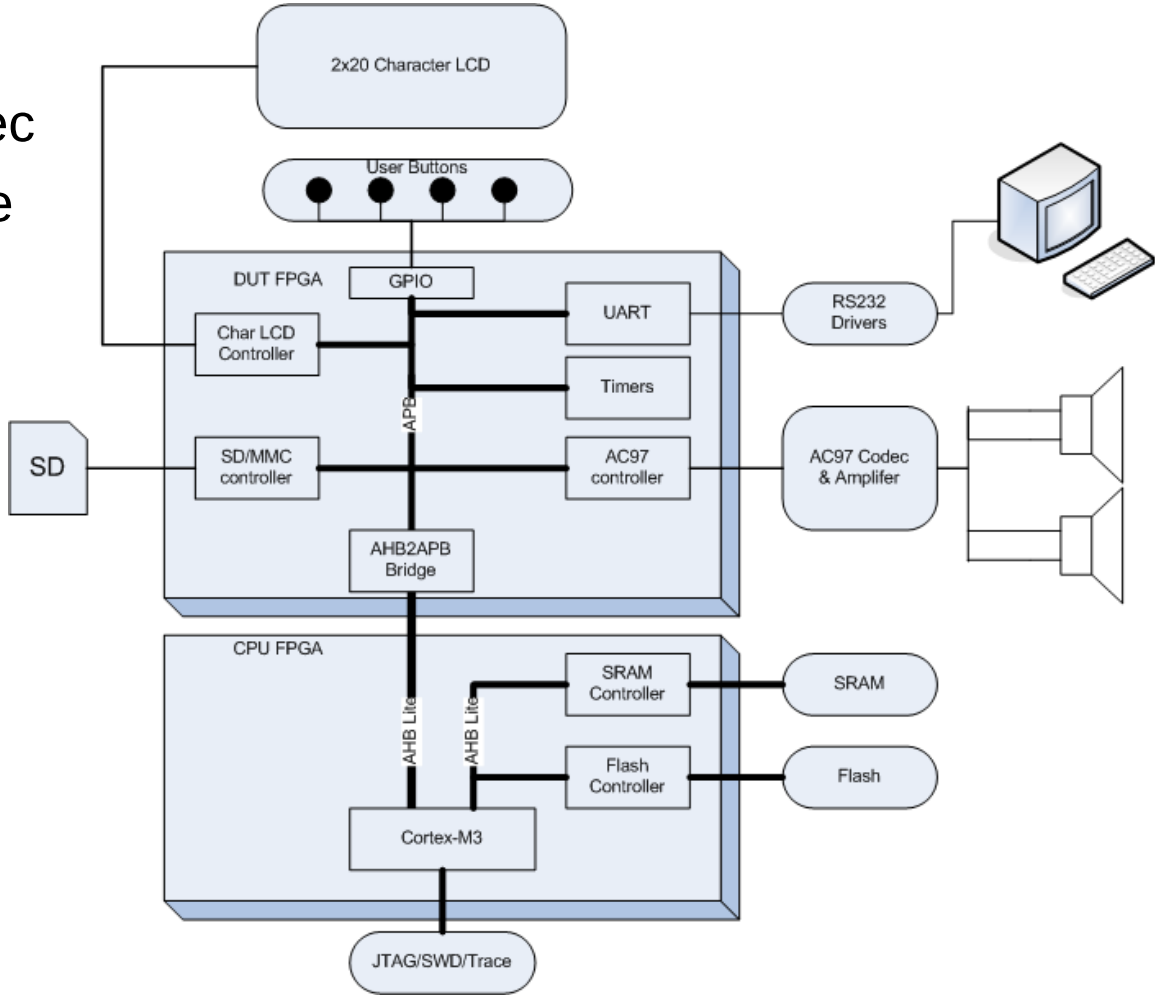




Demonstration

MP3 Player demonstration

- Uses MPS example design
  - Cortex-M3 processor
  - AACI/AC97 audio codec
  - SD/MMC card interface
  - Memory controllers
  - Character LCD
  - Serial Port
  - Timers
  - Buttons
  - JTAG/SWD debug



References

- Keil MPS - www.keil.com/mps
  - Application notes on MPS (June 09)
  - MPS Whitepaper (June 09)
- Keil MDK - http://www.keil.com/arm/
- Altera Quartus II - www.altera.com
- MSC/Gleichmann HPE_desk - http://www.ge-research.com
- Doulos Training - www.doulos.com

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