

HT-80C51 microcontroller

The HT-80C51 is the second-generation Handshake Technology implementation of the ubiquitous 80C51 8-bit microcontroller. Functionally compatible with the original 80C51, it allows designers to leverage the vast existing software library available on the market. It is ideal for use in any 80C51 application, delivering improved performance at a significantly lower power level. This highly flexible block is capable of operating in either synchronous or asynchronous mode and is fully configurable with a growing range of peripheral functions.

As with all Handshake Technology implementations, the HT-80C51 boasts minimal operational power consumption, zero stand-by power and immediate wake-up. This enables the maximum functionality to be squeezed into even the tightest energy budget and ensures optimal performance at any system-clock speed. Furthermore, very low electromagnetic emission (EME) levels and current peaks offer easy integration with RF and analog circuitry.

Applications

The HT-80C51 delivers unique benefits to any application where a clocked 80C51 core can be used, particularly when power consumption or electromagnetic interference is an important issue. Handshake Technology implementations of the 80C51 have been used in numerous ICs across various markets including wireless, smart card and automotive.

Key features

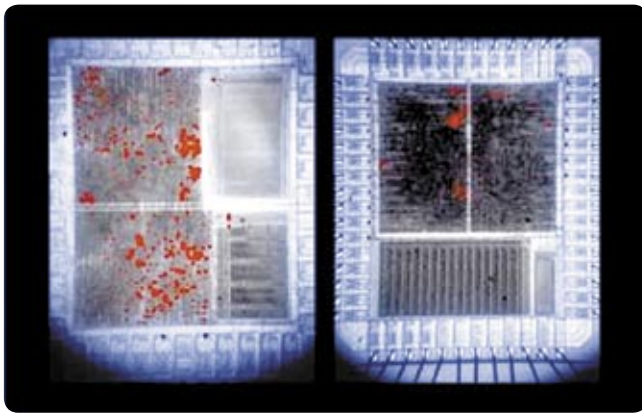
- Extremely low power consumption, just 0.15 nJ per instruction
- Very low electromagnetic emission
- Supply current peaks at least a factor of five lower than clocked alternatives
- Configurable core with a range of 80C51 peripherals and customizable memory interfaces
- Both core and peripherals consume zero power in idle mode yet immediately respond to interrupts
- Can operate in *asynchronous* or *synchronous* mode, controlled via a dedicated input or special function register (SFR)
 - In *asynchronous* mode the CPU runs at its natural speed and is not affected by a slow system clock
 - In *synchronous* mode the CPU synchronizes to the clock such that the number of clock cycles per instruction is the same as the number of machine cycles for a clocked implementation

Modules

The HT-80C51 implementation is functionally compatible with the original 80C51 core, with identical CPU and peripheral states at the instruction cycle boundaries. Numerous core and peripheral modules are available. These include:

- HT-80C51 CPU
- Interrupt controllers with different numbers of interrupt lines
- Timer 0
- Timer 1
- UART
- SPI
- I²C
- Peripheral bus bridge (connects synchronous peripheral modules)

Further peripheral functions are being developed, and specific modules can be implemented on demand.

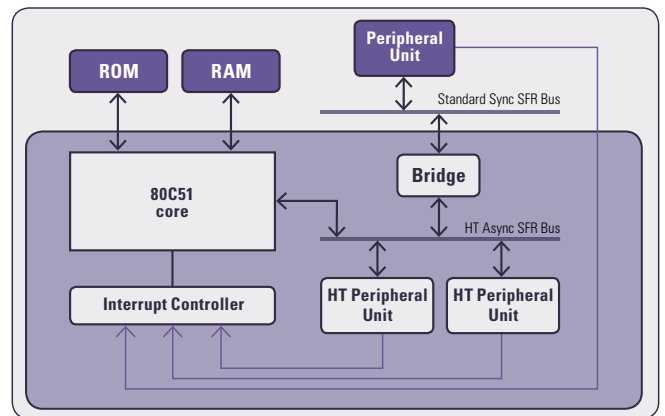


Photon emission images of a clocked (left) and Handshake Technology (right) 80C51 microcontroller executing the same program. The red dots indicate the level and distribution of power dissipation, which is clearly lower and more localized in the HT-80C51.

Delivery

The HT-80C51 delivery comprises:

- A firm netlist with the HT-80C51 design mapped onto the customer-selected standard-cell library
 - The netlist includes an optional Design-for-Test solution based on scan testing
- Test patterns for embedded scan test or the re-model files to enable generation of the patterns
- Various scripts to support the hardening of the design via tasks such as
 - Drive-strength fixing
 - Local clock tree balancing
 - Scan-clock distribution
 - Delay adjustment to adapt timing margins to post-layout timing parameters



HT-80C51 Subsystem

Characterization

The following table is valid at 25 °C for fully scan-testable cores manufactured in a typical 1.8 V, 0.18 μm CMOS process.

	Area (Geq)	Performance ¹		Power consumption	
		(MIPS)	(MHz)	(pJ / instruction)	(mW / MHz)
HT-80C51	6000	6.3	60.5 ²	150	0.016
Standard clocked 80C51 ³	5600	4.8	46.0	500	0.052

¹ The average execution time of an instruction is 9.6 clock cycles (1.6 machine cycles)

² Equivalent performance assuming 6 clock cycles per machine cycle

³ 6 clock cycles per machine cycle