Flip80251 Typhoon

Top performance 8/16-bit microcontroller

Overview

The Virtual Component Flip80251 "Typhoon" is an **accelerated version** of the Intel C251 microcontroller. It is 100 % binary code upward compatible with the legacy 80C251 but optimized for **the best ratio Performance/ Complexity!**
Flip80251 Typhoon targets 8/16 microcontroller applications requiring an increase processing power, a reduced operating frequency or a larger memory space.

Its enhanced pipeline architecture provides an increase of processing speed an average of 2.0 times, when running at the same clock frequency as a standard C251 real component and up 24 times faster than a legacy 80C51.
The extra processing power can be used, either to increase the performance of any 80C51/C251-based application, or to run the same application at a lower clock frequency so as to save power!
The architecture can provide a significant code size reduction when compiling C programs while fully preserving assembly code written for 80C51 microcontroller.
Flip80251 Typhoon, as any other member of our family of microcontrollers, is fully configurable, which means it is delivered in the precise configuration meeting user's requirements together with its **Virtual TestBench** for ensuring a **SoC right-on-first pass** per the **VSIA** standard.

Key Features

- Full binary code compatibility with 80C51/8xC251
- **Speed** is on average **2.0 times faster** than the legacy 8xC251 based on **the total number of clock cycles for all the instructions** and **Speed** is up to **24 times faster** than a standard 80C51
- Conversely, the **clock frequency** can **be divided by 2.0** on average while preserving the same performance than with the legacy 8xC251
- An instruction pipeline that allows single cycle execution for most of the instructions
- Enriched C51 instruction set **(source mode)**
  - 16-bit & 32-bit arithmetic and logic instructions.

Compare and conditional jump instruction

- **Hardware Wait State** solution for asynchronous peripherals and low cost memories
- 24-bit linear addressing
  - Up to **8 Mbytes of program memory**
  - Up to **8 Mbytes of data memory**
- Register-based CPU with registers accessible as **Bytes, Words and Double Words**
- Power-saving modes (**Idle** and **Power-down**) and an external **Clock/Power Management Unit** provide solutions for low-power applications

Configurable Features

- A full set of peripherals:
  - **P**rogrammable **C**ounter **A**rray
  - Watchdog Timer
  - Enhanced UART
  - Up to 3 Timer/counters
  - SPI
  - I2C Master/Slave
- A patented new emulation system using JTAG interface (**Emulation link**): Processor Open Clone (**POC**)
- AHB bus interface allowing the Flip80251-Typhoon to be used either as a **P**eripheral **C**ontroller **U**nit or as the main controller in an AMBA-based system.

Applications

Central **P**rocessing **U**nit

- High-Speed Modems
- Printers
- DVD ROM and players
- Scanner
- High-End Joystick

Peripheral **C**ontrollers

- Smart card
- Portable Telecom devices

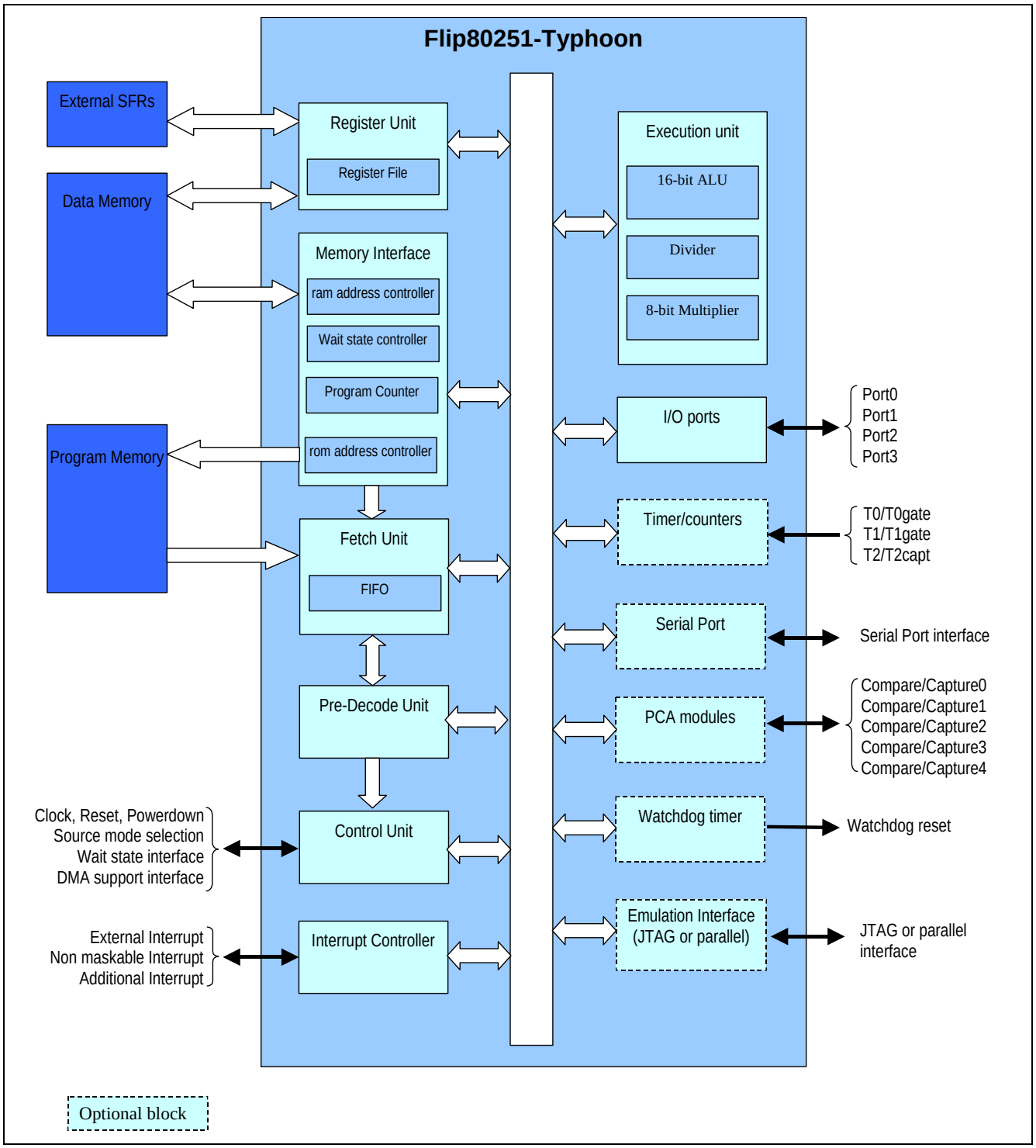

Figure 1: Flip80251-Typhoon Block Diagram

Functional Description

The Flip80251-Typhoon is partitioned into modules as shown in Figure 1:

- **Fetch Unit**

This block stores the current instruction and its operands.

- **Pre-decode Unit**

This block decodes the current instruction and prepares the execution of this instruction.

- **Control Unit**

This block is the instruction sequencer. It generates the control signals for the data path depending on the instruction being executed.

- **Execution Unit**

It includes a 16-bit ALU that allows to perform 8, 16 and 32-bit arithmetic and logic operations, an 8-bit multiplier and a parallel divider. It can also perform single bit manipulation.

- **Register Unit**

The Flip80251-Typhhon implements a register file that consists in 40 bytes location accessible as bytes, words and double words. Additionally, the register unit implements the logic needed to access external SFRs.

- **Memory Interface**

This block interfaces with Program and Data Memory, generating the memory control signals. It also implements the Program Counter that provides the addresses of the instruction to be fetched and the data memory address bus.
The memory interface provides a flexible hardware-control solution for wait state purpose. Once the device that needs a longer access asserts the busy input signal, the CPU is stalled. This wait state solution is available for both program and data memory.

Interrupt Controller

Block that manages up to 9 interrupts (externals + peripherals) in standard configuration. 7 additional interrupts can be added to the design on request. The interrupt controller determines whether an interrupt should be granted or not and when it will be granted. It also provides the vector address of the corresponding interrupt to the PC Unit.

I/O Ports

The Flip80251-Typhoon separates out external interrupts from the I/O ports allowing real 32 bits of general purpose I/O.
It is possible to connect the signals PjIn, PjOut and PjDir (where j=0,1,2,3) to bi-directional pads to obtain an I/O port. The I/O port signal direction PjDir is controlled by an extra Special Function Register called Pj_Dir. PjDir registers are located at addresses 0xAC, 0xAD, 0xAE, 0xAF. When bit I of PjDir is set to '1', bit I of Pj is used as input (PjIn[I]), otherwise bit I of Pj is used as output (PjOut[I]).

- **Jtag or parallel emulation interface**

To debug a system including a SoC embedding Flip8051 or a prototype of this SoC, the developer can use a POC-based emulator so called Core Emulator. To allow the use of such emulator, the Flip8051 model must include the Emulation Interface, based either on the JTAG protocol in order to have no dedicated pins for emulation or on a parallel interface to benefit from real-time emulation.

- **Peripherals**

The Flip80251 is provided with the standard 8xC251 peripherals including 3 timers (timer 0, 1 and 2), a watchdog timer, an enhanced UART, a programmable counter array (PCA). Moreover, a large set of peripherals is available from Dolphin portfolio (I2C Master/Slave, SPI, HDLC…)

Clock/Power Management Unit (located outside the core)

Flip8051 can be provided with an external peripheral named Clock/Power Management Unit. The purpose of this block is to provide the clock to the Flip8051. It is available as **CPMU** (Clock/Power Management Unit)

The **CPMU** enables:
- to use a programmable frequency divider, enabling to **divide the clocks** by 2 to **16384**,
- to switch off the clock by program.
- to use an external ring-oscillator during an initialization phase of the main clock (e.g. issued from a crystal oscillator with a long wake-up time) that allows to speed up the wake-up of the microcontroller after a power down.

Instruction set

The Flip80251 has got two running mode which uses two different instruction set:

- In **binary mode**, the Flip80251 Typhoon is fully binary compatible with the original 80C51.
- In **source mode**, it uses an extended instruction set that allows performing 16-bit&32-bit operation.

Binary mode

In this mode, the Flip80251 Typhoon is fully binary compatible with the original 80C51 instruction set. Nevertheless, there are some differences between the Flip80251 Typhoon and the standard part. The number of clock cycle for each instruction is reduced for higher performance.

Most of the instructions are executed in a single clock cycle, instead of 2 clock cycles for the standard 8xC251. As a result, the speedup is approximately 2.0 times faster than the standard C251 and up to 24 times faster than standard 80C51.

Source mode

The source mode provides a new instruction set with

- an expanded set of move instructions
- new compare and conditional jump instructions
- 16-bit and 32-bit arithmetic and logic instructions.

This allows a great increase of the overall performance by reducing the number of instructions required for a given application. Both the execution time and the code size are significantly reduced.

Performance

- Overall speed improvement[1]: 1.9 X
- Typical Gate count[2]: 20 K gates

Instruction Set Speed comparison between standard C251 and Flip80251-Typhoon

Binary mode		Source mode	
Number of opcodes	**Speed Improvement (S.I.)**	***Number of instructions***	**Speed Improvement (S.I.)**
20	S.I. ≥ 3.0	**19**	S.I. ≥ 3.0
134	3 > S.I. ≥ 2.0	**47**	3 > S.I. ≥ 2.0
73	2> S.I. ≥ 1.0	**91**	2> S.I. ≥ 1.0
28	1.0 > S.I.	**0**	1.0 > S.I.
Total 255	**Weighted Average 2.0 X**	**Total 157**	**Weighted Average 1.8 X**

[1] Actual speed improvement depends on application program
[2] Flip80251 processor only. The given gate count does not include the peripherals since it depends on the configuration.

Pinout

Signal names are provided in the block diagram shown in figure 1 and described in the tables below.
I: input / O: output
Items marked with "*" indicate that they may not exist in some configurations

Name	I/O	Function
General Pins		
rst	I	Asynchronous reset. Active high.
clk	I	System Clock.
pwd	O	Powerdown mode indicator.
scanmode	I	Scan mode signal. Used to ease scan insertion
emrst*	O	Emulation asynchronous reset.
Memory interface		
romaddr [23:0]	O	Program memory address bus.
romdatain[7:0]	I	Data input for program fetch.
romoe_n	O	Output enable signal for program memory. Active Low.
ramaddr [23:0]	O	DATA memory address bus.
ramdatain[7:0]	I	Data input from DATA memory
ramdataout[7:0]	O	Data to write into DATA memory.
ramoe_n	O	Output enable signal for DATA memory. Active low.
ramwe_n	O	DATA memory write enable signal. Active low.
Memory wait state interface		
rombusy	I	Program memory wait state input
rambusy	I	Data memory wait state input.
External SFR interface		
sfraddr [7:0]	O	Address bus for external User-define Special Function Registers
sfrdatain [7:0]	I	Data read from external SFRs.
sfrdataout [7:0]	O	Data write to external SFRs.
sfrwe	O	SFR write control. Active high.
sfroe	O	SFR read control. Active high.
I/O ports		
port0in [7:0]	I	Port 0 Input.
port1in [7:0]	I	Port 1 Input.
port2in [7:0]	I	Port 2 Input.
port3in [7:0]	I	Port 3 Input.
port0out [7:0]	O	Port 0 Output.
port1out [7:0]	O	Port 1 Output.
port2out [7:0]	O	Port 2 Output.
port3out [7:0]	O	Port 3 Output.
port0dir [7:0]*	O	Direction control signal for port 0.
port1dir [7:0]*	O	Direction control signal for port 1.
port2dir [7:0]*	O	Direction control signal for port 2.
port3dir [7:0]*	O	Direction control signal for port 3.
Serial Port interface		
serialin*	I	Serial port data input.
serialout*	O	Serial port data output.
serialclk*	O	Serial Clock output for mode 0.
serialdir*	O	Serial Data direction for mode 0.
serialmode0*	O	Serial mode 0 indicator.
Timer interface		
timer0*	I	Timer 0 input.
imer0gate*	I	Timer 0 Gate control input.
timer1*	I	Timer 1 input.
timer1gate*	I	Timer 1 Gate control input.
timer2*	I	Timer 2 input.
timer2capt*	I	Timer 2 Capture control input.
wdtrst	O	Watchdog timer overflow.

Name	I/O	Function
PWM interface		
pwmout*	I	Pulse width modulator output signal.
PCA interface		
eci	I	PCA external input clock
capture0	I	Capture input 0
capture1	I	Capture input 1
capture2	I	Capture input 2
capture3	I	Capture input 3
capture4	I	Capture input 4
compare0	O	Compare output 0
compare1	O	Compare output 1
compare2	O	Compare output 2
compare3	O	Compare output 3
compare4	O	Compare output 4
pcarst		PCA software reset. Active high.
External interrupt interface		
int0_n	I	External interrupt 0
int1_n	I	External interrupt 1.
nmi	I	Non maskable interrupt input
extraint [6-0]*	I	Additional External Interrupt
Pins for the test		
busmon[31:0]	O	Debug purpose interface (No additional gates)
Direct Memory Access support interface		
busrequest*	I	Request from a DMA controller to take control of the memory busses (active high)
busgranted*	O	Indication that bus control is granted to the DMA controller (active high)
Emulation interface (JTAG or parallel)		
JTAG interface		
trst*	I	Test Reset, active low.
tck*	I	Test clock..
tdi*	I	Test Data Input. Serial test instruction and data are received by the test logic at tdi.
tdoflip*	O	Test Data Output. It is the serial output for the data registers from the test logic.
ntck*	I	Not tck. Used to have only positive edge trigger register in the design and no gated clock within the core
instrreg[7:0]	I	JTAG instruction register
tapctrl[2:0]*	I	Enable for data register. Output from TAP controller.
Parallel interface		
emuldatain[15:0]	I	Input data bus for emulation.
emuldataout[15:0]	O	Output data bus for emulation.
emuldatadir	O	Control for mux emuldata busses.
emulctrl[2:0]	I	Control signals for emulation.

Deliverables

- Available as fully synthesizable equational model either in VHDL or Verilog-HDL format.
- Supplied with a large set of program for testing the core and its peripherals, providing 100 % code coverage.
- Automatic error detection during test simulation (self test program)
- Synopsys synthesis scripts
- User Documentation
  - ViC specification
  - User guide

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