R8051XC-B

80515-Compatible Microcontroller Core

A pre-configured version of the R8051XC that implements an 80515-like 8-bit microcontroller that executes all ASM51 instructions. It has the same instruction set as the 80C31, but executes operations an average of eight times faster.

The R8051XC-B provides hardware and software interrupts, interfaces for serial communication, a timer system with compare-capture-reload resources, a watchdog timer, I/O ports, an Infineon-compatible interrupt scheme, and a power management unit. Integrated on-chip debugging is also available, using either native OCDS or FS2's OCI.

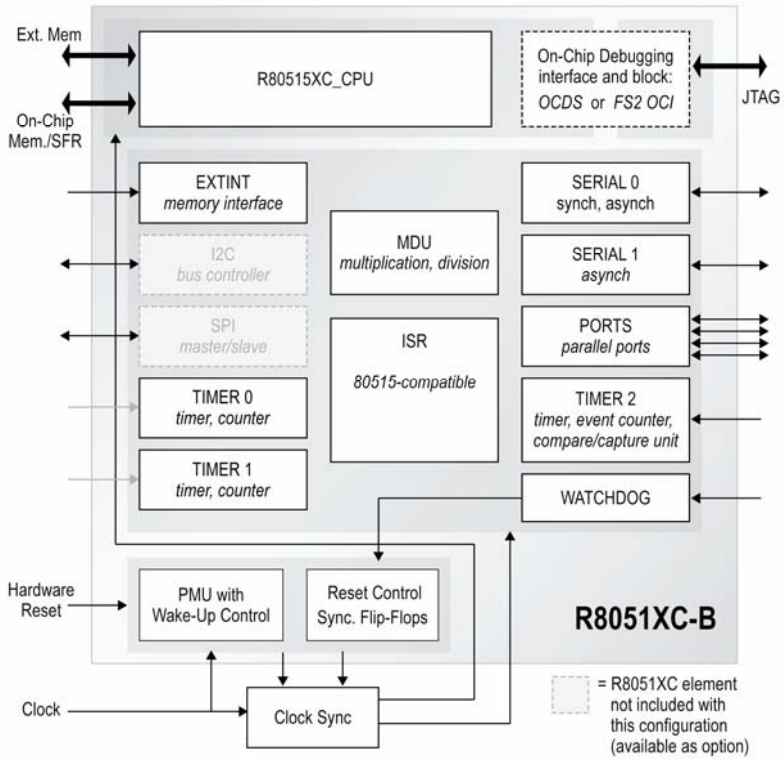
The R8051XC-B is one of our proven 8051 family of processor cores, which have been successfully implemented in a hundred different customer products. Representative ASIC implementation data shows it to offer competitive performance and area results, requiring for example about 24,000 gates for 256 MHz or 17,000 gates for 100 MHz.

Developed for easy reuse in ASIC and FPGA implementations, the microcode-free design is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset. Scan insertion is straightforward.

Applications

The R051XC-B is suitable as a primary or secondary controller in a wide variety of applications, including 8-bit data processing systems, mobile and other products requiring low power consumption, high-speed control systems, and mixed-signal SoC applications.

Block Diagram



Features

- Control Unit
  - Eight-bit instruction decoder for MCS® 51 instruction set
  - Executes instructions with one clock per cycle (versus twelve for standard 80C51) for an average 8x speed up
- ALU performs 8-bit arithmetic and logical operations, Boolean manipulations
- Multiplication-Division Unit
  - 16 x 16 bit multiplication
  - 32/16 bit and 16/16 bit division
  - 32 bit L/R shifting and normalization
- 32-bit Input/Output ports: four 8-bit I/O ports; Alternate port functions such as external interrupts and serial interface are separated, providing extra port pins when compared with the standard 8051
- Three 16-bit Timer/Counters
- Compare/Capture Unit
  - Four 16-bit Compare registers for pulse width modulation
  - Four external Capture inputs for pulse width measuring
  - 16-bit Reload register for pulse generation
- Interrupt Controller with four priority levels and 13 sources
- 15 bit Prog. Watchdog Timer
- Internal Data Memory Interface can address up to 256 bytes of Read/Write Data Memory Space
- Special Function Registers interface services up to 74 External SFRs
- Power Management Unit – IDLE and STOP modes
- External Memory interface
  - Can address up to 64 KB of External Program and Data Memory each
  - De-multiplexed Address/Data Bus for easy connection to memories
  - Variable length MOVX to access fast/slow RAM or peripherals
  - Variable length code fetch and MOVC to access fast/slow program memory
- Optional interface for on-chip debug: native On-Chip Debug Support (OCDS) or FS2 On-Chip Instrumentation (OCI)

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Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

Central Processing Unit

Fetches instructions from program memory and uses RAM or SFRs as operands. Provides the ALU for 8-bit arithmetic, logic, multiplication and division operations and Boolean manipulations. The RAM and SFR interface can address up to 256 bytes of Read/Write Data Memory Space and built-in and off-core Special Function Registers. The memory interface can address from 64K to 8M bytes of Program Memory, and up to 64K bytes of External Data Memory.

Ports

The parallel I/O port controller serves up to 4 parallel 8-bit I/O ports to be used with off-core buffers. It is compatible with the classic Intel™ 80C51, but lacks the multiplexed memory feature and alternate functions (which could be combined off-core if required).

Timers 0 and 1

Timers 0 and 1 are nearly identical, with three modes: 13-bit timer/counter, 16-bit timer/counter, 8-bit timer/counter with auto reload. Timer 0's additional mode is two 8-bit timers.

Each timer can also count external pulses (1 to 0 transition) on the corresponding 't0' or 't1' pin. Another option is to gate the timer/counter using an external control signal, allowing it to measure the pulse width of external signals.

Timer 2

Operates as a timer, event counter, or compare/capture unit.

In timer mode, Timer 2 can be incremented every machine cycle or every second machine cycle, depending on the 2:1 prescaler. In event counter mode, Timer 2 is incremented when an external signal changes from 1 to 0 (sampled every machine cycle). Timer 2 is incremented in the cycle following the one in which that transition was detected. In gated timer mode, Timer 2's incrementing is gated by an external signal.

A reload of Timer 2 can be executed in two modes:

- Mode 0: Reload signal is generated by Timer 2 overflow (auto reload)
- Mode 1: Reload signal is generated by a negative transition at the corresponding input pin 't2ex'.

Compare/Capture Unit

The CCU within Timer2 performs compare and capture functions. For the Compare function, values stored in four 16-bit compare/capture registers are compared with the contents of the Timer 2 register. The results are signaled and interrupts are generated.

For the Capture function, actual timer/counter contents can be saved into one of four 16-bit registers upon an external event (mode 0) or software write operation (mode 1).

Multiplication Division Unit

This on-chip arithmetic unit performs these unsigned integer operations:

- 16-bit x 16-bit multiplication
- 32-bit/16-bit division and 16-bit/16-bit division
- 32-bit normalization and L/R shifting

The MDU allows operations concurrently to and independent of the engine activity.

Serial 0 and 1

The core includes two independent serial ports for simultaneous communication over two channels. They can operate in identical or different modes and at different communication speeds. Serial Port 0 is capable of both synchronous and asynchronous transmission, while Serial 1 provides asynchronous mode only.

In synchronous mode, the microcontroller generates a clock and operates in half-duplex mode. In asynchronous mode, full-duplex operation is available. Received data is buffered in a holding register, allowing the serial ports to receive an incoming word before software has read the previous value.

Serial Port 0 offers these different communication protocols:

- Synchronous mode, fixed baud rate
- 8- and 9-bit UART modes, variable baud rate
- 9-bit UART mode, fixed baud rate

Serial Port 1 has two operating modes:

- 8- and 9-bit UART mode, variable baud rate

Both include an additional Baud Rate Generator.

Power Management Unit (PMU) & Reset Control

Generates clock enable signals for the main CPU and for peripherals; serves Power Down Modes IDLE and STOP; and generates internal synchronous reset signal (upon external reset or watchdog timer overflow).

IDLE mode leaves the clock of the internal peripherals running. Power consumption drops because the CPU is not active. Any interrupt or reset will wake the CPU.

STOP mode turns off all internal clocks. The CPU will exit this state with an external interrupt or reset. Internally generated interrupts (timer, serial port, watchdog, ...) are disabled since they require clock activity.

Wake-up Control

The Wake-up From Power-Down Mode Control Unit services two external interrupts during power-down modes.

SFR Mux

The SFR Multiplexer provides a common bus multiplexer for all the internal and external Special Function Registers.

On-Chip Debugging

Serves as the interface for On-Chip Debug Support through an IEEE1149.1 (JTAG) port. Implements either native On-Chip Debug Support (OCDS) or FS2's On-Chip Instrumentation (OCI). See their respective datasheets for details.

Watchdog Timer

A 15-bit counter incremented every 24 or 384 clock cycles. After an external reset, it is disabled and all registers are set to zeros.

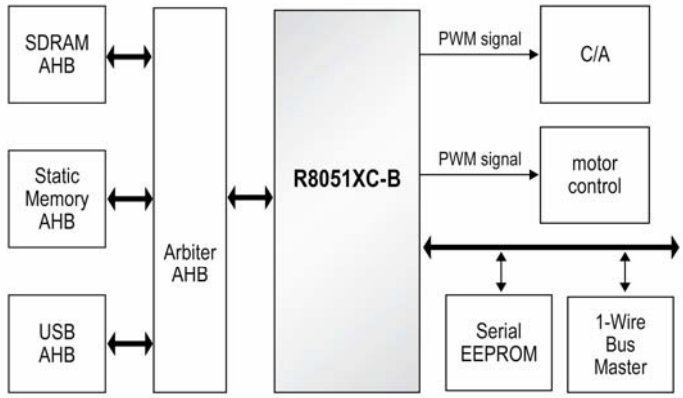
Can be started by applying an active input during reset (hardware automatic start), or by setting the enable bit by software. Once started, it cannot be stopped unless the internal reset signal becomes active. This occurs when the Watchdog enters the state of 7CFFh, and can be avoided by software-refreshing the Watchdog before it reaches 7CFFh.

Interrupt Service Routine Unit

The R8051XC-B provides an 80515-compatible interrupt controller with up to 18 interrupt sources and four priority levels. Each source has its own request flag(s) located in a dedicated special function register. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

Example Application

This block diagram suggests one way the core might be used in with AMBA AHB based system. Here an Arbiter interfaces the core with the AHB elements, its Timer2 communicates with external peripherals using pulse width modulation and very little CPU intervention; and other peripherals connect through the core's external memory (SFR) interface.



Implementation Results

R8051XC-B reference designs have been evaluated in a variety of technologies. The following results use worst-case conditions, exclude memories, and were optimized either for 100 MHz or for maximum speed.

Configuration	ASIC Technology	Approx. Area	Frequency
R8051XC-B	UMC 0.13µ	18,172 gates	100 MHx
	UMC 0.13µ	23,713 gates	256 MHz
	UMC 0.18µ	17,364 gates	100 MHz
	UMC 0.18µ	20,709 gates	184 MHz

Configuration Notes:

R8051XC-B – 3 timers/counters; 2 serial interface; 4-priority/13-source interrupt controller; MDU; Watchdog Timer; OCI interface

Does not include on-chip debug: OCDS or OCI implemented with two hardware breakpoints will add about 5,000 gates.

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The R80515-B core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 and Siemens SAB80C537 chips, and the results compared with the core's simulation outputs. The core was also verified through extensive functional simulation, and has achieved high code coverage results.

The core satisfies the requirements of the Reuse Methodology Manual and VSIA Quality IP Metric.

Deliverables

The core is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation:

- ASIC cores: HDL RTL source code
  FPGA cores: Post-synthesis EDIF netlist
- An example implementation with sample system
- Sophisticated self-checking HDL Testbench including everything needed to test the core
- Simulation scripts, vectors, and expected results
- Synthesis or place and route script
- Comprehensive user documentation, including a detailed specification and a system integration guide

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