February 20, 2009

# C8051F700/1/2/3/4/5/6/7/8/9 and C8051F710/1/2/3/4/5

# Revision A Errata

## Errata Status Summary

| Errata # | Title | Impact | Status | |
|---|---|---|---|---|
| | | | Affected Revisions | Fixed Revision |
| 1 | VDD Dropout voltage | Major | Revision A | Revision B |
| 2 | ESD Tolerance | Major | Revision A | Revision B |
| 3 | Flash Write/Erase timing | Major | Revision A | Revision B |
| 4 | Analog Bias Enable Control | Minor | Revision A | Revision B |
| 5 | Last Page of FLASH space | Major | Revision A | Revision B |
| 6 | SMBus Hardware ACK behavior | Major | Revision A | Revision B |
| 7 | Oscillator Startup Divider Value | Minor | Revision A | Revision B |

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

## Errata Details

1. **Description**: The voltage drop of the internal 1.8 V LDO is 150 mV at 1.8 V input, when the expected voltage drop is 40 mV.

   **Impact**: The minimum operating voltage of the device is 1.91 V when using the on-chip LDO.

   **Workaround**: Systems using the on-chip LDO and powering the device at voltages close to the minimum voltage must compensate for this voltage drop. Please note that the VDD monitor measures voltage at the VDD pin and not the output of the internal LDO.

   **Resolution**: The LDO drop-out will be 40 mV in Revision B devices.

2. **Description:** The device is sensitive to ESD events.

   **Impact:** The devices fail the Human Body Model ESD test at voltages above 750 V. The 64-pin QFP package fails the charge device model test above 1.25 kV. The 48-pin QFN package fails the charge device model test above 1 kV. The 48-pin QFP package fails the charge device model test above 750 V.

   **Workaround:** No workaround exists for this issue.

3. **Description**: Flash writes and erases take additional time to complete.

   **Impact**: Code executing writes and erases will take longer than expected to execute. Page erase time is typically 30 ms, while byte write time is typically 55 µs.

   **Workaround**: No workaround exists for this issue.

   **Resolution**: Flash page erases will be typically 20 ms and Flash byte writes will be typically 40 µs for Revision B devices.

4. **Description:** The reference bias enable bit is not controlled by hardware as defined in the data sheet.

   **Impact:** When operating the LDO in bypass mode and enabling the crystal oscillator circuit, the analog reference bias must be explicitly enabled. Whenever the on-chip LDO is not in bypass mode, the reference bias is forced on.

   **Workaround:** Firmware must manually set or clear the reference bias enable bit (REF0CN.1) whenever using the crystal oscillator circuit with the LDO operating in bypass mode.

   **Resolution:** Hardware reference bias control will be handled automatically when enabling/disabling the external crystal oscillator in Revision B devices.

5. **Description:** The last page of Flash space cannot be accessed through MOVX and MOVC instructions.

   **Impact:** Firmware executing on the device cannot read or write data on the last page of FLASH. This issue does not affect writes and reads through the C2 debug interface. Code can be programmed into this page of Flash and firmware can execute code residing on this page.

   **Workaround:** No workaround exists for this issue.

   **Resolution:** MOVC and MOVX instructions will read and write data on the last page of FLASH in Revision B devices.

6. **Description**: The Address Hardware Acknowledge mechanism of the SMBus peripheral can cause an unexpected SMBus interrupt or cause an incorrect SMBus state transition. The behavior depends on the EXTHOLD bit in the SMB0CF register.

   a) When Hardware Acknowledge is enabled (EHACK = 1b, SMB0ADM) and SDA setup and hold times are not extended (EXTHOLD = 0, SMB0CF), the SMBus hardware will generate an SMBus interrupt, whether or not the address on the bus matches the hardware address match conditions. The expected behavior is that an interrupt is only generated when the address matches. When the device enters the interrupt service routine, the SMBus peripheral will be in the appropriate state and indicate the reception of a slave address.

   b) When Hardware Acknowledge is enabled (EHACK = 1b, SMB0ADM) and SDA setup and hold times are extended (EXTHOLD = 1, SMB0CF) the SMBus hardware will incorrectly clear the Start bit (STA) on reception of a slave address, which causes the firmware to interpret the state as the "Slave Receiver -- Data Byte received" state. This will only happen when the address match conditions determined by the SMB0ADR and SMB0MASK registers are met by the address presented on the bus.

c) When Hardware Acknowledge is enabled and the ACK bit is set to 1, an unaddressed slave may cause interference on the SMBus by driving SDA low during an ACK cycle. The ACK bit may be set to 1 if any device on the bus generates an ACK.

**Impact**:

a) Once the CPU enters the interrupt service routine, SCL will be asserted low until SI is cleared. Incompliant SMBus masters that do not support SCL clock stretching will not recognize that the clock is being stretched. If the received address does not match the conditions of SMB0ADR and SMB0MASK, the slave will generate a NACK. If the CPU issues a write to SMB0DAT, it will have no effect on the bus. No data collisions will occur.

b) Once the hardware has matched an address and entered the interrupt service routine, the firmware will not be able to use the Start bit to distinguish between the reception of an address byte versus the reception of a data byte. However, the hardware will still correctly acknowledge the address byte (SLA+R/W).

c) The SMBus master and addressed slave are not able to generate a NACK since the unaddressed slave is holding SDA low during the ACK cycle. There is a potential for the SMBus to lock up.

**Workarounds**:

a) The SMBus interrupt service routine should verify an address when it is received and clear SI as soon as possible if the address does not match.

b) It is recommended that setup and hold times should not be extended when Hardware Acknowledge is enabled. Contact mcuapps@silabs.com for alternate workarounds if these two features are required.

c) Schedule a timer interrupt to clear the ACK bit at an interval shorter than 7 bit periods when the slave is not being addressed. For example, on a 400 kHz SMBus, the ACK bit should be cleared every 17.5 uS (or at 1/7 the bus frequency, 57 kHz).

As soon as a matching slave address is detected, the timer which clears the ACK bit should be stopped and its interrupt flag cleared. The timer should be re-started once a stop condition is detected.

A code example demonstrating this workaround can be found in the SMBus examples folder with the following default location:

C:\SiLabs\MCU\Examples\C8051F70x_71x\SMBus\F70x_SMBus_Slave_Multibyte_HWACK.c

The SMBus examples folder, along with examples for many additional peripherals, is created when the Silicon Laboratories IDE is installed. The latest version of the IDE may be downloaded from the software downloads page on the Silicon Laboratories website: www.silabs.com/MCUDownloads.

**Resolution:** The above behaviors will be corrected for Revision B.

7. **Description:** The IFCN[1:0] bits in register OSCICN default to 11 (binary) after a reset, instead of the specified 00 (binary).

   **Impact:** The reset value of the IFCN[1:0] bits selects the default oscillator divider value to be 1 instead of 8. After a reset, the device core will be clocking at 24.5 MHz, instead of 3.0625 MHz.

   **Workaround:** Write the OSCICN register with the desired IFCN[1:0] bit settings for the application as soon after power-on as possible. Including this in firmware workaround will result in the same device

behavior between Revision A and later revisions, and eliminate the need for any code modifications between Revision A and Revision B.

**Resolution:** The reset value of IFCN[1:0] will be 00 (binary) in Revision B devices.

8. **Description:** The VDD Monitor Threshold (VRST) is 1.9 V instead of the specified 1.8 V.

   **Impact:** The minimum operating voltage of the device is 1.91 V. Detection of voltage below 1.9 V will cause the VDD monitor to hold the device in reset.

   **Workaround:** No workaround exists for this issue.

   **Resolution:** The VDD monitor will operate as specified in the in Revision B devices.