January 2003

8 - Bit Micro-controller

with 8KB flash & 256 Bytes RAM embedded

Product List

SM79108L25, 25 MHz 8KB internal memory MCU
SM79108C40, 40 MHz 8KB internal memory MCU

Description

The SM79108 series product is an 8 - bit single chip micro controller with 8 KB flash & 256 bytes RAM embedded. It has 4-channel, 8-bit ADC function build-in, 1-channel SPWM and 1-channel PWM build-in and A14(segment) x 4(common) LCD driver. It provides hardware features and a powerful instruction set necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 64K byte flash memory for program and/or for data.

To program the flash block, a commercial programmer is capable to do it.

Ordering Information

yywwv: production date code identifier
SM79108ihhk

yy: year, ww: weak, v: version
i: process identifier {L=3.0V ~ 3.6V, C=4.5V ~ 5.5V}
hh: working clock in MHz {25, 40}
k: package type postfix {as below table}

Postfix	Package	Pin/Pad Configuration	Dimension
P	40L PDIP	page 2	page 22
J	44L PLCC	page 2	page 23
Q	44L QFP	page 2	page 24

Features

- Working voltage: 3.0V ~ 3.6V For L Version
  4.5V ~ 5.5V For C Version
- General 8052 family compatible
- 12 clocks per machine cycle
- 8 KB internal flash memory
- 256 bytes on-chip data RAM
- Three 16 bit timers/counters
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- A14 x 4 LCD driver (P0, P2, ALE, PSEN)
- 1 Channel SPWM (P1.2)
- 1 Channel PWM (P1.5)
- Full duplex serial channel
- Bit operation instruction
- Industrail Level
- 8-bit unsigned division
- 8-bit unsigned multiply
- BCD arithmetic
- Direct addressing
- Indirect addressing
- Nested interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes: Idle mode and power down mode
- Code protection function
- One watch dog timer (WDT)
- Low EMI (inhibit ALE)

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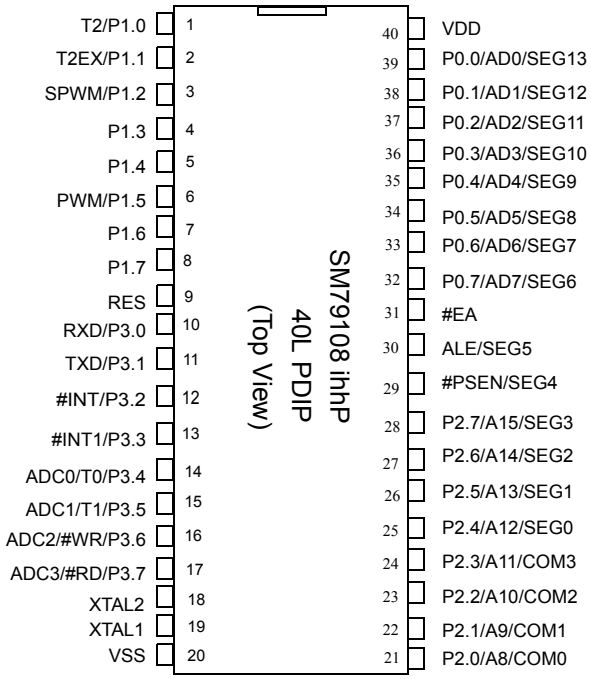
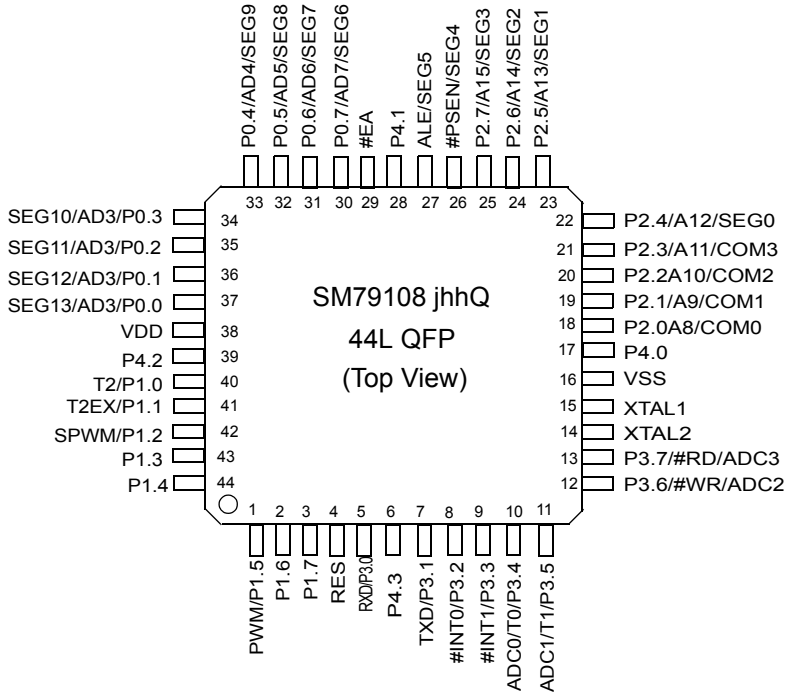
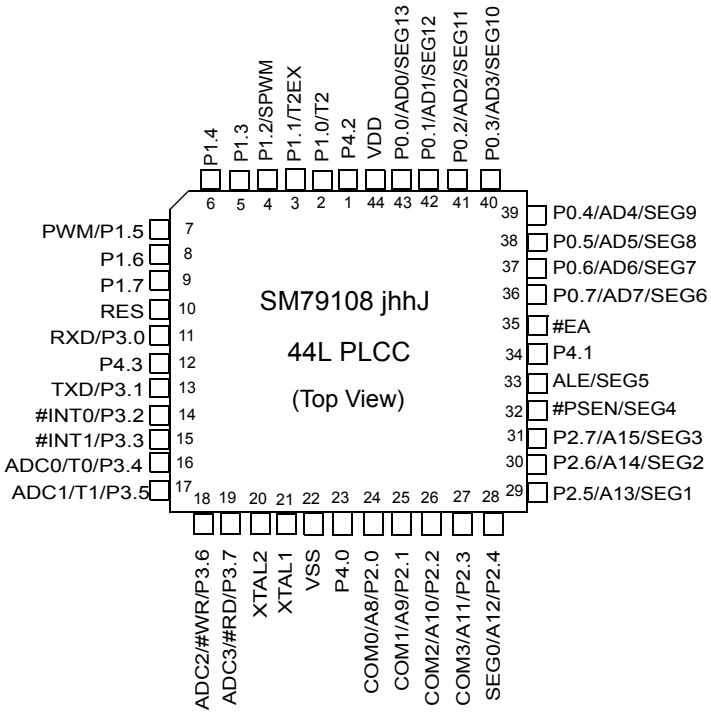
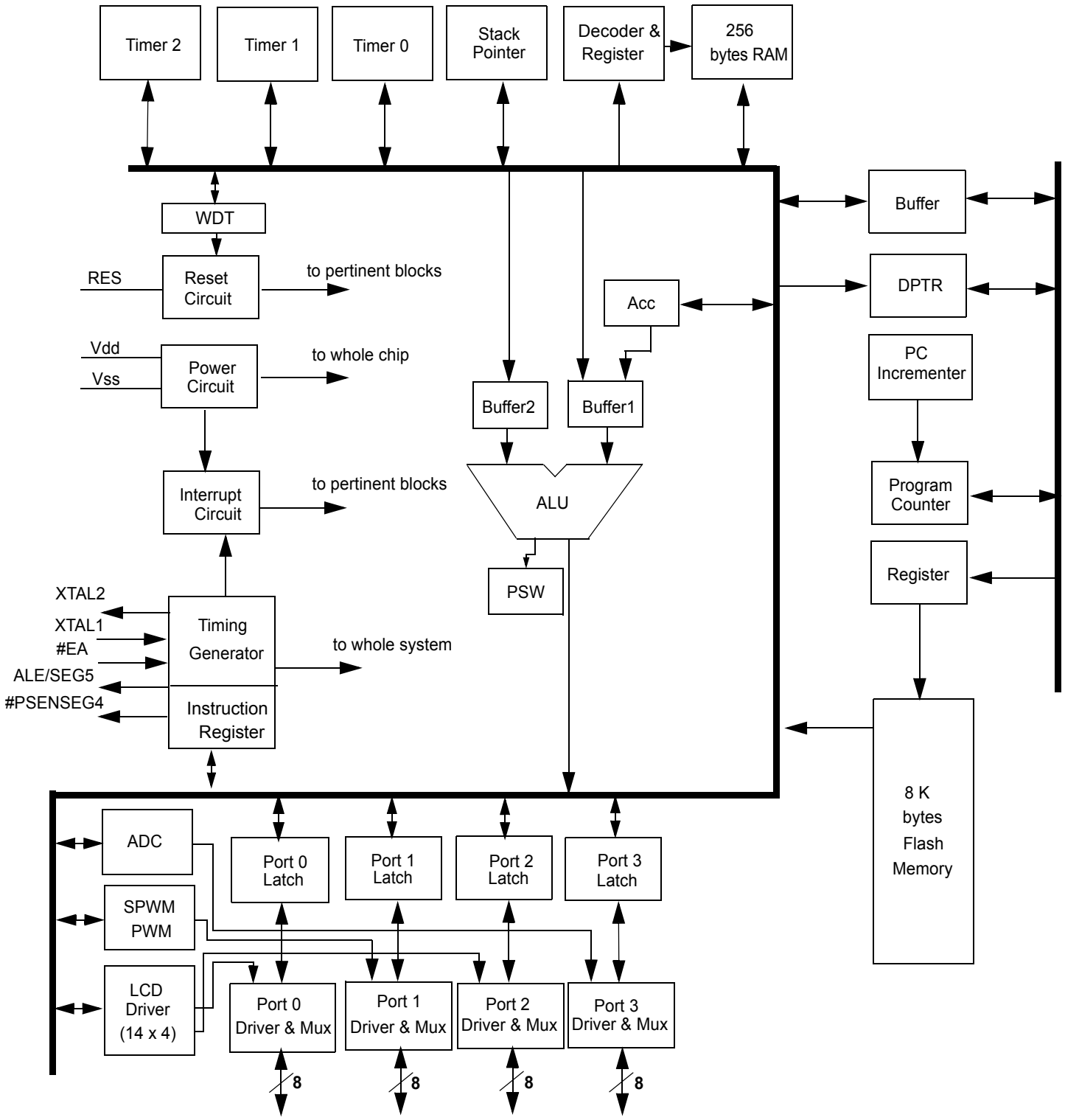
Pin Configurations







Block Diagram



Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O (GPIO)	Names
1	40	2	P1.0/T2		i/o	bit 0 of port 1 & timer 2 clock out
2	41	3	P1.1/T2EX		i/o	bit 1 of port 1 & timer 2 control
3	42	4	P1.2/SPWM		i/o	bit 2 of port 1 & SPWM channel
4	43	5	P1.3		i/o	bit 3 of port 1
5	44	6	P1.4		i/o	bit 4 of port 1
6	1	7	P1.5/PWM		i/o	bit 5 of port 1 & PWM channel
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & receive data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & transmit data
12	8	14	P3.2/#INT0	-/L	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	-/L	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0/ADC0		i/o	bit 4 of port 3 & ADC channel 0 & Timer 0
15	11	17	P3.5/T1/ADC1		i/o	bit 5 of port 3 & ADC channel 1 &Timer 1
16	12	18	P3.6/#WR/ADC2		i/o	bit 6 of port 3 & ADC channel 2 & external memory write
17	13	19	P3.7/#RD/ADC3		i/o	bit 7 of port 3 & ADC channel 3 & external memory read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8/COM0		i/o	bit 0 of port 2 & bit 8 of external memory address & LCCD common 0 output
22	19	25	P2.1/A9/COM1		i/o	bit 1 of port 2 & bit 9 of external memory address & LCCD common 1 output
23	20	26	P2.2/A10/COM2		i/o	bit 2 of port 2 & bit 10 of external memory address & LCCD common 2 output
24	21	27	P2.3/A11/COM3		i/o	bit 3 of port 2 & bit 11 of external memory address & LCCD common 3 output
25	22	28	P2.4/A12/SEG0		i/o	bit 4 of port 2 & bit 12 of external memory address & LCCD seg 0 output
26	23	29	P2.5/SEG1		i/o	bit 5 of port 2 & LCCD seg 1 output
27	24	30	P2.6/SEG2		i/o	bit 6 of port 2 & LCCD seg 2 output
28	25	31	P2.7/SEG3		i/o	bit 7 of port 2 & LCCD seg 3 output
29	26	32	#PSEN/SEG4		o	program storage enable & LCCD seg 4 output
30	27	33	ALE/SEG5		o	address latch enable & LCCD seg 5 output
31	29	35	#EA	L	i	external access
32	30	36	P0.7/AD7/SEG6		i/o	bit 7 of port 0 & data/address bit 7 of external memory & LCCD seg 6 output
33	31	37	P0.6/AD6/SEG7		i/o	bit 6 of port 0 & data/address bit 6 of external memory & LCCD seg7 output
34	32	38	P0.5/AD5/SEG8		i/o	bit 5 of port 0 & data/address bit 5 of external memory & LCCD seg 8 output
35	33	39	P0.4/AD4/SEG9		i/o	bit 4 of port 0 & data/address bit 4 of external memory & LCCD seg 9 output
36	34	40	P0.3/AD3/SEG10		i/o	bit 3 of port 0 & data/address bit 3 of external memory & LCCD seg 10 output
37	35	41	P0.2/AD2/SEG11		i/o	bit 2 of port 0 & data/address bit 2 of external memory & LCCD seg 11 output
38	36	42	P0.1/AD1/SEG12		i/o	bit 1 of port 0 & data/address bit 1 of external memory & LCCD seg 12 output
39	37	43	P0.0/AD0/SEG13		i/o	bit 0 of port 0 & data/address bit 0 of external memory & LCCD seg 13 output
40	38	44	VDD		i	Drive Voltage, Vcc
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of Port 4

SFR Memory MAP

0F8H									0FFH
0F0H	B								0F7H
0E8H									0EFH
0E0H	ACC	LCDB0	LCDB1	LCDB2	LCDB3	LCDB4	LCDB5	LCDB6	0E7H
0D8H	P4							LCDCON	0DFH
0D0H	PSW			PWMC0					0D7H
0C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			0CFH
0C0H									0C7H
0B8H	IP	IP1						**SCONF**	0BFH
0B0H	P3			PWMD0					0B7H
0A8H	IE	IE1	IFR						0AFH
0A0H	P2			SPWMC	SPWMD0				0A7H
98H	SCON	SBUF	P0CON	P1CON	P2CON	P3CON		**WDTC**	9FH
90H	P1							**WDTKEY**	97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1	ADSCR	ADCD	8FH
80H	P0	SP	DPL	DPH	(Reserved)			PCON	87H

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM79108

Addr	SFR	Reset	7	6	5	4	3	2	1	0
8EH	**ADSCR**	0000_00**	COM	CON	ADCSS1	ADCSS0	CH1	CH0	Reserved	Reserved
8FH	**ADCD**	00H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
97H	**WDTKEY**	00H	WDTKEY7	WDTKEY6	WDTKEY5	WDTKEY4	WDTKEY3	WDTKEY2	WDTKEY1	WDTKEY0
9AH	**P0CON**	00H	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SGE12	SEG13
9BH	**P1CON**	**0*_*0**			PWME0			SPWME0		
9CH	**P2CON**	00H	SEG3	SEG2	SEG1	SEG0	COME3	COME2	COME1	COME0
9DH	**P3CON**	00H	ADCE3	ADCE2	ADCE1	ADCE0				
9FH	**WDTC**	000*_*000	WDTE	R	CLEAR			PS2	PS1	PS0
0A3H	**SPWMC0**	****_**00							SPFS1	SPFS0
0A4H	**SPWMD0**	00H	SPWMD04	SPWMD03	SPWMD02	SPWMD01	SPWMD00	BRM02	BRM01	BRM00
0A9H	**IE1**	****_0***					EADC			
0AAH	**IFR**	****_0***					ADCIF			
0B3H	**PWMD0**	00H	PWMD07	PWMD06	PWMD05	PWMD04	PWMD03	PWMD02	PWMD01	PWMD00
0B9H	**IP1**	****_0***					PADC			
0BFH	**SCONF**	0***_***0	WDR					Reserved		ALEI
0D3H	**PWMC0**	****_*000						PBS	PFS1	PFS0
0D8H	**P4**	****_1111					P4.3	P4.2	P4.1	P4.1
0DFH	**LCDCON**	000*_*000	Lout_en	Lcd_en	SEG			LS2	LS1	LS0
0E1H	**LCDB0**	00H	SEG0	SEG0	SEG0	SEG0	SEG1	SEG1	SEG1	SEG1

Addr	SFR	Reset	7	6	5	4	3	2	1	0
0E2H	**LCDB1**	00H	SEG2	SEG2	SEG2	SEG2	SEG3	SEG3	SEG3	SEG3
0E3H	**LCDB2**	00H	SEG4	SEG4	SEG4	SEG4	SEG5	SEG5	SEG5	SEG5
0E4H	**LCDB3**	00H	SEG6	SEG6	SEG6	SEG6	SEG7	SEG7	SEG7	SEG7
0E5H	**LCDB4**	00H	SEG8	SEG8	SEG8	SEG8	SEG9	SEG9	SEG9	SEG9
0E6H	**LCDB5**	00H	SEG10	SEG10	SEG10	SEG10	SEG11	SEG11	SEG11	SEG11
0E7H	**LCDB6**	00H	SEG12	SEG12	SEG12	SEG12	SEG13	SEG13	SEG13	SEG13

1. Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDR bit of SCONF register whenever unpracticed reset happened

The purpose of the secure procedure is to prevent the WDTC value from being changed when system runaway.

There is a 250KHz RC oscillator embedded in chip. Set WDTE = “1” will enable the RC oscillator and the frequency is independent to the system frequency.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM79108 been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

1.1 Watch Dog Timer Registers:

Watch Dog Key Register - (WDTKEY, 97H)

	bit-7							bit-0
	WDT KEY7	WDT KEY6	WDT KEY5	WDT KEY4	WDT KEY3	WDT KEY2	WDT KEY1	WDT KEY0
Read / Write:	W	W	W	W	W	W	W	W
Reset value:	0	0	0	0	0	0	0	0

By default, the WDTC is read only. User need to write values 1EH, 0E1H sequentially to the WDTKEY(97H) register to enable the WDTC write attribute, That is

```
MOV WDTKEY, # 1EH
MOV WDTKEY, # E1H
```

When WDTC is set, user need to write another values E1H, 1EH sequentially to the WDTKEY(97H) register to disable the WDTC write attribute, That is

```
MOV WDTKEY, # E1H
MOV WDTKEY, # 1EH
```

Watch Dog Timer Registers - WDT Control Register (WDTC, 9FH)

	bit-7							bit-0
	WDTE	R	CLEAR	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	R/W	-	-	R/W	R/W	R/W
Reset value:	0	0	0	*	*	0	0	0

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS[2:0] : Overflow period select bits

PS [2:0]	Overflow Period (ms)
000	2.048
001	4.096
010	8.192
011	16.384
100	32.768
101	65.536
110	131.072
111	262.144

System Control Register (SCONF, 0BFH)

	bit-7							bit-0
	WDR	Unused	Unused	Unused	Unused	Reserved	Unused	ALEI
Read / Write:	R/W	-	-	-	-	-	-	R/W
Reset value:	0	*	*	*	*	*	*	0

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1
ALEI : ALE output inhibit bit, to reduce EMI

Setting bit 0 (ALEI) of SCONF can inhibit the clock signal in Fosc/6Hz output to the ALE pin.

The bit 7 (WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever unpredicted reset happened.

2. Reduce EMI Function

The SM79108 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin.

3. Port 4 for PLCC or QFP package:

The bit addressable port 4 is available with PLCC or QFP package. The port 4 has only 4 pins and its port address is located at 0D8H. The function of port 4 is the same as the function of port 1, port 2 and port 3.

Port4 (P4, 0D8H)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	P4.3	P4.2	P4.1	P4.0
Read / Write:	-	-	-	-	R/W	R/W	R/W	R/W
Reset value:	*	*	*	*	1	1	1	1

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

4. SPWM Function Description:

The 8-bit SPWM channel is composed of an 8-bit register which contains a 5-bit SPWM in MSB portion and a 3-bit binary rate multiplier (BRM) in LSB portion. The value programmed in the 5-bit SPWM portion will determine the pulse length of the output. The 3-bit BRM portion will generate and insert certain narrow pulses among an 8-SPWM-cycle frame. The number of pulses generated is equal to the number programmed in the 3-bit BRM portion. The usage of the BRM is to generate equivalent 8-bit resolution SPWM type DAC with reasonably high repetition rate through 5-bit SPWM clock speed. The SPFS[1:0] settings of SPWMC (0A3H) register are divided of Fosc to be SPWM clock, Fosc/ 2^(SPFS[1:0]+1). The SPWM output cycle frame repetition rate (frequency) equals (SPWM clock)/32 which is [Fosc/ 2^(SPFS[1:0]+1)]/32.

4.1 SPWM Registers - P1CON, SPWMC0, SPWMD0

SPWM Registers - Port1 Configuration Register (P1CON, 9BH)

	bit-7							bit-0
	Unused	Unused	PWME0	Unused	Unused	SPWME0	Unused	Unused
Read / Write:	-	-	R/W	-	-	R/W	-	-
Reset value:	*	*	0	*	*	0	*	*

SPWME0 : When the bit set to one, the corresponding SPWM pin is active as SPWM function. When the bit reset to zero, the corresponding SPWM pin is active as I/O pin. Four bits are cleared upon reset.

PWME0 : When the bit set to one, the corresponding PWM pin is active as PWM function. When the bit reset to zero, the corresponding PWM pin is active as I/O pin. Four bits are cleared upon reset.

SPWM Registers - SPWM Control Register (SPWMC, 0A3H)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	Unused	Unused	SPFS1	SPFS0
Read / Write:	-	-	-	-	-	-	R/W	R/W
Reset value:	*	*	*	*	*	*	0	0

SPFS[1:0]: These two bits is 2's power parameter to form a frequency divider for input clock.

SPFS1	SPFS0	Divider	SPWM clock, Fosc=20MHz	SPWM clock, Fosc=24MHz
0	0	2	10MHz	12MHz
0	1	4	5MHz	6MHz
1	0	8	2.5MHz	3MHz
1	1	16	1.25MHz	1.5MHz

SPWM Registers - SPWM Data Register (SPWMD0, 0A4H)

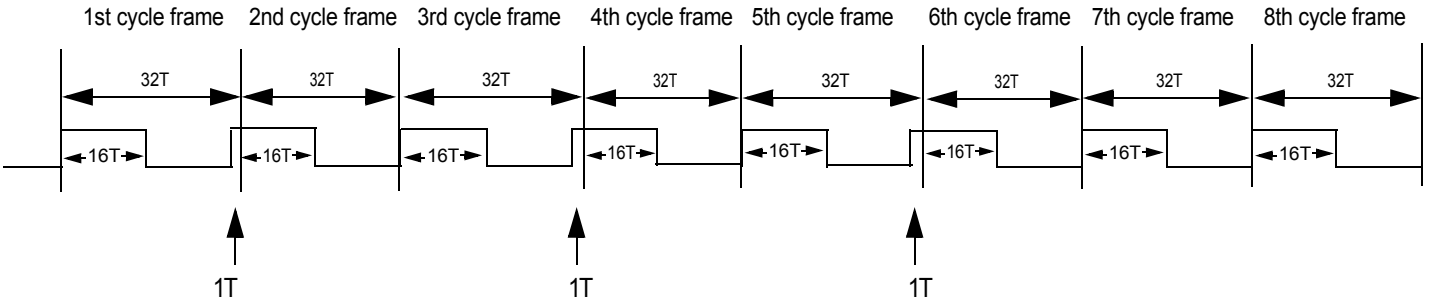
	bit-7							bit-0
	SPWMD04	SPWMD03	SPWMD02	SPWMD01	SPWMD00	BRM02	BRM01	BRM00
Read/Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

SPWMD0[4:0]: content of SPWM Data Register. It determines duty cycle of SPWM output waveform.
BRM[2:0]: will insert certain narrow pulses among an 8-SPWM-cycle frame

N = BRM[2:0]	Number of SPWM cycles inserted in an 8-cycle frame
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Example of SPWM timing diagram:

```
MOV  SPWMD0 , #83H      ; SPWMD0[4:0]=10h (=16T high, 16T low), BRM0[2:0] = 3
MOV  P1CON , #04H       ; Enable P1.2 as SPWM output pin
```



(narrow pulse inserted by BRM0[2:0] setting, here BRM0[2:0]=3)

SPWM clock = 1 / T = Fosc / 2^(SPFS[1:0]+1)
The SPWM output cycle frame frequency = SPWM clock / 32 = [Fosc/2^(SPFS[1:0]+1)]/32

If user use Fosc=20MHz, SPFS[1:0] of SPWMC=#03H, then
SPWM clock = 20MHz/2^4 = 20MHz/16 = 1.25MHz
SPWM output cycle frame frequency = (20MHz/2^4)/32=39.1KHz

5. PWM Function Description:

Each PWM channel contains a 8-bit wide PWM data register (PWMDR) to decide number of continuous pulses within a PWM frame cycle. The value programmed in the register will determine the pulse length of the output. The PWM channel can be configured as 5-bit or 8-bit resolution. If a channel is configured as 5-bit resolution, only LSB 5 bits are available. The value of each PWM Data Register (PWMDR) is continuously compared with the content of an internal counter to determine the state of each PWM channel output pin.

5.1 PWM Registers - PWMC0, PWMD0

PWM Registers - PWM Control Register (PWMC0, 0D3H)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	Unused	PBS	PFS1	PFS0
Read / Write:	-	-	-	-	-	R/W	R/W	R/W
Reset value:	*	*	*	*	*	0	0	0

PFS[1:0]: These two bits is 2's power parameter to form a frequency divider for input clock.
PBS: This bit decides channel bit resolution. If PBS is set, the channel is 5-bit resolution.

PFS1	PFS0	Divider	PWM clock, Fosc=12MHz	PWM clock, Fosc=24MHz
0	0	16	750KHz	1.5MHz
0	1	32	375KHz	750KHz
1	0	64	187.5KHz	375KHz
1	1	128	93.75KHz	187.5KHz

Example : If user use Fosc = 20MHz, PFS[1:0] of PWMC = #03H, PBS = 0, then
PWM Clock = 20MHz / 128 = 156.25KHz
PWM Output cycle frame frequency = 156.25KHz / 256 = 610 Hz
Note : For bzzer application

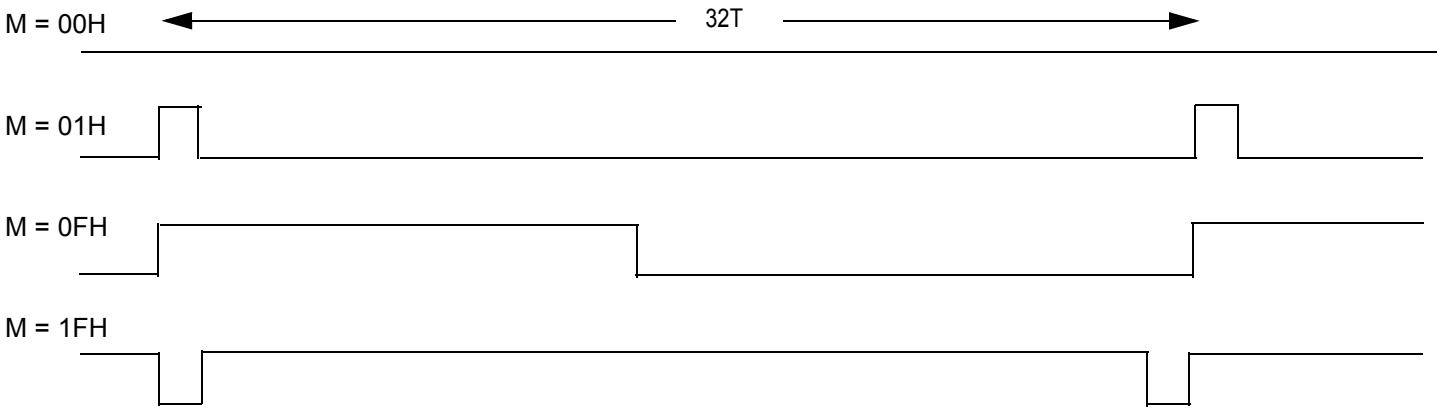
PWM Registers - PWM Data Register (PWMD0, 0B3H)

	bit-7							bit-0
	PWMD07	PWMD06	PWMD05	PWMD04	PWMD03	PWMD02	PWMD01	PWMD00
Read /Write:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value:	0	0	0	0	0	0	0	0

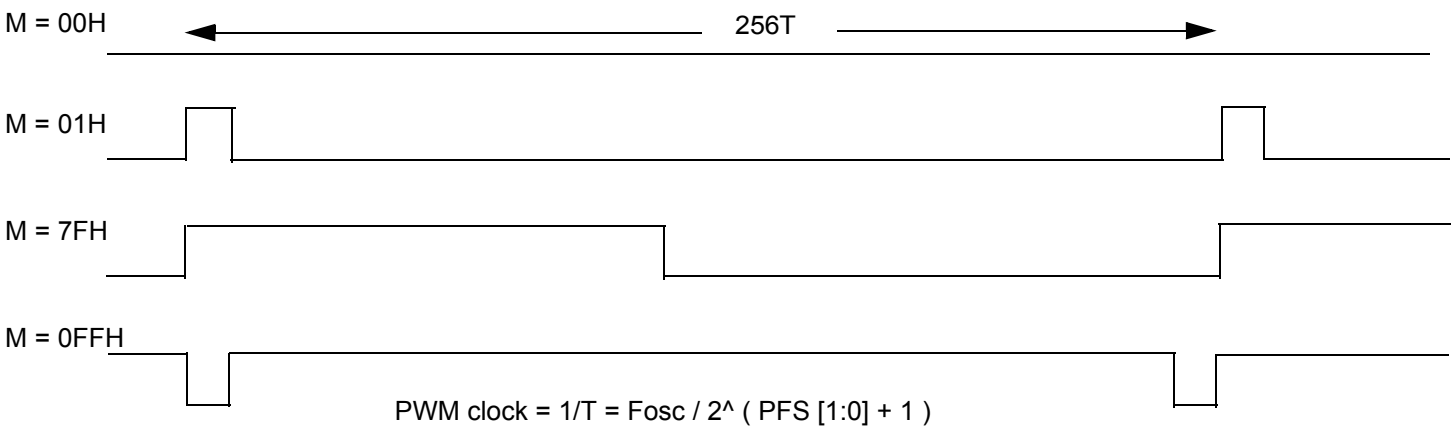
PWM[7:0]: content of PWM Data Register. If PBS is set, only PWM[4:0] are available.

Example of PWM timing diagram:

For 5-bit resolution channel, M = content of PWMD0:



For 8-bit resolution channel:



PWM clock = 1/T = Fosc / 2^ (PFS [1:0] + 1)

6. Analog-to-Digital Converter (ADC)

The SM79108 equips with 4-channels, 8-bit ADC which is available at P3.4~P3.7. S/W can select one of the 4 ADC channels by setting SFR ADC Status and Control Register (ADSCR, 8EH) bit CH0~CH1. The ADC can do single conversion or continuously conversion. When the conversion is completed, ADC puts the result in the ADC Data Register (ADCD, 8FH) and sets COM bit of ADSCR (ADSCR.7). After channel selection bit CH[1:0] of ADSCR and P3CON been set, the selected pin of P3.4~P3.7 will function as ADC input pin instead of general purpose I/O pin which is due to priority of ADC function is higher than I/O function. The rest of the P3.4~P3.7 pin will still function as general purpose I/O pin. Writes to the port register will have no affect on the port pin that is selected by the ADC. Read of a port pin which is in use by the ADC will return the value in the port which is been read.

6.1 Straight line conversion

The ADC conversion relationship of input analog signal to digital output value is a linear straight line conversion relationship. It will convert input signal in +Vdd V or above to 0FFH (full scale) and convert input signal +0V or below to 00H. The +Vdd is the voltage applied to the IC.

6.2 ADC input clock frequency range

ADC input clock frequency range = 500KHz ~ 2.5MHz. User need to be aware of this frequency range limitation when using ADC function. The frequency range limitation was induced by the sample-and-hold and DAC converter circuits inside of the ADC submodule. If the ADC input clock frequency resides outside of the range then ADC function may not work.

ADC input clock frequency = oscillator frequency / divider. Divider elected by ADCSS[1:0] setting of ADSCR

One conversion time = 20 ADC clock cycles / ADC input clock frequency

Maximum sample rate of ADC = ADC input clock frequency / 20

6.3 ADC registers - ADSCR, ADR

ADC Registers - ADSCR, 8EH)

	bit-7							bit-0
	COM	CON	ADCSS1	ADCSS0	CH1	CH0	R	R
Read /Write:	R	R/W	R/W	R/W	R/W	R/W	-	-
Reset value:	0	0	0	0	0	0	*	*

COM: ADC conversion complete bit. This bit is a read only bit which is set each time conversion is completed. It is cleared whenever ADSCR is written or ADCD is read. Reset clears this bit.
COM = 1 means conversion completed
COM = 0 means conversion not completed

CON: ADC continuous conversion bit. When set, the ADC will convert samples continuously and update the ADCD register at the end of each conversion. When reset, only one conversion is allowed. Reset clears this bit.
CON = 1 means continuous mode
CON = 0 means signal mode

ADCSS[1:0]: ADCSS channel select bit.

ADCSS1	ADCSS0	ADC_CLK
0	0	Fosc / 8 (below 20MHz)
0	1	Fosc / 16
1	0	Fosc / 32
1	1	Fosc / 64

CH[1:0] : ADC channel select bit. These bits are used to select one of the ADC channels.

CH1	CH0	Input select
0	0	CH0
0	1	CH1
1	0	CH2
1	1	CH3

Note: ADC_CLK frequency range 500KHz ~ 2.5MHz

ADC registers - ADC Data Register (ADCD, 8FH)

	bit-7							bit-0
	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Read /Write:	R	R	R	R	R	R	R	R
Reset value:	0	0	0	0	0	0	0	0

ADC puts the result in the ADC Data Register (ADCD, 8FH) after each conversion. The ADCD register is read only register. The content of the ADCD will be 00H after reset.

Ex : Osc = 20MHz ADCSS[1:0] = 00

ADC input clock = 20/8 = 2.5MHz (Max)

One conversion time = 20 / 2.5MHz = 8us

ADC Max sample reta = 2.5MHz / 20 = 125KHz

Port 3 Configuration Register (P3CON, 9DH)

	bit-7							bit-0
	ADCE3	ADCE2	ADCE1	ADCE0	Unused	Unused	Unused	Unused
Read /Write:	R/W	R/W	R/W	R/W	-	-	-	-
Reset value:	0	0	0	0	*	*	*	*

Set ADCE3 = 1 enables the ADC function on pin P3.7/A15/ADC3,

ADCE3 = 0 disables the ADC function on pin P3.7/A15/ADC3,

Set ADCE2 = 1 enables the ADC function on pin P3.6/A14/ADC2,

ADCE2 = 0 disables the ADC function on pin P3.6/A14/ADC2,

Set ADCE1 = 1 enables the ADC function on pin P3.5/A13/ADC1,
ADCE1 = 0 disables the ADC function on pin P3.5/A13/ADC1,
Set ADCE0 = 1 enables the ADC function on pin P3.4/A12/ADC0,
ADCE0 = 0 disables the ADC function on pin P3.4/A12/ADC0,

User may compare bits ADCE[3:0] of P3CON with bits CH[1:0] of ADSCR. User may consider P3CON as register for distinguish general purpose I/O function from other specific functions. After bit ADCE[3:0] been set, the corresponding I/O pin will be assigned as high impedance input pins for signal input. On the other hand, the setting of CH[1:0] will select ADC channels accordingly.

6.4 ADC Interrupt

The ADC module will generate one interrupt once one analog-to-digital conversion is completed. The ADC interrupt vector locates at 4BH. There are three SFRs for configuring ADC interrupt: IP1, IE1 and IFR. To use ADC interrupt is the same as to use other generic 8052 interrupts. That means using EADC of IE1 for enable/disable ADC interrupt, using PADC for assign ADC interrupt priority. Whenever ADC interrupt occurs, ADCIF will be set to 1. After ADC interrupt subroutine (vector) been executed, ADCIF will be cleared to 0.

Interrupt Priority I Register (IP1, 0B9H)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	PADC	Unused	Unused	Unused
Read /Write:	-	-	-	-	R/W	-	-	-
Reset value:	*	*	*	*	0	*	*	*

Interrupt priority bit PADC = 1 assigns high interrupt priority of ADC interrupt
Interrupt priority bit PADC = 0 assigns low interrupt priority of ADC interrupt

Interrupt Enable I Register (IE1, 0A9H)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	EADC	Unused	Unused	Unused
Read /Write:	-	-	-	-	R/W	-	-	-
Reset value:	*	*	*	*	0	*	*	*

Interrupt enable bit EADC = 1 enables the ADC interrupt
Interrupt priority bit EADC = 0 disables the ADC interrupt

Interrupt Flag Register (IFR, 0AAH)

	bit-7							bit-0
	Unused	Unused	Unused	Unused	ADCIF	Unused	Unused	Unused
Read /Write:	-	-	-	-	R/W	-	-	-
Reset value:	*	*	*	*	0	*	*	*

Interrupt flag bit ADCIF will be set to 1 when ADC interrupt occurs. Interrupt flag bit ADCIF will be clear to 0 if ADC Interrupt subroutine executed.

7. LCD Driver

SM79108 incorporates an on-chip LCD driver which generates segment and common signals output according to the display data saved in LCD buffer registers (0E1H~0E7H) and incorporates segment and common drivers which can drive the LCD panel directly.

The on chip LCD Driver has the following features:

- 1/4 duty (time multiplexing by 4) and 1/3 bias LCD segment driver
- 0.88 mA operation current (1.2 uA in power down mode)
- 56 bits of display data buffer
- 14 segment driver and 4 common driver outputs
- A frames frequency can be selected

7.1 LCD Control register (LCDCON, 0DFH)

	bit-7							bit-0
	LCD_ON	LCD_EN	SEG	Unused	Unused	LS2	LS1	LS0
Read /Write:	R/W	R/W	R/W	-	-	R/W	R/W	R/W
Reset value:	0	0	0	*	*	0	0	0

LCDCON7~LCDCON0: LCD control register is used to control LCD driver operation
LCD_ON: LCD display bit
= 1:LCD display ON
= 0:LCD display OFF
LCD_EN: LCD enable bit
SEG: = 1:enables the LCD function on pin #PSEN/SEG4 and ALE/SEG5
= 0:no operation
LS[2:0]: Frequency prescaler select, determine the clock frequency of LCD driver, Fclk_lcd

LS2	LS1	LS0	PRESCALER SELECT
0	0	0	1
0	0	1	2
	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The clock frequency of LCD driver is obtained using the following formula:

Fclk_lcd = { [Fosc / 2] / 32 x PRESCALER }

The frame of LCD driver is determined as follows:

Frame = Fclk_lcd / 256

The typical range of Fframe is:

1026HZ ~ 8HZ at 16MHz (Fosc = 8MHz)

7.2 LCD Buffer Registers (LCDB0 ~ LCDB6, 0E1H ~ 0E7H)

Addressing Map of the LCD buffer registers is shown as following:

		com3	com2	com1	com0	com3	com2	com1	com0
Mnemonic	address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDB0	E1H	SEG0	SEG0	SEG0	SEG0	SEG1	SEG1	SEG1	SEG1
LCDB1	E2H	SEG2	SEG2	SEG2	SEG2	SEG3	SEG3	SEG3	SEG3
LCDB2	E3H	SEG4	SEG4	SEG4	SEG4	SEG5	SEG5	SEG5	SEG5
LCDB3	E4H	SEG6	SEG6	SEG6	SEG6	SEG7	SEG7	SEG7	SEG7
LCDB4	E5H	SEG8	SEG8	SEG8	SEG8	SEG9	SEG9	SEG9	SEG9
LCDB5	E6H	SEG10	SEG10	SEG10	SEG10	SEG11	SEG11	SEG11	SEG11
LCDB6	E7H	SEG12	SEG12	SEG12	SEG12	SEG13	SEG13	SEG13	SEG13

7.3 Timing chart of LCD driver output

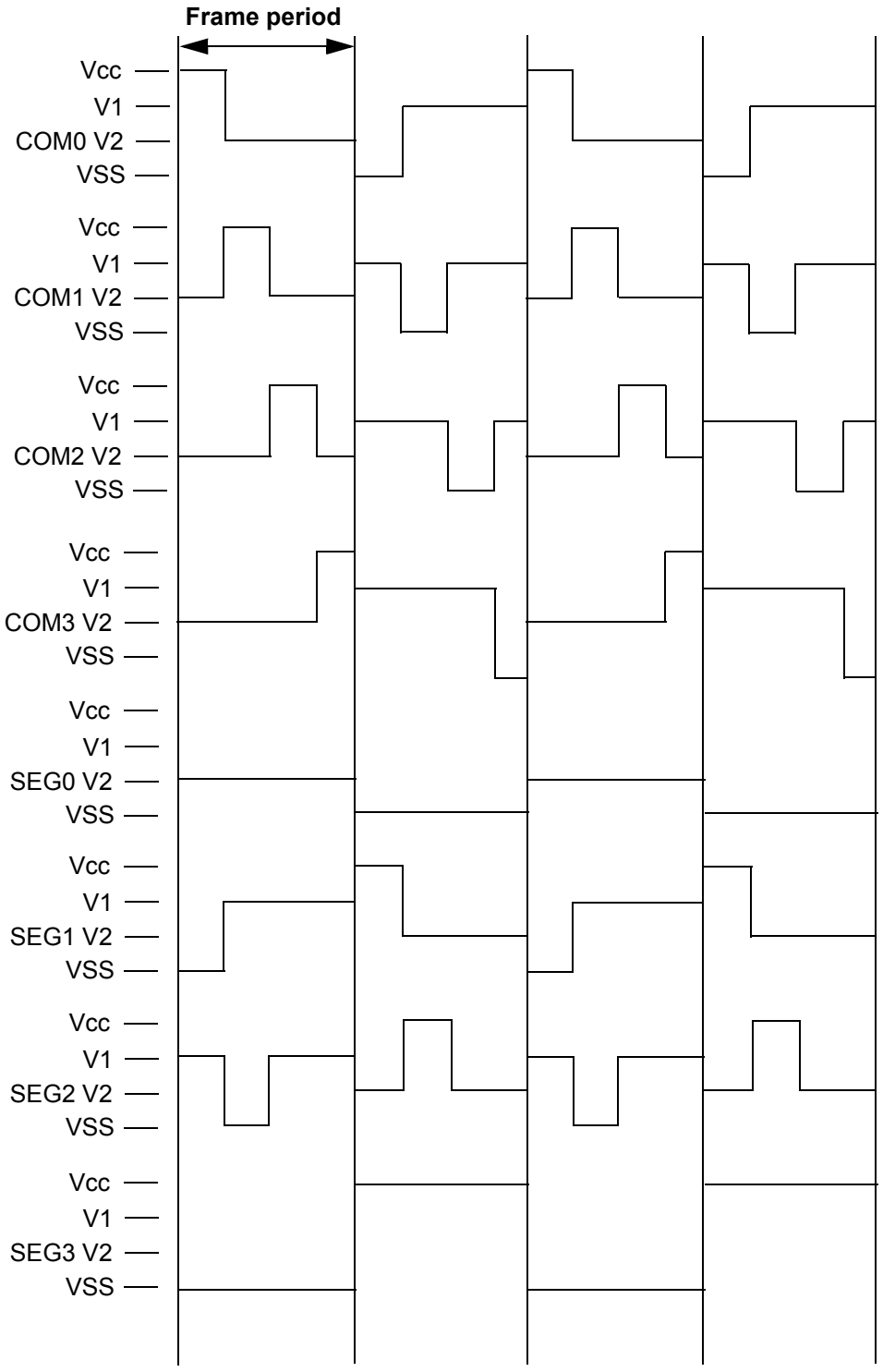
The 14 segment drivers and the 4 common drivers are 4-level outputs that switch between Vcc and the V1, V2 and Vss LCD driver voltages levels.

The output states are determined by the display data values which stored in the LCD buffer registers (0E1H ~0E7H).
The LCD driver's outputs are used to drive a 1/3-bias, 1/4-duty LCD panel.

7.4 The Output Control of Segments and Commons

Port 2 Configuration Register (P2CON) control COM0 ~ COM3 and SEG0 ~ SEG3 output; Port 0 Configuration Register (P0CON) controls SEG6 ~ SEG13 outputs.
The bit 5 of LCD Control Register control the SEG4 and SEG5 outputs.

Figure 6.1 Output states determination



COM0	COM1	COM2	COM3	
0	0	0	0	All segments are OFF
1	0	0	0	Segments connected to COM0 are ON
0	1	0	0	Segments connected to COM1 are ON
1	1	1	1	All segments are ON

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	°C	Ambient temperature under bias
TS	Storage temperature	-55	25	155	°C	
VCC5	Supply voltage	4.5	5.0	5.5	V	
VCC3	Supply voltage	3	3.3	3.6	V	
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V, 3.3V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

DC Characteristics

(TA = -40 °C to 85 °C, Vcc = 5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	1.0	V	Vcc = 5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	"
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	"
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	"
VOL1	Output Low Voltage	port 12,3,4		0.4	V	IOL = 1.6mA
VOL2	Output Low Voltage	port 0,2,port 3.0~port 3.3, ALE, #PSEN		0.4	V	IOL = 3.2mA
VOH1	Output High Voltage	port 1, 2, 3, ALE, #PSEN	2.4		V	IOH = -60uA
			90%Vcc		V	IOH = -10uA
VOH2	Output High Voltage	port 0	2.4		V	IOH = -800uA
			90%Vcc		V	IOH = -80uA
IIL	Logical 0 Input Current	port 1,2,4, port 3.0~port 3.3		-50	uA	Vin = 0.45V
ITL	Logical Transition Current	port 1,2,4, port 3.0~ port3.3		-650	uA	Vin = 2.0V
ILI	Input Leakage Current	port 0, #EA		10	uA	Vin = 0.45V
				10	uA	Vin = 5V
R RST	Reset Pulldown Resistor		18	90	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				10	mA	Idle mode, 16MHz
				100	uA	down mode, 16MHz

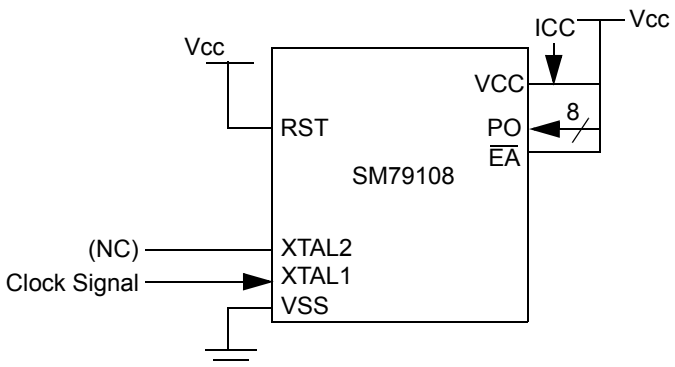
Note1: Under steady state (non-transient) conditions, IOL must be externally
Limited as follows: Maximum IOL per port pin : 10mA
Maximum IOL per 8-bit port : port 0 :26mA
port 1,2,3 :15mA
Maximum total IOL for all output pins : 71mA
If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
Note2 : Minimum VCC for Power-down is 2V.

AC Characteristics

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all Other Output=80pF)

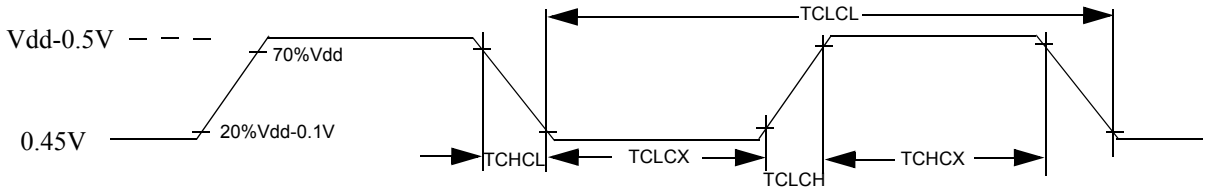
Symbol	Parameter	Valid Cycle	fosc=16MHz			Variable fosc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

ICC Active mode test circuit

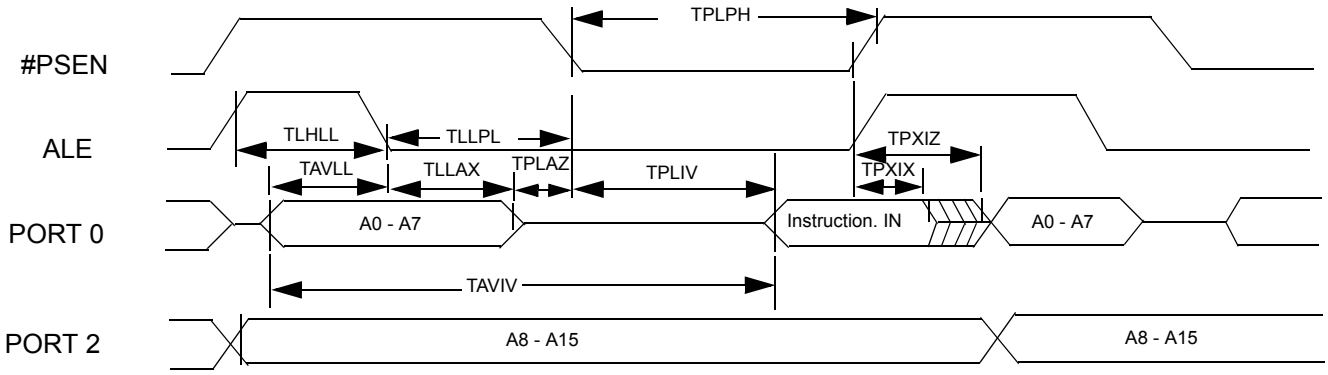


Specifications subject to change without notice,contact your sales representatives for the most recent information.

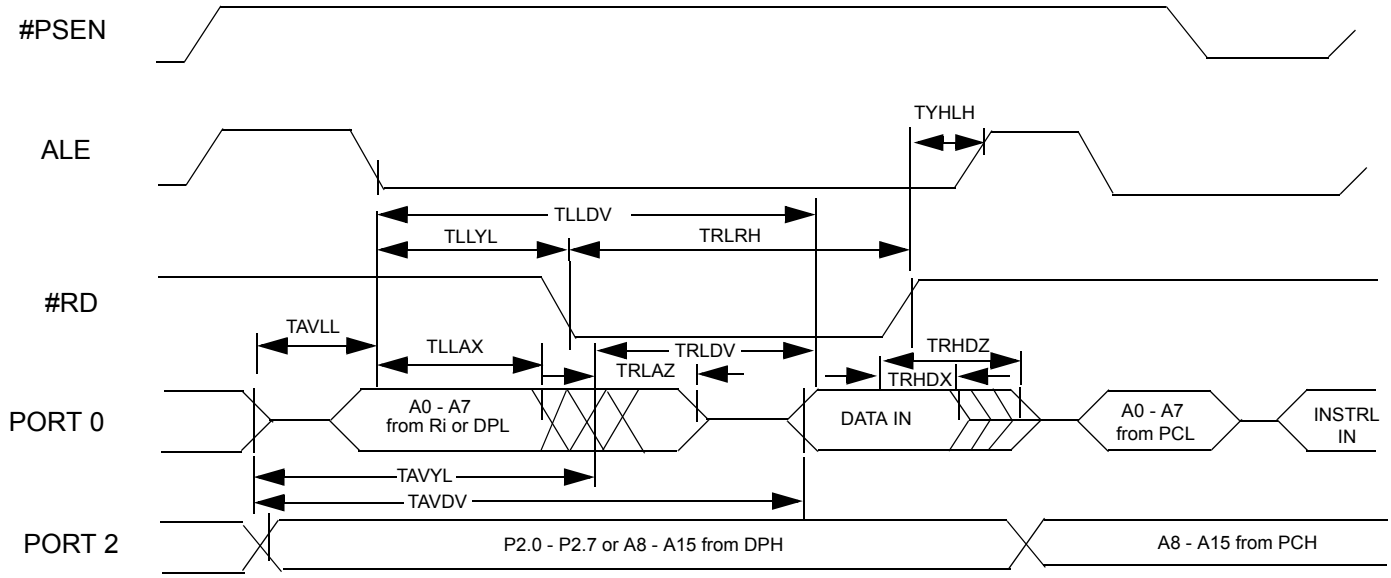
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



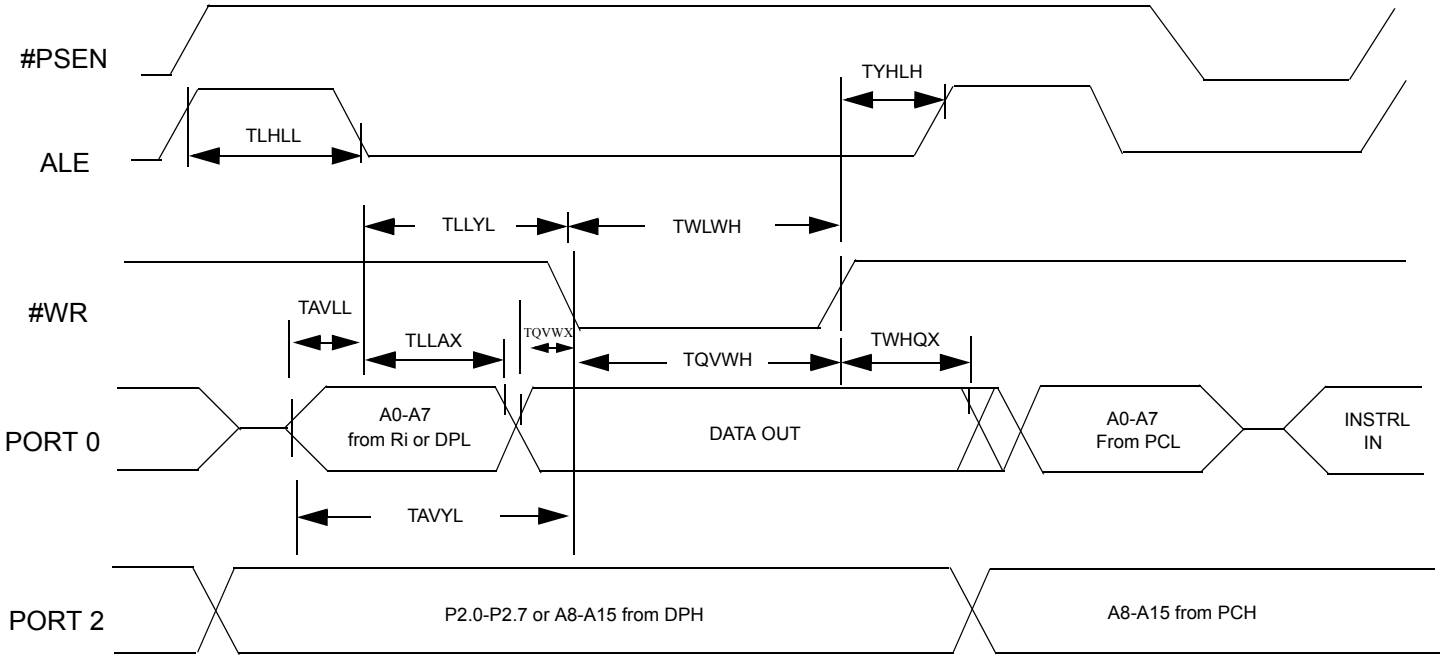
Tm.I External Program Memory Read Cycle



Tm.II External Data Memory Read Cycle



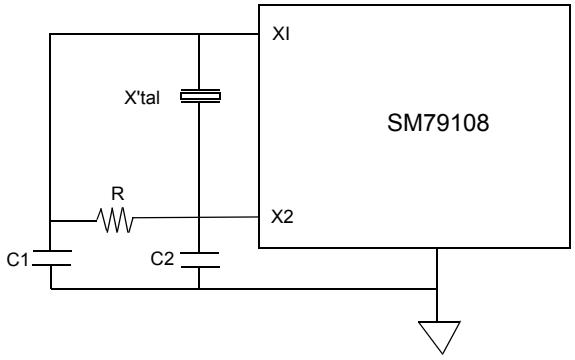
Tm.III External Data Memory Write Cycle



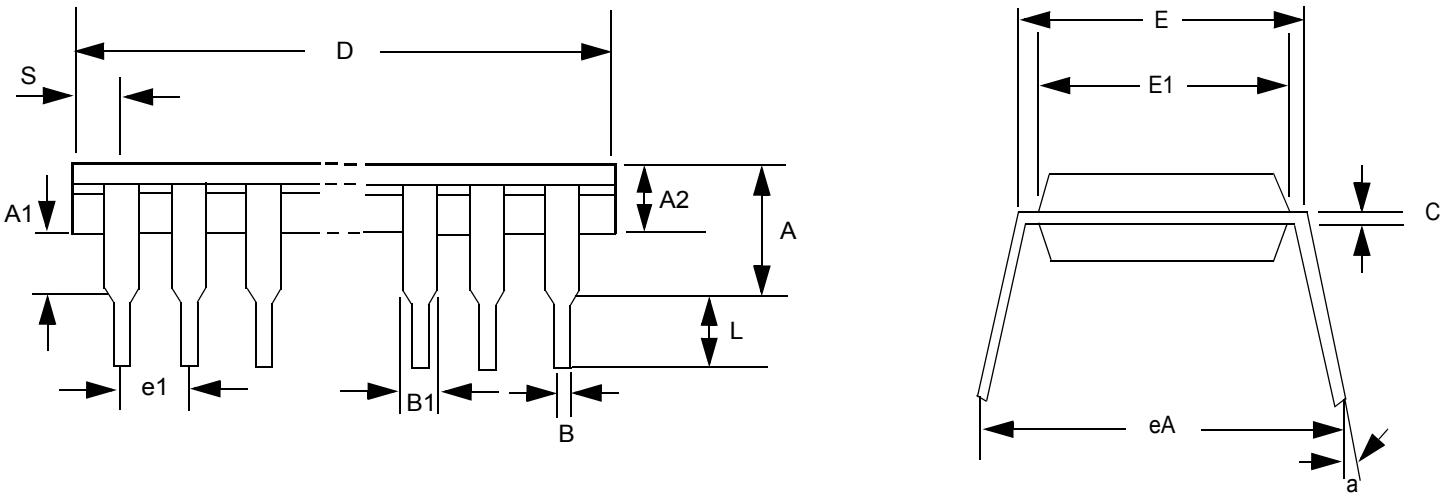
Application Reference

Valid for SM79108				
X'tal	3MHz	6MHz	12MHz	16MHz
C1	30pF	30pF	30pF	30pF
C2	30pF	30pF	30pF	30pF
R	open	open	open	open
X'tal	20MHz	25MHz	33MHz	40MHz
C1	22pF	15pF	5pF	2pF
C2	22pF	15pF	5pF	2pF
R	open	62KΩ	6.8KΩ	4.7KΩ

NOTE: Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.



40L 600mil PDIP Information

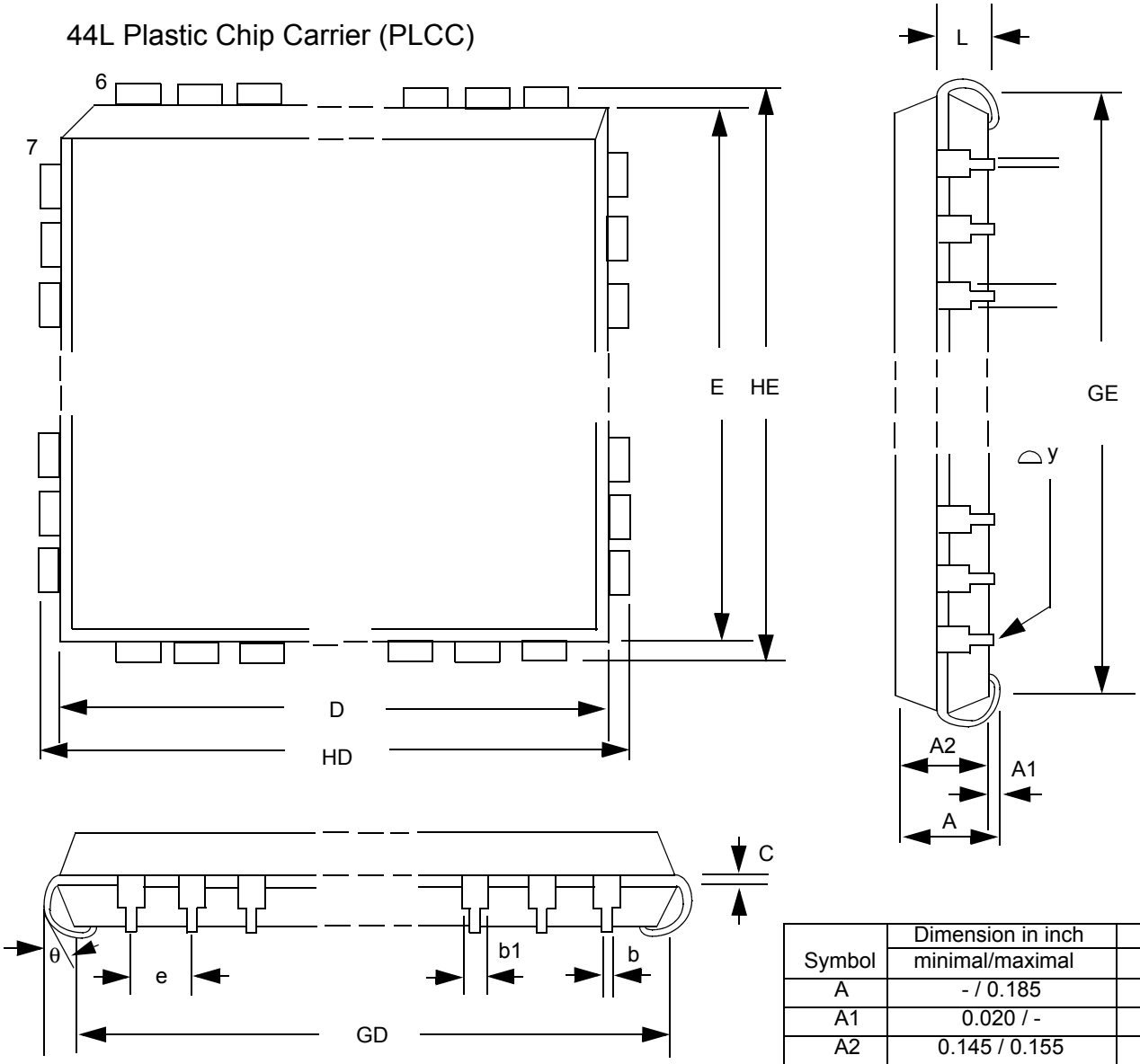


Note:

1. Dimension D Max & include mold flash or tie bar burrs.
2. Dimension E1 does not include inter lead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/ intrusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0°/ 15°	0°/ 15°
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

44L Plastic Chip Carrier (PLCC)

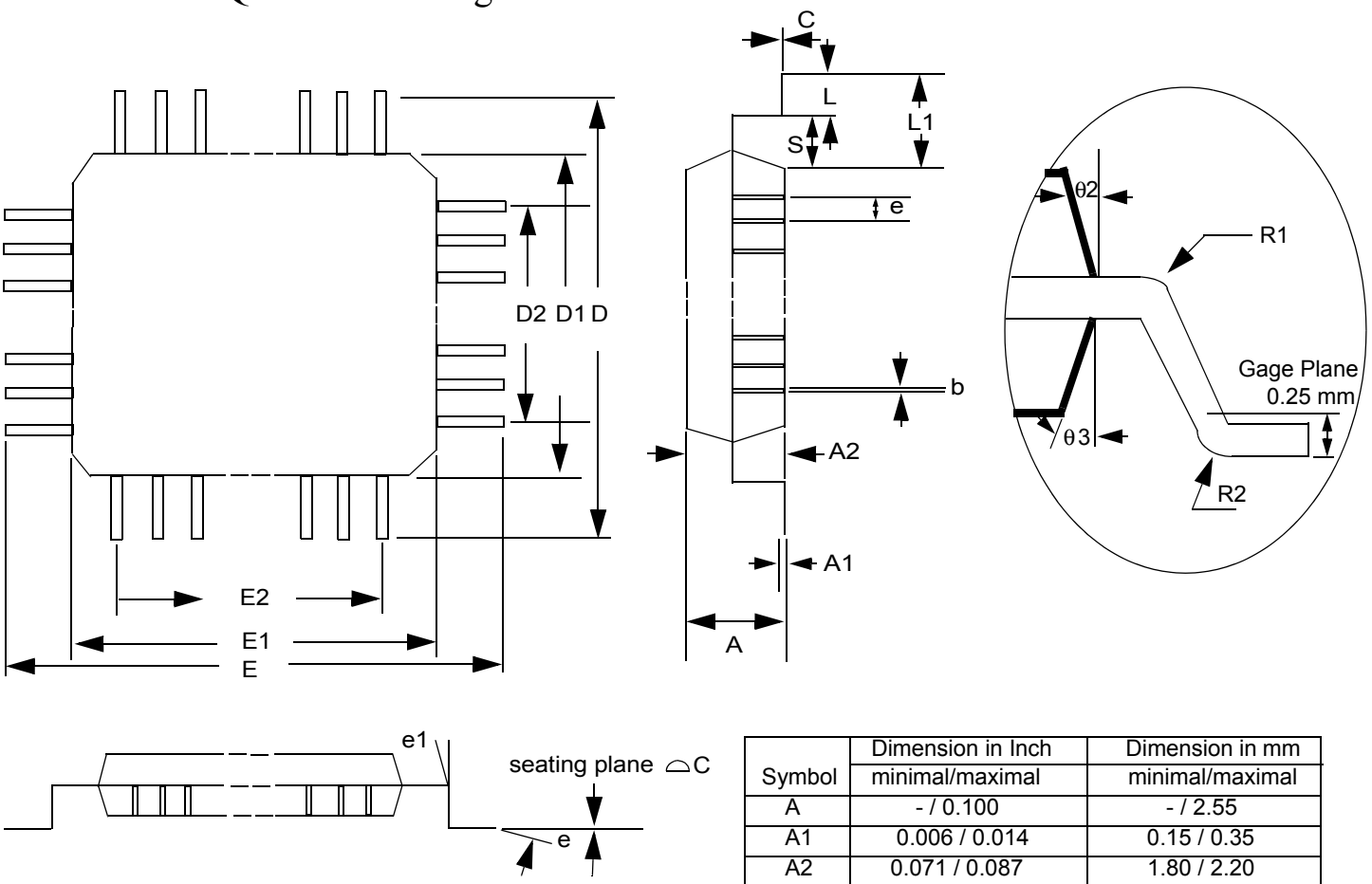


Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
⌓ y	/	/

Note:

1. Dimension D & E does not include inter lead flash.
2. Dimension b1 does not include dambar protrusion/ intrusion.
3. Controlling dimension: Inch
4. General appearance spec. should base on final visual inspection spec.

44L Plastic Quad Flat Package



Note:

Dimension D1 and E1 do not include mold protrusion.
Allowance protrusion is 0.25mm per side.
Dimension D1 and E1 do include mold mismatch
and are determined datum plane.
Dimension b does not include dumber protrusion.
Allowance dumber protrusion shall be 0.08 mm total
in excess of the b dimension at maximum material
condition. Dumber cannot be located on the lower
radius or the lead foot.

Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
⌓C	0.004	0.10

eMCU Writer List		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	LabTool - 48 (1 * 1) LabTool - 848 (1*8) * Note: Not yet, about 3/E'03
Hi-Lo 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Web site: http://www.hilosystems.com.tw	Tel:02-87923301 Fax:02-87923285 E-mail: support@hilosystems.com.tw	All - 11 (1*1) Gang - 08 (1*8) * Note: Not yet, about 3/E'03
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Web site: http://www.leap.com.tw	Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	SU - 2000 (1*8) * Note: Not yet, about 3/E'03
Xeltek Electronic Co., Ltd 338 Hongwu Road, Nanjing, China 210002 Web site: http://www.xeltek-cn.com	Tel:+86-25-4408399, 4543153-206 E-mail: xelclw@jlonline.com, xelgbw@jlonline.com	Superpro/2000 (1*1) Superpro/680 (1*1) Superpro/280 (1*1) Superpro/L+(1*1) * Note: Not yet, about 3/E'03

Feedback / Inquiry:

To :SyncMOS Technologies, Inc. Attn :MKT / Customer Service Dept. Fax :886-3-579-2960 :886-3-578-0493 Tel :886-3-579-2987 :886-3-578-3344 # 2667	From : Company : Dept, Section : Position Title : Inquiry Date : Ref No :

Description: