P89LPC904

8-bit microcontrollers with two-clock accelerated 80C51 core
1 kB 3 V byte-erasable Flash with 8-bit A/D converter

Rev. 02 — 25 June 2004 **Preliminary data**

1. General description

The P89LPC904 is a single-chip microcontroller in a low-cost 8-pin package based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC904 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 1 kB byte-erasable Flash code memory organized into 256-byte sectors and 16-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 128-byte RAM data memory.
- Two 16-bit counter/timers.
- 23-bit system timer that can also be used as a Real-Time clock.
- 2 -input multiplexed A/D converter/single DAC output. Two analog comparators with selectable reference.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, automatic address detection and versatile interrupt capabilities.
- High-accuracy internal RC oscillator option allows operation without external oscillator components. The RC oscillator option is selectable and ne tunable.
- 2.4 V to 3.6 V V_{DD} operating range with 5 V tolerant I/O pins (may be pulled up or driven to 5.5 V). Industry-standard pinout with V_{DD}, V_{SS}, and reset at locations 1, 8, and 4.
- Up to six I/O pins when using internal oscillator and reset options.
- 8-pin SO-8 package.

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 167 ns to 333 ns for all instructions except multiply and divide when executing at 12 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- In-Application Programming (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage.

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- Serial Flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The Watchdog prescaler is selectable from 8 values.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be con□gured as an interrupt.
- Idle and two different Power-down reduced power modes. Improved wake-up from Power-down mode (a low interrupt input starts execution). Typical Power-down current is 1 μA (total Power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Programmable port output con□guration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port □input pattern match□ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is speci□ed for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC904 when internal reset option is selected.
- Four interrupt priority levels.
- One keypad interrupt input.
- Second data pointer.
- External clock input.
- Schmitt trigger port inputs.
- Emulation support.

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
P89LPC904FD	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT96-1

3.1 Ordering options

Table 2: Part options

Type number	Temperature range	Frequency
P89LPC904FD	–40 °C to +85 °C	Internal RC or Watchdog

4. Block diagram

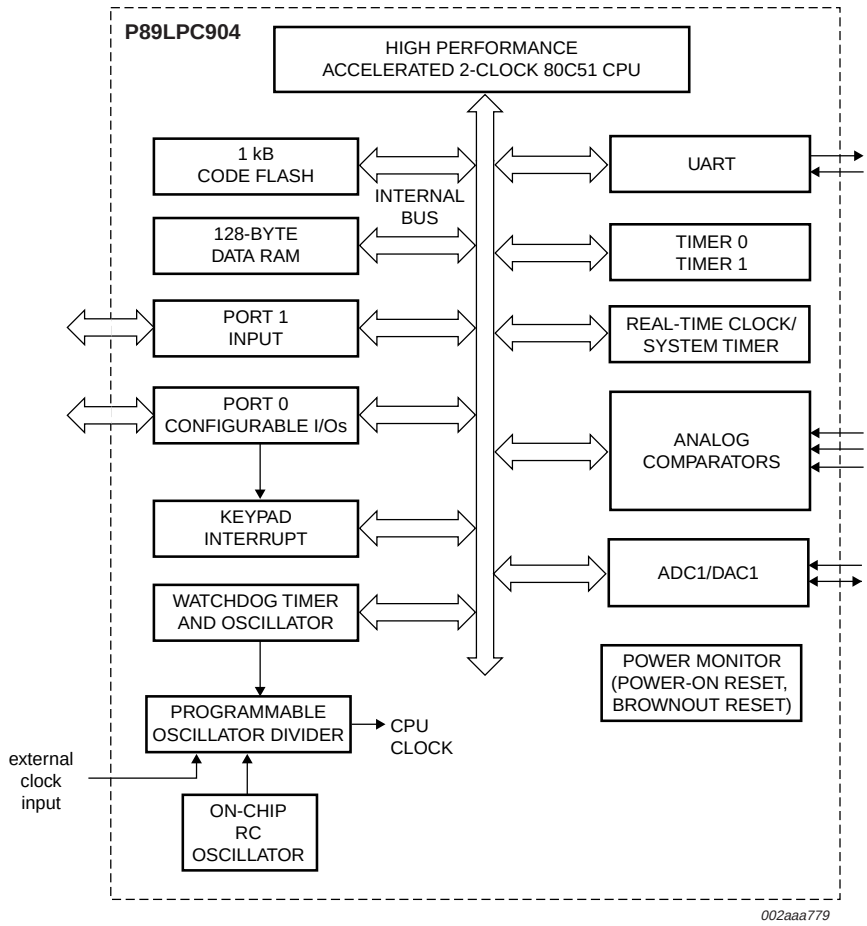


Fig 1. P89LPC904 block diagram.

5. Pinning information

5.1 Pinning

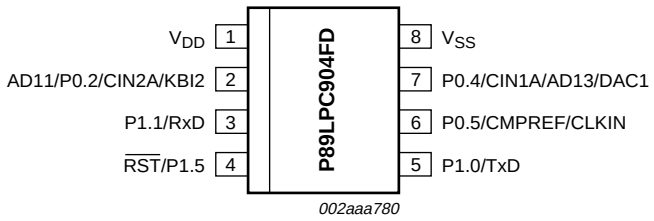


Fig 2. P89LPC904 pinning (SO8).

5.2 Pin description

Table 3: P89LPC904 pin description

Symbol	Pin	Type	Description
P0.0 to P0.6	2, 6, 7	I/O	**Port 0:** Port 0 is an I/O port with a user-con□gurable output type. During reset Port 0 latches are con□gured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port con□guration selected. Each port pin is con□gured independently. Refer to Section 8.13.1 □Port con□gurations□ and Table 8 □DC electrical characteristics□ for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
	2	I/O	**P0.2** □ Port 0 bit 2.
		I	**CIN2A** □ Comparator 2 positive input.
		I	**KBI2** □ Keyboard input 2.
		I	**AD11** □ ADC1 channel 1 analog input.
	7	I/O	**P0.4** □ Port 0 bit 4.
		I	**CIN1A** □ Comparator 1 positive input.
		I	**AD13** □ ADC1 channel 3 analog input.
		O	**DAC1** □ Digital to analog converter output.
	6	I/O	**P0.5** □ Port 0 bit 5.
		I	**CMPREF** □ Comparator reference (negative) input.
		I	**CLKIN** □ External clock input.

Table 3: P89LPC904 pin description *continued*

Symbol	Pin	Type	Description
P1.0 to P1.5	3, 4, 5		**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 "Port configurations" and Table 8 "DC electrical characteristics" for details. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
	5	I/O	**P1.0** – Port 1 bit 0.
		O	**TxD** – Serial port transmitter data.
	3	I/O	**P1.1** – Port 1 bit 1.
		I	**RxD** – Serial port receiver data.
	4	I	**P1.5** – Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$** – External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force In-System Programming mode.
V_{SS}	8	I	**Ground:** 0 V reference.
V_{DD}	1	I	**Power Supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

6. Logic symbols

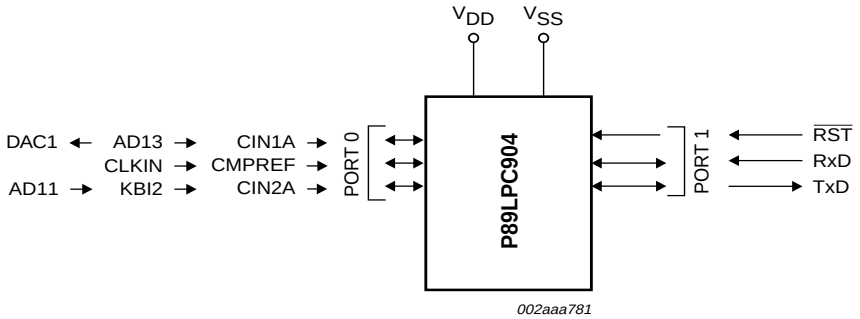


Fig 3. P89LPC904 logic symbol.

7. Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not de□ned.
- Accesses to any de□ned SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled □-□, □0□ or □1□ can **only** be written and read as follows:
  - □-□ Unless otherwise speci□ed, **must** be written with □0□, but can return any value when read (even if it was written with □0□). It is a reserved bit and may be used in future derivatives.
  - □0□ **must** be written with □0□, and will return a □0□ when read.
  - □1□ **must** be written with □1□, and will return a □1□ when read.

Table 4: P89LPC904 Special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	00000000
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	00000000
ADINS	A/D input select	A3H	ADI13	-	ADI11	-	-	-	-	-	00	00000000
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	00000000
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1	-	00	000x0000
AD1BH	A/D_1 boundary high register	C4H									FF	11111111
AD1BL	A/D_1 boundary low register	BCH									00	00000000
AD1DAT0	A/D_1 data register 0	D5H									00	00000000
AD1DAT1	A/D_1 data register 1	D6H									00	00000000
AD1DAT2	A/D_1 data register 2	D7H									00	00000000
AD1DAT3	A/D_1 data register 3	F5H									00	00000000
AUXR1	Auxiliary function register	A2H	-	EBRR	-	-	SRST	0	-	DPS	00[1]	000000x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	00000000
BRGR0[2]	Baud rate generator rate LOW	BEH									00	00000000
BRGR1[2]	Baud rate generator rate HIGH	BFH									00	00000000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxxxx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	-	CN1	-	CO1	CMF1	00[1]	xx000000
CMP2	Comparator 2 control register	ADH	-	-	CE2	-	CN2	-	CO2	CMF2	00	xx000000
DIVM	CPU clock divide-by-M control	95H									00	00000000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer HIGH	83H									00	00000000
DPL	Data pointer LOW	82H									00	00000000
FMADRH	Program Flash address HIGH	E7H									00	00000000
FMADRL	Program Flash address LOW	E6H									00	00000000

Table 4: P89LPC904 Special function registers *continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMCON	Program Flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	01110000
	Program Flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program Flash data	E5H									00	00000000
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	-	00	00000000
	Bit address		EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	-	EST	-	-	-	EC	EKBI	-	00[1]	00x00000
	Bit address		BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	-	00[1]	x0000000
IP0H	Interrupt priority 0 HIGH	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	-	00[1]	x0000000
	Bit address		FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI	-	00[1]	00x00000
IP1H	Interrupt priority 1 HIGH	F7H	PADH	PSTH	-	-	-	PCH	PKBIH	-	00[1]	00x00000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxxxx00
KBMASK	Keypad interrupt mask register	86H									00	00000000
KBPATN	Keypad pattern register	93H									FF	11111111
	Bit address		87	86	85	84	83	82	81	80		
P0*	Port 0	80H	-	-	CMPREF	CIN1A	-	KB2	-	-	[1]	
	Bit address		97	96	95	94	93	92	91	90		
P1*	Port 1	90H	-	-	$\overline{RST}$	-	-	-	RxD	TxD		
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	-	(P0M1.2)	-	-	FF	11111111
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	-	(P0M2.2)	-	-	00	00000000
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	-	(P1M1.1)	(P1M1.0)	FF[1]	11111111
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	-	(P1M2.1)	(P1M2.0)	00[1]	00000000
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	00000000
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	SPD		00[1]	00000000

Table 4: P89LPC904 Special function registers *continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
PCONB	reserved for Power Control Register B	B6H	-	-	-	-	-	-	-	-	00[1]	xxxxxxxx
	Bit address		D7	D6	D5	D4	D3	D2	D1	D0		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	00000000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	-	PT0AD.2	-	-	00	xx00000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1] [7]	011xxx00
RTCH	Real-time clock register HIGH	D2H									00[7]	00000000
RTCL	Real-time clock register LOW	D3H									00[7]	00000000
SADDR	Serial port address register	A9H									00	00000000
SADEN	Serial port address enable	B9H									00	00000000
SBUF	Serial port data buffer register	99H									xx	xxxxxxxx
	Bit address		9F	9E	9D	9C	9B	9A	99	98		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	00000000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	00000000
SP	Stack pointer	81H									07	00000111
	Bit address		8F	8E	8D	8C	8B	8A	89	88		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-	-	00	00000000
TH0	Timer 0 HIGH	8CH									00	00000000
TH1	Timer 1 HIGH	8DH									00	00000000
TL0	Timer 0 LOW	8AH									00	00000000
TL1	Timer 1 LOW	8BH									00	00000000
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1	T0M0	00	00000000
TRIM	Internal oscillator trim register	96H	RCCLK	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1	TRIM.0	[5] [6]	
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF	WDCLK	[4] [6]	
WDL	Watchdog load	C1H									FF	11111111
WFEED1	Watchdog feed 1	C2H										
WFEED2	Watchdog feed 2	C3H										

[1] All ports are in input only (high-impedance) state after power-up.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.

[3] Unimplemented bits in SFRs (labeled □-□) are X (unknown) at all times. Unless otherwise speci□ed, ones should not be written to these bits since they may be used for other purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[4] The RSTSRC register re□ects the cause of the P89LPC904 reset. Upon a power-up reset, all reset source □ags are cleared except POF and BOF; the power-on reset value is xx110000.

[5] After reset, the value is 111001x1, i.e., PRE2-PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after Watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTOF.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] The only reset source that affects these SFRs is power-on reset.

8. Functional description

Remark: Please refer to the *P89LPC904 User's Manual* for a more detailed functional description.

8.1 Enhanced CPU

The P89LPC904 uses an enhanced 80C51 CPU which runs at 6 times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.2 Clocks

8.2.1 Clock definitions

The P89LPC904 device has internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of the clock sources (see Figure 4) and can also be optionally divided to a slower frequency (see Section 8.7 "CPU CLOCK (CCLK) modification: DIVM register").

Note: f_{ext} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output.

PCLK — Clock for the various peripheral devices and is CCLK/2

8.2.2 CPU clock (CCLK)

The P89LPC904 provides several user-selectable options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the FLASH is programmed and include an on-chip Watchdog oscillator and an on-chip RC oscillator.

8.3 On-chip RC oscillator option

The P89LPC904 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz, ±1 % at room temperature. End-user applications can write to the Trim register to adjust the on-chip RC oscillator to other frequencies. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

8.4 Watchdog oscillator option

The Watchdog has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

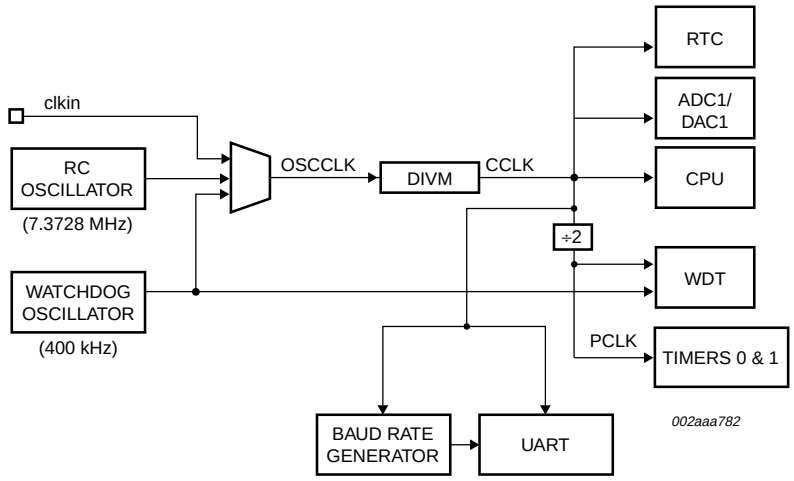


Fig 4. Block diagram of oscillator control.

8.5 External clock input option

In this con□guration, the processor clock is derived from an external source driving the P0.5/CMPREF/CLKIN pin. The rate may be from 0 Hz up to 12 MHz. The P0.5/CMPREF/CLKIN pin may also be used as a standard port pin.

8.6 CPU CLock (CCLK) wake-up delay

The P89LPC904 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used.

8.7 CPU CLOCK (CCLK) modi□cation: DIVM register

The OSCCLK frequency can be divided down up to 510 times by con□guring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.8 Low power select

If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0.

8.9 A/D converter

8.9.1 General description

The P89LPC904 has an 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter. A block diagram of the A/D converter is shown in Figure 5. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the successive approximation register (SAR) drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

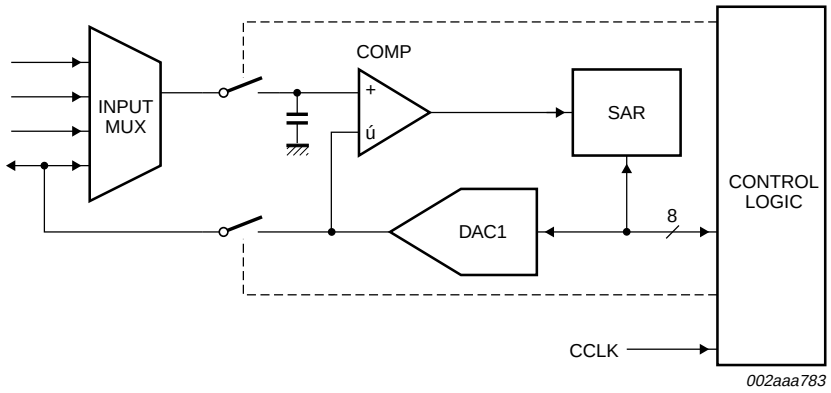


Fig 5. ADC block diagram.

8.9.2 Features

- 8-bit, 4-channel multiplexed input, successive approximation A/D converter.
- Four result registers.
- Six operating modes
  - Fixed channel, single conversion mode
  - Fixed channel, continuous conversion mode
  - Auto scan, single conversion mode
  - Auto scan, continuous conversion mode
  - Dual channel, continuous conversion mode
  - Single step mode
- Four conversion start modes
  - Timer triggered start
  - Start immediately
  - Edge triggered
  - Dual start immediately
- 8-bit conversion time of ≥3.9 µs at an ADC clock of 3.3 MHz
- Interrupt or polled operation
- Boundary limits interrupt
- DAC output to a port pin with high output impedance
- Clock divider
- Power-down mode

8.9.3 A/D operating modes

Fixed channel, single conversion mode: A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

Fixed channel, continuous conversion mode: A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

Auto scan, single conversion mode: Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

Auto scan, continuous conversion mode: Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the

selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the □rst selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results.Continous conversions continue until terminated by the user.

Dual channel, continuous conversion mode: This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the □rst channel is placed in result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The □rst channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

Single step mode: This special mode allows □single-stepping□ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

8.9.4 Conversion start modes

Timer triggered start: An A/D conversion is started by the over□ow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

Start immediately: Programming this mode immediately starts a conversion.This start mode is available in all A/D operating modes.

Edge triggered: An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

8.9.5 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

8.9.6 DAC output to a port pin with high output impedance

The A/D converter□s DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC (written to AD1DAT3), the DAC output will appear on the channel 3 pin.

8.9.7 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.9.8 Power-down and idle mode

In idle mode the A/D converter, if enabled, will continue to function and can cause the device to exit idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

8.10 Memory organization

The various P89LPC904 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00h:7Fh) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the Stack may be in this area.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC904 has 1 kB of on-chip Code memory.

8.11 Data RAM arrangement

The 128 bytes of on-chip RAM is organized as follows:

Table 5: On-chip data memory usages

Type	Data RAM	Size (Bytes)
DATA	Memory that can be addressed directly and indirectly	128

8.12 Interrupts

The P89LPC904 supports 10 interrupt sources: timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, Watchdog/real-time clock, keyboard, and comparators 1 and 2, and the A/D converter.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.12.1 External interrupt inputs

The P89LPC904 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC904 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.15 “Power reduction modes” for details.

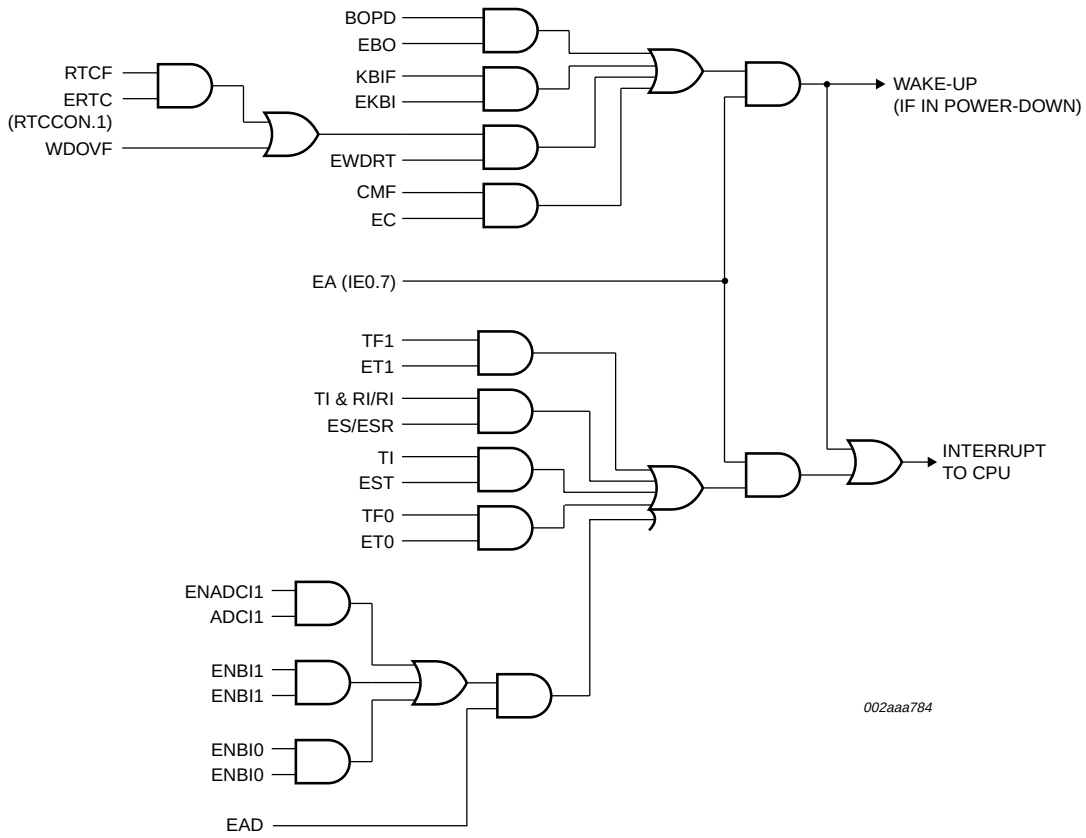


Fig 6. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC904).

8.13 I/O ports

The P89LPC904 has either 5 or 6 I/O pins depending on the reset pin option chosen. Refer to Table 6.

Table 6: Number of I/O pins available

Clock source	Reset option	Number of I/O pins (8-pin package)
On-chip oscillator or Watchdog oscillator	No external reset (except during power-up)	6
	External $\overline{\text{RST}}$ pin supported	5
External clock input	No external reset (except during power-up)	5
	External $\overline{\text{RST}}$ pin supported	4

8.13.1 Port con□gurations

All but one I/O port pin on the P89LPC904 may be con□gured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two con□guration registers for each port select the output type for each port pin.

P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be con□gured.

8.13.2 Quasi-bidirectional output con□guration

Quasi-bidirectional output type can be used as both an input and output without the need to recon□gure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC904 is a 3 V device, however, the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current □owing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.3 Open-drain output con□guration

The open-drain output con□guration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port con□gured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.4 Input-only con□guration

The input-only port con□guration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

8.13.5 Push-pull output con□guration

The push-pull output con□guration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.6 Port 0 analog functions

The P89LPC904 incorporates an Analog Comparator. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode as described in Section 8.13.4 □Input-only con□guration□

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, the PT0AD bits default to logic 0s to enable digital functions.

8.13.7 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up all I/O pins, except P1.5, may be configured by software.
- Pin P1.5 is input only.

Every output on the P89LPC904 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 8 "DC electrical characteristics" for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.14 Power monitoring functions

The P89LPC904 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

8.14.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however, it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the operating voltage range for V_{DD} is 2.7 V to 3.6 V, and the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{BO} (see Table 8 "DC electrical characteristics"), and is negated when V_{DD} rises above V_{BO}. If brownout detection is disabled, the operating voltage range for V_{DD} is 2.4 V to 3.6 V. If the P89LPC904 device is to operate with a power supply that can be below 2.7 V, BOE should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 8 "DC electrical characteristics" for specifications.

8.14.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.15 Power reduction modes

The P89LPC904 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

8.15.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.15.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC904 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the RAM keep-alive voltage V_{RAM}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{RAM}, therefore it is highly recommended to wake up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down. These include: Brownout detect, Watchdog Timer, Comparators (note that Comparators can be powered-down separately), and Real-Time Clock (RTC)/System Timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled.

8.15.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the Real-Time Clock running during Power-down.

8.16 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as de□ned by the RPE bit. Only a power-up reset will temporarily override the selection de□ned by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see Table 8 □DC electrical characteristics□) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user con□gured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog Timer
- Software reset
- UART break character detect reset.

For every reset source, there is a □ag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These □ag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one □ag bit may be set:

- During a power-on reset, both POF and BOF are set but the other □ag bits are cleared.
- For any other reset, previously set □ag bits that have not been cleared will remain set.

8.17 Timers/counters 0 and 1

The P89LPC904 has two general purpose timers which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have four operating modes (modes 0, 1, 2, and 3). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different.

8.17.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is con□gured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.17.3 Mode 2

Mode 2 con□gures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.18 Real-Time clock/system timer

The P89LPC904 has a simple Real-Time clock that allows a user to continue running an accurate timer while the rest of the device is powered-down. The Real-Time clock can be a wake-up or an interrupt source. The Real-Time clock is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it

reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter is the CPU clock (CCLK). Only power-on reset will reset the Real-Time clock and its associated SFRs to the default state.

8.19 UART

The P89LPC904 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC904 does include an independent Baud Rate Generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in 4 modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

8.19.1 Mode 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $^1/_{16}$ of the CPU clock frequency.

8.19.2 Mode 1

10 bits are transmitted (through TxD) or received (through RxD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.19.5 "Baud rate generator and selection").

8.19.3 Mode 2

11 bits are transmitted (through TxD) or received (through RxD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $^1/_{16}$ or $^1/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.19.4 Mode 3

11 bits are transmitted (through TxD) or received (through RxD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.19.5 "Baud rate generator and selection").

8.19.5 Baud rate generator and selection

The P89LPC904 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 7). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses CCLK.

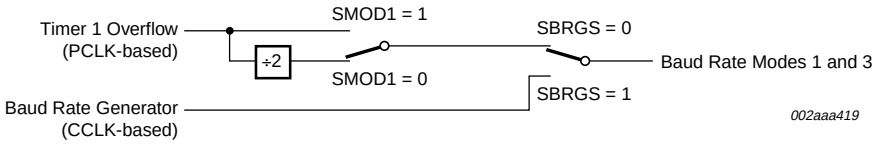


Fig 7. Baud rate sources for UART (Modes 1, 3).

8.19.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7, respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

8.19.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device.

8.19.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the rst character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

8.19.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.19.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.20 Analog comparators

Two analog comparators are provided on the P89LPC904. Comparator operation is such that the output is a logic 1 (which may be read in a register) when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. The comparator may be con□gured to cause an interrupt when the output value changes.

The connections to the comparator are shown in Figure 8. The comparator functions to V_{DD} = 2.4 V.

When the comparator is □rst enabled, the comparator□s interrupt □ag is not guaranteed to be stable for 10 microseconds. The comparator interrupt should not be enabled during that time, and the comparator interrupt □ag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator□s output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator □ag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator □ag, CMFx, after disabling the comparator.

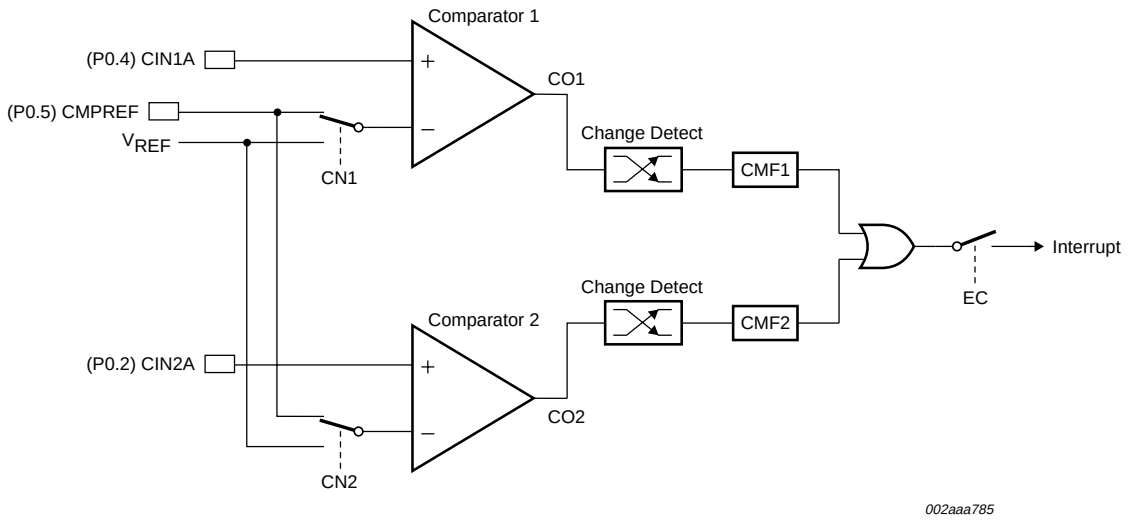


Fig 8. Comparator input and output connections.

8.21 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as V_{REF}, is 1.23 V ±10 %.

8.22 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt.

8.23 Comparator and power reduction modes

The comparators may remain enabled when Power-down or Idle mode is activated, but the comparators are disabled automatically in Total Power-down mode.

If the comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

The comparator consumes power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparator via PCONA.5 or put the device in Total Power-down mode.

8.24 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

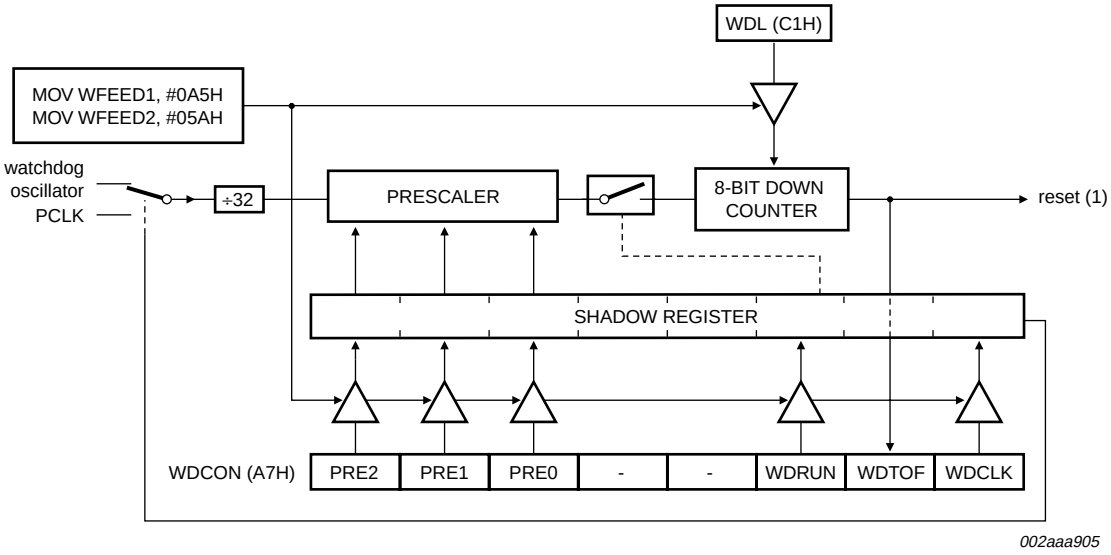
The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than 6 CCLKs.

8.25 Watchdog timer

The Watchdog timer causes a system reset when it under□ows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz Watchdog oscillator. The Watchdog timer can only be reset by a power-on reset. When the Watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 9 shows the Watchdog timer in Watchdog mode. Feeding the Watchdog requires a two-byte sequence. If PCLK is selected as the Watchdog clock and the CPU is powered-down, the Watchdog is disabled. The Watchdog timer has a time-out period that ranges from a few μs to a few seconds. Please refer to the *P89LPC904 User□s Manual* for more details.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 9. Watchdog timer in Watchdog mode (WDTE = 1).

8.26 Additional features

8.26.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or Watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.26.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

8.27 Flash program memory

8.27.1 General description

The P89LPC904 Flash memory provides in-circuit electrical erasure and programming. The Flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any Flash sector (256 bytes) or page (16 bytes). The Chip Erase operation will erase the entire program memory. In-Circuit Programming using standard commercial programmers is available. In addition, In-Application Programming (IAP) and byte erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC904 Flash reliably stores memory contents even after more than 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC904 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.27.2 Features

- Programming and erase over the full operating voltage range.
- Byte-erase allowing code memory to be used for data storage.
- Read/Programming/Erase using ICP.
- Any □ash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the Flash for each sector.
- More than 100,000 minimum erase/program cycles for each byte.
- 10-year minimum data retention.

8.27.3 Flash organization

The P89LPC904 program memory consists of four 256 byte sectors. Each sector can be further divided into 16-byte pages. In addition to sector erase, page erase, and byte erase, a 16-byte page register is included which allows from 1 to 16 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. In addition, erasing and reprogramming of user-programmable con□guration bytes including UCFG1, the Boot Status Bit, and the Boot Vector is supported.

8.27.4 Flash programming and erasing

Different methods of erasing or programming of the Flash are available. The Flash may be programmed or erased in the end-user application (IAP) under control of the application□s □rmware. Another option is to use the In-Circuit Programming (ICP) mechanism. This ICP system provides for programming through a serial clock- serial data interface. Third, the Flash may be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct veri□cation of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 1 KB of user code space.

8.27.5 In-circuit programming (ICP)

In-Circuit Programming is performed without removing the microcontroller from the system. The In-Circuit Programming facility consists of internal hardware resources to facilitate remote programming of the P89LPC904 through a two-wire serial

interface. The Philips In-Circuit Programming facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses □ve pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC904 User□s Manual*

8.27.6 In-application programming

In-Application Programming is performed in the application under the control of the microcontroller□s □rmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The Philips In-Application Programming has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC904 User□s Manual*

8.27.7 Using □ash as data storage

The Flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.27.8 User con□guration bytes

Some user-con□gurable features of the P89LPC904 must be de□ned at power-up and therefore cannot be set by the program after start of execution. These features are con□gured through the use of the Flash byte UCFG1. Please see the*P89LPC904 User□s Manual*for additional details.

8.27.9 User sector security bytes

There are four User Sector Security Bytes, each corresponding to one sector. Please see the *P89LPC904 User□s Manual*for additional details.

9. Limiting values

Table 7: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	operating bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature range		–65	+150	°C
V_n	voltage on any pin to V_{SS}		–0.5	+5.5	V
$I_{OH(I/O)}$	HIGH-level output current per I/O pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per I/O pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	120	mA
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] Stresses above those listed under Table 7 “Limiting values” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 8 “DC electrical characteristics” and Table 9 “AC characteristics” section of this specification are not implied.

[2] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects ofexcessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[3] Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

10. Static characteristics

Table 8: DC electrical characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	power supply current, operating	3.6 V; 12 MHz	[7]	-	3.1	<tbd>	mA
$I_{DD(idle)}$	power supply current, Idle mode	3.6 V; 12 MHz	[7]	-	2	<tbd>	mA
$I_{DD(PD)}$	Power supply current, Power-down mode, voltage comparators powered-down	3.6 V	[7]	-	55	<tbd>	µA
$I_{DD(TPD)}$	Power supply current, total Power-down mode	3.6 V	[8]	-	<0.1	<tbd>	µA
V_{DDR}	V_{DD} rise time			-	-	2	mV/µs
V_{DDF}	V_{DD} fall time			-	-	50	mV/µs
V_{POR}	Power-on reset detect voltage			-	-	0.2	V
V_{RAM}	RAM keep-alive voltage			1.5	-	-	V
$V_{th(HL)}$	negative-going threshold voltage (Schmitt trigger input)			$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	positive-going threshold voltage (Schmitt trigger input)			-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage; all ports, all modes except Hi-Z	I_{OL} = 20 mA		-	0.6	1.0	V
		I_{OL} = 10 mA		-	0.3	0.5	V
		I_{OL} = 3.2 mA		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage, all ports	I_{OH} = −8 mA; push-pull mode		V_{DD} − <tbd>	-	-	V
		I_{OH} = −3.2 mA; push-pull mode		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −20 µA; quasi-bidirectional mode		V_{DD} − 0.3	V_{DD} − 0.2	-	V
C_{ig}	input-ground capacitance		[6]	-	-	15	pF
I_{IL}	logic 0 input current, all ports	V_{IN} = 0.4 V	[5]	-	-	−80	µA
I_{LI}	input leakage current, all ports	V_{IN} = V_{IL} or V_{IH}	[4]	-	-	± 10	µA
I_{TL}	logic 1-to-0 transition current, all ports	V_{IN} = 2.0 V at V_{DD} = 3.6 V	[2][3]	−30	-	−450	µA
R_{RST}	internal reset pull-up resistor			10	-	30	kΩ
V_{BO}	brownout trip voltage with BOV = 1, BOPD = 0	2.4 V < V_{DD} < 3.6 V		2.40	-	2.70	V
V_{REF}	band gap reference voltage			1.11	1.23	1.34	V
$TC_{(VREF)}$	band gap temperature coefficient			-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups)

[3] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_{IN} is approximately 2 V.

[4] Measured with port in high-impedance mode.

[5] Measured with port in quasi-bidirectional mode.

[6] Pin capacitance is characterized but not tested.

[7] The $I_{DD(oper)}$ and $I_{DD(PD)}$ speci□cations are measured with the following functions disabled: comparators and Watchdog timer.

[8] The $I_{DD(TPD)}$ speci□cation is measured with the following functions disabled: comparators, brownout detect, and Watchdog timer.

11. Dynamic characteristics

Table 9: AC characteristics

T_{amb} = −40 °C to +85 °C for industrial, unless otherwise speci□ed.[1]

Symbol	Parameter	Conditions	Variable clock		f_{ext} = 12 MHz		Unit
			Min	Max	Min	Max	
f_{RCOSC}	internal RC oscillator frequency (nominal f = 7.3728 MHz) trimmed to ± 1 % at T_{amb} = 25 °C		7.189	7.557	7.189	7.557	MHz
f_{WDOSC}	internal Watchdog oscillator frequency (nominal f = 400 kHz)		280	480	280	480	kHz
Glitch □lter							
	glitch rejection, P1.5/$\overline{RST}$ pin		-	50	-	50	ns
	signal acceptance, P1.5/$\overline{RST}$ pin		125	-	125	-	ns
	glitch rejection, any pin except P1.5/$\overline{RST}$		-	15	-	15	ns
	signal acceptance, any pin except P1.5/$\overline{RST}$		50	-	50	-	ns
Shift register (UART mode 0)							
t_{XLXL}	serial port clock cycle time	see Figure 10	$16t_{CLCL}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 10	$13t_{CLCL}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 10	-	t_{CLCL} + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 10	-	0	-	0	ns
t_{DVXH}	input data valid to clock rising edge	see Figure 10	150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise speci□ed.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

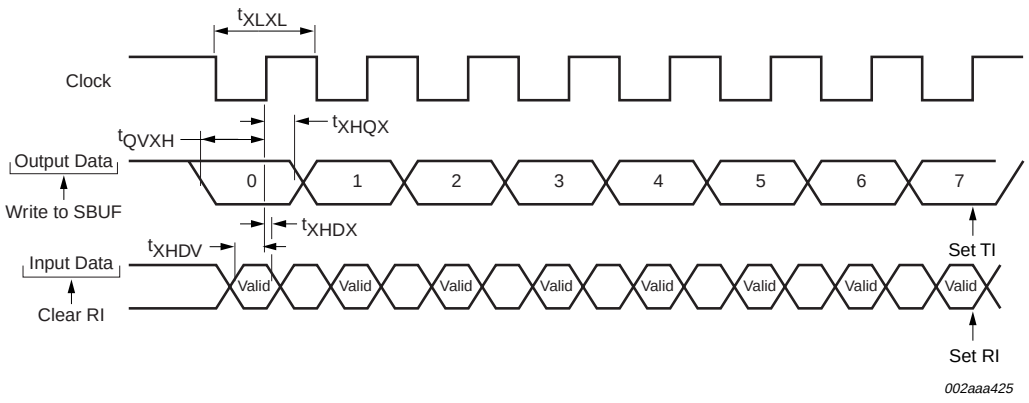


Fig 10. Shift register mode timing.

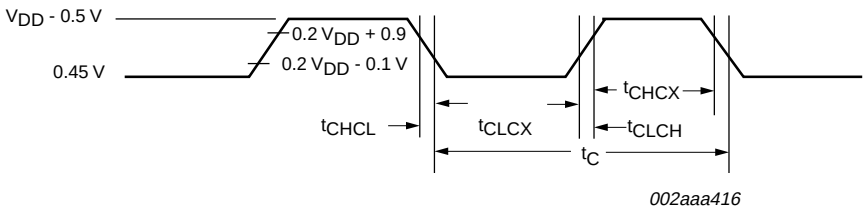


Fig 11. External clock timing.

12. Comparator electrical characteristics

Table 10: Comparator electrical characteristics

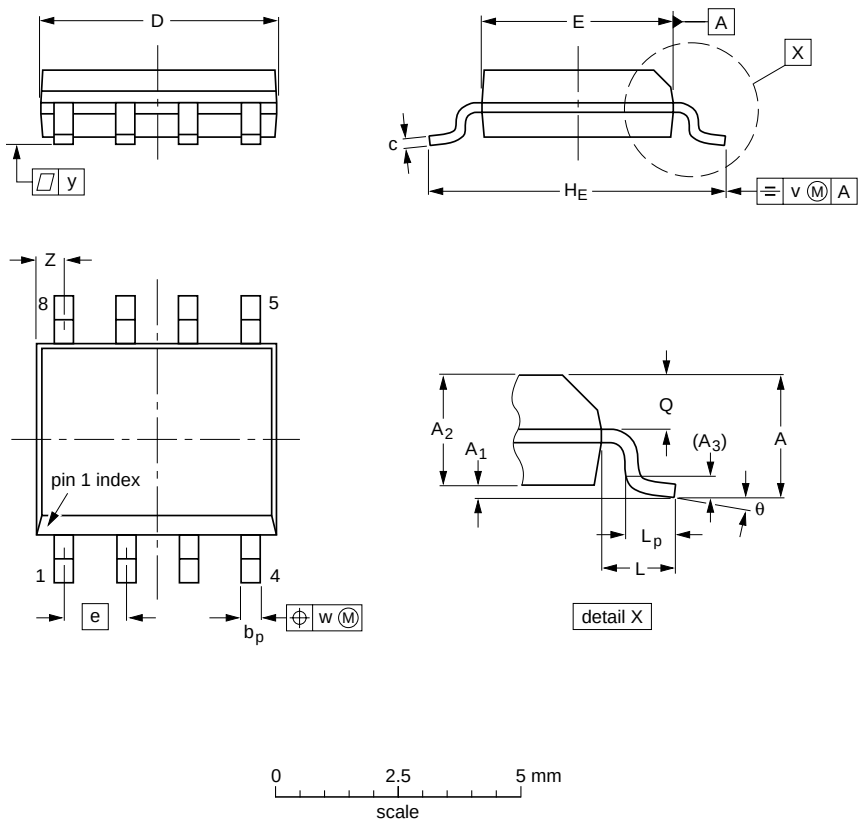
V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40°C to +85°C for industrial, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IO}	offset voltage comparator inputs			-	-	± 20	mV
V_{CR}	common mode range comparator inputs			0	-	V_{DD} − 0.3	V
CMRR	common mode rejection ratio		[1]	-	-	−50	dB
	response time			-	250	500	ns
	comparator enable to output valid			-	-	10	µs
I_{IL}	input leakage current, comparator	$0 < V_{IN} < V_{DD}$		-	-	± 10	µA

[1] This parameter is characterized, but not tested in production.

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 12. SOT96-1.

14. Revision history

Table 11: Revision history

Rev	Date	CPCN	Description
02	20040625	-	**Preliminary data (9397 750 13521)** Modi□cations: ¥ Updated references to keypad interrupt inputs (changed from 3 to 1) throughout data sheet. ¥ Table 4 □P89LPC904 Special function registers□ on page 9, adjusted rows ADMODB, IP1, IP1H, P0, P1M1, P1M2, PCONA, and TRIM. ¥ Section 8.2.1 □Clock de□nitions□ on page 12, adjusted note. ¥ Section 8.2.2 □CPU clock (CCLK)□ on page 13, adjusted title and paragraph. ¥ Figure 5 □ADC block diagram.□ on page 16, adjusted graphic. ¥ Section 8.9.2 □Features□ on page 17, adjusted 8-bit conversion time. ¥ Section 8.9.7 □Clock divider□ on page 19, adjusted range (3 MHz now 3.3 MHz). ¥ Figure 9 □Watchdog timer in Watchdog mode (WDTE = 1).□ on page 30, updated graphic to new standard. ¥ Table 8 □DC electrical characteristics□ on page 34, added note for $I_{DD(TPD)}$ spec.
01	20040413	-	**Preliminary data (9397 750 12854)**

15. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	De□nition
I	Objective data	Development	This data sheet contains data from the objective speci□cation for product development. Philips Semiconductors reserves the right to change the speci□cation in any manner without notice.
II	Preliminary data	Quali□cation	This data sheet contains data from the preliminary speci□cation. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the speci□cation without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product speci□cation. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Noti□cation (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. De□nitions

Short-form speci□cation □ The data in a short-form speci□cation is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values de□nition □ Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the speci□cation is not implied. Exposure to limiting values for extended periods may affect device reliability.

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