DATA SHEET

P80CL31; P80CL51
Low voltage 8-bit microcontrollers with UART

Product specification
Supersedes data of January 1995
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CONTENTS

1 FEATURES

- Full static 80C51 Central Processing Unit
- 8-bit CPU, ROM, RAM, I/O in a 40-lead DIP, 40-lead VSO or 44-lead QFP package
- 128 bytes on-chip RAM Data Memory
- 4 kbytes on-chip ROM Program Memory for P80CL51
- External memory expandable up to 128 kbytes: RAM up to 64 kbytes and ROM up to 64 kbytes
- Four 8-bit ports; 32 I/O lines
- Two 16-bit Timer/Event counters
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector, nested interrupt structure with two priority levels
- Full duplex serial port (UART)
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8-byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 128 bytes)
  - multiply, divide, subtract and compare instructions
- Reduced power consumption through Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Frequency range: 0 to 16 MHz (P80C51: 3.5 MHz min.)
- Supply voltage: 1.8 to 6.0 V (P80C51: 5.0 V ±10%)
- Very low current consumption
- Operating ambient temperature range: –40 to +85 °C.

2 GENERAL DESCRIPTION

The P80CL31; P80CL51 (hereafter generally referred to as the P80CLx1) is manufactured in an advanced CMOS technology. The P80CLx1 has the same instruction set as the 80C51, consisting of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. The device operates over a wide range of supply voltages and has low power consumption; there are two software selectable modes for power reduction: Idle and Power-down. For emulation purposes, the P85CL000 (piggy-back version) with 256 bytes of RAM is recommended.

This data sheet details the specific properties of the P80CL31; P80CL51. For details of the 80C51 core see *“Data Handbook IC20”*.

2.1 Versions: P80CL31 and P80C51

The P80CL31 is the ROMless version of the P80CL51. The mask options on the P80CL31 are fixed as follows:

- All ports have option ‘1S’ (standard, HIGH after reset)
- Oscillator option: Oscillator 3
- Power-on-reset option: OFF.

The P80C51 is a restricted-voltage range version of the P80CL51. The operating voltage is 5.0 V ±10%.

3 APPLICATIONS

The P80CLx1 is especially suited for real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products. The P80CLx1 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

4 ORDERING INFORMATION

TYPE NUMBER[1]		PACKAGE		
ROMless	**ROM**	**NAME**	**DESCRIPTION**	**VERSION**
P80CL31HFP	P80CL51HFP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
P80CL31HFT	P80CL51HFT	VSO40	plastic very small outline package; 40 leads	SOT158-1
P80CL31HFH	P80CL51HFH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2
–	P80C51HFP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
–	P80C51HFT	VSO40	plastic very small outline package; 40 leads	SOT158-1
–	P80C51HFH	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2

Note

1. Refer to the Order Entry Form (OEF) for this device for the full type number, including options/program.

5 BLOCK DIAGRAM

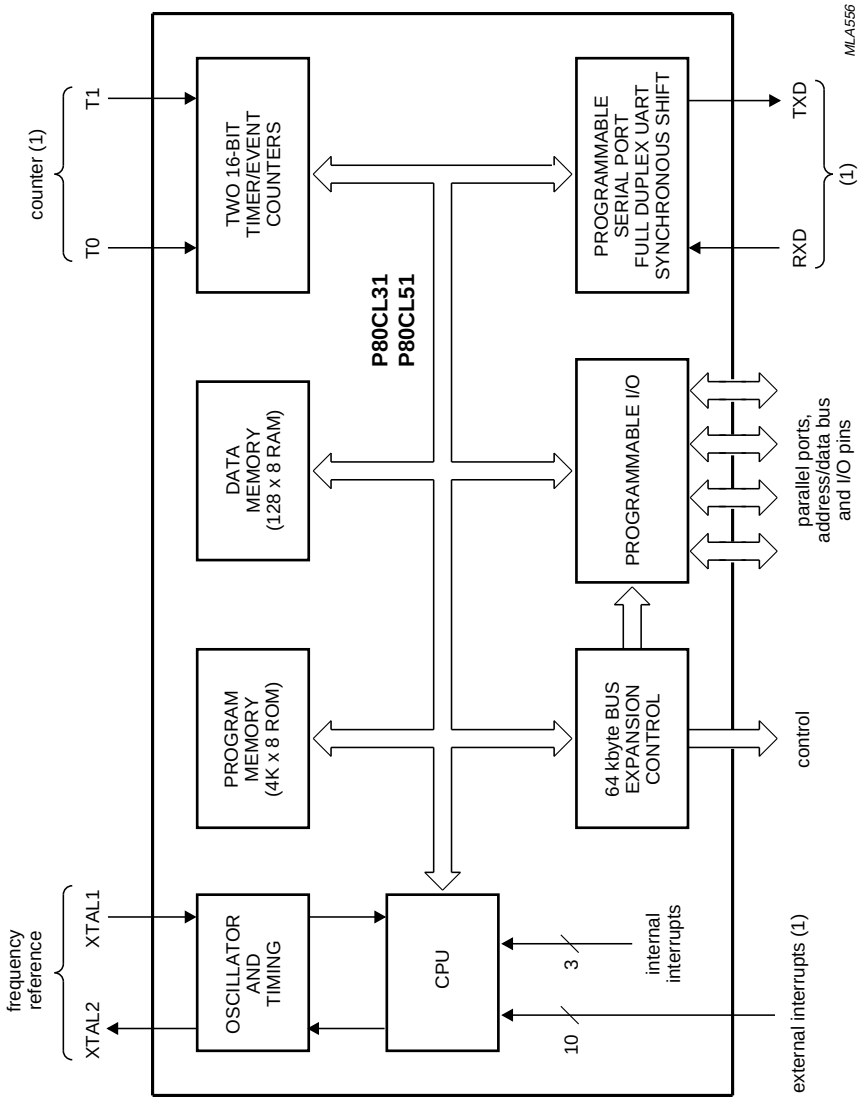


Fig.1 Block diagram.

(1) Pins shared with parallel port pins.

6 FUNCTIONAL DIAGRAM

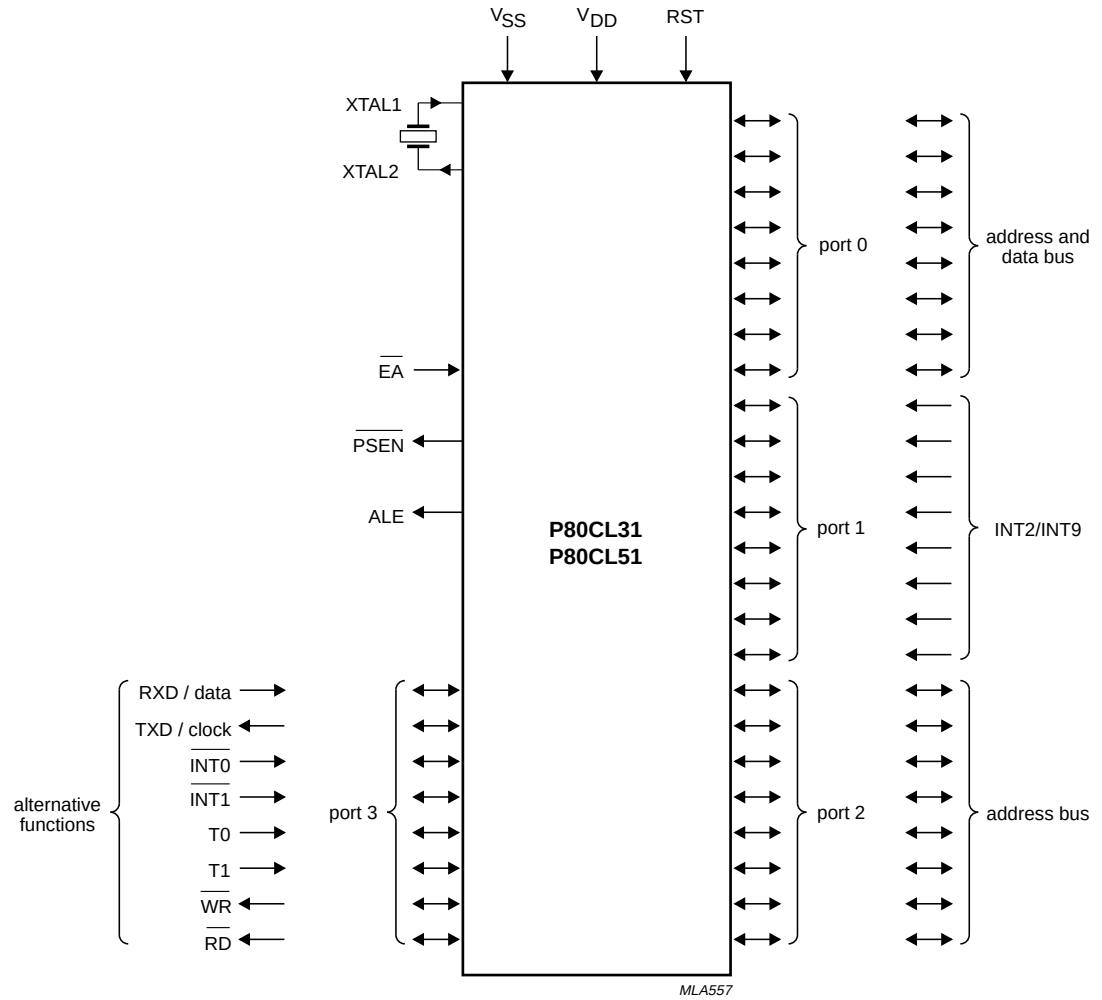


Fig.2 Functional diagram.

7 PINNING INFORMATION

7.1 Pinning

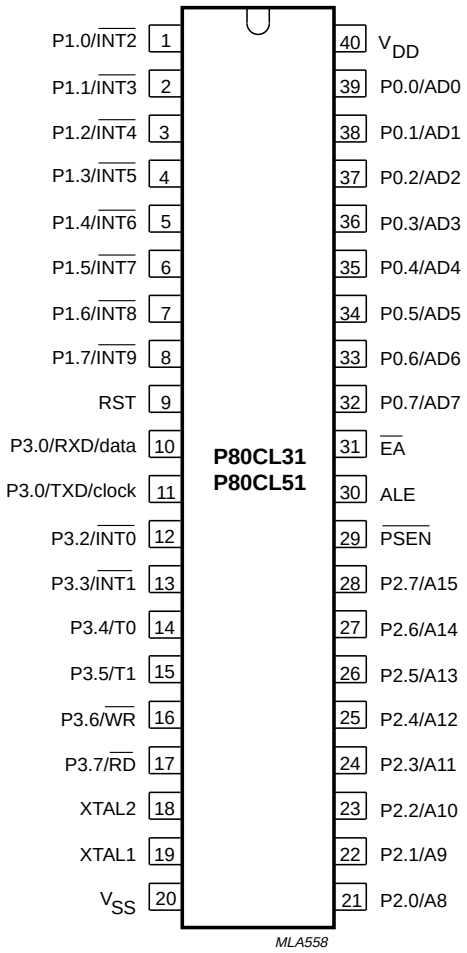


Fig.3 Pin configuration for DIP40 and VSO40 packages.

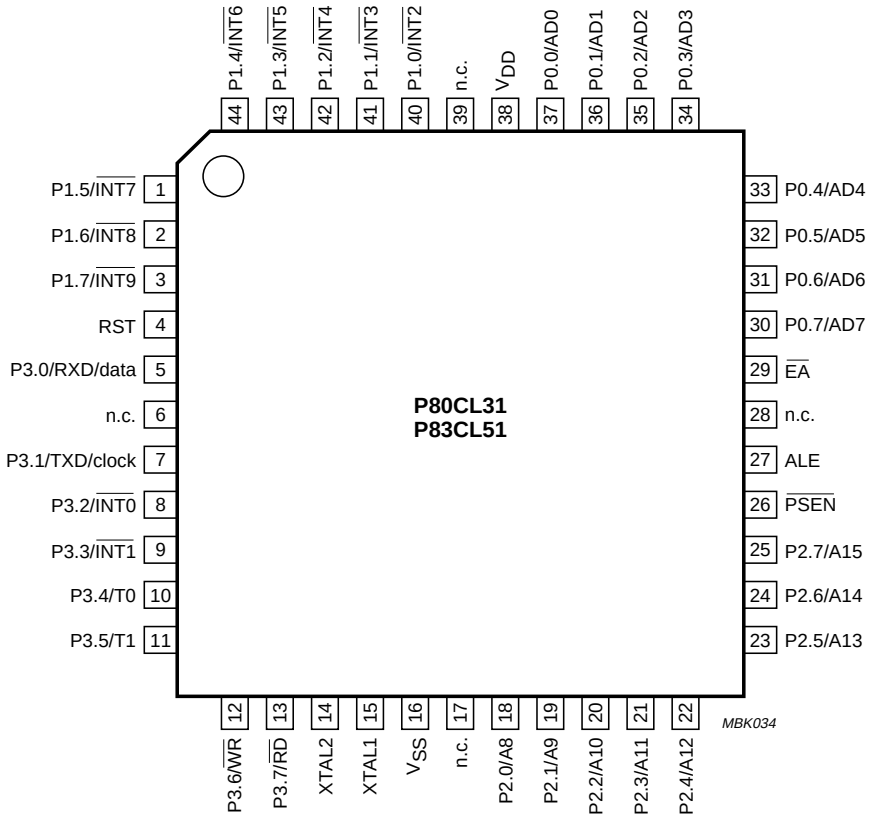


Fig.4 Pin configuration for QFP44 package.

7.2 Pin description

Table 1 Pin description for DIP40 (SOT190-1), VSO40 (SOT319-2) and QFP44 (SOT307-2) packages
For more extensive description of the port pins see Chapter 10 “I/O facilities”.

SYMBOL	PIN		DESCRIPTION
	DIP40 VSO40	QFP44	
P1.0/$\overline{\text{INT2}}$	1	40	• **Port 1**: 8-bit bidirectional I/O port (P1.0 to P1.7). Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, Port 1 pins that are externally pulled LOW will source current (I_{IL}, see Chapter 21) due to the internal pull-ups. Port 1 output buffers can sink/source 4 LS TTL loads. • **Alternative functions:** – $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$ are external interrupt inputs.
P1.1/$\overline{\text{INT3}}$	2	41	
P1.2/$\overline{\text{INT4}}$	3	42	
P1.3/$\overline{\text{INT5}}$	4	43	
P1.4/$\overline{\text{INT6}}$	5	44	
P1.5/$\overline{\text{INT7}}$	6	1	
P1.6/$\overline{\text{INT8}}$	7	2	
P1.7/$\overline{\text{INT9}}$	8	3	
RST	9	4	**Reset**: a HIGH level on this pin for two machine cycles while the oscillator is running resets the device.
P3.0/RXD/data	10	5	• **Port 3:** 8-bit bidirectional I/O port (P3.0 to P3.7). Same characteristics as Port 1. • **Alternative functions:** – RXD/data is the serial port receiver data input (asynchronous) or data input/output (synchronous) – TXD/clock is the serial port receiver data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are external interrupts 0 and 1 – T0 and T1 are external inputs for timers 0 and 1 – $\overline{\text{WR}}$ is the external Data Memory write strobe – $\overline{\text{RD}}$ is the external Data Memory read strobe.
P3.1/TXD/clock	11	7	
P3.2/$\overline{\text{INT0}}$	12	8	
P3.3/$\overline{\text{INT1}}$	13	9	
P3.4/T0	14	10	
P3.5/T1	15	11	
P3.6/$\overline{\text{WR}}$	16	12	
P3.7/$\overline{\text{RD}}$	17	13	
XTAL2	18	14	**Crystal oscillator output**: output of the inverting amplifier of the oscillator. Left open when external clock is used.
XTAL1	19	15	**Crystal oscillator input**: input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
V_{SS}	20	16	Ground: circuit ground potential.
P2.0 to P2.7 A8 to A15	21 to 28	18 to 25	• **Port 2**: 8-bit bidirectional I/O port (P2.0 to P2.7) with internal pull-ups. Same characteristics as Port 1. • **High-order addressing**: Port 2 emits the high-order address byte (A8 to A15) during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pull-ups when emitting logic 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
$\overline{\text{PSEN}}$	29	26	**Program Store Enable**. Output read strobe to external Program Memory. When executing code out of external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle. However, during each access to external Data Memory two $\overline{\text{PSEN}}$ activations are skipped.

SYMBOL	PIN		DESCRIPTION
	DIP40 VSO40	QFP44	
ALE	30	27	**Address Latch Enable**. Output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of $\frac{1}{6} \times f_{osc}$, and may be used for external timing or clocking purposes (assuming MOVX instructions are not used).
$\overline{EA}$	31	29	**External Access**. When $\overline{EA}$ is held HIGH the CPU executes out of internal program memory (unless the program counter exceeds 0FFFH). Holding $\overline{EA}$ LOW forces the CPU to execute out of external memory regardless of the value of the program counter.
P0.7 to P0.0 AD7 to AD0	32 to 39	30 to 37	• **Port 0**: 8-bit open-drain bidirectional I/O port. As an open-drain output port it can sink 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in that state will function as high impedance inputs. • **Low-order addressing**: Port 0 is also the multiplexed low-order address and data bus during access to external memory. The strong internal pull-ups are used while emitting logic 1s within the low order address.
V_{DD}	40	38	Power supply.
n.c.	–	6, 17, 28, 39	Not connected.

8 FUNCTIONAL DESCRIPTION OVERVIEW

This chapter gives a brief overview of the device. The detailed functional description is in the following chapters as follows:

Chapter 9 “Memory organization”

Chapter 10 “I/O facilities”

Chapter 11 “Timers/event counters”

Chapter 12 “Reduced power modes”

Chapter 13 “Standard serial interface SIO0: UART”

Chapter 14 “Interrupt system”

Chapter 15 “Oscillator circuitry”

Chapter 16 “Reset”.

8.1 General

The P80CLx1 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of Program Memory and/or up to 64 kbytes of Data Memory.

The P80CLx1 contains 4 kbytes Program Memory (ROM; P80CL51 only); a static 128 bytes Data Memory (RAM); 32 I/O lines; two16-bit timer/event counters; a thirteen-source, two priority-level, nested interrupt structure and on-chip oscillator and timing circuit. A standard UART serial interface is also provided.

The device has two software-selectable modes of reduced activity for power reduction:

- **Idle mode**; freezes the CPU while allowing the timers, serial I/O and interrupt system to continue functioning.
- **Power-down mode**; saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

8.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency (f_{osc}) is 12 MHz.

9 MEMORY ORGANIZATION

The P80CLx1 has 4 kbytes of Program Memory (ROM; P80CL51 only) plus 128 bytes of Data Memory (RAM) on board.The device has separate address spaces for Program and Data Memory (see Fig.5). Using Port latches P0 and P2, the P80CLx1 can address a maximum of 64 kbytes of program memory and a maximum of 64 kbytes of data memory. The CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

9.1 Program Memory

The P80CL51 contains 4 kbytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 4 kbytes of Program Memory can be implemented in either on-chip ROM or external Program Memory.

If the $\overline{EA}$ pin is tied to V_{DD}, then Program Memory fetches from addresses 0000H to 0FFFH are directed to the internal ROM. Fetches from addresses 1000H to FFFFH are directed to external ROM. Program Counter values greater than 0FFFH are automatically addressed to external memory regardless of the state of the $\overline{EA}$ pin.

9.2 Data Memory

The P80CLx1 contains 128 bytes of internal RAM and 25 Special Function Registers (SFR). The memory map (Fig.5) shows the internal Data Memory space divided into the lower 128, the upper 128, and the SFR space. The lower 128 bytes of the internal RAM are organized as mapped in Fig.6. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions refer to these registers within a register bank as R0 through R7. Two bits in the Program Status Word select which register bank is in use. The next 16 bytes above the register banks form a block of bit-addressable memory space. The 128 bits in this area can be directly addressed by the single-bit manipulation instructions. The remaining registers (30H to 7FH) are directly and indirectly byte addressable.

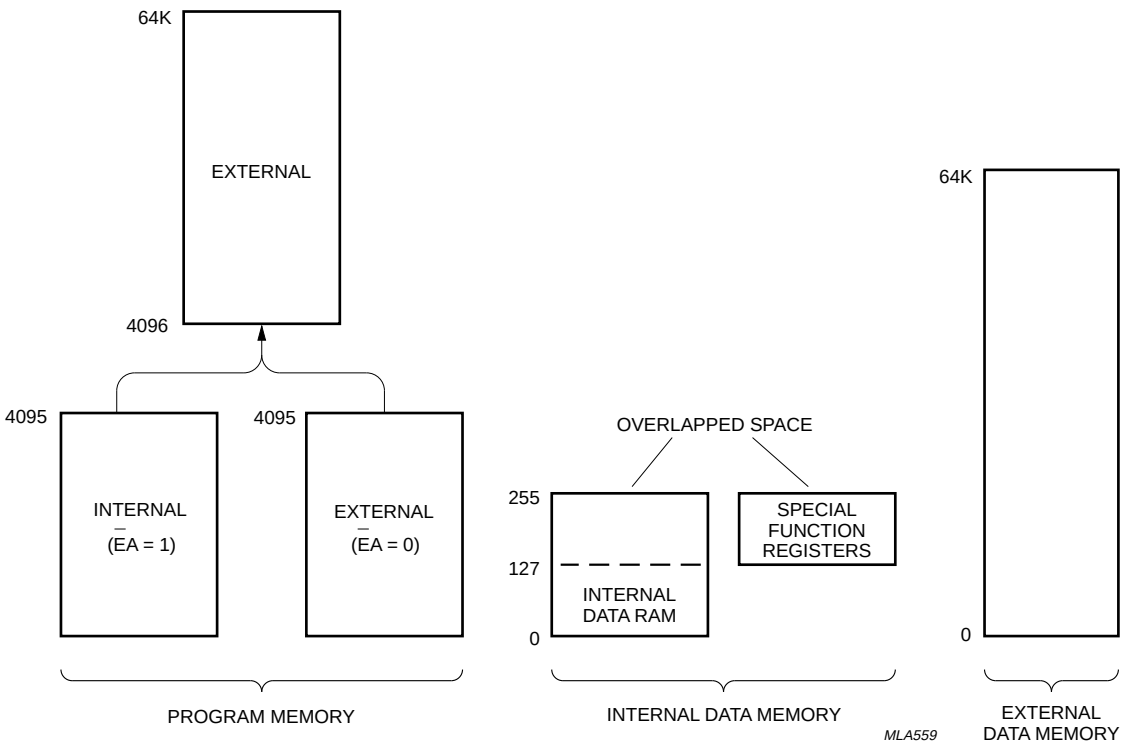


Fig.5 Memory map.

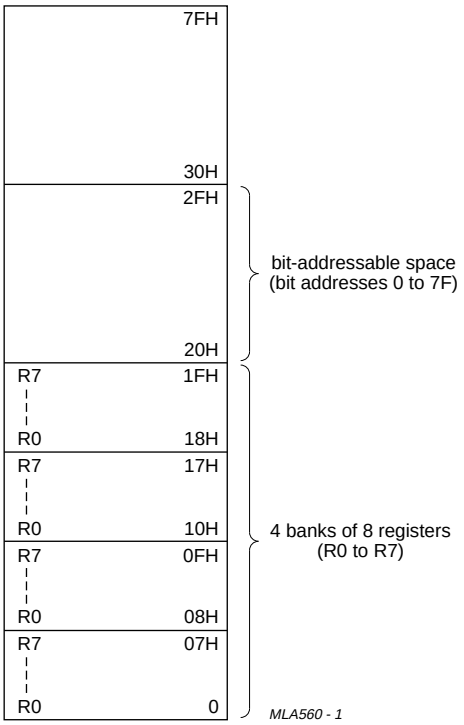


Fig.6 The lower 128 bytes of internal RAM.

9.3 Special Function Registers (SFRs)

The upper 128 bytes are the address locations of the SFRs. Figure 7 shows the SFR space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 directly addressable locations in the SFR address space (SFRs with addresses divisible by eight).

9.4 Addressing

The P8xCL410 has five methods for addressing source operands:

- Register
- Direct
- Register-indirect
- Immediate
- Base-register plus index-register-indirect.

The first three methods can be used for addressing destination operands. Most instructions have a 'destination/source' field that specifies the data type, addressing methods and operands involved.
For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or register-indirect
- Internal RAM (128 bytes) through direct or register-indirect
- Special Function Registers through direct
- External data memory through register-indirect
- Program Memory look-up tables through base-register plus index-register-indirect.

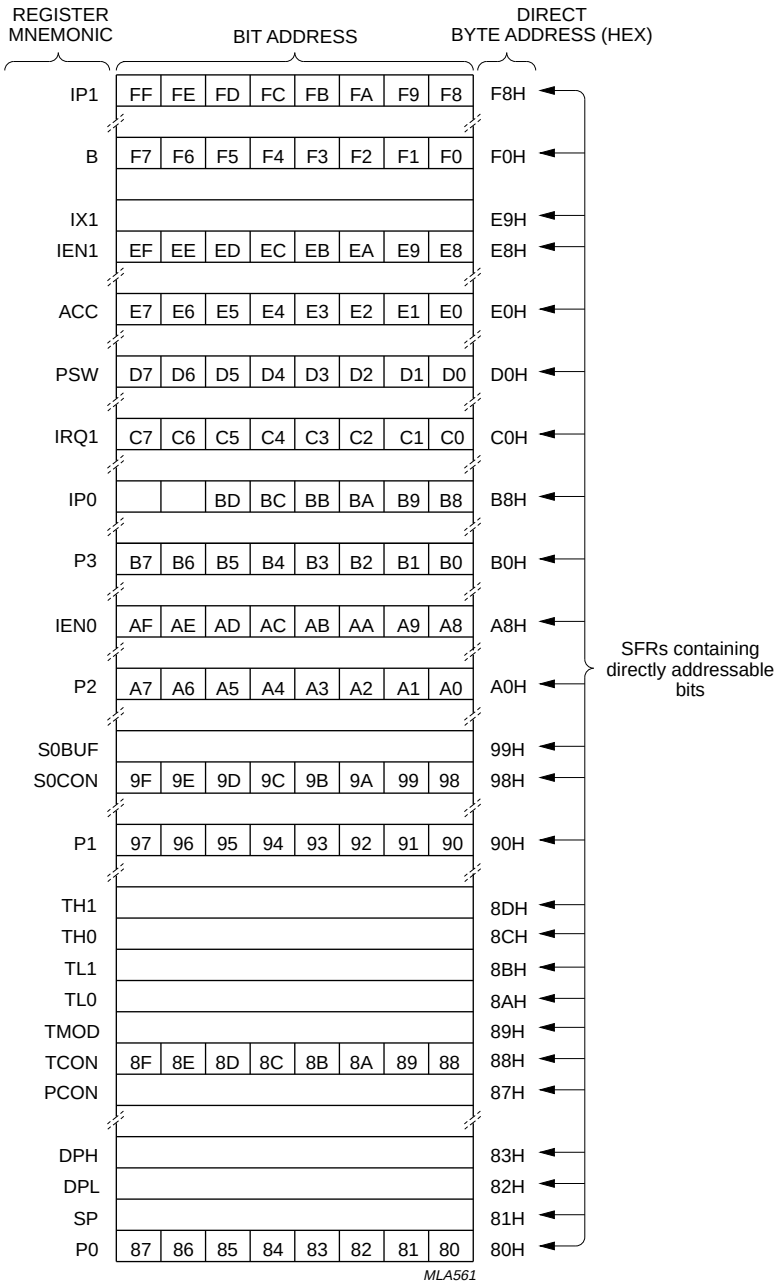


Fig.7 Special Function Register memory map.

10 I/O FACILITIES

10.1 Ports

The P80CLx1 has 32 I/O lines treated as 32 individually addressable bits or as four parallel 8-bit addressable ports. Ports 0, 1, 2 and 3 perform the alternative functions detailed below. To enable a port pin alternate function, the port bit latch in its SFR must contain a logic 1.

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Provides the inputs for the external interrupts $\overline{INT2}$ to $\overline{INT9}$.

Port 2 Provides the high-order address when expanding the device with external Program or Data Memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs: $\overline{INT1}$ and $\overline{INT0}$
- Timer/counter inputs: T1 and T0
- Control signals to read and write to external memories: $\overline{RD}$ and $\overline{WR}$
- UART input and output: RXD/data and TXD/clock.

Each port consists of a latch (SFRs P0 to P3), an output driver and input buffer. Ports 1, 2, and 3 have internal pull-ups Figure 8(a) shows that the strong transistor ‘p1’ is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on ‘p3’ (a weak pull-up) through the inverter. This inverter and ‘p3’ form a latch which holds the logic 1. In Port 0 the pull-up ‘p1’ is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 0 bit latch leaves both output transistors switched off so that the pin can be used as a high-impedance input.

10.2 Port options

The pins of port 1, port 2 and port 3 may be individually configured with one of the following options. These options are also shown in Fig.8.

Option 1 **Standard Port**; quasi-bidirectional I/O with pull-up. The strong booster pull-up ‘p1’ is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch; Fig.8(a).

Option 2 **Open-drain**; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; see Fig.8(b).

Option 3 **Push-pull**; output with drive capability in both polarities. Under this option, pins can only be used as outputs; see Fig.8(c).

10.3 Port 0 options

The definition of port options for Port 0 is slightly different. Two cases are considered. First, access to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary) and second, I/O accesses.

10.3.1 External memory accesses

Option 1 True logic 0 and logic 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

10.3.2 I/O Accesses

Option 1 When writing a logic 1 to the port latch, the strong pull-up ‘p1’ will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open-drain; quasi-directional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.8(b).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs. See Fig.8(c).

10.4 SET/RESET options

Individual mask selection of the post-reset state is available with any of the above pins. The required selection is made by appending ‘S’ or ‘R’ to Options 1, 2, or 3 above.

Option R RESET, at reset this pin will be initialized LOW.

Option S SET, at reset this pin will be initialized HIGH.

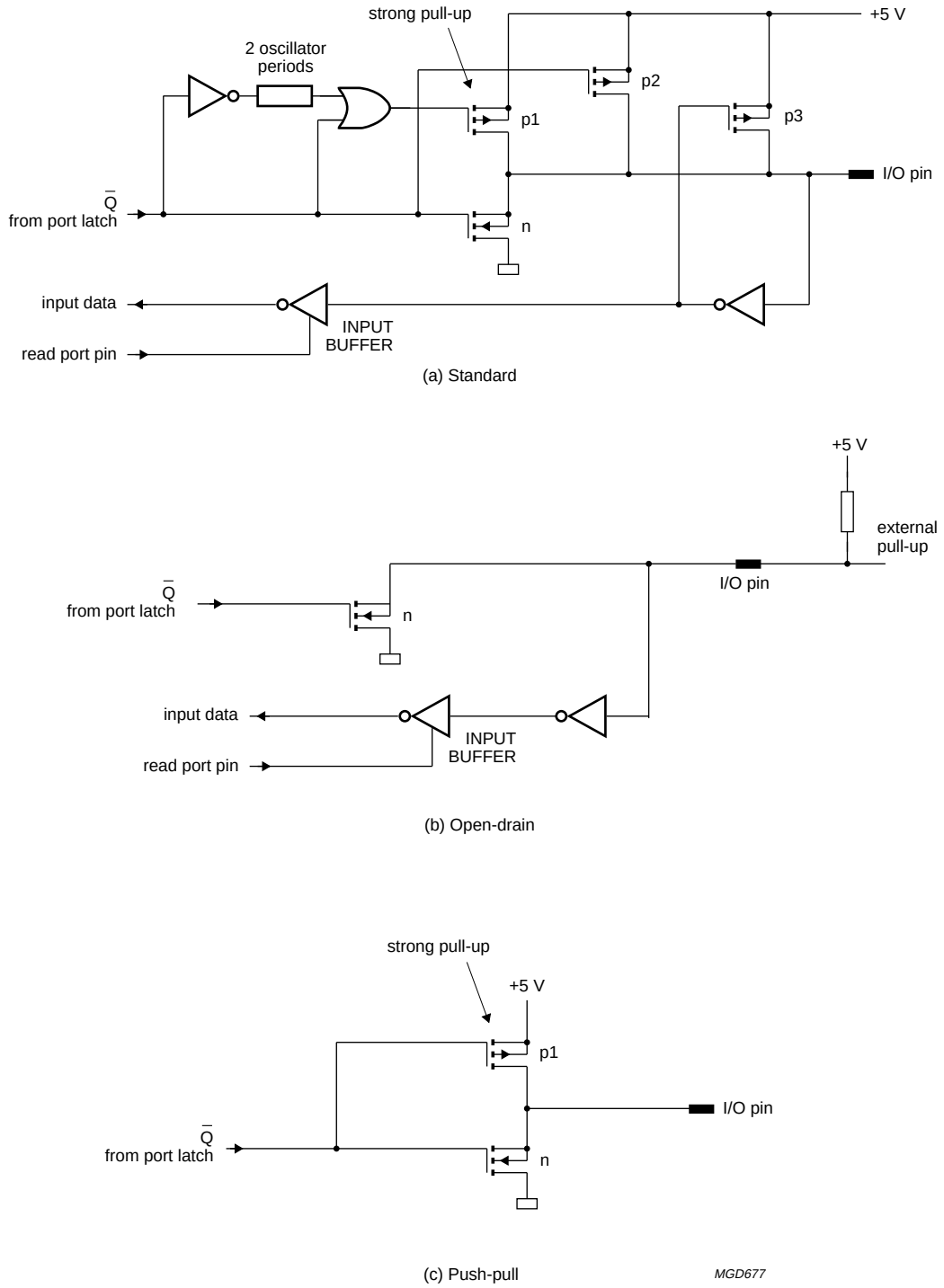


Fig.8 Port configuration options.

11 TIMERS/EVENT COUNTERS

The P80CLx1 contains two16-bit timer/event counter registers; Timer 0 and Timer 1, which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

In the 'Timer' operating mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $1/12 \times f_{osc}$.

In the 'Counter' operating mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $1/24 \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

12 REDUCED POWER MODES

There are two software selectable modes of reduced activity for further power reduction: Idle and Power-down.

12.1 Idle mode

Idle mode operation permits the external interrupts, UART, and timer blocks to continue to function while the clock to the CPU is halted.

Idle mode is entered by setting the IDL bit in the Power Control Register (PCON.0, see Table 2). The instruction that sets IDL is the last instruction executed in the normal operating mode before the Idle mode is activated.

Once in Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 3.

The following functions remain active during the Idle mode:

- Timer 0 and Timer 1
- UART
- External interrupt.

These functions may generate an interrupt or reset; thus ending the Idle mode.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause IDL (PCON.0) to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 (PCON.2) and GF1 (PCON.3) may be used to determine whether the interrupt was received during normal execution or during the Idle mode.
   For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

12.2 Power-down mode

Operation in Power-down mode freezes the oscillator. The internal connections which link both Idle and Power-down signals to the clock generation circuit are shown in Fig.9.

Power-down mode is entered by setting the PD bit in the Power Control Register (PCON.1, see Table 2).
The instruction that sets PD is the last executed prior to going into the Power-down mode.

Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and $\overline{PSEN}$ are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

12.3 Wake-up from Power-down mode

When in Power-down mode the controller can be woken-up with either the external interrupts $\overline{INT2}$ to $\overline{INT9}$, or a reset operation. The wake-up operation has two basic approaches as explained in Section 12.3.1; 12.3.2 and illustrated in Fig.10.

12.3.1 WAKE-UP USING $\overline{INT2}$ TO $\overline{INT9}$

If any of the interrupts $\overline{INT2}$ to $\overline{INT9}$ are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

12.3.2 WAKE-UP USING RST

To wake-up the P80CLx1, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted.

12.4 Power Control Register (PCON)

See Tables 2 and 3. Idle and Power-down modes are activated by software using this SFR. PCON is not bit-addressable.

12.5 Status of external pins

The status of the external pins during Idle and Power-down mode is shown in Table 4. If the Power-down mode is activated whilst accessing external Program Memory, the port data that is held in the Special Function Register P2 is restored to Port 2.

If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor ‘p1’; see Fig.8(a).

Table 2 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	–	GF1	GF0	PD	IDL

Table 3 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
7	SMOD	**Double Baud rate bit;** see description of UART
6, 5, 4	–	reserved
3 and 2	GF1 and GF0	**General purpose flag bits**
1	PD	**Power-down bit;** setting this bit activates the Power-down mode
0	IDL	**Idle mode bit;** setting this bit activates the Idle mode

Table 4 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4
Idle	internal	1	1	port data	port data	port data	port data	port data
	external	1	1	floating	port data	address	port data	port data
Power-down	internal	0	0	port data	port data	port data	port data	port data
	external	0	0	floating	port data	port data	port data	port data

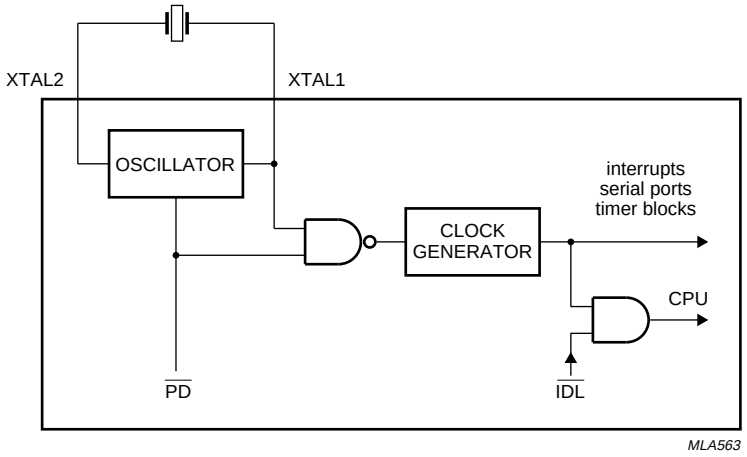


Fig.9 Internal clock control in Idle and Power-down mode.

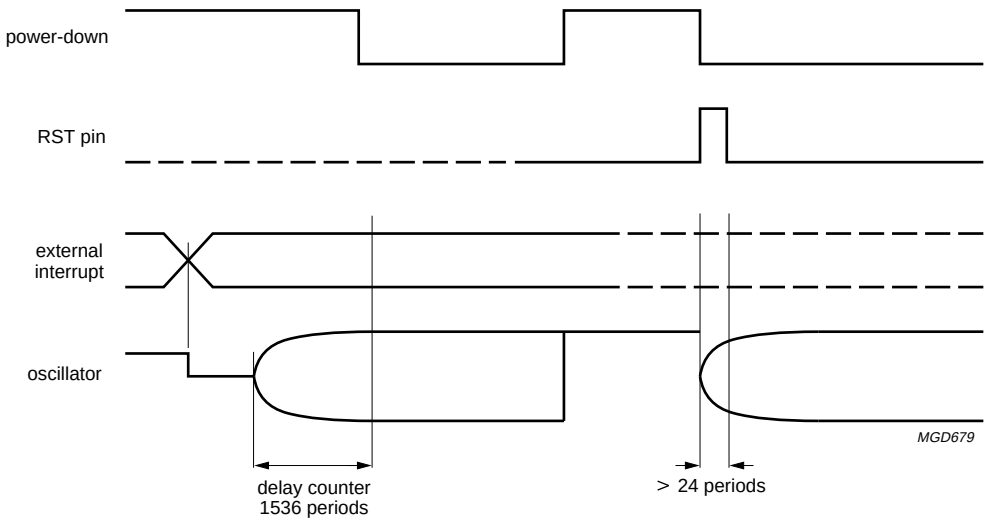


Fig.10 Wake-up operation.

13 STANDARD SERIAL INTERFACE SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. Eight bits are transmitted/received (LSB first). The baud rate is fixed at $\frac{1}{12} \times f_{osc}$.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of a logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $\frac{1}{32}$ or $\frac{1}{64} \times f_{osc}$.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

13.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

13.2 Serial Port Control and Status Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 5 Serial Port Control Register (address 98H)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Table 6 Description of S0CON bits

BIT	SYMBOL	DESCRIPTION
7	SM0	These bits are used to select the serial port mode; see Table 7.
6	SM1	
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be a logic 0.
4	REN	Enables serial reception and is set by software to enable reception, and cleared by software to disable reception.
3	TB8	Is the 9th data bit that will be transmitted in Modes 2 and 3; set or cleared by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received; in Mode 0, RB8 is not used.
1	TI	**The transmit interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
0	RI	**The receive interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (except see SM2). Must be cleared by software.

Table 7 Selection of the serial port modes

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	Mode 0	Shift register	$^1/_{12} \times f_{osc}$
0	1	Mode 1	8-bit UART	variable
1	0	Mode 2	9-bit UART	$^1/_{32}$ or $^1/_{64} \times f_{osc}$
1	1	Mode 3	9-bit UART	variable

13.3 Baud rates

The baud rate in Mode 0 is fixed and may be calculated as:

$$\text{Baud Rate} = \frac{f_{osc}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON and may be calculated as:

$$\text{Baud Rate} = \frac{2^{SMOD}}{64} \times f_{osc}$$

- If SMOD = 0 (value on reset), the baud rate is $1/64 \times f_{osc}$
- If SMOD = 1, the baud rate is $1/32 \times f_{osc}$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

13.3.1 Using Timer 1 to generate baud rates

When Timer 1 is used as the Baud Rate Generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD bit as follows:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 Overflow Rate.}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either ‘timer’ or ‘counter’ operation in any of its 3 running modes. In most typical applications, it is configured for ‘timer’ operation, in the Auto-reload mode (high nibble of TMOD = 0010B). In this case the baud rate is given by the formula:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{f_{osc}}{\{12 \times (256 - TH1)\}}$$

By configuring Timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rates can be achieved. Table 8 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 8 Commonly used baud rates generated by Timer 1

BAUD RATE (kbits/s)	f_{osc} (MHz)	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
1330.0(1)	16.000	X(2)	X	X	X
500.0(3)	16.000	1	X	X	X
83.3(4)	16.000	1	0	Mode 2	FFH
19.2	11.059	1	0	Mode 2	FDH
9.6	11.059	0	0	Mode 2	FDH
4.8	11.059	0	0	Mode 2	FAH
2.4	11.059	0	0	Mode 2	F4H
1.2	11.059	0	0	Mode 2	E8H
137.5	11.986	0	0	Mode 2	1DH
110.0	6.000	0	0	Mode 2	72H
110.0	12.000	0	0	Mode 1	FEEBH

Notes

1. Maximum in Mode 0.
2. X = don’t care.
3. Maximum in Mode 2.
4. Maximum in Modes 1 and 3.

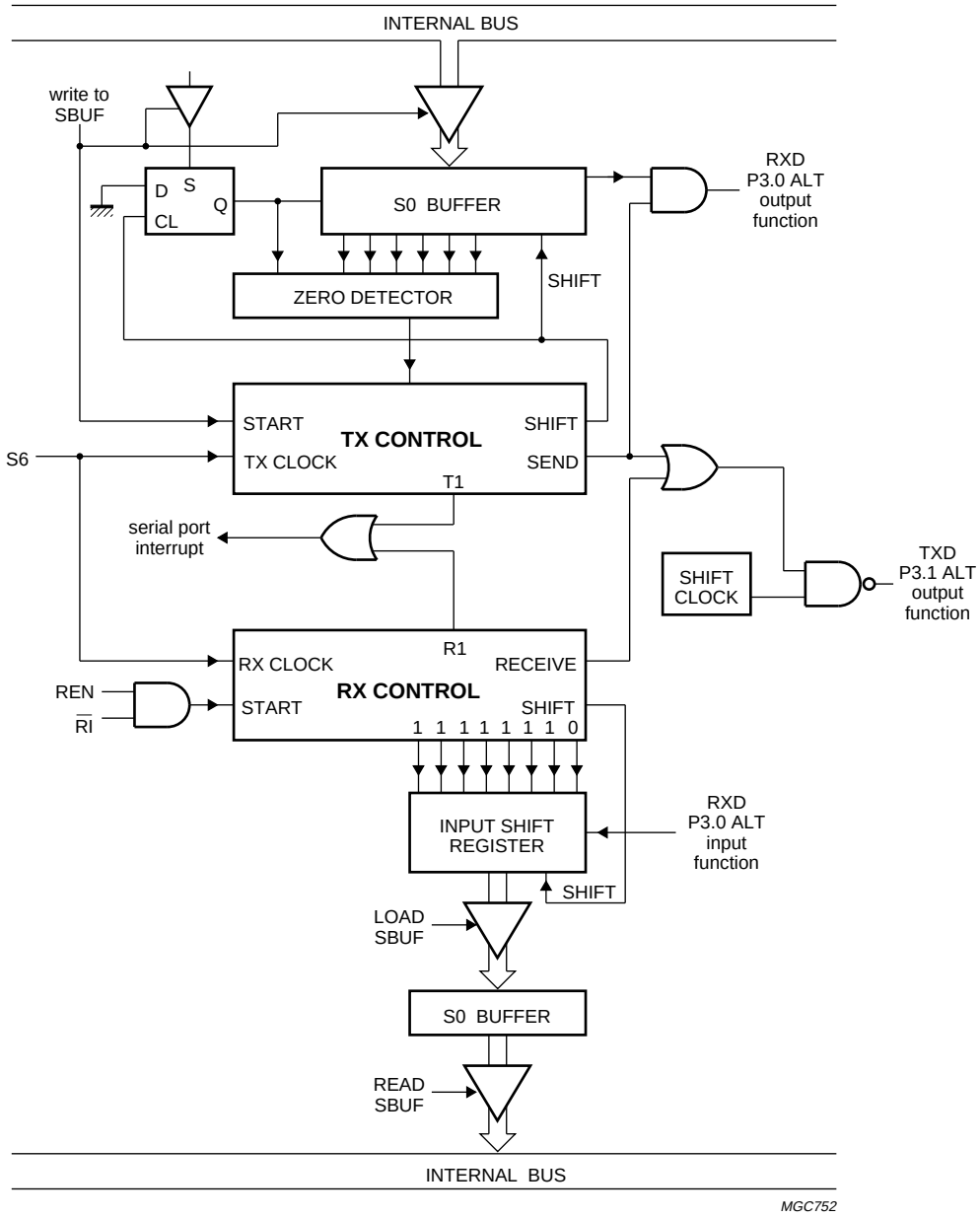


Fig.11 Serial port Mode 0.

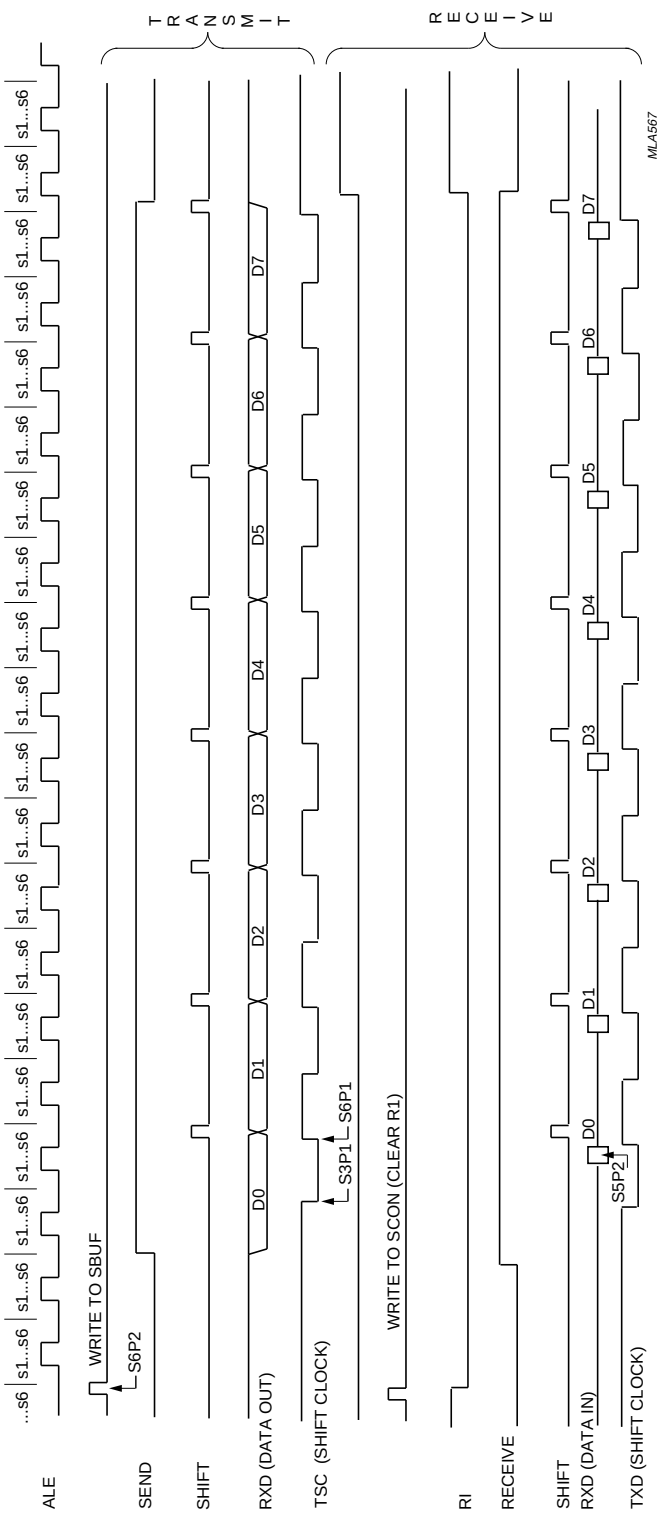


Fig.12 Serial port Mode 0 timing.

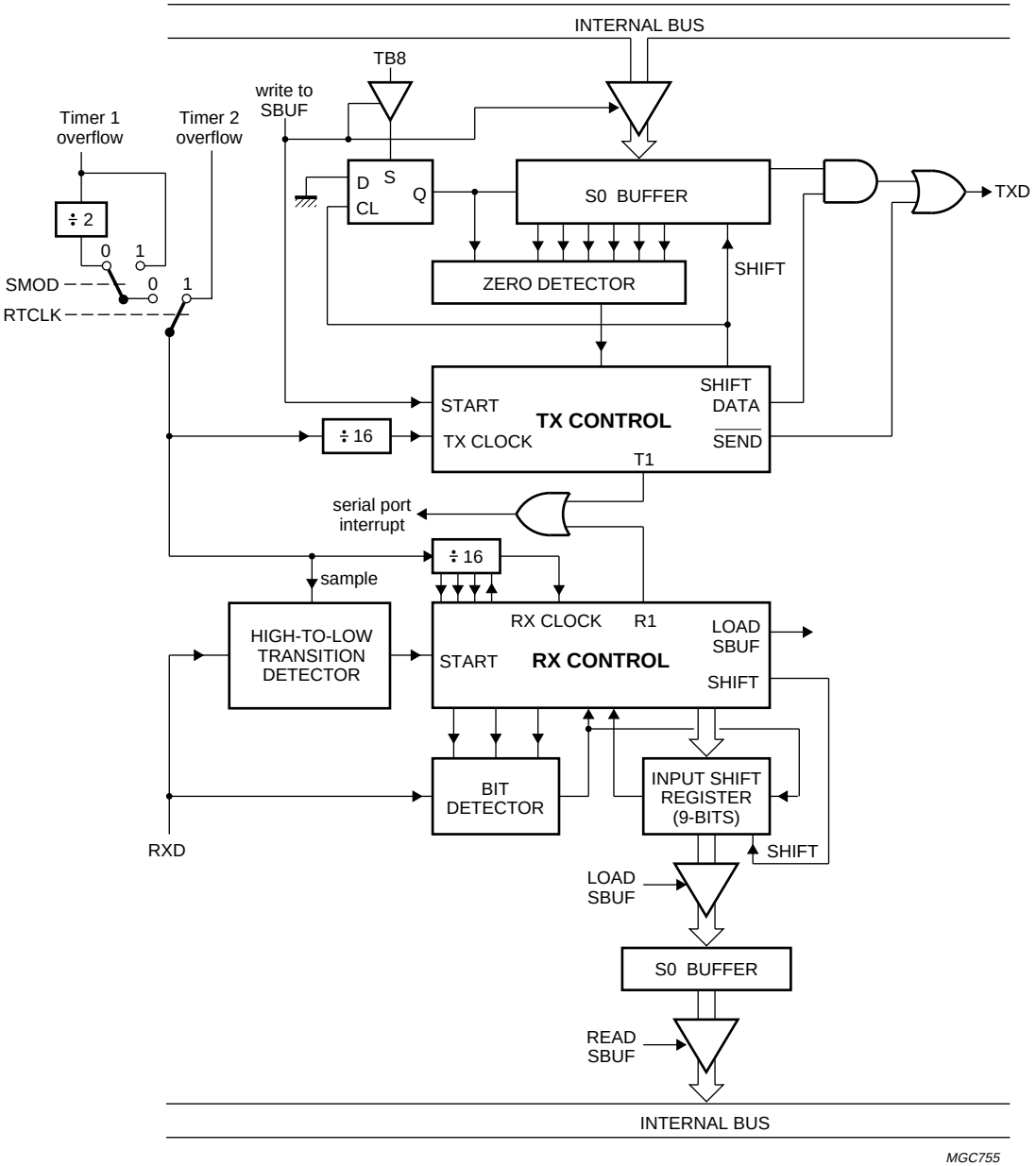


Fig.13 Serial port Mode 1.

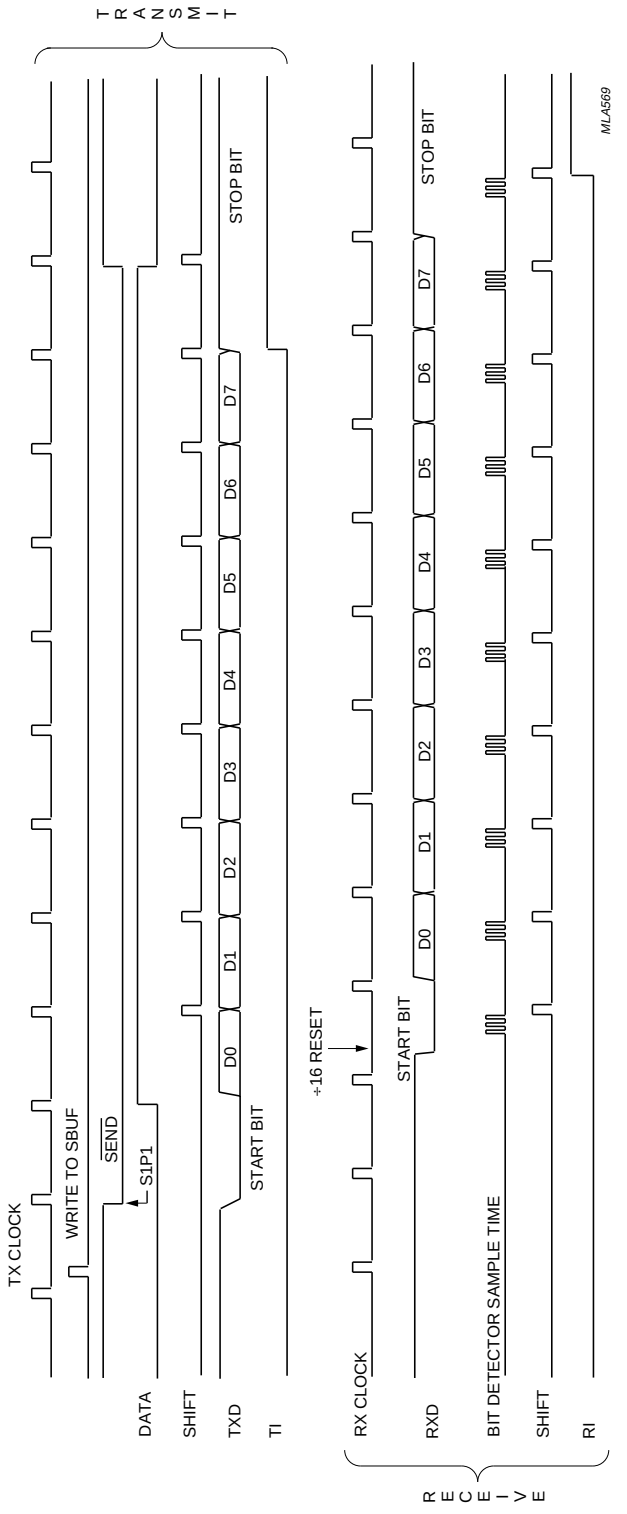


Fig.14 Serial port Mode 1 timing.

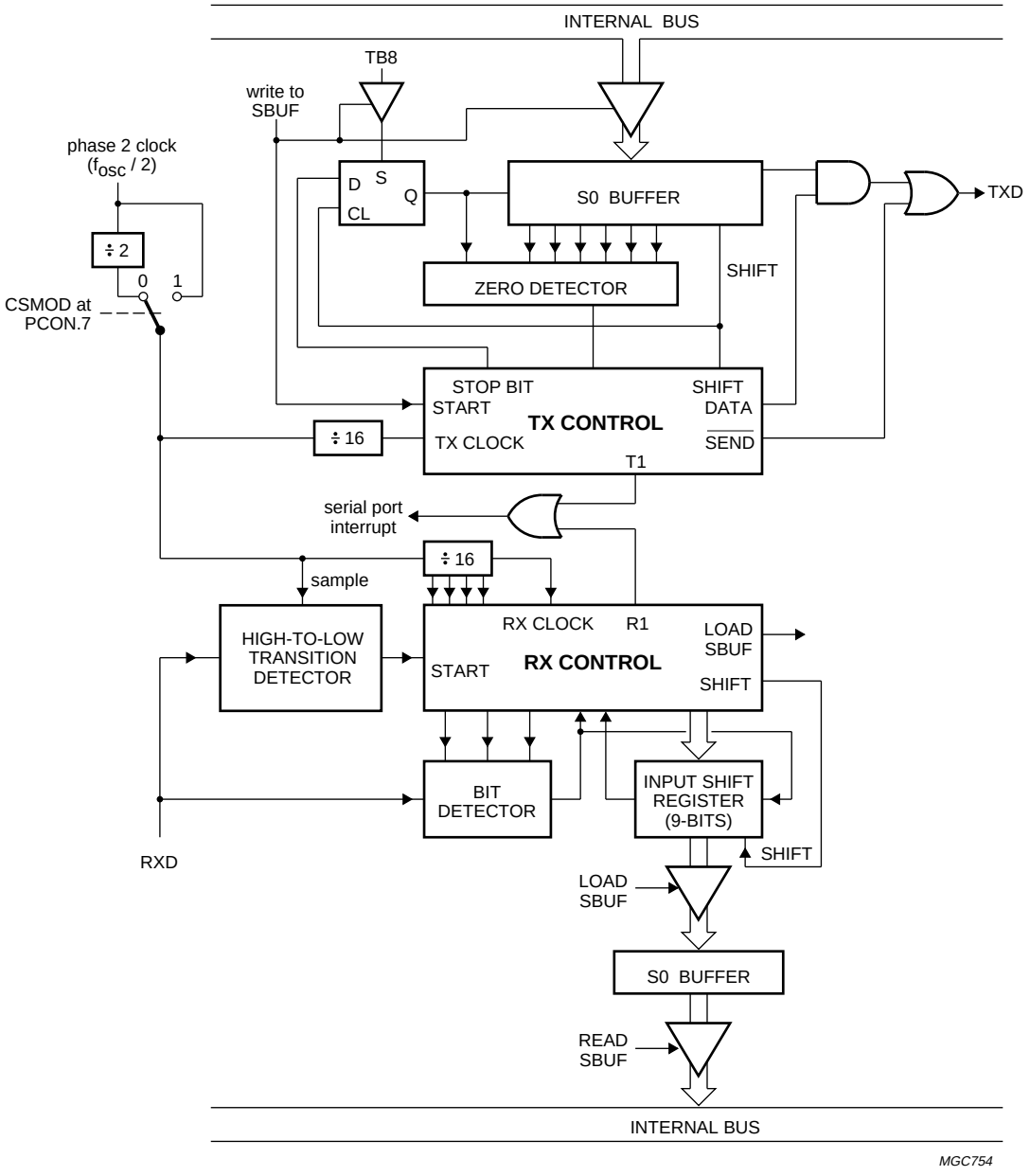


Fig.15 Serial port Mode 2.

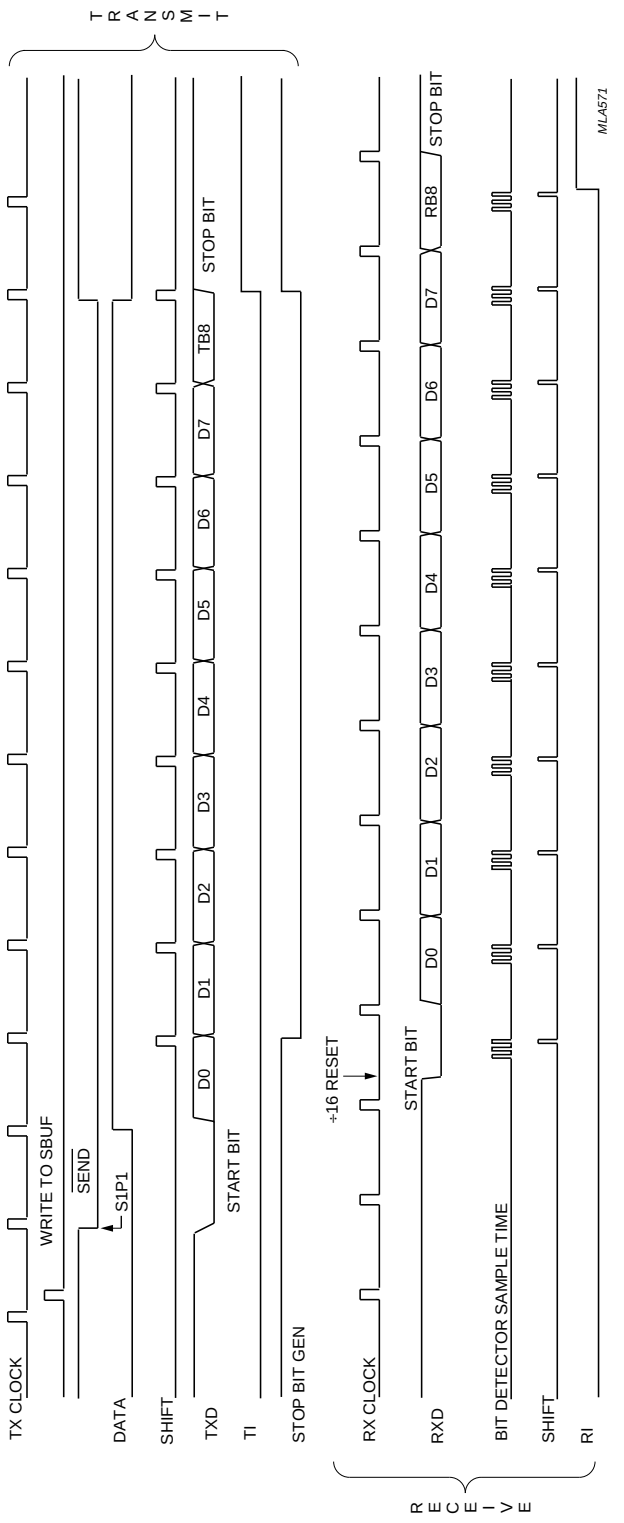


Fig.16 Serial port Mode 2 timing.

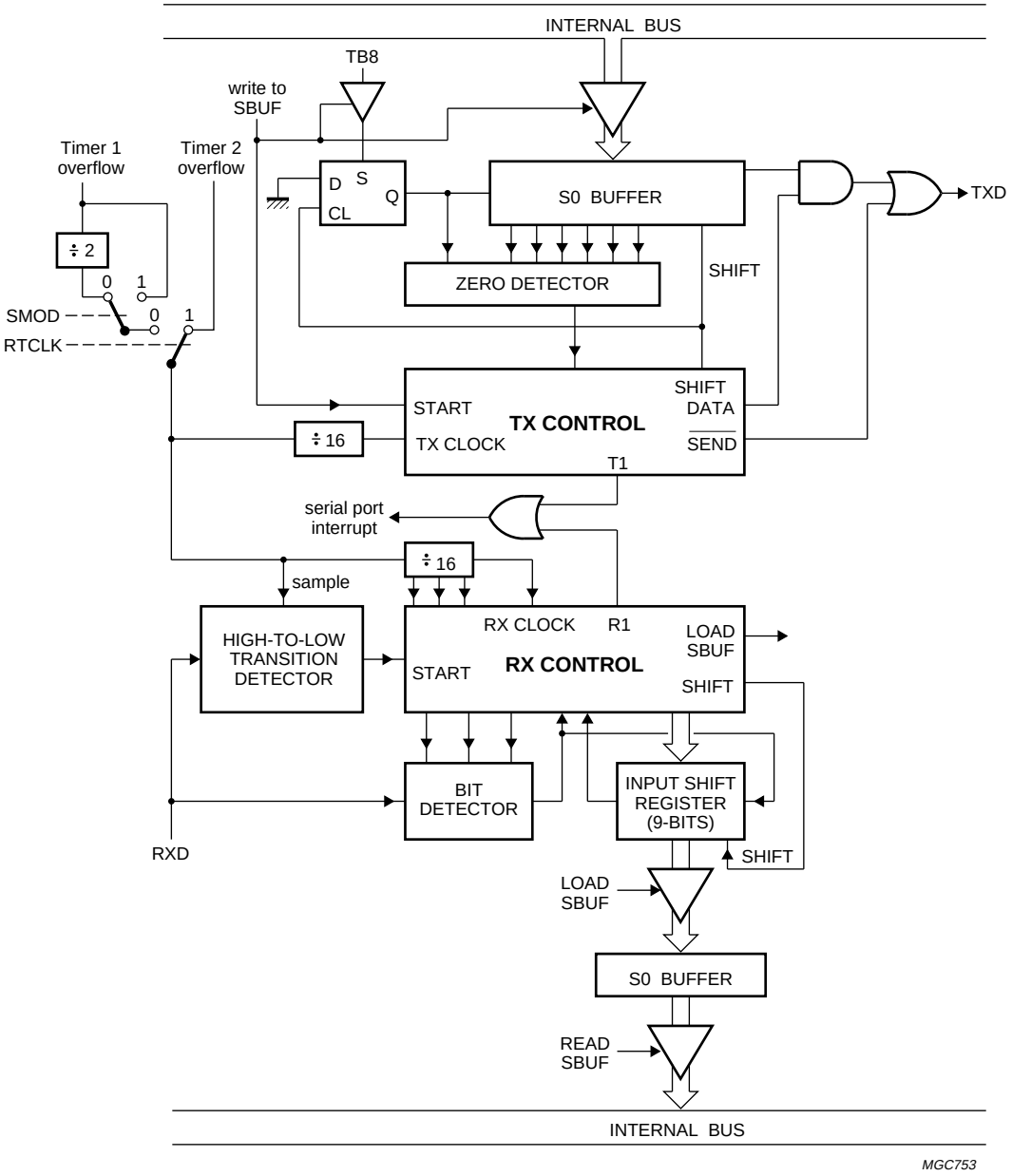


Fig.17 Serial port Mode 3.

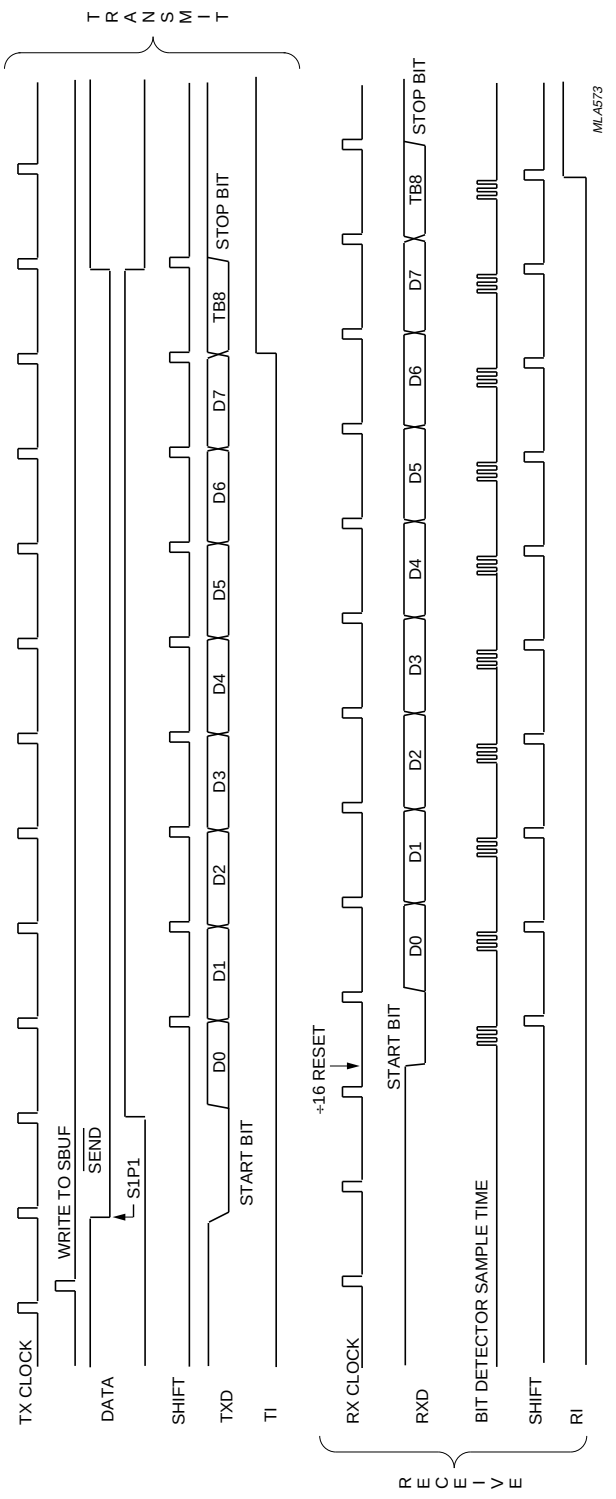


Fig.18 Serial port Mode 3 timing.

14 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU at unpredictable times. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The system is shown in Fig.19. The P80CLx1 acknowledges interrupt requests from thirteen sources as follows:

- $\overline{\text{INT0}}$ to $\overline{\text{INT9}}$
- Timer 0 and Timer 1
- UART.

Each interrupt vectors to a separate location in Program Memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (IEN0 and IEN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled. Figure 19 shows the interrupt system.

14.1 External interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$

Port 1 lines serve an alternative purpose as eight additional interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT9}}$. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. Figure 20 shows the external interrupt configuration.

14.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If a low priority interrupt is received simultaneously with a high priority interrupt, the high priority interrupt will be dealt with first.

If interrupts of the same priority are requested simultaneously, the processor will branch to the interrupt polled first, according to the sequence shown in Table 9 and in Fig.19. The ‘vector address’ is the ROM location where the appropriate interrupt service routine starts.

Table 9 Interrupt vector polling sequence

SYMBOL	VECTOR ADDRESS (HEX)	SOURCE
X0 (first)	0003	External 0
S0	002B	UART
X5	0053	External 5
T0	000B	Timer 0
X6	005B	External 6
X1	0013	External 1
X2	003B	External 2
X7	0063	External 7
T1	001B	Timer 1
X3	0043	External 3
X8	006B	External 8
X4	004B	External 4
X9 (last)	0073	External 9

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

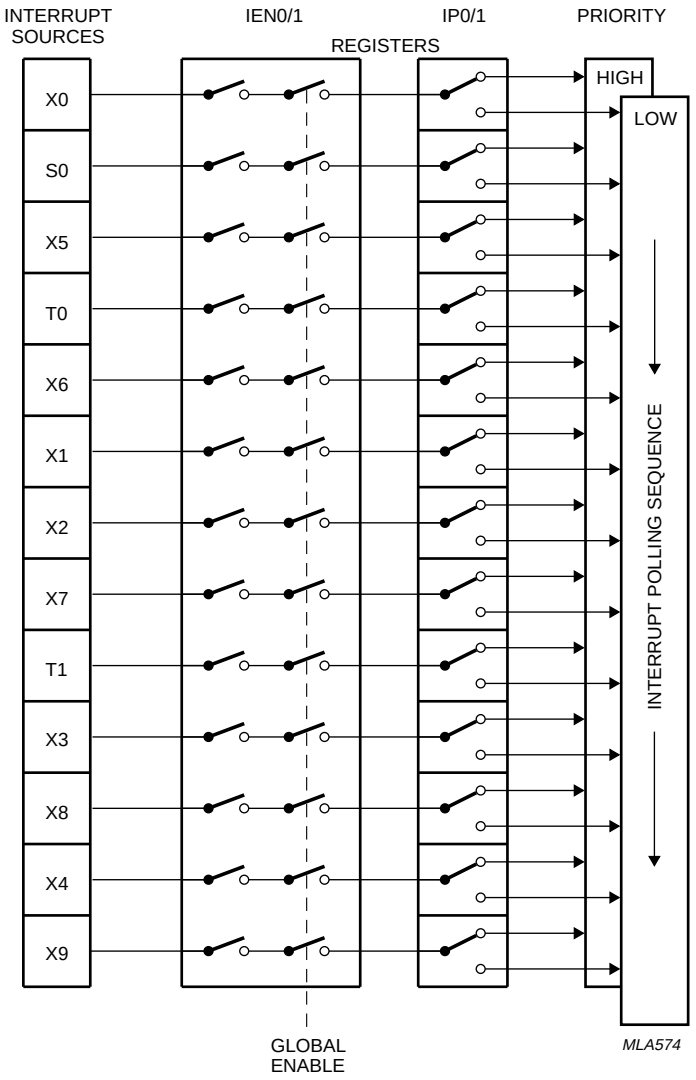


Fig.19 Interrupt system.

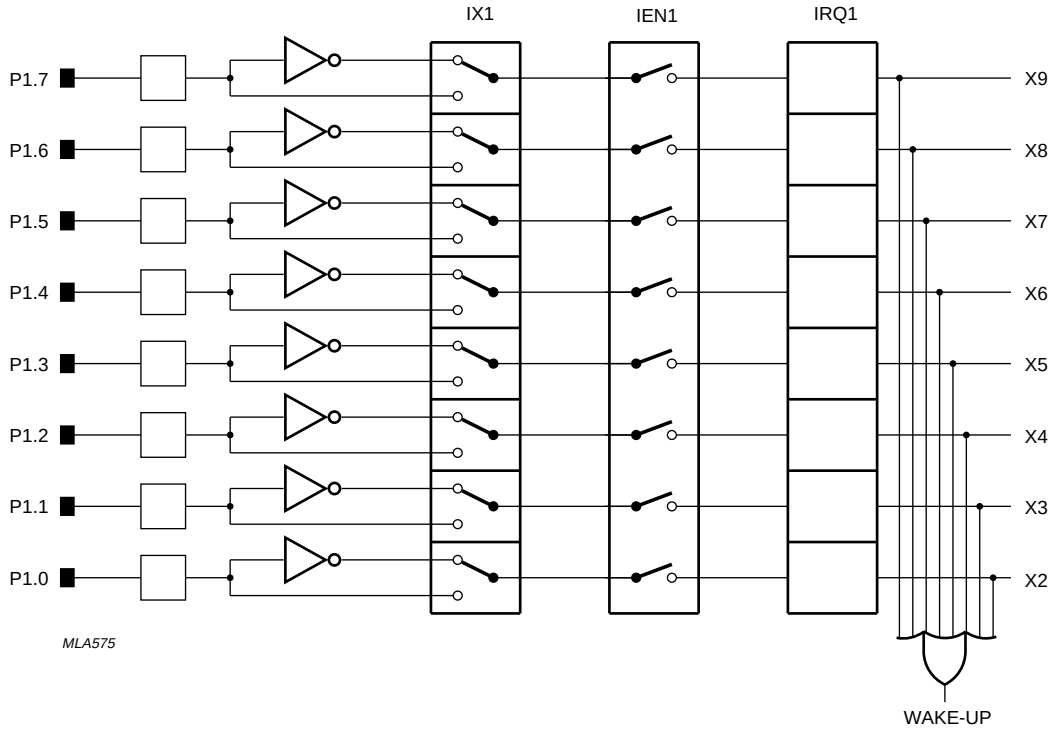


Fig.20 External interrupt configuration.

14.3 Interrupt registers

The registers used in the interrupt system are listed in Table 10. Tables 11 to 22 describe the contents of these registers.

Table 10 Special Function Registers related to the interrupt system

ADDRESS	REGISTER	DESCRIPTION
A8H	IEN0	Interrupt Enable Register
E8H	IEN1	Interrupt Enable Register ($\overline{INT2}$ to $\overline{INT9}$)
B8H	IP0	Interrupt Priority Register
F8H	IP1	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT9}$
E9H	IX1	Interrupt Polarity Register
C0H	IRQ1	Interrupt Request Flag Register

14.3.1 Interrupt Enable Register (IEN0)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 11 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	–	–	ES0	ET1	EX1	ET0	EX0

Table 12 Description of IEN0 bits

BIT	SYMBOL	DESCRIPTION
7	EA	general enable/disable control. If EA = 0, no interrupt is enabled; if EA = 1, any individually enabled interrupt will be accepted
6	–	reserved
5	–	reserved
4	ES0	enable UART SIO interrupt
3	ET1	enable Timer 1 interrupt (T1)
2	EX1	enable external interrupt 1
1	ET0	enable Timer 0 interrupt (T0)
0	EX0	enable external interrupt 0

14.3.2 Interrupt Enable Register (IEN1)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 13 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 14 Description of IEN1 bits

BIT	SYMBOL	DESCRIPTION
7	EX9	enable external interrupt 9
6	EX8	enable external interrupt 8
5	EX7	enable external interrupt 7
4	EX6	enable external interrupt 6
3	EX5	enable external interrupt 5
2	EX4	enable external interrupt 4
1	EX3	enable external interrupt 3
0	EX2	enable external interrupt 2

14.3.3 Interrupt Priority Register (IP0)

Bit values: 0 = low priority; 1 = high priority.

Table 15 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	–	–	PS0	PT1	PX1	PT0	PX0

Table 16 Description of IP0 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	–	reserved
5	–	reserved
4	PS0	UART SIO interrupt priority level
3	PT1	Timer 1 interrupt priority level
2	PX1	external interrupt 1 priority level
1	PT0	Timer 0 interrupt priority level
0	PX0	external interrupt 0 priority level

14.3.4 Interrupt Priority Register (IP1)

Bit values: 0 = low priority; 1 = high priority.

Table 17 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 18 Description of IP1 bits

BIT	SYMBOL	DESCRIPTION
7	PX9	external interrupt 9 priority level
6	PX8	external interrupt 8 priority level
5	PX7	external interrupt 7 priority level
4	PX6	external interrupt 6 priority level
3	PX5	external interrupt 5 priority level

BIT	SYMBOL	DESCRIPTION
2	PX4	external interrupt 4 priority level
1	PX3	external interrupt 3 priority level
0	PX2	external interrupt 2 priority level

14.3.5 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 19 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 20 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
7	IL9	external interrupt 9 polarity level
6	IL8	external interrupt 8 polarity level
5	IL7	external interrupt 7 polarity level
4	IL6	external interrupt 6 polarity level
3	IL5	external interrupt 5 polarity level
2	IL4	external interrupt 4 polarity level
1	IL3	external interrupt 3 polarity level
0	IL2	external interrupt 2 polarity level

14.3.6 Interrupt Request Flag Register (IRQ1)

Table 21 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 22 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
7	IQ9	external interrupt 9 request flag
6	IQ8	external interrupt 8 request flag
5	IQ7	external interrupt 7 request flag
4	IQ6	external interrupt 6 request flag
3	IQ5	external interrupt 5 request flag
2	IQ4	external interrupt 4 request flag
1	IQ3	external interrupt 3 request flag
0	IQ2	external interrupt 2 request flag

15 OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the P80CLx1 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.22. For operation as a standard quartz oscillator, no external components are needed, except for the 32 kHz option. When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 23 and Fig.21).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator inverter is switched off to ensure no current will flow regardless of the voltage at XTAL1, for configurations (a), (b), (c), (d), (e) and (g) of Fig.21.

To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.21(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 23 and shown in Fig.21. The required option should be stated when ordering.

Table 23 Oscillator options

OPTION	APPLICATION
Oscillator 1	for 32 kHz clock applications with external trimmer for frequency adjustment; a 4.7 MΩ bias resistor is needed for use in parallel with the crystal; see Fig.21(c)
Oscillator 2	low-power, low-frequency operations using LC components; see Fig.21(e)
Oscillator 3	medium frequency range applications
Oscillator 4	high frequency range applications
RC oscillator	RC oscillator configuration; see Figs 21(g) and 23

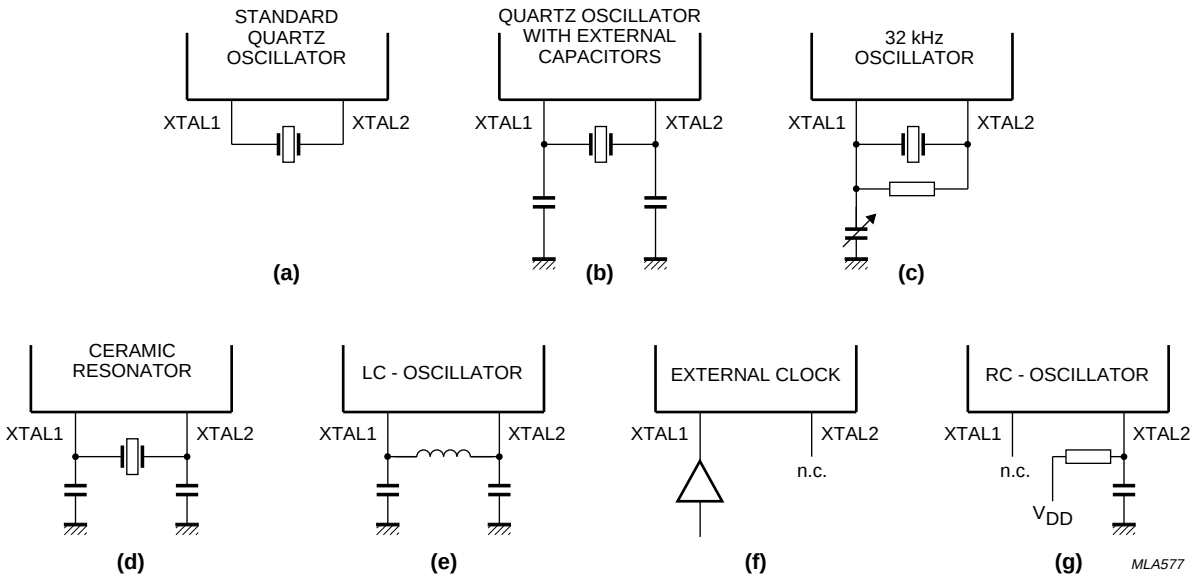


Fig.21 Oscillator configurations.

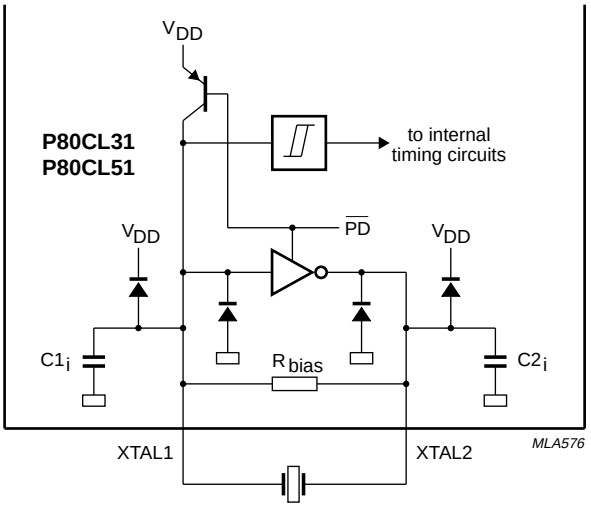
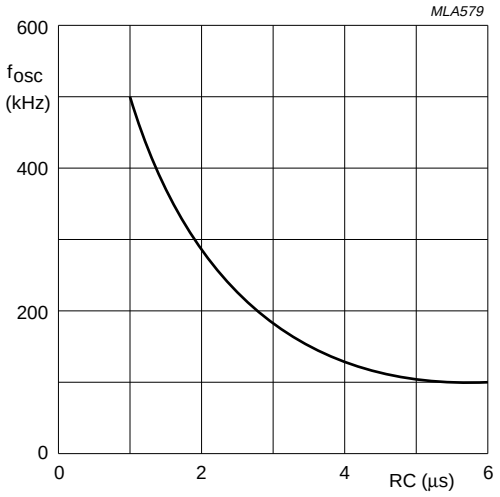


Fig.22 Standard oscillator.



RC oscillator frequency is externally adjustable; 100 kHz ≤ f_{osc} ≤ 500 kHz.

Fig.23 RC oscillator frequency as a function of RC.

Table 24 Oscillator type selection guide

RESONATOR	FREQUENCY (MHz)	OPTION (see Table 23)	C1 EXT. (pF)		C2 EXT. (pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Oscillator 1	0	0	5	15	15 kΩ(1)
	1.0	Oscillator 2	0	30	0	30	600 Ω
	3.58		0	15	0	15	100 Ω
	4.0		0	20	0	20	75 Ω
	6.0	Oscillator 3	0	10	0	10	60 Ω
	10.0	Oscillator 4	0	15	0	15	60 Ω
	12.0		0	10	0	10	40Ω
	16.0		0	15	0	15	20 Ω
PXE	0.455	Oscillator 2	40	50	40	50	10 Ω
	1.0		15	50	15	50	100 Ω
	3.58		0	40	0	40	10 Ω
	4.0		0	40	0	40	10 Ω
	6.0		0	20	0	20	5 Ω
	10.0	Oscillator 3	0	15	0	15	6 Ω
	12.0	Oscillator 4	10	40	10	40	6 Ω
LC	–	Oscillator 2	20	90	20	90	10 μH = 1 Ω 100 μH = 5 Ω 1 mH = 75 Ω

Note

1. 32 kHz quartz crystals with a series resistance >15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5 V.

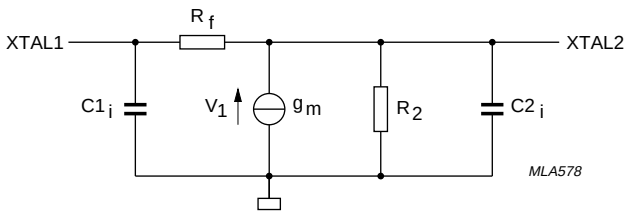


Fig.24 Oscillator equivalent circuit diagram.

Table 25 Oscillator equivalent circuit parameters

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

SYMBOL	PARAMETER	OPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
g_m	transconductance	Oscillator 1; 32 kHz	T_{amb} = +25 °C; V_{DD} = 4.5 V	–	15	–	µS
		Oscillator 2		200	600	1000	µS
		Oscillator 3		400	1500	4000	µS
		Oscillator 4		1000	4000	10000	µS
$C1_i$	input capacitance	Oscillator 1; 32 kHz		–	3.0	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
$C2_i$	output capacitance	Oscillator 1; 32 kHz		–	23	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
R2	output resistance	Oscillator 1; 32 kHz		–	3800	–	kΩ
		Oscillator 2		–	65	–	kΩ
		Oscillator 3		–	18	–	kΩ
		Oscillator 4		–	5.0	–	kΩ

16 RESET

To initialize the P80CLx1 a reset is performed by either of three methods:

- Applying an external signal to the RST pin
- Via Power-on-reset circuitry.

A reset leaves the internal registers as shown in Chapter 18. The reset state of the port pins is mask-programmable and can be defined by the user.

16.1 External reset using the RST pin

The reset input for the P80CLx1 is RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. Port pins adopt their reset state immediately after the RST goes HIGH. During reset, ALE and $\overline{PSEN}$ are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated until RST goes LOW. The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

16.2 Power-on-reset

The device contains on-chip circuitry which switches the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V; if the mask option 'ON' has been chosen. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. During that time the CPU is held in a reset state. A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation (see Fig.27).

The on-chip Power-on-reset circuitry can also be switched off via the mask option 'OFF'. This option reduces the Power-down current to typically 800 nA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset, option 'OFF' should be chosen.

An automatic reset can be obtained by connecting the RST pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The Power-on-reset circuitry is shown in Fig.26.

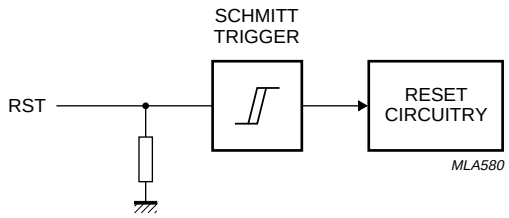


Fig.25 Reset configuration.

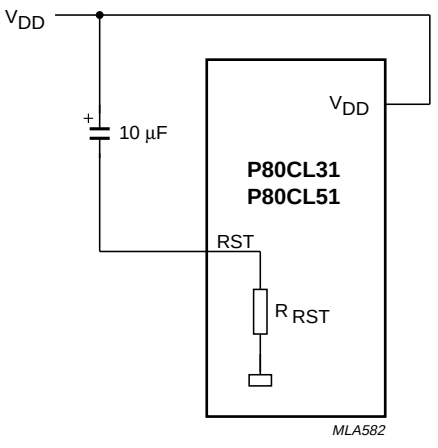


Fig.26 Recommended Power-on-reset circuitry.

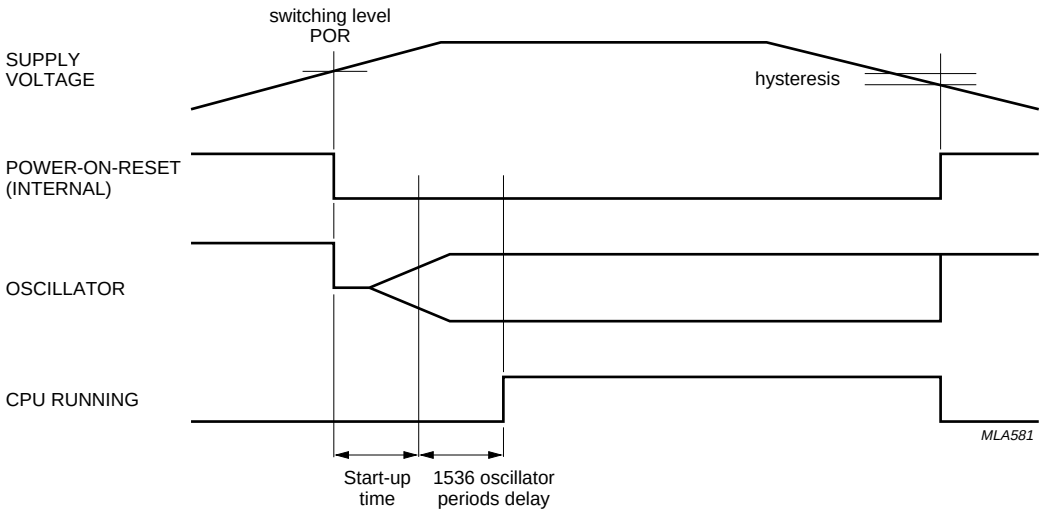


Fig.27 Power-on-reset switching level.

17 MASK OPTIONS FOR P80CL31 AND P80C51

17.1 P80CL31: ROMless version

The P80CL31 is a low voltage ROMless version of the P80CL51 microcontroller. The mask options for the P80CL31 are fixed as follows:

- Port options: all ports have option “1S”, i.e. standard port, HIGH after reset
- Oscillator option: Oscillator 3
- Power-on-reset option: OFF.

17.2 P80C51: 5 V standard version

The P80C51 is a 5 V version of the low voltage P80CL51 microcontroller. All functional features of the P80CL51 are maintained in the P80C51 with the exception of the mask options. The mask options on the P80C51 are fixed as follows:

- Port options: all ports have option “1S”, i.e. standard port, HIGH after reset
- Oscillator option: Oscillator 3
- Power-on-reset option: OFF.

18 SPECIAL FUNCTION REGISTERS OVERVIEW

The P80CLx1 has 25 SFRs available to the user.

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
F8	IP1[1]	00000000	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT9}$)
F0	B[1]	00000000	B Register
E9	IX1	00000000	Interrupt Polarity Register
E8	IEN1[1]	00000000	Interrupt Enable Register 1
E0	ACC[1]	00000000	Accumulator
D0	PSW[1]	00000000	Program Status Word
C0	IRQ1[1]	00000000	Interrupt Request Flag Register
B8	IP0[1]	X0000000	Interrupt Priority Register 0
B0	P3[1]	XXXXXXXX[2]	Digital I/O Port Register 3
A8	IEN0[1]	00000000	Interrupt Enable Register
A0	P2[1]	XXXXXXXX[2]	Digital I/O Port Register 2
99	S0BUF	XXXXXXXX	Serial Data Buffer Register 0
98	S0CON[1]	00000000	Serial Port Control Register 0
90	P1[1]	XXXXXXXX[2]	Digital I/O Port Register 1
8D	TH1	00000000	Timer 1 High byte
8C	TH0	00000000	Timer 0 High byte
8B	TL1	00000000	Timer 1 Low byte
8A	TL0	00000000	Timer 0 Low byte
89	TMOD	00000000	Timer 0 and 1 Mode Control Register
88	TCON[1]	00000000	Timer 0 and 1 Control/External Interrupt Control Register
87	PCON	0XX00000	Power Control Register
83	DPH	00000000	Data Pointer High byte
82	DPL	00000000	Data Pointer Low byte
81	SP	00000111	Stack Pointer
80	P0[1]	XXXXXXXX[2]	Digital I/O Port Register 0

Notes

1. Bit addressable register.
2. Port reset state determined by the customer.

19 INSTRUCTION SET

The P80CLx1 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

For the description of the **Data Addressing modes** and **Hexadecimal opcode cross-reference** see Table 30.

Table 26 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	add register to A	1	1	2*
ADD	A,direct	add direct byte to A	2	1	25
ADD	A,@Ri	add indirect RAM to A	1	1	26, 27
ADD	A,#data	add immediate data to A	2	1	24
ADDC	A,Rr	add register to A with carry flag	1	1	3*
ADDC	A,direct	add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	subtract register from A with borrow	1	1	9*
SUBB	A,direct	subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	subtract immediate data from A with borrow	2	1	94
INC	A	increment A	1	1	04
INC	Rr	increment register	1	1	0*
INC	direct	increment direct byte	2	1	05
INC	@Ri	increment indirect RAM	1	1	06, 07
DEC	A	decrement A	1	1	14
DEC	Rr	decrement register	1	1	1*
DEC	direct	decrement direct byte	2	1	15
DEC	@Ri	decrement indirect RAM	1	1	16, 17
INC	DPTR	increment data pointer	1	2	A3
MUL	AB	multiply A and B	1	4	A4
DIV	AB	divide A by B	1	4	84
DA	A	decimal adjust A	1	1	D4

Table 27 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	exclusive-OR register to A	1	1	6*
XRL	A,direct	exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	exclusive-OR immediate data to A	2	1	64
XRL	direct,A	exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	exclusive-OR immediate data to direct byte	3	2	63
CLR	A	clear A	1	1	E4
CPL	A	complement A	1	1	F4
RL	A	rotate A left	1	1	23
RLC	A	rotate A left through the carry flag	1	1	33
RR	A	rotate A right	1	1	03
RRC	A	rotate A right through the carry flag	1	1	13
SWAP	A	swap nibbles within A	1	1	C4

Table 28 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	move register to A	1	1	E*
MOV	A,direct (note 1)	move direct byte to A	2	1	E5
MOV	A,@Ri	move indirect RAM to A	1	1	E6, E7
MOV	A,#data	move immediate data to A	2	1	74
MOV	Rr,A	move A to register	1	1	F*
MOV	Rr,direct	move direct byte to register	2	2	A*
MOV	Rr,#data	move immediate data to register	2	1	7*
MOV	direct,A	move A to direct byte	2	1	F5
MOV	direct,Rr	move register to direct byte	2	2	8*
MOV	direct,direct	move direct byte to direct	3	2	85
MOV	direct,@Ri	move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	move immediate data to direct byte	3	2	75
MOV	@Ri,A	move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	push direct byte onto stack	2	2	C0
POP	direct	pop direct byte from stack	2	2	D0
XCH	A,Rr	exchange register with A	1	1	C*
XCH	A,direct	exchange direct byte with A	2	1	C5
XCH	A,@Ri	exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 29 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	clear carry flag	1	1	C3
CLR	bit	clear direct bit	2	1	C2
SETB	C	set carry flag	1	1	D3
SETB	bit	set direct bit	2	1	D2
CPL	C	complement carry flag	1	1	B3
CPL	bit	complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	move direct bit to carry flag	2	1	A2
MOV	bit,C	move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	absolute subroutine call	2	2	•1
LCALL	addr16	long subroutine call	3	2	12
RET		return from subroutine	1	2	22
RETI		return from interrupt	1	2	32
AJMP	addr11	absolute jump	2	2	♦1
LJMP	addr16	long jump	3	2	02
SJMP	rel	short jump (relative address)	2	2	80
JMP	@A+DPTR	jump indirect relative to the DPTR	1	2	73
JZ	rel	jump if A is zero	2	2	60
JNZ	rel	jump if A is not zero	2	2	70
JC	rel	jump if carry flag is set	2	2	40
JNC	rel	jump if carry flag is not set	2	2	50
JB	bit,rel	jump if direct bit is set	3	2	20
JNB	bit,rel	jump if direct bit is not set	3	2	30
JBC	bit,rel	jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	decrement direct and jump if not zero	3	2	D5
NOP		no operation	1	1	00

Table 30 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	working register R0-R7
direct	128 internal RAM locations and any special function register (SFR)
@Ri	indirect internal RAM location addressed by register R0 or R1 of the actual register bank
#data	8-bit constant included in instruction
#data 16	16-bit constant included as bytes 2 and 3 of instruction
bit	direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP; the branch will be anywhere within the 64 kbytes Program Memory address space
addr11	111-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction
rel	signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps; range is –128 to +127 bytes relative to first byte of the following instruction
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F
•	1, 3, 5, 7, 9, B, D, F
♦	0, 2, 4, 6, 8, A, C, E

Table 31 Instruction map

First hexadecimal character of opcode ↓	← Second hexadecimal character of opcode →															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0 | 1		0	1	2	3	4	5	6	7
									INC Rr							
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0 | 1		0	1	2	3	4	5	6	7
									DEC Rr							
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									ADD A,Rr							
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									ADDC A,Rr							
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									ORL A,Rr							
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									ANL A,Rr							
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									XRL A,Rr							
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0 | 1		0	1	2	3	4	5	6	7
									MOV Rr,#data							
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0 | 1		0	1	2	3	4	5	6	7
									MOV direct,Rr							
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									SUB A,Rr							
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0 | 1		0	1	2	3	4	5	6	7
									MOV Rr,direct							
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0 | 1		0	1	2	3	4	5	6	7
									CJNE Rr,#data,rel							
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									XCH A,Rr							
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									DJNZ Rr,rel							
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0 | 1		CLR A	MOV A,direct (1)	MOV A,@Ri 0 | 1		0	1	2	3	4	5	6	7
									MOV A,Rr							
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0 | 1		CPL A	MOV direct,A	MOV @Ri,A 0 | 1		0	1	2	3	4	5	6	7
									MOV Rr,A							

Note

1. MOV A, ACC is not a valid instruction.

20 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
I_I	DC current on any input	–5.0	+5.0	mA
I_O	DC current on any output	–5.0	+5.0	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
T_j	operating junction temperature	–	+125	°C

21 DC CHARACTERISTICS FOR P80CL31 AND P80CL51

V_{SS} = 0 V; T_{amb} = –40 to +85 °C; all voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	operating	V_{SS} = 0 V	1.8	6.0	V
	RAM retention in Power-down mode		1.0	–	V
Supply current (note 1, note 2)					
I_{DD}	operating supply current	Oscillator 1; f_{clk} = 32 kHz; V_{DD} = 1.8 V; T_{amb} = 25 °C	–	50	µA
		Oscillator 2; f_{clk} = 3.58 MHz; V_{DD} = 3 V	–	2.5	mA
		Oscillator 3; f_{clk} = 16 MHz; V_{DD} = 5 V	–	24	mA
		Oscillator 4; f_{clk} = 16 MHz; V_{DD} = 5 V	–	26	mA
Supply current (Idle mode) (note 2, note 3)					
$I_{DD(idle)}$	supply current (Idle mode)	Oscillator 1; f_{clk} = 32 kHz; V_{DD} = 1.8 V; T_{amb} = 25 °C	–	25	µA
		Oscillator 2; f_{clk} = 3.58 MHz; V_{DD} = 3 V	–	1.0	mA
		Oscillator 3; f_{clk} = 16 MHz; V_{DD} = 5 V	–	10	mA
		Oscillator 4; f_{clk} = 16 MHz; V_{DD} = 5 V	–	12	mA
Supply current (Power-down mode) (note 2, note 4)					
$I_{DD(pd)}$	supply current (Power-down mode)	V_{DD} = 1.8 V; T_{amb} = 25 °C	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Inputs					
V_{IL}	LOW level input voltage		V_{SS}	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD}	V
I_{IL}	input current logic 0 (port 1,2,3)	V_{DD} = 5 V; V_I = 0.4 V	–	–100	µA
		V_{DD} = 2.5 V; V_I = 0.4 V	–	–50	µA
I_{ITL}	input current logic 0, HIGH-to-LOW transition (port 1,2,3)	V_{DD} = 5 V; $V_I = 0.5V_{DD}$	–	–1.0	mA
		V_{DD} = 2.5 V; $V_I = 0.5V_{DD}$	–	–500	µA
I_{LI}	input leakage current (port 0, $\overline{EA}$)	$V_{SS} < V_I < V_{DD}$	–	10	µA
Port outputs					
I_{OL}	LOW level output current	V_{DD} = 5 V; V_{OL} = 0.4 V	1.6	–	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	0.7	–	mA
I_{OH}	HIGH level output current (push-pull options)	V_{DD} = 5 V; $V_{OH} = V_{DD} - 0.4$ V	–1.6	–	mA
		V_{DD} = 2.5 V; $V_{OH} = V_{DD} - 0.4$ V	–0.7	–	mA
R_{RST}	RST pull-down resistor		10	200	kΩ

Notes

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL 2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}; all open drain outputs connected to V_{SS}.
2. Circuits with Power-on-reset option ‘OFF’ are tested at $V_{DD(min)}$ = 1.8 V; within option ‘ON’ (typically 1.3 V) they are tested at $V_{DD(min)}$ = 2.3 V. Please note, option ‘ON’ is only available on P80CL51.
3. The Idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$. XTAL 2 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
4. The Power-down current is measured with all output pins disconnected; XTAL 1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.

22 DC CHARACTERISTICS FOR P80C51

V_{SS} = 0 V; V_{DD} = 5.0V ±10%; f_{clk} = 3.5 to 16 MHz; T_{amb} = –40 to +85 °C all voltages with respect to V_{SS} unless otherwise specified. Note that the Power-on-reset option is 'OFF' and the Oscillator option is 'Oscillator 3'.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage				
	operating	V_{SS} = 0 V	4.5	5.5	V
	RAM retention in Power-down mode		1.0	–	V
I_{DD}	operating supply current	f_{clk} = 16 MHz; V_{DD} = 5.0 V; note 1	–	24	mA
$I_{DD(idle)}$	supply current (Idle mode)	f_{clk} = 16 MHz; V_{DD} = 5.0 V; note 2	–	10	mA
$I_{DD(pd)}$	supply current (Power-down mode)	V_{DD} = 5.0 V; note 3	–	50	mA
Inputs					
V_{IL}	LOW level input voltage		V_{SS}	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	V_{DD}	V
I_{IL}	input current logic 0 (port 1,2,3)	V_I = 0.4 V	–	100	µA
I_{TL}	input current logic 0, HIGH- to-LOW transition (port 1,2,3)	$V_I = 0.5V_{DD}$	–	1.0	mA
I_{LI}	input leakage current (port 0, $\overline{EA}$)	$V_{SS} < V_I < V_{DD}$	–	10	µA
Port outputs					
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1.6	–	mA
I_{OH}	HIGH level output current (push-pull options)	$V_{OH} = V_{DD} – 0.4$ V	–1.6	–	mA
R_{RST}	RST pull-down resistor		10	200	kΩ

Notes

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL 2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}; all open drain outputs connected to V_{SS}.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$. XTAL 2 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.
3. The Power-down current is measured with all output pins disconnected; XTAL 1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}; all open drain outputs connected to V_{SS}.

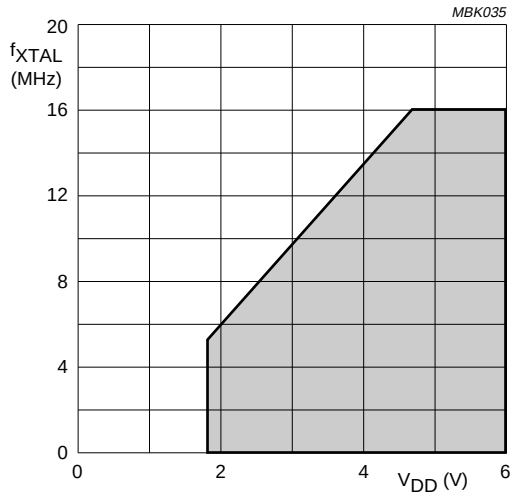
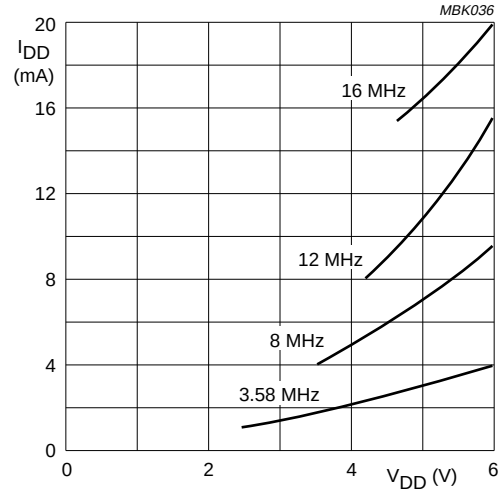
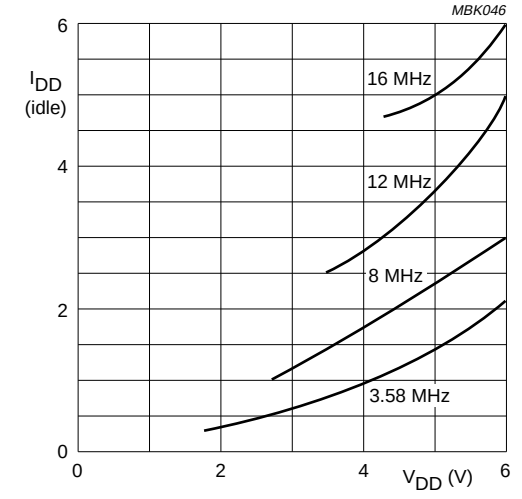


Fig.28 Frequency operating range.



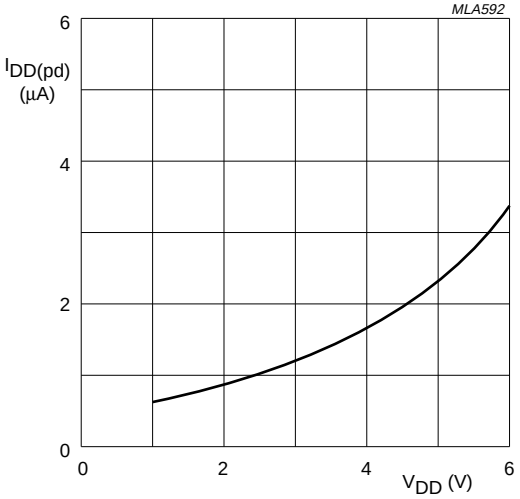
T_{amb} = 25 °C.

Fig.29 Typical operating current as a function of frequency and V_{DD}.



T_{amb} = 25 °C.

Fig.30 Typical Idle current as a function of frequency and V_{DD}.



T_{amb} = 25 °C.

Fig.31 Typical Power-down current as a function of V_{DD}.

23 AC CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 40 pF for all other outputs unless specified; $t_{CLK} = 1/f_{CLK}$.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Program Memory (Fig.32)						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLK} - 40$	–	ns
t_{AVLL}	address valid to ALE LOW	43	–	$t_{CLK} - 40$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	233	–	$4t_{CLK} - 100$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	58	–	$t_{CLK} - 25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLK} - 35$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	125	–	$3t_{CLK} - 125$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLK} - 20$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid	75	–	$t_{CLK} - 8$	–	ns
t_{AVIV}	address to valid instruction in	–	302	–	$5t_{CLK} - 115$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	12	–	0	–	ns
External Data Memory (Figs 33 and 34)						
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	150	–	$5t_{CLK} - 165$	ns
t_{RHDZ}	data float after $\overline{RD}$	–	97	–	$2t_{CLK} - 70$	ns
t_{LLDV}	ALE LOW to valid data in	–	517		$8t_{CLK} - 150$	ns
t_{AVDV}	address to valid data in	–	585	–	$9t_{CLK} - 165$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	200	300	$3t_{CLK} - 50$	$3t_{CLK} + 50$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	203	–	4	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	43	123	$t_{CLK} - 40$	$t_{CLK} + 40$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	23	–	$t_{CLK} - 60$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	433	–	$7t_{CLK} - 150$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	33	–	$t_{CLK} - 50$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	12	–	12	ns

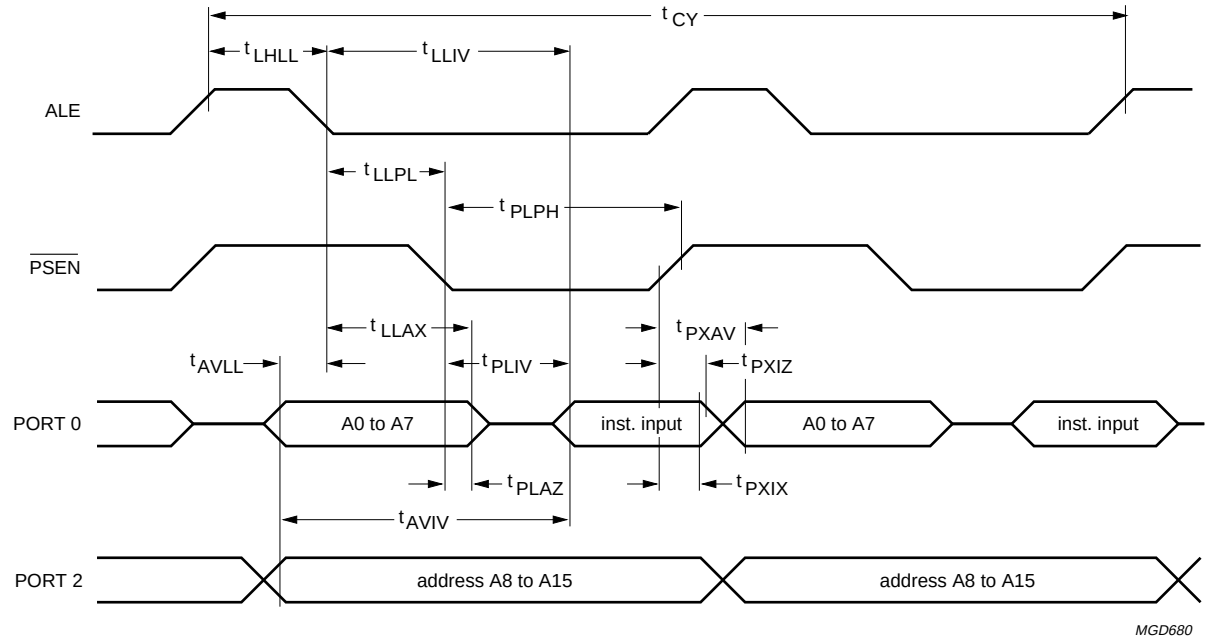


Fig.32 Read from Program Memory.

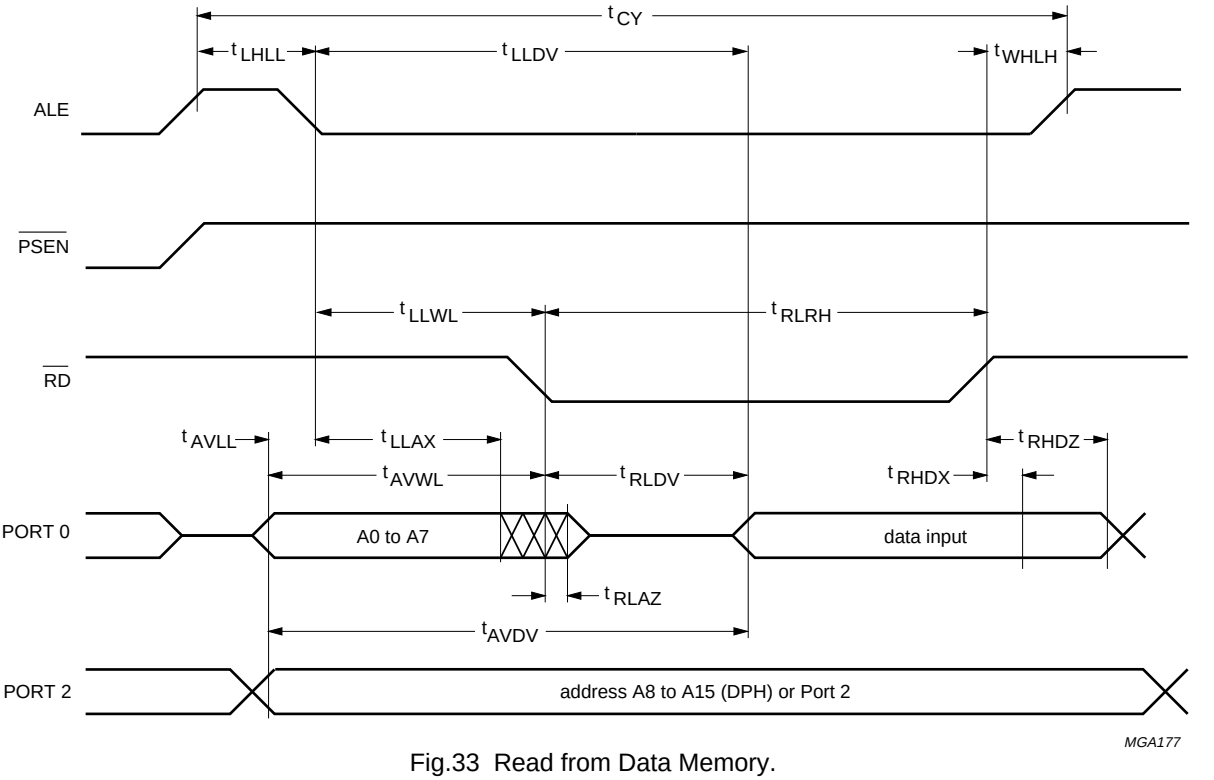


Fig.33 Read from Data Memory.

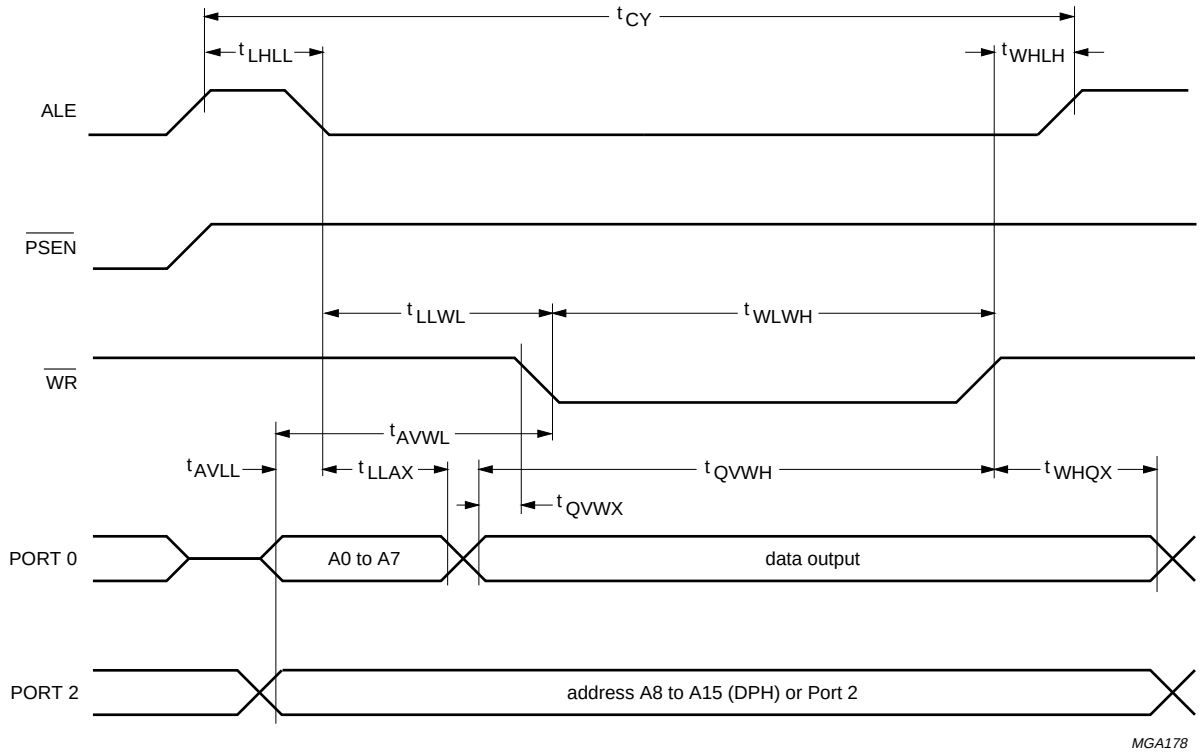


Fig.34 Write to Data Memory.

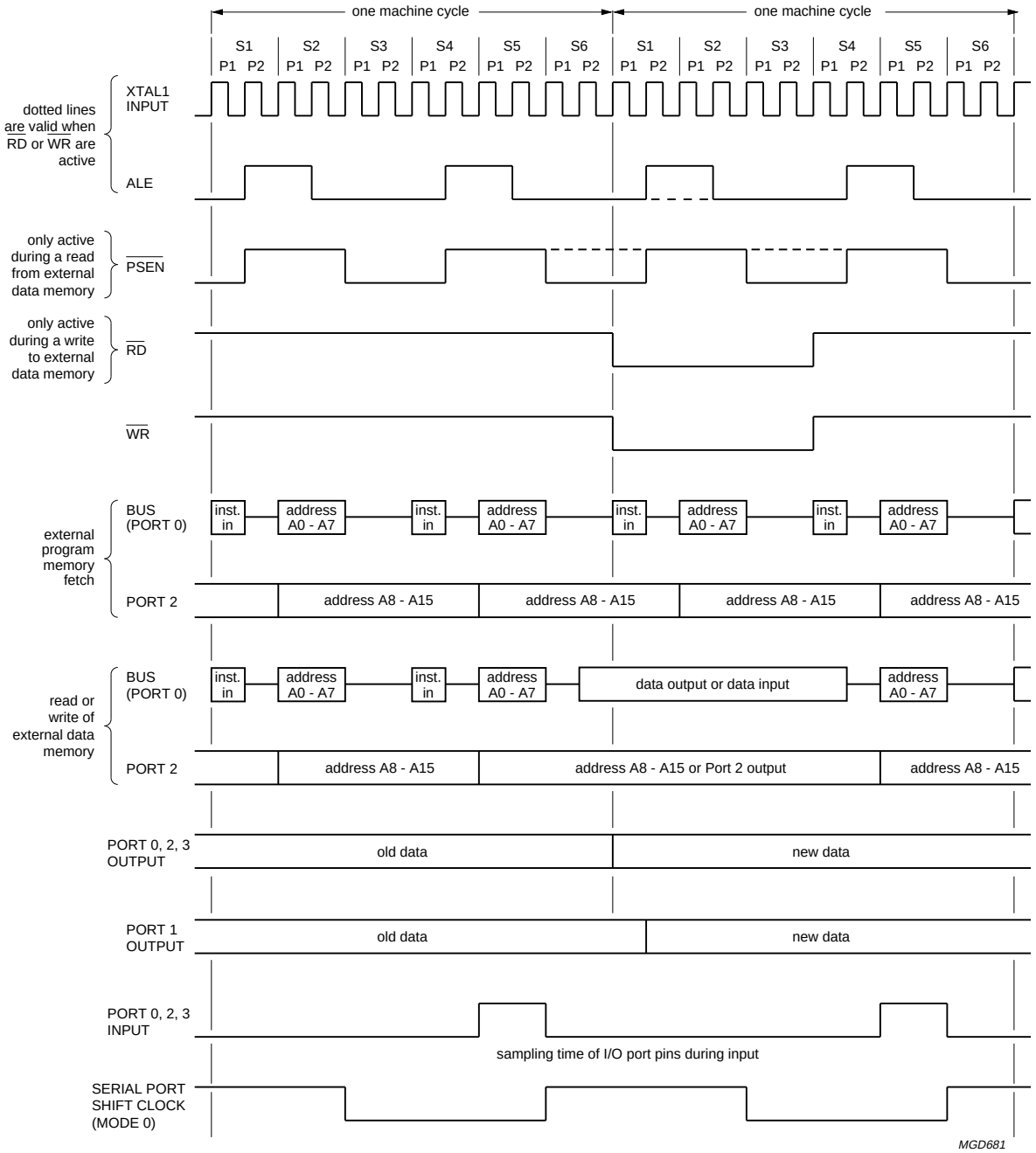


Fig.35 Instruction cycle timing.

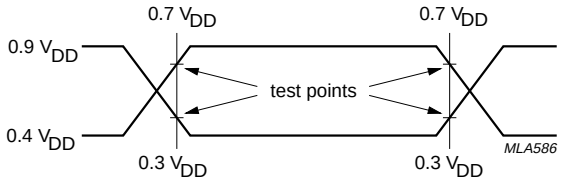


Fig.36 AC testing input waveform.

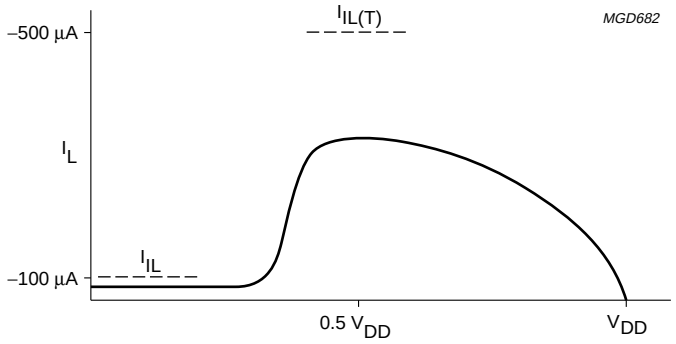


Fig.37 Input current.

24 P85CL000HFZ 'PIGGY-BACK' SPECIFICATION

The differences between the masked version and the piggy-back are described below.

24.1 General description

The P85CL000HFZ is a piggy-back version with 256 bytes of RAM used for emulation of the P80CL51 and the P83CL410 microcontrollers. The P85CL000HFZ is manufactured in an advanced CMOS technology.
The instruction set of the P85CL000HFZ is based on that of the 8051. The device has low power consumption and a wide supply voltage range. The P85CL000HFZ has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. For timing and AC/DC characteristics, please refer to the P80CL51 specifications.

24.2 Feature differences/additional features with respect to P80CL51

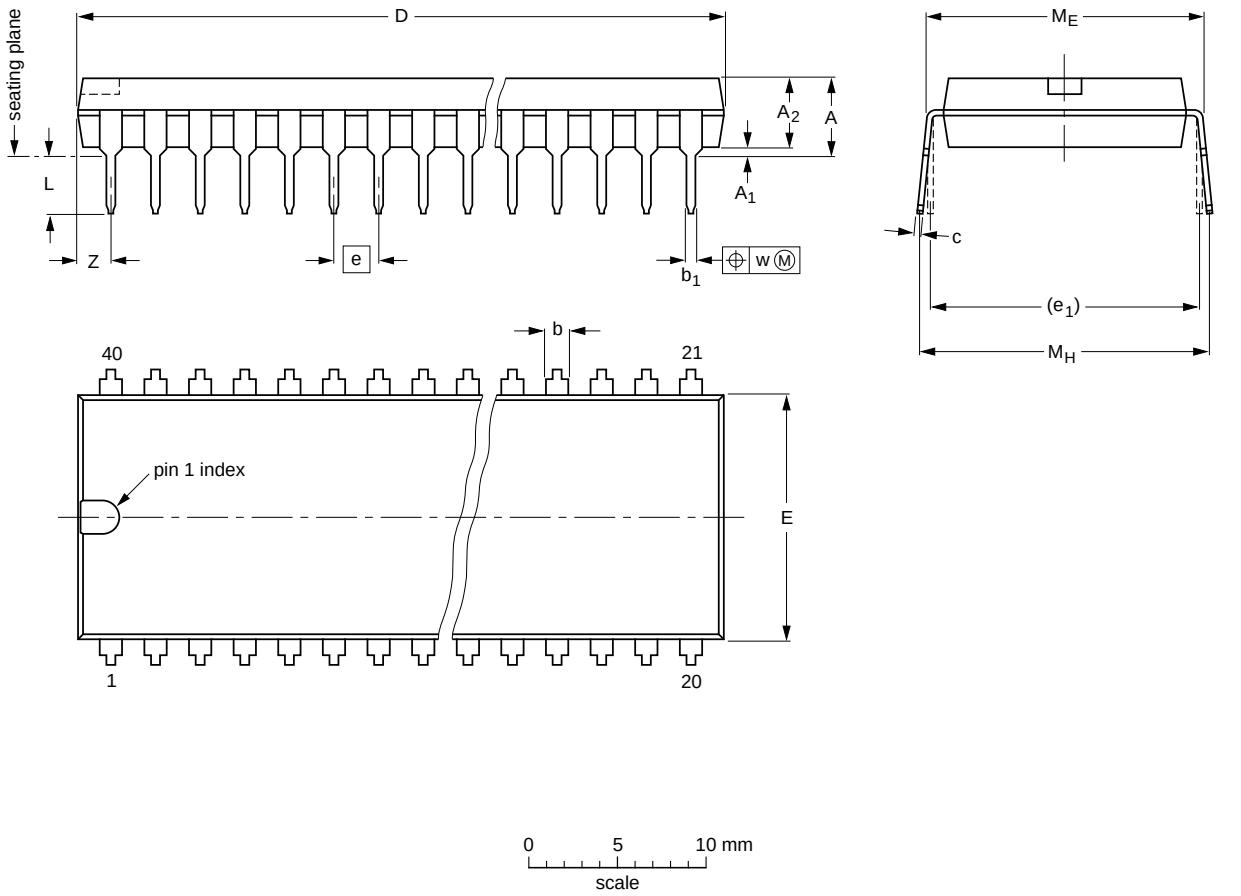
- No internal ROM
- 8-bit CPU, RAM, I/O in a single 40-lead package with DIP pin-out
- Socket for up to 16 kbytes external EPROM
- 256 bytes RAM, expandable externally to 64 kbytes
- I^2C-bus interface for serial transfer on two lines
- On-chip oscillator: Oscillator 4 option only.

24.3 Common specification/feature differences between P85CL000HFZ and P83CL410/P80CL51

PARAMETER	P83CL410/P80CL51	P85CL000HFZ 'PIGGY-BACK'
RAM size	128	256
ROM size	4K	EPROM size dependent (max. 16K)
Port options	1, 2, 3	1
Oscillator options	Oscillator 1, 2, 3, 4, RC	Oscillator 4
Mechanical dimensions	standard dual in-line, small outline	same pin-out as SOT129-1, but larger package size
Current consumption	I_{DD}	I_{DD} (Oscillator 4) + I_{EPROM}
Voltage range	full	full, **limited by EPROM**
ESD	specification	not tested (different package)

25 PACKAGE OUTLINES

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

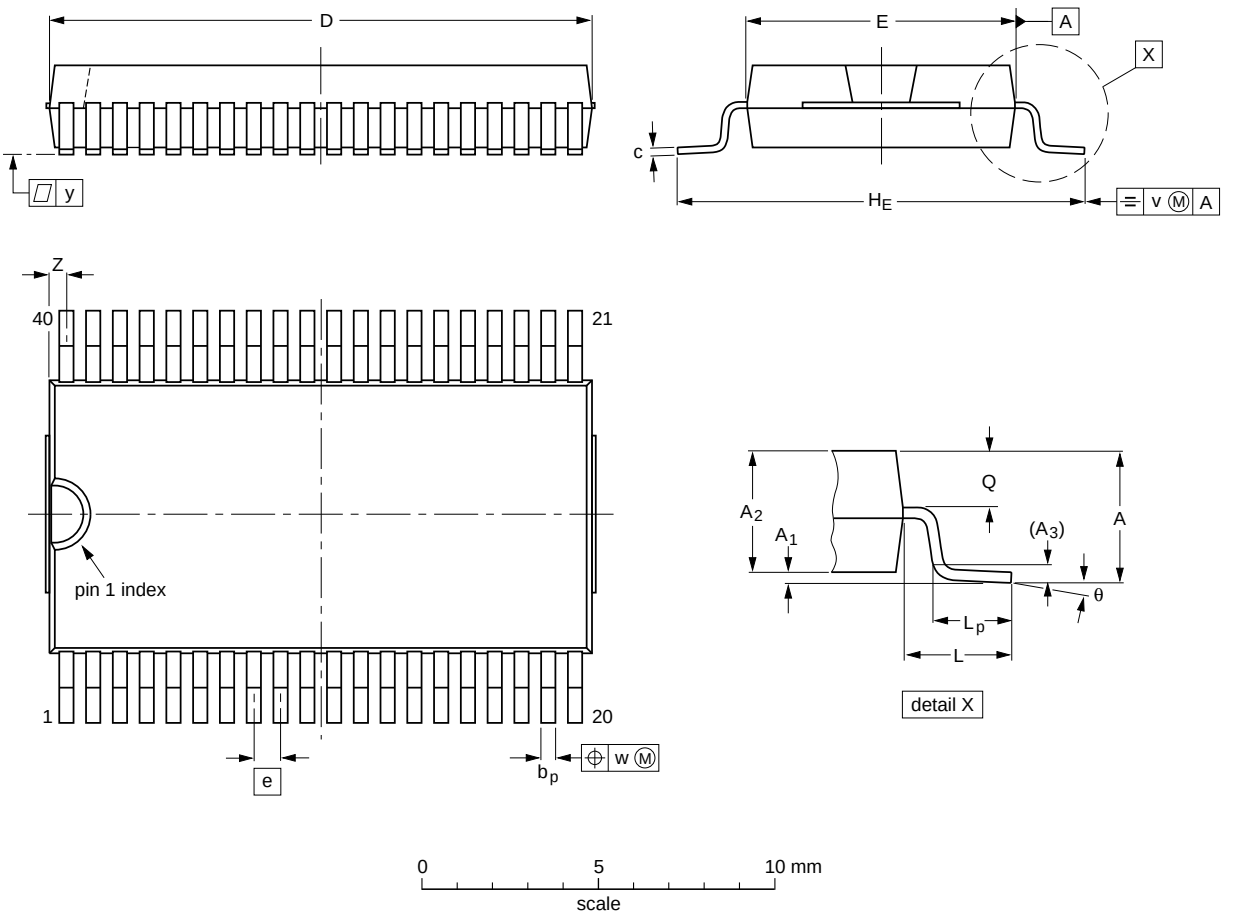
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

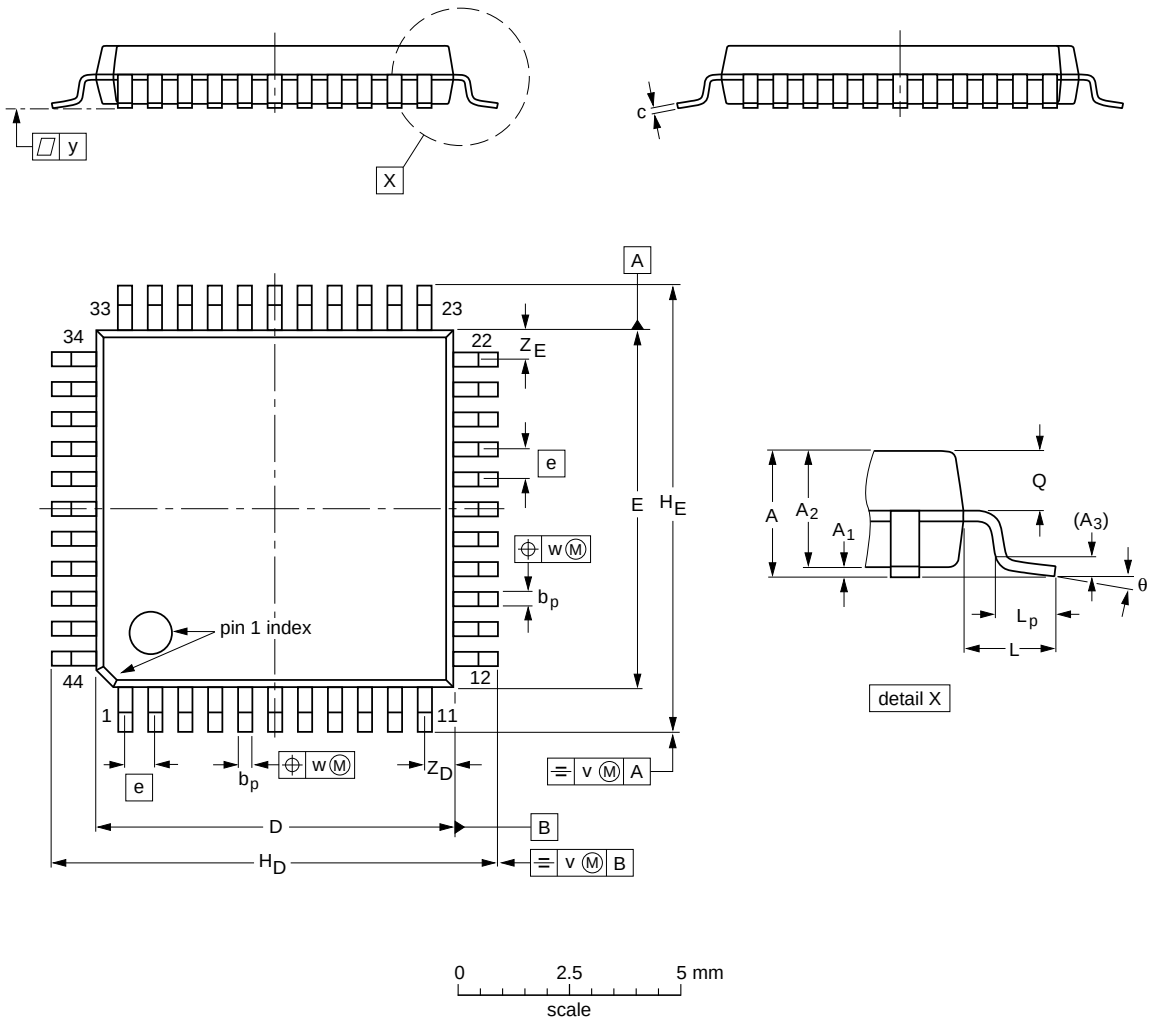
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7^o 0^o
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

26 SOLDERING

26.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

26.2 DIP

26.2.1 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

26.2.2 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

26.3 QFP and VSO

26.3.1 Reflow soldering

Reflow soldering techniques are suitable for all QFP and VSO packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

26.3.2 Wave soldering

26.3.2.1 QFP

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

26.3.2.2 VSO

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

26.3.2.3 Method (QFP and VSO)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

26.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

27 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

28 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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