Oki Semiconductor

advantage™ microcontrollers

ML675K Series

ML675001/ML67Q5002/ML67Q5003
32-Bit ARM®-Based General Purpose Microcontrollers

General Purpose

Description

The Oki ML675001/ML67Q5002/ML67Q5003 family of microcontrollers (MCUs) are the newest members of an extensive and growing family of 32-bit ARM®-based standard products for general-purpose applications that require 32-bit CPU performance and low cost afforded by MCU integrated features.

The ML675001, ML67Q5002 and ML67Q5003 devices each provide 8 Kbytes of unified cache memory, 32 Kbytes of built-in SRAM, 4 Kbytes of built-in boot ROM, and a host of other useful peripherals such as auto-reload timers, a watchdog timer (WDT), two pulse-width modulators (PWM), A/D converters, multiple UARTs, synchronous serial port, I2C serial interface, GPIOs, DMA controller, external memory controller, and boundary scan capability. In addition, the ML67Q5002 and ML67Q5003 devices offer 256 Kbytes and 512 Kbytes of built-in Flash memory respectively. The ML675001, ML67Q5002 and ML67Q5003 devices are pin-to-pin compatible with each other, and are pin-to-pin compatible with the Oki ML674001/Q4002/Q4003 family of microcontrollers for easy performance updates.

The ARM7TDMI® Advantage

The ML675001/ML67Q5002/ML67Q5003 family of low-cost ARM-based MCUs offers system designers a bridge from 8- and 16-bit proprietary MCU architectures to ARM's higher-performance, affordable, widely-accepted industry standard architecture and its industry-wide support infrastructure. The ARM industry infrastructure offers the system developers many advantages including software compatibility, many ready-to-use software applications, large choices among hardware and software development tools. These ARM-based advantages allow Oki's customers to better leverage engineering resources, lower development costs, minimize project risks, and reduce their product time to market. In addition, migration of a design with an Oki standard MCU to an Oki custom solution is easily facilitated with its award-winning µPLAT™ product development architecture.

Features

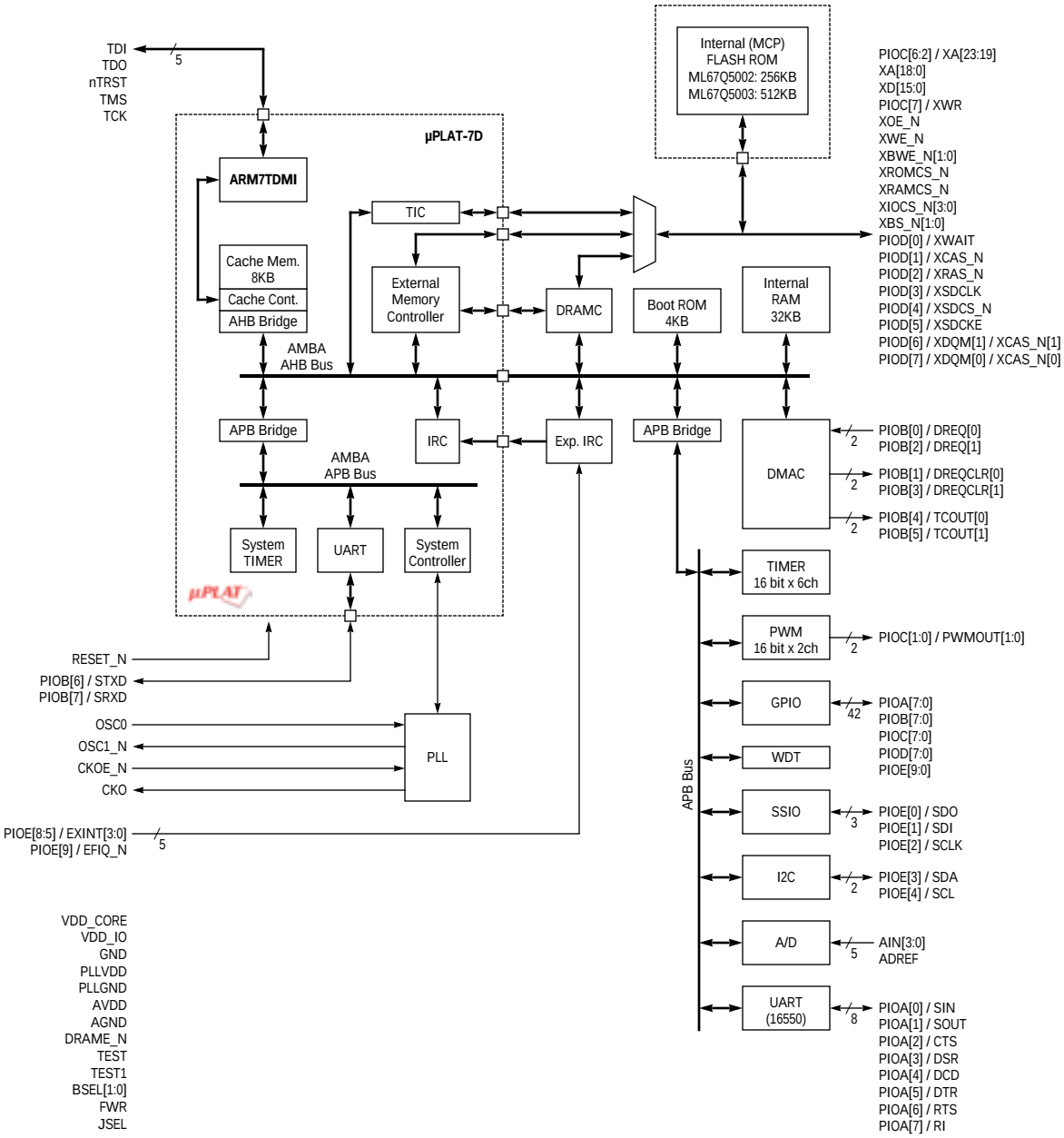
- ARM7TDMI 32-bit RISC CPU
  - 16-bit Thumb™ instruction set for power efficiency applications
- 32-bit mode (ARM) and/or 16-bit mode (Thumb)
- Built-in external memory controller supports glueless connectivity to memory (including SDRAM and EDO DRAM) and I/O
- Built in Flash ROM
  - 256 KB (ML67Q5002)
  - 512 KB (ML67Q5003)
- 32-KBytes built in zero-wait-state SRAM
- 28 interrupt sources
- DMA: 2 channels with external access
- Timers: 7 16-bit timers
- Watch-Dog Timer: dual stage 16 bit
- PWM: Two 16-bit channels
- Serial Interfaces: SIO, UART, USART, I2C
- GPIO: 42 bits
- A/D Converter: Four 10-bit channels
- Built-in boot ROM accommodates in-circuit Flash ROM re-programming and field-updates
- Package
  - 144-pin plastic LQFP
  - 144-pin plastic LFBGA

ML675001/Q5002/Q5003 MCUs

Part Number	Clock Frequency	Built-in Flash Size	Packages
ML675001	60 MHz	n/a	144-pin plastic LQFP (ML675001TC) 144-pin plastic LFBGA (ML675001LA)
ML67Q5002	60 MHz	256 KB	144-pin plastic LQFP (ML67Q5002TC) 144-pin plastic LFBGA (ML67Q5002LA)
ML67Q5003	60 MHz	512 KB	144-pin plastic LQFP (ML67Q5003TC) 144-pin plastic LFBGA (ML67Q5003LA)

Data Sheet

Block Diagram



Functional Description

CPU

CPU core:	ARM7TDMI
Operating frequency:	1 MHz to 60 MHz (max)
Byte Ordering:	Little endian.
Instructions:	ARM instruction (32-bit length) and Thumb instruction (16-bit length) can be mixed
General register bank:	31 x 32 bits
Built-in barrel shifter:	ALU and barrel shift operations can be executed by one instruction.
Multiplier:	32 bits x 8 bits (Modified Booth's Algorithm)
Built-in debug function:	JTAG interface, break point register

Built-in Memory

FLASH ROM:	ML675001: ROM-less version
	ML67Q5002: 256Kbytes (128K x 16 bits)
	ML67Q5003: 512Kbytes (256K x 16 bits)
	Access timing of this FLASH memory is configured by the ROM bank control register of the external memory controller.
SRAM:	32KB (8K x 32bits)
	Connected to processor bus (1 cycle read, 2 cycle write)
Cache memory:	8K unified memory with 4-way set-associative

Interrupt Controller

Fast interrupt request (FIQ) and interrupt request (IRQ) are employed as interrupt input signals. The interrupt controller controls these interrupt signals going to ARM core.

1. Interrupt sources
   - FIQ: 1 external source (external pin: EFIQ_N)
   - IRQ: Total of 27 sources. 23 internal sources, and 4 external sources (External pins EXINT[3:0])
2. Interrupt priority level
   - Configurable, 8-level priority for each source
3. External interrupt pin input
   - EXINT[3:0] can be set as Level or Edge sensing
   - Configurable High or Low when Level sensing. Configurable Rise or Falling edge triggering when Edge sensing.
   - EFIQ_N is set as Falling edge triggering.

Timers

The MCU contains seven 16-bit reload timers. Of these, 1 timer is used as system timer for operating system. The other 6 timers are used by application software.

1. System timer: 1 channel
   - 16-bit auto reload timer: Used as system timer for OS. Interrupt request by timer overflow.
2. Application timer: 6 channels
   - 16-bit auto reload timer. Interrupt request by compare match.
   - One shot, interval
   - Clock can be independently set for each channel

Watch Dog Timer

Functions as an interval timer or a watch dog timer.

- 16-bit timer
- Watch dog timer or interval timer mode can be selected
- Interrupt reset generation
- Maximum period: longer than 200 msec

Serial Interface

The ML675001/Q5002/Q5003 contains four serial interfaces.

1. UART without FIFO: 1 channel

   This is the serial port which performs data transmission, taking a synchronization per character. Selection of various parameters, such as addition of data length, a stop bit, and a parity bit, is possible.
   - Asynchronous full duplex operation
   - Sampling Rate = Baud rate x 16 samples
   - Character Length: 7, 8 bit
   - Stop Bit Length: 1, 2 bit
   - Parity: Even, Odd, none
   - Error Detection: Parity, Framing, Over run
   - Loop Back Function: ON/OFF, Parity, framing, Over run Compulsive addition
   - Baud Rate Generation: Exclusive baud rate generator built-in (8-bit counter) Independent from a bus clock
   - Internal-Baud-Rate-Clock-Stop at the Time of HALT Mode.
2. UART with 16 byte FIFO: 1 channel

   Features 16 byte FIFO in both send and receive. Uses the industry standard 16550A ACE (Asynchronous Communication Element).
   - Asynchronous full duplex operation
   - Reporting function for all status
   - 16 Byte transmission and reception FIFO
   - Transmission, reception, interrupt of line status Data set and Independent FIFO control.
   - Modem control signals: CTS, DCD, DSR, DTR, RI and RTS
   - Data length: 5, 6, 7, or 8 bits
   - Stop bit length: 1, 1.5, or 2 bits
   - parity: Even, Odd, or none
   - Error Detection: Parity, Framing, Overrun
   - Baud Rate Generation: Exclusive baud rate generator built-in
3. Synchronous serial interface: 1 channel

   Clock-synchronous 8-bit serial port
   - selectable 1/8, 1/16 or 1/32 of the system clock frequency.
   - LSB First or MSB First.
   - Master / Slave Mode

- Transceiver buffer empty interrupt
- Loopback test function

4. I2C: 1 channel

   Based on the I2C Bus specification. Operates as a single master device.
   - Communication mode: Master transmitter /master receiver
   - Transmission Speed: 100 kbps (Standard mode) / 400 kbps (Fast mode)
   - Addressing format: 7 bit / 10 bit
   - Data buffer: 1 Byte (1step)
   - Communication Voltage: 2.7V to 3.3V

GPIO

42-bit parallel port (four 8-bit ports and one 10-bit port).

PIOA[7:0]	Combination port	UART
PIOB[7:0]	Combination port	DMAC, UART (µPLAT-7B)
PIOC[7:0]	Combination port	PWM, XA[23:19], XWR
PIOD[7:0]	Combination port	DRAM control signals etc.
PIOE[9:0]	Combination port	SSIO, I2C, External interrupt signal

1. Input/output selectable at bit level.
2. Each bit can be used as an interrupt source.
3. Interrupt mask and interrupt mode (level) can be set for all bits.
4. The ports are configured as inputs immediately after reset.
5. Primary/secondary function of each port can be set independently.

Direct Memory Access Controller

Two DMA channels that transfer data between:

- Memory and memory.
- I/O and memory.
- I/O and I/O.

1.	Number of channels:	2 channels	
2.	Channel priority level:	Fixed mode:	Channel priority level is always fixed (channel 0 >1).
		Roundrobin:	Priority level of the channel requested for transfer is kept lowest.
3.	Maximum number of transfers:	65,536 (64K times).	
4.	Data transfer size:	Byte (8 bits), Half-word (16 bits), Word (32 bits)	
5.	Bus request system:	Cycle steal mode:	Bus request signal is asserted for each DMA transfer cycle.
		Burst mode:	Bus request signal is asserted until all transfers of transfer cycles are complete.
6.	DMA transfer request:	Software request:	By setting the software transfer request bit inside the DMAC, the CPU starts DMA transfer.
		External request:	DMA transfer is started by external request allocated to each channel.
7.	Interrupt request:	Interrupt request is generated in CPU after the end of DMA transfer for the set number of transfer cycles, or after the occurrence of an error. Interrupt request signal is output separately for each channel. Interrupt request signal output can be masked for each channel.	

Pulse Width Modulation

The ML675001/Q5002/Q5003 contains two Pulse Width Modulation (PWM) channels that can change the duty cycle of a waveform with a constant period. The PWM output resolution is 16 bits for each channel.

A/D Converter

Successive approximation type A/D converter.

1. 10 bits x 4 channels
2. Sample and hold function
3. Scan mode and select mode are supported
4. Interrupt is generated after completion of conversion.
5. Conversion time: 5 µs (min).

External Memory Controller

Controls access of externally connected devices such as ROM (FLASH), SRAM, SDRAM (EDO DRAM) and I/O devices.

1. ROM (FLASH) access function: 1 bank
   Supports 16-bit devices
   Supports FLASH memory: Byte write (can be written only by IF equivalent to SRAM). In ML67Q5002/5003, control internal FLASH access.
   Configurable access timing.
2. SRAM access function: 1 bank
   Supports 16-bit devices
   Supports asynchronous SRAM
   Configurable access timing.
3. DRAM access function: 1 bank
   Supports 16-bit devices
   Supports EDO/SDRAM: Simultaneous connections to EDO-DRAM and SDRAM cannot be made.
   Configurable access timing.
4. External I/O access function: 2 banks
   Supports 8-bit/16-bit access: Independent configuration for each bank.
   Each bank has two chip selects: XIOCS_N[3:0].
   Supports external wait input: XWAIT
   Access timing configurable for each bank independently.

Power Management

HALT, STANDBY and clock gear clock functions are supported as power save functions.

1. HALT mode
   HALT object
   - CPU, internal RAM, AHB bus control
   HALT mode setting: Set by the system control register.
   Exit HALT mode due to: Reset, interrupt
2. STANDBY mode
   Stops the clock for the entire device.
   STANDBY mode setting: Specified by the system control register.
   Exit STANDBY mode due to: Reset, external interrupt (other than EFIQ_N)
3. Clock gear
   The device has two clock systems, HCLK and CCLK. Configure HCLK and CCLK frequency.
   HCLK: CPU, bus control, synchronous serial interface, I2C.
   CCLK: Timers, PWM, UART, AD converter, etc.
4. Clock control by each function unit
   A/D converter, PWM, Timers, DRAMC, DMAC, UART(FIFO), UART, Synchronous SIO, I2C.

Built-In Flash ROM Programming

The robust features of the flash permit simple and optimized programming of the flash-ROM.

1. There are three methods for programming the FLASH-ROM
   - Programming via the JTAG interface.
   - Programming using boot mode. Boot mode is used by the host to download data to the FLASH ROM via the UART interface.
     A program stored in the on-chip boot ROM is used to transfer the incoming serial data on the UART interface to the internal Flash ROM.
   - Programming via a user application running from external memory
     Internal flash can be programmed by executing a user flash programming application from external memory.
2. Single power source for reading and programming of FLASH: 3.0V to 3.6V
3. Programming units: 2 bytes
4. Selectable erasing size
   - Sector erase: 2 Kbytes/sector
   - Block erase: 64 Kbytes/block
   - Chip erase: All memory cell
5. Word program time: 30 µsec
6. Sector/block erase time: 25 msec
7. Chip erase time: 100 msec
8. Write protection
   - Block protect: top address 8Kwords can be protected
   - Chip protect: all words can be protected
9. Number of commands: 9
10. Highly reliable read/program
    - Sector programming: 10000 times
    - Data hold period: 10 years

Pin Configuration

PIOD[6]/ XDQM[1]	XIOCS_N [3]	XIOCS_N [1]	XRAMCS _N	XBWE _N[0]	XOE_N	PIOC[4]/ XA[21]	XA[16]	XA[14]	XA[11]	XA[9]	XA[7]	XA[6]	N
PIOD[7]/ XDQM[0]	XIOCS_N [2]	XIOCS_N [0]	XWE_N	PIOC[7]/ XWR	PIOC[6]/ XA[23]	PIOC[2]/ XA[19]	XA[17]	XA[15]	XA[13]	XA[10]	XA[4]	XA[5]	M
PIOB[1]/ DREQCL R[0]	PIOB[2]/ DREQ[1]	PIOB[0]/ DREQ[0]	XROMCS _N	XBWE_N [1]	PIOC[5]/ XA[22]	PIOC[3]/ XA[20]	XA[18]	XA[12]	VDD_IO	XA[8]	XA[2]	GND	L
PIOB[3]/ DREQCLR[1]	PIOB[5]/ TCOUT [1]	VDD_IO	GND	VDD_IO	VDD_ CORE	VDD_IO	GND	GND	XA[3]	XA[0]	XD[13]	XA[1]	K
PIOC[0]/ PWMOUT[0]	GND	PIOB[4]/ TCOUT [0]	PIOC[1]/ PWMOUT [1]						VDD_IO	XD[15]	XD[11]	XD[14]	J
XBS_N [0]	XBS_N [1]	PIOD[0]/ XWAIT	VDD_ CORE						VDD_ CORE	XD[10]	NC	XD[12]	H
PIOD[2]/ XRAS_N	PIOD[1]/ XCAS_N	VDD_IO	GND			**144-Pin LFBGA (TOP VIEW)**			VDD_IO	XD[8]	CLKMD1	XD[9]	G
BSEL[1]	PIOD[5]/ XSDCKE	PIOD[3]/ XSDCLK	PIOD[4]/ XSDCS_N						GND	XD[7]	XD[6]	XD[5]	F
PIOE[7]/ EXINT[2]	BSEL[0]	PIOE[8]/ EXINT[3]	PIOE[5]/ EXINT[0]						GND	XD[2]	CLKMD0	XD[4]	E
PIOE[0]/ SCLK	PIOE[6]/ EXINT[1]	PIOE[9]/ EFIQ_N	PIOE[2]/ SDO	OSC1_N	PIOA[1]/ SOUT	AIN[0]	VREFN	VDD_IO	GND	VDD_IO	XD[3]	XD[1]	D
TDI	PIOE[1]/ SDI	CKO	TMS	CKOE_N	AVDD	AIN[1]	AIN[3]	VDD_ CORE	PIOA[5]/ DTR	FWR	XD[0]	RESET _N	C
nTRST	TDO	TCK	GND	VDD_IO	PIOA[0/ SIN	VREFP	AGND	GND	PIOA[3]/ DSR	PIOA[7]/ RI	PIOE[4]/ SCL	PIOB[7]/ SRXD	B
PLLVDD	PLLGND	JSEL	DRAME_ N	OSC0	TEST	AIN[2]	PIOA[2]/ CTS	PIOA[4]/ DCD	PIOA[6] RTS	PIOE[3]/ SDA	PIOB[6]/ STXD	TEST1	A
13	12	11	10	9	8	7	6	5	4	3	2	1	

Figure 1. 144-Pin LFBGA

Notes:

1. For pins that have multiple functions, the signals are noted by their primary / secondary functions.
2. NC pins are electrically unconnected in the package. NC pins can be connected to VDD or GND.

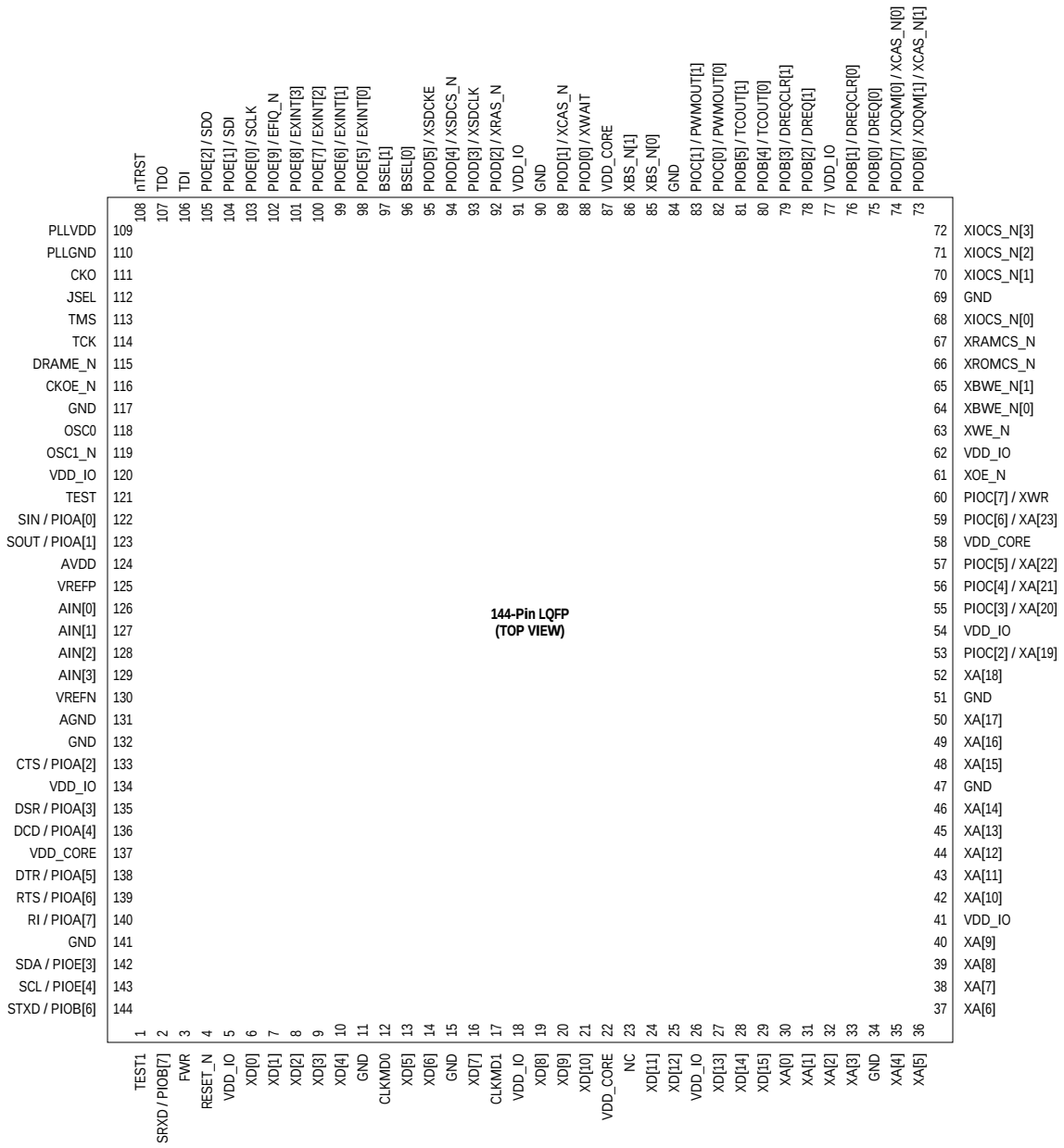


Figure 2. 144-Pin Plastic LQFP

Notes:

1. For pins that have multiple functions, the primary function is the name closest to the package.
2. Leave NC pins unconnected.

List of Pins

Pin		Primary Function			Secondary Function		
LQFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description
1	A1	TEST1	–	Test mode input	–	–	
2	B1	PIOB[7]	I/O	General port (with interrupt function)	SRXD	I	SIO receive signal
3	C3	FWR	I	Test mode input	–	–	
4	C1	RESET_N	I	Reset input	–	–	
5	D3	VDD_IO	VDD	IO power supply	–	–	
6	C2	XD[0]	I/O	External data bus	–	–	
7	D1	XD[1]	I/O	External data bus	–	–	
8	E3	XD[2]	I/O	External data bus	–	–	
9	D2	XD[3]	I/O	External data bus	–	–	
10	E1	XD[4]	I/O	External data bus	–	–	
11	E4	GND	GND	GND	–	–	
12	E2	CLKMD0	I	Clock mope input	–	–	
13	F1	XD[5]	I/O	External data bus	–	–	
14	F2	XD[6]	I/O	External data bus	–	–	
15	F4	GND	GND	GND	–	–	
16	F3	XD[7]	I/O	External data bus	–	–	
17	G2	CLKMD1	I	Clock mode input	–	–	
18	G4	VDD_IO	VDD	I/O power supply	–	–	
19	G3	XD[8]	I/O	External data bus	–	–	
20	G1	XD[9]	I/O	External data bus	–	–	
21	H3	XD[10]	I/O	External data bus	–	–	
22	H4	VDD_CORE	VDD	CORE power supply	–	–	
23	H2	NC	–	NC	–	–	
24	J2	XD[11]	I/O	External data bus	–	–	
25	H1	XD[12]	I/O	External data bus	–	–	
26	J4	VDD_IO	VDD	I/O power supply	–	–	
27	K2	XD[13]	I/O	External data bus	–	–	
28	J1	XD[14]	I/O	External data bus	–	–	
29	J3	XD[15]	I/O	External data bus	–	–	
30	K3	XA[0]	O	External address output	–	–	
31	K1	XA[1]	O	External address output	–	–	
32	L2	XA[2]	O	External address output	–	–	
33	K4	XA[3]	O	External address output	–	–	
34	L1	GND	GND	GND	–	–	
35	M2	XA[4]	O	External address output	–	–	
36	M1	XA[5]	O	External address output	–	–	
37	N1	XA[6]	O	External address output	–	–	
38	N2	XA[7]	O	External address output	–	–	
39	L3	XA[8]	O	External address output	–	–	
40	N3	XA[9]	O	External address output	–	–	
41	L4	VDD_IO	VDD	I/O power supply	–	–	
42	M3	XA[10]	O	External address output	–		
43	N4	XA[11]	O	External address output	–	–	
44	L5	XA[12]	O	External address output			

List of Pins (Continued)

Pin		Primary Function			Secondary Function		
LQFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description
45	M4	XA[13]	O	External address output			
46	N5	XA[14]	O	External address output			
47	K5	GND	GND	GND	–	–	
48	M5	XA[15]	O	External address output	–	–	
49	N6	XA[16]	O	External address output	–	–	
50	M6	XA[17]	O	External address output	–	–	
51	K6	GND	GND	GND	–	–	
52	L6	XA[18]	O	External address output	–	–	
53	M7	PIOC[2]	I/O	General port (with interrupt function)	XA[19]	O	External address output
54	K7	VDD_IO	VDD	I/O power supply	–	–	
55	L7	PIOC[3]	I/O	General port (with interrupt function)	XA[20]	O	External address output
56	N7	PIOC[4]	I/O	General port (with interrupt function)	XA[21]	O	External address output
57	L8	PIOC[5]	I/O	General port (with interrupt function)	XA[22]	O	External address output
58	K8	VDD_CORE	VDD	CORE power supply	–	–	
59	M8	PIOC[6]	I/O	General port (with interrupt function)	XA[23]	O	External address output
60	M9	PIOC[7]	I/O	General port (with interrupt function)	XWR	O	Transfer direction of external bus
61	N8	XOE_N	O	Output enable (excluding SDRAM)	–	–	
62	K9	VDD_IO	VDD	I/O power supply	–	–	
63	M10	XWE_N	O	Write enable	–	–	
64	N9	XBWE_N[0]	O	Write enable (LSB)	–	–	
65	L9	XBWE_N[1]	O	Write enable (MSB)	–	–	
66	L10	XROMCS_N	O	External ROM chip select	–	–	
67	N10	XRAMCS_N	O	External RAM chip select	–	–	
68	M11	XIOCS_N[0]	O	IO chip select 0	–	–	
69	K10	GND	GND	GND	–	–	
70	N11	XIOCS_N[1]	O	IO chip select 1	–	–	
71	M12	XIOCS_N[2]	O	IO chip select 2	–	–	
72	N12	XIOCS_N[3]	O	IO chip select 3	–	–	
73	N13	PIOD[6]	I/O	General port (with interrupt function)	XDQM[1]/XCAS_N[1]	O	INPUT/OUTPUT mask/CAS (MSB)
74	M13	PIOD[7]	I/O	General port (with interrupt function)	XDQM[0]/XCAS_N[0]	O	INPUT/OUTPUT mask/CAS (LSB)
75	L11	PIOB[0]	I/O	General port (with interrupt function)	DREQ[0]	I	DMA request signal (CH0)
76	L13	PIOB[1]	I/O	General port (with interrupt function)	DREQCLR[0]	O	DREQ Clear Signal (CH0)
77	K11	VDD_IO	VDD	I/O power supply	–	–	
78	L12	PIOB[2]	I/O	General port (with interrupt function)	DREQ[1]	I	DMA request signal (CH1)
79	K13	PIOB[3]	I/O	General port (with interrupt function)	DREQCLR[1]	O	DREQ Clear Signal (CH1)
80	J11	PIOB[4]	I/O	General port (with interrupt function)	TCOUT[0]	O	DMAC Terminal Count (CH0)
81	K12	PIOB[5]	I/O	General port (with interrupt function)	TCOUT[1]	O	DMAC Terminal Count (CH1)
82	J13	PIOC[0]	I/O	General port (with interrupt function)	PWMOUT[0]	O	PWM output (CH0)
83	J10	PIOC[1]	I/O	General port (with interrupt function)	PWMOUT[1]	O	PWM output (CH1)
84	J12	GND	GND	GND	–	–	
85	H13	XBS_N[0]	O	External bus byte select (LSB)	–	–	
86	H12	XBS_N[1]	O	External bus byte select (MSB)	–	–	
87	H10	VDD_CORE	VDD	CORE power supply	–	–	
88	H11	PIOD[0]	I/O	General port (with interrupt function)	XWAIT	I	Wait input signal for I/O Banks 0, 1
89	G12	PIOD[1]	I/O	General port (with interrupt function)	XCAS_N	O	Column address strobe (SDRAM)

List of Pins (Continued)

Pin		Primary Function			Secondary Function		
LQFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description
90	G10	GND	GND	GND	–	–	
91	G11	VDD_IO	VDD	I/O power supply	–	–	
92	G13	PIOD[2]	I/O	General port (with interrupt function)	XRAS_N	O	Row address strobe (SDRAM/EDO)
93	F11	PIOD[3]	I/O	General port (with interrupt function)	XSDCLK	O	Clock for SDRAM
94	F10	PIOD[4]	I/O	General port (with interrupt function)	XSDCS_N	O	Chip select for SDRAM
95	F12	PIOD[5]	I/O	General port (with interrupt function)	XSDCKE	O	Clock enable (SDRAM)
96	E12	BSEL[0]	I	Select boot device	–	–	
97	F13	BSEL[1]	I	Select boot device	–	–	
98	E10	PIOE[5]	I/O	General port (with interrupt function)	EXINT[0]	I	Interrupt input
99	D12	PIOE[6]	I/O	General port (with interrupt function)	EXINT[1]	I	Interrupt input
100	E13	PIOE[7]	I/O	General port (with interrupt function)	EXINT[2]	I	Interrupt input
101	E11	PIOE[8]	I/O	General port (with interrupt function)	EXINT[3]	I	Interrupt input
102	D11	PIOE[9]	I/O	General port (with interrupt function)	EFIQ_N	I	FIQ input
103	D13	PIOE[0]	I/O	General port (with interrupt function)	SCLK	I/O	SSIO clock
104	C12	PIOE[1]	I/O	General port (with interrupt function)	SDI	I	SSIO Serial Data In
105	D10	PIOE[2]	I/O	General port (with interrupt function)	SDO	O	SSIO Serial Data Out
106	C13	TDI	I	JTAG Data Input	–	–	
107	B12	TDO	O	JTAG data out	–	–	
108	B13	nTRST	I	JTAG reset	–	–	
109	A13	PLLVDD	VDD	Power supply for PLL	–	–	
110	A12	PLLGND	GND	GND for PLL	–	–	
111	C11	CKO	O	Clock output	–	–	
112	A11	JSEL	I	JTAG select	–	–	
113	C10	TMS	I	JTAG mode select	–	–	
114	B11	TCK	I	JTAG clock	–	–	
115	A10	DRAME_N	I	DRAM enable	–	–	
116	C9	CKOE_N	I	Clock out enable	–	–	
117	B10	GND	GND	GND	–	–	
118	A9	OSC0	I	Oscillation input pin	–	–	
119	D9	OSC1_N	O	Oscillation output pin	–	–	
120	B9	VDD_IO	VDD	IO power supply	–	–	
121	A8	TEST	I	Test Mode	–	–	
122	B8	PIOA[0]	I/O	General port (with interrupt function)	SIN	I	UART Serial Data In
123	D8	PIOA[1]	I/O	General port (with interrupt function)	SOUT	O	UART Serial Data Out
124	C8	AVDD	VDD	A/D Converter power supply	–	–	
125	B7	VREF	I	A/D Converter reference	–	–	
126	D7	AIN[0]	I	A/D Converter analog input port	–	–	
127	C7	AIN[1]	I	A/D Converter analog input port	–	–	
128	A7	AIN[2]	I	A/D Converter analog input port	–	–	
129	C6	AIN[3]	I	A/D Converter analog input port	–	–	
130	D6	AGND	GND	GND for A/D Converter			
131	B6	AGND	GND	GND for A/D Converter	–	–	
132	B5	GND	GND	GND	–	–	
133	A6	PIOA[2]	I/O	General port (with interrupt function)	CTS	I	UART Clear To Send
134	D5	VDD_IO	VDD	IO power supply	–	–	

List of Pins (Continued)

Pin		Primary Function			Secondary Function		
LQFP	BGA	Symbol	I/O	Description	Symbol	I/O	Description
135	B4	PIOA[3]	I/O	General port (with interrupt function)	DSR	I	UART Set Ready
136	A5	PIOA[4]	I/O	General port (with interrupt function)	DCD	I	UART Carrier Detect
137	C5	VDD_CORE	VDD	CORE power supply	–	–	
138	C4	PIOA[5]	I/O	General port (with interrupt function)	DTR	O	UART Data Terminal Ready
139	A4	PIOA[6]	I/O	General port (with interrupt function)	RTS	O	UART Request To Send
140	B3	PIOA[7]	I/O	General port (with interrupt function)	RI	I	UART Ring Indicator
141	D4	GND	GND	GND	–	–	
142	A3	PIOE[3]	I/O	General port (with interrupt function)	SDA	I/O	I2C Data In/Out
143	B2	PIOE[4]	I/O	General port (with interrupt function)	SCL	O	I2C Clock out
144	A2	PIOB[6]	I/O	General port (with interrupt function)	STXD	O	SIO send data output

Pin Descriptions

Pin Name	I/O	Description	Primary/ Secondary	Logic
System				
RESET_N	I	Reset input	–	Negative
BSEL[1:0]	I	Boot device select signal. BSEL[1] / BSEL[0] / Boot device 0 / 0 / Internal Flash (External ROM for ML675001) 0 / 1 / External ROM 1 / x / Boot ROM The selected device is mapped to BANK0 (0x0000_0000 - 0x07FF_FFFF) after reset. x = don't care	–	Positive
CLKMD[1:0]	I	Clock mode inputs. Normally connected to GND.	–	Positive
OSC0	I	Crystal oscillator connection or external clock input. If used, connect a crystal oscillator (5 MHz to 14 MHz) to OSC0 and OSC1_N. It is also possible to input a direct clock (5 MHz, 20 MHz to 56 MHz).	–	–
OSC1_N	O	Oscillation output pin. When not using a crystal oscillator, leave this pin unconnected.	–	–
CKO	O	Clock out.	–	–
CKOE_N	I	Clock out enable.	–	Negative
JTAG Interface				
TCK	I	Debugging pin. Normally connect to ground level.	–	–
TMS	I	Debugging pin. Normally drive at High level.	–	Positive
nTRST	I	Debugging pin. Normally connect to ground level.	–	Negative
TDI	I	Debugging pin. Normally drive at High level.	–	Positive
TDO	O	Debugging pin. Normally leave open.	–	Positive
General-purpose I/O Interface				
PIOA[7:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use.	Primary	Positive
PIOB[7:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use.	Primary	Positive
PIOC[7:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use.	Primary	Positive
PIOD[7:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use. Note that enabling the DRAM controller by asserting the DRAME_N inputs permanently configures PIOD[7:0] for their secondary functions, making them unavailable for use as port pins.	Primary	Positive
PIOE[9:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use.	Primary	Positive
External Bus Interface (Global)				
XA[23:19]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM. After a reset, these pins are configured for their primary function PIOC[6:2].	Secondary	Positive
XA[18:0]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM.	–	Positive
XD[15:0]	I/O	Data bus to external RAM, external ROM, external I/O banks, and external DRAM.	–	Positive
External Bus Interface (ROM, SRAM and I/O)				
XROMCS_N	O	ROM bank chip select.	–	Negative
XRAMCS_N	O	SRAM bank chip select.	–	Negative
XIOCS_N[0]	O	I/O chip select 0.	–	Negative
XIOCS_N[1]	O	I/O chip select 1.	–	Negative

Pin Descriptions

Pin Name	I/O	Description	Primary/ Secondary	Logic
XIOCS_N[2]	O	I/O chip select 2.	–	Negative
XIOCS_N[3]	O	I/O chip select 3.	–	Negative
XOE_N	O	Output enable/ Read enable.	–	Negative
XWE_N	O	Write enable.	–	Negative
XBS_N[1:0]	O	Byte select: XBS_N[1] is for MSB, XBS_N[0] is for LSB.	–	Negative
XBWE_N[0]	O	LSB Write enable.	–	Negative
XBWE_N[1]	O	MSB Write enable.	–	Negative
XWR	O	Data transfer direction for external bus, used when connecting to Motorola I/O devices. This represent the secondary function of pin PIOC[7]. L: read, H: write. Available for I/O bank 0/1	Secondary	–
XWAIT	I	External I/O bank 0/1/2/3 WAIT signal. This pin permits access to devices slower than register settings.	Secondary	Positive
External Bus Interface (EDO-DRAM and SDRAM)				
XRAS_N	O	Row address strobe. Used for both EDO DRAM and SDRAM.	Secondary	Negative
XCAS_N	O	Column address strobe signal (SDRAM).	Secondary	Negative
XSDCLK	O	SDRAM clock (same frequency as internal system clock).	Secondary	–
XSDCKE	O	Clock enable (SDRAM).	Secondary	–
XSDCS_N	O	Chip select (SDRAM).	Secondary	Negative
XDQM[1]/XCAS_N[1]	O	Connected to SDRAM: DQM (MSB). Connected to EDO-DRAM: column address strobe signal (MSB).	Secondary	Positive
XDQM[0]/XCAS_N[0]	O	Connected to SDRAM: DQM (LSB). Connected to EDO-DRAM: column address strobe signal (LSB).	Secondary	Positive
DMA Interface				
DREQ[0]	I	Channel 0 DMA request signal. Used then DMA controller is configured for DREQ type.	Secondary	Positive
DREQCLR[0]	O	Channel 0 DREQ signal clear request. The DMA device responds to the assertion of this signal by negating DREQ.	Secondary	Positive
TCOUT[0]	O	This signal is driven by the MCU and indicates to the Channel 0 DMA device that the last transfer of the DMA operation has started.	Secondary	Positive
DREQ[1]	I	Channel 1 DMA request signal. Used then DMA controller is configured for DREQ type.	Secondary	Positive
DREQCLR[1]	O	Channel 1 DREQ signal clear request. The DMA device responds to the assertion of this signal by negating DREQ.	Secondary	Positive
TCOUT[1]	O	This signal is driven by the MCU and indicates to the Channel 1 DMA device that the last transfer of the DMA operation has started.	Secondary	Positive
UART Interface				
SIN	I	SIO receive signal.	Secondary	Positive
SOUT	O	SIO transmit signal.	Secondary	Positive
CTS	I	Clear To Send. Indicates that modem or data set is ready to transfer data. Bit 4 in the modem status register reflects this input.	Secondary	Negative
DSR	I	Data Set Ready. Indicates that modem or data set is ready to establish a communications link with UART. Bit 5 in the modem status register reflects this input.	Secondary	Negative
DCD	I	Data Carrier Detect. Indicates that modem or data set has detected data carrier signal. Bit 7 in the modem status register reflects this input.	Secondary	Negative
DTR	O	Data Terminal Ready. Indicates that UART is ready to establish a communications link with the modem or data set. Bit 0 in the modem control register controls this output.	Secondary	Negative
RTS	O	Request To Send. indicates that UART is ready to transfer data to modem or data set. Bit 1 in the modem control register controls this output.	Secondary	Negative

Pin Descriptions

Pin Name	I/O	Description	Primary/ Secondary	Logic
RI	O	Ring Indicator. Indicates that the modem or data set has received a telephone ring indicator. Bit 6 in the modem status register reflects this input.	Secondary	Negative
SIO Interface				
STXD	O	SIO transmit signal.	Secondary	Positive
SRXD	I	SIO receive signal.	Secondary	Positive
I2C Interface				
SDA	I/O	I2C Data. This pin operates as NMOS Open drain. Connect pull-up resistor.	Secondary	—
SCL	O	I2C Clock. This pin operates as NMOS Open drain. Connect pull-up resistor.	Secondary	—
Synchronous SIO Interface				
SCLK	I/O	Serial clock.	Secondary	—
SDI	I	Serial receive data.	Secondary	—
SDO	O	Serial transmit data.	Secondary	—
Pulse Width Modulator (PWM) Interface				
PWMOUT[0]	O	PWM output of CH0.	Secondary	Positive
PWMOUT[1]	O	PWM output of CH1.	Secondary	Positive
Analog-to-digital Converter Interface				
AIN[0]	I	Ch0 analog input.	—	—
AIN[1]	I	Ch1 analog input.	—	—
AIN[2]	I	Ch2 analog input.	—	—
AIN[3]	I	Ch3 analog input.	—	—
VREF	I	Analog-to-digital converter convert reference voltage.	—	—
AVDD		Analog-to-digital converter power supply.	—	—
AGND		Analog-to-digital converter ground.	—	—
Interrupt Interface				
EXINT[3:0]	I	External interrupt input signals.	Secondary	Positive / Negative
EFIQ_N	I	External fast interrupt input signal. Interrupt controller connects this to CPU FIQ input.	Secondary	Negative
MODE Configuration Interface				
DRAME_N	I	DRAM enable mode.	—	Negative
TEST	I	Test mode.	—	Positive
TEST1	I	Test mode.	—	Positive
FWR	I	Test mode.	—	Positive
JSEL	I	JTAG select signal. L: On-board debug, H: Boundary scan.	—	—
Power and Ground Interface				
VDD_CORE		Core power supply.	—	—
VDD_IO		I/O power supply.	—	—
GND		GND for core and I/O.	—	—
PLLVDD		PLL power supply.		
PLLGND		GND for PLL.		

Electrical Characteristics

Absolute Maximum Ratings [1]

Item	Symbol	Conditions	Rating	Unit
Digital power supply voltage (core)	V_{DD_CORE}	GND = AGND = 0 V PLLGND = 0 V Ta = 25°C	-0.3 to +3.6	V
Digital power supply voltage (I/O)	V_{DD_IO}		-0.3 to +4.6	
PLL power supply voltage	V_{DD_PLL}		-0.3 to +3.6	
Input voltage	V_I		-0.3 to V_{DD_IO}+0.3	
Output voltage	V_O		-0.3 to V_{DD_IO}+0.3	
Analog power supply voltage	A_{VDD}		-0.3 to V_{DD_IO}+0.3	
Analog reference voltage	V_{REF}		-0.3 to V_{DD_IO}+0.3 and -0.3 to AV_{DD} +0.3	
Analog input voltage	V_{AI}		-0.3 to V_{REF}	
Input current	I_I		-10 to +10	mA
Output current [2]	I_O		-20 to +20	
Output current [3]			-30 to +30	
Power dissipation	P_D	LFBGA, Ta = 85°C per package	680	mW
		LQFP, Ta = 85°C per package	1000	mW
Storage temperature	T_{STG}	—	-50 to +150	°C

1. These are maximum ratings not for general operation. Exceeding these maximum ratings could cause damage or lead to permanent deterioration of the device.
2. All output pins except XA[15:0]
3. XA[15:0]

Recommended Operating Conditions

(GND = 0 V)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Digital power supply voltage (core)	V_{DD_CORE}	$V_{DD\_IO} \Delta V_{DD\_CORE}$	2.25	2.5	2.75	V
Digital power supply voltage (I/O)	V_{DD_IO}		3.0	3.3	3.6	
PLL power supply voltage	V_{DD_PLL}	$V_{DD\_PLL} = V_{DD\_CORE}$	2.25	2.5	2.75	
Analog power supply voltage	A_{VDD}	$A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Analog reference voltage	V_{REF}	$V_{REF} = A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Operating frequency [1]	f_{OP}	V_{DD_CORE} = 2.25 to 2.75, V_{DD_IO} = 3.0 to 3.6	1	—	60	MHz
Ambient temperature	Ta	—	-40	25	+85	°C

1. Oscillator frequencies between 5 MHz and 14 MHz. Minimum of 2.56 MHz for external SDRAM. Minimum of 6.4 MHz for external EDO-DRAM. Minimum of 2 MHz for analog-to-digital converter.

DC Characteristics

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = -40 to +85°C)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
High level input voltage	V_{IH}	—	V_{DD_IO}x0.8	—	V_{DD_IO}+0.3	V
Low level input voltage	V_{IL}		-0.3	—	V_{DD_IO}x0.2	
Schmitt input buffer threshold voltage	V_{T+}		—	1.6	2.1	
	V_{T-}		0.7	1.1	—	
	V_{HYS}		0.4	0.5	—	
High level output voltage	V_{OH}	I_{OH} = -100 µA	V_{DD}–0.2	—	—	
		I_{OH} = -4 mA	2.35	—	—	
Low level output voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.2	
Low level output voltage [1]		I_{OL} = 4 mA	—	—	0.45	
Low level output voltage [2]		I_{OL} = 6 mA	—	—	0.45	

DC Characteristics

(V_{DD_CORE} = 2.25 to 2.75V, V_{DD_IO} = 3.0 to 3.6V, Ta = -40 to +85°C)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input leakage current [3]	I_{IH}/I_{IL}	V_I = 0 V/V_{DD_IO}	-50	—	50	µA
Input leakage current [4]	I_{IL}	V_I = 0 V, Pull-up resistance of 50 kΣ	-200	-73	-10	
Input leakage current [5]	I_I	V_I = AV_{DD_IO} / 0 V	-5	—	5	
Output leakage current	I_{LO}	V_O = 0 V/V_{DD_IO}	-50	—	50	µA
Input pin capacitance	C_I	—	—	6	—	pF
Output pin capacitance	C_O	—	—	9	—	pF
I/O pin capacitance	C_{IO}	—	—	10	—	pF
Analog reference power supply current	I_{REF}	Analog-to-digital converter enabled [6]	—	320	650	µA
		Analog-to-digital converter disabled	—	1	2	
Current consumption (STANDBY)	I_{DDS_CORE}	Ta = 25°C [7]	—	20	150	µA
	I_{DDS_IO}		—	10	40	
Current consumption (HALT) [8]	I_{DDH_CORE}	f_{OP} = 60 MHz		37	55	mA
	I_{DDH_IO}	C_L = 30 pF	—	6	10	
Current consumption (RUN) [9]	I_{DD_CORE}		—	75	120	mA
	I_{DD_IO}		—	17	25	

1. All output pins except XA[15:0].
2. XA[15:0].
3. All input pins except RESET_N.
4. RESET_N pin, with 50 kΣ pull-up resistance.
5. Analog input pins (AIN0 to AIN3).
6. Analog-Digital Converter operation ratio is 20%.
7. V_{DD_IO} or 0 V for input ports; no load for other pins.
8. DRAM function stopped by deasserting the DRAME_N pin.
9. Cacheable setting and external ROM used.

Analog-to-Digital Converter Characteristics [1]

(V_{DD_CORE} = 2.50 V, V_{DD_IO} = 3.3 V, Ta = 25°C)

Item	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Resolution [2]	n	—	—	—	10	bit
Linearity error [3]	E_L	Analog input source impedance Ri Ω1kΣ	—	±3	—	LSB
Differential linearity error [4]	E_D		—	±3	—	
Zero scale error [5]	E_{ZS}		—	±3	—	
Full scale error [6]	E_{FS}		—	±3	—	
Conversion time	t_{CONV}	—	5	—	—	µs
Throughput		—	10	—	200	kHz

1. V_{DD_IO} and A_{VDD} should be supplied separately.
2. Resolution: Minimum input analog value recognized. For 10-bit resolution, this is (V_{REF} – A_{GND}) ÷1024.
3. Linearity error: Difference between the theoretical and actual conversion characteristics. (Note that it does not include quantization error.) The theoretical conversion characteristic divides the voltage range between V_{REF} and A_{GND} into 1024 equal steps.
4. Differential linearity error: Difference between the theoretical and actual input voltage change producing a 1-bit change in the digital output anywhere within the conversion range. This is an indicator of conversion characteristic smoothness. The theoretical value is (V_{REF} – A_{GND}) ÷ 1024.
5. Zero scale error: Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from "0x000" to "0x001."
6. Full scale error: Difference between the theoretical and actual conversion characteristics at the point where the digital output switches from "0x3FE" to "0x3FF."

Package Dimensions

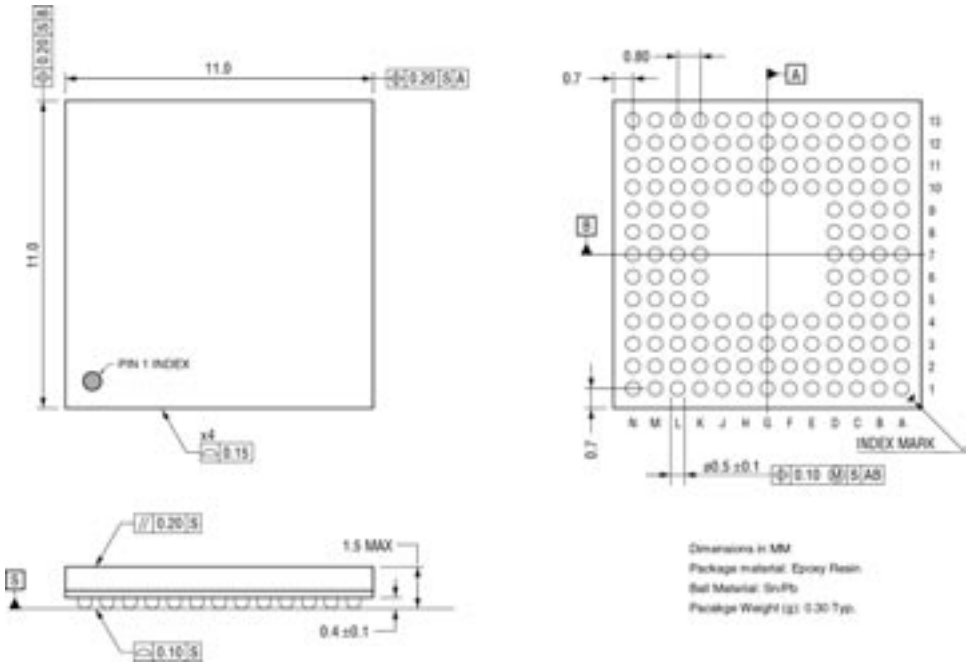


Figure 3. P-LFBGA144-1111-0.80

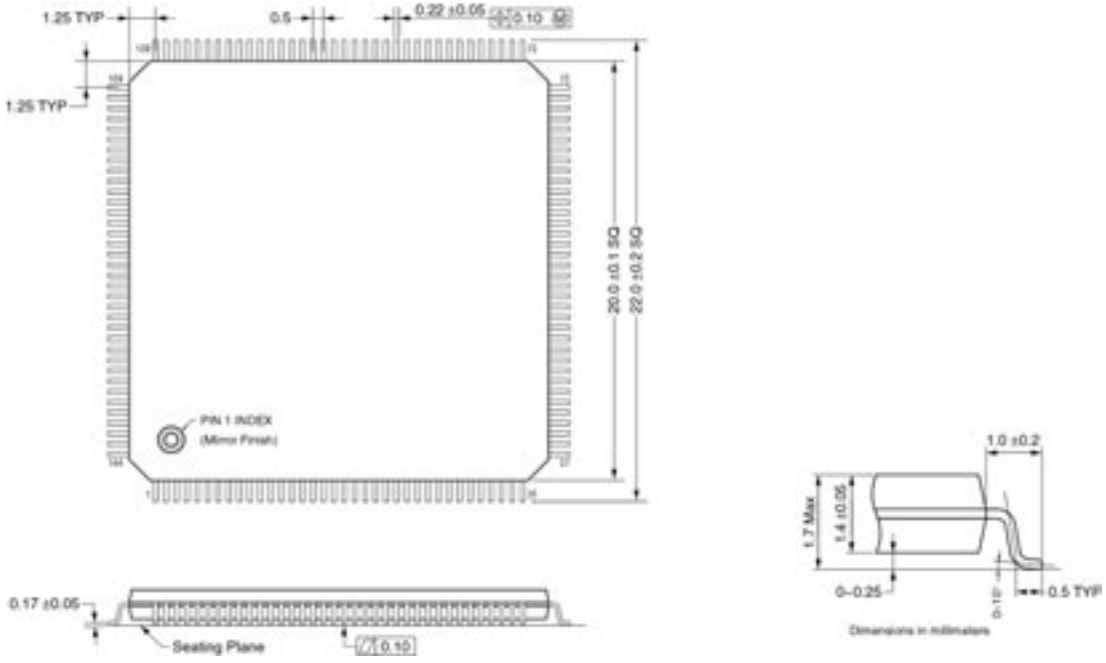


Figure 4. LQFP144-P-2020-0.50-K

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before performing reflow mounting, contact the Oki's sales department for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Related Oki Documents for the ML675001/2/3 [1]

Document	Date
ML674001/2/3 and ML5001/2/3 User's Manual	April, 2003
ML674001/2/3 and ML5001/2/3 Boot Program User's Manual	April, 2003
ML67Q4003 and ML67Q5003 Flash Memory User's Manual	April, 2003
ML67Q5003 CPU Board User's Manual	April, 2003
ML67Q5003 Power Management User's Manual	April, 2003
ML67Q5003 Sample Program User's Manual	April, 2003

1. Available on the Oki Semiconductor web site www.okisemi.com/us.

Notice

The information contained herein can change without notice owing to product and/or technical improvements.

Please make sure before using the product that the information you are referring to is up-to-date.

The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembly designs.

Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters outside the specified maximum ratings or operation outside the specified operating range.

Neither indemnity against nor license of a third party's industrial and intellectual property right,etc.is granted by us in connection with the use of product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges, including but not limited to operating voltage, power dissipation, and operating temperature.

The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by Oki, authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans. Such applications include, but are not limited to: traffic control, automotive, safety, aerospace, nuclear power control, and medical, including life support and maintenance.

Certain parts in this document may need governmental approval before they can be exported to certain countries. The purchaser assumes the responsibility of determining the legality of export of these parts and will take appropriate and necessary steps, at their own expense, for export to another country.

Oki Semiconductor reserves the right to make changes in specifications at anytime and without notice. This information furnished by Oki Semiconductor in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Oki Semiconductor for its use; nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Oki.

Trademarks:

µPlat is a trademark of Oki Semiconductor. ARM, ARM7TDMI, and the ARM Powered Logo are registered trademarks, and AMBA, ARM7, and Multi-ICE are trademarks of Advanced RISC Machines, Ltd.

Regional Sales Offices – Semiconductor Products

Northwest Area

785 N. Mary Avenue
Sunnyvale, CA 94085
Tel: 408/720-1900
Fax: 408/720-8965

Northeast Area

Shattuck Office Center
138 River Road
Andover, MA 01810
Tel: 978/688-8687
Fax: 978/688-8896

North Central Area

1450 East American Lane, Suite 1400
Schaumburg, IL 60143
Tel: 847/330-4494
847/330-4498
Fax: 847/330-4491

Southwest and South Central Area

1902 Wright Place, Suite 200
Carlsbad, CA 92008
Tel: 760/918-5830
Fax: 760/918-5505

Southeast Area

4800 Whitesburg Drive # 30
PMB 263
Huntsville, AL 35802
Tel: 256/520-8035
Fax: 408/737-6417

Oki Web Site:

http://www.okisemi.com/us

February 2004

Oki Semiconductor

Corporate Headquarters

785 N. Mary Avenue
Sunnyvale, CA 94085-2909
Tel: 408/720-1900
Fax: 408/720-1918