Systems and Peripherals Datasheet

R8051XC2 Microcontroller IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence R8051XC2 Microcontroller IP** is compliant with the Intel® MCS® 51 instruction set.

The **Cadence R8051XC2 Microcontroller IP** is a single-chip 8-bit microcontroller core that implements numerous processor variations executing the MCS 51 instruction set. Being fast, easily configurable and highly efficient, it runs on average 8.8X faster than the 80C51 at the same clock frequency.

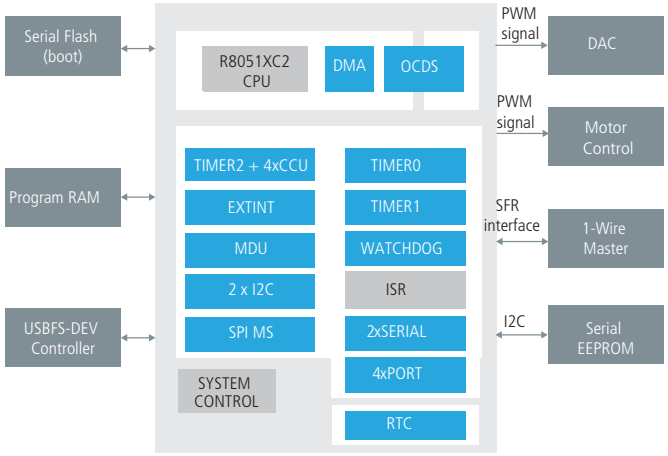

Figure 1: Example System-level Block Diagram

The **Cadence R8051XC2 Microcontroller IP** is architected to quickly and easily integrate into any SoC. The design matches specific application and hardware requirements, such as FPGA, ASIC, or structured ASIC. Available options include memory pointers, interrupts, interfaces for serial communication, I2C, and SPI interfaces, among many others.

Designed to run at frequencies exceeding 400MHz on a typical 90nm process, the **Cadence R8051XC2 Microcontroller IP** uses 7K to 70K gates, depending on technology and configuration used. It offers a technology-independent design that can be implemented in a variety of process technologies, since it eliminates redundant bus states and implements parallel processing of fetch and execution phases.

Cadence SoC Peripheral IP is silicon proven and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

Key Features

- Compliant with Intel MCS 51 instruction set
- 16 x 16-bit multiplication, 32/16 and 16/16-bit division, 32-bit normalization and L/R shifting
- Extensive core configurability (user configurable versions and custom configurations available) combined with the best power usage per DMIPS
- 36 to 119 External Special Function Registers, power-down modes (IDLE/STOP), OCDS, OCDS One Wire, two-option interrupt controller
- External memory interface with up to 8MB program and data memory, additional arithmetic unit, external DMA controller, and program memory write mode
- Up to eight independent DMA controller channels, read/write access to all memory spaces, up to 8MB linear addressing, address auto-increment/decrement

Product Details

The **Cadence R8051XC2 Microcontroller IP**, as a single-chip 8-bit microcontroller core designed in a highly efficient way, belongs to the proven 8051 family of processor cores that have so far seen their successful implementation in hundreds of various customer products.

CPU (Central Processing Unit)

The CPU fetches instructions from program memory, using RAM or SFR interfaces as operands. Both these interfaces can address up to 256 bytes of Read/Write Data Memory Space, as well as built-in and off-core SFRs. CPU provides the ALU for 8-bit arithmetic, logic, multiplication operations, division operations and Boolean manipulations.

DMA Controller

The direct memory access (DMA) controller contains up to eight individual channels, each capable of transferring data from or to any addressable location (program memory, SFR, internal or external data memory), allowing every channel to operate in synchronous or asynchronous mode.

OCDS

The OCDS unit serves as the interface for EASE through either IEEE1149.1 (JTAG) or SWORD (One Wire) port, offering functions such as: run, stop, single-step, software breakpoint, debugger program execution, hardware breakpoints, read/write access to program memory, external/internal data memory and SFRs, program trace and data trace (optional).

Unit Types

This core consists of various units, including 4xCCU (compare-capture Unit), which performs compare and capture functions, MDU (multiplication division unit) used for performing unsigned integer operations and ISR (interrupt service routine unit), which provides the core with two types of interrupt controllers.

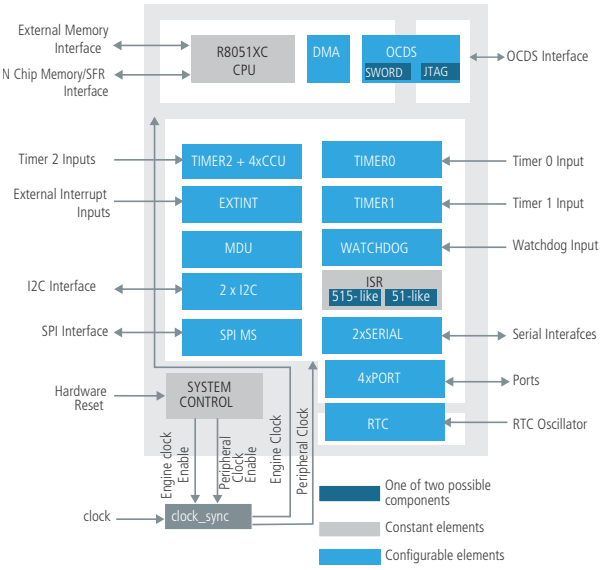

Figure 2: IP-level Block Diagram

2x I2C and SPI Interfaces

The primary and secondary I2C bus controllers provide a serial interface that meets the Philips I2C bus specification 2.1 and support all master/slave receiver/transmitter modes. Each is a true multi-master bus controller, including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer. SPI provides full-duplex, synchronous communication between the core and other peripheral devices, including other MCUs. It operates as master or slave, with programmable clock rate, phase, and polarity.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of SoC Peripheral IP to meet your design requirements.

For more information, visit ip.cadence.com

Benefits

- Low-risk solutions—Silicon-proven design
- Fully configurable—easy interrupts setting
- Ease-of-use—customizable with easy integration

Related Products

- EASE-8051 IP

Deliverables

- Clean, readable, synthesizable Verilog HDL, VHDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- R8051XC2 Microcontroller IP

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