TERIDIAN
SEMICONDUCTOR CORP.

73S1215F

80515 System-on-Chip with USB, ISO-7816 / EMV, PINpad and more

PRELIMINARY DATA SHEET

Jan 2006

GENERAL DESCRIPTION

The TERIDIAN Semiconductor Corporation 73S1215F is an 8-bit, high performance, low-cost CMOS System-on-Chip dedicated to smart card reader applications. The circuit features primarily an ISO-7816 / EMV interface, an USB 2.0 interface (full-speed 12Mbps - slave) and a 5x6 PINpad interface. Maximum design flexibility is supported with additional features such as up to 9 user I/Os, multiple interrupts, up to 4 current programmable outputs (to drive external LEDs), and 1 analog voltage input (suitable for DC voltage monitoring like battery level detection). Other built-in hardware interfaces include an asynchronous serial and an I^2C interface.

The System-on-Chip is built around an 80515 high-performance core. Its feature set is compatible with the industry standard 8051, while offering one clock-cycle per instruction processing power (most instructions). With a CPU clock running up to 24MHz, it results in up to 24MIPS available that meets the requirements of various encryption needs such as AES, DES / 3-DES and even RSA (for PIN encryption for instance). The circuit requires a single crystal, which frequency can be between 4MHz and 16MHz. In addition, a 32kHz sub-system oscillator (optional) with an independent real-time-clock counter enables stand-alone applications to access an RTC value. The respective 73S1215F embedded memories are; 64KB Flash program memory, 2KB user XRAM memory, and 256B IRAM memory. On top of these memories are added independent FIFOs dedicated to the ISO7816 UART and to the USB interface. Overall, the 73S1215F offers a cost effective solution to implement hand-held PINpad smart card readers - USB connected, serial connected, standalone or combo – as well as turnkey smart card reader modules, USB or ExpressCard^{TM} type.

Embedded Flash memory is in-system programmable and lockable by means of on-silicon fuses. This makes the TERIDIAN 73S1215F suitable for both development and production phases.

For high-volume and very low-cost applications, TERIDIAN Semiconductor Corporation offers migration to a masked-ROM version, as well as die form.

TERIDIAN Semiconductor Corporation offers with its 73S1215F a very comprehensive set of software libraries, including the smart card and USB protocol layers that are pre-approved against USB, Microsoft WHQL and EMV, as well as a CCID reference design. Refer to the TERIDIAN Semiconductor Corporation 73S12xx Software User's Guide for a complete description of the Application Programming Interface (API Libraries) and related Software modules.

A complete array of development and programming tools, libraries and demonstration boards enable rapid development and certification of smart card readers that meet most demanding smart card standards.

APPLICATIONS

- **Hand-held PINpad smart card readers:**

→ **Connected through USB, serial or un-connected**

→ **CCID-compliant**

- **E-banking (MasterCard CAP, etc)**
- **Smart card reader modules for PC laptops and desktops: ExpressCard™ , USB**
- **Digital Identification (Secure Login, Gov't ID...)**
- **General purpose smart card readers**

ADVANTAGES

- **The ideal compromise cost / features for high volume, USB-connected PINpad type of applications:**
  - o **Larger built-in Flash / RAM than its competitors**
  - o **Higher performance CPU core**
  - o **Powerful JTAG In-Circuit- Emulation and Programming**
  - o **A unique set of ready-to-use EMV4.1 / USB / CCID libraries**

[1]

Designed for Microsoft® Windows® XP

CERTIFIED USB

EMVCo

[1] Pending

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FEATURES

80515 core:

- 1 clock cycle per instruction (most instructions)
- CPU clocked up to 24MHz
- 64kB Flash memory with security
- 2kB XRAM (User Data Memory)
- 256 byte IRAM
- Hardware watchdog timer

Oscillators:

- Single low-cost 4MHz to 16MHz crystal
- Optional 32kHz crystal (with internal RTC)
- An Internal PLL provides all the necessary clocks to each block of the system

Interrupts:

- Standard 80C515 4-priority level structure
- 9 different sources of interrupt to the core

Power Down Modes:

- 2 standard 80C515 Power Down and IDLE modes
- Extensive device power down mode

Timers:

- (2) Standard 80C52 timers T0 and T1
- (1) 16-bit timer that can generate RTC interrupts from the 32kHz clock

Built-in ISO-7816 card interface:

- LDO regulator produces VCC for the card (1.8V, 3V or 5V)
- Full compliance with EMV 4.1
- Activation/Deactivation sequencers
- Auxiliary I/O lines (C4-C8 signals)
- 6kV ESD protection on all interface pins

Communication with smart cards:

- ISO-7816 UART 9600 to 115kbps for protocols T=0, T=1
- (2) 2-Byte FIFOs for transmit and receive
- Possibility to drive external Teridian 73S8010x interfaces (for multi-SAM architectures)

Communication interfaces:

- Full-duplex serial interface (1200 to 115kbps UART)
- USB 2.0 Full Speed 12Mbps Interface, PC/SC compliant with 4 Endpoints:
  - Control (16B FIFO)
  - Interrupt IN (32B FIFO)
  - Bulk IN (128B FIFO)
  - Bulk OUT (128B FIFO)
- I^{2}C Master Interface (400kbps)

Man-Machine Interface and I/Os:

- 5x6 Keyboard (hardware scanning, debouncing and scrambling)
- (9) User I/Os
- Up to 4 programmable current outputs (LED)

Voltage Detection:

- Analog Input (detection range: 0.2V to 2.5V)

Operating Voltage:

- 2.7V to 3.6V (3V to 3.6V when USB is in use)
- 4.75 to 5.5V for smart card supply

Operating Temperature:

- -40°C to 85°C

Package:

- 68 pin QFN, 44 pin QFN, Die form

Software:

- Two-level Application Programming Interface (ANSI C-language libraries)
- USB, T=0/T=1 and EMV-compliant smart card protocol layers
- CCID reference design and Windows driver

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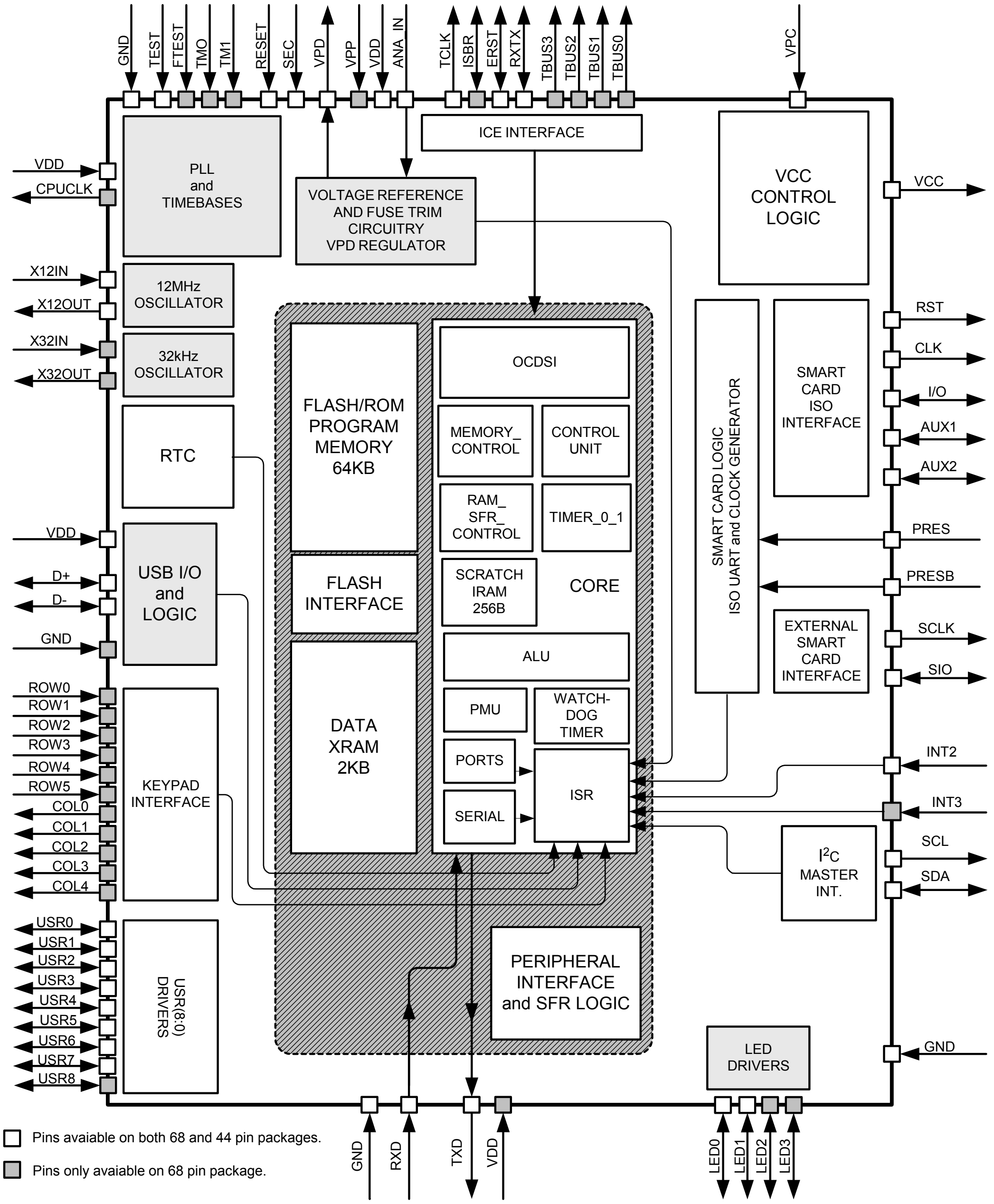


Figure 1: IC Functional Block Diagram

HARDWARE DESCRIPTION

Pin Description

Pin Name		Pin (68 QFN)	Pin (44 QFN)	Type	Description
X12IN		10	8	I	MPU/USB clock crystal oscillator input pin. A 12MHz crystal is required for USB operation. A 1M ohm resistor is required between pins X12IN and X12OUT
X12OUT		11	9	O	MPU/USB clock crystal oscillator output pin
X32IN		8		I	RTC clock crystal oscillator input pin. A 32768Hz crystal is required for low-power RTC operation
X32OUT		7		O	RTC clock crystal oscillator output pin
CPUCLK		39		O	Output signal, square wave at the frequency of the MPU clock
DP		26	16	IO	USB D+ IO pin, requires series 27 ohm resistor
DM		27	17	IO	USB D- IO pin, requires series 27 ohm resistor
ROW(5:0)	0	21		I	Keypad row input sense
	1	22			
	2	24			
	3	34			
	4	37			
	5	38			
COL(4:0)	0	12		O	Keypad column output scan pins
	1	13			
	2	14			
	3	16			
	4	19			
USR(8:0)	0	36	24	IO	General-purpose user pins, individually configurable as inputs or outputs or as external input interrupt ports
	1	35	23		
	2	33	22		
	3	31	21		
	4	30	20		
	5	29	19		
	6	23	14		
	7	20	13		
	8	32			
SCL		5	5	O	I^2C (master mode) compatible Clock signal
SDA		6	6	IO	I^2C (master mode) compatible data I/O

Pin Name		Pin (68 QFN)	Pin (44 QFN)	Type	Description
LED(3:0)	0	1	3	IO	Special output drivers, programmable pull-down current to drive LEDs. May also be used as inputs.
	1	3	4		
	2	2			
	3	4			
RXD		17	11	I	Serial UART Receive data pin.
TXD		18	12	O	Serial UART Transmit data pin.
INT3		51		I	General purpose interrupt input
INT2		52	32	I	General purpose interrupt input
SIO		50	31	IO	IO data signal for use with external Smart Card interface circuit such as 73S8024.
SCLK		48	30	O	Clock signal for use with external Smart Card interface circuit.
PRES		64	43	I	Smart Card presence. Active high
PRESB		56	35	I	Smart Card presence. Active low
CLK		57	36	O	Smart card clock signal
RST		59	38	O	Smart card Reset signal
IO		63	42	IO	Smart card Data IO signal
AUX1		62	41	IO	Auxiliary Smart Card IO signal (C4)
AUX2		61	40	IO	Auxiliary Smart Card IO signal (C8)
VCC		60	39	PSO	Smart Card VCC supply voltage output
GND		58	37	GND	Smart Card Ground
VPC		55	34	PSI	Smart Card LDO regulator power supply source.
TBUS(3:0)	0	53		IO	Trace bus signals for ICE
	1	49			
	2	47			
	3	43			
RXTX		45	28	IO	ICE control
ERST		40	25	IO	ICE control
ISBR		68		IO	ICE control
TCLK		41	26	I	ICE control
ANA_IN		15	10	AI	Analog input pin. This signal goes to a programmable comparator and is used to sense the value of an external voltage.

Pin Name	Pin (68 QFN)	Pin (44 QFN)	Type	Description
SEC	67	2	I	Input pin for use in programming security fuse and selecting test modes
TEST	54	33	DI	Test pin, should be left unconnected.
VDD	28 42 65	18 27 44	I	General positive power supply pins. All digital IO is referred to this supply voltage. There is an on-chip regulator that uses VDD to provide power for internal circuits (VPD)
VPD	46	29	0	Internal positive logic power supply. Only a 0.1uF bypass capacitor should be connected to this pin.
GND	9 25 44	7 15	GND	General ground supply pins for all IO and logic circuits.
RESET	66	1	I	Reset input, positive assertion. Resets logic and registers to default condition.

Table 1: 73S1215 Pinout Description

Hardware Overview

The TERIDIAN 73S1215F single smart card controller integrates all primary functional blocks required to implement a smart card reader. Included on chip are an 8051-compatible microprocessor (MPU) which executes up to one instruction per clock cycle (80515), a fully integrated IS0-7816 compliant smart card interface, expansion smart card interface, full speed USB 2.0 compatible interface, serial interface, I2C interface, 6 x 5 keypad interface, 4 LED drivers, RAM, FLASH memory, a real time clock (RTC), and a variety of I/O pins. A functional block diagram of the 73S1215F is shown in Figure 1.

80515 MPU Core

80515 Overview

The 73S1215F includes an 80515 MPU (8-bit, 8051-compatible) that performs most instructions in one clock cycle. Using a 4MHz clock results in a processing throughput of up to 4 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency.

Actual processor clocking speed can be adjusted to the total processing demand of the application (cryptographic calculations, key management, memory management, and I/O management) using the XRAM special function register *MPUCKCtl [5:0]*.

Typical smart card, USB, serial, keyboard, I2C, and RTC management functions are available for the MPU as part of TERIDIAN's standard library. A standard ANSI "C" 80515-application programming interface library is available to help reduce design cycle. Refer to the 12XX Software Users Guide.

Memory Organization

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces.

Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (Flash), external data memory (XRAM), and internal data memory (IRAM). Data bus address space is allocated to on-chip memory as shown Table 2

Address (hex)	Memory Technology	Memory Type	Typical Usage	Memory Size (bytes)
0000-FFFF	Flash Memory	Non-volatile	Program and non-volatile data	64KB
0000-07FF	Static RAM	Volatile	MPU data XRAM,	2KB
FC00-FFFF	External SFR	Volatile	Peripheral control	1KB

Note: The IRAM is part of the core and is addressed differently.

Table 2: MPU Data Memory Map

Program Memory: The 80515 can address up to 64KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation. After reset, the MPU starts program execution from location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003 (Reset is located at 0x0000).

Flash Memory: The program memory consists of flash memory. The flash memory is intended to primarily contain MPU program code. Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

1. Write 1 to the *FLSH_MEEN* bit (SFR address 0xB2[1].
2. Write pattern 0xAA to *FLSH_ERASE* (SFR address 0x94)

Note: The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to *FLSH_PGADR* (SFR address 0xB7[7:1])
2. Write pattern 0x55 to *FLSH_ERASE* (SFR address 0x94)

The MPU may write to the flash memory. This is one of the non-volatile storage options available to the user. The *FLSHCRL* SFR bit *FLSH_PWE* (flash program write enable) differentiates 80515 data store instructions (MOVX@DPTR,A) between Flash and XRAM writes. Before setting *FLSH_PWE*, all interrupts need to be disabled by setting EAL = 1. Table 3 shows the location and description of the 73S1215 flash-specific SFRs.

Note: Any flash operations must set the CPUCLK to operate at 3.6923 MHz (MPUCLKCtl = 0x0C) before any flash memory operations are executed to insure the proper timing when modifying the flash memory.

Register	Alternative Name	SFR Address	R/W	Description
ERASE	*FLSH_ERASE*	0x94	W	This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for *FLSH_ERASE* in order to initiate the appropriate Erase cycle (default = 0x00). 0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a write to *FLSH_PGADR* @ SFR 0xB7. 0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a write to *FLSH_MEEN* @ SFR 0xB2 and the debug port must be enabled. Any other pattern written to FLSH_ERASE will have no effect.
PGADDR	*FLSH_PGADR*	0xB7	R/W	Flash Page Erase Address register containing the flash memory page address (page 0 thru 127) that will be erased during the Page Erase cycle (default = 0x00). Must be re-written for each new Page Erase cycle.
FLSHCRL		0xB2	R/W	Bit 0 (*FLSH_PWE*): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
			W	Bit 1 (*FLSH_MEEN*): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
			R/W	Bit 6 (*SECURE*): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
			R	Bit 7 (*PREBOOT*): Indicates that the preboot sequence is active.

Register	Alternative Name	SFR Address	R/W	Description

SECReg		0xFFD7	W	Bit 7 (PARAMSEC):
				0 – Normal operation
				1 - Enable permanent programming of the security fuses.
				Bit 5 (SECPIN):
				Indicates the state of the SEC pin. The SEC pin is held low by a pull-down resistor. The user can force this pin high during boot sequence time to indicate to firmware that sec mode 1 is desired.
				Bit 1 (SECSET1):
				See Program Security section
				Bit 0 (SECSET0):

Table 3: Flash Special Function Registers

Internal Data Memory: The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always one byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addressees 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 4 shows the internal data memory map.

Address	Direct addressing	Indirect addressing
0xFF	Special Function Registers (SFRs)	RAM
0x80		
0x7F	Byte-addressable area	
0x30		
0x2F	Byte or bit-addressable area	
0x20		
0x1F	Register banks R0…R7 (x4)	
0x00		

Table 4: Internal Data Memory Map

External Data Memory: While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 2 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction.

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. This method allows the user access to the first 256 bytes of the 2KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address.

Address	Use
0xFFFF	Flash Program memory 64K Bytes
0x0000	
Program memory	

Address	Use
0xFFFF	Peripheral Control Registers (128b)
0XFF80	
0xFF7F	Smart Card Control (384b)
0XFE00	
0xFDFF	USB Registers (512b)
0XFC00	
0xFBFF	---
0x0800	
0x07FF	XRAM
0x0000	
External data memory	

Address	Use	
	Indirect Access	Direct Access
0xFF	Byte RAM	SFRs
0x80		
0x7F	Byte RAM	
0x48		
0x47	Bit/Byte RAM	
0x20		
0x1F	Register bank 3	
0x18		
0x17	Register bank 2	
0x10		
0x0F	Register bank 1	
0x08		
0x07	Register bank 0	
0x00		
Internal data memory		

Figure 2: Memory Map

Dual Data Pointer: The Dual Data Pointer accelerates the block moves of data. The standard DPTR is a 16-bit register that is used to address external memory. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located at the LSB of the DPS IRAM special function register (DPS.0). DPTR is selected when DPS.0 = 0 and DPTR1 is selected when DPS.0 = 1.

The user switches between pointers by toggling the LSB of the DPS register. All DPTR-related instructions use the currently selected DPTR for any activity.

Note: The second data pointer may not be supported by certain compilers.

Program Security

Two levels of program and data security are available. Mode 0 security, when enabled by setting the SECSEC0 bit, limits the ICE to only bulk erase of the flash program memory. All other ICE operations are blocked. This guarantees the security of the user's MPU program code. Security (mode0) is enabled by MPU code that is executed in a 32 clock cycle pre-boot interval which sets bit 6 of SFR register FLSHCRL (0xB2). The pre-boot sequence occurs before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the flash followed by a full circuit reset. Global erase of the flash will also clear the data XRAM memory.

The first 32 MPU cycles of the boot is called pre-boot because the ICE is inhibited. A read-only status bit, PREBOOT (SFR 0xB2[7]), identifies these cycles to the MPU. Upon completion of pre-boot, the ICE is fully enabled and is permitted to take control.

The security enable bit SECURE (SFR 0xB2[6]) is reset whenever the MPU is reset. Hardware associated with the bit only allows it to be set. Thus, preboot code may set the SECURE bit to enable the security feature but may not reset it. Once SECURE is set, the preboot code is protected and no external read of program code in flash or data (in XRAM) is possible. In order to invoke the security mode, the SECURE bit must be programmed beforehand. The SECSETx fuses cannot be overridden.

Specifically, when *SECURE* is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's preboot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases XRAM whether the SECURE bit is set or not.
- Writes to page zero, whether by MPU or ICE, are inhibited.

Security mode 1 is in effect when the SECSET1 fuse has been programmed (open). In security mode 1, the ICE is completely disabled. The Flash program memory and the MPU are not available for alteration, observation, nor control. The state of this bit is determined by the state of the SEC pin (or is the SECPIN has been set under firmware control). The SEC pin shall be set to = VDD and when all the other fuse programming criteria are met, the SEC2 fuse bit shall be programmed. Page erase and writes to page 0 by the MPU are not allowed. This fuse condition is not related to nor affected by, firmware or program code. As soon as the fuse has been blown, the ICE is disabled. This will occur during the reset and before the start of pre-boot and boot cycles. This mode is not reversible, nor recoverable.

Special Function Registers (SFRs)

The 1215 utilizes numerous SFRs to communicate with the 1215s many peripherals. This results in the need for more SFR locations outside the direct address IRAM space (0x80 to 0xFF). While some peripherals are mapped to unused IRAM SFR locations, additional SFRs for the USB, smart card and other peripheral functions are mapped to the top of the XRAM data space (0xFC00 to 0xFFFF).

Internal Data Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 5.

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8									FF
F0	*B*								F7
E8									EF
E0	*A*								E7
D8	*BRCON*								DF
D0	*PSW*	***KCOL***	***KROW***	***KSCAN***	***KSTAT***	***KSIZE***	***KORDERL***	***KORDERH***	D7
C8	*T2CON*								CF
C0	*IRCON*								C7
B8	*IEN1*	*IP1*	*S0RELH*	*S1RELH*					BF
B0			***FLSHCTL***					***PGADR***	B7
A8	*IEN0*	*IP0*	*S0RELL*						AF
A0	***USR8***	***UDIR8***							A7
98	*S0CON*	*S0BUF*	*IEN2*	*S1CON*	*S1BUF*	*S1RELL*			9F
90	***USR70***	***UDIR70***	*DPS*		***ERASE***				97
88	*TCON*	*TMOD*	*TL0*	*TL1*	*TH0*	*TH1*		***MCLKCTL***	8F
80		*SP*	*DPL*	*DPH*	*DPL1*	*DPH1*	*WDTREL*	*PCON*	87

Table 5: IRAM Special Function Registers Locations

Only a few addresses are used, the others are not implemented. SFRs specific to the 1215 are shown in **bold** print (gray background). Any read access to unimplemented addresses will return undefined data, while most write access will have no effect. However, a few locations are reserved, but not user configurable in the 1215. **Writes to the unused SFR locations can affect the operation of the core and therefore must not be written to. This applies to all the SFR areas in both the IRAM and XRAM spaces.**

IRAM Special Function Registers (Generic 80515 SFRs)

Table 6 shows the location of the SFRs and the value they assume at reset or power-up.

Name	Location	Reset value	Description
SP	0x81	0x07	Stack Pointer
DPL	0x82	0x00	Data Pointer Low 0
DPH	0x83	0x00	Data Pointer High 0
DPL1	0x84	0x00	Data Pointer Low 1
DPH1	0x85	0x00	Data Pointer High 1
WDTREL	0x86	0x00	Watchdog Timer Reload register
PCON	0x87	0x00	Power Control
TCON	0x88	0x00	Timer/Counter Control
TMOD	0x89	0x00	Timer Mode Control
TL0	0x8A	0x00	Timer 0, low byte
TL1	0x8B	0x00	Timer 1, high byte
TH0	0x8C	0x00	Timer 0, low byte
TH1	0x8D	0x00	Timer 1, high byte
MCLKCTL	0x8F	0x0A	Master Clock Control
USR70	0x90	0xFF	User Port Data (7:0)
UDIR70	0x91	0xFF	User Port Direction (7:0)
DPS	0x92	0x00	Data Pointer select Register
ERASE	0x94	0x00	Flash Erase
S0CON	0x98	0x00	Serial Port 0, Control Register
S0BUF	0x99	0x00	Serial Port 0, Data Buffer
IEN2	0x9A	0x00	Interrupt Enable Register 2
S1CON	0x9B	0x00	Serial Port 1, Control Register
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte
USR8	0xA0	0x00	User Port Data (8)
UDIR8	0x91	0x01	User Port Direction (8)
IEN0	0xA8	0x00	Interrupt Enable Register 0
IP0	0xA9	0x00	Interrupt Priority Register 0
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte
FLSHCTL	0xB2	0x00	Flash Control
IEN1	0xB8	0x00	Interrupt Enable Register 1
IP1	0xB9	0x00	Interrupt Priority Register 1
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte
IRCON	0xC0	0x00	Interrupt Request Control Register
T2CON	0xC8	0x00	Timer 2 Control
PSW	0xD0	0x00	Program Status Word
KCOL	0XD1	0x1F	KEYPAD COLUMN
KROW	0XD2	0x3F	KEYPAD ROW
KSCAN	0XD3	0x00	KEYPAD SCAN TIME

Name	Location	Reset value	Description
KSTAT	0XD4	0x00	KEYPAD CONTROL/STATUS
KSIZE	0XD5	0x00	KEYPAD SIZE
KORDERL	0XD6	0x00	KEYPAD COLUMN LS SCAN ORDER
KORDERH	0XD7	0x00	KEYPAD COLUMN MS SCAN ORDER
BRCON	0xD8	0x00	Baud Rate Control Register (only BRCON.7 bit used)
A	0xE0	0x00	Accumulator
B	0xF0	0x00	B Register

Table 6: IRAM Special Function Registers Reset Values

External Data Special Function Registers (SFRs)

A map of the XRAM Special Function Registers is shown in Table 5.

Name	Location	Reset value	Description
DAR	0x FF80	0x00	Device Address Register (I^2C)
WDR	0x FF81	0x00	Write Data Register (I^2C)
TWDR	0x FF82	0x00	Test Write Data Register (I^2C)
RDR	0x FF83	0x00	Read Data Register (I^2C)
TRDR	0x FF84	0x00	Test Read Data Register (I^2C)
CSR	0x FF85	0x00	Control and Status Register (I^2C)
USRIntCtl1	0x FF90	0x00	External Interrupt Control 1
USRIntCtl2	0x FF91	0x00	External Interrupt Control 2
USRIntCtl3	0x FF92	0x00	External Interrupt Control 3
USRIntCtl4	0x FF93	0x00	External Interrupt Control 4
INT5Ctl	0x FF94	0x00	External Interrupt Control 5
INT6Ctl	0x FF95	0x00	External Interrupt Control 6
MPUCKCtl	0x FFA1	0x0C	MPU Clock Control
RTCCtl	0x FFB0	0x81	Real Time Clock Control
RTCCnt3	0x FFB1	0x00	RTC Count 3
RTCCnt2	0x FFB2	0x00	RTC Count 2
RTCCnt1	0x FFB3	0x00	RTC Count 1
RTCCnt0	0x FFB4	0x00	RTC Count 0
RTCACC2	0x FFB5	0x00	RTC Accumulator 2
RTCACC1	0x FFB6	0x00	RTC Accumulator 1
RTCACC0	0x FFB7	0x00	RTC Accumulator 0
RTCTrim2	0x FFB8	0x00	RTC TRIM 2
RTCTrim1	0x FFB9	0x00	RTC TRIM 1
RTCTrim0	0x FFBA	0x00	RTC TRIM 0

Name	Location	Reset value	Description
ACOMP	0x FFD0	0x00	Analog Compare Register
TRIMPCtl	0x FFD1	0x00	TRIM Pulse Control
FUSECtl	0x FFD2	0x00	FUSE Control
VRCtl	0x FFD3	0x00	VREF Control
VDDFCtl	0x FFD4	0x00	VDDFault Control
LEDCal	0x FFD5	0x00	LED Calibrate Register
LOCKCtl	0x FFD6	0x00	LOCK Control Register
SECReg	0x FFD7	0x00	Security Register
MISCtl0	0x FFF1	0x00	Miscellaneous Control Register 0
MISCtl1	0x FFF2	0x10	Miscellaneous Control Register 1
LEDCtl	0x FFF3	0xFF	LED Control Register

Table 7: XRAM Special Function Registers Reset Values

Accumulator (ACC, A): ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as “A”, not ACC.

B Register: The B register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

Program Status Word (PSW):

MSB							LSB
CV	AC	F0	RS1	RS	OV	-	P

Table 8: PSW Register Flags

<table>
<tr><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>PSW.7</td><td>CV</td><td>Carry flag.</td></tr>
<tr><td>PSW.6</td><td>AC</td><td>Auxiliary Carry flag for BCD operations.</td></tr>
<tr><td>PSW.5</td><td>F0</td><td>General purpose Flag 0 available for user.</td></tr>
<tr><td>PSW.4</td><td>RS1</td><td rowspan="2">Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
<table>
<tr><th>RS1/RS0</th><th>Bank selected</th><th>Location</th></tr>
<tr><td>00</td><td>Bank 0</td><td>(0x00 – 0x07)</td></tr>
<tr><td>01</td><td>Bank 1</td><td>(0x08 – 0x0F)</td></tr>
<tr><td>10</td><td>Bank 2</td><td>(0x10 – 0x17)</td></tr>
<tr><td>11</td><td>Bank 3</td><td>(0x18 – 0x1F)</td></tr>
</table></td></tr>
<tr><td>PSW.3</td><td>RS0</td></tr>
<tr><td>PSW.2</td><td>OV</td><td>Overflow flag.</td></tr>
<tr><td>PSW.1</td><td>F1</td><td>General purpose Flag 1 available for user.</td></tr>
<tr><td>PSW.0</td><td>P</td><td>Parity flag, affected by hardware to indicate odd / even number of “one” bits in the Accumulator, i.e. even parity.</td></tr>
</table>

Table 9: PSW bit functions

Stack Pointer (SP): The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer: The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter: The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory. Note: The program counter is not mapped to the SFR area.

Port Registers: The I/O ports are controlled by Special Function Registers *USR70*, and *USR158*. The contents of the SFR can be observed on corresponding pins on the chip. Writing a ‘1’ to any of the ports (see Table 10) causes the corresponding pin to be at high level (3.3V), and writing a ‘0’ causes the corresponding pin to be held at low level (GND). The data direction registers *UDIR70,* and *UDIR158* define individual pins as input or output pins (see section User (USR) Ports for details).

Register	SFR Address	R/W	Description
USR70	0x80	R/W	Register for User port bit 7:0 read and write operations (pins USR0… USR7).
UDIR70	0xA2	R/W	Data direction register for User port bits 0:7. Setting a bit to 1 means that the corresponding pin is an output.
USR8	0x90	R/W	Register for User port bit 8 read and write operations (pin USR8).
UDIR8	0x91	R/W	Data direction register for port 1.

Table 10: Port Registers

All ports on the chip are bi-directional. Each of them consists of a Latch (SFR ‘USR70’ to ‘USR8’), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports if they are not used for alternate purposes.

Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the 12XX Software User’s Guide (SUG).

Peripheral Descriptions

Oscillator and Clock Generation

The 73S1215F has two oscillator circuits; one for the main CPU clock and another for the RTC. The main oscillator circuit is designed to operate with multiple crystals or external clock frequencies. An internal divider working in conjunction with a PLL and VCO needs to provide a 96MHz internal clock within the 73S1215F. 96 MHz is the required frequency for proper operation of specific peripheral blocks such as the USB, specific timers, ISO-7816 UART and interfaces, Step-up converter, and keypad. The clock generation and control circuits are shown in Figure 4.

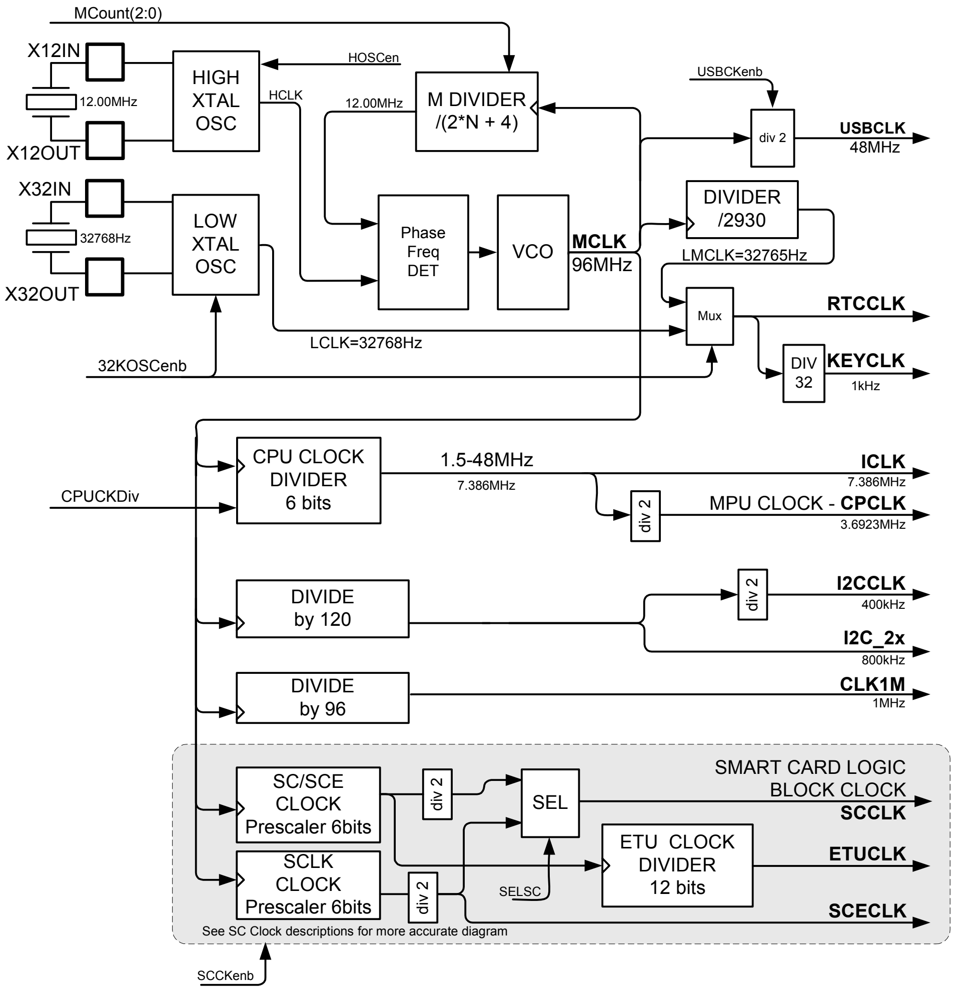


Figure 3: Clock Generation and Control Circuits

The master clock control register enables different sections of the clock circuitry and specifies the value of the VCO Mcount divider. The MCLK must be configured to operate at 96MHz to insure proper operation of some of the peripheral blocks according to the following formula:

$$MCLK = (Mcount * 2 + 4) * F_{XTAL} = 96MHz$$

Mcount is configured in the MCLKCtl register must be bound between a value of 1 to 10. The possible crystal or external clock frequencies are shown in Table 11.

F_{XTAL} (MHz)	Mcount (N)
16.00	1
12.00	2
9.60	3
8.00	4
6.86	5
6.00	6
5.33	7
4.80	8
4.36	9
4.00	10

Table 11: External clock frequencies and Mcount value combinations available for the main oscillator.

Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A

MSB							LSB
HSOEN	KBEN	SCEN	USBEN	32KEN	MCT.2	MCT.1	MCT.0

Table 12: The MCLKCtl Register

Bit	Symbol	Function
MCLKCtl.7	HSOEN	High-speed oscillator disable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system.
MCLKCtl.6	KBEN	1 => Disable the keypad logic clock.
MCLKCtl.5	SCEN	1 => Disable the smart card logic clock.
MCLKCtl.4	USBEN	1=> Disable the USB logic clock.
MCLKCtl.3	32KEN	1=> Disable the 32Khz oscillator. When the 32kHz oscillator is enabled, the RTC is clocked the 32kHz oscillator output. When disabled, the main oscillator provides the 32kHz clock for the RTC.
MCLKCtl.2	MCT.2	This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that: MCLK=(MCount*2 + 4)* F_{XTAL}. The default value is MCount= 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz.
MCLKCtl.1	MCT.1	
MCLKCtl.0	MCT.0	

Table 13: The MCLKCtl Register Bit Functions

The MPU clock that drives the CPU core defaults to 3.6923MHz after reset. The MPU clock is scalable by configuring the MPU Clock Control register.

MPU Clock Control Register (MPUCKCtl): 0xFFA1 ← 0x0C

MSB							LSB
-	-	MDIV.5	MDIV.4	MDIV.3	MDIV.2	MDIV.1	MDIV.0

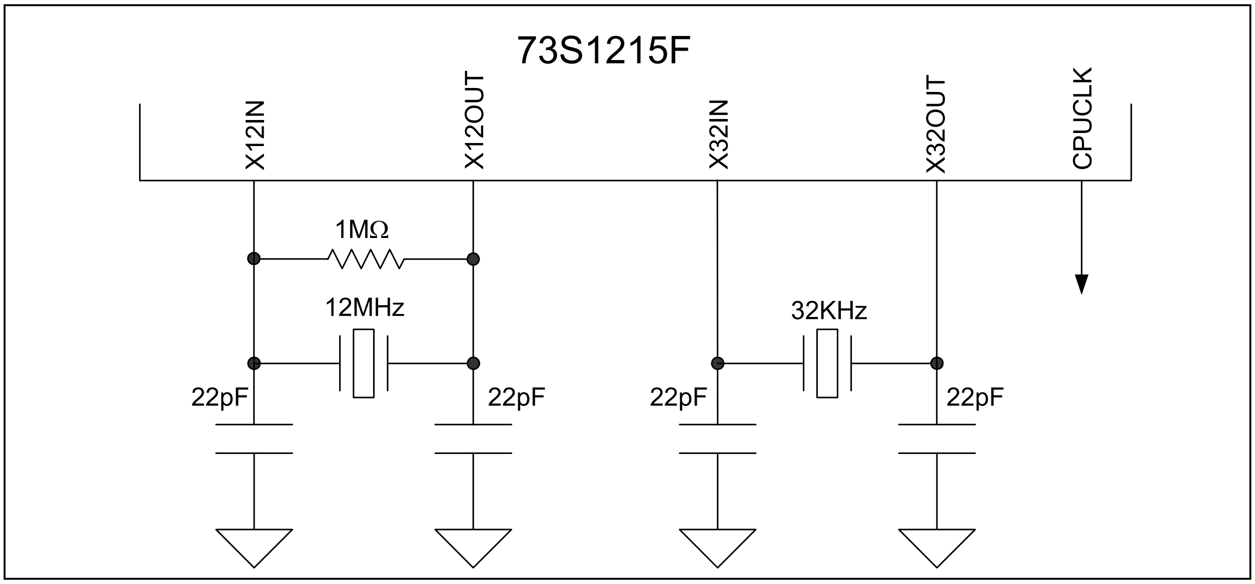
Table 14: The TCON Register

Bit	Symbol	Function
MPUCKCtl.7	-	
MPUCKCtl.6	-	
MPUCKCtl.5	MDIV.5	This value determines the ratio of the MPU master clock frequency to the VCO frequency (MCLK) such that MPUClk = MCLK/(2 * (MPUCKDiv(5:0) + 1)). Do not use values of 0 or 1 for MPUCKDiv(n). Default is 0Ch to set CPCLK = 3.6923MHz.
MPUCKCtl.4	MDIV.4	
MPUCKCtl.3	MDIV.3	
MPUCKCtl.2	MDIV.2	
MPUCKCtl.1	MDIV.1	
MPUCKCtl.0	MDIV.0	

Table 15: The MCLKCtl Register Bit Functions

The oscillator circuits are designed to connect directly to standard parallel resonant crystal in a Pierce oscillator configuration. Each side of the crystal should include a 22pF capacitor to ground for both oscillator circuits and a 1M resistor is required across the 12MHz crystal.

The CPU clock is available as an output on pin CPUCLK.

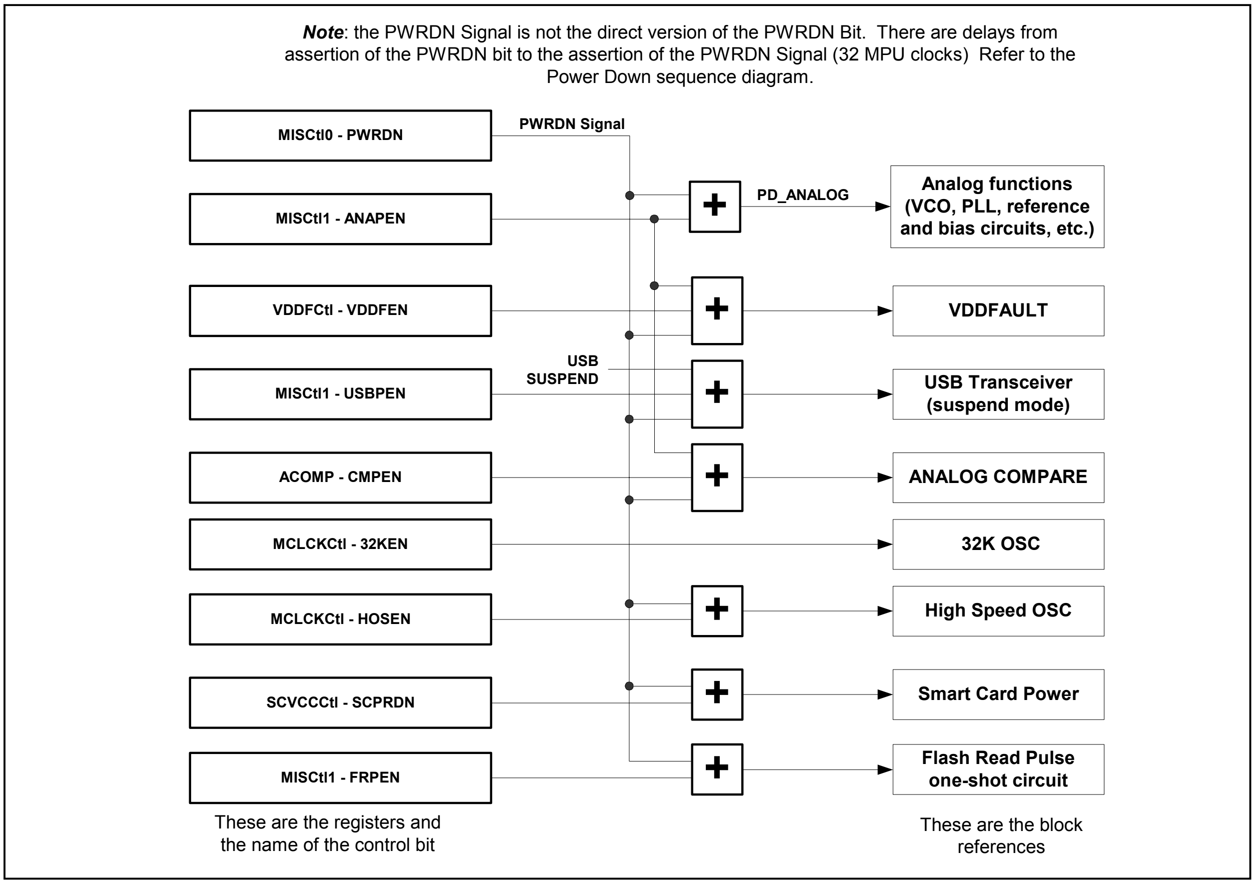


Note: The crystals should be placed as close as possible to the IC, and vias should be avoided.

Figure 4: Oscillator Circuit

Power Control Modes

The 73S1215F contains circuitry to disable portions of the device and place it into lower power standby modes. This is accomplished by either shutting off the power or disabling the clock going to the block. The miscellaneous control registers MISCtl0, MISCtl1 and the master clock control register (MCLKCtl) provide control over the power modes. There is also a device power down mode that will stop the core, clock subsystem and the peripherals connected to it. The PWRDN bit in MISCtl0 will setup the 73S1215F for power down and disable all clocks except the 32kHz oscillator. The power down mode should only be initiated by setting the PWRDN bit in the MISCtl0 register and not by manipulating individual control bits in various registers. Figure 4 shows how the PWRDN bit controls the various functions that comprise power down state.



Note: the PWRDN Signal is not the direct version of the PWRDN Bit. There are delays from assertion of the PWRDN bit to the assertion of the PWRDN Signal (32 MPU clocks) Refer to the Power Down sequence diagram.

These are the registers and the name of the control bit

These are the block references

Figure 5: Power-Down Control

When the PWRDN bit is set, the clock subsystem will provide a delay of 32 MPUCLK cycles to allow the program to set the STOP bit in the PCON register. This delay will enable the program to properly halt the core before the analog circuits shut down (high speed oscillator, VCO/PLL, voltage reference and bias circuitry, etc.). The PDMUX bit in SFR INT5Ctl should be set prior to setting the PWRDN bit in order to configure the wake up interrupt logic. The power down mode is awakened from interrupts connected to external interrupts 0, 4 and 5 (external USR[0:7], smart card, USB, RTC and Keypad). These interrupt sources are OR'ed together and routed through some delay logic into INT0 to provide this functionality. The interrupt will turn on the power to all sections that were shut off and start the clock subsystem. After the clock subsystem clocks start running, the MPUCLK begins to clock a 512 count delay counter. When the counter times out, the interrupt will then be active on INT0 and the program can resume. Figure 6 shows the detailed logic for waking up the 73S1215F from a power down state using these specific interrupt sources. Figure 7 shows the timing associated with the power down mode.

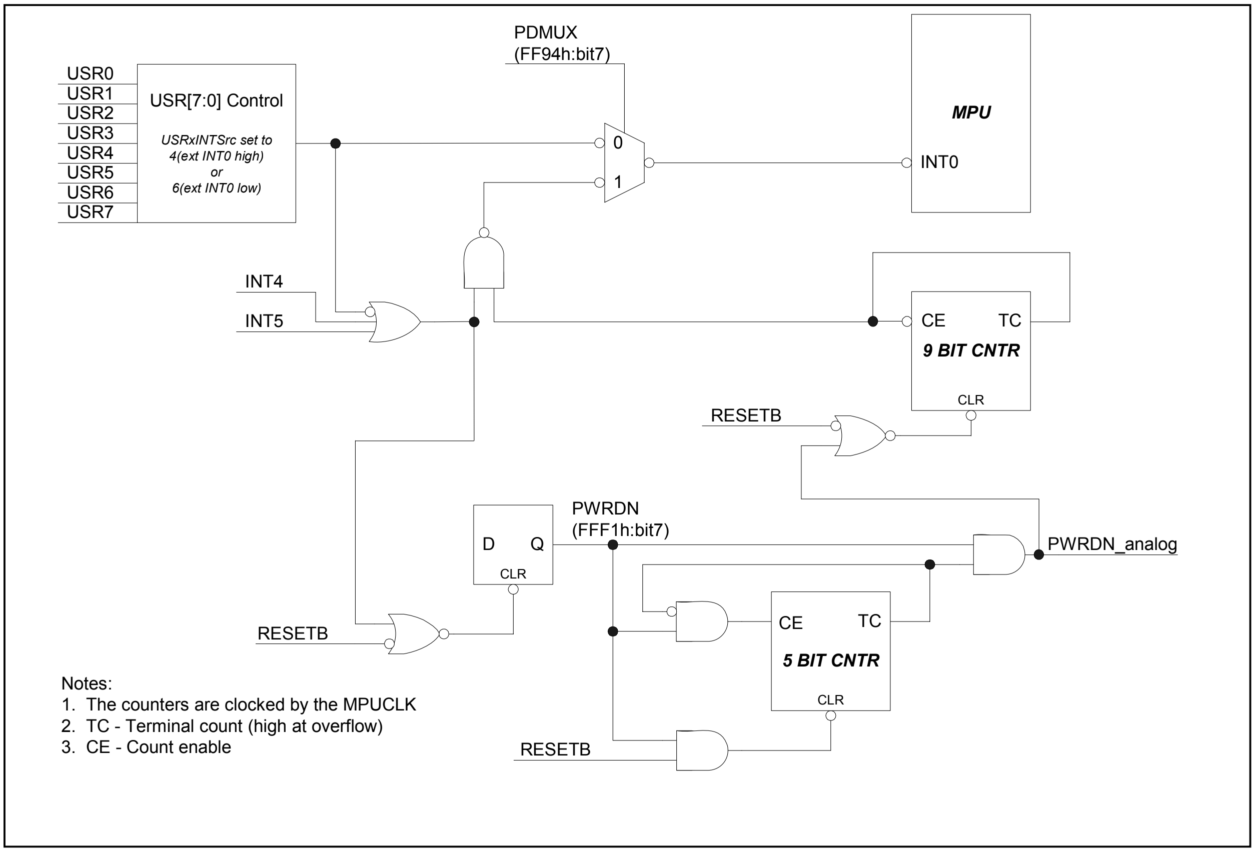
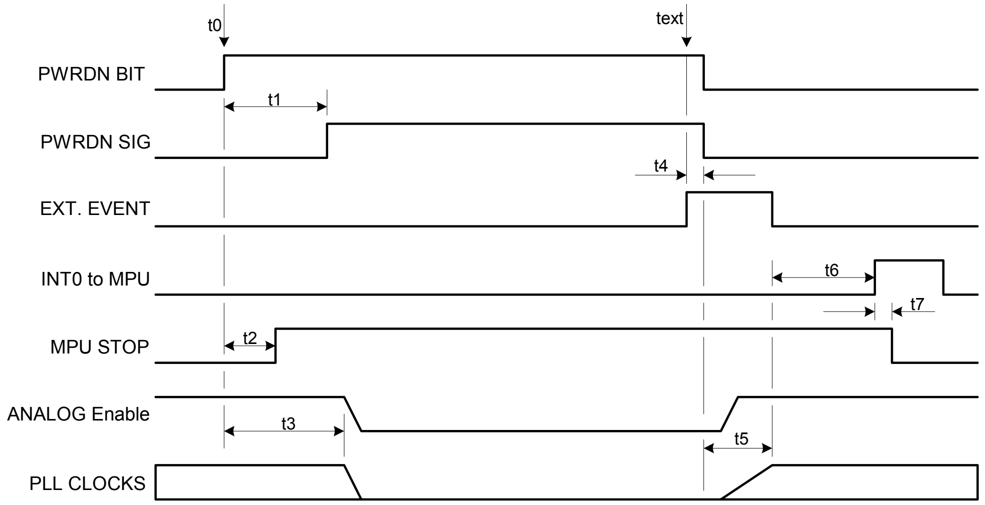


Figure 6: Detail of Power-Down Interrupt logic



t0: MPU sets PWRDN bit
t1: 32 MPU clock cycles after t0, the PWRDN SIG is asserted, turning all analog functions OFF
t2: MPU executes STOP instruction, must be done prior to t1
t3: Analog functions go to OFF condition. No Vref, PLL/VCO, Ibias, etc
text: An external event (RTC, Keypad, Card event, USB) occurs
t4: PWRDN bit and PWRDN signal are cleared by external event
t5: High-speed oscillator/PLL/VCO operating
t6: After 512 MPU clock cycles, INT0 to MPU is asserted
t7: INT0 causes MPU to exit STOP condition

Figure 7: Power-Down Sequencing

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

MSB LSB

PDMUX	-	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Table 16: The INT5Ctl Register

Bit	Symbol	Function
INT5Ctl.7	PDMUX	When set=1, enables interrupts from USB, RTC, Keypad (normally going to int5), Smart Card interrupts (normally going to int4), or USR(7:0) pins (int0) to cause interrupt on int0. The assertion of the interrupt to int0 is delayed by 512 MPU clocks to allow the analog circuits, including the clock system, to stabilize. This bit must be set prior to asserting the PWRDN bit in order to properly configure the interrupts that will wake up the circuit. This bit is reset=0 when this register is read.
INT5Ctl.6	-	
INT5Ctl.5	RTCIEN	RTC interrupt enable.
INT5Ctl.4	RTCINT	RTC interrupt flag.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Table 17: The INT5Ctl Register Bit Functions

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

MSB							LSB
PWRDN	-	-	-	-	-	SLPBK	SSEL

Table 18: The MISCtl0 Register

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit sets the circuit into a low-power condition. All analog (high speed oscillator and VCO/PLL) functions are disabled 32 MPU clock cycles after this bit is set=1. This allows time for the next instruction to set the STOP bit in the PCON register to stop the CPU core. The RTC will stay active if it is set to operate from the 32kHz oscillator. The MPU is not operative in this mode. When set, this bit overrides the individual control bits that otherwise control power consumption.
MISCtl0.6	-	
MISCtl0.5	-	
MISCtl0.4	-	
MISCtl0.3	-	
MISCtl0.2	-	
MISCtl0.1	SLPBK	UART loop back testing mode.
MISCtl0.0	SSEL	Serial port pins select.

Table 19: The MISCtl0 Bit Functions

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

MSB							LSB
-	-	FRPEN	FLSH66	-	ANAPEN	USBPEN	USBCON

Table 20: The MISCtl1 Register

Bit	Symbol	Function
MISCtl1.7	-	
MISCtl1.6	-	
MISCtl1.5	FRPEN	Flash Read Pulse enable (low). If FRPEN=1, the Flash Read signal is passed through with no change. When FRPEN=0 a one-shot circuit that shortens the Flash Read signal is enabled to save power. The Flash Read pulse will shorten to 40 or 66ns (approx based on the setting of the FLSH66 bit) in duration, regardless of the MPU clock rate. For MPU clock frequencies greater than 10MHz, this bit should be set high.
MISCtl1.4	FLSH66	When high, creates a 66ns Flash read pulse, otherwise creates a 40ns read pulse when FRPEN is set.
MISCtl1.3	-	
MISCtl1.2	ANAPEN*	0= Enable the analog functions that generate VREF and bias current functions. Setting high will turn off the VPD regulator and VCO/PLL functions.
MISCtl1.1	USBPEN	0= Enable the USB differential transceiver.
MISCtl1.0	USBCON	USB pull-up resistor connect enable.

*Note: The ANAPEN bit should never be set under normal circumstances. Power down control should only be initiated via use of the PWRDN bit in MISCtl0.

Table 21: The MISCtl0 Bit Functions.

Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A

MSB							LSB
HSOEN	KBEN	SCEN	USBEN	32KEN	MCT.2	MCT.1	MCT.0

Table 22: The MCLKCtl Register

Bit	Symbol	Function
MCLKCtl.7	HSOEN*	High-speed oscillator enable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. This bit is not changed when the PWRDN bit is set but the oscillator/VCO/PLL is disabled.
MCLKCtl.6	KBEN	1 => Disable the keypad logic clock. This bit is not changed in PWRDN mode but the function is disabled.
MCLKCtl.5	SCEN	1 => Disable the smart card logic clock. This bit is not changed in PWRDN mode but the function is disabled. Interrupt logic for card insertion/removal remains operable even with smart card clock disabled.
MCLKCtl.4	USBEN	1=> Disable the USB logic clock. This bit is not changed in PWRDN mode but the function is disabled.
MCLKCtl.3	32KEN	1=> Disable the 32Khz oscillator. This function is not affected by PWRDN mode.
MCLKCtl.2	MCT.2	This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that: MCLK=(MCount*2 + 4)*Fxtal. The default value is MCount= 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz.
MCLKCtl.1	MCT.1	
MCLKCtl.0	MCT.0	

*Note: The HSOEN bit should never be set under normal circumstances. Power down control should only be initiated via use of the PWRDN bit in MISCtl0.

Table 23: The MCLKCtl Register Bit Functions

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is setup via this register.

MSB							LSB
SMOD	-	-	-	GF1	GF0	STOP	IDLE

Table 24: The PCON Register

Bit	Symbol	Function
PCON.7	SMOD	If SM0D=1, the baud rate is doubled.
PCON.6	-	
PCON.5	-	.
PCON.4	-	
PCON.3	GF1	General purpose flag 1
PCON.2	GF0	General purpose flag 1
PCON.1	STOP	Sets CPU to Stop mode
PCON.0	IDLE	Sets CPU to Idle mode

Table 25: The MISCtl0 Bit Functions

Interrupts

The 80515 core provides 10 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (TCON, IRCON, and SCON). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs IEN0, IEN1, and IEN2. Some of the 10 sources are multiplexed in order to expand the number of interrupt sources. These will be described in more detail in the respective sections.

External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 73S1215F, for example the USB interface, USR I/O, RTC, smart card interface, analog comparators, etc. The external interrupt configuration is shown in Figure.

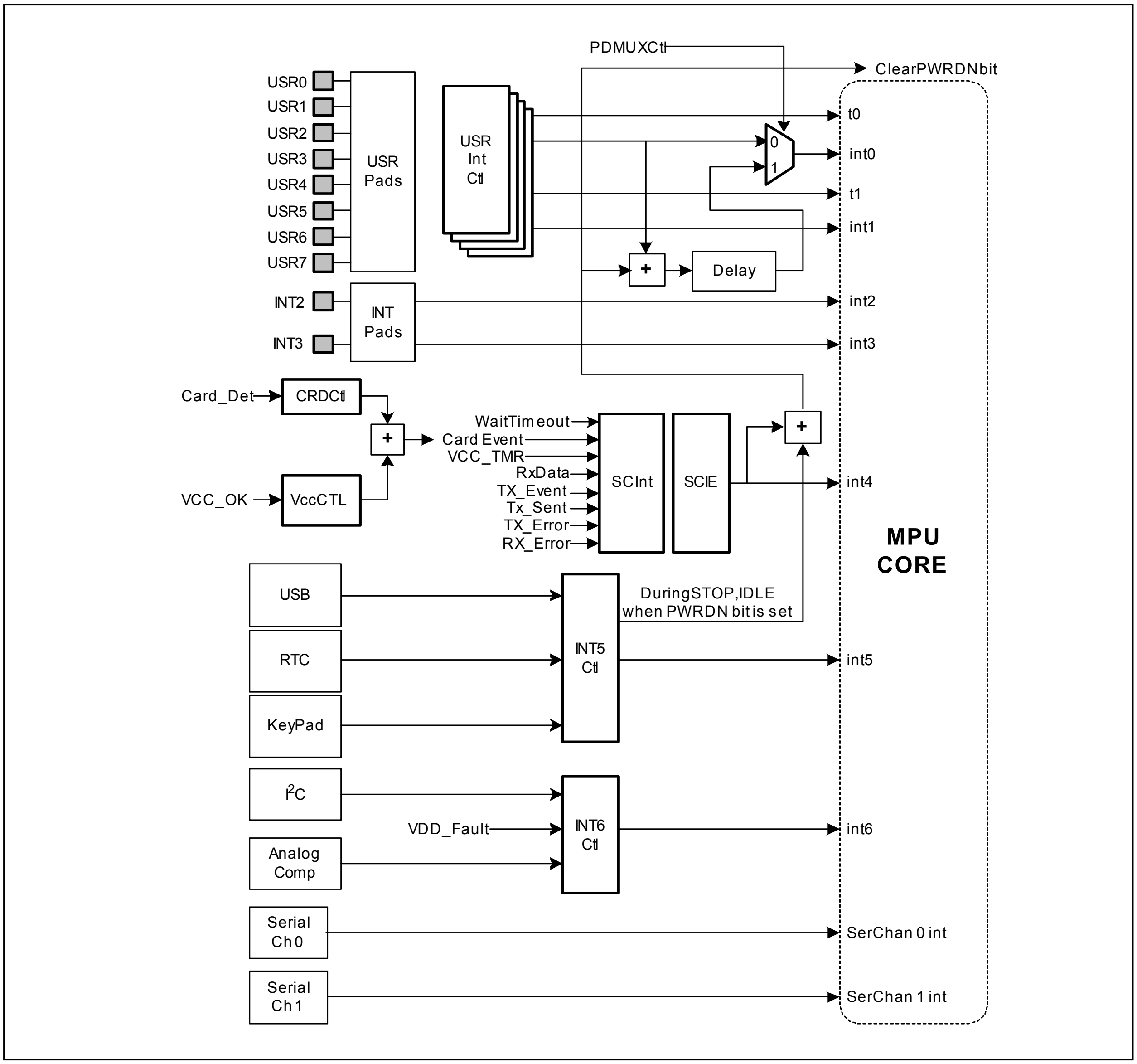


Figure 8: External Interrupt Configuration

Interrupt Overview: When an interrupt occurs, the MPU will vector to the predetermined address as shown in Table 45. Once the interrupt service has begun, it can only be interrupted by a higher priority interrupt. The interrupt service is terminated by a return from instruction, "RETI". When an RETI is performed, the processor will return to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt will be acknowledged by hardware forcing an LCALL to the appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of the MPU when the interrupt occurs. If the MPU is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on the current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles to perform the LCALL.

Special Function Registers for Interrupts:

Interrupt Enable 0 register (IEN0): 0xA8 ← 0x00

MSB							LSB
EAL	WDT	-	ES0	ET1	EX1	ET0	EX0

Table 26: The IEN0 Register

Bit	Symbol	Function
IEN0.7	EAL	EAL = 0 – disable all interrupts.
IEN0.6	WDT	Not used for interrupt control.
IEN0.5	-	
IEN0.4	ES0	ES0 = 0 – disable serial channel 0 interrupt.
IEN0.3	ET1	ET1 = 0 – disable timer 1 overflow interrupt.
IEN0.2	EX1	EX1 = 0 – disable external interrupt 1.
IEN0.1	ET0	ET0 = 0 – disable timer 0 overflow interrupt.
IEN0.0	EX0	EX0 = 0 – disable external interrupt 0.

Table 27: The IEN0 Bit Functions

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

MSB							LSB
-	SWDT	EX6	EX5	EX4	EX3	EX2	-

Table 28: The IEN1 Register

Bit	Symbol	Function
IEN1.7	-	
IEN1.6	SWDT	Not used for interrupt control.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	-	

Table 29: The IEN1 Bit Functions

Interrupt Enable 2 register (IEN2): 0x9A ← 0x00

MSB							LSB
-	-	-	-	-	-	-	ES1

Table 30: The IEN2 Register

Bit	Symbol	Function
IEN2.0	ES1	ES1 = 0 – disable serial channel interrupt.

Table 31: The IEN2 Bit Functions

Timer/Counter Control register (TCON): 0x88 ← 0x00

MSB							LSB
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 32: The TCON Register

Bit	Symbol	Function
TCON.7	TF1	Timer 1 overflow flag.
TCON.6	TR1	Not used for interrupt control.
TCON.5	TF0	Timer 0 overflow flag.
TCON.4	TR0	Not used for interrupt control.
TCON.3	IE1	Interrupt 1 edge flag is set by hardware when the falling edge on external interrupt int1 is observed. Cleared when an interrupt is processed.
TCON.2	IT1	Interrupt 1 type control bit. Selects either the falling edge or low level on input pin to cause an interrupt.
TCON.1	IE0	Interrupt 0 edge flag is set by hardware when the falling edge on external interrupt int0 is observed. Cleared when an interrupt is processed.
TCON.0	IT0	Interrupt 0 type control bit. Selects either the falling edge or low level on input pin to cause interrupt.

Table 33: The TCON Bit Functions

Timer/Interrupt 2 Control Register (T2CON): 0xC8 ← 0x00

MSB							LSB
-	I3FR	I2FR	-	-	-	-	-

Table 34: The T2CON Register

Bit	Symbol	Function
T2CON.7	-	

T2CON.6	I3FR	External interrupt 3 failing/rising edge flag.
		I3FR = 0 external interrupt 3 negative transition active.
		I3FR = 1 external interrupt 3 positive transition active.

T2CON.5	I2FR	External interrupt 3 failing/rising edge flag.
		I2FR = 0 external interrupt 3 negative transition active.
		I2FR = 1 external interrupt 3 positive transition active.

T2CON.4	-	
T2CON.3	-	
T2CON.2	-	
T2CON.1	-	
T2CON.0	-	

Table 35: The T2CON Register Bit Functions

Interrupt Request register (IRCON): 0xC0 ← 0x00

MSB							LSB
-	-	EX6	IEX5	IEX4	IEX3	IEX2	-

Table 36: The IRCON Register

Bit	Symbol	Function
IRCON.7	-	
IRCON.6	-	
IRCON.5	IEX6	External interrupt 6 flag.
IRCON.4	IEX5	External interrupt 5 flag.
IRCON.3	IEX4	External interrupt 4 flag.
IRCON.2	IEX3	External interrupt 3 flag.
IRCON.1	IEX2	External interrupt 2 flag.
IRCON.0	-	

Table 37: The IRCON Bit Functions

External Interrupts

The external interrupts (external to the CPU core) are connected as shown in Table 38. Interrupts with multiple sources are OR'ed together and individual interrupt source control is provided in XRAM SFRs to mask the individual interrupt sources and provide the corresponding interrupt flags. Multifunction USR [7:0] pins control Interrupts 0 and 1. Dedicated external interrupt pins INT2 and INT3 control interrupts 2 and 3. The polarity of interrupts 2 and 3 is programmable in the MPU. Interrupts 4, 5 and 6 have multiple peripheral sources and are multiplexed to one of these three interrupts. The peripheral functions will be described in subsequent sections. Generic 80515 MPU literature states that interrupts 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 4, 5 and 6 are converted to rising edge level by the hardware.

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler.

External Interrupt	Connection	Polarity	Flag Reset
0	USR I/O High Priority	see *USRxINTSrc*	Automatic
1	USR I/O Low Priority	see *USRxINTSrc*	Automatic
2	External Interrupt Pin INT2	Edge selectable	Automatic
3	External Interrupt Pin INT3	Edge selectable	Automatic
4	Smart Card Interrupts	N/A	Automatic
5	USB, RTC and Keypad	N/A	Automatic
6	I^2C, V_{DD}_Fault, Analog Comp	N/A	Automatic

Note 1: Interrupts 4, 5 and 6 have multiple interrupt sources and the flag bits are cleared upon reading of the corresponding register. To prevent any interrupts from being ignored, the register containing multiple interrupt flags should be stored temporary to allow each interrupt flag to be tested separately to see which interrupt(s) is/are pending.

Table 38: External MPU Interrupts

Enable Bit	Description
EX0	Enable external interrupt 0
EX1	Enable external interrupt 1
EX2	Enable external interrupt 2
EX3	Enable external interrupt 3
EX4	Enable external interrupt 4
EX5	Enable external interrupt 5
EX6	Enable external interrupt 6

Flag Bit	Description
IE0	External interrupt 0 flag
IE1	External interrupt 1 flag
IEX2	External interrupt 2 flag
IEX3	External interrupt 3 flag
IEX4	External interrupt 4 flag
IEX5	External interrupt 5 flag
IEX6	External interrupt 6 flag

Table 39: Control Bits for External Interrupts

Power Down Interrupt Logic

The 73S1215F contains special interrupt logic to allow INT0 to wake up the CPU from a power down (CPU STOP) state. See the power control modes section for details

Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 40:

Group			
0	External interrupt 0	Serial channel 1 interrupt	
1	Timer 0 interrupt	-	External interrupt 2
2	External interrupt 1	-	External interrupt 3
3	Timer 1 interrupt	-	External interrupt 4
4	Serial channel 0 interrupt	-	External interrupt 5
5	-	-	External interrupt 6

Table 40: Priority Level Groups

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level are received simultaneously, an internal polling sequence as per Table 44 determines which request is serviced first.

IEN enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler.

Interrupt Priority 0 Register (IP0): 0xA9 ← 0x00

MSB LSB

--	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Note: WDTS is not used for interrupt controls.

Table 41: The IP0 Register:

Interrupt Priority 1 Register (IP1): 0xB9 ← 0x00

MSB LSB

-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0

Table 42: The IP1 Register:

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 43: Priority Levels

External interrupt 0	Polling sequence
Serial channel 1 interrupt	
Timer 0 interrupt	
External interrupt 2	
External interrupt 1	
External interrupt 3	
Timer 1 interrupt	
Serial channel 0 interrupt	
External interrupt 4	
External interrupt 5	
External interrupt 6	

Table 44: Interrupt Polling Sequence

Interrupt Sources and Vectors

Table 45 shows the interrupts with their associated flags and vector addresses.

Interrupt Request Flag	Description	Interrupt Vector Address
N/A	Chip Reset	0x0000
IE0	External interrupt 0	0x0003
TF0	Timer 0 interrupt	0x000B
IE1	External interrupt 1	0x0013
TF1	Timer 1 interrupt	0x001B
RI0/TI0	Serial channel 0 interrupt	0x0023
RI1/TI1	Serial channel 1 interrupt	0x0083
IEX2	External interrupt 2	0x004B
IEX3	External interrupt 3	0x0053
IEX4	External interrupt 4	0x005B
IEX5	External interrupt 5	0x0063
IEX6	External interrupt 6	0x006B

Table 45: Interrupt Vectors

UART

The 80515 core of the 73S1215F includes two separate UARTs that can be programmed to communicate with a host. The 73S1215F can only connect one UART at a time since there is only one set of TX and Rx pins. The MISCtl0 register is used to select which UART is connected to the TX and RX pins. Each UART has a different set of operating modes that the user can select according to their needs. The UART is a dedicated 2-wire serial interface, which can communicate with an external host processor at up to 115,200 bits/s. The TX and RX pins operate at the V_{DD} supply voltage levels and should never exceed 3.6V. The operation of each pin is as follows:

RX: Serial input data is applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first. The voltage applied at RX must not exceed 3.6V.

TX: This pin is used to output the serial data. The bytes are output LSB first.

The 73S1215F has several UART-related read/write registers. All UART transfers are programmable for parity enable, parity select, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 115200 bps. Table 42 shows the selectable UART operation modes and table 43 shows how the baud rates are calculated.

	UART 0	**UART 1**
Mode 0	N/A	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator)
Mode 1	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1)	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator)
Mode 2	Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of f_{CKMPU}	N/A
Mode 3	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1)	N/A

Note: Parity of serial data is available through the P flag of the accumulator. Seven-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. Seven-bit serial modes without parity can be simulated by setting bit 7 to a constant 1. 8-bit serial modes with parity can be simulated by setting and reading the 9th bit, using the control bits S0CON3 and S1CON3 in the S0COn and S1CON SFRs.

Table 46: UART Modes

	Using Timer 1	**Using Internal Baud Rate Generator**
Serial Interface 0	$2^{smod} * f_{CKMPU}/ (384 * (256\text{-}TH1))$	$2^{smod} * f_{CKMPU}/(64 * (2^{10}\text{-}S0REL))$
Serial Interface 1	N/A	$f_{CKMPU}/(32 * (2^{10}\text{-}S1REL))$

Note: S0REL (9:0) and S1REL (9:0) are 10-bit values derived by combining bits from the respective timer reload registers SxRELH (bits 1:0) and SxRELL (bits 7:0). TH1 is the high byte of timer 1. The SMOD bit is located in the PCON SFR.

Table 47: Baud Rate Generation

Power Control Register 0 (PCON): 0x87 ← 0x00

The SMOD bit used for the baud rate generator is setup via this register.

MSB							LSB
SMOD	-	-	-	GF1	GF0	STOP	IDLE

Table 48: The PCON Register

Bit	Symbol	Function
PCON.7	SMOD	If SM0D=1, the baud rate is doubled.
PCON.6	-	
PCON.5	-	.
PCON.4	-	
PCON.3	GF1	General purpose flag 1
PCON.2	GF0	General purpose flag 1
PCON.1	STOP	Sets CPU to Stop mode
PCON.0	IDLE	Sets CPU to Idle mode

Table 49: The MISCtl0 Bit Functions

Baud Rate Control Register 0 (BRCON): 0xD8 ← 0x00

The BSEL bit used to enable the baud rate generator is setup via this register.

MSB							LSB
BSEL	-	-	-	-	-	-	-

Table 50: The BRCON Register

Bit	Symbol	Function
BRCON.7	BSEL	If BSEL =1, the baud rate is derived using timer 1. If BSEL=1 the baud rate generator circuit is used.
BRCON.6	-	
BRCON.5	-	.
BRCON.4	-	
BRCON.3	-	
BRCON.2	-	
BRCON.1	-	
BRCON.0	-	

Table 51: The BRCON Bit Functions

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Transmit and receive (TX and RX) pin selection and loop back test configuration are setup via this register.

MSB LSB

PWRDN	-	-	-	-	-	SLPBK	SSEL

Table 52: The MISCtl0 Register

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit places the 1215F into a power down state.
MISCtl0.6	-	
MISCtl0.5	-	.
MISCtl0.4	-	
MISCtl0.3	-	
MISCtl0.2	-	
MISCtl0.1	SLPBK	1= UART loop back testing mode. The pins TXD and RXD are to be connected together externally (with SLPBK =1) and therefore: SLPBK SSEL Mode 0 0 normal using Serial_0 0 1 normal using Serial_1 1 0 Serial_0 TX feeds Serial_1 RX 1 1 Serial_1 TX feeds Serial_0 RX
MISCtl0.0	SSEL	Selects either Serial_1 if set =1 or Serial_0 if set = 0 to be connected to RXD and TXD pins.

Table 53: The MISCtl0 Bit Functions

Serial Interface 0

The Serial Interface 0 can operate in 4 modes:

- **Mode 0**

Pin RX serves as input and output. TX outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and REN0 = 1. In other modes, a start bit when REN0 = 1 starts receiving serial data

- **Mode 1**

Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and stop bit sets the flag RB80 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate.

- **Mode 2**

This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 or 1/64 of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB80 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB80 in Special Function Register S0CON.

- **Mode 3**

The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate.

The S0BUF register is used to read/write data to/from the serial 0 interface.

Serial Interface 0 Control Register (S0CON): 0x9B ← 0x00

Transmit and receive data are transferred via this register.

MSB							LSB
SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0

Table 54: The S0CON Register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>S0CON.7</td><td>SM0</td><td rowspan="2">These two bits set the UART0 mode:
<table>
<tr><th>Mode</th><th>Description</th><th>SM0</th><th>SM1</th></tr>
<tr><td>0</td><td>N/A</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>8-bit UART</td><td>0</td><td>1</td></tr>
<tr><td>2</td><td>9-bit UART</td><td>1</td><td>0</td></tr>
<tr><td>3</td><td>9-bit UART</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>S0CON.6</td><td>SM1</td></tr>
<tr><td>S0CON.5</td><td>SM20</td><td>Enables the inter-processor communication feature.</td></tr>
<tr><td>S0CON.4</td><td>REN0</td><td>If set, enables serial reception. Cleared by software to disable reception.</td></tr>
<tr><td>S0CON.3</td><td>TB80</td><td>The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)</td></tr>
<tr><td>S0CON.2</td><td>RB80</td><td>In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM20 is 0, RB80 is the stop bit. In Mode 0 this bit is not used. Must be cleared by software</td></tr>
<tr><td>S0CON.1</td><td>TI0</td><td>Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.</td></tr>
<tr><td>S0CON.0</td><td>RI0</td><td>Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software</td></tr>
</table>

Table 55: The S0CON Bit Functions

Serial Interface 1

The Serial Interface 1 can operate in 2 modes:

- **Mode A**

This mode is similar to Mode 2 and 3 of Serial interface 0, 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB81 in S1CON is outputted as the 9th bit, and at receive, the 9th bit affects RB81 in Special Function Register S1CON. The only difference between Mode 3 and A is that in Mode A only internal baud rate generator can be use to specify baud rate.

- **Mode B**

This mode is similar to Mode 1 of Serial interface 0. Pin RX serves as input, and TX serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S1BUF, and stop bit sets the flag RB81 in the Special Function Register S1CON. In mode 1 internal baud rate generator is use to specify the baud rate.

The S1BUF register is used to read/write data to/from the serial 1 interface.

Serial Interface Control Register (S1CON): 0x9B ← 0x00

The function of the serial port depends on the setting of the Serial Port Control Register S1CON.

MSB							LSB
SM	-	SM21	REN1	TB81	RB81	TI1	RI1

Table 56: The S1CON register

<table>
<tr><th>Bit</th><th>Symbol</th><th>Function</th></tr>
<tr><td>S1CON.7</td><td>SM</td><td>Sets the UART operation mode.
<table>
<tr><th>SM</th><th>Mode</th><th>Description</th><th>Baud Rate</th></tr>
<tr><td>0</td><td>A</td><td>9-bit UART</td><td>variable</td></tr>
<tr><td>1</td><td>B</td><td>8-bit UART</td><td>variable</td></tr>
</table></td></tr>
<tr><td>S1CON.6</td><td>-</td><td></td></tr>
<tr><td>S1CON.5</td><td>SM21</td><td>Enables the inter-processor communication feature.</td></tr>
<tr><td>S1CON.4</td><td>REN1</td><td>If set, enables serial reception. Cleared by software to disable reception.</td></tr>
<tr><td>S1CON.3</td><td>TB81</td><td>The 9th transmitted data bit in Mode A. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.)</td></tr>
<tr><td>S1CON.2</td><td>RB81</td><td>In Mode B, if sm21 is 0, rb81 is the stop bit. Must be cleared by software</td></tr>
<tr><td>S1CON.1</td><td>TI1</td><td>Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.</td></tr>
<tr><td>S1CON.0</td><td>RI1</td><td>Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software</td></tr>
</table>

Table 57: The S1CON Bit Functions

Multiprocessor operation mode: The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface 0 or in Mode A of Serial Interface 1 can be used for multiprocessor communication. In this case, the slave processors have bit SM20 in S0CON or SM21 in S1CON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear SM20 or SM21 and receive the rest of the message, while other slaves will leave the SM20 or SM21 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from USR[0:7] pins, see the USR Ports section). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

The Timer 0 load registers are designated as TL0 and TH0 and the Timer 1 load registers are designated as TL1 and TH1.

Timer/Counter Mode Control register (TMOD): 0x89 ← 0x00

MSB							LSB
GATE	C/T	M1	M0	GATE	C/T	M1	M0
Timer 1				Timer 0			

Table 58: The TMOD Register

Bits TR1 and TR0 start their associated timers when set.

Bit	Symbol	Function
TMOD.7 TMOD.3	Gate	If set, enables external gate control (USR pin(s) connected to T0 or T1 for Counter 0 or 1, respectively). When T0 or T1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on T0 or T1 input pin. If not set, the TRx bit controls the corresponding timer.
TMOD.6 TMOD.2	C/T	Selects Timer or Counter operation. When set to 1, the counter operation is performed based on the falling edge of T0 or T1. When cleared to 0, the corresponding register will function as a timer.
TMOD.5 TMOD.1	M1	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description.
TMOD.4 TMOD.0	M0	Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description.

Table 59: TMOD Register Bit Description

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter/Timer.
0	1	Mode 1	16-bit Counter/Timer.
1	0	Mode2	8-bit auto-reload Counter/Timer
1	1	Mode3	If Timer 1 M1 and M0 bits are set to '1', Timer 1 stops. If Timer 0 M1 and M0 bits are set to '1', Timer 0 acts as two independent 8-bit Timer/Counters.

Table 60: Timers/Counters Mode Description

Mode 0

Putting either timer/counter into mode 0 configures it as an 8-bit timer/counter with a divide-by-32 prescaler. In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1's to all 0's, it sets the timer overflow flag TF0. The overflow flag TF0 then can be used to request an interrupt. The counted input is enabled to the timer when TRx = 1 and either GATE = 0 or TX = 1 (setting GATE = 1 allows the timer to be controlled by external input TX, to facilitate pulse width measurements). TRx are control bits in the special function register TCON; GATE is in TMOD. The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TRx) does not clear the registers. Mode 0 operation is the same for timer 0 as for timer 1.

Mode 1

Mode 1 is the same as mode 0, except that the timer register is run with all 16 bits.

Mode 2

Mode 2 configures the timer register as an 8-bit counter (TLx) with automatic reload. The overflow from TLx not only sets TFx, but also reloads TLx with the contents of THx, which is preset by software. The reload leaves THx unchanged.

Mode 3

Mode 3 has different effects on timer 0 and timer 1. Timer 1 in mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in mode 3 establishes TL0 and TH0 as two separate counters. TL0 uses the timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from timer 1. Thus, TH0 now controls the "timer 1" interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When timer 0 is in mode 3, timer 1 can be turned on and off by switching it out of and into its own mode 3, or can still be used by the serial channel as a baud rate generator, or in fact, in any application not requiring an interrupt from timer 1 itself.

Timer/Counter Control Register (TCON): 0x88 ← 0x00

MSB LSB

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 61: The TCON Register

Bit	Symbol	Function
TCON.7	TF1	The Timer 1 overflow flag is set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON.6	TR1	Timer 1 Run control bit. If cleared, Timer 1 stops.
TCON.5	TF0	Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed.
TCON.4	TR0	Timer 0 Run control bit. If cleared, Timer 0 stops.
TCON.3	IE1	External Interrupt 1 edge flag.
TCON.2	IT1	External interrupt 1 type control bit.
TCON.1	IE0	External Interrupt 0 edge flag.
TCON.0	IT0	External Interrupt 0 type control bit.

Table 62: The TCON Register Bit Functions

WD Timer (Software Watchdog Timer)

The software watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After a reset, the watchdog timer is disabled and all registers are set to zero. The watchdog consists of a 16-bit counter (WDT), a reload register (WDTREL), prescalers (by 2 and by 16), and control logic. Once the watchdog starts, it cannot be stopped unless the internal reset signal becomes active.

Note: It is recommended to use the hardware watchdog timer instead of the software watchdog timer (refer to the RTC description).

WD Timer Start Procedure: The WDT is started by setting the SWDT flag. When the WDT register enters the state 0x7CFF, an asynchronous WDTS signal will become active. The signal WDTS sets bit 6 in the IP0 register and requests a reset state. WDTS is cleared either by the reset signal or by changing the state of the WDT timer.

Refreshing the WD Timer: The watchdog timer must be refreshed regularly to prevent the reset request signal from becoming active. This requirement imposes an obligation on the programmer to issue two instructions. The first instruction sets WDT and the second instruction sets SWDT. The maximum delay allowed between setting WDT and SWDT is 12 clock cycles. If this period has expired and SWDT has not been set, WDT is automatically reset, otherwise the watchdog timer is reloaded with the content of the WDTREL register and WDT is automatically reset.

Interrupt Enable 0 Register (IEN0): 0xA8 ← 0x00

MSB							LSB
EAL	WDT	ET2	ES0	ET1	EX1	ET0	EX0

Table 63: The IEN0 Register

Bit	Symbol	Function
IEN0.7	EAL	EAL = 0 – disable all interrupts.
IEN0.6	WDT	Watchdog timer refresh flag. Set to initiate a refresh of the watchdog timer. Must be set directly before SWDT is set to prevent an unintentional refresh of the watchdog timer. WDT is reset by hardware 12 clock cycles after it has been set.
IEN0.5	-	
IEN0.4	ES0	ES0 = 0 – disable serial channel 0 interrupt.
IEN0.3	ET1	ET1 = 0 – disable timer 1 overflow interrupt.
IEN0.2	EX1	EX1 = 0 – disable external interrupt 1.
IEN0.1	ET0	ET0 = 0 – disable timer 0 overflow interrupt.
IEN0.0	EX0	EX0 = 0 – disable external interrupt 0.

Table 64: The IEN0 Bit Functions

Interrupt Enable 1 Register (IEN1): 0xB8 ← 0x00

MSB LSB

-	SWDT	EX6	EX5	EX4	EX3	EX2	

Table 65: The IEN1 Register

Bit	Symbol	Function
IEN1.7	-	
IEN1.6	SWDT	Watchdog timer start/refresh flag. Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset by the hardware 12 clock cycles after it has been set.
IEN1.5	EX6	EX6 = 0 – disable external interrupt 6.
IEN1.4	EX5	EX5 = 0 – disable external interrupt 5.
IEN1.3	EX4	EX4 = 0 – disable external interrupt 4.
IEN1.2	EX3	EX3 = 0 – disable external interrupt 3.
IEN1.1	EX2	EX2 = 0 – disable external interrupt 2.
IEN1.0	-	

Table 66: The IEN1 Bit Functions

Interrupt Priority 0 Register (IP0): 0xA9 ← 0x00

MSB LSB

--	WDTS	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0

Table 67: The IP0 Register

Bit	Symbol	Function
IP0.6	WDTS	Watchdog timer status flag. Set when the watchdog timer has expired. The internal reset will be generated, but this bit will not be cleared by the reset. This allows the user program to determine if the watchdog timer caused the reset to occur and respond accordingly. Can be read and cleared by software.

Table 68: The IP0 bit Functions

Note: The remaining bits in the IP0 register are not used for watchdog control.

Watchdog Timer Reload Register (WDTREL): 0x86 ← 0x00

MSB							LSB
WDPSEL	WDREL6	WDREL5	WDREL4	WDREL3	WDREL2	WDREL1	WDREL0

Table 69: The WDTREL Register

Bit	Symbol	Function
WDTREL.7	WDPSEL	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler
WDTREL.6 to WDTREL.0	WDREL6-0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT.

Table 70: The WDTREL Bit Functions

User (USR) Ports

The 73S1215F includes 9 pins of general purpose digital I/O (GPIO). On reset or power-up, all USR pins are inputs until they are configured for the desired direction. The pins are configured and controlled by the *USR* and *UDIR* SFRs. Each pin declared as USR can be configured independently as an input or output with the bits of the *UDIRn* registers. Table 71 lists the direction registers and configurability associated with each group of USR pins. USR pins 0 to 7 are multiple use pins that can be used for general purpose I/O, external interrupts and timer control. Table 72 shows the configuration for a *USR* pin through its associated bit in its *UDIR* register. Values read from and written into the GPIO ports use the data registers *USR70* and *USR8*.

USR Pin Group	Type	Direction Register Name	Direction Register (SFR) Location	Data Register Name	Data Register (SFR) Location
USR_0…USR_7	Multi-use	*UDIR70*	0x91 [7:0]	*USR70*	0x90 [7:0]
USR_8	GPIO only	*UDIR8*	0xA1 [0]	*USR8*	0xA0 [0]

Table 71: Direction Registers and Internal Resources for DIO Pin Groups

	UDIR bit	
	0	**1**
USR Pin Function	input	output

Table 72: *UDIR* Control Bit

Four XRAM SFR registers (USRIntTCtl0, USRIntTCtl1, USRIntTCtl2, and USRIntTCtl3) control the use of the USR [7:0] pins. Each of the USR [7:0] pins can be configured as GPIO or individually be assigned an internal resource such as an interrupt or a timer/counter control. Each of the four registers contain two 3-bit configuration words named UxIS (where x corresponds to the USR pin). The control resources selectable for the USR pins are listed in . If more than one input is connected to the same resource, the resources are combined using a logical OR.

UxIS Value	Resource Selected for USRx Pin
0	None
1	None
2	T0 (counter0 gate/clock)
3	T1 (counter1 gate/clock)
4	Interrupt 0 rising edge/high level on USRx
5	Interrupt 1 rising edge/high level on USRx
6	Interrupt 0 falling edge/low level on USRx
7	Interrupt 1 falling edge/low level on USRx

Note: x denotes the corresponding USR pin. Interrupt edge or level control is assigned in the IT0 and IT1 bits in the TCON register.

Table 73: Selectable Controls using the UxIS Bits

External Interrupt Control Register (USRIntTCtl0)

MSB							LSB
--	U1IS.6	U1IS.5	U1IS.4	-	U0IS.2	U0IS.1	U0IS.0

Table 74: The USRIntTCtl0 Register:

External Interrupt Control Register (USRIntTCtl1)

MSB							LSB
--	U3IS.6	U3IS.5	U3IS.4	-	U2IS.2	U2IS.1	U2IS.0

Table 75: The USRIntTCtl0 Register:

External Interrupt Control Register (USRIntTCtl2)

MSB							LSB
--	U5IS.6	U5IS.5	U5IS.4	-	U4IS.2	U4IS.1	U4IS.0

Table 76: The USRIntTCtl0 Register:

External Interrupt Control Register (USRIntTCtl3)

MSB LSB

--	U7IS.6	U7IS.5	U7IS.4	-	U6IS.2	U6IS.1	U6IS.0

Table 77: The USRIntTCtl0 Register:

Real-Time Clock with Hardware Watchdog (RTC)

Figure 5 shows the block diagram of the Real Time Clock. The RTC block uses the 32768Hz oscillator signal and divider logic to produce 0.5-second time marks. The time marks are used to create interrupts at intervals from 0.5 seconds to 8 seconds as selected by RTC Interval (RTCINV(2:0)). The 32768Hz oscillator can be disabled but is intended to operate at all times and in all power consumption modes.

If a 32kHz crystal is not provided, the 32 kHz oscillator should be disabled and the RTC will operate from MCLK (96MHz) divided by 2930 (refer to the oscillator and clock generation section). The clock generated by the high speed oscillator will not yield exactly 32768 Hz, but a frequency of approximately 32764.505119 Hz. This yields a negative 106.6 PPM (1 / 9375) error with respect to 32768Hz. The RTC circuit provides hardware to compensate for this error by providing an offset circuit that will adjust the RTC counter.

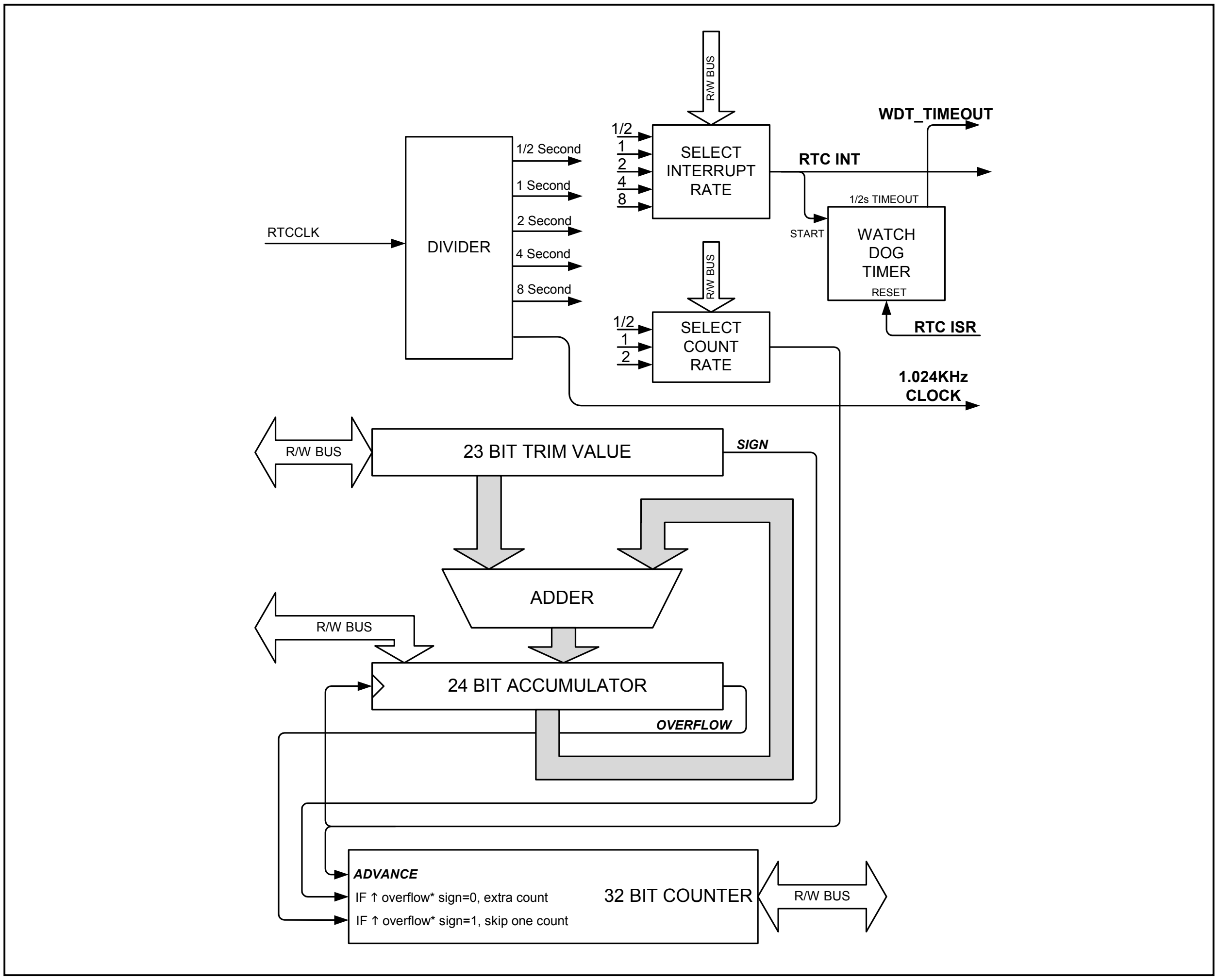


Figure 9: Real Time Clock Block Diagram.

A 32-bit RTC counter is clocked by a selectable clock (1/2, 1, 2 second) to measure time. A trimming function is provided such that a trim value is accumulated in a 24-bit accumulator at the same rate as the RTC counter. The trim value is sign magnitude number. When the accumulator reaches overflow, it will advance the counter one additional count if the trim value is positive, or prevent the counter from advancing one count if the trim value is negative. This mechanism allows the RTC counter to be adjusted to keep accurate time with a minimum 0.5 second resolution. When using the high speed oscillator, the RTC counter wants to have an extra count added every 9375 seconds to keep the RTC counter at the proper time. If the one second RTC counter rate is used, the RTC Trim value should be set to 0x6FD (1789 decimal). This value is derived by taking the resolution of the 24 bit accumulator (2 ^ 24 = 16777216) and dividing this by 9375. This means the RTC accumulator will overflow every 9375 seconds and will cause the RTC counter to advance by 2 when the accumulator overflow occurs, thus bringing the RTC count to the proper time.

In addition to the basic software watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, hardware watchdog timer (WDT) is included with the 73S1215F RTC. The Watch Dog timer will give the MPU ½ second to respond to the RTC Interrupt. If the processor does not perform an RTC Interrupt service, a full RESET will be performed. The RTC interrupt is connected to the core interrupt "external interrupt 5" signal. The RTC interrupt must be enabled to obtain the watchdog timer function. Note: if the power down mode doesn't want the watchdog to wake up the MPU, the RTC interrupt should be masked before entering the power down mode.

Real Time Clock Control Register (RTCCtl)

MSB							LSB
-	-	RTCLD	CTSEL.1	CTSEL.0	RINT.2	RINT.1	RINT.0

Table 78: The RTCCtl Register

Bit	Symbol	Function
RTCCtl.7	-	
RTCCtl.6	-	
RTCCtl.5	RTCLD	When set, RTC parameters (RTC Count, RTC Accumulator, and RTC Trim) are loaded at the next 32kHz clock positive edge.
RTCCtl.4	CTSEL.1	Selects the time value that is counted by the real time clock: 0x – 1 second (default) 10 – ½ second 11 – 2 seconds
RTCCtl.3	CTSEL.0	
RTCCtl.2	RINT.2	RTC interrupt internal selection bits: (listed as bits 2,1,0) 100 – 0.5 second 0xx – 1 second (default) 101 – 2 seconds 110 – 4 seconds 111 – 8 seconds
RTCCtl.1	RINT.1	
RTCCtl.0	RINT.0	

Table 79: The RTCCtl Register Bit Functions

There are 3 sets of registers to load the RTC 24-bit accumulator, 32-bit counter and 23 bit-trim registers. The registers are loaded when the RTCLD bit is set in RTCCtl.

RTC Counter:

Register	RTCCnt3	RTCCnt2	RTCCnt1	RTCCnt0
	RTCCnt[31:24]	RTCCnt[23:16]	RTCCnt[15:8]	RTCCnt[7:0]

Table 80: The 32-bit RTC Counter

RTC Accumulator:

Register		RTCACC2	RTCACC1	RTCACC0
		RTCACC [23:16]	RTCACC [15:8]	RTCACC [7:0]

Table 81: The 24-bit RTC Accumulator

RTC Trim (24 bit sign magnitude value):

Register		RTCTrim2	RTCTrim1	RTCTrim0
		RTCTrim [23:16]	RTCTrim [15:8]	RTCTrim [7:0]

Table 82: The 24-bit RTC Trim

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

MSB							LSB
PDMUX	-	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Table 83: The INT5Ctl Register

Bit	Symbol	Function
INT5Ctl.7	PDMUX	Power down multiplexer control.
INT5Ctl.6	-	
INT5Ctl.5	RTCIEN	When set =1, enables RTC interrupt.
INT5Ctl.4	RTCINT	When set =1, indicates interrupt from Real Time Clock function. Cleared on read of register.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Table 84: The INT5Ctl Register Bit Functions

Analog Voltage Comparator

The 73S1215F includes a programmable comparator that is connected to the ANA_IN pin. The comparator can be configured to trigger an interrupt if the input voltage rises above or falls below a selectable threshold voltage. The comparator will disable the interrupt for a short period of time after modifying the comparator control register to guard against any false interrupt that might be generated when the comparator is modified and built-in hysteresis prevents the comparator from repeatedly responding to low-amplitude noise. The maximum voltage on the ANA_IN pad should be less than 3 volts. An external resistor divider is required for detecting voltages greater than 3.0 volts. Interrupt control is handled in the INT6Ctl register

Analog Compare Control Register (ACOMP): 0xFFD0 ← 0x00

MSB LSB

ANALVL	-	ONCHG	CPOL	CMPEN	TSEL.2	TSEL.1	TSEL.0

Table 85: The ACOMP Register

Bit	Symbol	Function
ACOMP.7	ANALVL	When read, indicates whether the input level is above or below the threshold. This is a real time value and is not latched, so it may change from the time of the interrupt trigger until read.
ACOMP.6	-	
ACOMP.5	ONCHG	If set, the Ana_interrupt is invoked on any change above or below the threshold, bit 4 is ignored.
ACOMP.4	CPOL	If set = 1, Ana_interrupt is invoked when signal rises above selected threshold. If set = 0, Ana_interrupt is invoked when signal goes below selected threshold (default).
ACOMP.3	CMPEN	Enables power to the analog comparator. 1= Enabled. 0 = Disabled (default).
ACOMP.2	TSEL.2	Sets the voltage threshold for comparison to the voltage on pin ANA_IN. Thresholds are as follows: 000 - 1.00V 001 - 1.24V 010 - 1.40V 011 - 1.50V 100 - 1.75V 101 - 2.00V 110 - 2.30V 111 - 2.50V
ACOMP.1	TSEL.1	
ACOMP.0	TSEL.0	

Table 86: The ACOMP Register Bit Functions

External Interrupt Control Register (INT6Ctl): 0xFF95 ← 0x00

MSB LSB

-	-	VFTIEN	VFTINT	I2CIEN	I2CINT	ANIEN	ANINT

Table 87: The INT6Ctl Register

Bit	Symbol	Function
INT6Ctl.7	-	
INT6Ctl.6	-	
INT6Ctl.5	VFTIEN	VDD fault interrupt enable
INT6Ctl.4	VFTINT	VDD fault interrupt flag
INT6Ctl.3	I2CIEN	I^{2}C interrupt enabled
INT6Ctl.2	I2CINT	I^{2}C interrupt flag
INT6Ctl.1	ANIEN	If ANIEN=1 Analog Compare event interrupt is enabled. When masked (ANIEN=0), ANINT (bit 0) may be set, but no interrupt is generated
INT6Ctl.0	ANINT	(Read Only) Set when the selected ANA_IN signal changes with respect to the selected threshold if Compare_Enable is asserted. Cleared on read of register.

Table 88: The INT6Ctl Register Bit Functions

LED Drivers

The 1215F provides four dedicated output pins for driving LED outputs. The LED driver pins can be configured as current sources that will pull to ground to drive LEDs that are connected to VDD without the need for external current limiting resistors. These pins may be used as general purpose outputs with the programmed pull-down current and a strong (CMOS) pull-up, if enabled. The analog block must be enabled when these outputs are being used to drive the selected output current.

The pins can be used as inputs with consideration of the programmed output current and level. The register bit when read, indicates the state of the pin.

LED Control Register (LEDCtl): 0xFFF3 ← 0xFF

MSB							LSB
-	LPUEN	ISET.1	ISET.0	LEDD3	LEDD2	LEDD 1	LEDD0

Table 89: The LEDCtl Register

Bit	Symbol	Function
LEDCtl.7	-	
LEDCtl.6	LPUEN	0 = Pull-ups are enabled for all of the LED pins.
LEDCtl.5	ISET.1	These two bits control the drive current (to ground) for all of the LED driver pins. Current levels are: 00 = 0ma(off), 01 = 2ma, 10 = 4ma, 11 = 10ma
LEDCtl.4	ISET.0	
LEDCtl.3	LEDD3	Write data controls output level of pin LED3. Read will report level of pin LED3.
LEDCtl.2	LEDD2	Write data controls output level of pin LED2. Read will report level of pin LED2.
LEDCtl.1	LEDD1	Write data controls output level of pin LED1. Read will report level of pin LED1.
LEDCtl.0	LEDD0	Write data controls output level of pin LED0. Read will report level of pin LED0.

Table 90: The LEDCtl Register Bit Functions

I^{2}C Master Interface

The 72S1215F includes a dedicated fast mode, 400kHz I^{2}C Master interface. The I^{2}C interface can read or write 1 or 2 bytes of data per data transfer frame. The MPU communicates with the interface through six dedicated SFR registers: Device Address (*DAR),* Write Data (*WDR*), Secondary Write Data (*SWDR*), Read Data (*RDR*), Secondary Read Data (*SRDR*) and Control and Status (*CSR*). The DAR register is used to set up the slave address and specify if the transaction is a read or write operation. The CSR register sets up, starts the transaction and reports any errors that may occur. When the I^{2}C transaction is complete, the I^{2}C interrupt is reported via external interrupt 6. The I^{2}C interrupt is automatically de-asserted when a subsequent I^{2}C transaction is started. The I^{2}C interface uses a 400kHz clock from the time-base circuits.

I^{2}C Write Sequence

To write data on the I^{2}C Master Bus, the 80515 has to program the following registers according to the following sequence:

1. Write slave device address to Device Address register (DAR). The data contains 7 bits for the slave device address and 1 bit of op-code. The op-code bit should be written with a ‘0’ to indicate a write operation.
2. Write data to Write Data register (WDR). This data will be transferred to the slave device.
3. If writing 2 bytes, set bit 0 of the Control and Status register (CSR) and load the second data byte to Secondary Write Data register (SWDR).
4. Set bit 1 of the CSR register to start I^{2}C Master Bus.
5. Wait for I^{2}C interrupt to be asserted. It indicates that the write on I^{2}C Master Bus is done. Refer to information about the INT6Ctl, IEN1 and IRCON register for masking and flag operation.

The following diagram shows the timing of the I^{2}C write mode:

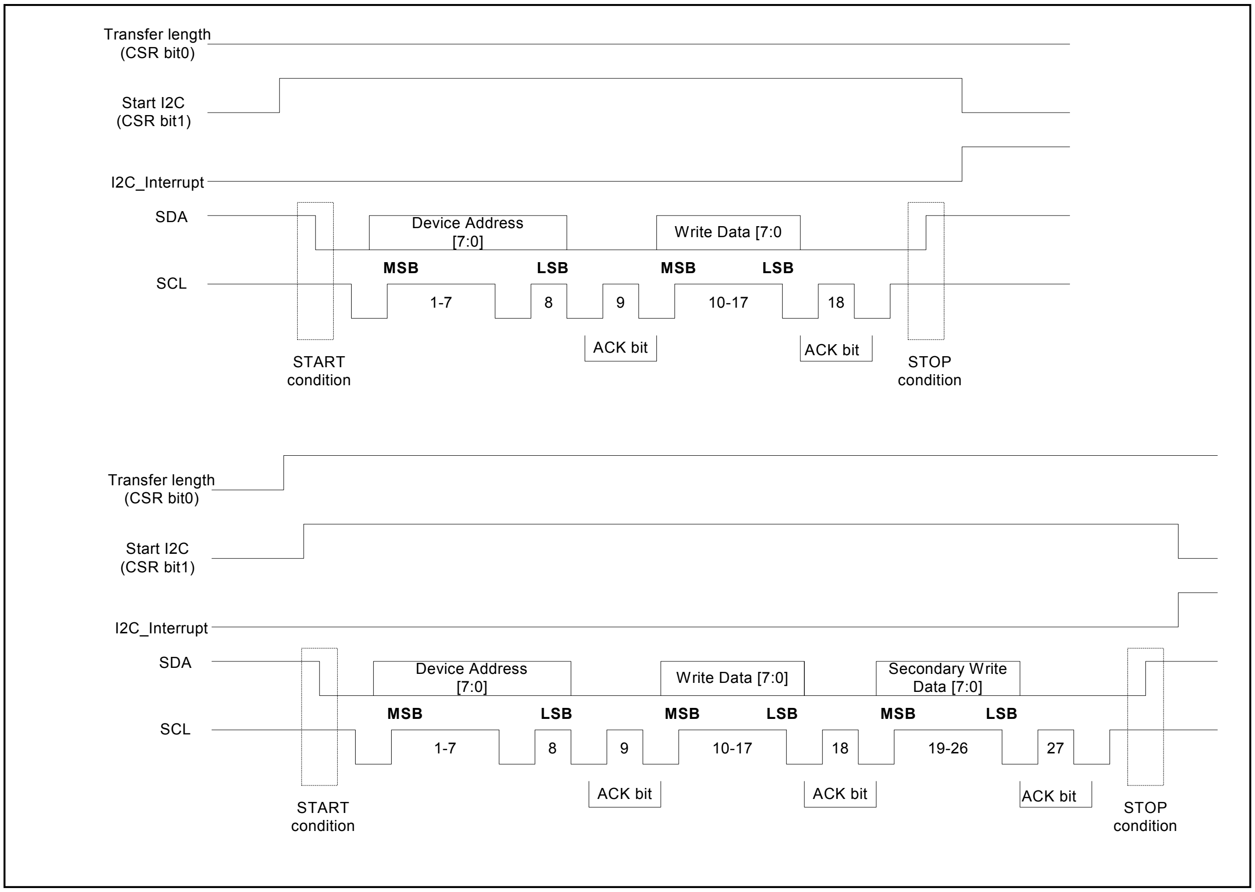


Figure 10 I^{2}C Write Mode Operation

I^{2}C Read Sequence

To read data on the I^{2}C Master Bus from a slave device, the 80515 has to program the following registers in this sequence:

6. Write slave device address to Device Address register. The data contains 7 bits device address and 1 bit of op-code. The op-code bit should be written with a '1'.
7. Write control data to Control and Status register. Write a '1' to bit 1 to start I^{2}C Master Bus. Also write a '1' to bit 0 if the Test Read Data register is to be captured from the I^{2}C Slave device.
8. Wait for I^{2}C interrupt to be asserted. It indicates that the read operation on the I^{2}C bus is done. Refer to information about the INT6Ctl, IEN1 and IRCON registers for masking and flag operation.
9. Read data from the Read Data register.
10. Read data from Test Read Data register if bit 0 of Control and Status register is written with a '1'.

The following diagram shows the timing of the I^{2}C read mode:

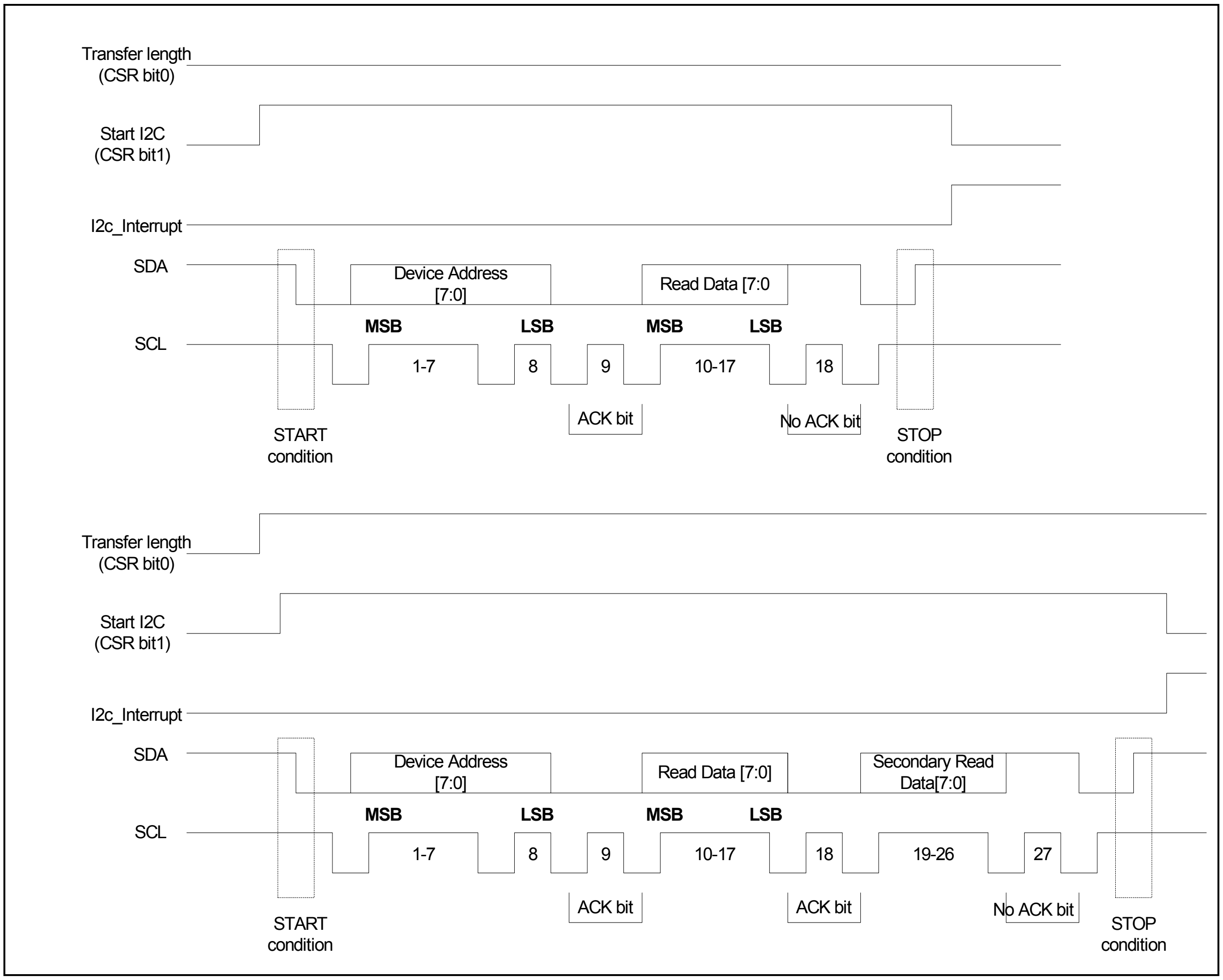


Figure 11 I^{2}C Read Operation

Device Address Register (DAR): 0xFF80 ← 0x00

MSB							LSB
DVADR.6	DVADR.5	DVADR.4	DVADR.3	DVADR.2	DVADR.1	DVADR.0	I2CRW

Table 91: The DAR Register

Bit	Symbol	Function
DAR.7	DVADR [0:6]	Slave device address.
DAR.6		
DAR.5		
DAR.4		
DAR.3		
DAR.2		
DAR.1		
DAR.0	I2CRW	If set=0, the transaction is a write operation. If set=1, read

Table 92: The DAR Register Bit Functions

I2C Control and Status Register (CSR): 0xFF85 ← 0x00

MSB							LSB
-	-	-	-	-	AKERR	I2CST	I2CLEN

Table 93: The CSR Register

Bit	Symbol	Function
CSR.7	-	
CSR.6	-	
CSR.5	-	
CSR.4	-	
CSR.3	-	
CSR.2	AKERR	Set to '1' if acknowledge bit from Slave Device is not '0'. Automatically reset when the new bus transaction is started.
CSR.1	I2CST	Write a '1' to start I^{2}C transaction. Automatically reset to '0' when the bus transaction is done. This bit should be treated as a "busy" indicator on reading. If it is high, the serial read/write operations are not completed and no new address or data should be written.
CSR.0	I2CLEN	Set to '1' for 2 byte read or write operations. Set to '1' for 1 byte operations.

Table 94: The CSR Register Bit Functions

External Interrupt Control Register (INT6Ctl): 0xFF95 ← 0x00

MSB							LSB
-	-	VFTIEN	VFTINT	I2CIEN	I2CINT	ANIEN	ANINT

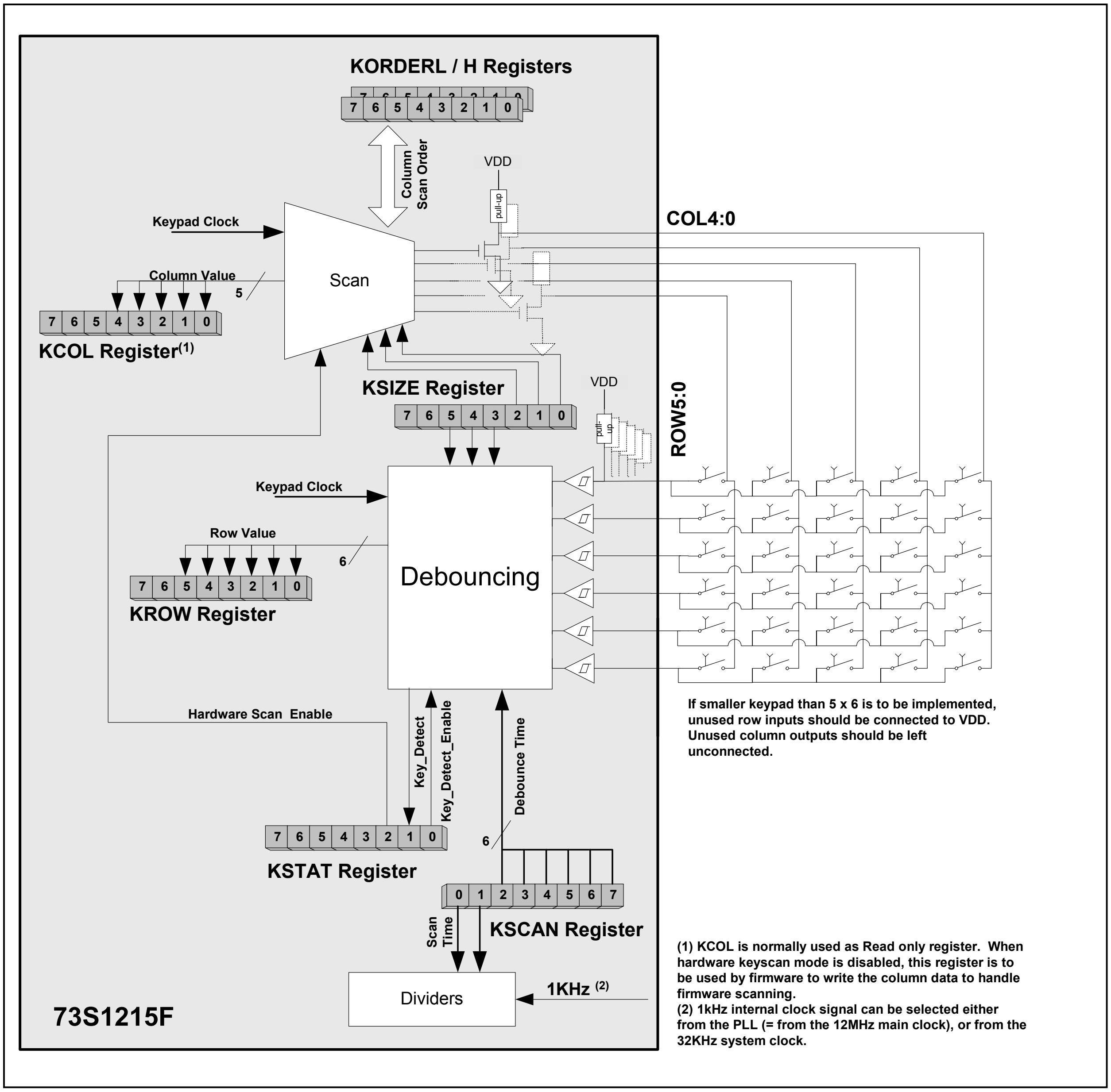
Table 95: The INT6Ctl Register

Bit	Symbol	Function
INT6Ctl.7	-	
INT6Ctl.6	-	
INT6Ctl.5	VFTIEN	VDD fault interrupt enable
INT6Ctl.4	VFTINT	VDD fault interrupt flag
INT6Ctl.3	I2CIEN	When set = 1, the I^2C interrupt is enabled
INT6Ctl.2	I2CINT	When set =1, the I^2C transaction has completed. Cleared upon the start of a subsequent I^2C transaction.
INT6Ctl.1	ANIEN	Analog compare interrupt enable
INT6Ctl.0	ANINT	Analog compare interrupt flag

Table 96: The INT6Ctl Register Bit Functions

Keypad Interface

The 73S1215F supports a 30 (5 row x 6 column) button keypad (SPST Mechanical Contact Switches) interface using 11 dedicated I/O pins. Figure 12 shows a simplified block diagram of the keypad interface.



If smaller keypad than 5 x 6 is to be implemented, unused row inputs should be connected to VDD. Unused column outputs should be left unconnected.

(1) KCOL is normally used as Read only register. When hardware keyscan mode is disabled, this register is to be used by firmware to write the column data to handle firmware scanning.
(2) 1kHz internal clock signal can be selected either from the PLL (= from the 12MHz main clock), or from the 32KHz system clock.

Figure 12 Simplified keypad block diagram

There are 5 drive lines (outputs) corresponding to columns and 6 sense lines(inputs) corresponding to rows. Hysteresis and pull-ups are provided on all inputs (rows), which eliminate the need for external resistors in the keypad. Key scanning happens by asserting one of the 5 column lines low and looking for a low on a sense line indicating that a key is pressed (switch closed) at the intersection of the drive/sense (col/row) line in the keypad. Key detection is performed by hardware with an incorporated debounce timer. Debouncing time is adjustable through the KSCAN Register. Internal hardware circuitry performs column scanning at an adjustable scanning rate and column scanning order through registers KSCAN and KORDERL / KORDERH. Key scanning is disabled at reset and must be enabled by firmware. When a valid key is detected, an interrupt is generated and the valid value of the pressed key is automatically written into KCOL and KROW registers. The keypad interface uses a 1kHz clock derived from either the 32768Hz crystal or the 12MHz crystal (selection is made external to this block, by setting of the bit 6 – KBEN - in the register MCLKCtl, see oscillator and clock generation section) to carry out scanning and debouncing. The keypad size can be adjusted within KSIZE register.

Normal scanning is performed by hardware when the bit SCNEN is set at 1 in register KSTAT. Figure 13 shows the flowchart of how the hardware scanning operates. In order to minimize power, scanning does not occur until a key-press is detected: Once hardware key scanning is enabled, the hardware drives all column outputs low and waits for a low to be detected on one of the inputs. When a low is detected on any row, and before key scanning starts, the hardware checks that the low level is still detected after a debounce time. The debounce time is defined by firmware in the KSCAN register (bits 7:0, DBTIME). Debounce times from 4ms to 256ms in 4ms increments are supported. If a key is not pressed after the debounce time, the hardware will go back to looking for any input to be low. If a key is confirmed to be pressed, key scanning begins.

Key scanning asserts one of the 5 drive lines (COL 4:0) low and looks for a low on a sense line indicating that a key is pressed at the intersection of the drive/sense line in the keypad. After all sense lines have been checked without a key-press being detected, the next column line is asserted. The time between checking each sense line is the scan time and is defined by firmware in the KSCAN register (bits 0:1 – SCTIME). Scan times from 1ms to 4ms are supported. Scanning order does not affect the scan time. This scanning continues until the entire keypad is scanned. If only one key is pressed, a valid key is detected. Simultaneous key presses are not considered as valid (If two keys are pressed, no key is reported to firmware).

Possible scrambling of the column scan order is provided by means of KORDERL and KORDERH registers that define the order of column scanning. Values in these registers must be updated every time a new keyboard scan order is desired. It is not possible to change the order of scanning the sense lines.

The column and row intersection for the detected valid key are stored in the KCOL and KROW registers. When a valid key is detected an interrupt is generated. Firmware can then read those registers to determine which key had been pressed. After reading the KCOL and KROW registers, the firmware can update the KORDERL / KORDERH registers if a new scan order is needed.

When the SCNEN bit is enabled in the KSTAT register, the KCOL and KROW registers are only updated after a valid key has been identified. The hardware does not wait for the firmware to service the interrupt in order to proceed with the key scanning process. Once the valid key (or invalid key – e.g. two keys pressed) is detected, the hardware waits for the key to be released. Once the key is released, the debounce timer is started. If the key is not still released after the debounce time, the debounce counter starts again. After a key release, all columns will be driven low as before and the process will repeat waiting for any key to be pressed.

When SCNEN bit is disabled, all drive outputs are set to the value in KCOL register. If firmware clears the SCNEN bit in the middle of a key scan, the KCOL register contains the last value stored in there which will then be reflected on the output pins.

A bypass mode is provided so that the firmware can do the key scanning manually (SCNEN bit must be cleared). In bypass mode, the firmware writes/reads the Column and Row registers to perform the key scanning.

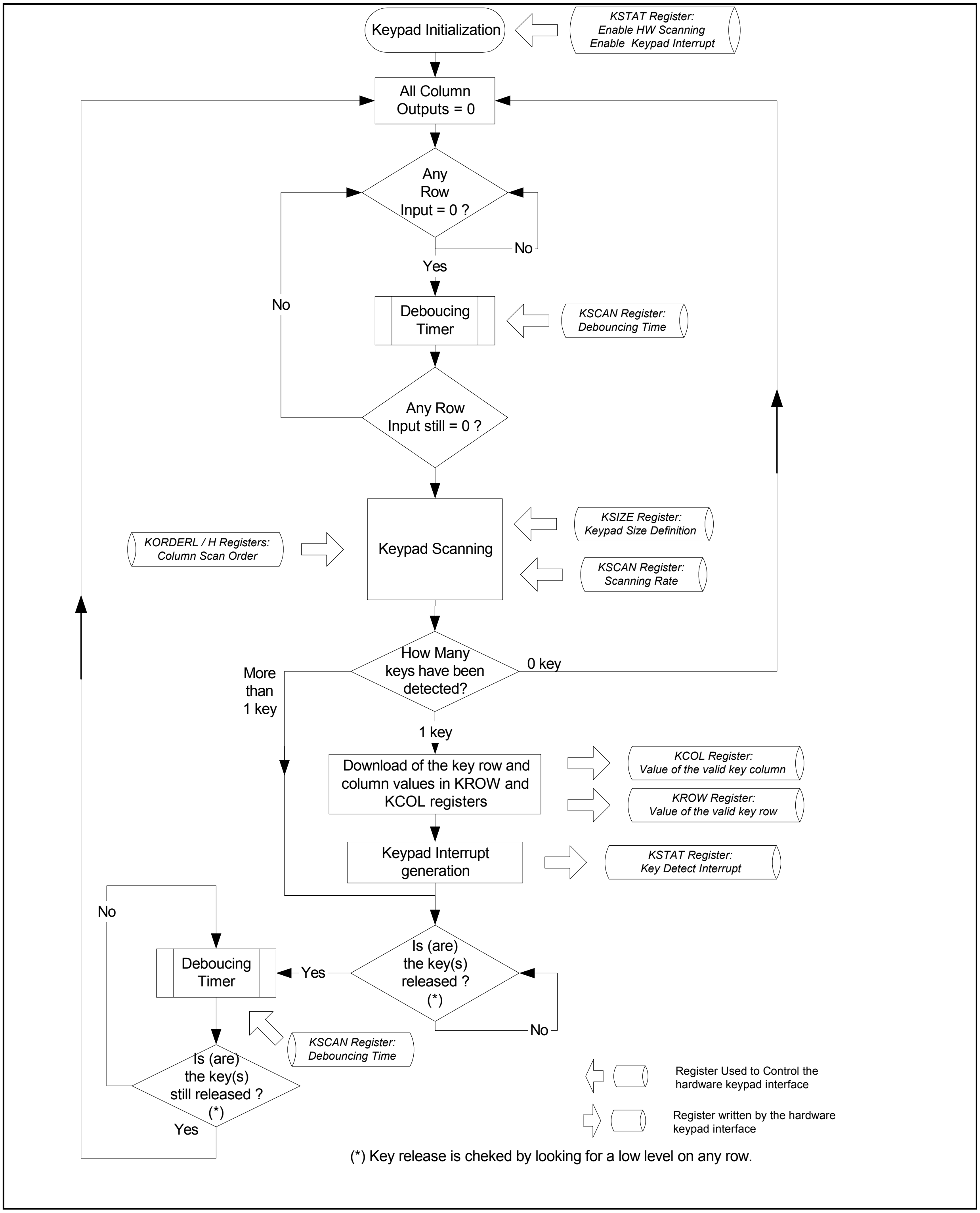

Keypad Initialization
KSTAT Register: Enable HW Scanning Enable Keypad Interrupt
All Column Outputs = 0
Any Row Input = 0 ?
No
Yes
No
Deboucing Timer
KSCAN Register: Debouncing Time
Any Row Input still = 0 ?
KORDERL / H Registers: Column Scan Order
Keypad Scanning
KSIZE Register: Keypad Size Definition
KSCAN Register: Scanning Rate
How Many keys have been detected?
More than 1 key
0 key
1 key
Download of the key row and column values in KROW and KCOL registers
KCOL Register: Value of the valid key column
KROW Register: Value of the valid key row
Keypad Interrupt generation
KSTAT Register: Key Detect Interrupt
No
Deboucing Timer
Yes
Is (are) the key(s) released ? (*)
No
KSCAN Register: Debouncing Time
Is (are) the key(s) still released ? (*)
Yes
Register Used to Control the hardware keypad interface
Register written by the hardware keypad interface
(*) Key release is cheked by looking for a low level on any row.

Figure 13: Keypad interface flow chart

Keypad Column Register (KCOL): 0xD1 ← 0x1F

MSB							LSB
-	-	-	COL.4	COL.3	COL.2	COL.1	COL.0

Table 97: The KCOL Register

This register contains the value of the column of a key detected as valid by the hardware. In bypass mode, this register firmware writes directly this register to carry out manual scanning.

Bit	Symbol	Function
KCOL.7	-	
KCOL.6	-	
KCOL.5	-	
KCOL.4	COL.4	Drive lines bit mapped to corresponding with pins COL(4:0). When a key is detected firmware reads this register to determine column. In bypass (S/W keyscan) mode, Firmware writes this register directly. 0x1E = COL(0) low, all others high. 0x0F = COL(4) low, all others high. 0x1F = COL(4:0) all high.
KCOL.3	COL.3	
KCOL.2	COL.2	
KCOL.1	COL.1	
KCOL.0	COL.0	

Table 98: The KCOL Register Bit Functions

Keypad Row Register (KROW): 0xD2 ← 0x3F

MSB							LSB
-	-	ROW.5	ROW.4	ROW.3	ROW.2	ROW.1	ROW.0

Table 99: The KROW Register

This register contains the value of the row of a key detected as valid by the hardware. In bypass mode, this register firmware reads directly this register to carry out manual detection.

Bit	Symbol	Function
KROW.7	-	
KROW.6	-	
KROW.5	ROW.6	Sense lines bit mapped to correspond with pins ROW(5:0). When key detected, firmware reads this register to determine row. In bypass mode, firmware reads rows and has to determine if there was a key press or not. 0x3E = ROW(0) low, all others high. 0x1F = ROW(5) low, all others high. 0x3F = ROW(5:0) all high.
KROW.4	ROW.4	
KROW.3	ROW.3	
KROW.2	ROW.2	
KROW.1	ROW.1	
KROW.0	ROW.0	

Table 100: The KROW Register Bit Functions

Keypad Scan Time Register (KSCAN): 0xD3 ← 0x00

MSB							LSB
DBTIME.5	DBTIME.4	DBTIME.3	DBTIME.2	DBTIME.1	DBTIME.0	SCTIME.1	SCTIME.0

Table 101: The KSCAN Register

This register contains the values of scanning time and debouncing time.

Bit	Symbol	Function
KSCAN.7	DBTIME.5	De-bounce time in 4ms increments. 1 = 4ms De-bounce time, 0x3F = 252ms, 0x00 = 256ms. Key presses and key releases are de-bounced by this amount of time.
KSCAN.6	DBTIME.4	
KSCAN.5	DBTIME.3	
KSCAN.4	DBTIME.2	
KSCAN.3	DBTIME.1	
KSCAN.2	DBTIME.0	
KSCAN.1	SCTIME.1	Scan time in ms. 01= 1ms, 02 = 2ms, 00 = 3ms, 00 = 4ms. Time between checking each key during keypad scanning.
KSCAN.0	SCTIME.0	

Table 102: The KSCAN Register Bit Functions

Keypad Control/Status Register (KSTAT): 0xD4 ← 0x00

MSB							LSB
-	-	-	-	KEYCLK	HWSCEN	KEYDET	KYDTEN

Table 103: The KSTAT Register

This register is used to control the hardware keypad scanning and detection capabilities, as well as the keypad interrupt control and status

Bit	Symbol	Function
KSTAT.7	-	
KSTAT.6	-	
KSTAT.5	-	
KSTAT.4	-	
KSTAT.3	KEYCLK	The current state of the keyboard clock can be read from this bit.
KSTAT.2	HWSCEN	Hardware Scan Enable - When set, the hardware will perform automatic key scanning. When cleared, the firmware must perform the key scanning manually (bypass mode).
KSTAT.1	KEYDET	Key Detect - When HWSCEN = 1 this bit is set causing an interrupt that indicates a valid key press was detected and the key location can be read from the Keypad Column and Row registers. When HWSCEN = 0, this bit is an interrupt which indicates a falling edge on any Row input if all Row inputs had been high previously (note: multiple Key Detect interrupts may occur in this case due to the keypad switch bouncing). In all cases, this bit is cleared when read. When HWSCEN = 0 and the keypad interface 1kHz clock is disabled, a key press will still set this bit and cause an interrupt.
KSTAT.0	KYDTEN	Key Detect Enable - When set, the KEYDET bit can cause an interrupt and when cleared the KEYDET cannot cause an interrupt. KEYDET can still get set even if the interrupt is not enabled.

Table 104: The KSTAT Register Bit Functions

Keypad Scan Time Register (KSIZE): 0xD5 ← 0x00

MSB LSB

-	-	ROWSIZ.2	ROWSIZ.1	ROWSIZ.0	COLSIZ.2	COLSIZ.1	COLSIZ.0

Table 105: The KSIZE Register

This register is not applicable when HWSCEN is not set. Unused row inputs should be connected to VPD.

Bit	Symbol	Function
KSIZE.7	-	
KSIZE.6	-	
KSIZE.5	ROWSIZ.2	Defines the number of rows in the keypad. Maximum number is 6 given the number of row pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.4	ROWSIZ.1	
KSIZE.3	ROWSIZ.0	
KSIZE.2	COLSIZ.2	Defines the number of columns in the keypad. Maximum number is 5 given the number of column pins on the package. Allows for a reduced keypad size for scanning.
KSIZE.1	COLSIZ.1	
KSIZE.0	COLSIZ.0	

Table 106: The KSIZE Register Bit Functions

Keypad Column LS Scan Order Register (KORDERL): 0xD6 ← 0x00

MSB							LSB
3COL.1	3COL.0	2COL.2	2COL.1	2COL.0	1COL.2	1COL.1	1COL.0

Table 107: The KORDERL Register

Keypad Column MS Scan Order Register (KORDERM): 0xD7 ← 0x00

MSB							LSB
-	5COL.2	5COL.1	5COL.0	4COL.2	4COL.1	4COL.0	3COL.2

Table 108: The KORDERN Register

In registers KORDERL and KORDERM Column Scan Order(14:0) is grouped into 5 sets of 3 bits each. Each set determines which column (COL(4:0) pin) to activate by loading the column number into the 3 bits. When in HW_Scan_Enable mode, the hardware will step through the sets from 1Col to 5Col (up to the number of columns in Colsize) and scan the column defined in the 3 bits. To scan in sequential order, set a counting pattern with 0 in set 0, and 1 in set 1,and 2 in set 2, and 3 in set 3, and 4 in set 4. The firmware should update this as part of the interrupt service routine so that the new scan order is loaded prior to the next key being pressed. For example, to scan COL(0) first, 1Col(2:0) should be loaded with 000'b. To scan COL(4) fifth, 5Col(2:0) should be loaded with 100'b.

Bit	Symbol	Function
KORDERL.7	3COL.1	Column to scan 3rd (lsb's).
KORDERL.6	3COL.0	
KORDERL.5	2COL.2	Column to scan 2nd.
KORDERL.4	2COL.1	
KORDERL.3	2COL.0	
KORDERL.2	1COL.2	Column to scan 1st.
KORDERL.1	1COL.1	
KORDERL.0	1COL.0	

Table 109: The KORDERL Register Bit Functions

Bit	Symbol	Function
KORDERH.7	-	
KORDERH.6	5COL.2	Column to scan 5th.
KORDERH.5	5COL.1	
KORDERH.4	5COL.0	
KORDERH.3	4COL.2	Column to scan 4th.
KORDERH.2	4COL.1	
KORDERH.1	4COL.0	
KORDERH.0	3COL.2	Column to scan 3rd (msb).

Table 110: The KORDERH Register Bit Functions

Emulator Port

The emulator port, consisting of the pins E_RST, E_TCLK and E_RXTX provides control of the MPU through an external in-circuit emulator. The E_TBUS[3:0] pins, together with the E_ISYNC/BRKRQ add trace capability to the emulator. The emulator port is compatible with the ADM51 emulators manufactured by Signum Systems.

The signals of the emulator port have weak pull-ups. Adding resistor footprints for signals E_RST, E_TCLK and E_RXTX on the PCB is recommended. If necessary, adding 1kΩ pull-up resistors will help the emulator operate normally if a problem arises.

USB Interface

The 73S1215F provides a single interface, full speed -12Mbps - USB device port as per USB Spec 2.0 (backward compatible with USB 1.1). USB circuitry gathers the transceiver, the Serial Interface Engine (SIE), and the data buffers. An internal pull-up to V_{DD} on D+ indicates that the device is a full speed device attached to the USB bus (allows full speed recognition by the host without adding any external components). When using the USB interface, V_{PD} must be between 3.0V – 3.6V in order to meet the USB VOH requirement. The interface is highly configurable under firmware control. Control (Endpoint 0), Interrupt IN, Bulk IN and Bulk OUT transfers are supported. Four endpoints are supported and are configured by firmware:

- Endpoint 0, the default (Control) endpoint as required by the USB spec, is used to exchange control and status information between the 73S1215F and the USB host.
- Bulk IN Endpoint #1
- Bulk OUT Endpoint #1
- Interrupt IN Endpoint #2

The USB block contains several FIFOs used for communication.

- There is a 128 byte RAM FIFO for each BULK endpoint. Maximum Bulk packet size is 64 bytes.
- There is a 32 byte RAM FIFO for the interrupt endpoint. Maximum Interrupt packet size is 16 bytes.
- There is a 16 byte RAM FIFO for the control endpoint. Maximum Control packet size is 16 bytes.

Figure 14 shows the simplified block diagram of the USB interface.

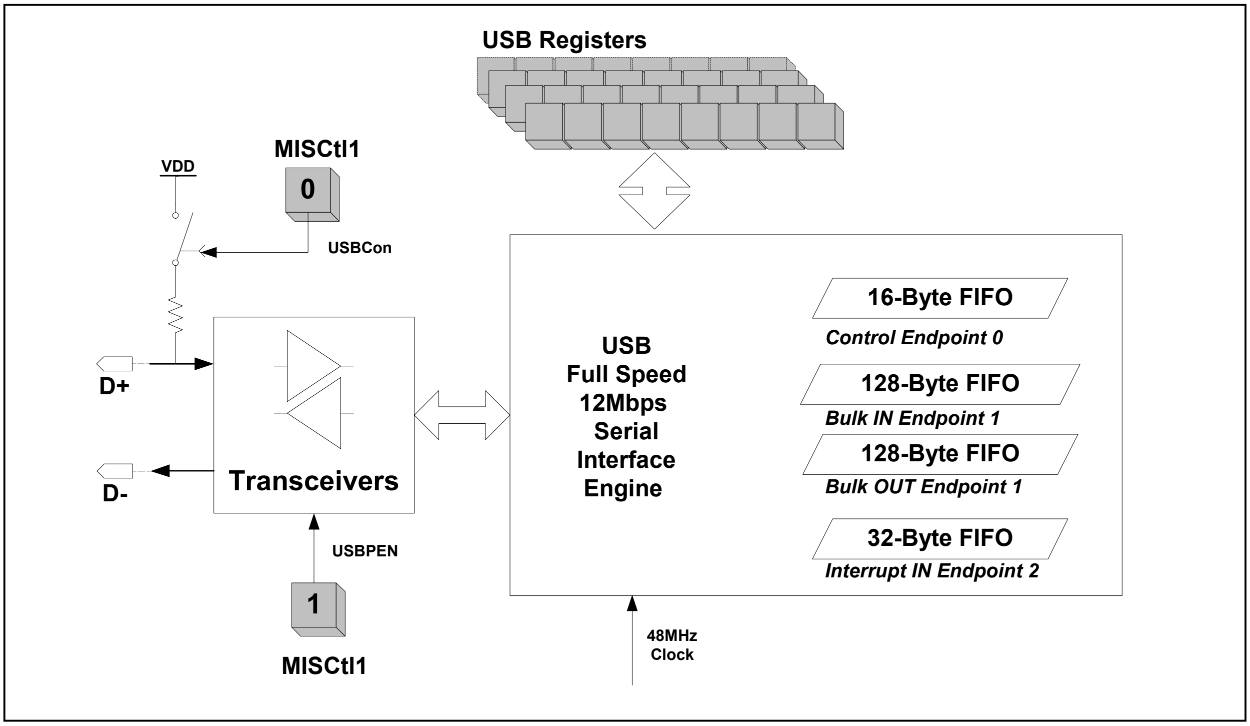


Figure 14: USB Block Diagram

USB interface consists in a SIE that handles NRZI encoding/decoding, bit stuffing / unstuffing, and CRC generation/checking. It also generates headers for packets to be transmitted and decodes the headers of received packets. An analog transceiver interfaces with the external USB bus. The USB interface hardware performs error checking and removes the USB protocol fields from the incoming messages before passing the data to the firmware. The hardware also adds the USB protocol fields to the outgoing messages coming from the firmware. The hardware implements NRZI encoding/decoding, CRC checking/generation (both on data and token packets), device address decoding, handshake packet generation, Data0/Data1 toggle synchronization, bit stuffing, bus idle detection and other protocol generation/checking required in Chapter 8 of the USB specification.

The firmware is responsible for servicing and building of the messages required under Chapter 9 of the USB specification. Device configuration is stored in the firmware. Data received from the USB port is stored in the appropriate IN FIFO that is read by the firmware and processed. The messages to be sent back to the USB host are generated by firmware and placed back into the appropriate OUT FIFO. Stall/NAK handshakes are generated as appropriate if the RAM is not available for another message from the USB host. Suspend and resume modes are supported. All register/FIFO spaces are located in Data Memory space. The FIFOs are dedicated for USB storage and are unused in a configuration that is not using USB. All registers in the USB interface are located in external data memory address (XRAM) space starting at address FC00'h.

USB Interface Implementation

TERIDIAN Semiconductor provides within the 73S1215F Application Programming Interface, some dedicated software commands to configure the USB interface, to get a status of each USB Endpoint, to stall / unstall portions of the USB, and to send / receive data to / from each endpoint.

USB API entirely manages the USB circuitry, the USB registers and the FIFOs. Use of those commands facilitates USB implementation, without dealing with low-level programming.

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

MSB LSB

-	-	FRPEN	FLSH66	-	ANAPEN	USBPEN	USBCON

Table 111: The MISCtl1 Register

Bit	Symbol	Function
MISCtl1.7	-	
MISCtl1.6	-	
MISCtl1.5	FRPEN	Flash Read Pulse enable.
MISCtl1.4	FLSH66	Flash read pulse.
MISCtl1.3	-	
MISCtl1.2	ANAPEN	Analog power enable.
MISCtl1.1	USBPEN	0= Enable the USB differential transceiver.
MISCtl1.0	USBCON	1=Connect pull-up resistor from VDD to D+. If connected, the USB host will recognize the attachment of a USB device and begin enumeration.

Table 112: The MISCtl0 Bit Functions.

Note: When using the USB on the 73S1215F, external 27 ohm series resistors must be added to the D+ and D- signals to provide the proper impedance matching on these pins.

Smart card interface Function

The 73S11xxF integrates one ISO-7816 (T=0, T=1) UART, one complete ICC electrical interface as well as an external smart card interface to allow multiple smart cards to be connected using the Teridian 8010 family of interface devices. Figure 15 shows the simplified block diagram of the card circuitry (UART + interfaces), with detail of dedicated XRAM registers.

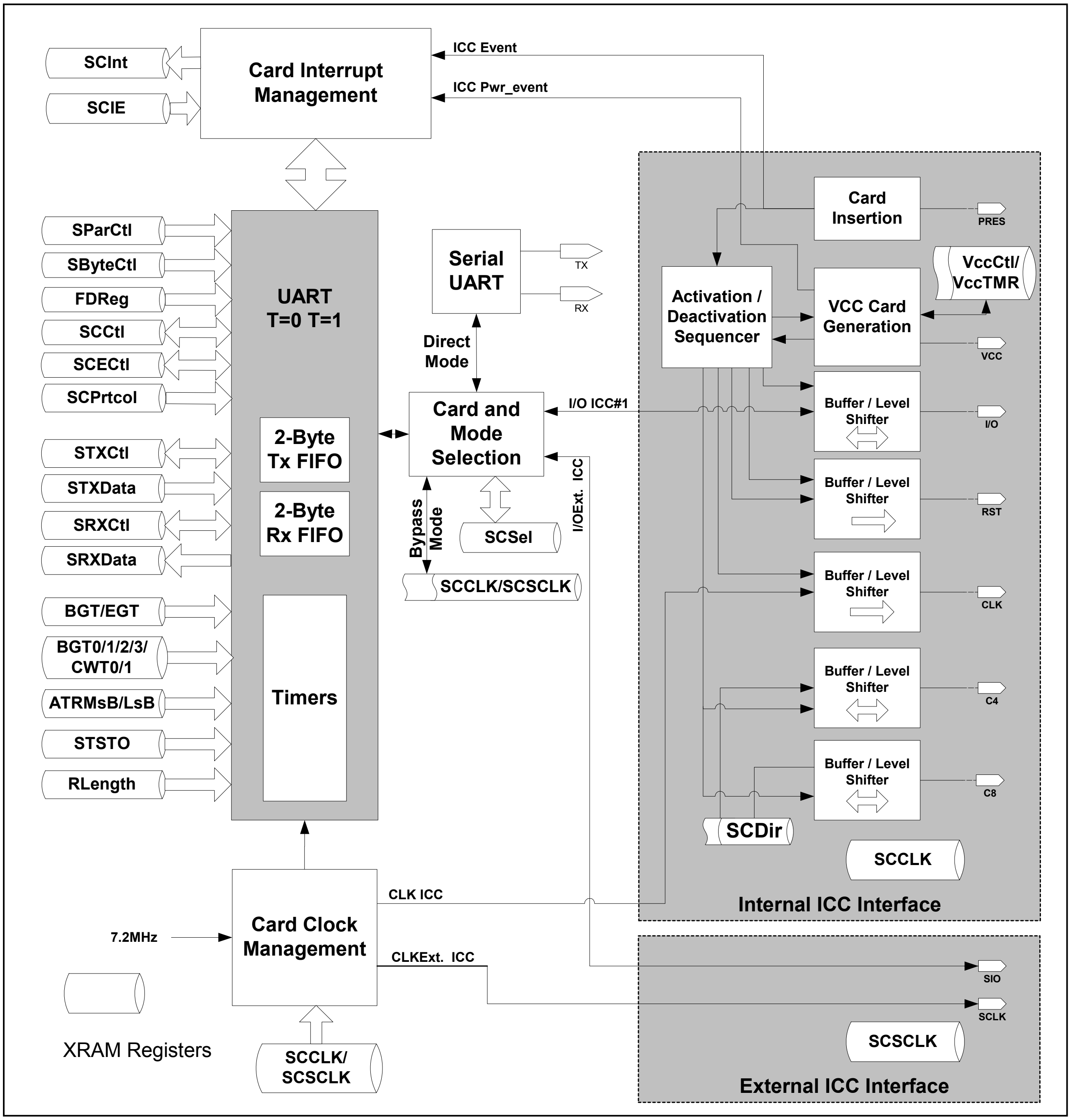


Figure 15: Smart Card Interface Block Diagram

Card interrupts are managed through two dedicated registers SCIE (Interrupt Enable to define which interrupt is allowed) and SCInt (Interrupt status). They allow the firmware to determine the cause of an interrupt, that can be a card insertion / removal, card power fault, or a transmission (TX) or reception (RX) event / fault. It should be noted that even when card clock is disabled, an ICC interrupt can be generated on a card insertion / removal to allow power saving modes. Card insertion / removal is generated from the respective card switch detection inputs (whose polarity is programmable).

The built-in ICC Interface has a low dropout regulator (V_{CC} generator) capable of driving 1.8, 3.0 and 5.0V smart cards in accordance with the ISO-7816-3 and EMV4.0 standards. This converter requires a separate 5.0V input supply source designated as VPC. Auxiliary I/O lines C4 and C8 are only provided for the built-in interface. If support for the auxiliary lines is necessary for the external interfaces, they need to be handled manually through the USR GPIO pins. The external 8010 devices directly connect the I/O (SIO) and clock (SCLK) signals and control is handled via the I^2C interface.

Figure 16 shows how multiple 8010 devices can be connected to the 73S1215F.

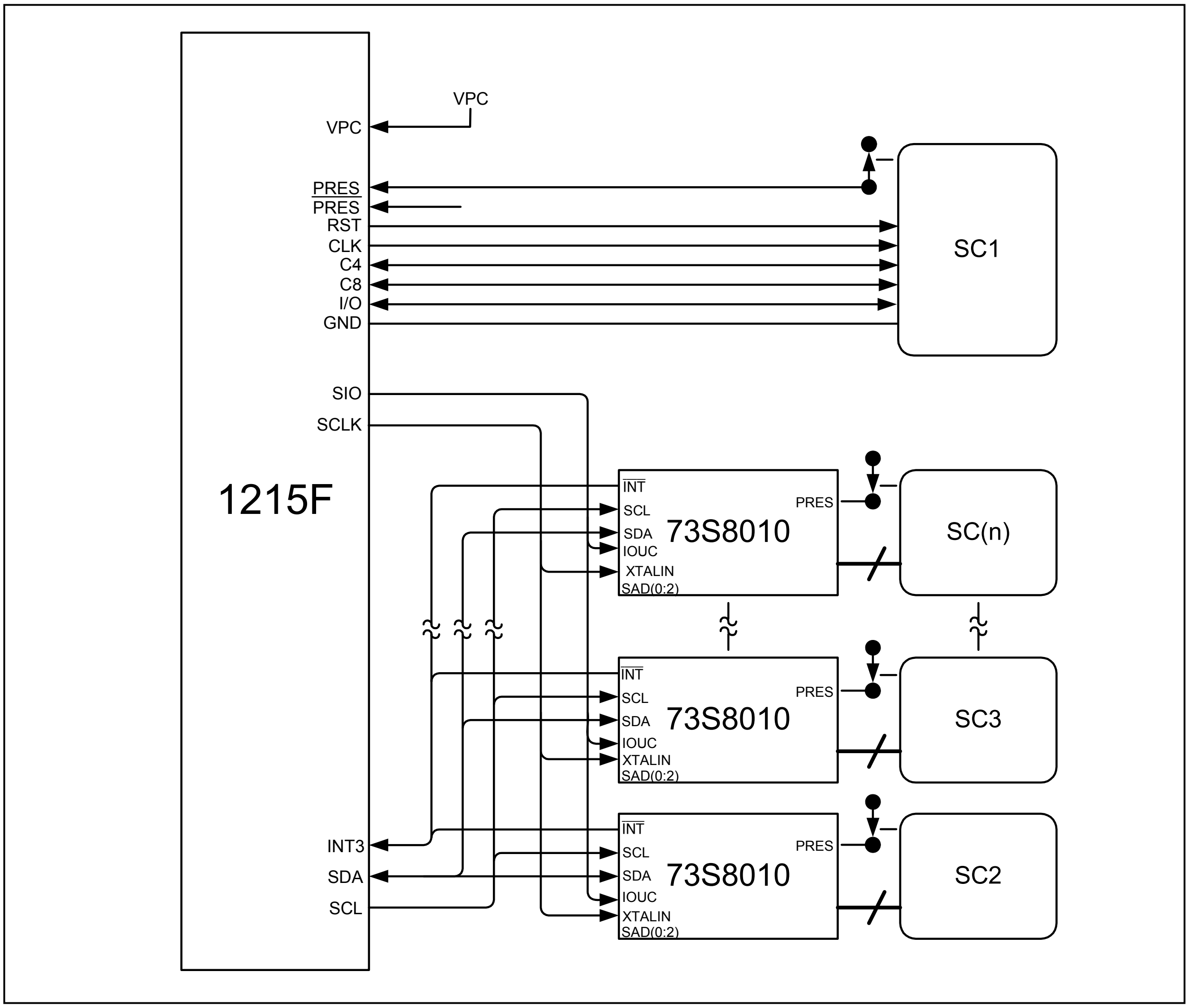


Figure 16: Smart Card Interface Block Diagram

ISO-7816 UART

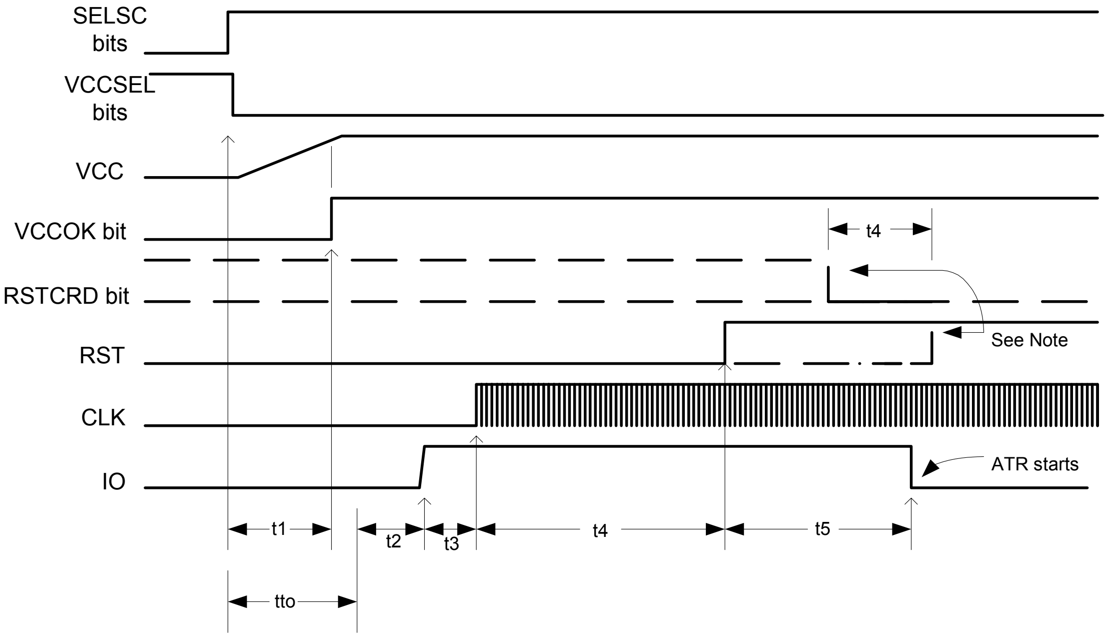
An embedded ISO-7816 (hardware) UART is provided to control communications between a smart card and the 73S1215F MPU. The UART can be shared between the one built-in ICC interface and the external ICC interface. Selection of the desired interface is made by register SCSel. Control of the external interface is handled by the I^2C interface for any external 8010 devices. The following is a list of features for the ISO-7816 UART:

- Two-byte FIFO for temporary data storage on both TX and Rx data.
- Parity checking in T=0. This feature can be enabled/disabled by firmware. Parity error reporting to firmware and Break generation to ICC can be controlled independently
- Parity error generation for test purposes.
- Retransmission of last byte if ICC indicates T=0 parity error. This feature can be enabled/disabled by firmware.
- Deletion of last byte received if ICC indicates T=0 parity error. This feature can be enabled/disabled by firmware.
- CRC/LRC generation and checking. CRC/LRC is automatically inserted into T=1 data stream by the hardware. This feature can be enabled/disabled by firmware
- Support baud rates: 115200, 57600, 38400, 28800, 19200, 14400, 9600 under firmware control (assuming 12MHz crystal) with various F/D settings
- Firmware manages F/D. All F/D combinations are supported in which F/D is directly divisible by 31 or 32 (i.e. F/D is a multiple of either 31 or 32).
- Flexible ETU clock generation and control.
- Detection of convention (direct or indirect) character TS. This affects both polarity and order of bits in byte. Convention can be overridden by firmware
- Supports WTX Timeout with an expanded Wait Time Counter (28 bits)
- A Bypass Mode is provided to bypass the hardware UART in order for the software to emulate the UART (for non-standard operating modes). In such a case, the I/O line value is reflected in SFR SCCtl or SCECtl respectively for the built-in or external interfaces. This mode is appropriate for synchronous and non T=0 / T=1 cards.
- Direct mode allows connecting the I/O line of the selected ICC interface to serial interface TX/RX for direct connection to a host.

The single integrated smart card UART is capable of supporting T=0 and T=1 cards in hardware therefore offloading the bit manipulation tasks from the firmware. The embedded firmware instructs the hardware which smart card it should communicate with at any point in time. Firmware reconfigures the UART as required when switching between smart cards. When the 73S1215F has transmitted a message with an expected response, the firmware should not switch the UART to another smart card until the first smart card has responded. If the smart card responds while another smart card is selected, that first smart card's response will be ignored.

Answer To Reset Processing

A card insertion event generates an interrupt to the firmware, which is then responsible for the configuration of the electrical interface, the UART and activation of the card. The activation sequencer goes through the power up sequence as defined in the ISO-7816-3 specification. An asynchronous activation timing diagram is shown in Figure 17. After the card reset is de-asserted, the firmware instructs the hardware to look for a TS byte that begins the ATR response. If a response is not provided within the pre-programmed timeout period, an interrupt is generated and the firmware can then take appropriate action, including instructing the 73S1215F to begin a deactivation sequence. Once commanded, the deactivation sequencer goes through the power down sequence as defined in the ISO-7816-3 specification. If an ATR response is received, the hardware looks for a TS byte that determines direct/inverse convention. The hardware handles the indirect convention conversion such that the embedded firmware only receives direct convention. This feature can be disabled by firmware within SByteCtl register. Parity checking and break generation is performed on the TS byte unless disabled by firmware. If during the card session, a card removal, over-current or other error event was detected, the hardware will automatically perform the deactivation sequence and then generate an interrupt to the firmware. The firmware can then perform any other error handling required for proper system operation. Smart card RST, I/O and CLK, C4, C8 shall be low before the end of the deactivation sequence. Figure 18 shows the timing for a deactivation sequence.



t1: SELSC.1 bit set (selects internal ICC interface) and a non-zero value in VCCSEL bits (calling for a value of Vcc of 1.8, 3.0, or 5.0 volts) will begin the activation sequence. t1 is the time for Vcc to rise to acceptable level, declared as Vcc OK (bit VCCOK gets set). This time depends on filter capacitor value and card Icc load.

tto: The time allowed for Vcc to rise to Vcc OK status after setting of the VCCSEL bits. This time is generated by the VCCTMR counter. If Vcc OK is not set, (bit VCCOK) at this time, a deactivation will be initiated. VCCSEL bits are not automatically cleared. The firmware must clear the VCCSEL bits before starting a new activation.

t2: Time from VCCTmr timeout and VCC OK to IO reception (high), typically 2-3 CLK cycles if RDYST = 0. If RDYST = 1, t2 starts when VCCOK = 1.

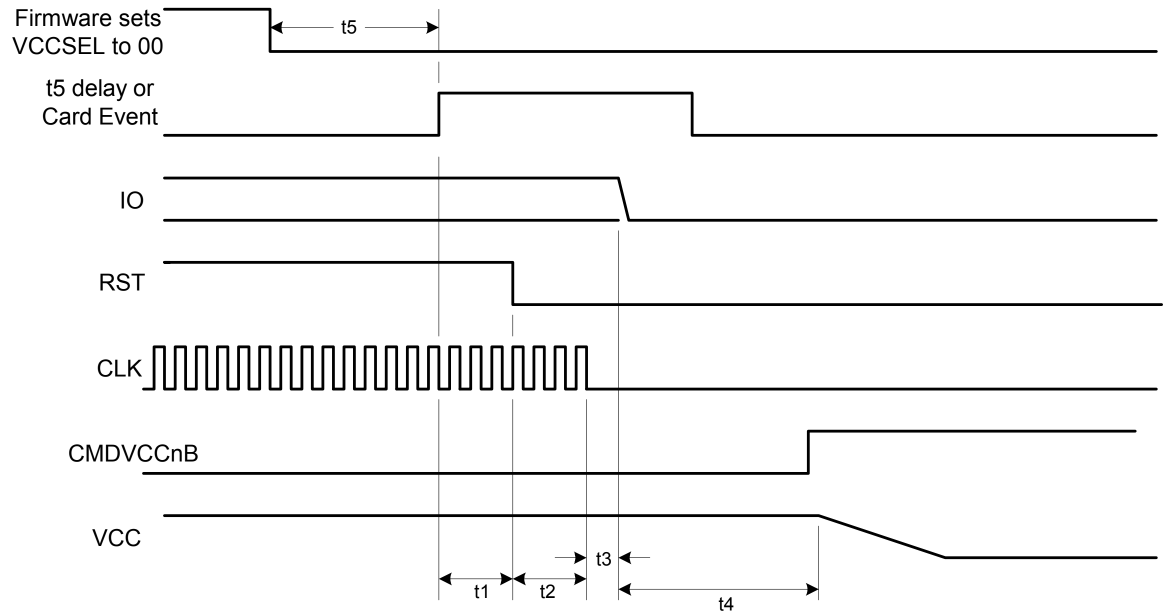
t3: Time from IO = high to CLK start, typically 2-3 CLK cycles.

t4: Time allowed for start of CLK to de-assertion of RST. Programmable by RLength register.

t5: Time allowed for ATR timeout, set by the STSTO register.

Note: If the RSTCRD bit is set, RST is asserted (low). Upon clearing RSTCRD bit, RST will be de-asserted after t4.

Figure 17: Asynchronous Activation Sequence Timing



t1: Time after either a “card event” occurs or firmware sets the VCCSela and VCCSelb bits to 0 (see t5, VCCOff_tmr) occurs until RST is asserted low.

t2: Time after RST goes low until CLK stops.

t3: Time after CLK stops until IO goes low.

t4: Time after IO goes low until VCC is powered down.

t5: Delayed VCC off time (in ETUs per VCCOff_tmr bits). Only in effect due to firmware de-activation.

Figure 18: De-activation Sequence

Data Reception/Transmission

When a 12Mhz crystal is used, the smart card UART will generate a 3.69Mhz (default) clock to both smart card interfaces. This will allow approximately 9600bps (1/ETU) communication during ATR (ISO-7816 default). As part of the PPS negotiation between the smart card and the reader, the firmware may determine that the smart card parameters F & D may be changed. After this negotiation, the firmware may change the ETU by writing to the SFR FDReg to adjust the ETU and CLK. The firmware may also change the smart card clock frequency by writing to the SFR SCCLK (SCSCLK for external interface). Independent clock frequency control is provided to each smart card interface. Clock stop high or Clock stop low is supported in asynchronous mode. Figure 19 shows the ETU and CLK control circuits. The firmware determines when clock stop is supported by the smart card and when it is appropriate to go into that mode (and when to come out of it). The smart card UART is clocked by the same clock is provided to the selected smart card. The transition between smart card clocks is handled in hardware to eliminate any glitches for the UART during switchover. The external smart card clock is not affected when switching the UART to communicate with the internal smart card. The internal interface should not be left in an active state with VCC “on” and CLK running when using the external interface.

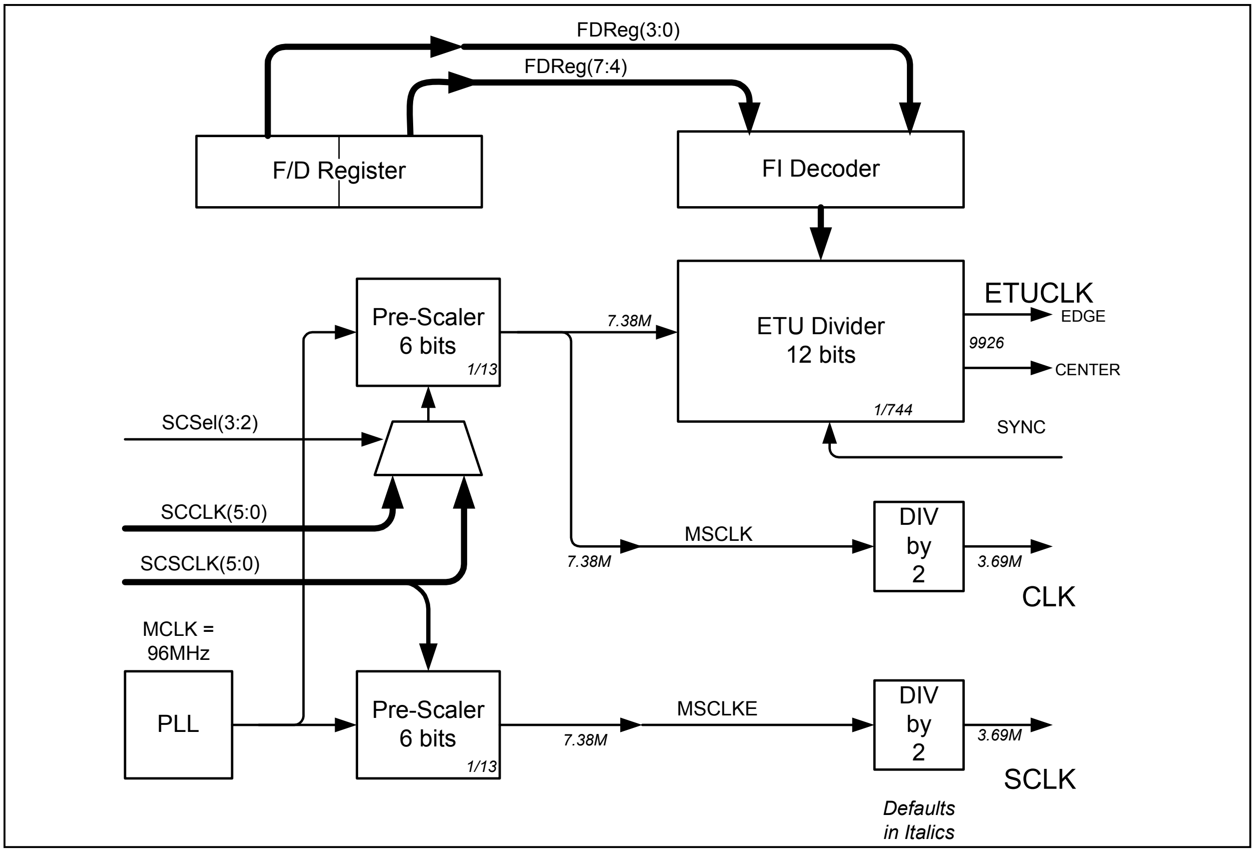


Figure 19: Smart Card CLK and ETU generation

There are two, two-byte FIFOs that are used to buffer transmit and receive data. During a T=0 processing, if a parity error is detected by the 73S1215F during message reception, an error signal (BREAK) will be generated to the smart card. The byte received will be discarded and the firmware notified of the error. Break generation and receive byte dropping can be disabled under firmware control. During the transmission of a byte, if an error signal (BREAK) is detected, the last byte is retransmitted again and the firmware notified. Retransmission can be disabled by firmware. When a correct byte is received, an interrupt is generated to the firmware which then reads the byte from the receive FIFO. Receive overruns are detected by the hardware and reported via an interrupt. During transmission of a message, the firmware will write bytes into the transmit FIFO. The hardware will send them to the smart card. When the last byte of a message has been written, the firmware will need to set the LASTTX bit in the STXCtl SFR. This will cause the hardware to insert the CRC/LRC if in a T=1 protocol mode. CRC/LRC generation/checking is only provided during T=1 processing. Firmware will need to instruct the smart function to go into receive mode after this last transmit data byte if it expects a response from the smart card. At the end of the smart card response, the firmware will put the interface back into transmit mode if appropriate.

The hardware can check for several card related timeouts. These are: the Character Waiting Time (CWT), Block Waiting Time (BWT) and Initial Waiting Time (IWT). The firmware will load the Wait Time registers with the appropriate value for the operating mode at the appropriate time. Figure 20 shows the guard, block, wait and ATR time definitions. If a timeout occurs, an interrupt will be generated and the firmware can take appropriate recovery steps. Support is provided for adding additional guard times between characters (Extra Guard Time register) and between the last byte received by the 73S1215F and the first byte transmitted by the 73S1215F (Block guard time register (BGT). Other than the protocol checks described above, the firmware is responsible for all protocol checking and error recovery.

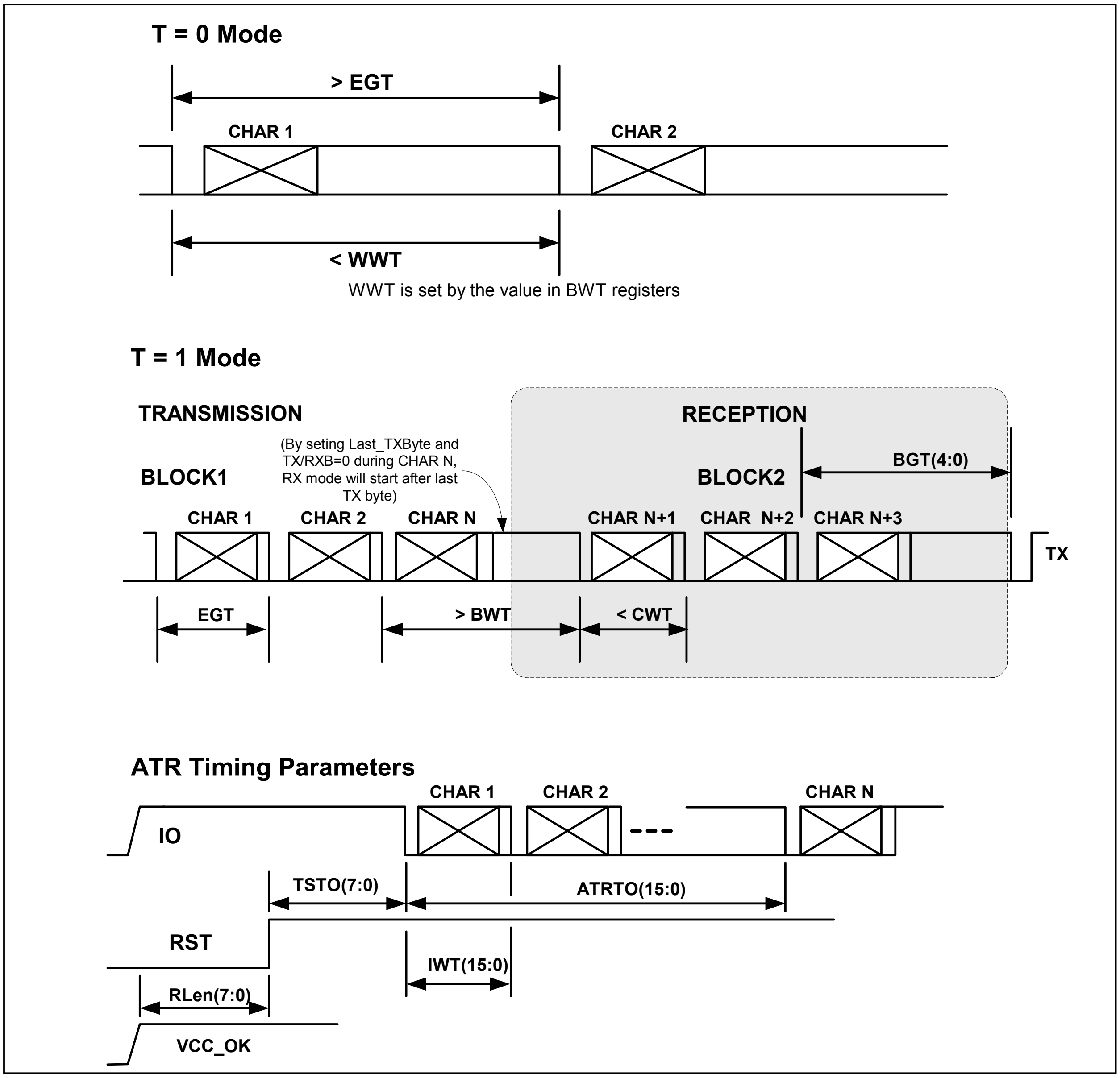


Figure 20: Guard, Block, Wait and ATR Time Definitions

Bypass/Direct Modes

It is possible to bypass the smart card UART in order for the firmware to support non-T=0/T=1 smart cards. This is called Bypass mode. In this mode the embedded firmware will communicate directly with the selected smart card and drive I/O during transmit and read I/O during receive in order to communicate with the smart card. In this mode, ATR processing is under firmware control. The firmware must sequence the interface signals as required. Firmware must perform TS processing, parity checking, break generation and CRC/LRC calculation (if required).

In some applications, it may be desirable for the device (e.g. PC) communicating with the 73S1215F over the serial interface to directly communicate with the smart card instead of using the integrated serial UART and smart card UART. This is called

Direct mode. In Direct mode, the 73S1215F will activate the smart card, receive and process the ATR. It will then pass the ATR over the serial interface to the host (PC). The PC will then instruct the 73S1215F to go into direct mode. When this occurs, a virtual “wire” will connect the smart card I/O line to the serial TXD/RXD lines on the serial interface. The command to go into Direct mode is under firmware control. The hardware will go into Direct mode when commanded by the firmware. The direct mode is shown in Figure 21.

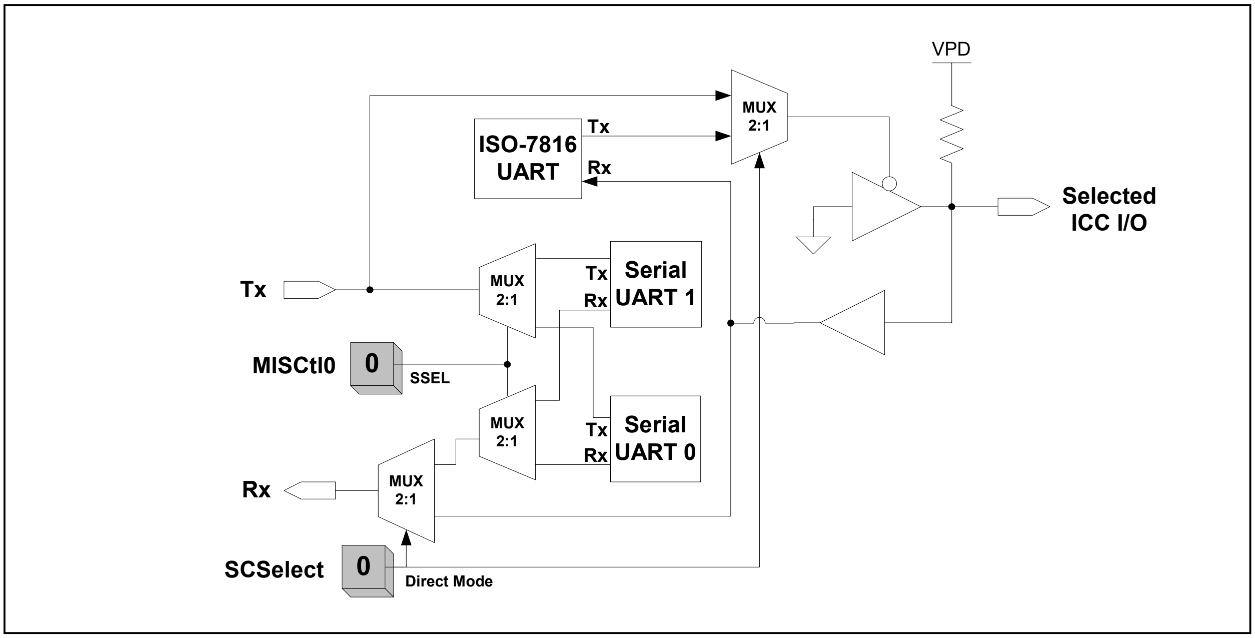


Figure 21: ICC Direct Mode Block Diagram

Synchronous Operation Mode

The 73S1215F supports synchronous operation. When sync mode is selected for either interface, the CLK signal is generated by the ETU counter. The values in FDREG, SCCLK, and SCECLK must be set to obtain the desired sync CLK rate. There is only one ETU counter and therefore, in sync mode, the interface must be selected to obtain a smart card clock signal. The ETU clock is held in reset condition until the activation sequence begins (either by VCCOK = 1 or VCCTMR timeout) and will go high ½ the ETU period thereafter. In sync mode, input data is sampled on the rise of CLK, and output data is changed on the fall of CLK.

Special Notes Regarding Synchronous Mode Operation

When the SCISYN or SCESNC bits (SCPrtcol, bit 7, bit 5, respectively) are set, the selected smart card interface operates in synchronous mode and there are changes in the definition and behavior of pertinent register bits and associated circuitry. The following requirements are to be noted:

1. The source for the smart card clock (CLK or SCLK) is the ETU counter. Only the actively selected interface can have a running synchronous clock. In contrast, an unselected interface may have a running clock in the asynchronous mode of operation.
2. The control bits CLKLVL, SCLKLVL, CLKOFF, and SCLKOFF are functional in synchronous mode. When the CLKOFF bit is set, it will not truncate either the logic low or logic high period when the (stop at) level is of opposite polarity. The CLK/SCLK signal will complete a correct logic low or logic high duty cycle before stopping at the selected level. The CLK “start” is a result of the falling edge of the CLKOFF bit. Setting clock to run when it is stopped low will result in a half period of low before going high. Setting clock to run when it is stopped high will result

in the clock going low immediately and then running at the selected rate with 50% duty cycle (within the limitations of the ETU divisor value).

3. The Rlen(7:0) is configured to count the falling edges of the ETU clock (CLK or SCLK) after it has been loaded with a value from 1 to 255. A value of 0 disables the counting function and RLen functions such as CLK stopping and I/O source selection (I/O signal bypasses the FIFOs and is controlled by the SCCLK/SCSCLK SFRs). When the RLen counter reaches the “max” (loaded) value, it sets the WAITTO interrupt (SEInt, bit 7) which is maskable via WTOIEN (SCIE, bit 7). If CLKOFF/SCLKOFF is high and SYCKST is set =1(STXCtl, b7=1), RLen=max will stop the clock at the selected (CLKLVL or SCLKLVL) level. It must be reloaded in order to start the counting/clocking process again. This allows the processor to select the number of CLK cycles and hence, the number of bits to be read or written to/from the card.
4. The FIFO is not clocked by the first CLK (falling) edge resulting from a CLKOFF de-assertion (a clock start event) when the CLK was stopped in the high state and RLen has been loaded but not yet clocked and SYCKST is set.
5. The state of the pin IO or SIO is sampled on the rising edge of CLK/SCLK and stored in bit 5 of the SCCtl/SCECtl register.
6. When Rlen = max or 0 and SYCKST = 1 (STXCtl, b7), the IO or SIO signal is directly controlled by the data and direction bits in the respective SCCtl and SCECtl register. The state of the data in the TX FIFO is bypassed.
7. In the SCPrtcol register, bit 6 (MODE9/8B) becomes active. When set, the RXData FIFO will read nine-bit words with the state of the ninth bit being readable in SRXCtl, bit 7 (B9DAT). The RXDAV interrupt will occur when the ninth bit has been clocked in (rising edge of CLK or SCLK).
8. Care must be taken to clear the RX and TX FIFOs at the start of any transaction. The user shall read the RX FIFO until it indicates empty status. Reading the TX FIFO twice will reset the input byte pointer and the next write to the TX FIFO will load the byte to the “first out” position. Note that the bit pointer (serializer/deserializer) is reset to bit 0 on any change of the TX/RXD bit.
9. The most complicated protocol is for the sync clock start/stop style interfaces. The SYCKST bit is provided to allow the generation of start and stop signaling operations. Start and stop bits are transitions of the IO signal when CLK is high and by using CLKOFF, CLKLVL, SYCKST bits along with the RLen counter, such patterns can be generated without critical MPU timing.

Special bits that are only active for sync mode include: SRXCTL, b7 “BIT9DAT”, SCPrtcol b6 “MODE9/8B”, STXCtl, b7 “SYCKST”, and the definition of SCInt b7, was “WAITTO”, becomes RLenINT interrupt, and SCIE b7, was “WTOIEN”, becomes RLenIEN.

Table 112 shows the special operating modes for Synchronous and Asynchronous modes of operation. The purpose of this table is to give an overview of the differences between certain outputs when using async or sync operation. The outputs of focus are the smart card CLK , RST, the internal I/O signal routing and the wait timeout interrupt source and trigger.

SCxSYNC	SSYCKST	Rlen	CLK_OFF	CLK_LVL	CLK Output	RST Output	I/O Routing	Wait Timout Interrupt
0	X	0, max	X	X	-	! RSTCRD	FIFO	SC Timers
0	X	1	X	X	-	0	FIFO	SC Timers
0	X	→ max	X	X	-	RSTCRD = 0: ↑ RSTCRD = 1: 0	FIFO	SC Timers
0	X	-	0	X	⎍⎍	-	FIFO	SC Timers
0	X	-	1	0	0	-	FIFO	SC Timers
0	X	-	1	1	1	-	FIFO	SC Timers
1	0	0, max	0	X	⎍⎍	RSTCRD	(S)IO	0
1	0	0, max	1	0	0	RSTCRD	(S)IO	0
1	0	0, max	1	1	1	RSTCRD	(S)IO	0
1	0	0, max	↑	0	0	RSTCRD	(S)IO	0
1	0	0, max	↑	1	1	RSTCRD	(S)IO	0
1	0	1	0	X	⎍⎍	RSTCRD	FIFO	0
1	0	1	1	0	0	RSTCRD	FIFO	0
1	0	1	1	1	1	RSTCRD	FIFO	0
1	0	→ max*	0	0	⎍↓	RSTCRD	FIFO → (S)IO	↑
1	0	→ max*	0	1	⎍↑	RSTCRD	FIFO → (S)IO	↑
1	0	→ max	1	0	0	RSTCRD	FIFO → (S)IO	↑
1	0	→ max	1	1	1	RSTCRD	FIFO → (S)IO	↑
1	1	0, max	X	0	0	RSTCRD	(S)IO	0
1	1	0, max	X	1	1	RSTCRD	(S)IO	0
1	1	1	0	X	⎍⎍	RSTCRD	FIFO	0
1	1	1	1	0	0	RSTCRD	FIFO	0
1	1	1	1	1	1	RSTCRD	FIFO	0
1	1	→ max	0	0	⎍↑	RSTCRD	FIFO → (S)IO	↑
1	1	→ max	0	1	⎍↓	RSTCRD	FIFO → (S)IO	↑
1	1	→ max	1	0	0	RSTCRD	FIFO → (S)IO	↑
1	1	→ max	1	1	1	RSTCRD	FIFO → (S)IO	↑
1	1	1	↓	0	↓	RSTCRD	FIFO	0
1	1	1	↓ = t0	1	t0 → ↑ = ½ ETU	RSTCRD	FIFO	0

SCxSYNC: SPrtcol register bits SCISYN and SCESYN (internal/external SC interfaces) - 0 = async, 1 = sync

SYCKST: STXCtl register bit SYCKST - 0 = nominal, 1 = clock start/stop mode

Rlen: 0 = zero, 1 = non-zero value, max = terminal count (count = Rlen value), → max = terminal count reached

CLK_OFF: 0 = run, 1 = stop. CLK_LVL: 0 = low, 1 = high. RSTCRD: The RSTCRD bit in SCCtl.

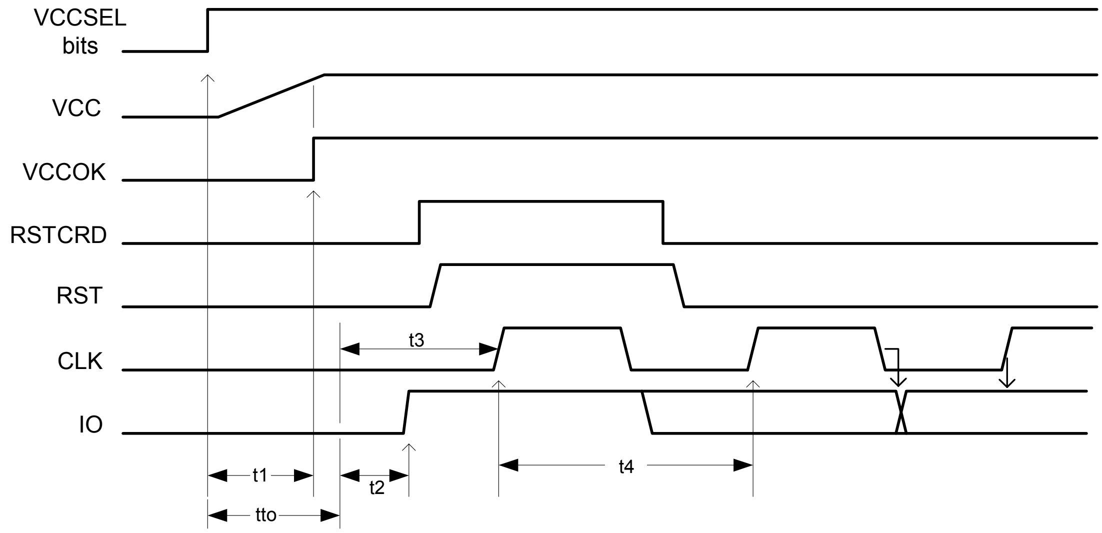
I/O Routing: FIFO corresponds to the ISO UART data FIFO, (S)IO corresponds to the IO bit in SCCtl and SIO bit in SCECtl for the internal/external interfaces (sync mode only).

↓ = t0 – time when CLK_OFF is set low, t0 → ↑ = ½ ETU – CLK goes high one half cycle after CLK_OFF is set low.

Wait timer Interrupt: SC Timers – smart card wait timeout timers, 0 - no interrupt, ↑ - interrupt is set.

*Note: 50% duty cycle will be maintained regardless of when Rlen reaches terminal count within the clock cycle

Table 113: Special Operating Modes for Sync and Async Operation.



t1: The time from setting VCCSEL bits until VCCOK = 1.

tto: The time from setting VCCSEL bits until VCCTMR times out. At t1 (if RDYST = 1) or tto (if RDYST = 0), activation starts. It is suggested to have RDYST = 0 and use the VCCTMR interrupt to let MPU know when sequence is starting.

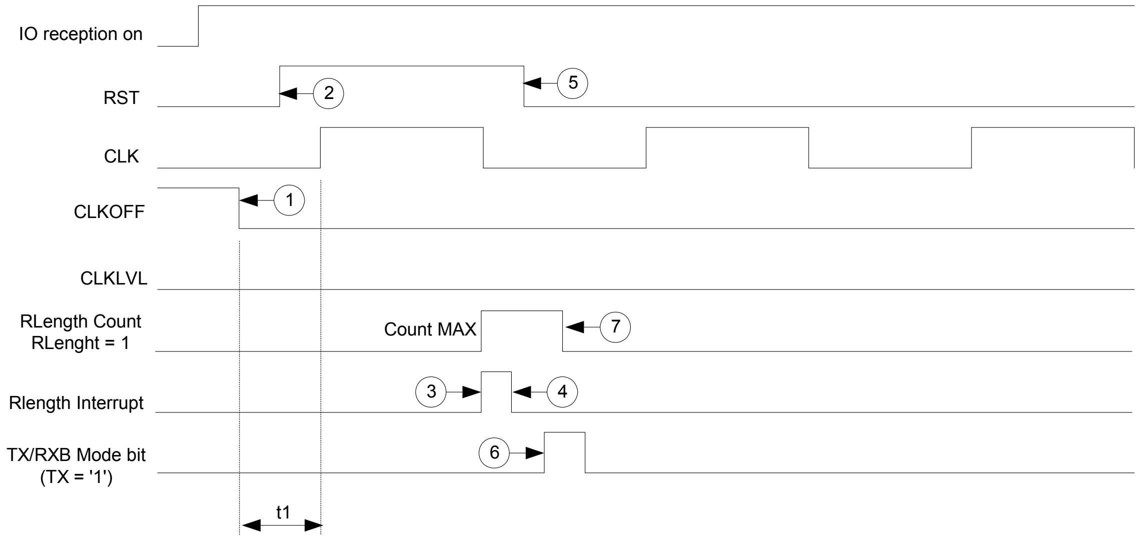
t2: time from start of activation (no external indication) until IO goes into reception mode (= 1). This is approximately 4 SCCLK (or SCECLK) clock cycles.

t3: one half of ETU period

t4: ETU period

Note that in Sync mode, IO as input is sampled on the rising edge of CLK. IO changes on the falling edge of CLK, either from the card or from the 73S1215F. The RST signal to the card is directly controlled by the RSTCRD bit (non-inverted) via the MPU and is shown as an example of a possible RST pattern.

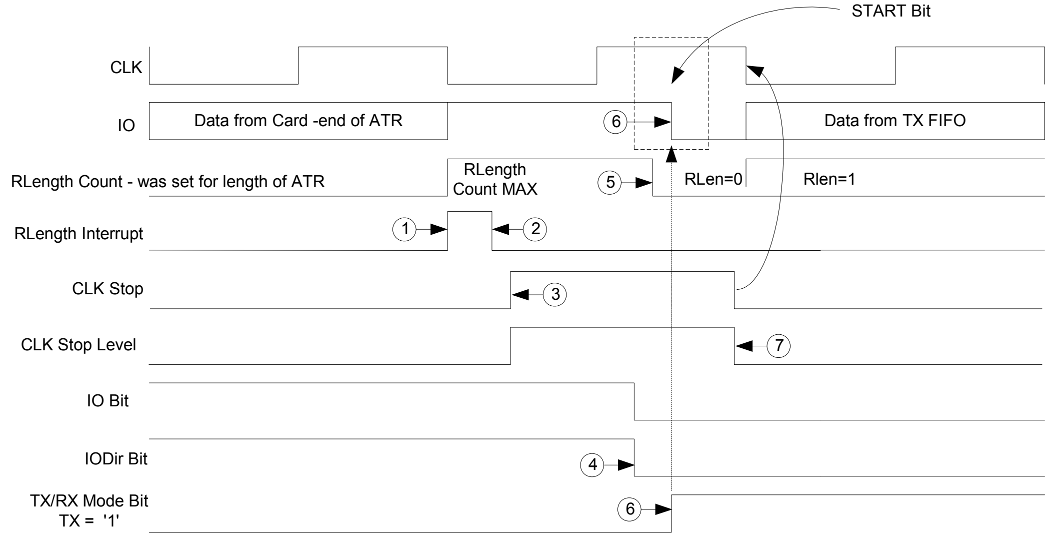
Figure 22: Synchronous Activation



1. Clear CLKOFF after Card is in reception mode
2. Set RST bit
3. Interrupt is generated when Rlength counter is MAX
4. Read and clear Interrupt
5. Clear RST bit
6. Toggle TX/RXB to reset bit counter
7. Reload RLength Counter

t1. CLK wll start 1/2 ETU afer CLKOFF is set low when CLKLVL = 0

Figure 23: Example of Sync Mode operation: Generating/Reading ATR signals

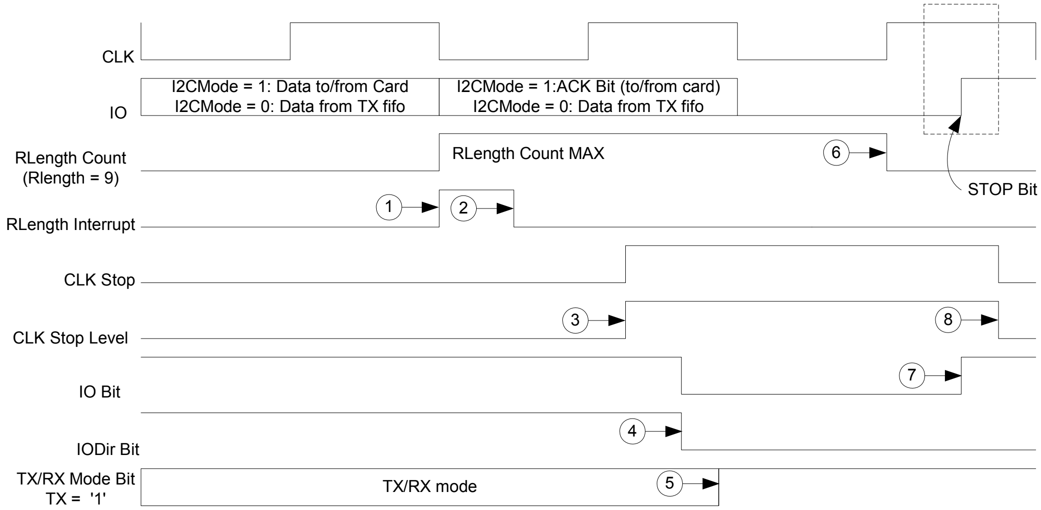


1. Interrupt generated when Rlength counter is MAX
2. Read and clear Interrupt
3. Set CLK Stop and CLK Stop level high in Interrupt routine
4. Set IO Bit low and IODir = Output
5. Reload Rlength Counter
6. Set TX/RX Bit to TX mode. Since Rlen=(MAX or 0) and TX/RX =1, IO pin is controlled by IO bit
7. Clear CLK Stop and CLK Stop level

Note: Data in TX fifo should not be Empty here.

Synchronous Clock Start/Stop Mode style Start bit procedure. This procedure should be used to generate the start bit insertion in Synchronous mode for Synchronous Clock Start/Stop Mode protocol.

Figure 24: Creation of Synchronous Clock Start/Stop Mode Start Bit in Sync Mode



1. Interrupt generated when Rlength counter is MAX
2. Read and clear Interrupt
3. Set CLK Stop and CLK Stop level high
4. Set IO Bit low and IODir = Output
5. Set TX/RX Bit to TX mode.
6. Reload Rlength Counter
7. Set IO Bit High and IODir = Output
8. Clear CLK Stop and CLK Stop level
   Note: Data in TX fifo should not be Empty here.

Synchronous Clock Start/Stop Mode Stop bit procedure. This procedure should be used to generate the Stop bit in Synchronous Mode. SYCKST is bit 7 of STXCTL register.

Figure 25: Creation of Synchronous Clock Start/Stop Mode Stop Bit in Sync Mode

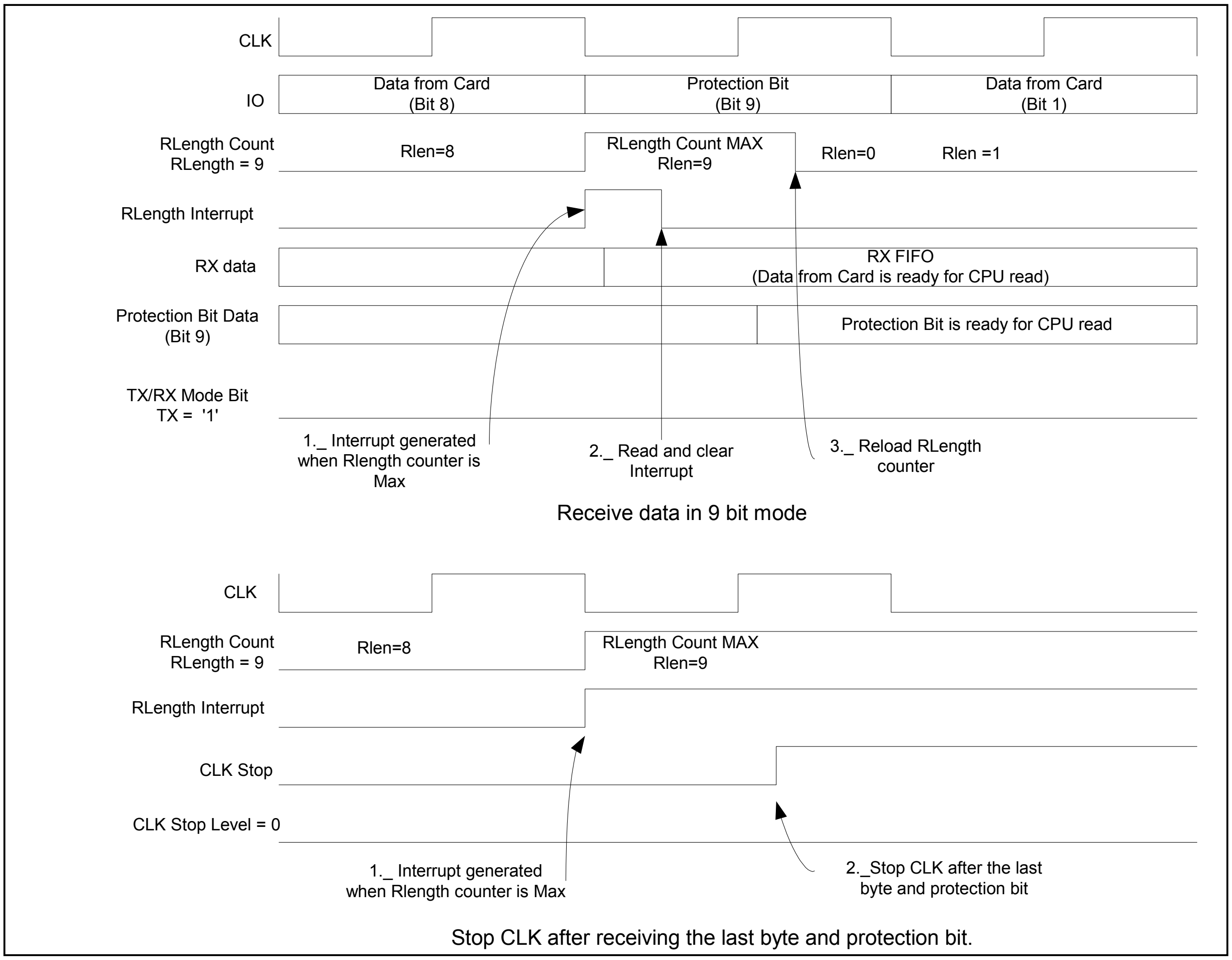

CLK
IO
Data from Card (Bit 8)
Protection Bit (Bit 9)
Data from Card (Bit 1)
RLength Count RLength = 9
Rlen=8
RLength Count MAX Rlen=9
Rlen=0
Rlen =1
RLength Interrupt
RX data
RX FIFO (Data from Card is ready for CPU read)
Protection Bit Data (Bit 9)
Protection Bit is ready for CPU read
TX/RX Mode Bit TX = '1'
1._ Interrupt generated when Rlength counter is Max
2._ Read and clear Interrupt
3._ Reload RLength counter
Receive data in 9 bit mode
CLK
RLength Count RLength = 9
Rlen=8
RLength Count MAX Rlen=9
RLength Interrupt
CLK Stop
CLK Stop Level = 0
1._ Interrupt generated when Rlength counter is Max
2._Stop CLK after the last byte and protection bit
Stop CLK after receiving the last byte and protection bit.

Figure 26: Operation of 9-bit mode in Sync Mode

Smart Card SFRs

Smart Card Select Register (SCSel): 0xFE00 ← 0x00

MSB							LSB
-	-	-	-	SELSC.1	SELSC.0	BYPASS	DIRECT

Table 114: The SCSel Register

The smart card select register is used to determine which smart card interface is using the ISO UART. The internal Smart Card has integrated 7816-3 compliant sequencer circuitry to drive an external smart card interface. The external smart card interface relies on 73S8010 parts to generate the ISO7816-3 compatible signals and sequences. Multiple 73S8010 devices can be connected to the external smart card interface.

Bit	Symbol	Function
SCSel.7	-	
SCSel.6	-	
SCSel.5	-	
SCSel.4	-	
SCSel.3	SELSC.1	Select Smart Card Interface - These bits select the interface that is using the IS0 UART. These bits do not activate the interface. Activation is performed by the VCCCtl register.
SCSel.2	SELSC.0	00 = No smart card interface selected. All de-asserted. 01 = External Smart Card Interface selected (using SCLK, SIO). 1X = Internal Smart Card Interface selected.
SCSel.1	BYPASS	1 = Enabled, 0 = Disabled. When enabled, ISO UART is bypassed and the I/O line is controlled via the SCCtl and SCECtl registers.
SCSel.0	DIRECT	1 = Enabled, 0 = Disabled. When enabled, the PC serial interface directly controls the I/O line for the selected smart card. VCC, RST, C4, C8, CLK are still controlled by the 73S1215F**.**

Table 115: The SCSel Bit Functions.

Smart Card Interrupt Register (SCInt): 0xFE01 ← 0x00

MSB							LSB
WAITTO	CRDEVT	VCCTMRI	RXDAV	TXEVT	TXSENT	TXERR	RXERR

Table 116: The SCInt Register

When the smart card interrupt is asserted, the firmware can read this register to determine the actual cause of the interrupt. The bits are cleared when this register is read. Each interrupt can be disabled by the Smart Card Interrupt Enable register. Error processing must be handled by the firmware. This register relates to the interface that is active – see SCSel register (above).

Bit	Symbol	Function
SCInt.7	WAITTO	Wait Timeout - An ATR or card wait timeout has occurred. In sync mode, this interrupt is asserted when the RLen counter (it advances on falling edges of CLK/ETU) reaches the loaded (max) value. This bit is cleared when the SCINT register is read. When running in Synchronous Clock Stop Mode, this bit becomes RLenINT interrupt (set when the Rlen counter reaches the terminal count).
SCInt.6	CRDEVT	Card Event - A card event is signaled via pin DETCARD either when the Card was inserted or removed (Read Control/Status register to determine card presence) or there was a fault condition in the interface circuitry. This bit is functional even if the smart card logic clock is disabled and when the PWRDN bit is set. This bit is cleared when the SCInt register is read.
SCInt.5	VCCTMRI	VCC Timer - This bit is set when the VCCTMR times out. This bit is cleared when the SCInt register is read.
SCInt.4	RXDAV	Rx Data Available - Data was received from the smart card because the Rx FIFO is not empty. In bypass mode, this interrupt is generated on a falling edge of the smart card I/O line. After receiving this interrupt in bypass mode, firmware should disable it until the firmware has received the entire byte and is waiting for the next start delimiter. This bit is cleared when there is no RX data available in the RX FIFO.
SCInt.3	TXEVNT	TX Event - Set whenever the TXEMTY or TXFULL bits are set in the SRXCtl SFR. This bit is cleared when the STXCtl register is read.
SCInt.2	TXSENT	TX Sent - Set whenever the ISO UART has successfully transmitted a byte to the smart card. Also set when a CRC/LRC byte is sent in T=1 mode. Will not be set in T=0 when a break is detected at the end of a byte (when break detection is enabled). This bit is cleared when the SCInt register is read.
SCInt.1	TXERR	TX Error - An error was detected during the transmission of data to the smart card as indicated by either BREAKD or TXUNDR bit being set in the TXCtl SFR. Additional information can be found in that register description. This bit is cleared when the STXCtl register is read.
SCInt.0	RXERR	RX Error - An error was detected during the reception of data from the smart card. Additional information can be found in the SRXCtl register. This interrupt will be asserted for RXOVRR, or RX Parity error events. This bit is cleared when the SRXCtl register is read.

Table 117: The SCInt Bit Functions.

Smart Card Interrupt Enable Register (SCIE): 0xFE02 ← 0x00

MSB							LSB
WTOIEN	CDEVEN	VTMREN	RXDAEN	TXEVEN	TXSNTEN	TXEREN	RXEREN

Table 118: The SCIE Register

When set to a 1, the respective condition can cause a smart card interrupt. When set to a 0, the respective condition cannot cause an interrupt. When disabled, the respective bit in the Smart Card Interrupt register can still be set, but it will not interrupt the MPU.

Bit	Symbol	Function
SCIE.7	WTOIEN	Wait Timeout Interrupt Enable - Enable for ATR or Wait Timeout Interrupt. In sync mode, function is RLIEN (RLen=max.) interrupt enable.
SCIE.6	CDEVEN	Card Event Interrupt Enable.
SCIE.5	VTMREN	VCC Timer Interrupt Enable.
SCIE.4	RXDAEN	Rx Data Available Interrupt Enable.
SCIE.3	TXEVEN	TX Event Interrupt Enable.
SCInt.2	TXSNTEN	TX Sent Interrupt Enable.
SCIE.1	TXEREN	TX Error Interrupt Enable.
SCIE.0	RXEREN	RX Error Interrupt Enable.

Table 119: The SCIE Bit Functions.

Smart Card V_{CC} Control/Status Register (VccCtl): 0xFE03 ← 0x00

MSB							LSB
VCCSEL.1	VCCSEL.0	VDDFLT	RDYST	VCCOK	-	-	SCPWRDN

Table 120: The VccCtl Register

This register is used to control the power up and power down of the integrated smart card interface. It is used to determine whether to apply 5V, 3V, or 1.8 to the smart card. Perform the voltage selection with one write operation, setting both VCCSEL.1 and VCCSEL.0 bits simultaneously.

Bit	Symbol	Function
VccCtl.7	VCCSEL.1	Setting non-zero value for bits 7,6 will begin activation sequence with target Vcc as given below: State VCCSEL.1 VCCSEL.0 VCC 1 0 0 0V. 2 0 1 1.8V. 3 1 0 3.0V. 4 1 1 5V. A card event or VCCOK going low will initiate a de-activation sequence. When the de-activation sequence for RST, CLK and I/O is complete, V_{CC} will be turned off. When this type of deactivation occurs, the bits must be reset before initiating another activation.
VccCtl.6	VCCSEL.0	
VccCtl.5	VDDFLT	When there is a VDD Fault event, this bit will be set=0. This causes VCCSEL.1 and VCCSEL.0 bits to be immediately set=0 to begin deactivation.
VccCtl.4	RDYST	If this bit is set=1, the activation sequence will start when bit VCCOK is set=1. If not set, the deactivation sequence shall start when the VCCTMR times out.
VccCtl.3	VCCOK	(Read only). Indicates that V_{CC} output voltage is stable.
VccCtl.2	-	
VccCtl.1	-	
VccCtl.0	SCPWRDN	This bit controls the power-down mode of the internal smart card interface circuit. 1 = power down, 0 = normal operation.

Table 121: The VccCtl Bit Functions.

V_{CC} Stable Timer Register (VccTmr): 0xFE04 ← 0x0F

MSB							LSB
OFFTMR.3	OFFTMR.2	OFFTMR.1	OFFTMR.0	VCCTMR.3	VCCTMR.2	VCCTMR.1	VCCTMR.0

Table 122: The VccTmr Register

A programmable timer is provided to set the time from activation start (setting the VCCSEL.1and VCCSEL.0 bits to non-zero) to when VCC_OK is evaluated. VCC_OK must be true at the end of this timers programmed interval (tto in Figure 17: Asynchronous Activation Sequence Timing) in order for the activation sequence to continue. If VCC_OK is not true and the end of the interval (tto), the Card Event interrupt will be set, and a de-activation sequence shall begin including clearing of the VCCSEL bits.

Bit	Symbol	Function
VccTmr.7	OFFTMR.3	VCC Off Timer - The bits set the delay (in number of ETUs) for de-activation after the VCCSEL.1 and VCC SEL.0 have been set to 0. The time value is a count of the 32768Hz clock and is given by tto = OFFTMR(7:4) * 30.5us. This delay does not affect emergency de-activations due to VDD Fault or card events. A value of 0000 results in no additional delay.
VccTmr.6	OFFTMR.2	
VccTmr.5	OFFTMR.1	
VccTmr.4	OFFTMR.0	
VccTmr.3	VCCTMR.3	VCC Timer - VCCOK must be true at the time set by the value in these bits in order for the activation sequence to continue. If not, the VCCSEL bits will be cleared. The time value is a count of the 32768Hz clock and is given by tto = VCCTMR(3:0) * 30.5us. A value of 0000 results in no timeout, not zero time, and activation requires that RDYST is set and RDY goes high.
VccTmr.2	VCCTMR.2	
VccTmr.1	VCCTMR.1	
VccTmr.0	VCCTMR.0	

Table 123: The VccTmr Bit Functions.

Card Status/Control Register (CRDCtl): 0xFE05 ← 0x00

MSB							LSB
DEBOUN	CDETEN	-	-	DETPOL	PUEN	PDEN	CARDIN

Table 124: The CRDCtl Register

This register is used to configure the card detect pin (DETCARD) and monitor card detect status. This register be written to properly configure Debounce, Detect_Polarity (=0 or =1), and the pull-up/down enable before setting CDETEN. The card detect logic is functional even without smart card logic clock. When the PWRDN bit is set=1, no debounce is provided but card presence is operable.

Bit	Symbol	Function
CRDCtl.7	DEBOUN	Debounce - When set = 1, this will enable hardware de-bounce of the card detect pin. The de-bounce function shall wait for 64ms of stable card detect assertion before setting the CARDIN bit. This counter/timer uses the keypad clock as a source of 1kHz signal. De-assertion of the CARDIN bit is immediate upon de-assertion of the card detect pin(s).
CRDCtl.6	CDETEN	Card Detect Enable - When set = 1, activates card detection input. Default upon power-on reset is 0.
CRDCtl.5	-	
CRDCtl.4	-	
CRDCtl.3	DETPOL	Detect Polarity - When set = 1, the DETCARD pin shall interpret a logic 1 as card present.
CRDCtl.2	PUEN	Enable pull-up current on DETCARD pin.
CRDCtl.1	PDEN	Enable pull-down current on DETCARD pin.
CRDCtl.0	CARDIN	Card Inserted - (Read only). 1 = card inserted, 0 = card not inserted. A change in the value of this bit is a “card event.” A read of this bit indicates whether smart card is inserted or not inserted in conjunction with the DETPOL setting.

Table 125: The CRDCtl Bit Functions.

TX Control/Status Register (STXCtl): 0xFE06 ← 0x00

MSB							LSB
SYCKST	-	TXFULL	TXEMTY	TXUNDR	LASTTX	TX/RXB	BREAKD

Table 126: The STXCtl Register

This register is used to control transmission of data to the smart card. Some control and some status bits are in this register.

Bit	Symbol	Function
STXCtl.7	SYCKST	Synchronous Clock Start/Stop Mode - When in sync mode, setting this bit will allow the RLen counter to automatically stop the clock (if CLKSTOP is set) when Rlen reaches its terminal count value. When this bit is set and the RLen count value = max or 0, the source of the smart card data for IO pin (or SIO pin) will be connected to the IO bit in SCCtl (or SCECtl) register rather than the TX FIFO. See the description for the protocol mode control register for more detail.
STXCtl.6	-	
STXCtl.5	TXFULL	TX FIFO is full. Additional writes may corrupt the contents of the FIFO. This bit it will remain set as long as the TX FIFO is full. Generates TX_Event interrupt upon going full.
STXCtl.4	TXEMTY	1 = TX FIFO is empty, 0 = TX FIFO is not empty. If there is data in the TX FIFO, the circuit will transmit it to the smart card if in transmit mode. In T=1 mode, if the LASTTX bit is set and the hardware is configured to transmit the CRC/LRC, the TXEMTY will not be set until the CRC/LRC is transmitted. In T=0, if the LASTTX bit is set, TXEMTY will be set after the last word has been successfully transmitted to the smart card. Generates TXEVNT interrupt upon going empty.
STXCtl.3	TXUNDR	TX Underrrun - (Read only) Asserted when a transmit under-run condition has occurred. An under-run condition is defined as an empty TX FIFO when the last data word has been successfully transmitted to the smart card and the LASTTX bit was not set. No special processing is performed by the hardware if this condition occurs. Cleared when read by firmware. This bit generates TXERR interrupt.
STXCtl.2	LASTTX	Last TX Byte - Set by firmware (in both T=0 and T=1) when the last byte in the current message has been written into the transmit FIFO. In T=1 mode, the CRC/LRC will be appended to the message. Should be set after the last byte has been written into the transmit FIFO. Should be cleared by firmware before writing first byte of next message into the transmit FIFO. Used in T=0 to determine when to set TXEMTY.
STXCtl.1	TX/RXB	1 = Transmit mode, 0 =Receive mode. Configures the hardware to be receiving from or transmitting to the smart card. Determines which counters should be enabled. This bit should be set to receive mode prior to switching to another interface. Setting and resetting this bit shall initialize the CRC logic. If LASTTX is set, this bit can be reset to RX mode and UART logic will automatically change mode to RX when TX operation is completed (TX_Empty =1).
STXCtl.0	BREAKD	Break Detected - (Read only) 1 = A break has been detected on the I/O line indicating that the smart card detected a parity error. Cleared when read. This bit generates TXERR interrupt.

Table 127: The STXCtl Bit Functions.

STX Data Register (STXData): 0xFE07 🡐 0x00

MSB LSB

STXDAT. 7	STXDAT. 6	STXDAT. 5	STXDAT. 4	STXDAT. 3	STXDAT. 2	STXDAT. 1	STXDAT. 0

Table 128: The STXData Register

Bit	Function
STXData.7	Data to be transmitted to smart card. Gets stored in the TX FIFO and then extracted by the hardware and sent to the selected smart card. When the MPU reads this register, the byte pointer is changed to effectively "read out" the data. Thus, two reads will always result in an "empty" FIFO condition. The contents of the FIFO registers are not cleared, but will be overwritten by writes.
STXData.6	
STXData.5	
STXData.4	
STXData.3	
STXData.2	
STXData.1	
STXData.0	

Table 129: The STXCtl Bit Functions.

RX Control/Status Register (SRXCtl): 0xFE08 🡐 0x00

MSB LSB

BIT9DAT	-	LASTRX	CRCERR	RXFULL	RXEMTY	RXOVRR	PARITYE

Table 130: The SRXCtl Register

This register is used to monitor reception of data from the smart card.

Bit	Symbol	Function
SRXCtl.7	BIT9DAT	Bit 9 Data - When in sync mode and with MODE9/8B set, this bit will contain the data on IO (or SIO) pin that was sampled on the ninth CLK (or SCLK) rising edge. This is used to read data in synchronous 9-bit formats.
SRXCtl.6	-	
SRXCtl.5	LASTRX	Last RX Byte - User sets this bit during the reception of the last byte. When byte is received and this bit is set, logic checks CRC to match 0x1D0F (T=1 mode) or LRC to match 00h (T=1 mode), otherwise a CRC or LRC error is asserted.
SRXCtl.4	CRCERR	(Read only) 1 = CRC (or LRC) error has been detected.
SRXCtl.3	RXFULL	(Read only) RX FIFO is full. Status bit to indicate RX FIFO is full.
SRXCtl.2	RXEMTY	(Read only) RX FIFO is empty. This is only a status bit and does not generate a RX interrupt.
SRXCtl.1	RXOVRR	RX Overrun - (Read Only) Asserted when a receive-over-run condition has occurred. An over-run is defined as a byte was received from the smart card when the RX FIFO was full. Invalid data may be in the receive FIFO. Firmware should take appropriate action. Cleared when read. Additional writes to the RX FIFO are discarded when a RXOVRR occurs until the overrun condition is cleared. Will generate RXERR interrupt.
SRXCtl.0	PARITYE	Parity Error - (Read only) 1 = The logic detected a parity error on incoming data from the smart card. Cleared when read. Will generate RXERR interrupt.

Table 131: The STXCtl Bit Functions.

SRX Data Register (SRXData): 0xFE09 ← 0x00

MSB							LSB
SRXDAT.7	SRXDAT.6	SRXDAT.5	SRXDAT.4	SRXDAT.3	SRXDAT.2	SRXDAT.1	SRXDAT.0

Table 132: The SRXData Register

Bit	Function
SRXData.7	(Read only) Data received from the smart card. Data received from the smart card gets stored in a FIFO that is read by the firmware.
SRXData.6	
SRXData.5	
SRXData.4	
SRXData.3	
SRXData.2	
SRXData.1	
SRXData.0	

Table 133: The STXCtl Bit Functions.

Smart Card Control Register (SCCtl): 0xFE0A ← 0x21

MSB							LSB
RSTCRD	-	IO	IOD	C8	C4	CLKLVL	CLKOFF

Table 134: The SCCtl Register

This register is used to monitor reception of data from the smart card.

Bit	Symbol	Function
SCCtl.7	RSTCRD	1 = Asserts the RST (set RST = 0) to the smart card interface, 0 = De-assert the RST (set RST = 1) to the smart card interface. Can be used to extend RST to the smart card. Refer to RLength register description. This bit is operational in all modes and can be used to extend RST during activation or perform a “Warm Reset” as required. In auto-sequence mode, this bit should be set=0 to allow the sequencer to de-assert RST per the RLength parameters. In sync mode (see SPrtcol register) the sense of this bit is non-inverted, if set=1, RST=1, if set=0, RST=0. Rlen has no effect on Reset in sync mode.
SCCtl.6	-	
SCCtl.5	IO	Smart Card I/O. Read is state of I/O signal (Caution, this signal is not synchronized to the MPU clock). In Bypass mode, write value is state of signal on I/O. In sync mode, this bit will contain the value of I/O pin on the latest rising edge of CLK.
SCCtl.4	IOD	Smart Card I/O Direction control Bypass mode or sync mode. 1 = input (default), 0 = output.
SCCtl.3	C8	Smart Card C8. When C8 is an output, the value written to this bit will appear on the C8 line. The value read when C8 is an output is the value stored in the register. When C8 is an input, the value read is the value on the C8 pin (Caution, this signal is not synchronized to the MPU clock). When C8 is an input, the value written will be stored in the register but not presented to the C8 pin.
SCCtl.2	C4	Smart Card C4. When C4 is an output, the value written to this bit will appear on the C4 line. The value read when C4 is an output is the value stored in the register. When C4 is an input, the value read is the value on the C4 pin (Caution, this signal is not synchronized to the MPU clock). When C4 is an input, the value written will be stored in the register but not presented to the C4 pin.
SCCtl.1	CLKLVL	1 = High, 0 = Low. If CLKOFF is set = 1, the CLK to smart card will be at the logic level indicated by this bit. If in bypass mode, this bit directly controls the state of CLK.
SCCtl.0	CLKOFF	0 = CLK is enabled. 1 = CLK is not enabled. When asserted, the CLK will stop at the level selected by CLKLVL. This bit has no effect if in bypass mode.

Table 135: The SCCtl Bit Functions.

External Smart Card Control Register (SCECtl): 0xFE0B ← 0x00

MSB							LSB
-	-	SIO	SIOD	-	-	SCLKLVL	SCLKOFF

Table 136: The SCECtl Register

Used to directly set and sample signals of External Smart Card interface. There are three modes of asynchronous operation, an “automatic sequence” mode, the direct mode, and bypass mode. Clock stop per the ISO 7816-3 interface is also supported but firmware must handle the protocol for SIO and SCLK for I^{2}C clock stop and start. Control for Reset (to make RST signal), activation control, voltage select, etc. should be handled via the I^{2}C interface when using external 72S8010 devices. USR(n) pins shall be used for C4, C8 functions if necessary.

Bit	Symbol	Function
SCECtl.7	-	
SCECtl.6	-	
SCECtl.5	SIO	External Smart Card I/O. Bit when read indicates state of pin SIO for SIOD=1 (Caution, this signal is not synchronized to the MPU clock), when written, sets state of pin SIO for SIOD=0. Ignored if not in bypass or sync modes. In sync mode, this bit will contain the value of IO pin on the latest rising edge of SCLK.
SCECtl.4	SIOD	1 = input, 0 = output. External Smart Card I/O Direction control. Ignored if not in bypass or sync modes.
SCECtl.3	-	
SCECtl.2	-	
SCECtl.1	SCLKLVL	Sets the state of SCLK when disabled by SCLKOFF bit. If in bypass mode, this bit directly controls the state of SCLK.
SCECtl.0	SCLKOFF	0 = SCLK enabled, 1 = SCLK disabled. When disabled, SCLK level is determined by SCLKLVL. This bit has no effect if in bypass mode.

Table 137: The SCECtl Bit Functions.

C4/C8 Data Direction Register (SCDIR): 0xFE0C ← 0x00

MSB							LSB
-	-	-	-	C8D	C4D	-	-

Table 138: The SCDIR Register

This register determines the direction of the internal interface C4/C8 lines. After reset, all signals are tri-stated.

Bit	Symbol	Function
SCDIR.7	-	
SCDIR.6	-	
SCDIR.5	-	
SCDIR.4	-	
SCDIR.3	C8D	1 = input, 0 = output. Smart Card C8 direction.
SCDIR.2	C4D	1 = input, 0 = output. Smart Card C4 direction.
SCDIR.1	-	
SCDIR.0	-	

Table 139: The SCDIR Bit Functions.

Protocol Mode Register (SPrtcol): 0xFE0D ← 0x03

MSB LSB

SCISYN	MOD9/8B	SCESYN	0	TMODE	CRCEN	CRCMS	RCVATR

Table 140: The SPrtcol Register

This register determines the protocol to be use when communicating with the selected smart card. This register should be updated as required when switching between smart card interfaces.

Bit	Symbol	Function
SPrtcol.7	SCISYN	Smart Card Internal Synchronous mode - Configures internal smart card interface for synchronous mode. This mode routes the internal interface buffers for RST, IO, C4, C8 to SCCtl register bits for direct firmware control. CLK is generated by the ETU counter.
SPrtcol.6	MOD9/8B	Synchronous 8/9 bit mode select - For sync mode, in protocols with 9 bit words, set this bit. The first eight bits read go into the RX FIFO and the ninth bit read will be stored in the IO (or SIO) data bit of the SRXCtl register.
SPrtcol.5	SCESYN	Smart Card External Synchronous mode - Configures External Smart Card interface for synchronous mode. This mode routes the external smart card interface buffers for SIO to SCECtl register bits for direct firmware control. SCLK is generated by the ETU counter.
SPrtcol.4	0	Reserved bit, must always be set to 0.
SPrtcol.3	TMODE	Protocol mode select - 0: T=0, 1: T=1. Determines which smart card protocol is to be used during message processing.
SPrtcol.2	CRCEN	CRC Enable - 1 = Enabled, 0 = Disabled. Enables the checking/generation of CRC/LRC while in T=1 mode. Has no effect in T=0 mode. If enabled and a message is being transmitted to the smart card, the CRC/LRC will be inserted into the message stream after the last TX byte is transmitted to the smart card. If enabled, CRC/LRC will be checked on incoming messages and the value made available to the firmware via the CRC LS/MS registers.
SPrtcol.1	CRCMS	CRC Mode Select - 1 = CRC, 0 = LRC. Determines type of checking algorithm to be used.
SPrtcol.0	RCVATR	Receive ATR - 1 = Enable ATR timeout, 0 = Disable ATR timeout. Set by firmware after the smart card has been turned on and the hardware is expecting ATR.

Table 141: The SPrtcol Bit Functions.

SC Clock Configuration Register (SCCLK): 0xFE0F ← 0x0C

MSB LSB

-	-	ICLKFS.5	ICLKFS.4	ICLKFS.3	ICLKFS.2	ICLKFS.1	ICLKFS.0

Table 142: The SCCLK Register

This register controls the internal smart card (CLK) clock generation.

Bit	Symbol	Function
SCCLK.7	-	
SCCLK.6	-	
SCCLK.5	ICLKFS.5	Internal Smart Card CLK Frequency Select - Division factor to determine internal smart card CLK frequency. MCLK clock is divided by (register value + 1) to clock the ETU divider, and then by 2 to generate CLK. Default ratio is 13. The programmed value in this register is applied to the divider after this value is written, in such a manner as to produce a glitch-free output, regardless of the selection of active interface. A register value = 0 will default to the same effect as register value = 1.
SCCLK.4	ICLKFS.4	
SCCLK.3	ICLKFS.3	
SCCLK.2	ICLKFS.2	
SCCLK.1	ICLKFS.1	
SCCLK.0	ICLKFS.0	

Table 143: The SCCLK Bit Functions.

External SC Clock Configuration Register (SCSCLK): 0xFE10 ← 0x0C

MSB LSB

-	-	ECLKFS.5	ECLKFS.4	ECLKFS.3	ECLKFS.2	ECLKFS.1	ECLKFS.0

Table 144: The SCSCLK Register

This register controls the external smart card (SCLK) clock generation.

Bit	Symbol	Function
SCSCLK.7	-	
SCSCLK.6	-	
SCSCLK.5	ECLKFS.5	External Smart Card CLK Frequency Select - Division factor to determine external smart card CLK frequency. MCLK clock is divided by (register value + 1) to clock the ETU divider, and then by 2 to generate SCLK. Default ratio is 13. The programmed value in this register is applied to the divider after this value is written, in such a manner as to produce a glitch-free output, regardless of the selection of active interface. A register value = 0 will default to the same effect as register value = 1.
SCSCLK.4	ECLKFS.4	
SCSCLK.3	ECLKFS.3	
SCSCLK.2	ECLKFS.2	
SCSCLK.1	ECLKFS.1	
SCSCLK.0	ECLKFS.0	

Table 145: The SCSCLK Bit Functions.

Parity Control Register (SParCtl): 0xFE11 ← 0x00

MSB LSB

-	DISPAR	BRKGEN	BRKDET	RETRAN	DISCRX	INSPE	FORCPE

Table 146: The SParCtl Register

This register provides the ability to configure the parity circuitry on the smart card interface. The settings apply to both integrated smart card interfaces.

Bit	Symbol	Function
SParCtl.7	-	
SParCtl.6	DISPAR	Disable Parity Check - 1 = disabled, 0 = enabled. If enabled, the UART will check for even parity (the number of 1's including the parity bit is even) on every character. This also applies to the TS during ATR.
SParCtl.5	BRKGEN	Break Generation Disable - 1 = disabled, 0 = enabled. If enabled, and T=0 protocol, the UART will generate a Break to the smart card if a parity error is detected on a receive character. No Break will be generated if parity checking is disabled. This also applies to TS during ATR.
SParCtl.4	BRKDET	Break Detection Disable - 1 = disabled, 0 = enabled. If enabled, and T=0 protocol, the UART will detect the generation of a Break by the smart card.
SParCtl.3	RETRAN	Retransmit Byte - 1 = enabled, 0 = disabled. If enabled and a Break is detected from the smart card (Break Detection must be enabled), the last character will be transmitted again. This bit applies to T=0 protocol.
SParCtl.2	DISCRX	Discard Received Byte - 1 = enabled, 0 = disabled. If enabled and a parity error is detected (Parity checking must be enabled), the last character received will be discarded. This bit applies to T=0 protocol.
SParCtl.1	INSPE	Insert Parity Error - 1 = enabled, 0 = disabled. Used for test purposes. If enabled, the UART will insert a parity error in every character transmitted by generating odd parity instead of even parity for the character.
SParCtl.0	FORCPE	Force Parity Error - 1 = enabled, 0 = disabled. Used for test purposes. If enabled, the UART will generate a parity error on a character received from the smart card.

Table 147: The SCECtl Bit Functions.

Byte Control Register (SByteCtl): 0xFE12 ← 0x2C

MSB LSB

-	DETTS	DIRTS	BRKDUR.1	BRKDUR.0	-	-	-

Table 148: The SByteCtl Register

This register controls the processing of characters and the detection of the TS byte. When receiving, a Break is asserted at 10.5 ETU after the beginning of the start bit. Break from the card is sampled at 11 ETU.

Bit	Symbol	Function
SByteCtl.7	-	
SByteCtl.6	DETTS	Detect TS Byte - 1 = Next Byte is TS, 0 = Next byte is not TS. When set, the hardware will treat the next character received as the TS and determine if direct or indirect convention is being used. Direct convention is the default used if firmware does not set this bit prior to transmission of TS by the smart card to the firmware. The hardware will check parity and generate a break as defined by the DISPAR and BRKGEN bits in the parity control register. This bit is cleared by hardware after TS is received. TS is decoded prior to the FIFO and is stored in the receive FIFO.
SByteCtl.5	DIRTS	Direct Mode TS Select - 1 = direct mode, 0 = indirect mode. Set/cleared by hardware when TS is processed indicating either direct/indirect mode of operation. When switching between smart cards, the firmware should write the bit appropriately since this register is not unique to an individual smart card (firmware should keep track of this bit).
SByteCtl.4	BRKDUR.1	Break Duration Select - 00 = 1 ETU, 01 = 1.5 ETU, 10 = 2 ETU, 11 = reserved. Determines the length of a Break signal which is generated when detecting a parity error on a character reception in T=0 mode.
SByteCtl.3	BRKDUR.0	
SByteCtl.2	-	
SByteCtl.1	-	
SByteCtl.0	-	

Table 149: The SByteCtl Bit Functions.

FD Control Register (FDReg): 0xFE13 ← 0x11

MSB							LSB
FVAL.3	FVAL.2	FVAL.1	FVAL.0	DVAL.3	DVAL.2	DVAL.1	DVAL.0

Table 150: The FDReg Register

This register uses the transmission factors F and D to set the ETU (baud) rate. The values in this register are mapped to the ISO 7816 conversion factors as described below. The CLK signal for each interface is created by dividing a high-frequency, intermediate signal (MSCLK) by 2. The ETU baud rate is created by dividing MSCLK by 2 times the Fi/Di ratio specified by the codes below. For example, if FI = 0001 and DI = 0001, the ratio of Fi/Di is 372/1. Thus the ETU divider is configured to divide by 2 * 372 = 744. The maximum supported F/D ratio is 4096.

FI (code)	0000	0001	0010	0011	0100	0101	0110	0111
Fi (ratio)	372	372	558	744	1116	1488	1860	1860⊕
FCLK max	4	5	6	8	12	16	20	20⊕

FI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Fi(ratio)	512⊕	512	768	1024	1536	2048	2048⊕	2048⊕
FCLK max	5⊕	5	7.5	10	15	20	20⊕	20⊕

DI(code)	0000	0001	0010	0011	0100	0101	0110	0111
Di(ratio)	1⊕	1	2	4	8	16	32	32⊕

DI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Di(ratio)	12	20	16⊕	16⊕	16⊕	16⊕	16⊕	16⊕

Note: values marked with ⊕ are not included in the ISO definition and arbitrary values have been assigned.

Table 151 Divider ratios provided by the ETU counter

The values given below are used by the ETU divider to create the ETU clock. The entries that are not shaded will result in precise CLK/ETU per ISO requirements. Shaded areas are not precise but are within 1% of the target value.

	Fi code	0000	0001	0010	0011	0100	0101
Di code	F→ D↓	372	372	558	744	1116	1488
0001	1	744	744	1116	1488	2232	2976
0010	2	372	372	558	744	1116	1488
0011	4	186	186	279	372	558	744
0100	8	93	93	138	186	279	372
1000	12	62	62	93	124	186	248
0101	16	47	47	70	93	140	186
1001	20	37	37	56	74	112	149
0110	32	23	23	35	47	70	93

	Fi code	0110	1001	1010	1011	1100	1101
Di code	F→ D↓	1860	512	768	1024	1536	2048
0001	1	3720	1024	1536	2048	3072	4096
0010	2	1860	512	768	1024	1536	2048
0011	4	930	256	384	512	768	1024
0100	8	465	128	192	256	384	512
1000	12	310	85	128	171	256	341
0101	16	233	64	96	128	192	256
1001	20	186	51	77	102	154	205
0110	32	116	32	48	64	96	128

Table 152 Divider values for the ETU clock

Bit	Symbol	Function
FDReg.7	FVAL.3	Refer to the Table 152 above. This value is converted per the table to set the divide ratio used to generate the baud rate (ETU). Default, also used for ATR, is 0001 (Fi=372). This value is used by the selected interface.
FDReg.6	FVAL.2	
FDReg.5	FVAL.1	
FDReg.4	FVAL.0	
FDReg.3	DVAL.3	Refer to Table 152 above. This value is used to set the divide ratio used to generate the smart card CLK. Default, also used for ATR, is 0001 (Di=1).
FDReg.2	DVAL.2	
FDReg.1	DVAL.1	
FDReg.0	DVAL.0	

Table 153: The FDReg Bit Functions.

CRC MS Value Registers (CRCMsB): 0xFE14 ← 0xFF, (CRCLsB): 0xFE15 ← 0xFF

MSB							LSB
CRC.15	CRC.14	CRC.13	CRC.12	CRC.11	CRC.10	CRC.9	CRC.8

Table 154: The CRCMsB Register

MSB							LSB
CRC.7	CRC.6	CRC.5	CRC.4	CRC.3	CRC.2	CRC.1	CRC.0

Table 155: The CRCLsB Register

The 16-bit CRC value forms the TX CRC word in TX mode (write value) and the RX CRC in RX mode (read value). The initial value of CRC to be used when generating a CRC to be transmitted at the end of a message (after the last TX byte is sent) when enabled in T=1 mode. Should be reloaded at the beginning of every message to be transmitted. When using CRC, the both CRC registers should be initialized to FF. When using LRC the CRCLsB Value register should be loaded to 00. When receiving a message, the firmware should load this with the initial value and then read this register to get the final value at the end of the message. These registers need to be reloaded for each new message to be received. When in LRC mode, bits (7:0) are used and bits (15:8) are undefined. During LRC/CRC checking and generation, this register is updated with the current value and can be read to aid in debugging. This information will be transmitted to the smart card using the timing specified by the Guard Time register. When checking CRC/LRC on an incoming message (CRC/LRC is checked against the data and CRC/LRC), the firmware reads the final value after the message has been received and determines if an error occurred (= 0x1D0F (CRC_ no error, else error; =0 (LRC) no error, else error). When a message is received, the CRC/LRC is stored in the FIFO. The polynomial used to generate and check CRC is $x^{16} + x^{12} + x^{5} + 1$. When in indirect convention, the CRC is generated prior to the conversion into indirect convention. When in indirect convention, the CRC is checked after the conversion out of indirect convention. For a given message, the CRC generated (and readable from this register) will be the same whether indirect or direct convention is used to transmit the data to the smart card. The CRCLsB / CRCMsB registers will be updated with CRC/LRC whenever bits are being received or transmitted from/to the smart card (even if CRCEN is not set and in mode T1). They are available to the firmware to use if desired.

Block Guard Time Register (BGT): 0xFE16 ← 0x10

MSB							LSB
EGT.8	-	-	-	BGT.3	BGT.1	BGT.2	BGT.0

Table 156: The BGT Register

This register contains the Extra Guard Time Value (EGT) most-significant bit. The Extra Guard Time indicates the minimum time between the leading edges of the start bit of consecutive characters. The delay is depends on the T=0/T=1 mode. Used in transmit mode. This register also contains the Block Guard Time (BGT) value. Block Guard Time is the minimum time between the leading edge of the start bit of the last character received and the leading edge of the start bit of the first character transmitted. This should not be set less than the character length. The transmission of the first character will be held off until BGT has elapsed regardless of the TX data and TX/RX control bit timing.

Bit	Symbol	Function
BGT.7	EGT.8	Most significant bit for 9-bit EGT timer. See EGT below.
BGT.6	-	
BGT.5	-	
BGT.4	-	
BGT.3	BGT.3	Time in ETUs between the start bit of the last received character to start bit of the first character transmitted to the smart card. Default value is 22.
BGT.2	BGT.2	
BGT.1	BGT.1	
BGT.0	BGT.0	

Table 157: The BGT Bit Functions.

Extra Guard Time Register (EGT): 0xFE16 ← 0x10

MSB							LSB
EGT.7	EGT.6	EGT.5	EGT.4	EGT.3	EGT.1	EGT.2	EGT.0

Table 158: The EGT Register

This register contains the Extra Guard Time Value (EGT) least-significant byte. The Extra Guard Time indicates the minimum time between the leading edges of the start bit of consecutive characters. The delay is depends on the T=0/T=1 mode. Used in transmit mode

Bit	Function
EGT.7	Time in ETUs between start bits of consecutive characters. In T=0 mode, the minimum is 1. In T=0, the leading edge of the next start bit may be delayed if there is a break detected from the smart card. Default value is 12. In T=0 mode, regardless of the value loaded, the minimum value is 12, and for T=1 mode, the minimum value is 11.
EGT.6	
EGT.5	
EGT.4	
EGT.3	
EGT.2	
EGT.1	
EGT.0	

Table 159: The EGT Bit Functions.

Block Wait Time Registers (BWTB0): 0xFE1B ← 0x00, (BWTB1): 0xFE1A ← 0x00, (BWTB2): 0xFE19 ← 0x00, (BWTB3): 0xFE18 ← 0x00

MSB							LSB
BWT.7	BWT.6	BWT.5	BWT.4	BWT.3	BWT.1	BWT.2	BWT.0

Table 160: The BWTB0Register

MSB							LSB
BWT.15	BWT.14	BWT.13	BWT.12	BWT.11	BWT.10	BWT.9	BWT.8

Table 161: The BWTB1Register

MSB							LSB
BWT.23	BWT.22	BWT.21	BWT.20	BWT.19	BWT.18	BWT.17	BWT.16

Table 162: The BWTB2Register

MSB							LSB
-	-	-	-	BWT.27	BWT.26	BWT.25	BWT.24

Table 163: The BWTB3Register

These registers (BWTB0, BWTB1, BWTB2, BWTB3) are used to set the Block Waiting Time(27:0) (BWT). All of these parameters define the maximum time the 73S1215F will have to wait for a character from the smart card. These registers serve a dual purpose. When T = 1, these registers are used to set up the block wait time. The block wait time defines the time in ETUs between the beginning of the last character sent to smart card and the start bit of the first character received from smart card. It can be used to detect an unresponsive card and should be loaded by firmware prior to writing the last TX byte. When T = 0, these registers are used to set up the work wait time. The work wait time is defined as the time between the leading edge of two consecutive characters being sent to or from the card. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action. A Wait Time Extension (WTX) is supported with the 28 bit BWT.

Character Wait Time Registers (CWTB0): 0xFE1D ← 0x00, (CWTB1): 0xFE1C ← 0x00

MSB LSB

CWT.7	CWT.6	CWT.5	CWT.4	CWT.3	CWT.1	CWT.2	CWT.0

Table 164: The CWTB0Register

MSB LSB

CWT.15	CWT.14	CWT.13	CWT.12	CWT.11	CWT.10	CWT.9	CWT.8

Table 165: The CWTB1Register

These registers (CWTB0, CWTB1) are used to hold the Character Wait Time(15:0) (CWT) or Initial Waiting Time(15:0) (IWT) depending on the situation. Both the IWT and the CWT measure the time in ETUs between the leading edge of the start of the current character received from the smart card and the leading edge of the start of the next character received from the smart card. The only difference is the mode in which the card is operating. When T=1 these registers are used to configure the CWT and these registers configure the IWT when the ATR is being received. These registers should be loaded prior to receiving characters from the smart card. Firmware must manage which time is stored in the register. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action.

ATR Timeout Registers (ATRLsB): 0xFE20 ← 0x00, (ATRMsB): 0xFE21 ← 0x00

MSB LSB

ATRTO.7	ATRTO.6	ATRTO.5	ATRTO.4	ATRTO.3	ATRTO.1	ATRTO.2	ATRTO.0

Table 166: The ATRLsB Register

MSB LSB

ATRTO.15	ATRTO.14	ATRTO.13	ATRTO.12	ATRTO.11	ATRTO.10	ATRTO.9	ATRTO.8

Table 167: The ATRMsB Register

These registers (ATRLsB & ATRLsB) form the ATR timeout (ATRTO [15:0]) parameter. Time in ETU between the leading edge of the first character and leading edge of the last character of the ATR response. Timer is enabled when the RCVATR is set and starts when leading edge of the first start bit is received and disabled when the RCVATR is cleared. An ATR timeout is generated if this time is exceeded.

TS Timeout Register (STSTO): 0xFE21 ← 0x00

MSB LSB

TST0.7	TST0.6	TST0.5	TST0.4	TST0.3	TST0.1	TST0.2	TST0.0

Table 168: The STSTO Register

The TS timeout is the time in ETU between the de-assertion of smart card reset and the leading edge of the TS character in the ATR (when DETTS is set). The timer is started when smart card reset is de-asserted. An ATR timeout is generated if this time is exceeded (MUTE card).

Reset Time Register (RLength): 0xFE22 🡐 0x70

MSB LSB

RLen.7	RLen.6	RLen.5	RLen.4	RLen.3	RLen.1	RLen.2	RLen.0

Table 169: The RLength Register

Time in ETUs that the hardware delays the de-assertion of RST. If set to zero and RSTCRD=0, the hardware adds no extra delay and the hardware will release RST after VCCOK is asserted during power-up. If set to one, it will delay the release of RST by the time in this register. When the firmware sets the RSTCRD bit, the hardware will assert reset (RST = 0 on pin). When firmware clears the bit, the hardware will release RST after the delay specified in Rlen. If firmware sets the RSTCRD bit prior to instructing the power to be applied to the smart card, the hardware will not release RST after power-up until RLen after the firmware clears the RSTCRD bit. This provides a means to power up the smart card and hold it in reset until the firmware wants to release the RST to the selected smart card. Works with the selected smart card interface.

Shaded locations indicate functions not provided in sync mode.

Name	Address	b7	b6	b5	b4	b3	b2	b1	b0
SCSel	FE00					SelSC(1:0)		BYPASS	DIRECT
SCInt	FE01	WAITTO/ RLIEN	CRDEVT	VCCTMR	RXDAVI	TXEVNT	TXSENT	TXERR	RXERR
SCIE	FE02	WTOI/ RLIEN	CDEVNT	VTMREN	RXDAEN	TXEVEN	TXSNTEN	TXERR	RXERR
VccCtl	FE03	VCCSEL.1	VCCSEL.0	VDDFLT	RDYST	VCCOK			SCPWRDN
VCCtmr	FE04	OFFTMR(3:0)				VCCTMR(3:0)			
CRDCtl	FE05	DEBOUN	CDETEN			DETPOL	PUEN	PDEN	CARDIN
STXCtl	FE06	SYCKST		TXFULL	TXEMTY	TXUNDR	LASTTX	TX/RXB	BREAKD
STXData	FE07	TXDATA(7:0)							
SRXCtl	FE08	BIT9DAT		LASTRX	CRCERR	RXFULL	RXEMTY	RXOVRR	PARITYE
SRXData	FE09	RXDATA(7:0)							
SCCtl	FE0A	RSTCRD		IO	IOD	C8	C4	CLKLVL	CLKOFF
SCECtl	FE0B			SIO	SIOD			SCLKLVL	SCLKOFF
SCDIR	FE0C					C8D	C4D		
SCPrtcol	FE0D	SCISYN	MOD9/8B	SCESYN	0	TMODE	CRCEN	CRCMS	RCVATR
SCCLK	FE0F			ICLKFS(5:0)					
SCSCLK	FE10			ECLKFS(5:0)					
SParCtl	FE11		DISPAR	BRKGEN	BRKDET	RTRAN	DISCRX	INSPE	FORCPE
SByteCtl	FE12		DETTS	DIRTS	BRKDUR (1:0)				
FDReg	FE13	FVAL(3:0)				DVAL (3:0)			
CRCMsB	FE14	CRC(15:8)							
CRCLsB	FE15	CRC(7:0)							
BGT	FE16	EGT8				BGT(4:0)			

Name	Address	b7	b6	b5	b4	b3	b2	b1	b0
EGT	FE17	EGT(7:0)							
BBWT3	FE18					BWT(27:24)			
BWTB2	FE19	BWT(23:16)							
BWTB1	FE1A	BWT(15:8)							
BWTB0	FE1B	BWT(7:0)							
CWTB1	FE1C	CWT(15:8)							
CWTB0	FE1D	CWT(7:0)							
ATRMsB	FE1F	ATRTO(15:8)							
ATRLsB	FE20	ATRTO(7:0)							
STSTO	FE21	TSTO(7:0)							
RLength	FE22	RLen(7:0)							

Table 170: Smart Card Timing Definitions

ELECTRICAL SPECIFICATION

Absolute Maximum Ratings

Operation outside these rating limits may cause permanent damage to the device. The smart card interface pins are protected against short circuits to V_{CC}, ground, and each other.

PARAMETER	RATING
DC Supply voltage, V_{DD}	-0.5 to 4.0 VDC
Supply Voltage V_{PC}	-0.5 to 6.5 VDC
Storage Temperature	-60 to 150°C
Pin Voltage (except card interface)	-0.3 to (V_{DD}+0.5) VDC
Pin Voltage (card interface)	-0.3 to (V_{CC}+0.5) VDC
ESD tolerance (except card interface)	+/- 2KV
ESD tolerance (card interface)	+/- 6KV
Pin Current	± 200 mA

Note: ESD testing on smart card pins is HBM condition, 3 pulses, each polarity referenced to ground.
Note: Smart Card pins are protected against shorts between any combinations of Smart Card pins.

Recommended operating conditions

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges:

PARAMETER	RATING
DC Voltage Supply VDD	2.7 to 3.6 VDC
DC Voltage Supply VDD for USB operation	3.0 to 3.6 VDC
Supply Voltage V_{PC} for Class A-B-C Reader	4.75 to 6.0 VDC
Ambient Operating Temperature (Ta)	-40°C to +85°C

Digital IO Characteristics

These requirements pertain to digital I/O pin types with consideration of the specific pin function and configuration. The LED(3:0) pins have pull-ups that may be enabled. The Row pins have 100Kohm pull-ups.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	UNIT
Voh	Output level, high	Ioh =-2mA	0.8 *VDD		VDD	V
Vol	Output level, low	Iol=2mA	0		0.3	V
Vih	Input voltage, high	2.7v < VDD <3.6v	1.8		VDD +0.3	V
Vil	Input voltage, low	2.7v < VDD <3.6v	-0.3		0.8	V
Ileak	Leakage current	0 < Vin < VDD All output modes disabled, pull-up/downs disabled	-5		5	µA.
Ipu	Pull-up current	If provided and enabled, Vout < 0.1v	-5			µA.
Ipd	Pull-down current	If provided and enabled, Vout > VDD – 0.1v			5	µA.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	UNIT
Iled	LED drive current	Vout = VDD, 2.7v < VDD < 3.6v		2 4 10		mA
Iolkrow	Keypad Row output low current	0.0v < Voh < 0.1v when pull-up R is enabled			-100	µA.
Iolkcol	Keypad column output high current	0.0v < Voh < 0.1v when col. is pulled low			-3	mA

Oscillator Interface Requirements

Symbol	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Low-power oscillator requirements. No external load beside the crystal and capacitor is permitted on XOUT32						
VILXIN32	Input Low Voltage		-0.3		0.8	V
VIHXIN32	Input High Voltage		1.8		5.5	V
Pxtal	Power in crystal				1	µW
IIL	Input Leakage Current	GND < Vin < VDD	-5		5	µA
High-frequency oscillator (XIN) Parameters. XIN is used as input for external clock for test purposes only. A resistor connecting X12IN to X12OUT is required, value = 1Mohm						
VILX12IN	Input Low Voltage – X12IN		-0.3		0.3*VDD	V
VIHX12IN	Input High Voltage – X12IN		0.7*VDD		Vdd+.0.3	V
IILXTAL	Input Current - X12IN	GND < Vin < Vdd	-10		10	µA
Fxtal	Crystal resonant frequency	Fundamental mode	5		15	MHz

USB Interface Requirements

PARAMETER		Condition	MIN	Typ.	MAX	UNIT
Receiver parameters						
Differential input sensitivity	***VDI***	|(DP)-(DM)|	0.2			V
Differential common mode range	VCM	Includes VDI range	0.8		2.5	V
Single ended receiver threshold	VSE		0.8		2.0	V
Transmitter levels						
Low Level Output Voltage	VOL	USBCon = 1 (DP pullup enabled)			0.3	V
High Level Output Voltage	VOH	15K ohm resistor to ground	VPD – 0.1V		VPD	V
Leakage parameters						
High-Z state data line leakage current	IOZ	0V < VIN < 3.6V			±5	nA
Output resistance (2)						
Driver output resistance	ZDRV	Steady state drive	10		14	Ω
PD Pullup Resistor (to VPD)	Zpu (1)	USBCon = 1	1.2	1.5	1.8	kΩ
Transceiver power requirements						
Operating supply current(output)	IPSO	Outputs enabled			5	mA
Operating supply current (input)	IPSI	Outputs Hi-Z			1	ma
Supply current in powerdown	IPDN				10	nA
Supply current in suspend.	IPSS				10	nA

(1) USB specifies that this value be 1.5k Ω +/- 5%. User to determine if the internal resistor meets system requirements. An external resistor could be used instead (MIUSCTRL bit 0 never set by firmware).

(2) External source (series) termination resistors of 27 ohms must be included in circuit board.

PARAMETER		Condition	MIN	Typ.	MAX	UNIT
C_L = 50pf, series 27Ω, 1% source termination resistor included						
Rise Time	USBTR	10% to 90%	4		20	ns
Fall Time	USBTF	90% to 10%	4		20	ns
Rise/fall time matching	TRFM	(USBTR/USBTF)	90		111.11	%
Output signal crossover voltage	VCRS	Includes VDI range	1.3		2.0	V
Source Jitter to Next Transition	TDJ1	Measured as in Figure 7-49 of USB 2.0 Spec	-3.5		3.5	ns
Source Jitter For Paired Transitions	TDJ2	Measured as in Figure 7-49 of USB 2.0 Spec	-4		4	ns
Receiver Jitter to Next Transition	TJR1	Measure as in Figure 7-51 of USB 2.0 Spec. Characterized but not production tested.	-18.5		18.5	ns
Receiver Jitter for Paired Transitions	TJR2	Measure as in Figure 7-51 of USB 2.0 Spec. Characterized but not production tested.	-9		9	ns
Source SE0 interval of EOP	TEOPT	Figure 7-50 of USB 2.0 Spec	160		175	ns
Receiver SEO interval of EOP	TEOPR	Figure 7-50 of USB 2.0 Spec.	82			ns

(1) For both transitions of differential signaling.

(2) Excluding first transition from the Idle state.

(3) Must accept as valid EOP.

Smart Card Interface Requirements

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Card Power Supply (V_{CC}) Regulator ***General conditions, -40°C < T < 85°C, 4.75v < V_{PC} < 6.0v, 2.7v < V_{DD} < 3.6v***						
V_{CC}	Card supply Voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode, I_{CC} = 1mA	-0.1		0.4	V
		Active mode; I_{CC} <65mA; 5v	4.65		5.25	V
		Active mode; I_{CC} <65mA; 5v, NDS condition	4.75		5.25	V
		Active mode; I_{CC} < 65mA; 3v	2.85		3.15	V
		Active mode; I_{CC} < 40mA; 1.8v	1.68		1.92	V
		Active mode; single pulse of 100mA for 2µs; 5 volt, fixed load = 25mA	4.6		5.25	V
		Active mode; single pulse of 100mA for 2µs; 3v, fixed load = 25mA	2.7		3.15	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t <400ns; 5V	4.6		5.25	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA, t <400ns; 5V	4.65		5.25	V
		Active mode; current pulses of 40nAs with peak $\|I_{CC}\|$ <200mA,t <400ns; 3V	2.7		3.15	V
		Active mode; current pulses of 20nAs with peak $\|I_{CC}\|$ <100mA,t <400ns; 1.8v	1.62		1.92	V
V_{CCrip}	V_{CC} Ripple	f_{RIPPLE} = 20kHz – 200MHz			350	mV
I_{CCmax}	Card supply output current	Static load current, V_{CC}>1.65			40	mA
		Static load current, V_{CC}>4.6 or 2.7 volts as selected			90	
I_{CCF}	I_{CC} fault current	Class A, B (5V and 3V)	100		180	mA
		Class C (1.8V)	60		130	
V_{SR}	Vcc slew rate, rise	Rise rate on activate C=1.0µF	0.06	0.15	0.25	V/µs
V_{SF}	Vcc slew rate, fall	Fall rate on de-activate, C=1.0µF	0.075	0.15	0.6	V/µs
V_{rdy}	Vcc ready voltage (VCCOK = 1)	5V operation, Vcc rising	4.6			V
		3V operation, Vcc rising	2.75			V
		1.8V operation, Vcc rising	1.65			V
C_F	External filter capacitor (V_{CC} to GND)	C_F should be ceramic with low ESR ($<100m\Omega$).	1		3.3	µF

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC. **I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I/OUC, AUX1UC, and AUX2UC.**						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} =0	0.9 * V_{CC}		V_{CC}+0.1	V
		I_{OH} = -40µA	0.75 V_{CC}		V_{CC}+0.1	V
V_{OL}	Output level, low (I/O, AUX1, AUX2)	I_{OL}=1mA			0.15 *V_{CC}	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)		0.6 * V_{CC}		V_{CC}+0.30	V
V_{IL}	Input level, low (I/O, AUX1, AUX2)		-0.15		0.2 * V_{CC}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}			10	µA
I_{IL}	Input current, low (I/O, AUX1, AUX2)	V_{IL} = 0			0.65	mA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33Ω			15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33Ω			15	mA
t_R, t_F	Output rise time, fall times	For I/O, AUX1, AUX2, C_L = 80pF, 10% to 90%.			100	ns
t_{IR}, t_{IF}	Input rise, fall times				1	µs
R_{PU}	Internal pull-up resistor	Output stable for >200ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate				1	MHz
C_{IN}	Input capacitance				10	pF
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} =-200µA	0.9 * V_{CC}		V_{CC}	V
V_{OL}	Output level, low	I_{OL}=200µA	0		0.15 *V_{CC}	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1mA			0.3	V
I_{RST_LIM}	Output current limit, RST				30	
I_{CLK_LIM}	Output current limit, CLK				70	mA
CLK_{SR3V}	CLK slew rate	V_{CC} = 3V	0.3			V/ns
CLK_{SR5V}	CLK slew rate	V_{CC} = 5V	0.5			V/ns

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
t_R, t_F	Output rise time, fall time	C_L = 35pF for CLK, 10% to 90%			8	ns
		C_L = 200pF for RST, 10% to 90%			100	ns
δ	Duty cycle for CLK	C_L =35pF, $F_{CLK} \leq$ 20MHz	45		55	%

DC Characteristics

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
I_{DD}	*Supply Current*	Default clock rates		12		mA
I_{PC}	Supply Current	V_{CC} on, ICC=0 I/O, AUX1, AUX2=high, CLK not toggling		450	650	µA
		Power down		1	10	
I_{PCOFF}	V_{PC} supply current when V_{CC} = 0	Smart card deactivated		345		µA

Voltage / Temperature Fault Detection Circuits

SYMBOL	PARAMETER	Condition	MIN	Typ.	MAX	UNIT
V_{PCF}	V_{PC} fault (V_{PC} Voltage supervisor threshold)	V_{PC}<V_{CC}, a transient event		V_{CC} > V_{PC} + 0.3		V
V_{CCF}	VCCOK = 0 (V_{CC} Voltage supervisor threshold)	V_{CC} = 5V			4.6	V
		V_{CC}= 3V			2.7	V
		V_{CC}= 1.8V			1.65	
T_F	Die over temperature fault		115		145	°C
ICCF	Vcc over current fault		110			mA

Package Pin Designation (68 pin QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

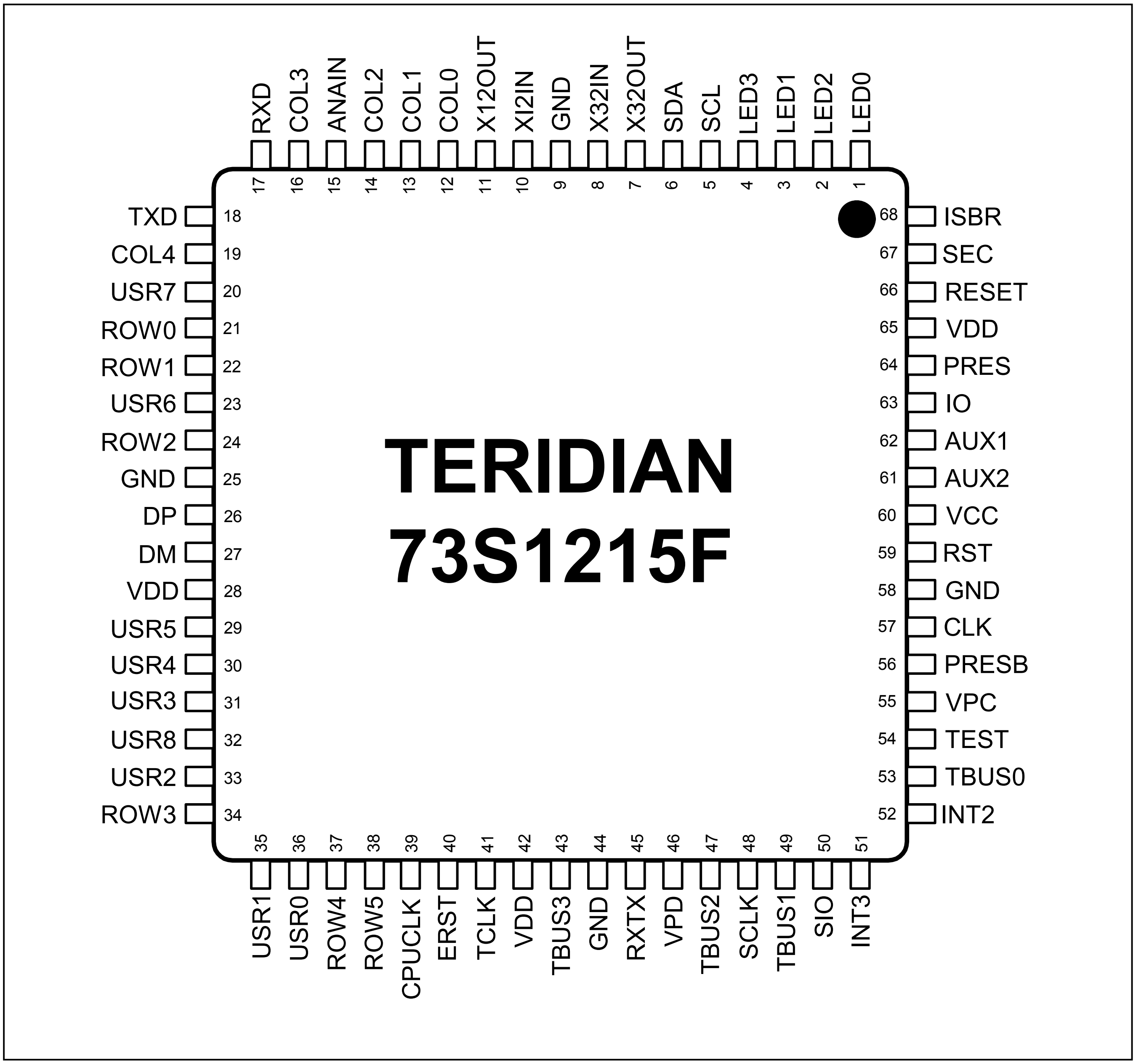


Figure 27: 73S1215F Pinout

Package Pin Designation (44 pin QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

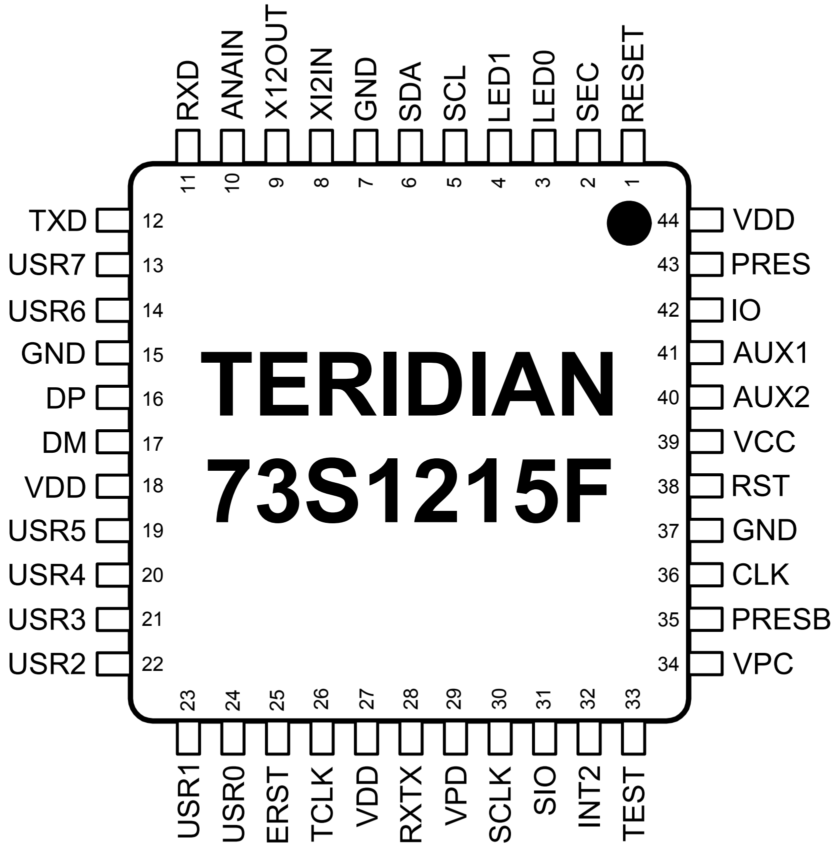


Figure 28: 73S1215F Pinout

Packaging Information

68-Pin QFN PACKAGE OUTLINE

NOTES: 6.4mm x 5mm EXPOSED PAD AREA MUST REMAIN UNCONNECTED (clear of PCB traces or vias).

CONTROLLING DIMENSIONS ARE IN mm.

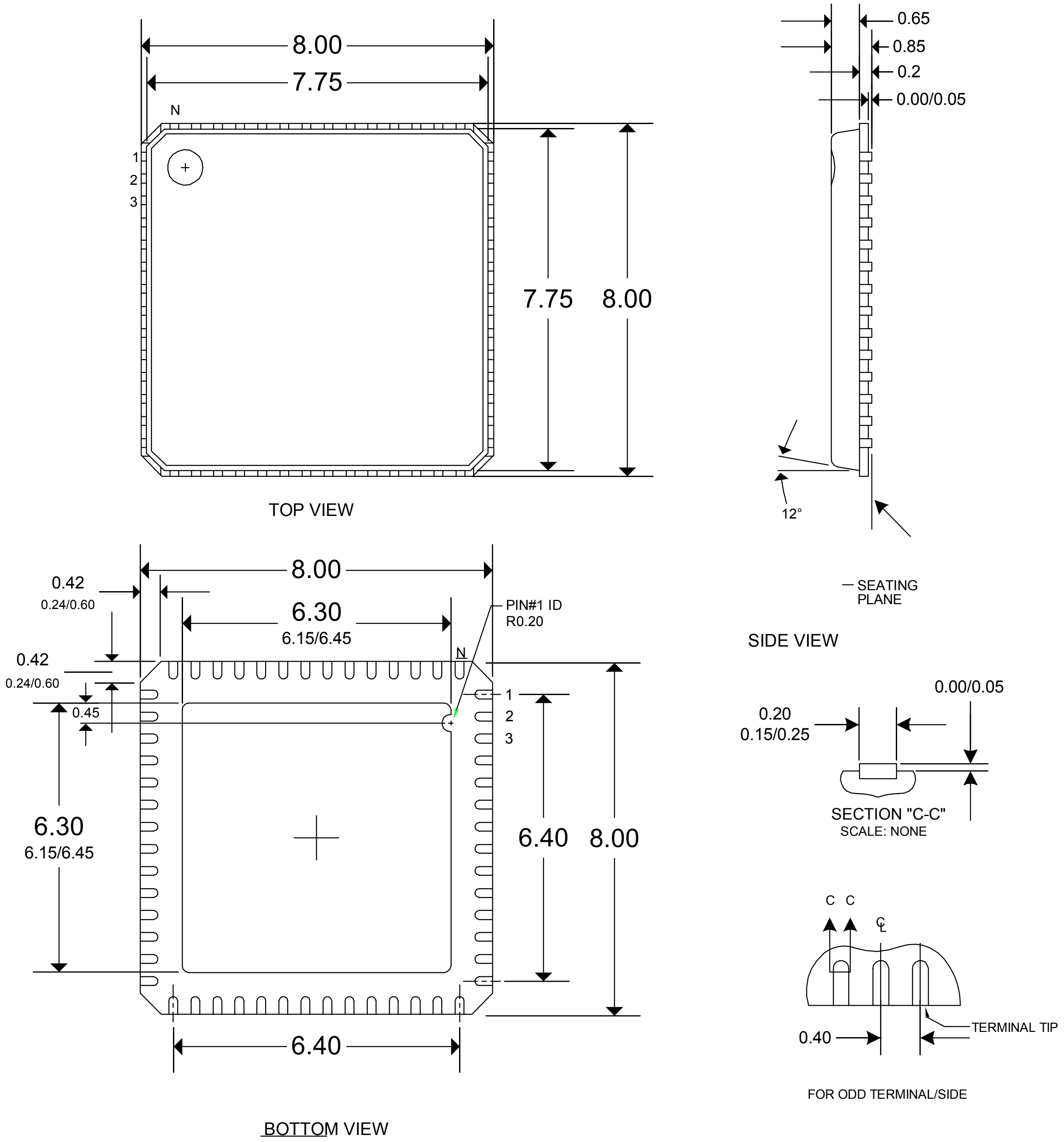


Figure 29: 73S1215F 68 QFN Pinout

44-Pin QFN PACKAGE OUTLINE

NOTES: **6.4mm x 5mm EXPOSED PAD AREA MUST REMAIN UNCONNECTED (clear of PCB traces or vias).**

CONTROLLING DIMENSIONS ARE IN mm.

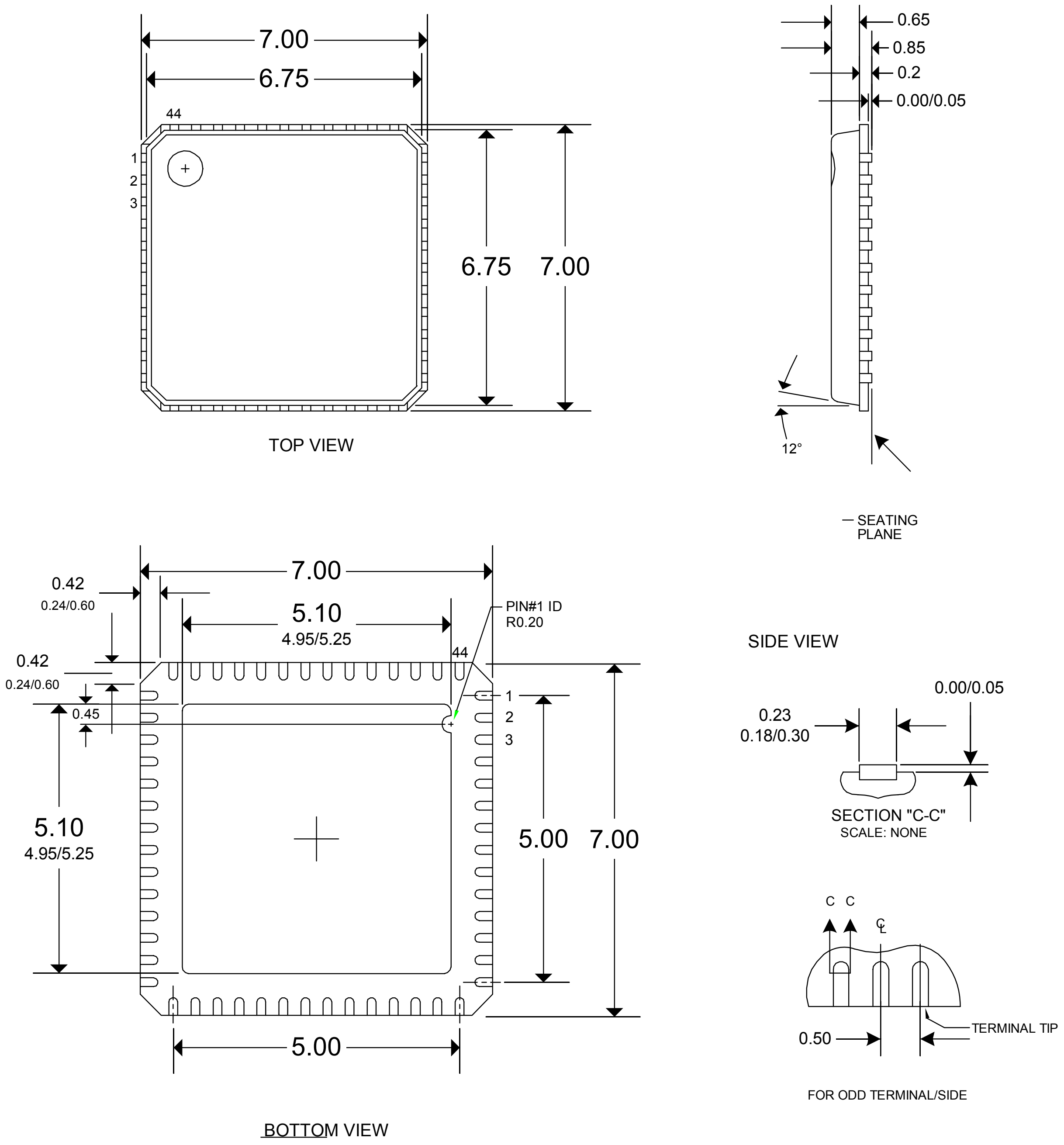


Figure 30: 73S1215F 44 QFN Pinout

TERIDIAN SEMICONDUCTOR CORP.

73S1215F

80515 System-on-Chip with USB, ISO-7816 / EMV, PINpad and more

PRELIMINARY DATA SHEET

Ordering Information

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING
73S1215F 68-pin QFN	73S1215F-68IM	73S1215F
73S1215F 68-pin QFN Tape & Reel	73S1215F-68IMR	73S1215F
73S1215F 68-pin QFN Lead Free	73S1215F-68IM/F	73S1215F
73S1215F 68-pin QFN Lead Free, Tape & Reel	73S1215F-68IMR/F	73S1215F
73S1215F 44-pin QFN	73S1215F-44IM	73S1215F
73S1215F 44-pin QFN Tape & Reel	73S1215F-44IMR	73S1215F
73S1215F 44-pin QFN Lead Free	73S1215F-44IM/F	73S1215F
73S1215F 44-pin QFN Lead Free, Tape & Reel	73S1215F-44IMR/F	73S1215F

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