



DATA SHEET

by

SYNTEK[®]

=====**STK6011Px-5V**=====

GP 8051 Microcontroller

1.3

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STK6011Px-5V Data Sheet

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1. Introduction

1.1 Brief Description

STK6011Px-5V is an 8-bit microprocessor and compatible with a 8051 processor standard; it includes a 8051 core comprising a 64k-byte program flash memory and providing the system an ISP function for upgrade of program, a 1K-byte static memory, 4 sets of 8-bit I/O ports, a set of extra 4-bit I/O port, two 16-bit timers/counters, a serial transmission interface, 5 interrupt sources, a watchdog timer, 5 sets of pulse width modulation converters, and a set of 3-channel 6-bit A/D converter.

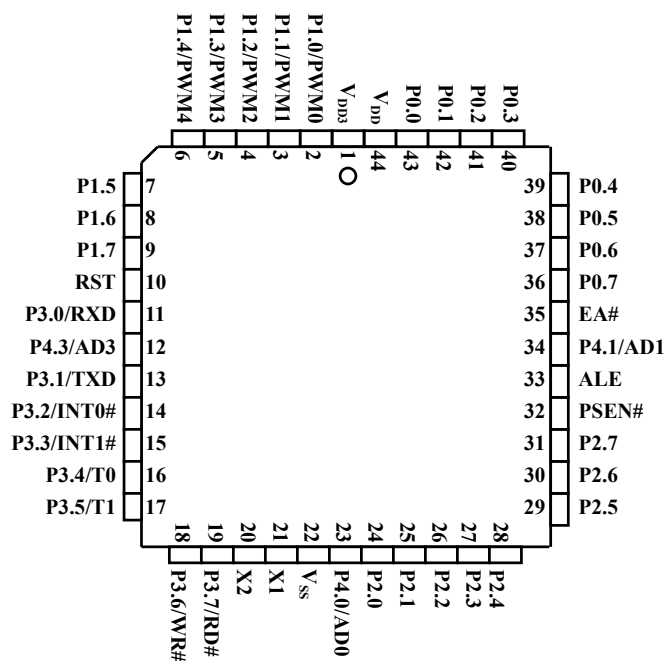
1.2. Features

- A 8051 processor standard
- 5V power supply
- Embedded with a 64k-byte program flash memory and providing the system an ISP function for upgrade of program
- A 1K-byte static memory embedded
- Optional maximum 3-channel 6-bit A/D converter
- Optional maximum 5 pulse width modulation converters
- Two 16-bit timers/counters
- Full-duplex serial transmission interfaces
- A watchdog timer programmable
- Optional maximum 35 bi-directional I/O pins
- Low-voltage reset circuit
- Interrupt wake-up (INT0# or INT1#) coming from outside at power-saving mode
- Packaging with 44-pin PLCC available



2. Pin Diagram

44 Pin PLCC





3. Pin Definition

| Pin Name | Pin Count | | | | | I/O | Description of the Functions |
|--|--|--|--|--|--|-----|---|
| | P | | | | | | |
| | L | | | | | | |
| | 44 | | | | | | |
| P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7 | 43 42 41 40 39 38 37 36 | | | | | I/O | General I/O port (8051 standard) |
| P1.0 P1.1 P1.2 P1.3 P1.4 P1.5 P1.6 P1.7 | 2 3 4 5 6 7 8 9 | | | | | I/O | General I/O port (8051 standard) |
| P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7 | 24 25 26 27 28 29 30 31 | | | | | I/O | General I/O port (8051 standard) |
| P3.0/RXD P3.1/TXD P3.2/INT0# P3.3/INT1# P3.4/T0 P3.5/T1 P3.6/WR# P3.7/RD# | 11 13 14 15 16 17 18 19 | | | | | I/O | P3.0~P3.7: general I/O port (8051 standard) RXD: serial signal input pin (8051 standard) TXD: serial signal output pin (8051 standard) INT0: external interrupt input signal pin 0, active low (8051 standard) INT1: external interrupt input signal pin 1, active low (8051 standard) T0: timer/counter input signal pin 0 (8051 standard) T1: timer/counter input signal pin 1 (8051 standard) WR#: external data memory write signal pin, active low (8051 standard) RD#: external data memory read signal pin, active low (8051 standard) |
| P4.0 P4.1 P4.3 | 23 34 12 | | | | | I/O | General I/O port |
| PWM0 PWM1 PWM2 PWM3 PWM4 | 2 3 4 5 6 | | | | | O | Pulse width modulation converter output (CMOS) |
| AD0 AD1 AD3 | 23 34 12 | | | | | I | A/D conversion input pin |
| X2 | 20 | | | | | O | Operating frequency output pin |
| X1 | 21 | | | | | I | Operating frequency input pin |
| RST | 10 | | | | | I | System reset pin, active high |
| ALE | 33 | | | | | O | External memory address latch enable signal |
| PSEN# | 32 | | | | | O | External program memory storage enable signal, active low |
| EA# | 35 | | | | | I | External program memory enable signal, active low |
| V _{DD} | 44 | | | | | - | +5 V power supply pin |
| V _{SS} | 22 | | | | | - | GND pin |
| V _{DD3} | 1 | | | | | - | +3.3 V power supply output pin, externally connected to a capacitor for voltage regulation |



4. Description of the Functions

4.1 8051 Core

STK6011Px-5V processor core is compatible with the 8051 standard; it is provided with a 256-byte static memory, a specific function register, two timers/counters, five interrupt sources, and a serial transmission interface, in which program is kept in a 64K-byte Flash.

4.2 Memory Allocation

4.2.1 Specific Function Register (SFR)

The specific function register is the same as a standard one except **P4** (D8h) and **CHIPCON** (BFh) registers.

STK6011Px-5V Specific Function Register

| | | | | | | | | |
|----|-----------|------|-----|-----|-----|-----|----------------|----|
| F8 | | | | | | | | FF |
| F0 | B | | | | | | | F7 |
| E8 | | | | | | | | EF |
| E0 | ACC | | | | | | | E7 |
| D8 | P4 | | | | | | | DF |
| D0 | PSW | | | | | | | D7 |
| C8 | | | | | | | | CF |
| C0 | | | | | | | | C7 |
| B8 | IP | | | | | | CHIPCON | BF |
| B0 | P3 | | | | | | | B7 |
| A8 | IE | | | | | | | AF |
| A0 | P2 | | | | | | | A7 |
| 98 | SCON | SBUF | | | | | | 9F |
| 90 | P1 | | | | | | | 97 |
| 88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | | 8F |
| 80 | P0 | SP | DPL | DPH | | | PCON | 87 |

4.2.1.1 Specific Function Register (Extra)

Address: D8h – Read/Write

Initial Value: 0Fh

| | | | | | | | |
|---|---|---|---|-----|---|-----|-----|
| 7 | | | | | | | 0 |
| - | - | - | - | P43 | - | P41 | P40 |

P4 (r/w): Port4 can be independently addressed and it is applied in a manner as the other ports



Address: BFh –Write-Only

Initial Value: 00h

7

0

| | | | | | | | |
|---|---|---|--------|--------|--------|---|---|
| - | - | - | XRAMen | ALEdis | CPUclk | - | - |
|---|---|---|--------|--------|--------|---|---|

| Bit 4~2 | 0/1 | Function |
|---------|-----|---|
| XRAMen | 0 | Internal auxiliary memory is not used (initial value). |
| | 1 | Internal auxiliary memory is used |
| ALEdis | 0 | ALE pin output is enabled (initial value) |
| | 1 | ALE pin output is disabled to lower EMI. |
| CPUclk | 0 | CPU works at a general operating frequency (initial value). |
| | 1 | CPU works at a double operating frequency. |

4.2.2 Internal Data Memory

The internal 256-byte memory of STK6011Px-5V is identical to 8052 standard.

4.2.3 Auxiliary Memory

All the 768 bytes of the auxiliary memory are defined in the addresses 0000h-02FFh of the extra data memory of 8051. Program can use “MOVX @Ri” to access the addresses 0000h – 00FFh of auxiliary memory or can use “MOVX @DPTR” to access the addresses 0000h – 02FFh of auxiliary memory. After reset, this auxiliary memory is disabled, and when it is used next time, the ”XRAMen” bit in CHIPCON register must be set to ”1”. When the auxiliary memory is used, the instruction “MOVX” will permanently access the internal auxiliary memory. Access of program from the auxiliary memory does not impact the signals of port 0, port 2, WR#, and RD#.

4.2.4 Extra Specific Function Register (XFR)

The extra specific function memory is defined in the addresses 0F00h – 0FFFh of the external memory of 8051, and program can use “MOVX” to access the register.

4.2.5 Program Memory

It is a 64K flash program memory, address of which ranges from 0000h to FFFFh.



4.2.6 System Reset

4.2.6.1 External Reset

At high level, the system reset pin will give birth to reset request.

4.2.6.2 Low Voltage Reset

When power voltage is not stable and the voltage level is lower than 75% VDD within a period of time, LVR will issue a reset signal to reset the CPU. When power recovers from 75% VDD, LVR stays around the reset state and 414 clock cycles are maintained, thereby stabilizing the oscillation frequency for normal operation of CPU.

4.2.6.3 Watchdog Timer Reset

When users use the watchdog timer, the timer will send a reset signal to reset CPU if it is not cleared in the overflow time.

4.3 I/O Port

Ports 0, 2, and 3 are I/O pins of 8051 standard, and they can be used for input and output.

Port 1 is an I/O pin of 8051 standard; when PWM of port 1 is enabled, the enabled pin is CMOS output.

Port 4 can be independently defined and its usage is similar to the other I/O ports'. If it functions as input or output, at the time of output of high potential, an extra pull-high resistor must be externally connected.

4.4 A/D Converter

STK6011Px-5V is embedded with a 3-channel 6-bit A/D converter. Software can be used to set bits CH3/CH1/CH0 to select a correct channel to be used. After an input channel is selected, ADC starts conversion. After conversion, the data is stored in ADC result register. If users want to execute a new ADC conversion, please re-set bits CH3/CH1/CH0 to completely implement the ADC conversion. The replacement rate of ADC can be gained at $1536/\text{Frequency}$. (For example, at 12MHz, the replacement rate is around 128 μ s.)



Cross Reference of Analog/Digital at 0V to 5V ($V_{DD}=5V$):

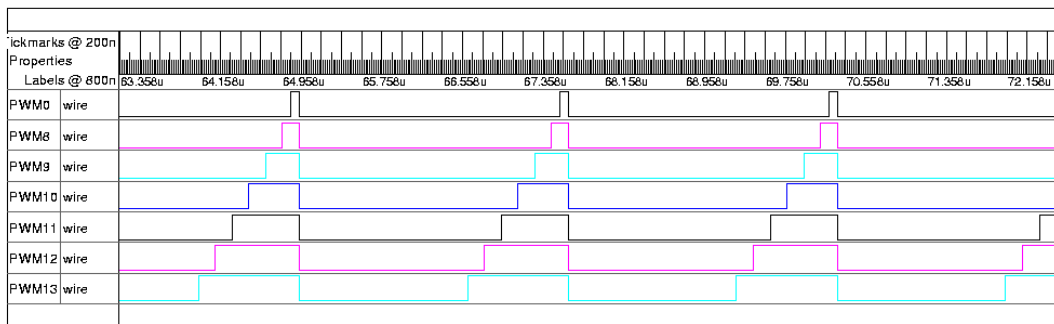
| Digital | Analog | Digital | Analog | Digital | Analog | Digital | Analog |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 0/h | -- | 10/h | 1.25 | 20/h | 2.5 | 30/h | 3.828125 |
| 1/h | 0.078125 | 11/h | 1.328125 | 21/h | 2.578125 | 31/h | 3.90625 |
| 2/h | 0.15625 | 12/h | 1.40625 | 22/h | 2.65625 | 32/h | 3.984375 |
| 3/h | 0.234375 | 13/h | 1.484375 | 23/h | 2.734375 | 33/h | 4.0625 |
| 4/h | 0.3125 | 14/h | 1.5625 | 24/h | 2.8125 | 34/h | 4.140625 |
| 5/h | 0.390625 | 15/h | 1.640625 | 25/h | 2.890625 | 35/h | 4.21875 |
| 6/h | 0.46875 | 16/h | 1.71875 | 26/h | 2.96875 | 36/h | 4.296875 |
| 7/h | 0.546875 | 17/h | 1.796875 | 27/h | 3.046875 | 37/h | 4.375 |
| 8/h | 0.625 | 18/h | 1.875 | 28/h | 3.203125 | 38/h | 4.453125 |
| 9/h | 0.703125 | 19/h | 1.953125 | 29/h | 3.28125 | 39/h | 4.53125 |
| A/h | 0.78125 | 1A/h | 2.03125 | 2A/h | 3.359375 | 3A/h | 4.609375 |
| B/h | 0.859375 | 1B/h | 2.109375 | 2B/h | 3.4375 | 3B/h | 4.6875 |
| C/h | 0.9375 | 1C/h | 2.1875 | 2C/h | 3.515625 | 3C/h | 4.765625 |
| D/h | 1.015625 | 1D/h | 2.265625 | 2D/h | 3.59375 | 3D/h | 4.84375 |
| E/h | 1.09375 | 1E/h | 2.34375 | 2E/h | 3.671875 | 3E/h | 4.921875 |
| F/h | 1.171875 | 1F/h | 2.421875 | 2F/h | 3.75 | 3F/h | 5 |

4.5 Watchdog Timer

The timer will send a reset signal to reset CPU in the case of overflow. Users can set the EWDT bit to enable the watchdog timer. When system is reset, this function is disabled. Further, users can also set the WDT register to adjust the overflow time.

4.6 Pulse Width Modulator

STK6011Px-5V provides 5 pulse width modulators, and all 8-bit **PWMDA** registers control the PWM DAC conversion outputs, respectively. The output signal pin is shared by general I/O ports. Users can set corresponding PWM outputs in the **PADOPT** register. Here, two types of PWM frequency outputs are provided for selections, and users can set PWMf bit and select one of them according to an operating frequency required; additionally, different regulation levels of resolutions are provided for users to flexibly use. (For the related registers, refer to **I/O Pin Function Register**.)



Output Waveform from the Pulse Width Modulator

4.7 Program Update Function (ISP)

Regarding the program update function of STK6011Px-5V, 3 layers - application layer, setting layer, and EEPROM read/write layer in order - are used to deal with such a work, and these 3 layers are described below together with their respective functions.

| Layer Name | Function |
|-------------------------|--|
| Application Layer | <ul style="list-style-type: none"> To define how to enter the program modification mode(It can use UART, key, and several I/Os to implement the task.) To detect when to enter the program modification mode |
| Setting Layer | <ul style="list-style-type: none"> To designate a bank among 32 banks to read/write To set EEPROM slave address, page deletion, or entire chip deletion |
| EEPROM Read/Write Layer | <ul style="list-style-type: none"> Each bank is equal to a standard 2K EEPROM. Standard EEPROM instructions are used for read/write. Completely compatible with 24C16 |



4.7.1 Application Layer

When power is on or system is reset, program executes the deserved application program until users enter the program update function to use. Entering the Program Update Function subroutine, the users must follow the execution steps listed below:

- (1) Disable watchdog timer and all interrupts,
- (2) Write ISP slave address to ISP control register,
- (3) Write a value, “93h”, to ISP control register, and
- (4) CPU is made to enter idle mode.

4.7.2 Setting Layer

At this layer, users can serve the 64K-Byte Flash as 32 EEPROMs (it works like 24C16, so in this datasheet we name it "EEPROM_like"). There is a manner of transmission:

Write: S-tttttt0k-000000wwk-ddddddddk-P

| Symbol | Descriptor |
|---------|---------------------|
| S | Start bit |
| P | Stop bit |
| tttttt | ISP slave address |
| ww | Instruction address |
| k | Slave response |
| K | Host response |
| ddddddd | Data byte |

Instruction Address:

| Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|--------|-------|-------|-------|-------|-------|-------|--------|
| 00h(w) | SDP | SDUP | ERASE | BLANK | | | | CPUclr |
| 01h(w) | | | | BANK4 | BANK3 | BANK2 | BANK1 | BANK0 |
| 02h(w) | EPSadr | | | | | | | |

00h(w): Bit 7~4 and Bit 0

| Symbol | Function |
|--------|--|
| SDP | Software protection; users must set the bit after program update. |
| SDUP | Cancellation of software protection; users must set the bit before program update. |
| ERASE | Deletion of each page (128 bytes) in flash |
| BLANK | Deletion of the whole flash |
| CPUclr | Reset of the STK6011Px-5V |

Attention: only one bit of the foregoing 6 bits can be set once at a time; when stop bit is received, it is cleared.

**01h(w): Bit 4~0**

| Symbol | Function |
|-----------------|---|
| BANK 4~0 | Selection of EEPROM_like bank; you can randomly select a EEPROM_like to access. |

02h(w): Bit 7~4

| Symbol | Function |
|----------------|------------------------------|
| EPSladr | An EEPROM_like slave address |

4.7.3 EEPROM Read/Write Layer

The steps of updating the program of STK6011Px-5V is described below:

1. Define the EEPROM_like slave address,
2. Set SDUP bit to disable the Flash software protection,
3. Define EEPROM_like block,
4. Set ERASE/BLANK bit for block-erase/chip-erase Flash,
5. Serve the Read/Write EEPROM_like as an EEPROM standard,
6. Set SDP bit to enable Flash software protection,
7. Set CPUclr bit to reset STK6011Px-5V.

Repeat steps 4~6 to read and write all data.

There are 4 ways of transmission in EEPROM_like:

For a single byte write: S-tttAAA0-k-wwwwwww-k-dddddd-k-P

For a page write: S-tttAAA0-k-wwwwwww-k-dddddd-k-dddddd-k- ... -P

For a random read: S-tttAAA0-k-wwwwwww-k(-P)-S-tttAAA1-k-dddddd-K-P

For a sequential read: S-tttAAA0-k-wwwwwww-k(-P)-S-tttAAA1-k-dddddd-K-dddddd-K- ... -P

| Symbol | Description |
|----------------|---------------------------|
| S | Start bit |
| P | Stop bit |
| ttt | EEPROM_like Slave Address |
| AAA | Page Block Address |
| wwwwwww | Word Address |
| k | Acknowledge from Slave |
| K | Acknowledge from Host |
| dddddd | Data bit |



5. Electrical Characteristics

The maximum absolute values are listed below:

1. Input/output voltage with respect to GND: $-0.5 \sim V_{DD} + 0.5V$
2. DC power supply voltage (V_{DD}): $-0.5 \sim 5.5V$
3. Operating temperature for power supply: $0 \sim 70^{\circ}C$
4. Storage temperature: $-25 \sim 125^{\circ}C$

5.1 DC Characteristics

Testing Conditions: $V_{dd} = 5V$, $T_a(\max) = 75^{\circ}C$, $X1/X2 = 12MHz$

| Parameter | Symbol | Specification | | | Conditions |
|---|---------|---------------|---------|---------|----------------------------------|
| | | Min. | Max. | Unit | |
| Operating Voltage | Vdd | 4.5 | 5.5 | V | |
| Operating Current | Idd | | 9.5 | mA | Vdd=5V, Test Pattern: PP33 |
| Power-Down Mode (PWDN) | Idwn | | 100 | μA | Vdd=5V, No External Pull-Up |
| Idle Mode (IDLE) | Idle | | 4.5 | mA | Vdd=5V, No External Pull-Up |
| Input Current (Pull-Up) EA | | -5 | -40 | μA | Vdd=5V Vin=0.0V |
| Input Current (Pull-Down) RST | | 20 | 100 | μA | Vdd=5V Vin=5V |
| Input Leakage Current | Iil/Iih | -5 | 5 | μA | Vdd=5V $0V < V_{in} < V_{dd}$ |
| Output High Voltage (CMOS) P1.0/PWM0, P1.1/PWM1 P1.2/PWM2, P1.3/PWM3 P1.4/PWM4 | Voh1 | 4 | | V | Vdd=5V Ioh=-4mA |
| Output High Voltage (8051 Standard) P1, P2, P3, and P4 | Voh2 | 4 | | V | Vdd=5V Ioh=-100 μA |
| Output Low Voltage P0, P1, P2, P3, and P4, ALE and PSEN | Vol | | 0.6 | V | Vdd=5V Iol=5mA |
| Input High Voltage | Vih | 2.4 | Vdd+0.2 | V | Vdd=5V |
| Input Low Voltage | Vil | 0 | 0.7 | V | Vdd=5V |

5.2 AC Characteristics

Testing Conditions: $T_a = 0 \sim 70^{\circ}C$, $V_{DD}=5V$, and $V_{SS}=0V$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------|--------|-------------|--------|------|-------|------|
| Oscillation Frequency | fXtal | | | 12 | | MHz |
| PWM DAC Frequency | fDA | fXtal=12MHz | 46.875 | | 94.86 | KHz |



6. Register

6.1 I/O Pin Function Control Register

Some I/O pins and special functions are made available only after users define them.

6.1.1 ADC Input Selection Register

Address: F50h - Write-Only

Initial Value: 00h

| | |
|------|------|
| 7 | 0 |
| - | - |
| - | - |
| - | - |
| AD3E | - |
| - | AD1E |
| - | AD0E |

| Bits 3~0 | 0/1 | Function |
|----------|-----|---|
| AD3E | 0 | The I/O pin (P4.3/AD3) is used as P4.3 (initial value) |
| | 1 | The I/O pin (P4.3/AD3) is used as AD3. |
| AD1E | 0 | The I/O pin (P4.1/AD1) is used as P4.1 (initial value). |
| | 1 | The I/O pin (P4.1/AD1) is used as AD1. |
| AD0E | 0 | The I/O pin (P4.0/AD0) is used as P4.0 (initial value). |
| | 1 | The I/O pin (P4.0/AD0) is used as AD0. |

6.1.2 PWM Output Selection Register

Address: F51h - Write-Only

Initial Value: 00h

| | |
|-------|-------|
| 7 | 0 |
| - | - |
| - | - |
| - | - |
| PWM4E | PWM3E |
| PWM2E | PWM1E |
| - | PWM0E |

| Bits 4~0 | 0/1 | Function |
|----------|-----|--|
| PWM4E | 0 | The I/O pin (P1.4/PWM4) is used as P1.4 (initial value). |
| | 1 | The I/O pin (P1.4/PWM4) is used as PWM4. |
| PWM3E | 0 | The I/O pin (P1.3/PWM3) is used as P1.3 (initial value). |
| | 1 | The I/O (P1.3/PWM3) pin is used as PWM3. |
| PWM2E | 0 | The I/O (P1.2/PWM2) pin is used as P1.2 (initial value). |
| | 1 | The I/O (P1.2/PWM2) pin is used as PWM2. |
| PWM1E | 0 | The I/O (P1.1/PWM1) pin is used as P1.1 (initial value). |
| | 1 | The I/O (P1.1/PWM1) pin is used as PWM1. |
| PWM0E | 0 | The I/O (P1.0/PWM0) pin is used as P1.0 (initial value). |
| | 1 | The I/O (P1.0/PWM0) pin is used as PWM0. |



6.1.3 PWM Frequency and Resolution Selection Register

Address: F56h - Write-Only

Initial Value: 00h

| | | | | | | | |
|------|------|---|---|---|---|---|---|
| 7 | | | | | | | 0 |
| PWMf | PWMr | - | - | - | - | - | - |

| Bits 7~6 | 0/1 | Function |
|-------------|----------|--|
| PWMf | 0 | 47KHz PWM frequency selected (initial value) |
| | 1 | 94KHz PWM frequency selected |
| PWMr | 0 | 256-level resolution of PWM (initial value) |
| | 1 | 253-level resolution of PWM |

6.2 PWM Register

(PWM0)

Address: F20h - Read/Write

Initial Value: 80h

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | | | | | | | 0 |
| PWM0_7 | PWM0_6 | PWM0_5 | PWM0_4 | PWM0_3 | PWM0_2 | PWM0_1 | PWM0_0 |

(PWM1)

Address: F21h - Read/Write

Initial Value: 80h

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | | | | | | | 0 |
| PWM1_7 | PWM1_6 | PWM1_5 | PWM1_4 | PWM1_3 | PWM1_2 | PWM1_1 | PWM1_0 |

(PWM2)

Address: F22h - Read/Write

Initial Value: 80h

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | | | | | | | 0 |
| PWM2_7 | PWM2_6 | PWM2_5 | PWM2_4 | PWM2_3 | PWM2_2 | PWM2_1 | PWM2_0 |

(PWM3)

Address: F23h - Read/Write

Initial Value: 80h

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | | | | | | | 0 |
| PWM3_7 | PWM3_6 | PWM3_5 | PWM3_4 | PWM3_3 | PWM3_2 | PWM3_1 | PWM3_0 |

**(PWM4)**

Address: F24h - Read/Write

Initial Value: 80h

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|
| 7 | | | | | | | 0 |
| PWM4_7 | PWM4_6 | PWM4_5 | PWM4_4 | PWM4_3 | PWM4_2 | PWM4_1 | PWM4_0 |

At the time of PWMr=1, the value written to **PWMDA** is FDH/FEH/FFH, while the output is fixed to a high-level output.

Further, when the value written to **PWMDA** is 00H, the output is fixed to a low-level output.

6.3 A/D Converter Register (ADCR)

Address: F10h – Read

Initial Value: 00h

| | | | | | | | |
|----|----|----|----|----|----|----|---|
| 7 | | | | | | | 0 |
| -- | D5 | D4 | D3 | D2 | D1 | D0 | |

| Bits 5~0 | Function |
|----------|--|
| D5~D0 | Results appear after the ADC conversion. |

Address: F10h – Write

Initial Value: 00h

| | | | | | | | |
|--------|--|--|-----|---|-----|-----|---|
| 7 | | | | | | | 0 |
| Enable | | | CH3 | - | CH1 | CH0 | |

| Bit 7 | 0/1 | Function |
|--------|-----|----------------------------------|
| Enable | 0 | ADC is disabled. (initial value) |
| | 1 | ADC is enabled. |

| Bits 3~0 | 0/1 | Function |
|----------|-----|--------------------------|
| CH3 | 0 | Not used (initial value) |
| | 1 | AD3 is selected. |
| CH1 | 0 | Not used (initial value) |
| | 1 | AD1 is selected. |
| CH0 | 0 | Not used (initial value) |
| | 1 | AD0 is selected. |



6.4 Watchdog Timer Register (WDT)

Address: F18h - Write-Only

Initial Value: 00h

| | | | | | | | |
|--------|--------|----|----|----|------|------|------|
| 7 | | | | | | | 0 |
| DISWDT | CLRWDT | -- | -- | -- | WDT2 | WDT1 | WDT0 |

Bit 7:

| | | |
|---------------|----------|--|
| DISWDT | 0 | For users to disable WDT (initial value) |
| | 1 | For users to enable WDT |

Bit 6:

| | | |
|---------------|----------|------------------------------|
| CLRWDT | 0 | No operation (initial value) |
| | 1 | For users to clear WDT |

Bits 2~0: (We take 12MHz, a fundamental frequency, into example.)

| WDT2~0 | Overflow Time |
|---------------|--------------------------|
| 0 | 2.00 sec. ± 8.096 ms |
| 1 | 0.25 sec. ± 8.096 ms |
| 2 | 0.50 sec. ± 8.096 ms |
| 3 | 0.75 sec. ± 8.096 ms |
| 4 | 1.00 sec. ± 8.096 ms |
| 5 | 1.25 sec. ± 8.096 ms |
| 6 | 1.50 sec. ± 8.096 ms |
| 7 | 1.75 sec. ± 8.096 ms |

6.5 Program Update Function (ISP) Register

6.5.1 ISP Slave Address Control Register (ISPSA)

Address: F0Bh - Write-Only

Initial Value: 00h

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|--------|---|
| 7 | | | | | | | 0 |
| ISPSA7 | ISPSA6 | ISPSA5 | ISPSA4 | ISPSA3 | ISPSA2 | ISPSA1 | - |

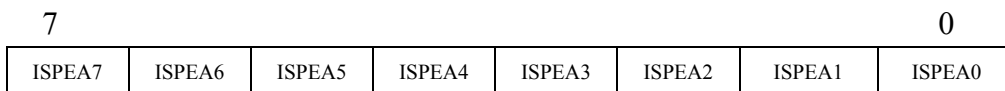
| | |
|------------------|-------------------|
| Bits 7~1 | Function |
| ISPSA 7~1 | ISP Slave Address |



6.5.2 ISP Enable Control Register (ISPEA)

Address: F0Ch - Write-Only

Initial Value: 00h



| Bits 7~0 | Function |
|----------|--|
| ISPEA7~0 | Only the value '93h' makes the ISP function available. |



Appendix A

List of All the Extra Specific Function Registers


| Address | Symbol | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0F0Bh (w) | ISPSA | ISPSA7 | ISPSA6 | ISPSA5 | ISPSA4 | ISPSA3 | ISPSA2 | ISPSA1 | - |
| 0F0Ch (w) | ISPEA | ISPEA7 | ISPEA6 | ISPEA5 | ISPEA4 | ISPEA3 | ISPEA2 | ISPEA1 | ISPEA0 |
| 0F10h (w) | ADCR | ENABLE | - | - | - | CH3 | - | CH1 | CH0 |
| 0F10h (r) | ADCR | - | - | D5 | D4 | D3 | D2 | D1 | D0 |
| 0F18h (w) | WDT | DISWDT | CLRWDT | - | - | - | WDT2 | WDT1 | WDT0 |
| 0F20h(r/w) | PWM0 | PWM0_7 | PWM0_6 | PWM0_5 | PWM0_4 | PWM0_3 | PWM0_2 | PWM0_1 | PWM0_0 |
| 0F21h(r/w) | PWM1 | PWM1_7 | PWM1_6 | PWM1_5 | PWM1_4 | PWM1_3 | PWM1_2 | PWM1_1 | PWM1_0 |
| 0F22h(r/w) | PWM2 | PWM2_7 | PWM2_6 | PWM2_5 | PWM2_4 | PWM2_3 | PWM2_2 | PWM2_1 | PWM2_0 |
| 0F23h(r/w) | PWM3 | PWM3_7 | PWM3_6 | PWM3_5 | PWM3_4 | PWM3_3 | PWM3_2 | PWM3_1 | PWM3_0 |
| 0F24h(r/w) | PWM4 | PWM4_7 | PWM4_6 | PWM4_5 | PWM4_4 | PWM4_3 | PWM4_2 | PWM4_1 | PWM4_0 |
| 0F50h(w) | PADOPT | - | - | - | - | AD3E | - | AD1E | AD0E |
| 0F51h(w) | PADOPT | - | - | - | PWM4E | PWM3E | PWM2E | PWM1E | PWM0E |
| 0F56h(w) | PADOPT | PWMf | PWMr | - | - | - | - | - | - |

Note: The last byte of Flash functions to provide protection for code, so please do not write in any data.



Appendix B

Order Information

| Part No. | Pin Count | Package | Marking |
|---------------|-----------|---------|--|
| STK6011P21-5V | 44 | PLCC |  STK6011P21-5V Manu. No |