FlashFlex51 MCU
SST89F54 / SST89F58

Preliminary Specifications

FEATURES:

- **8051 Compatible Multi-Purpose 8-bit Microcontroller Unit (MCU) with Embedded SuperFlash Memory for Design Flexibility**
- **Fully Software and Development Toolset Compatible as well as Pin-For-Pin Package Compatible with Standard 8xC5x Microcontrollers**
- **256 Bytes Register/Data RAM**
- **20/36 KByte Embedded High Performance Flexible SuperFlash EEPROM**
  - One 16/32 KByte block (128-Byte sector size)
  - One 4 KByte block (64-Byte sector size)
  - Individual Block Security Lock
  - 87C5x Programmer Compatible
  - Concurrent Operation during In-Application Programming (IAP)
- **Support External Address Range up to 64 KByte of Program and Data Memory**
- **High Current Drive on Port 1 (5, 6, 7) pins**
- **Three 16-bit Timer/Counters**
- **Programmable Serial Port (UART)**
- **Six Interrupt Sources at 2 Priority Levels**
- **Selectable Watchdog Timer (WDT)**
- **Four 8-bit I/O Ports (32 I/O Pins)**
- **TTL- and CMOS-Compatible Logic Levels**
- **0 to 33 MHz Operation at 5V±10% Supply**
- **0 to 12 MHz Operation at 3V±10% Supply**
- **PDIP-40, PLCC-44 and TQFP-44 Packages**
- **Temperature Ranges:**
  - Commercial (0°C to +70°C)
  - Industrial (-40°C to +85°C)

PRODUCT DESCRIPTION

SST89F54 and SST89F58 are members of the FlashFlex51 family of 8-bit microcontrollers. The FlashFlex51 family is a family of embedded microcontroller products designed and manufactured on the state-of-the-art SuperFlash CMOS semiconductor process technology.

As a member of the FlashFlex51 controller family, the SST89F54/58 uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with standard 8xC5x microcontroller devices.

SST89F54/58 comes with 20/36 KByte of integrated on-chip flash EEPROM program memory using the patented and proprietary Silicon Storage Technology, Inc. (SST) SuperFlash EEPROM technology with the SST field enhancing tunneling injector split-gate memory cells. The SuperFlash memory is partitioned into 2 independent program memory blocks. The primary SuperFlash block occupies lower most 16/32 KByte of internal program memory space and the secondary SuperFlash block occupies upper most 4 KByte of standard 8051 internal program address space. The flash memory blocks can be programmed via a standard 87C5x EPROM programmer or a standard flash EEPROM memory programmer fitted with a special adapter and firmware for SST89F54/58 devices. During power-on reset, the SST89F54/58 can be configured as a master for In-Application Programming™ (IAP)™ or as a slave to an external host. SST89F54/58 is designed to be programmed “in-place” and “in-operation” on the printed circuit board assembly for maximum flexibility.

The highly reliable, patented SuperFlash technology and memory cell have a number of important advantages for designing and manufacturing flash EEPROMs, when compared with other approaches. These advantages translate into significant cost and reliability benefits for our customers.

In addition to 20/36 KByte of SuperFlash EEPROM program memory on-chip, the SST89F54/58 can address up to 64 KByte of program memory external to the chip. The SST89F54/58 have 256 x8 bits of on-chip RAM. Up to 64 KByte of external data memory (RAM) can be addressed.

TABLE OF CONTENTS

PRODUCT FEATURES 1

PRODUCT DESCRIPTION 1

FUNCTIONAL BLOCKS 4
- Functional Block Diagram 4

PIN ASSIGNMENTS 5
- Pin Descriptions 6

MEMORY ORGANIZATION 8
- Program Memory 8
- Data Memory 10
- Special Function Registers (SFR) 10
  - *CPU Related SFRs* 10
  - *Flash Memory Programming SFRs* 11
  - *Chip Operational SFRs* 11
  - *Timer/Counters SFRs* 11
  - *Interface SFRs* 11

FLASH MEMORY PROGRAMMING 12
- External Host Mode 12
  - Product Identification 13
  - External Host Mode Commands 13
  - Programming a SST89F54/58 in External Host Mode 14
  - Flash Operation Status Detection (Ext. Host Handshake) 14
- In-Application Programming Mode 19
  - In-Application Programming Commands 19
  - Polling 20

WATCHDOG TIMER 22

SECURITY LOCK 23
- Activation and Deactivation of the Security Lock 23

SYSTEM DESIGN CONSIDERATIONS 24
Reset (Hardware) 24
Power-On Reset 24

POWER SAVING MODES 25

CLOCK INPUT OPTIONS 26

ELECTRICAL SPECIFICATION 27
Absolute Maximum Ratings 27
Operation Range 27
Reliability Characteristics 27
DC Electrical Characteristics 28
AC Electrical Characteristics 32
Explanation Of Symbols 33
External Clock Drive. 34
Serial Port Timing - Shift Register Mode 35

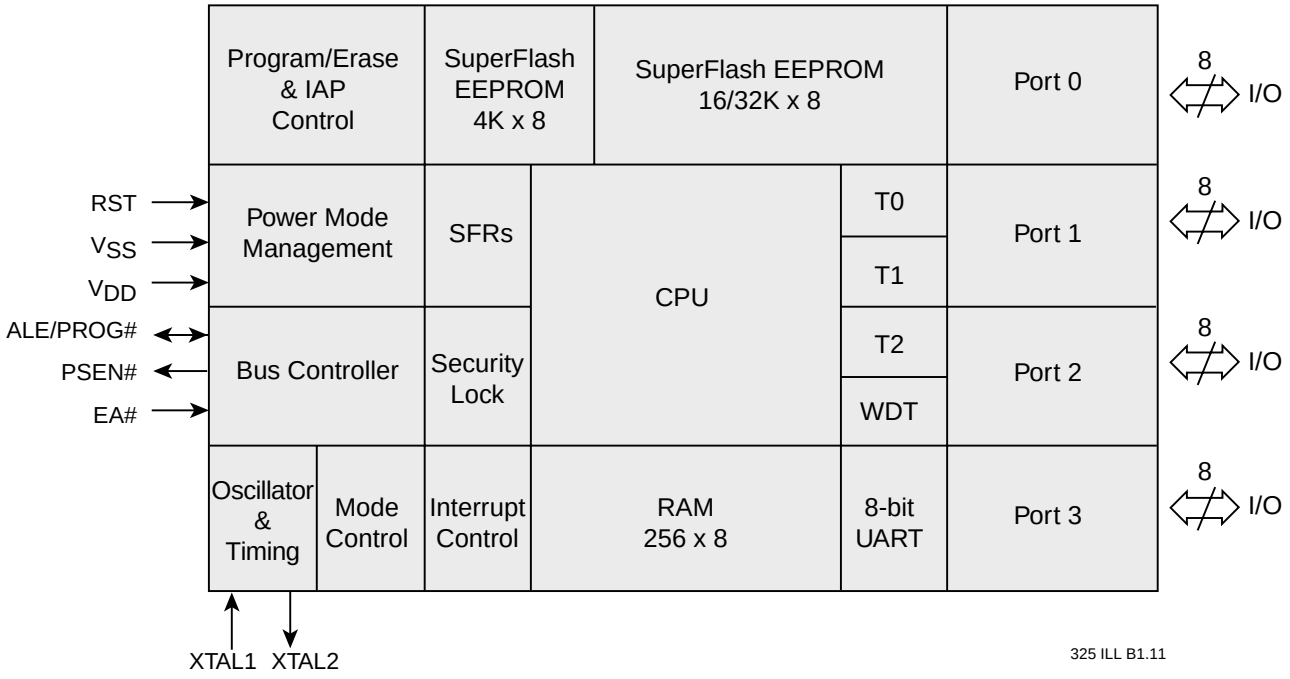
PRODUCT ORDERING INFORMATION 36
Part Number Valid Combinations 37
Part Number Cross Reference Guide 38

PACKAGING DIAGRAMS 39

SALES OFFICES 42

FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS

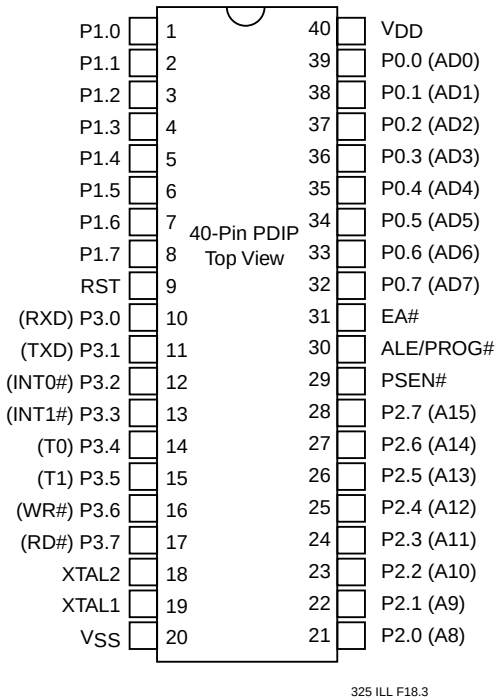


FIGURE 1: PIN ASSIGNMENTS FOR 40-PIN PLASTIC DIP PI - PACKAGE

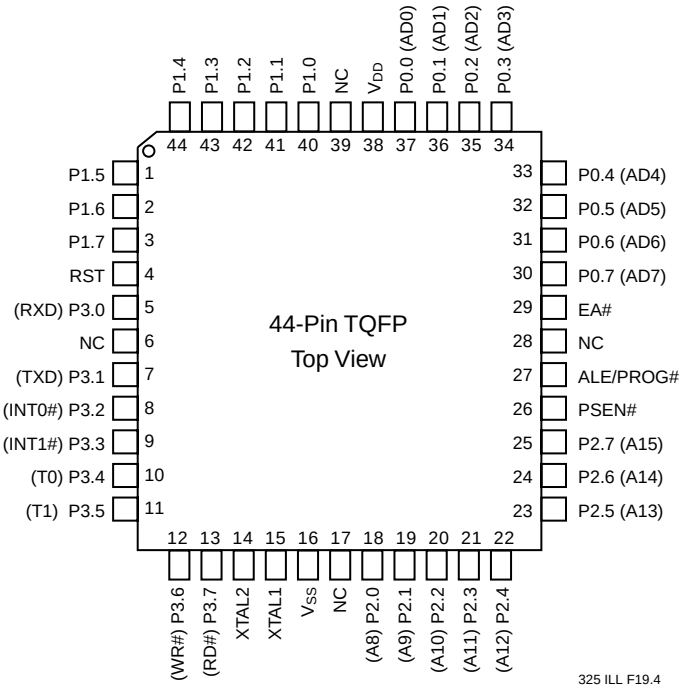


FIGURE 2: PIN ASSIGNMENTS FOR 44-PIN TQFP TQJ - PACKAGE

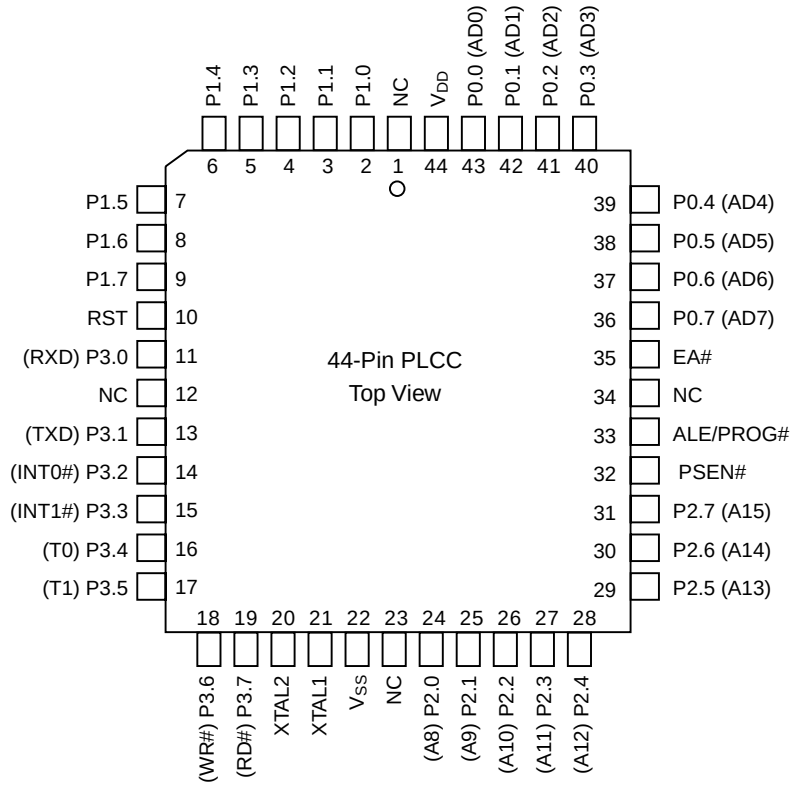


FIGURE 3: PIN ASSIGNMENTS FOR 44-PIN PLCC NJ - PACKAGE

Note: NC pins must be left unconnected.

TABLE 1: PIN DESCRIPTIONS

Symbol	Type[1]	Name and Functions
P0[7:0]	I/O[1]	***Port 0:*** Port 0 is an 8-bit open drain bi-directional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pull-ups when transitioning to 1's. Port 0 also receives the code bytes during FLASH MEMORY programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.
P1[7:0]	I/O with internal pull-ups	***Port 1:*** Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pull-ups. P1(5, 6, 7) have high current drive of 16 mA. Port 1 also receives the low-order address bytes during FLASH MEMORY programming and program verification.
P2[7:0]	I/O with internal pull-ups	***Port 2:*** Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. Port 2 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pull-ups. Port 2 sends the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX@DPTR). In this application it uses strong internal pull-ups when outputting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX@Ri), Port 2 sends the contents of the P2 Special Function Register. Port 2 also receives some control signals and a partial of high-order address bits during FLASH MEMORY programming and program verification.
P3[7:0]	I/O with internal pull-ups	***Port 3:*** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers could drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pull-ups. Port 3 also serves the functions of various special features of the FlashFlex51 Family. Port 3 also receives some control signals and a partial of high-order address bits during FLASH MEMORY programming and program verification.
P3.0	I	***RXD:*** Serial input line
P3.1	O	***TXD:*** Serial output line
P3.2	I	***INT0#:*** External Interrupt 0
P3.3	I	***INT1#:*** External Interrupt 1
P3.4	I	***T0:*** Timer 0 external input
P3.5	I	***T1:*** Timer 1 external input
P3.6	O	***WR#:*** External Data Memory Write strobe
P3.7	O	***RD#:*** External Data Memory Read strobe
PSEN#	O/I	***Program Store Enable:*** PSEN# is the Read strobe to External Program Memory. When the SST89F54/58 are executing from Internal Program Memory, PSEN# is inactive (high). When the device is executing code from External Program Memory, PSEN# is activated twice each machine cycle, except that two PSEN# activations are skipped during each access to External Data Memory. While the RST input is continually held high (for more than ten machine cycles), a forced high-to-low input transition on the PSEN# pin will bring the device into the "External Host" mode for the internal flash memory programming operation.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Type[1]	Name and Functions
RST	I	***Reset:*** A high logic state on this pin for two machine cycles (at least 24 oscillator periods), while the oscillator is running resets the device. After a successful reset is completed, if the PSEN# pin is driven by an input force with a high-to-low transition while the RST input pin is continually held high, the device will enter the "External Host" mode for the internal flash memory programming operation, otherwise the device will enter the "Normal" operation mode.
EA#	I	***External Access Enable:*** EA# must be connected to V_{SS} in order to enable the SST89F54/58 to fetch code from External Program Memory locations starting at 0000h up to FFFFh. Note, however, that if the Security Lock is activated on either block, the logic level at EA# is internally latched during reset. EA# must be connected to V_{DD} for internal program execution. The EA# pin can tolerate a high voltage[2] of 12V (see Electrical Specification).
ALE/PROG#	O/I	***Address Latch Enable:*** ALE is the output signal for latching the low byte of the address during accesses to external memory. This pin is also the programming pulse input (PROG#).
$XTAL_1$ $XTAL_2$	I O	***Oscillator:*** Input and output to the inverting oscillator amplifier. XTAL1 is input to internal clock generation circuits from an external clock source.
V_{DD}	I	***Power Supply:*** Supply voltage
Vss	I	***Ground:*** Circuit ground. (0V reference)

Note: 1) I = Input
O = Output
2) It is not necessary to receive a 12V programming supply voltage during flash programming.

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MEMORY ORGANIZATION

The SST89F54/58 has separate address spaces for program and data memory.

Program Memory

There are two internal flash memory blocks in the SST89F54/58. The primary flash memory block (Block 0) has 16/32 KByte and occupies the address space 0000h to 3FFFh/7FFFh. The secondary flash memory block (Block 1) has 4 KByte and occupies the address space F000h to FFFFh.

When internal code operation is enabled (EA# = 1), the primary 16/32 KByte flash memory block is always visible to the program counter for code fetching. Figure 4 and 5 shows the program memory organizations for the SST89F54/58.

The 16/32 KByte primary SuperFlash block are organized as 128/256 sectors with sector address from A15 to A7. Each sector contains 2 rows with row address from A15 to A6. Each row has 64 Bytes with byte address from A5 to A0.

When internal code operation is enabled (EA# = 1), the secondary 4 KByte flash memory block is selectively visible for code fetching. The secondary block is always accessible through the SuperFlash mailbox registers: SFCM, SFCF, SFAL, SFAH and SFDT. When bit 7 of the SuperFlash Configuration/Status mailbox register (SFCF:7), SFR address location F7h, is set, the secondary 4 KByte block will be visible by program counter.

The 4K x8 secondary SuperFlash block are organized as 64 sectors with sector address from A15 to A6. Each sector contains 2 rows with row address from A15 to A5. Each row contains 32 Bytes with byte address from A4 to A0.

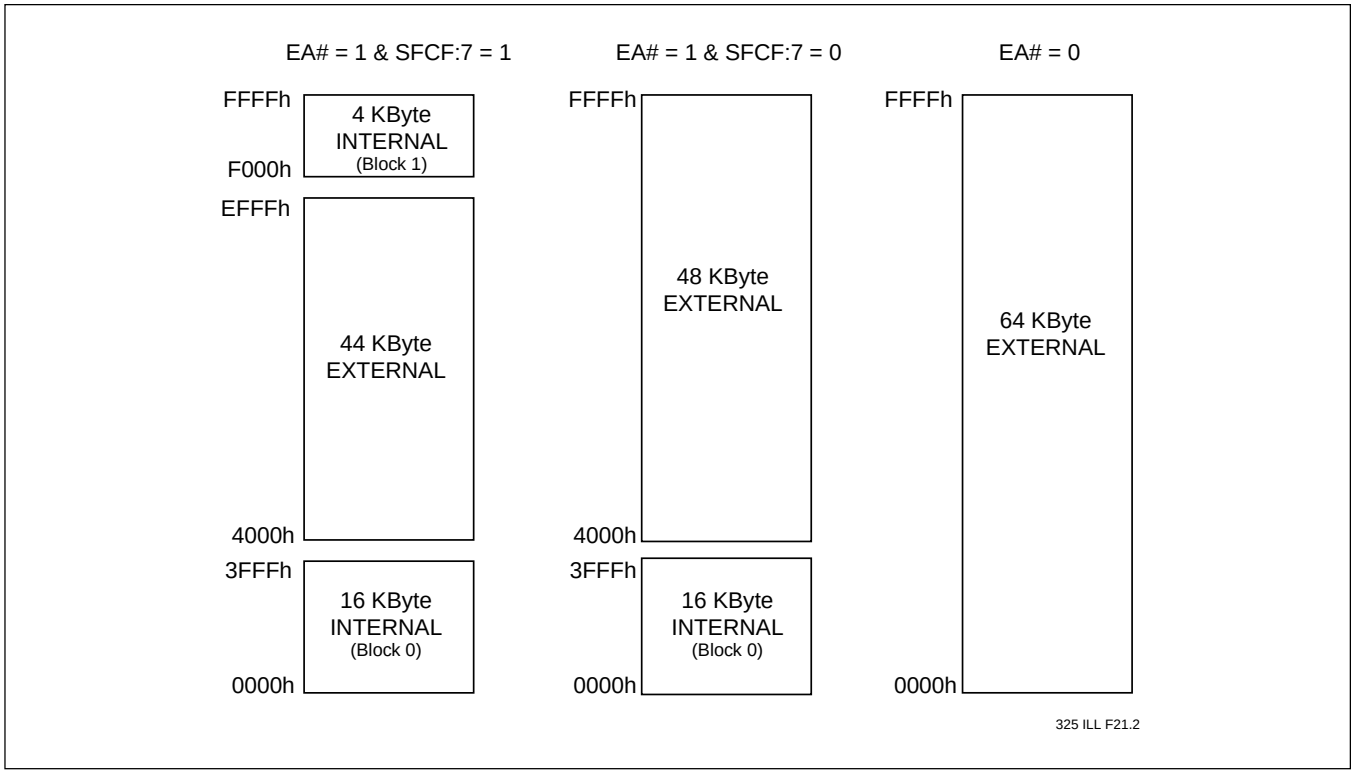

FIGURE 4: SST89F54 PROGRAM MEMORY ORGANIZATION

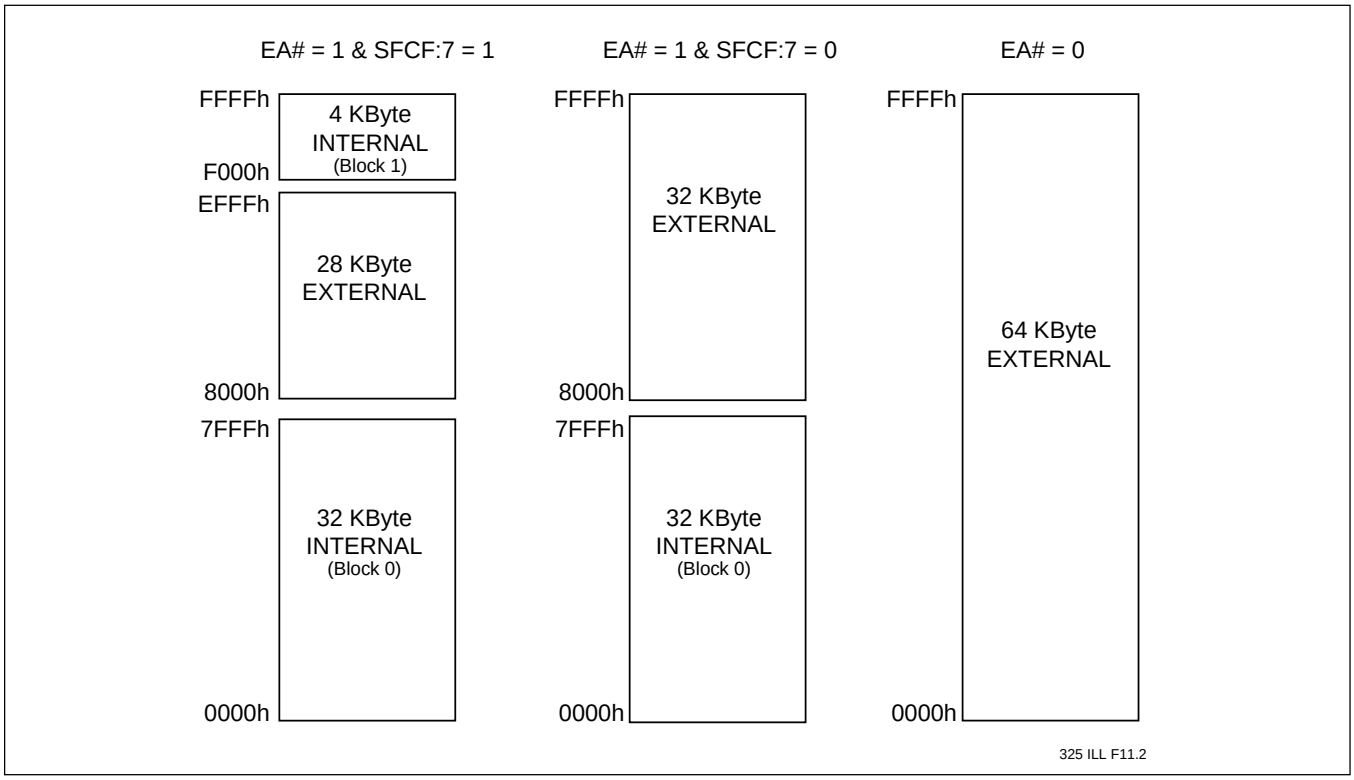

FIGURE 5: SST89F58 PROGRAM MEMORY ORGANIZATION

Data Memory

SST89F54/58 have 256 Bytes of on chip RAM and 4 KBytes of small sectors (64 Bytes per sector) on chip flash memory to be mapped either as program memory or data memory. When the 4 KByte flash is mapped as data memory (SFCF: 7 = 0) it is accessible via the mailbox registers.

Special Function Registers (SFR)

Most of the unique features of the FlashFlex51 microcontroller family are controlled by bits in special function registers (SFRs) located in the FlashFlex51 SFR Memory Map shown below. Individual descriptions of each SFR are provided and Reset values indicated in Tables 3A to 3E.

8 BYTES

F8	SFDT	SFAL	SFAH	SFCM				FF
F0	B*						SFCF	F7
E8								EF
E0	ACC*							E7
D8								DF
D0	PSW*							D7
C8	T2CON*		RCAP2L	RCAP2H	TL2	TH2		CF
C0	WDTC*							C7
B8	IP*							BF
B0	P3*							B7
A8	IE*							AF
A0	P2*							A7
98	SCON*	SBUF						9F
90	P1*							97
88	TCON*	TMOD	TL0	TL1	TH0	TH1		8F
80	P0*	SP	DPL	DPH			WDTD	PCON 87

FlashFlex51 SFR Memory Map

* SFRs are bit addressable
All addresses are hexadecimal

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SST89F54/58 Special Function Registers

TABLE 3A: CPU RELATED SFRS

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB						LSB	RESET Value
ACC*	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h
B*	B Register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h
PSW*	Program Status Word	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	00h
SP	Stack Pointer	81h	SP[7:0]								07h
DPL	Data Pointer Low 0	82h	DPL[7:0]								00h
DPH	Data Pointer High 0	83h	DPH[7:0]								00h
IE*	Interrupt Enable	A8h	EA	-	ET2	ES	ET1	EX1	ET0	EX0	0x000000b
IP*	Interrupt Priority	B8h	-	-	PT2	PS	PT1	PX1	PT0	PX0	xx000000b

* SFRs are bit addressable
x = don't care

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TABLE 3B: FLASH MEMORY PROGRAMMING SFRS

Symbol	Description	Direct Address	Bit Address, Symbol, or Alternative Port Function MSB LSB Value								RESET
SFCF	SuperFlash Configuration/Status	F7h	VIS	SECD		-	BUSY	FREQ			00h
SFCM	SuperFlash Command	FBh	FIE	FCM							00h
SFDT	SuperFlash Data	F8h	SuperFlash Data Register								00h
SFAL	SuperFlash Address Low	F9h	SuperFlash Low Order Byte Address Register – A7 to A0 (SFAL)								00h
SFAH	SuperFlash Address High	FAh	SuperFlash High Order Byte Address Register – A15 to A8 (SFAH)								00h

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TABLE 3C: CHIP OPERATIONAL SFRS

PCON	Power Control	87h	SMOD	-	-	-	GF1	GF0	PD	-	0xxx000xb
WDTC*	Watchdog Timer Control	C0h	-	-	-	-	WDRE	WDTS	WDT	SWDT	X0h
WDTD	Watchdog Timer Data/Reload	86h	WDRL								00h

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TABLE 3D: TIMER/COUNTERS SFRS

TMOD	Timer/Counter Mode Control	89h	Timer 1				Timer 0				00h
			GATE	C/T#	M1	M0	GATE	C/T#	M1	M0	
TCON*	Timer / Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h
TH0	Timer 0 MSB	8Ch	TH0[7:0]								00h
TL0	Timer 0 LSB	8Ah	TL0[7:0]								00h
TH1	Timer 1 MSB	8Dh	TH1[7:0]								00h
TL1	Timer 1 LSB	8Bh	TL1[7:0]								00h
T2CON*	Timer / Counter 2 Control	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	00h
TH2	Timer 2 MSB	CDh	TH2[7:0]								00h
TL2	Timer 2 LSB	CCh	TL2[7:0]								00h
RCAP2H	Timer 2 Capture MSB	CBh	RCAP2H[7:0]								00h
RCAP2L	Timer 2 Capture LSB	CAh	RCAP2L[7:0]								00h

325 PGM T9D.0

TABLE 3E: INTERFACE SFRS

SBUF	Serial Data Buffer	99h	SBUF[7:0]								Indeterminate
SCON*	Serial Port Control	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00h
P0*	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh
P1*	Port 1	90h	-	-	-	-	-		T2EX	T2	FFh
P2*	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
P3*	Port 3	B0h	RD#	WR#	T1	T0	INT1#	INT0#	TXD	RXD	FFh

* SFRs are bit addressable
x = don't care

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FLASH MEMORY PROGRAMMING

The SST89F54/58 internal flash memory can be programmed or erased using the following two modes:

- External Host Mode (parallel only)
- In-Application Programming (IAP) Mode (parallel or serial)

SST SuperFlash EEPROMs are single power supply reprogrammable nonvolatile memories intended to be altered in-system with the use of one power supply. Similar to SRAMs, there exists the possibility of unintentional writes. The security lock prevents inadvertent alteration of data and code stored in the flash memory. **In order to assure the preservation of data integrity, it is required that the device remains locked at all times.**

EXTERNAL HOST MODE

The SST89F54/58 provide the user with a direct flash memory access that can be used for programming into the flash memory without using the CPU. The direct flash memory access is entered using the External Host Mode. While the reset input (RST) is continually held active (high) and if the PSEN# pin is forced by an input with a transition from high-to-low state, the device enters the External Host Mode. The CPU core is stopped from running and all the chip I/O pins are reassigned and become flash memory access and control pins. After the device enters into the External Host Mode, the internal flash memory blocks are accessed through the re-assigned I/O port pins (please see Figure 6 for details) by an external host, such as a printed circuit board tester, a PC controlled development board or a programmer. The SST89F54/58 need a clock signal of 4-8 MHz on XTAL 1 to operate the External Host Mode. The clock signal is required to generate internal signals used to control Program and Erase operations.

When the chip is in the external host mode, Port 0 pins are assigned to be the parallel data input and output pins. Port 1 pins are assigned to be the non-muxed low order address bus signals for the internal flash memory (A0-A7). The first six bits of Port 2 pins (P2[0:5]) are assigned to be the non-muxed upper order address bus signals for the internal flash memory (A8-A13) along with two of the Port 3 pins (P3.4 as A14 and P3.5 as A15). Two upper order Port 2 pins (P2.6 and P2.7) and two upper order Port 3 pins (P3.6 and P3.7) along with RST, PSEN#, PROG#/ALE, EA# pins are assigned as the control signal pins. The Port 3 pin (P3.3) is assigned to be the Ready/Busy# status signal, which can be used for handshaking with the external host during a flash memory programming operation. The flash memory programming operation (Erase, Program, Verify, etc.) is internally self-timed and can be controlled by an external host asynchronously or synchronously.

The External Host Mode uses seven (7) hardware commands, which are decoded from the control signal pins, to facilitate the internal flash memory erase and programming process. The External Host Mode Commands are enabled on the falling edge of ALE/PROG#. The list in Table 4 outlines all the commands and its control signal assignment.

TABLE 4: EXTERNAL HOST MODE COMMANDS

Operation	RST	PSEN#	PROG# /ALE	EA#	P2.6	P2.7	P3.6	P3.7	P0[7:0]	P1[7:0]	P3[5:4] P2[5:0]
Read-ID	H	L	H	H	L	L	L	L	DO	AL	AH
Chip-Erase	H	L	⇓	H	H	H	H	L	X	X	X
Block-Erase	H	L	⇓	H	H	H	H	H	X	X	AH
Sector-Erase	H	L	⇓	H	H	H	L	H	X	AL	AH
Byte-Program	H	L	⇓	H	L	H	H	H	DI	AL	AH
Burst-Program	H	L	⇓	H	L	H	L	H	DI	AL	AH
Byte-Verify	H	L	H	H	L	L	H	H	DO	AL	AH

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Note: Symbol ⇓ signifies a negative pulse and the command is asserted during the low state of PROG#/ALE input. All other combinations of the above input pins are invalid and may result in unexpected behaviors.

Note: L = Logic low level; H = Logic high level; X = Don't care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output

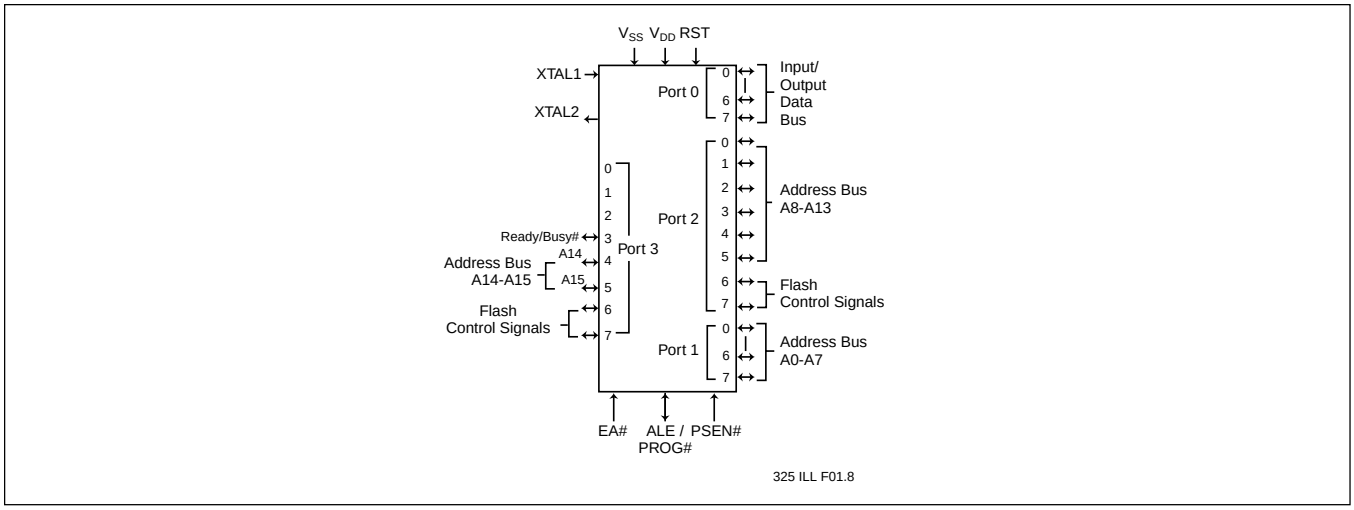


FIGURE 6: I/O PINS ASSIGNMENT FOR EXTERNAL HOST MODE

Product Identification

The Read-ID command accesses the Signature Bytes that identifies the device as an SST89F54/58 and the manufacturer as SST. External programmers primarily use these Signature Bytes, shown in Table 5, in the selection of programming algorithms. The Read-ID command is selected by the Byte Code of 00h on P2[6:7] and P3[6:7]. See Figure 7 for timing waveforms.

TABLE 5: SIGNATURE BYTES TABLE

	Address	Data
Manufacturer's Code	0030h	BFh
SST89F54 Device Code	0031h	E3h
SST89F58 Device Code	0031h	E1h

325 GPM T3.4

External Host Mode Commands

The seven SST89F54/58 External Host Mode Commands are Read-ID, Chip-Erase, Block-Erase, Sector-Erase, Byte-Program, Burst-Program, and Byte-Verify. The following is a brief description of the commands. See Table 4 for all signal logic assignments and Table 7 for all timing parameter values for the External Host Mode Commands. The critical timing for all Erase and Program commands is dependent upon the 4-8 MHz external clock input at the XTAL1 pin. The high-to-low transition of the PROG# signal initiates the Erase and Program commands, which are synchronized internally. The Read commands are static reads, independent of the PROG# signal level.

The following three commands are for erasing all or part of the memory array. All the data in the memory array will be erased to FFh. Memory addresses that are to be programmed must be in the erased state prior to programming. Selection of the Erase command to use, prior to programming the device, will be dependent upon the contents already in the array and the desired programming field size.

The Chip-Erase command erases both memory blocks (16/32K and 4K) of the SST89F54/58. This command ignores the security lock status and will erase the Security Byte. The Chip Erase command is selected by the byte code of 0Eh on P2[6:7] and P3[6:7]. See Figure 8 for timing waveforms.

The Block-Erase command erases one of the memory blocks (16/32K or 4K) of the SST89F54/58. This command will not enable if the selected memory block is security locked. The selection of the memory block to be erased is determined by P3[5:4] and P2[5:0]. If P3[5:4] and P2[5:0] is a "0Xh", then the primary flash memory block (16/32K) is selected. If P3[5:4] and P2[5:0] is a "FXh", then the secondary flash memory block (4K) is selected. The Block-Erase command is selected by the byte code of 0Fh on P2[6:7] and P3[6:7]. See Figure 9 for the timing waveforms.

The Sector-Erase command erases a sector. The sector size for the primary flash memory block (Address locations 0-3FFFh/7FFFh) is 128 Bytes. The sector size for the secondary flash memory block (Address locations F000h-FFFFh) is 64 Bytes. This command will not enable if the selected memory block is security locked. The selection of the memory sector to be erased is determined by P1[6:7] (A6 & A7), P2[0:5] (A8-A13) and P3[4:5] (A14 & A15). The Sector-Erase command is selected by the byte code of 0Dh on P2[6:7] and P3[6:7]. See Figure 10 for timing waveforms.

The following two Program commands are for programming new data into the memory array. Selection of which Program command to use for programming will be dependent upon the desired programming field size. The Program commands will not enable if the selected memory block is security locked.

The Byte-Program command programs data into a single byte. Ports P0[0:7] are used for data input. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). The Byte-Program command is selected by the byte code of 07h on P2[6:7] and P3[6:7]. See Figure 11 for timing waveforms.

The Burst-Program command programs data to an entire row, sequentially byte-by-byte. Ports P0[0:7] are used for data input. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). The Burst-Program command is selected by the byte code of 05h on P2[6:7] and P3[6:7]. See Figure 12 for timing waveforms.

The termination of the Burst-Program can be accomplished by: 1) Change to a new row-Addresses (Note: the address range are different for the 4Kx8 flash block and for the 16/32K x8 flash block.); 2) Change to a new command that requires a negative transition of the ALE/PROG# (i.e. any Erase or Program command); 3) Wait for time out limit expires (20 µs); programming the next byte.

The Byte-Verify command allows the user to verify that the SST89F54/58 correctly performed an Erase or Program command. Ports P0[0:7] are used for data output. The memory location is selected by P1[0:7], P2[0:5], and P3[4:5] (A0-A15). This command will not enable if the selected memory block is security locked. See Figure 13 for timing waveforms.

Programming a SST89F54/58 in External Host Mode

To program new data into the memory array, supply 5 volts to V_{DD} and RST, and perform the following steps.

1. Enable RST, and PSEN# in sequence per the appropriate timing diagram.
2. Raise EA# High (either V_{IH} or V_H).
3. Read the device and manufacturer ID, using the Read-ID command, to ensure the correct programming algorithm.
4. Verify that the memory blocks or sectors for programming are in the erased state, FFh. If they are not erased, then erase them using the appropriate Erase command.
5. Select the memory location using the address lines (P1[0:7], P2[0:5], P3[4:5]).
6. Present the data in on P0[0:7] and the program command on P2[6:7] and P3[6:7].
7. Pulse ALE/PROG#.
8. Wait for low to high transition on READY/BUSY# (P3.3).
9. Repeat steps 5 – 8 until programming is finished.
10. Verify the flash memory contents.

Flash Operation Status Detection (Ext. Host Handshake)

The SST89F54/58 provide two firmware means for an external host to detect the completion of a flash memory operation, therefore the external host can optimize the system Program or Erase cycle of the embedded flash memory. The end of a flash memory operation cycle (Erase or Program) can be detected by: 1) monitoring the Ready/Busy# bit at Port 3.3; 2) monitoring the Data# Polling bit at Port 0.7.

Ready/Busy# (P3.3)

The progress of the flash memory programming can be monitored by the Ready/Busy# output signal. P3.3 is driven low, sometime after ALE/PROG# goes low during a flash memory operation to indicate the Busy# status of the flash programming controller. P3.3 is driven high when the flash programming operation is completed to indicate the Ready status.

During a Burst-Program operation, P3.3 is driven high (Ready) in between each Byte-Program to indicate the ready status to receive the next byte. When the external host detects the Ready status after a byte among the burst is programmed, it may then put the data/address (in the same page) of the next byte on the bus and drive ALE/PROG# low (pulse) immediately, before the 20 µs time-out limit expires.

Data# Polling (P0.7)

SST89F54/58 also feature Data# Polling to indicate the flash memory programming operation status. The true data will be read from P0.7 via a Byte-Verify flash operation, which can be asserted immediately after the initiation of a Byte-Program or Burst-Program operation.

The operational sequence is as follows:

1. A Byte-Program or Burst-Program write operation is initiated.
2. The software immediately issues a Byte-Verify command, which internally writes the Data# Polling bit to P0.7.
3. The Data# Polling bit content initially shows the complements of the data programmed in Step 1 which indicates the Busy status of the flash block. When the Program operation completes, then true data will appear at P0.7, which indicates the Ready status of the flash block.
4. Repeat Steps 1 to 3 for additional flash operations.

Flash Memory Programming with External Host Mode (Figures 7-13)

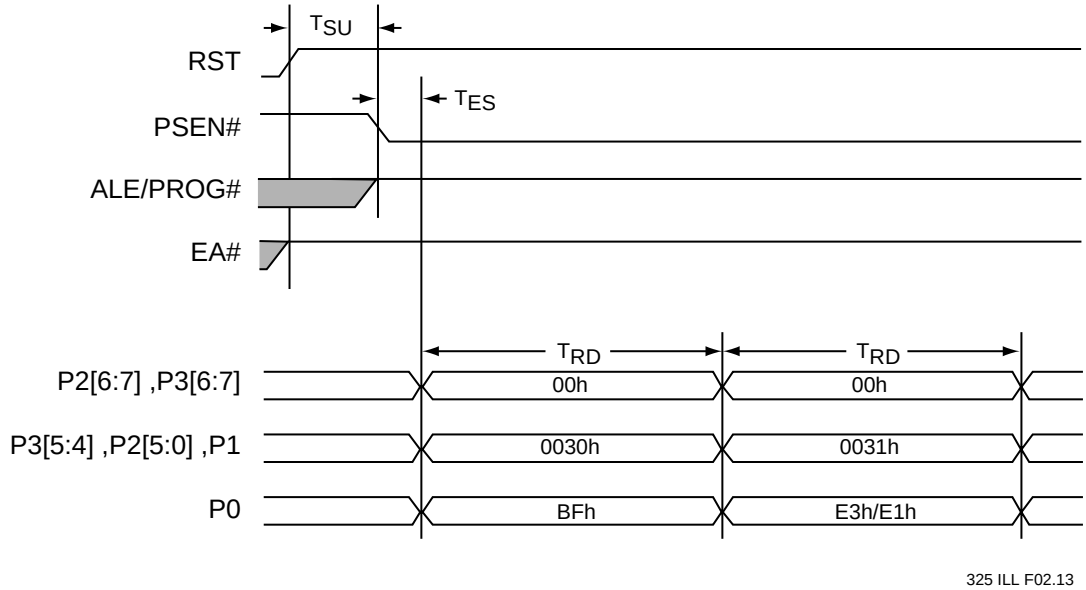


FIGURE 7: READ-ID
Read chip signature and identification registers at the addressed location.

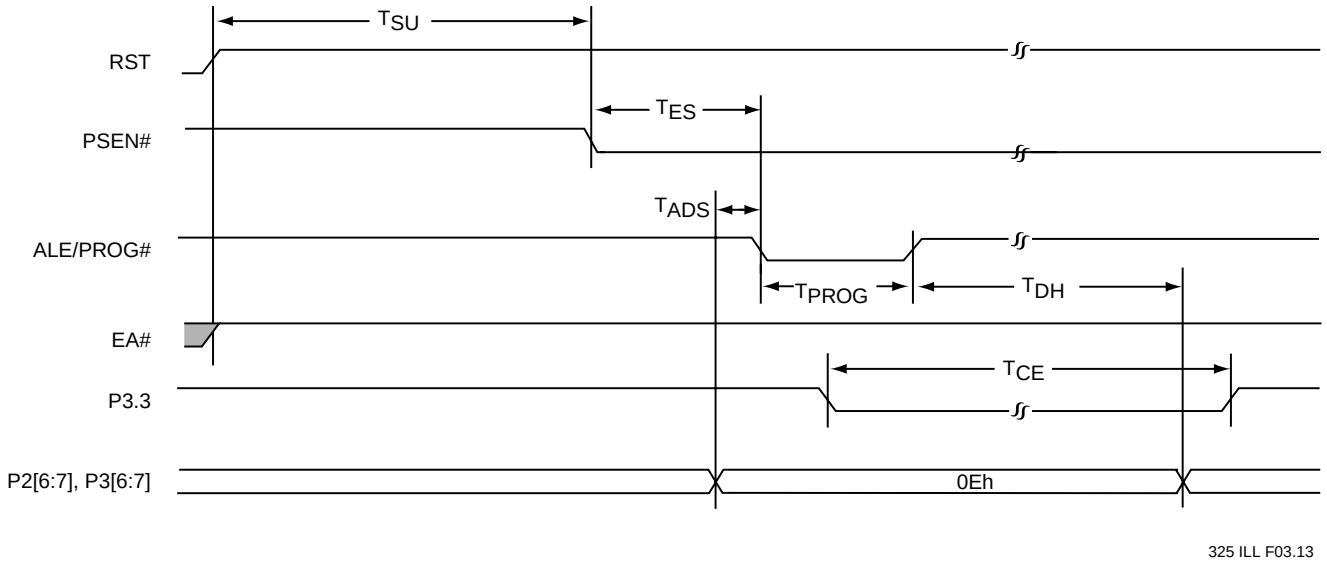


FIGURE 8: CHIP-ERASE
Erase both flash memory blocks. Security lock is ignored and the security byte is erased too.

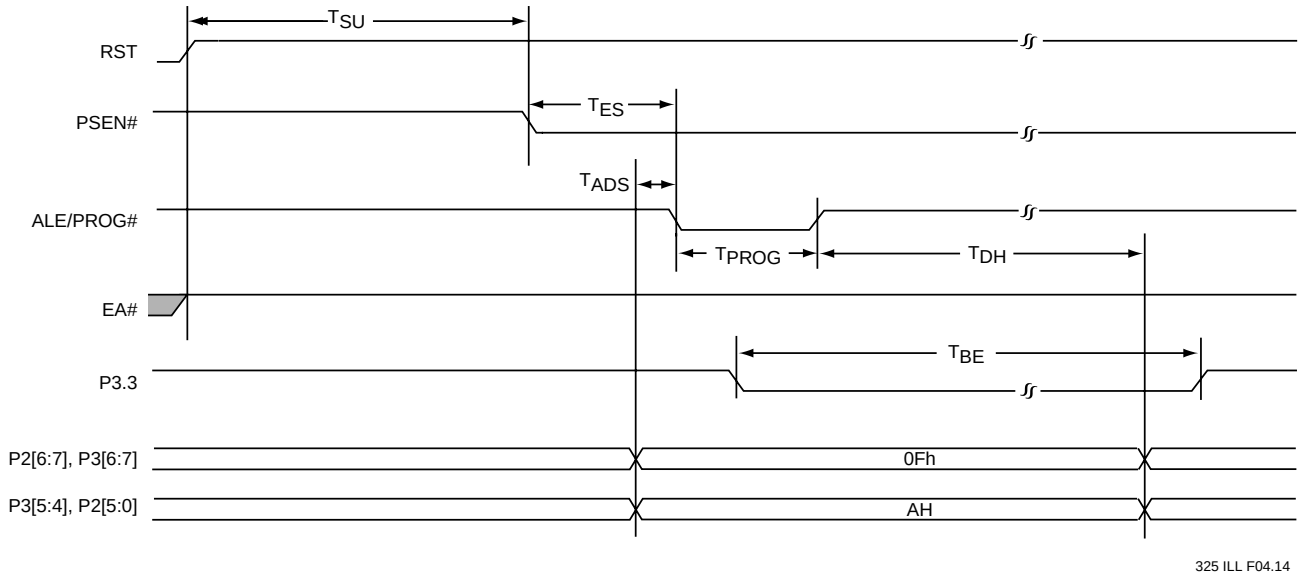


FIGURE 9: BLOCK-ERASE
Erase one of the flash memory blocks, if the security lock is not activated on that flash memory block. The high address byte determines which block is erased. For example, if AH = 0Xh, primary flash memory block is erased.

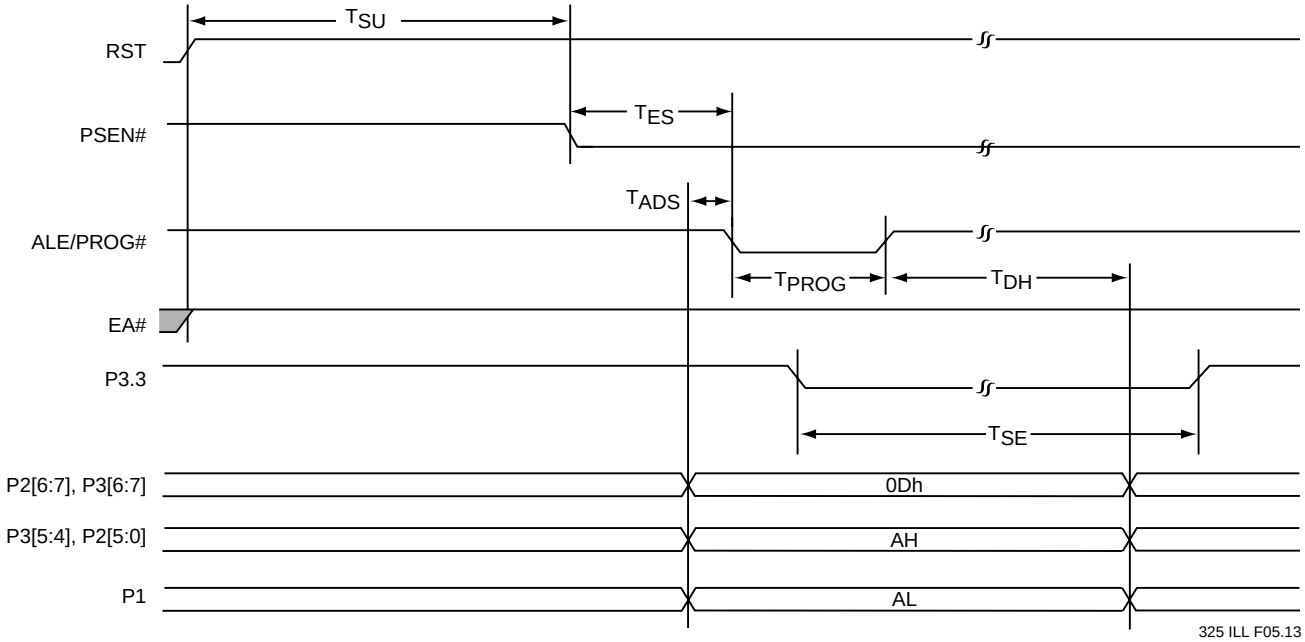


FIGURE 10: SECTOR-ERASE
Erase the addressed sector if the security lock is not activated on that flash memory block.

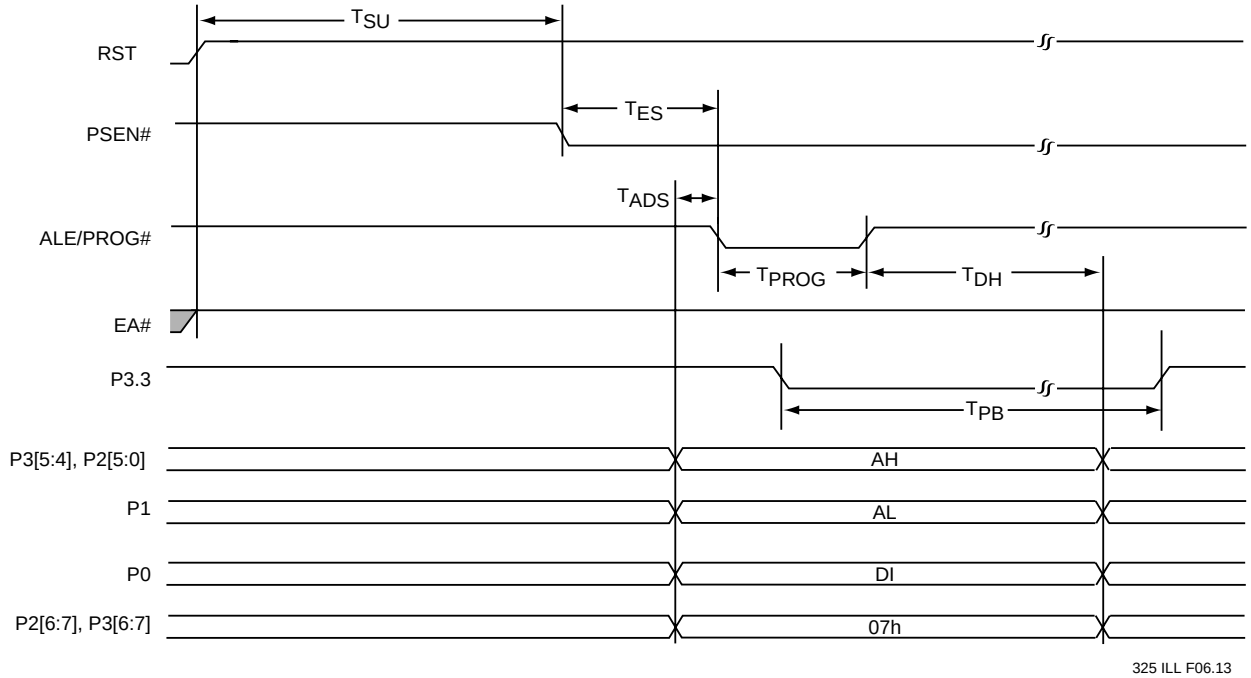


FIGURE 11: BYTE-PROGRAM
Program the addressed code byte if the byte location has been successfully erased and not yet programmed. This operation is only allowed when the security lock is not activated on that flash memory block.

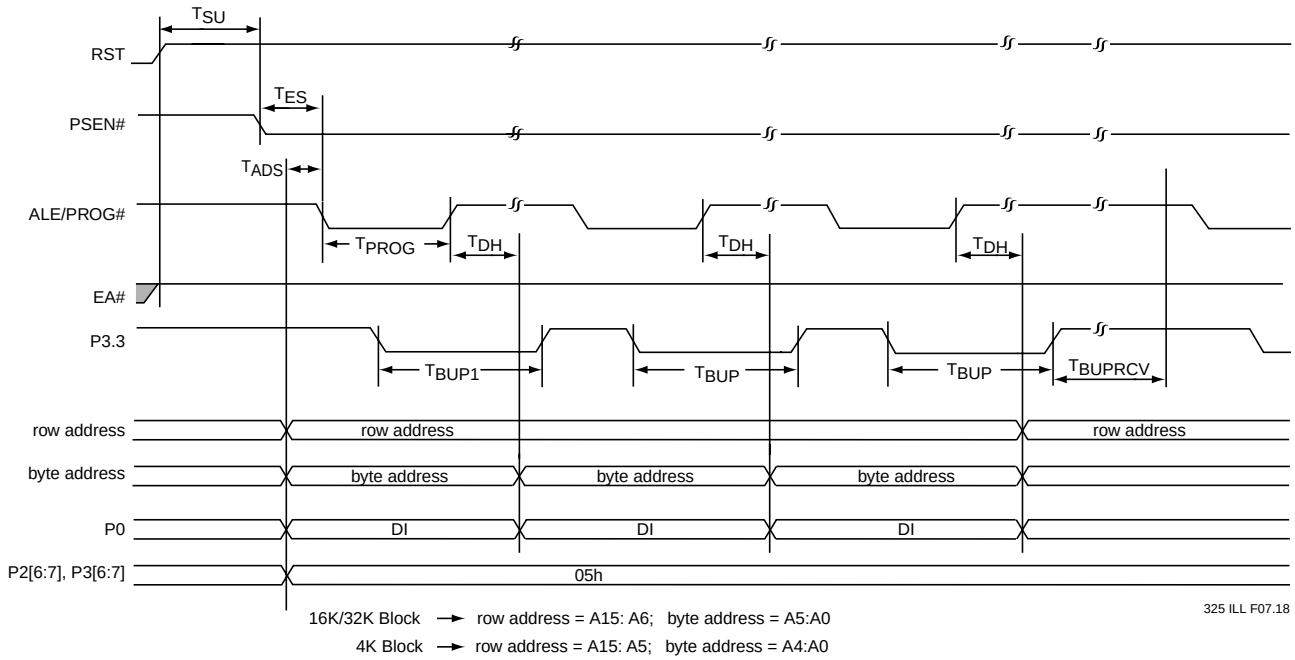


FIGURE 12: BURST-PROGRAM

Program the entire addressed row by burst programming each byte sequentially within the row if the byte location has been successfully erased and not yet programmed. This operation is only allowed when the security lock is not activated on that flash memory block.

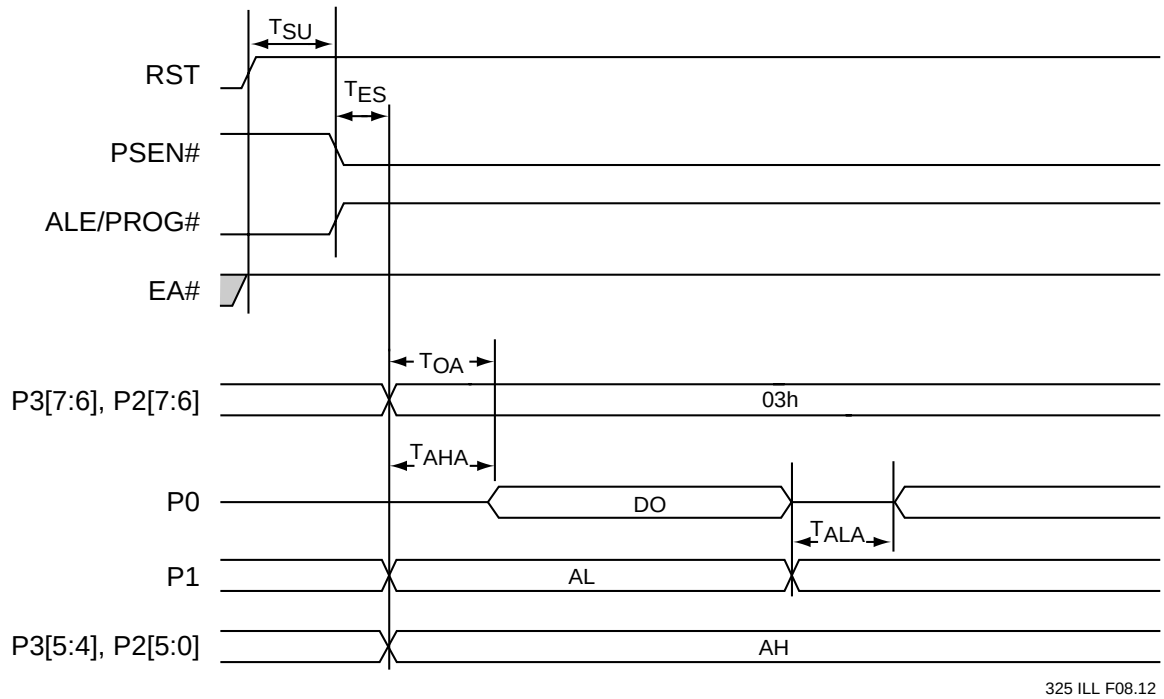


FIGURE 13: BYTE-VERIFY

Read the code byte from the addressed flash memory location if the security lock is not activated on that flash memory block.

IN-APPLICATION PROGRAMMING MODE

The SST89F54/58 offers 20/36 KByte of in-application reprogrammable flash memory. During In-Application Programming, the CPU of the microcontroller enters IAP Mode. The two blocks of flash memory allows the CPU to concurrently execute user code from one block, while the other is being reprogrammed. The CPU may also fetch code from an external memory while all internal flash is being reprogrammed. The chip can start the In-Application Programming operation either with the external program code execution being enabled (EA# = L) or disabled (EA#=H). The mailbox registers (SFCM, SFAL, SFAH, SFDT and SFCF) located in the Special Function Register (SFR), control and monitor the device's erase and program process.

SST SuperFlash EEPROMs are single power supply reprogrammable nonvolatile memories intended to be altered in-system with the use of one power supply. Similar to SRAMs, there exists the possibility of unintentional writes. The security lock prevents inadvertent alteration of data and code stored in the flash memory. **In order to assure the preservation of data integrity, it is required that the device remains locked at all times.**

There are six (6) IAP commands which can be issued via the command mailbox register, SFCM at SFR location FBh. A pair of mailbox register addresses the memory array of the SuperFlash blocks: SFAL, low order address at SFR location F9h, and SFAH, the high order address at SFR location FAh. Data is latched through the SFDT register at SFR location F8h. SFCF, the configuration/status register at SFR location F7h, provides security lock status and program counter visibility to the secondary flash memory block. The list in Table 6 outlines all the commands and their associated bit settings of the mailbox registers.

In-Application Programming Mode Commands

All of the following commands can only be initiated in the IAP Mode. In all situations, writing a command to the (SFCM) register will initiate all of the operations. All commands (except Chip-Erase) will be ignored if the selected memory block is security locked. The critical timing for all Erase and Program commands is dependent upon the minimum frequency pre-scaling factor specified in the SuperFlash Configuration/Status Register (SFCF[2:0]).

IAP Complete Command

To exit IAP mode and return the device to normal code execution (except when using the Chip-Erase command), an "IAP Complete" command must be issued. The IAP complete command is "MOV SFCM, #00h".

Chip-Erase

The Chip-Erase command erases both memory blocks (16/32 KByte and 4 KByte). This command ignores the security lock status and will erase the Security Byte. The Chip-Erase command is initiated as follows:

1.) Set the operational frequency pre-scaling factor FREQ in (SFCF[2:0]).
2.) Move 55h to the SuperFlash Data Register (SFDT), "MOV SFDT, #55h", where SFDT is the register address. This serves as a dual level precautionary measure to prevent accidental chip erasure.
3.) Move the Chip-Erase command to the SuperFlash Command Register (SFCM), "MOV SFCM, #87h" *or* "MOV SFCM, #07h". If SFCM[7] is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll SFCF[3] to determine when the erase is complete.

Block-Erase

The Block-Erase command erases one of the two memory blocks (16/32 KByte or 4 KByte). The selection of the memory block to be erased is determined by AH (SFAH) of the SuperFlash Address Register. If SFAH is a "0Xh", the primary flash memory block is selected (16/32K). If SFAH is a "FXh", the secondary flash memory block (4K) is selected. The Block-Erase command is initiated as follows:

1.) Set the operational frequency pre-scaling factor FREQ in SFCF[2:0].
2.) Move the block address to SFAH, "MOV SFAH, #F0h" *or* "MOV SFAH, #00h".
3.) Move 55h to the SuperFlash Data Register (SFDT), "MOV SFDT, #55h" where SFDT is the register address. This serves as a dual level precautionary measure to prevent accidental erasure.
4.) Move the Block-Erase command to SFCM, "MOV SFCM, #FFh" *or* "MOV SFCM, #0Fh". If SFCM[7] is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the SFCF[3] register to determine when the erase is complete.
5.) If this is the last command in the IAP set use IAP complete command, "MOV SFCM, #00h" to exit IAP mode.

Sector-Erase

The Sector-Erase command erases a sector. The sector size for the primary flash memory (Address locations 0-3FFFh/7FFFh) is 128 Bytes. The sector size for the secondary flash memory (Address locations F000h-FFFFh) is 64 Bytes. The Sector-Erase command is initiated as follows:

1.) Set the operational frequency pre-scaling factor FREQ in SFCF[2:0].
2.) Move the sector address to SFAH and to SFAL.
3.) Move the Sector-Erase command to SFCM, "MOV SFCM, #8Bh" *or* "MOV SFCM, #0Bh". If SFCM[7] is set, INT1# will interrupt the system when the erase is complete. Otherwise you must poll the SFCF[3] register to determine when the erase is complete.
4.) If this is the last command in the IAP set use IAP complete command, "MOV SFCM, #00h" to exit IAP mode.

The following Program command is for programming new data into the memory array. The portion of the memory array to be programmed should be in the erased state, FFh. If the memory is not erased, then erase it with the appropriate Erase command. WARNING: do not write (program or erase) to a block that the code is currently fetching from. This can "hang" the CPU and may even corrupt program data as it is being executed.

Byte-Program

The Byte-Program command programs data into a single byte. The Byte-Program command is initiated as follows:

1.) Set the operational frequency pre-scaling factor FREQ in (SFCF[2:0]).
2.) Move the high order address byte AH to SFAH.
3.) Move the low order address byte AL to SFAL.
4.) Move the data to the SFDT.
5.) Move the Byte-Program command to SFCM, "MOV SFCM, #8Eh" *or* "MOV SFCM, #0Eh". If SFCM[7] is set, INT1# will interrupt the system when the program is complete. Otherwise you must poll the SFCF[3] register to determine when the program is complete.
6.) If this is the last command in the IAP set use IAP complete command, "MOV SFCM, #00h" to exit IAP mode.

Byte-Verify

The Byte-Verify command allows the user to verify that the SST89F54/58 has correctly performed an Erase or Program command. The Byte-Verify command is initiated as follows:

1.) Set the operational frequency pre-scaling factor FREQ in (SFCF[2:0]).
2.) Move the high order address byte AH to SFAH.
3.) Move the low order address byte AL to SFAL.
4.) Move the Byte-Verify command to SFCM, "MOV SFCM, #0Ch".
5.) If this is the last command in the IAP set use IAP complete command, "MOV SFCM, #00h" to exit IAP mode.

Polling

A command that uses the polling method to signify the completion of an operation must check the BUSY bit (SFCF[3]). Copy the SFST register into temporary memory and mask the bit. Once it is isolated, the status of the BUSY bits can be checked.

MOVC instruction may also be used for verification of the Programming and Erase operation of the flash memory.

TABLE 6: IN-APPLICATION PROGRAMMING MODE COMMANDS

Operation	SFAH [7:0]	SFAL [7:0]	SFDT [7:0]	SFCM [7:0]
Chip-Erase	X	X	55h	87h/07h
Block-Erase	FXh/0Xh	X	55h	8Fh/0Fh
Sector-Erase	AH	AL	X	8Bh/0Bh
Byte-Program	AH	AL	DI	8Eh/0Eh
Byte-Verify	AH	AL	DO	0Ch
IAP Complete	X	X	X	00h

Notes: X = Don't Care; AL = Address low order byte; AH = Address high order byte; DI = Data Input; DO = Data Output

325 PGM T5.17

TABLE 7: FLASH MEMORY PROGRAMMING/VERIFICATION PARAMETERS

Parameter[1,2]	Symbol	4 MHz		8 MHz		Units
		Min	Max	Min	Max	
Programming Clock		250		125		ns
Reset Setup Time	T_{SU}	6		3		µs
Read-ID Command Width	T_{RD}		500		250	ns
PSEN# Setup Time	T_{ES}	2.25		1.125		µs
Address, Command, Data Setup Time	T_{ADS}	250		125		ns
Chip-Erase Time	T_{CE}	8.5		4.3		ms
Block-Erase Time	T_{BE}	8.5		4.3		ms
Sector-Erase Time	T_{SE}	2.2		1.1		ms
Program Setup Time	T_{PROG}	1.8		0.9		ms
Address, Command, Data Hold	T_{DH}	0		0		ns
Byte-Program Time [3]	T_{PB}	194		97		µs
Verify Command Delay Time	T_{OA}		45		45	ns
Verify High Order Address Delay Time	T_{AHA}		45		45	ns
Verify Low Order Address Delay Time	T_{ALA}		45		45	ns
First Burst-Program Byte Time[5]	T_{BUP1}	174	214	87	107	µs
Burst-Program Time [3,4,5]	T_{BUP}	62	102	31	51	µs
Burst-Program Recovery[5]	T_{BUPRCV}		70		35	µs
Read Setup Time	T_{RS}	1.25		0.63		µs

325 PGM T4.20

Note:

1. Program and Erase times will scale inversely relative to programming clock frequency.
2. All timing measurements are from the 50% of the input to 50% of the output.
3. Each byte must be erased before program.
4. The maximum time includes a 20µs Burst-Program time-out limit.
5. External Host Mode only.

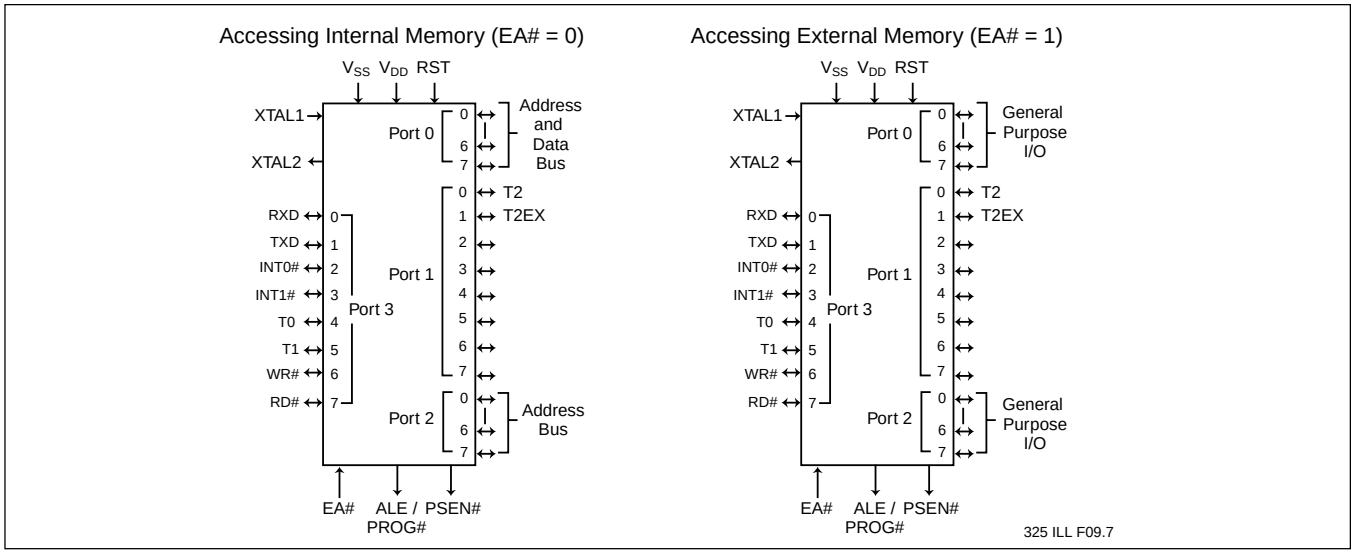


FIGURE 14: IN-APPLICATION PROGRAMMING MODE I/O ASSIGNMENT

WATCHDOG TIMER

The SST89F54/58 offer an enhanced programmable watchdog timer for fail safe protection against software "hang" and allows an automatic recovery from such software upset.

To protect the system against software "hang", the user's program has to refresh the watchdog timer within a previously programmed time period. If the software fails to do this periodical refresh, an internal hardware reset will be initiated. The software can be designed such that the watchdog times out if the program does not work properly. It also times out if a software error is based on the hardware related problems.

The watchdog timer in the SST89F54/58 share the same time base with the flash controller unit. When the flash controller unit is operating, the time base will be re-started by the hardware periodically, hence elongate the time-out period of the watchdog timer. The most significant 8-bits of the time base register are used as the reload register of the watchdog timer.

Figure 15 provides a block diagram of the Watchdog Timer. Two SFRs (WDTC and WDTD) control watchdog timer operation. During idle mode, WDT operation is temporarily suspended, and resumes upon an interrupt exit from idle. More specific information about the Watchdog Timer operation can be found in the ***User's Manual***.

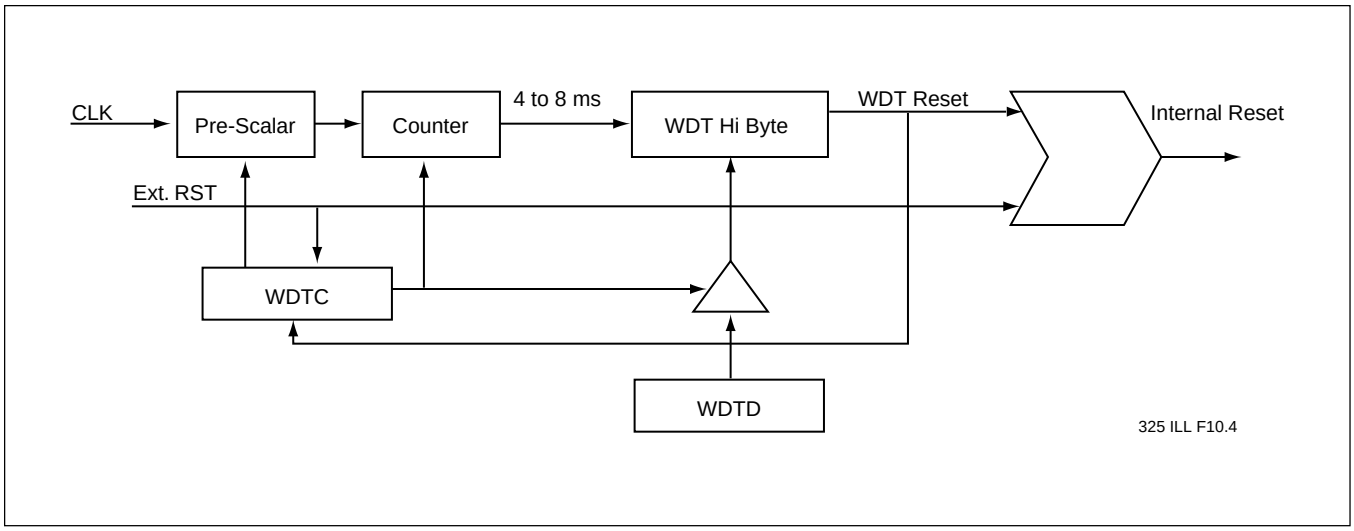


FIGURE 15: BLOCK DIAGRAM OF PROGRAMMABLE WATCHDOG TIMER

SECURITY LOCK

The Security feature protects against software piracy and prevents the contents of the flash from being read by unauthorized parties. It also protects against code corruption resulting from accidental erasing and programming to the internal flash memory locations. The security bits are located in the highest address location, FFFFh, of the SST89F54/58 program memory space. Table 9 lists the security lock options and commands allowed for each option. The three lock options are:

- Hard Lock
- Block 1 Lock
- SoftLock™

Hard Lock and Block 1 Lock

When the security lock is activated, the MOVC instructions executed from external program memory or flash memory are disabled from fetching code bytes from unlocked memory blocks (See Table 8). The security lock can either “hard” lock both flash memory blocks or just “hard” lock the upper flash memory block (Block 1) independently. When the memory blocks are locked, the following commands are not allowed on the locked flash memory blocks:

- Sector-Erase
- Block-Erase
- Byte-Program
- Burst-Program
- Byte-Verify

SoftLock

SoftLock allows flash contents to be altered under a secure environment. This lock option allows the user to update program code in the Block 0 (16K/32K) through In-Application Programming Mode under a pre-determined secure environment. The Block 1 (4K) memory block is hard locked, but the Block 0 (16K/32K) memory block is “soft” locked, which allows code residing in Block 1 to program Block 0. The following IAP mode commands issued through the command mailbox register, SFCM, executed from Block 1 can be operated on Block 0: Block-Erase, Sector-Erase, Byte-Program and Byte-Verify.

While in External Host Mode, the results of a SoftLock are the same as a HardLock.

ACTIVATION AND DEACTIVATION OF THE SECURITY LOCK

For both External Host and In-Application Programming modes, the security byte, 55h, F5h or 05h, must first be programmed into the address location FFFFh using the Byte or Burst-Program operation. After the security byte has been programmed into address location FFFFh, the security lock is activated following a successful system reset.

All values for security byte other than FFh, 00h, F5h, and 05h default to hard lock.

To deactivate the security lock, the security byte at location FFFFh is erased to a value of, FFh/00h, via the Chip-Erase operation. The default value of the security byte is FFh. (Chip-Erase will erase all the flash blocks data).

TABLE 8: INTERNAL AND EXTERNAL PROGRAM MEMORY ACCESS WITH SECURITY LOCK ACTIVATED FOR HARD LOCK AND BLOCK 1 LOCK

MOVC INSTRUCTIONS EXECUTED FROM	ACCESS TO LOCKED PROGRAM MEMORY	ACCESS TO UNLOCKED OR EXTERNAL PROGRAM MEMORY
locked program memory	YES	YES
unlocked or external program memory	NO	YES

TABLE 9: SECURITY LOCK OPTIONS (IN-APPLICATION PROGRAMMING MODE)

Sec Byte	SFCF [6:5]	EA#	Blk Sel	Block-Erase	Sector-Erase	Byte-Program	Byte-Verify	Description
FF/00h	00	X	X	Y	Y	Y	Y	No lock
55h	11	X	X	N	N	N	N	Hard lock
F5h	01	X	0	Y	Y	Y	Y	Block 1 (4KB) lock
		X	1	N	N	N	N	
05h	10	0	X	N	N	N	N	SoftLock™
		1	0	Y	Y	Y	Y	
		1	1	N	N	N	N	

325 PGM T6.15

NOTE: **SecByte** = Value of Security Byte at location FFFFh; **SFCF(6:5)** = Bit 5 and 6 of SFCF register; **EA#** = Ext. Access enable input pin: 1 – running code from internal memory, 0 – running code from external enable; **BlkSel** = Block Select signal (internal): 1 – block 1 (4Kx8), 0 – block 0 (32Kx8); **X** = don’t care; **Y** = command allowed; **N** = command not allowed.

TABLE 9: (CONTINUED) SECURITY LOCK OPTIONS (EXTERNAL HOST MODE)

Sec Byte	SFCF [6:5]	EA#	Blk Sel	Block-Erase	Sector-Erase	Byte-Program	Burst-Program	Byte-Verify	Description
FF/00h	00	1	X	Y	Y	Y	Y	Y	No Lock
55h	11	X	X	N	N	N	N	N	Hard Lock
F5h	01	X	0	Y	Y	Y	Y	Y	Block 1 (4KB) Lock
		X	1	N	N	N	N	N	
05h	10	X	X	N	N	N	N	N	SoftLock™

NOTE: **SecByte** = Value of Security Byte at location FFFFh; **SFCF(6:5)** = Bit 5 and 6 of SFCF register; 325 PGM T6.15
EA# = Ext. Access enable input pin: 1 – running code from internal memory, 0 – running code from external enable;
BlkSel = Block Select signal (internal): 1 – block 1 (4Kx8), 0 – block 0 (32Kx8); **X** = don't care; **Y** = command allowed;
N = command not allowed.

SYSTEM DESIGN CONSIDERATIONS

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 5 cm of the V_{DD} pin. If you use a socket for programming purposes add an additional 1-10 µF next to each socket.

RESET (Hardware)

A system reset initializes the MCU and begins program execution at program memory location 0000h. The reset input for the SST89F54/58 is the RST pin. In order to reset the SST89F54/58, a logic level high must be applied to the RST pin for at least two machine cycles (24 clocks), after the oscillator becomes stable. ALE, PSEN# are weakly pulled high during reset. During reset, ALE and PSEN# output a high level in order to perform a correct reset. This level must not be affected by external element. A system reset will not affect the 256 Bytes of on-chip RAM while the SST89F54/58 is running, however, the contents of the on-chip RAM during power up are indeterminate. All Special Function Registers (SFR) return to their reset values, which are outlined in Tables 3A to 3E.

Power-On Reset

At initial power up, the port pins will be in a random state until the oscillator has started and the internal reset algorithm has written one's to all the pins. Powering up the device without a valid reset could cause the CPU to start executing instructions from an indeterminate location. **Such undefined states may inadvertently corrupt the code in the flash.**

When power is applied to the SST89F5x, the RST pin must be held long enough for the oscillator to start up (usually several milliseconds for a low frequency crystal), in addition to two machine cycles for a valid Power-On Reset. An example of a method to extend the RST signal is to implement a RC circuit by connecting the RST pin to V_{DD} through a 10µF capacitor and to V_{SS} through an 8.2KΩ resistor as shown in Figure 16. Note that if an RC circuit is being used, provisions should be made to ensure the V_{DD} rise time does not exceed 1 millisecond and the oscillator start-up time does not exceed 10 milliseconds.

For a low frequency oscillator with slow start-up time the reset signal must be extended in order to account for the slow start-up time. This method maintains the necessary relationship between V_{DD} and RST to avoid programming at an indeterminate location, which may cause corruption in the code of the flash. For more information on system level design techniques, please review ***Design Considerations for the SST FlashFlex51 Family Microcontroller*** Application Note.

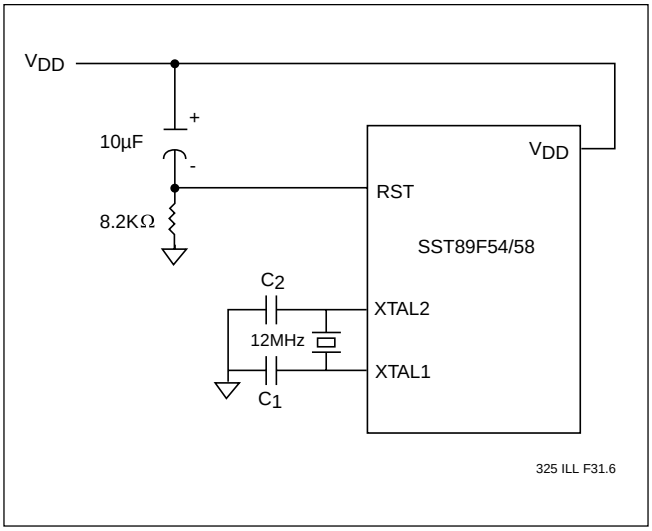


FIGURE 16: EXAMPLE POWER-ON RESET CIRCUIT

POWER-SAVING MODES

The FlashFlex51 Family of MCUs provide two power-saving modes of operation for applications where power consumption is critical. The two power-saving modes are Power Down and Standby (Stop Clock) modes. The Power Down and Standby (Stop Clock) modes are similar, both reduce device current drain to approximately 15 microamperes. However, entry to the two modes is different, Power Down mode is entered by software, while Standby (Stop Clock) mode is controlled by hardware (gating on and off the system clock). Table 10 below outlines the different power-saving modes, indicating entry and exit procedures and functionality within the MCU during the power-saving modes.

TABLE 10: FLASHFLEX51 POWER SAVING MODES

Mode	Initiated by	Current Drain	State of MCU	Exited by
Power Down Mode	Software (Set PD bit in PCON)	Approximately 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) power down mode.	CLK gated Off to MCU, serial port, timer/ counters and internal interrupts. On-chip SRAM and SFR data is maintained. ALE and PSEN# signals at a LOW level during Power Down.	Hardware reset. A hardware reset starts the device similar to power-on reset.
Standby (Stop Clock) Mode	External hardware gates OFF the external clock input to the MCU. This gating shall be synchronized with an input clock transition (low-to-high or high-to-low).	Approximately 15 microamps. And V_{DD} can be reduced by ext. hardware to 2V during (after entry and before exit) power down mode.	Internal state of the MCU is totally pre-served.	Gate ON external clock, and begin executing at next clock in normal processing.

325 PGM T8.4

Note: 1. Normal processing refers to program execution beginning at the instruction following the one that invoked this particular power reduction mode.

CLOCK INPUT OPTIONS

Shown in Figure 17 are the input and output of an internal inverting amplifier (XTAL1, XTAL2), which can be configured for use as an on-chip oscillator.

When driving the device from an external clock source, XTAL2 should be left disconnected and XTAL1 should be driven.

At start-up, the external oscillator may encounter a higher capacitive load at XTAL1 due to interaction between the amplifier and its feedback capacitance. However, the capacitance will not exceed 15 pF once the external signal meets the V_{IL} and V_{IH} specifications.

Recommended Capacitor Values for Crystal Oscillator

Crystal manufacturer, supply voltage, and other factors may cause circuit performance to differ from one application to another. C1 and C2 should be adjusted appropriately for each design. The table below, shows the typical values for C1 and C2 at a given frequency. If, following the satisfactory selection of all external components, the circuit is still over driven, a series resistor, R_S, may be added.

RECOMMENDED VALUES FOR CRYSTAL OSCILLATOR

Frequency	C1 and C2	R_S (Optional)
< 8 MHz	90-110 pF	100Ω
8-12 MHz	18-22 pF	200Ω
>12 MHz	18-22 pF	200Ω

More specific information on On-Chip oscillator design can be found in ***SST89F5x Oscillator Circuit Design Considerations*** Application Note.

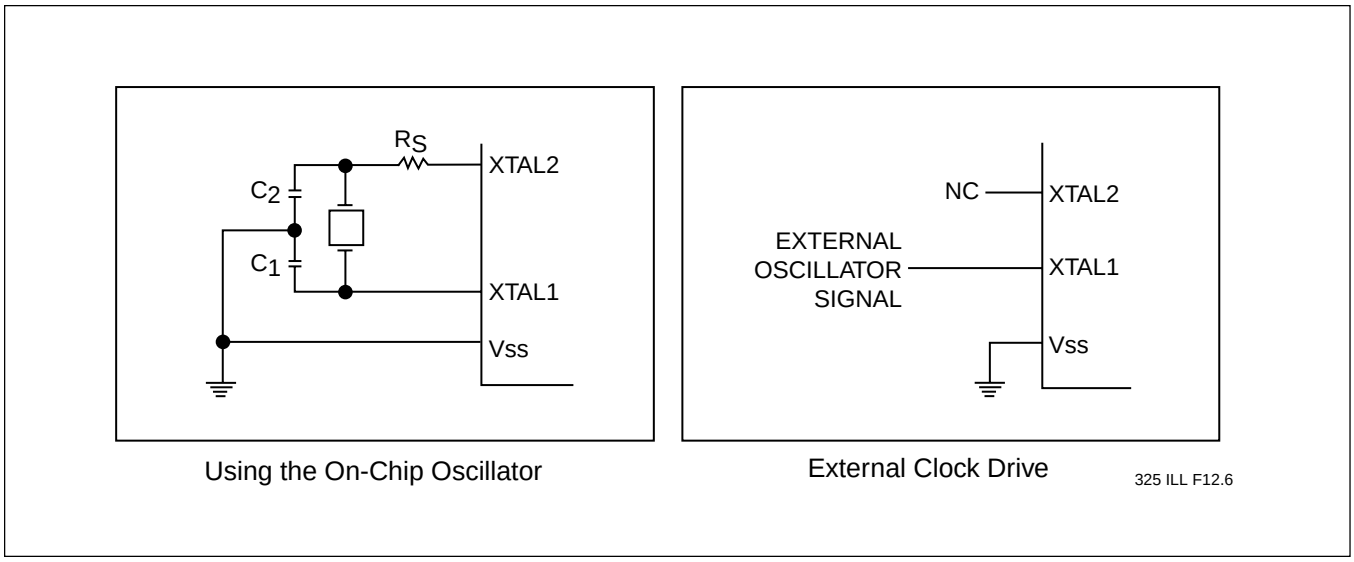


FIGURE 17: CLOCK INPUT OPTIONS

Preliminary Specifications

ELECTRICAL SPECIFICATION

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Ambient Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to + 150°C
Voltage (V_H) on EA# Pin to V_{SS} ..... -0.5V to +14.0V
Transient Voltage (<20ns) on Any Other Pin to V_{SS} ..... -1.0V to +6.5V
Maximum I_{OL} per I/O Pins P1.5, P1.6, P1.7 ..... 20 mA
Maximum I_{OL} per I/O for All Other Pins ..... 15 mA
Package Power Dissipation Capability (T_A = 25°C) 1.5W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current[1] ..... 100 mA

Note [1] Outputs shorted for no more than one second. No more than one output shorted at a time.
(Based on package heat transfer limitations, not device power consumption.)

NOTICE: This specification contains preliminary information on new products in production. The specifications are subject to change without notice.

Operation Range

TABLE 11: OPERATING RANGE

Symbol	Description	Min.	Max	Unit
T_A	Ambient Temperature Under Bias			
	Standard	0	+70	°C
	Industrial	-40	+85	°C
V_{DD}	Supply Voltage	2.7	5.5	V
f_{OSC}	Oscillator Frequency	0	33	MHz
	For In-Application Programming	0.25	33	MHz

325 PGM T10.1

TABLE 12: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}[1]	ESD Susceptibility Human Body Model	2000	Volts	JEDEC Standard A114
V_{ZAP_MM}[1]	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}[1]	Latch Up	100+I_{DD}	mA	JEDEC Standard 78

Note: [1]This parameter is measured only for initial qualification and after a design or process change that could affect this parameter. 325 PGM T11.2

TABLE 13A: DC ELECTRICAL CHARACTERISTICS

T_{AMB} = O°C TO + 70°C OR -40°C TO +85°C, 33MHZ DEVICES; 5V ±10%; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	4.5 < V_{DD} < 5.5	-0.5	0.2V_{DD} - 0.1	V
V_{IH}	Input High Voltage (ports 0,1,2,3)	4.5 < V_{DD} < 5.5	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	4.5 < V_{DD} < 5.5	0.7 V_{DD}	V_{DD} + 0.5	V
V_{OL2}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 4.5 V I_{OL} = 16 mA		1.0	V
V_{OL}	Output Low Voltage (Ports 1.0-1.4, 2, 3) [5]	V_{DD} = 4.5 V I_{OL} = 100 µA [1] I_{OL} = 1.6 mA [1] I_{OL} = 3.5 mA [1]		0.3 0.45 1.0	V V V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) [4,5]	V_{DD} = 4.5 V I_{OL} = 200 µA [1] I_{OL} = 3.2 mA [1]		0.3 0.45	V V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#) [2]	V_{DD} = 4.5 V I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA	 V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} – 1.5		 V V V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) [2]	V_{DD} = 4.5 V I_{OH} = -200 µA I_{OH} = -3.2 mA	 V_{DD} - 0.3 V_{DD} - 0.7		 V V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3.3-3.7)	V_{IN} = 0.4V	-1	-75	µA
I_{IL1}	Logical 0 Input Current (Ports 3.0, 3.1, 3.2)	V_{IN} = 0.4V	-1	-150	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) [3]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pulldown Resistor		40	225	kΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current [7] In-Application Programming Mode @ 12 MHz @ 33 MHz Active Mode @ 12 MHz @ 33 MHz Standby (Stop Clock) Mode Power Down Mode 	V_{DD} = 5V T_{amb} =0°C to + 70°C T_{amb} =-40°C to +85°C V_{DD} = 2V T_{amb} =0°C to + 70°C T_{amb} =-40°C to +85°C		 70 88 25 45 100 125 40 50	 mA mA mA mA µA µA µA µA

325 PGM T12A.5

TABLE 13B: DC ELECTRICAL CHARACTERISTICS

T_{AMB} = O°C TO + 70°C OR -40°C TO +85°C, 12 MHZ DEVICES; 3V ±10%; V_{SS} = 0V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	2.7 < V_{DD} < 3.3	-0.5	0.7	V
V_{IH}	Input High Voltage (ports 0,1,2,3)	2.7 < V_{DD} < 3.3	0.2 V_{DD} + 0.9	V_{DD} + 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.7 < V_{DD} < 3.3	0.7 V_{DD}	V_{DD} + 0.5	V
V_{OL2}	Output Low Voltage (Ports 1.5, 1.6, 1.7)	V_{DD} = 2.7 V I_{OL} = 10 mA		 1.0	 V
V_{OL}	Output Low Voltage (Ports 1.0-1.4, 2, 3) [5]	V_{DD} = 2.7 V I_{OL} = 100 µA [1] I_{OL} = 1.6 mA [1] I_{OL} = 3.5 mA [1]		 0.3 0.45 1.0	 V V V
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN#) [4,5]	V_{DD} = 2.7 V I_{OL} = 200 µA [1] I_{OL} = 3.2 mA [1]		 0.3 0.45	 V V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, PSEN#) [2]	V_{DD} = 2.7 V I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA	 V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} – 1.5		 V V V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) [2]	V_{DD} = 2.7 V I_{OH} = -200 µA I_{OH} = -3.2 mA	 V_{DD} - 0.3 V_{DD} - 0.7		 V V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3.3-3.7)	V_{IN} = 0.4V	-1	-75	µA
I_{IL1}	Logical 0 Input Current (Ports 3.0, 3.1, 3.2)	V_{IN} = 0.4V	-1	-150	µA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3) [3]	V_{IN} = 2V		-650	µA
I_{LI}	Input Leakage Current (Port 0)	0.45 < V_{IN} < V_{DD}-0.3		±10	µA
R_{RST}	RST Pulldown Resistor		40	225	kΩ
C_{IO}	Pin Capacitance[6]	@ 1 MHz, 25°C		15	pF
I_{DD}	Power Supply Current [7] In-Application Programming Mode Active Mode Standby (Stop Clock) Mode Power Down Mode	V_{DD} = 3 V T_{amb} =0°C to + 70°C T_{amb} =-40°C to +85°C V_{DD} = 2V T_{amb} =0°C to + 70°C T_{amb} =-40°C to +85°C		 70 22 70 88 40 50	 mA mA µA µA µA µA

325 PGM T12B.7

NOTES:

1. Capacitive loading on Ports 0 & 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and Ports 1 & 3. The noise due to external bus capacitance discharging into the Port 0 & 2 pins when the pins make 1 -to- 0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 & 2 may cause the V_{OH} on ALE and PSEN# to momentarily fall below the V_{DD} - 0.7 specification when the address bits are stabilizing.
3. Pins of Ports 1, 2 & 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin is approximately 2V.
4. Load capacitance for Port 0, ALE & PSEN#= 100pF, load capacitance for all other outputs= 80pF.
5. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum I_{OL} total for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
6. Pin capacitance is characterized but not tested. EA# is 25pF (max).
7. See Figures 18, 19 and 20 for test conditions. Minimum V_{DD} for Power Down is 2 V.

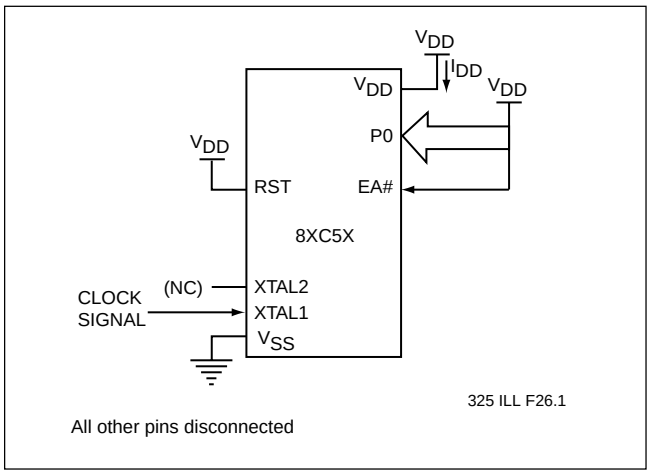


FIGURE 18: I_{DD} TEST CONDITION, ACTIVE MODE

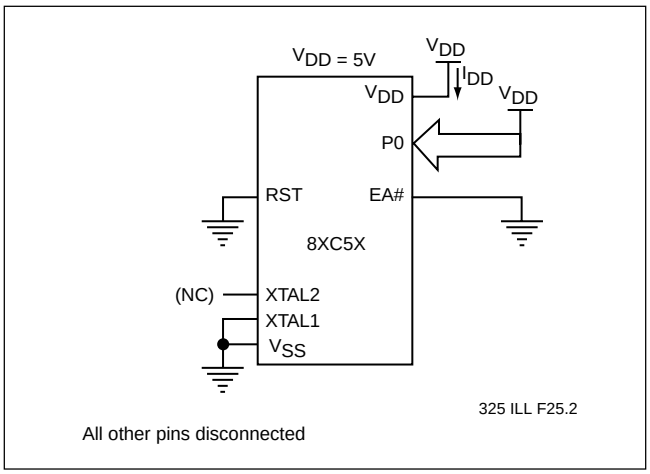


FIGURE 19: I_{DD} TEST CONDITION, STANDBY (STOP CLOCK) MODE

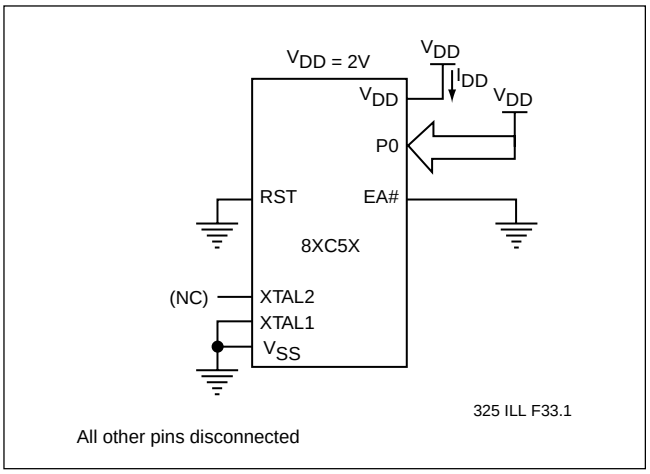


FIGURE 20: I_{DD} TEST CONDITION, POWER DOWN MODE

AC ELECTRICAL CHARACTERISTICS

AC Characteristics: (Over Operating Conditions; Load Capacitance for Port 0, ALE, and PSEN# = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

TABLE 14: AC ELECTRICAL CHARACTERISTICS

T_{AMB} = 0°C TO +70°C OR -40°C TO +85°C, V_{DD} = 3V ±10% @ 12 MHz, 5V ±10% @ 33 MHz, V_{SS} = 0

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
$1/T_{CLCL}$	Oscillator Frequency					0	33	MHz
T_{LHLL}	ALE Pulse Width	127		20		$2T_{CLCL}$ - 40		ns
T_{AVLL}	Address Valid to ALE Low	43		5		T_{CLCL} - 40 T_{CLCL} - 25		ns ns
T_{LLAX}	Address Hold After ALE Low	53		5		T_{CLCL} - 30 T_{CLCL} - 25		ns ns
T_{LLIV}	ALE Low to Valid Instr In		234		56		$4T_{CLCL}$ - 100 $4T_{CLCL}$ - 65	ns ns
T_{LLPL}	ALE Low to PSEN# Low	53		5		T_{CLCL} - 30 T_{CLCL} - 25		ns ns
T_{PLPH}	PSEN# Pulse Width	205		46		$3T_{CLCL}$ - 45		ns
T_{PLIV}	PSEN# Low to Valid Instr In		145		35		$3T_{CLCL}$ - 105 $3T_{CLCL}$ - 55	ns ns
T_{PXIX}	Input Instr Hold After PSEN#					0		ns
T_{PXIZ}	Input Instr Float After PSEN#		59		5		T_{CLCL} - 25 T_{CLCL} - 25	ns ns
T_{AVIV}	Address to Valid Instr In		312		71		$5T_{CLCL}$ - 105 $5T_{CLCL}$ - 80	ns ns
T_{PLAZ}	PSEN# Low to Address Float		10		10		10	ns
T_{RLRH}	RD# Pulse Width	400		82		$6T_{CLCL}$ - 100		ns
T_{WLWH}	Write Pulse Width (WE#)	400		82		$6T_{CLCL}$ - 100		ns
T_{RLDV}	RD# Low to Valid Data In		252		61		$5T_{CLCL}$ - 165 $5T_{CLCL}$ - 90	ns ns
T_{RHDX}	Data Hold After RD#	0		0		0		ns
T_{RHDZ}	Data Float After RD#		107		35		$2T_{CLCL}$ - 60 $2T_{CLCL}$ - 25	ns ns
T_{LLDV}	ALE Low to Valid Data In		517		150		$8T_{CLCL}$ - 150 $8T_{CLCL}$ - 90	ns ns
T_{AVDV}	Address to Valid Data In		585		180		$9T_{CLCL}$ - 165 $9T_{CLCL}$ - 90	ns ns
T_{LLWL}	ALE Low to RD# or WR# Low	200	300	40	140	$3T_{CLCL}$ - 50	$3T_{CLCL}$ + 50	ns
T_{AVWL}	Address to RD# or WR# Low	203		46		$4T_{CLCL}$ – 130 $4T_{CLCL}$ – 75		ns ns
T_{QVWX}	Data Valid to WR# Transition	33		0		T_{CLCL} - 50 T_{CLCL} - 30		ns ns
T_{WHQX}	Data Hold After WR#	33		3		T_{CLCL} - 50 T_{CLCL} - 27		ns ns
T_{QVWH}	Data Valid to WR# High	433		140		$7T_{CLCL}$ - 150 $7T_{CLCL}$ - 70		ns ns
T_{RLAZ}	RD# Low to Address Float		0		0		0	ns
T_{WHLH}	RD# or WR# High to ALE High	43	123	5	55	T_{CLCL} - 40 T_{CLCL} - 25	T_{CLCL} + 40 T_{CLCL} + 25	ns ns

325 PGM T13.6

AC CHARACTERISTICS

Explanation of Symbols

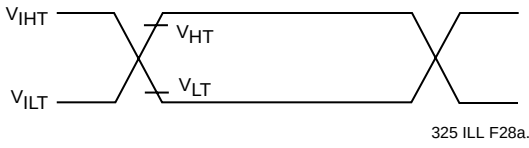
Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D Input data
H: Logic level HIGH
I: Instruction (program memory contents).
L: Logic level LOW or ALE
P: PSEN#
Q: Output data
R: RD# signal
T: Time
V: Valid
W: WR# signal
X: No longer a valid logic level
Z: High Impedance (Float)

For example:

T_{AVLL}=Time from Address Valid to ALE Low

T_{LLPL}=Time from ALE Low to PSEN# Low

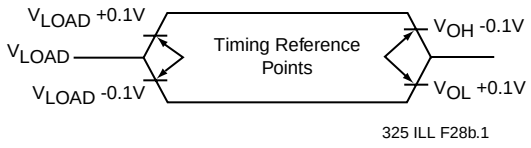


325 ILL F28a.2

AC Inputs during testing are driven at V_{IHT} (V_{DD} -0.5V) for Logic "1" and V_{ILT} (0.45V) for a Logic "0". Measurement reference points for inputs and outputs are at V_{HT} (0.2 V_{DD} + 0.9) and V_{LT} (0.2V_{DD} - 0.1)

Note: V_{HT}- V_{HIGH} Test
V_{LT}- V_{LOW} Test
V_{IHT}-V_{INPUT} HIGH Test
V_{ILT}- V_{INPUT} LOW Test

AC TESTING INPUT/OUTPUT



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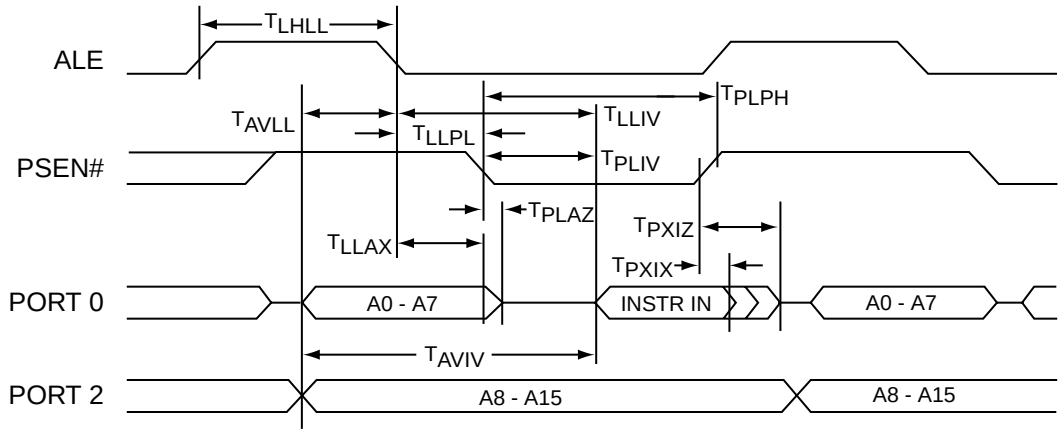
For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ± 20mA.

FLOAT WAVEFORM

FIGURE 21: AC TESTING INPUT/OUTPUT, FLOAT WAVEFORM



325 ILL F13.7

FIGURE 22: EXTERNAL PROGRAM MEMORY READ CYCLE

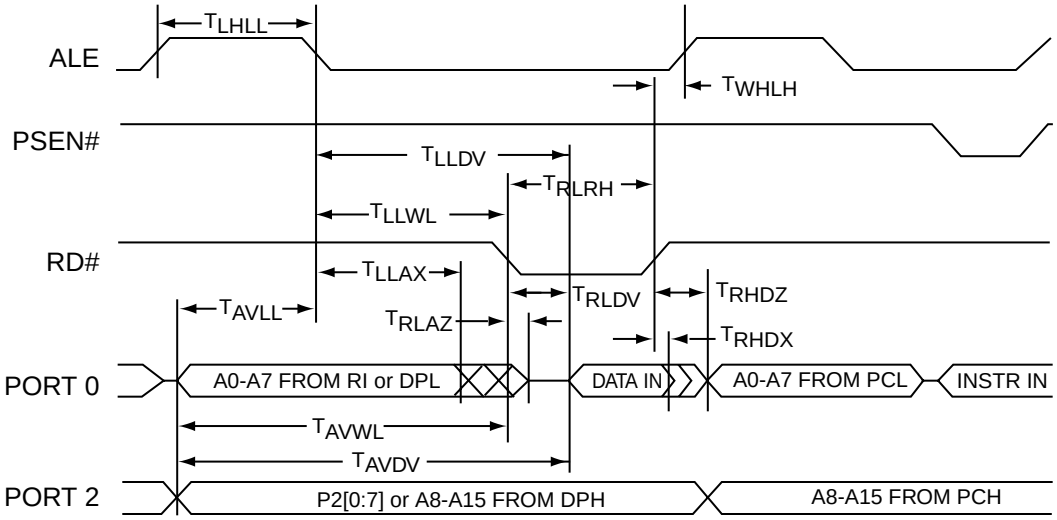


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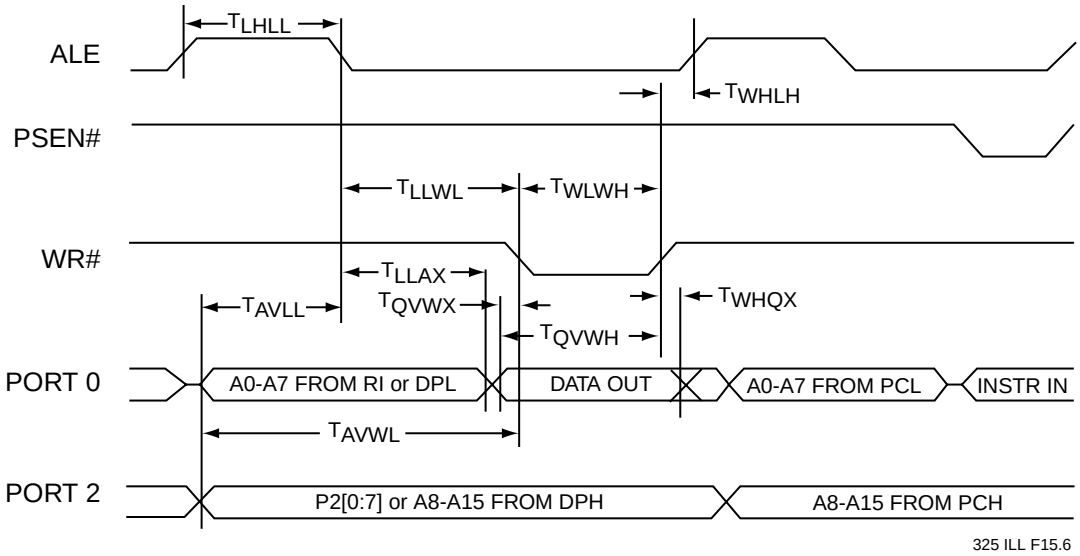
FIGURE 23: EXTERNAL DATA MEMORY READ CYCLE



325 ILL F15.6

FIGURE 24: EXTERNAL DATA MEMORY WRITE CYCLE

TABLE 15: EXTERNAL CLOCK DRIVE

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
$1/T_{CLCL}$	Oscillator Frequency					0	33	MHz
T_{CHCX}	High Time					$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCX}	Low Time					$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
T_{CLCH}	Rise Time		20		5			ns
T_{CHCL}	Fall Time		20		5			ns

325 PGM T14.4

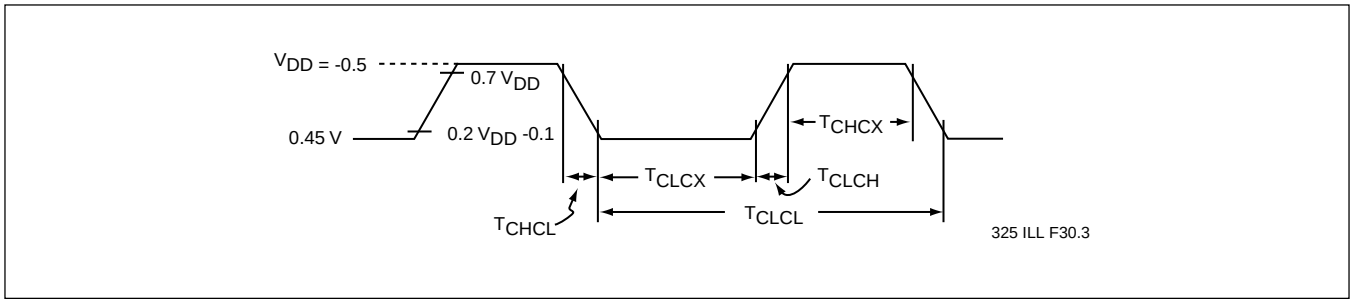


FIGURE 25: EXTERNAL CLOCK DRIVE WAVEFORM

TABLE 16: SERIAL PORT TIMING

Symbol	Parameter	Oscillator						Units
		12 MHz		33 MHz		Variable		
		Min	Max	Min	Max	Min.	Max.	
T_{XLXL}	Serial Port Clock Cycle Time	0		0.36		$12T_{CLCL}$		ms
T_{QVXH}	Output Data Setup to Clock Rising Edge	700		167		$10T_{CLCL}$ - 133		ns
T_{XHQX}	Output Data Hold After Clock Rising Edge	50		10		$2T_{CLCL}$ - 117 $2T_{CLCL}$ - 50		ns ns
T_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		167		$10T_{CLCL}$ - 133	ns

325 PGM T15.2

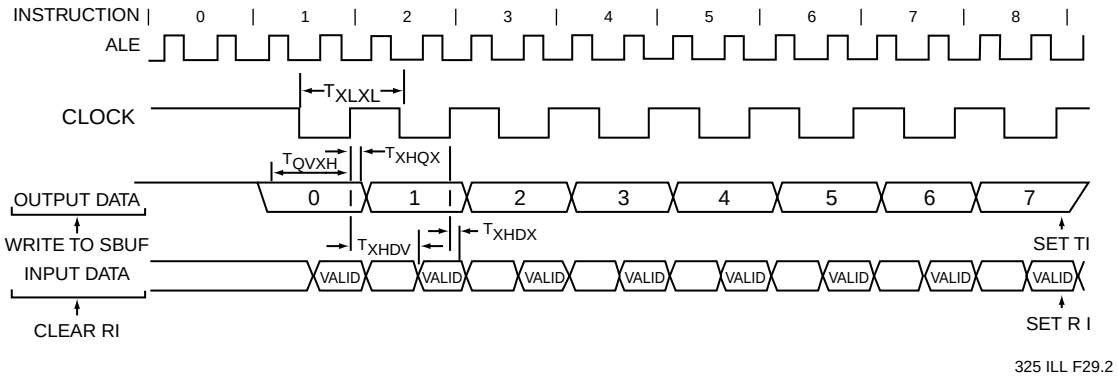
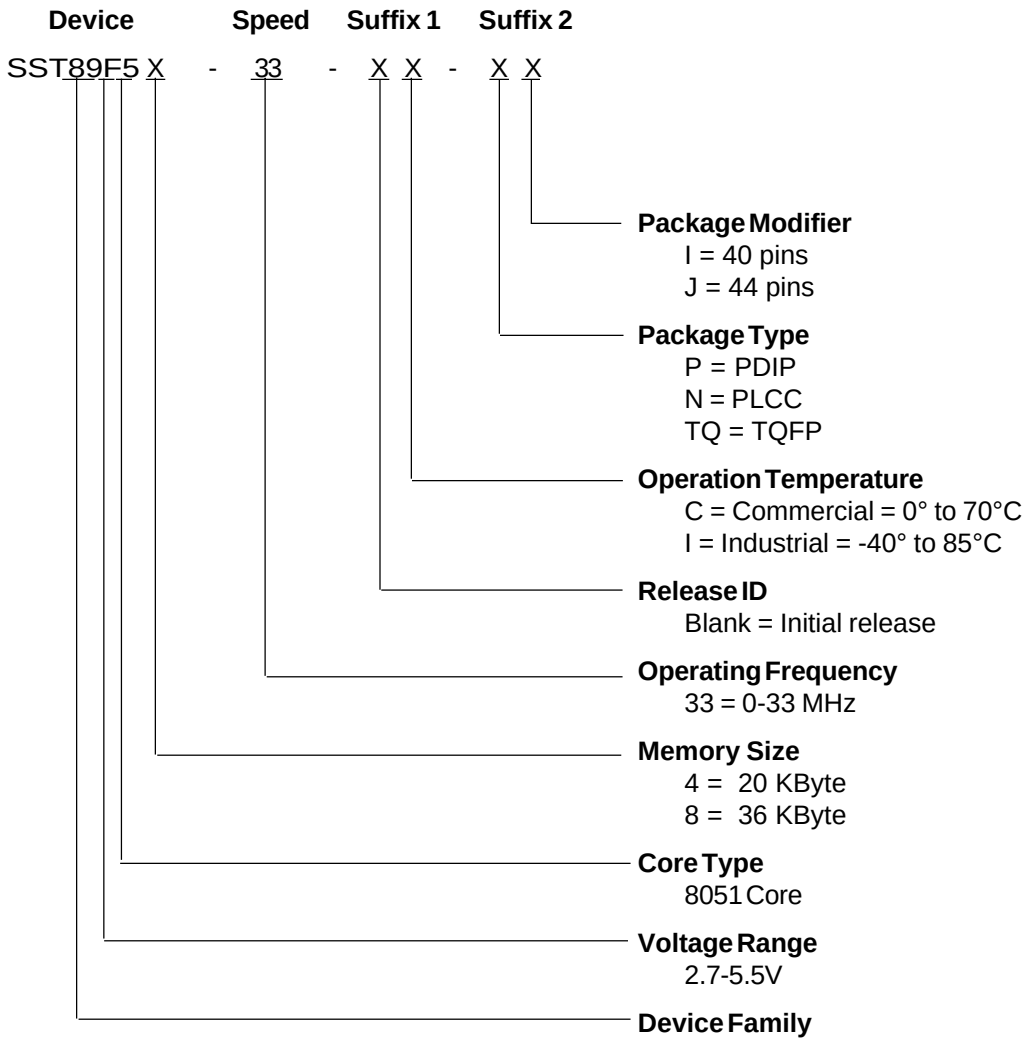


FIGURE 26: SHIFT REGISTER MODE TIMING WAVEFORMS

PRODUCT ORDERING INFORMATION

Product Identification Descriptor



Preliminary Specifications

Part Number Valid Combinations

SST89F54 Valid combinations

Part Number	*Package*	*Pins*	*V_{DD}*	*Speed*	*Temperature*
SST89F54-33-C-PI	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89F54-33-C-NJ	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89F54-33-C-TQJ	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89F54-33-I-PI	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89F54-33-I-NJ	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89F54-33-I-TQJ	TQFP	44	2.7-5.5	0-33MHz	Industrial

SST89F58 Valid combinations

Part Number	*Package*	*Pins*	*V_{DD}*	*Speed*	*Temperature*
SST89F58-33-C-PI	PDIP	40	2.7-5.5	0-33MHz	Commercial
SST89F58-33-C-NJ	PLCC	44	2.7-5.5	0-33MHz	Commercial
SST89F58-33-C-TQJ	TQFP	44	2.7-5.5	0-33MHz	Commercial
SST89F58-33-I-PI	PDIP	40	2.7-5.5	0-33MHz	Industrial
SST89F58-33-I-NJ	PLCC	44	2.7-5.5	0-33MHz	Industrial
SST89F58-33-I-TQJ	TQFP	44	2.7-5.5	0-33MHz	Industrial

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability and to determine availability of new combinations.

Part Number Cross-Reference Guide

Intel		SST		package
i87C54	16 KB EPROM & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
i87C58	32 KB EPROM & 256B RAM	SST89F58	4 KB Flash, 32 KB Flash & 256B RAM	D L Q
i87L54	16 KB ROM (OTP) & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	L Q
i87L58	32 KB ROM (OTP) & 256B RAM	SST89F58	4 KB Flash, 32 KB Flash & 256B RAM	L Q
i87C51FB	16 KB EPROM & 256B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
i87C51FC	32 KB EPROM & 256B RAM	SST89F58*	4 KB Flash, 32 KB Flash & 256B RAM	D L Q

Atmel		SST		package
AT89C52	8 KB Flash & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
AT89LV52	8 KB Flash & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
AT89S53	12 KB Flash & 256B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
AT89LS53	12 KB Flash & 256B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
AT89C55	20 KB Flash & 256B RAM	SST89F58*	4 KB Flash, 32 KB Flash & 256B RAM	D L Q
AT89LV55	20 KB Flash & 256B RAM	SST89F58*	4 KB Flash, 32 KB Flash & 256B RAM	D L Q

Temic		SST		package
80C51	4 KB ROM & 256B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
80C52	8 KB ROM & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
83C154	16 KB ROM & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
83C154D	32 KB ROM & 256B RAM	SST89F58	4 KB Flash, 32 KB Flash & 256B RAM	D L Q
87C51	4 KB EPROM & 256B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
87C52	8 KB EPROM & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q

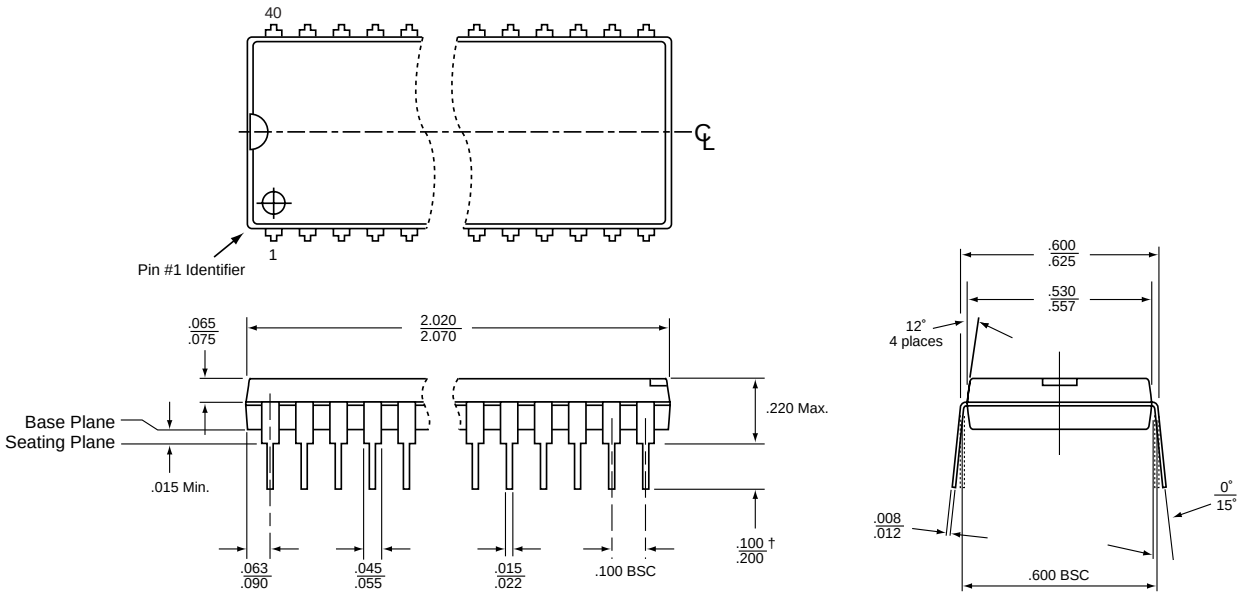
Philips		SST		package
P80C54	16 KB ROM & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
P80C58	32 KB ROM & 256B RAM	SST89F58	4 KB Flash, 32 KB Flash & 256B RAM	D L Q
P87C54	16 KB EPROM & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
P87C58	32 KB EPROM & 256B RAM	SST89F58	4 KB Flash, 32 KB Flash & 256B RAM	D L Q
P87C524	16 KB EPROM & 512B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	D L Q
P87C528	32 KB EPROM & 512B RAM	SST89F58*	4 KB Flash, 32 KB Flash & 256B RAM	D L Q
P83C524	16 KB ROM & 512B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	D L
P83C528	32 KB MROM & 512B RAM	SST89F58*	4 KB Flash, 32 KB Flash & 256B RAM	D L Q
P89CE558	32 KB Flash & 1K RAM	SST89F58*	4 KB Flash, 32 KB Flash & 256B RAM	

Siemens		SST		package
C501-1R	8 KB ROM & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L
C501-1E	8 KB ROM (OTP) & 256B RAM	SST89F54	4 KB Flash, 16 KB Flash & 256B RAM	D L
C513A-H	12 KB EPROM & 512B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	L
C503-1R	8 KB ROM & 256B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	L
C504-2R	16 KB ROM & 512B RAM	SST89F54*	4 KB Flash, 16 KB Flash & 256B RAM	Q

D: PDIP
L: PLCC
Q: TQFP

NOTE: The SST89F58 can be substituted for any SST89F54 listing above.
* Indicates SST similar function and not direct replacement/socket compatible.

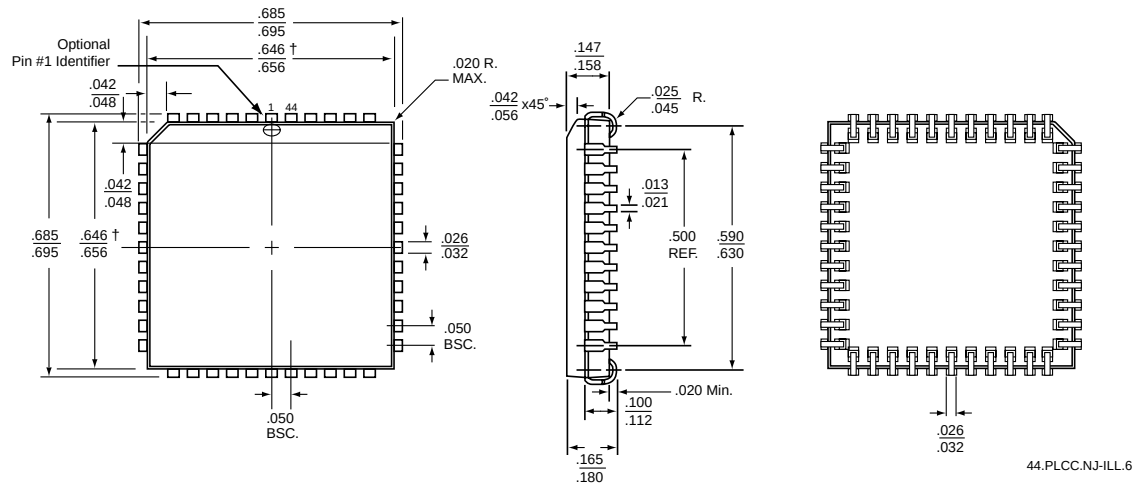
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-011 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .115; SST min is *less* stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

40.pdipPI-ILL.6

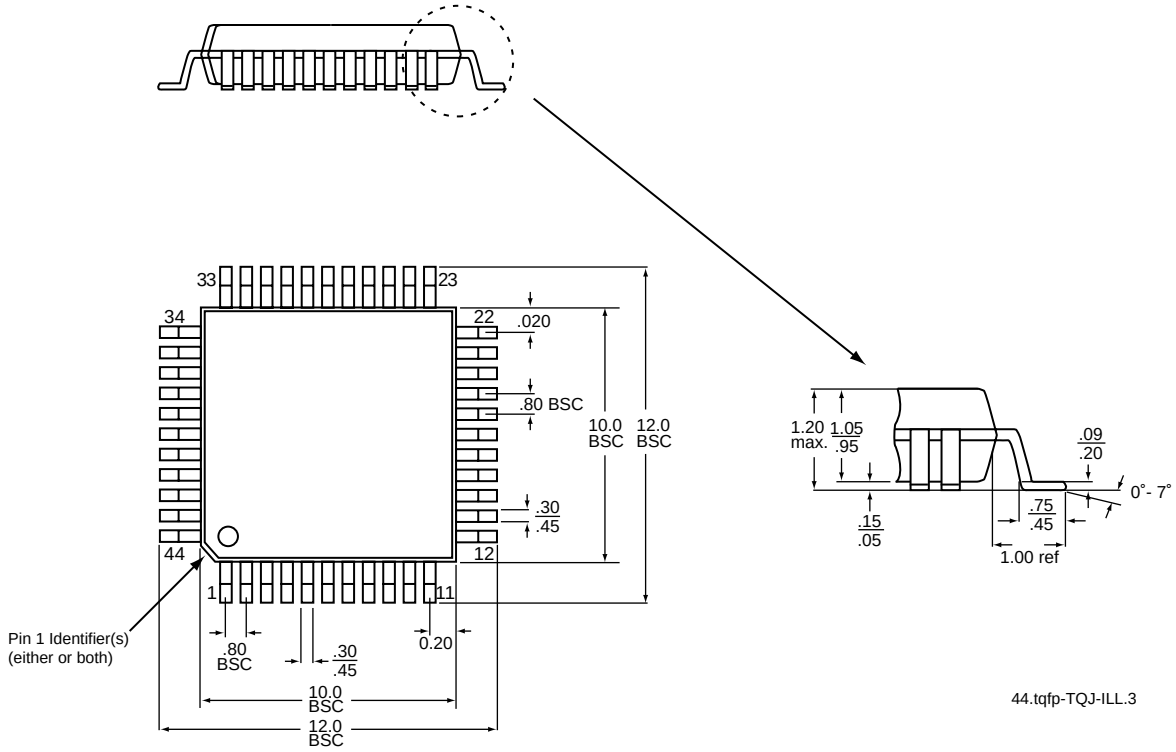
40-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PI



44.PLCC.NJ-ILL.6

Note: 1. Complies with JEDEC publication 95 MS-018 AC dimensions (except as noted), although some dimensions may be more stringent.
† = JEDEC min is .650; SST min is *less* stringent
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: ± 4 mils.

44-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NJ



Note:
1. Complies with JEDEC publication 95 MS-026 ACB dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in mm (min/max).
3. Coplanarity: 0.1 (±0.05) mm.

44-LEAD THIN QUAD FLAT PACK (TQFP)
SST PACKAGE CODE: TQJ

Notes:

SALES OFFICES

SST Area Offices

Customer Service	(408) 523-7754
Northwest USA, Rocky Mtns. & West Canada	(408) 523-7661
Southwest USA	(949) 495-6437
East USA & East Canada	(978) 356-3845
Corporate CEM Accounts	(727) 771-8819
North America - Distribution	(941) 505-8893
Asia Pacific	(408) 523-7762
East Asia	(81) 45-471-1851
Europe	(44) 1932-230555
Northern Europe	(45) 3833-5000

North American Sales Representatives

Alabama M-Squared, Inc. - Huntsville	(205) 830-0498
Arizona Reptronix, Ltd.	(602) 230-2630
California	
Costar - Northern	(408) 946-9339
Falcon Sales & Technology - San Marcos	(760) 591-0504
Westar Rep Company, Inc. - Calabasas	(818) 880-0594
Westar Rep Company, Inc. - Irvine	(949) 453-7900
Colorado Lange Sales, Inc.	(303) 795-3600
Florida	
M-Squared, Inc. - Clearwater	(727) 669-2408
M-Squared, Inc. - Longwood	(407) 682-6662
Georgia M-Squared, Inc. - Atlanta	(770) 447-6124
Illinois	
Oasis Sales Corporation - Northern	(847) 640-1850
Rush & West Associates - Southern	(314) 965-3322
Indiana Applied Data Management	(317) 257-8949
Iowa Rush & West Associates	(319) 398-9679
Kansas Rush & West Associates	(913) 764-2700
Maryland Nexus Technology Sales	(301) 663-4159
Massachusetts Innovative Applied Solutions	(781) 246-9996
Michigan Applied Data Management	(734) 741-9292
Minnesota Cahill, Schmitz & Cahill	(651) 699-0200
Missouri Rush & West Associates	(314) 965-3322
North Carolina	
M-Squared, Inc. - Charlotte	(704) 522-1150
M-Squared, Inc. - Raleigh	(919) 848-4300
New Mexico Reptronix, Ltd.	(505) 292-1718
New York	
Nova Technology	(516) 661-1800
Reagan/Compar - Endwell	(607) 754-2171
Reagan/Compar - E. Rochester	(716) 218-4370
Ohio	
Applied Data Management - Cincinnati	(513) 579-8108
Applied Data Management - Cleveland	(440) 946-6812
Oregon Thorson Pacific, Inc.	(503) 293-9001
Texas	
Technical Marketing, Inc. - Carrollton	(972) 387-3601
Technical Marketing, Inc. - Houston	(713) 783-4497
Technical Marketing, Inc. - Austin	(512) 343-6976
Utah Lange Sales, Inc.	(801) 487-0843
Washington Thorson Pacific, Inc.	(425) 603-9393
Wisconsin Oasis Sales Corporation	(414) 782-6660
Canada	
Electronics Sales Professionals - Ottawa	(613) 828-6881
Electronics Sales Professionals - Toronto	(905) 856-8448
Electronics Sales Professionals - Montreal	(514) 344-0420
Thorson Pacific, Inc. - B.C.	(604) 294-3999

International Sales Representatives & Distributors

Australia ACD	(61) 3-762 7644
Austria Endrich Bauelemente Vertriebs GMBH	(43) 2-236236-21
Belgium Memec Benelux	(32) 1540-0080
China/Hong Kong	
Actron Technology Co., Ltd. (HQ) Hong Kong	(852) 2727-3978
Actron Technology Co., Ltd. - Shanghai	(86) 21-6482-8021
Actron Technology Co., Ltd. - Shenzhen	(86) 755-376-2763
Actron Technology Co., Ltd. - Chengdu	(86) 28-553-2896
Actron Technology Co., Ltd. - Beijing	(86) 10-6261-0042
Actron Technology Co., Ltd. - Wuhan	(86) 27-8788-7226
Actron Technology Co., Ltd. - Xian	(86) 29-831-4585
MetaTech Limited (HQ) - Hong Kong	(852) 2421-2379
MetaTech Limited - Beijing	(86) 10-6858-2188
MetaTech Limited - Shanghai	(86) 21-6485-7530
MetaTech Limited - Chengdu	(86) 28-5577-415
MetaTech Limited - Fuzhou	(86) 591-378-1033
MetaTech Limited - Shenzhen	(86) 755-321-9726
Denmark C-88 AS	(45) 7010-4888
Finland Memec Finland Oy	(358)9 350 8880
France	
A2M - Bron	(33) 4 72 37 0414
A2M - Sevres	(33) 1 46 23 7900
Germany	
Endrich Bauelemente Vertriebs GMBH - Bramstedt	(49) 4192-8784-0
Endrich Bauelemente Vertriebs GMBH - Nagold	(49) 7452-60070
India	
Team Technology - Bangalore	(91) 80-526-1102
Team Technology - Hyderabad	(91) 40-231130
Team Technology - New Delhi	(91) 11-220-5624
Ireland Curragh Technology	(353) 61 316116
Israel Spectec Electronics	(972) 3-6498404
Italy Carlo Gavazzi Cefra SpA	(39) 2-424-1471
Japan	
Asahi Electronics Co., Ltd. - Tokyo	(81) 3-3350-5418
Asahi Electronics Co., Ltd. - Kitakyushu	(81) 93-511-6471
Microtek, Inc. - Osaka	(81) 6-6263-5080
Microtek, Inc. - Tokyo	(81) 3-5300-5515
Ryoden Trading Co., Ltd. - Osaka	(81) 6-6399-3443
Ryoden Trading Co., Ltd. - Tokyo	(81) 3-5396-6218
Silicon Technology Co., Ltd.	(81) 3-3795-6461
Korea Bigshine Korea Co., Ltd.	(82) 2-832-8881
Malaysia	
MetaTech (M) SDN BHD	(60)4-658-4276
Serial System SDN BHD	(60) 4-657-0204
Serial System - Kuala Lumpur	(60) 3-737-1243
Netherlands Memec Benelux	(31) 40-265-9399
Norway Endrich Elektronikk AS	(47) 22 52 13 20
Philippines MetaTech (S) Pte Ltd.	(65) 748-4844
Singapore	
MetaTech (S) Pte Ltd.	(65) 748-4844
Serial System Ltd. (HQ)	(65) 280-0200
South Africa KH Distributors	(27) 11 845-5011
Spain Tekelec Espana S.A.	(34) 91 371-7768
Sweden Memec Scandinavia	(46)8-459-7900
Switzerland Leading Technologies	(41) 27-721-7440/43
Taiwan, R.O.C.	
GCH-Sun Systems Co., Ltd. (GSS)	(886) 2-2555-0880
PCT Limited	(886) 2-2698-0098
United Kingdom Ambar Components, Ltd.	(44) 1296-397396

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