S3FM02G

32-Bit CMOS MICROCONTROLLERS

Revision 1.00

January 2011

Data Sheet

SAMSUNG ELECTRONICS

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Revision History

Revision No.	Date	Description	Author(s)
1.00	Jan. 10, 2011	•	Juil. Kim

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List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1'b1 and clears it by writing 1'b0.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	
1	
x	

Warning: Some bits of control registers are driven by hardware or write only. As a result the indicated reset value and the read value after reset might be different.

1 OVERVIEW

1.1 Purpose This Document

The purpose of this document is to provide a complete reference specification of S3FM02G.

1.2 Instruction to S3FM02G

S3FM02G is a family of cost-effective and high-performance microcontrollers with Cortex™-M3 designed by Advanced RISC Machines (ARM). This Microcontroller unit (MCU) applies to inverter motor control within the home appliance applications.

- ARM Cortex™-M3 Core
- Built-in up to 384 Kbytes Program Flash Memory
- Built-in up to 16 Kbytes Data Flash Memory
- Internal up to 24 Kbytes SRAM for stack, data memory, or code memory
- Operating temperature: -40 ~ 85 °C
- Operating voltage range: 2.7 ~ 5.5 V
- Interrupt controller: Dynamically reconfigurable Nested Vectored Interrupt Controller (NVIC)
- Clock and Power Controller (CM)
- 10ch x DMA Controller (DMAC)
- Watch-Dog Timer (WDT)
- 8ch x 16-bit Timer/Counters (TC)
- 32-bit Free-Running Timer (FRT)
- 8ch x 16-bit PWM
- 2ch x 16bit Encoder Counter (ENC)
- 2ch x 6-Phase Inverter Motor Controller (IMC)
- 2ch x I2C, 2ch x SSP, 2ch x CAN and 4ch x USART
- 12-bit ADC(4 channels with OP-AMP)
- 10-bit ADC
- 5ch OP-AMP
- 4com x 40seg LCD Controller (LCDC)
- Support Normal, High-speed, IDLE, and STOP mode

1.3 Features

- CPU
  - 32-bit RISC ARM Cortex™-M3 Core
  - ETM function embedded with ARM Cortex™-M3
  - SWD(Serial Wire Debug) and JTAG Debugging Solution

- Memory
  - Up to 384 Kbytes Internal Program Full Flash
  - Up to 16 Kbytes Internal Data Flash
  - Up to 24 Kbytes Internal SRAM
  - Only little-endian support

- Interrupt Controller
  - Supports Nested Vectored Interrupt Controller of Cortex™-M3
  - Dynamically reconfigurable Interrupt Priority (16 priority levels)

- Clock Manager (CM)
  - External Oscillator 4 ~ 8MHz (EMCLK: External Main Clock) and 32.768KHz (ESCLK: External Sub-Clock)
  - Internal Oscillator 8/16/20MHz (IMCLK: Internal Main Clock) and 32.768KHz (ISCLK: Internal Sub-Clock)
  - Up to 75MHz by Phase-Locked Loop Control (PLL)
  - Clock Monitor to detect an external main and sub-oscillator failure
  - Support Low Power Mode (IDLE / STOP) by Clock Gating Control
  - Programmable Clock Dividers (SDIV, PDIV)
  - Reset Management
  - Include basic timer for reset generation and STOP wake-up

- DMAC: Direct Memory Access Controller
  - Up to 10 channels
  - Transfer from Memory to Memory
  - Transfer between Peripheral and Memory
  - Transfer between Peripheral and Peripheral

- WDT: Watchdog Timer
  - Configurable micro-controller reset event
  - Programmable 16-bit down counter

- TC: 16-bit Timer/Counter
  - Up to 8 channels (TC0 ~ TC7)
  - Operation in an interval, capture, match & overflow, or PWM mode
  - Match and overflow interrupt
  - Selectable an internal or external timer clock

- FRT: Free Running Timer
  - 32-bit Timer
  - Can operate in stop mode with ISCLK, as an independent timer

- PWM: Pulse Width Modulation
  - Up to 8 channels
  - 16-bit PWM signal generation
  - Interval Mode
  - Programmable Idle Level
  - Support extension PWM function

- ENC: Encoder Counter
  - Up to 2 channels
  - 3 input signals: PHASEA, PHASEB, and PHASEZ
  - Support position counter and speed counter
  - Up/Down counter
  - Support capture mode

- IMC: Inverter Motor Controller
  - UP to 2 channels
  - Support 3-Phase 16-bit PWM generation
  - Programmable dead time insertion
  - ADC conversion start signal generation

- CAN: Controller Area Network
  - CAN0/1 With 32 Buffers
  - Support CAN 2.0A and 2.0B Full Speed
  - Stampable Message

- USART: Universal Sync/Async Receiver Transmitter
  - Up to 4 channels
  - Support 5, 6, 7, and 8bit Data length
  - Programmable baud rate generator
  - Parity, framing and overrun error detection
  - Support loop-back mode
  - Support full duplex
  - Idle flag for J1587 protocol
  - Support LIN protocol: LIN1.2 or LIN 2.0 configurable release
  - Smart-card protocol: Error signaling and re-transmission
  - Dedicated DMA channel

- SSP: Serial Synchronous Peripheral Interface
  - Up to 2 channels
  - Programmable data frame from 4 to 16-bit
  - Support Master and Slave Mode
  - Programmable Clock Pre-scale
  - Separate 16 x 32-bit width Transmit/Receive FIFO
  - Dedicated DMA channel

- IIC: Inter-Integrated Circuit
  - Up to 2 channels
  - Multi-Master IIC-Bus
  - Serial, 8-bit Oriented and Bi-directional Data Transfers
  - 100Kbit/s in Standard Mode and up to 400Kbit/s in Fast mode
  - Dedicated DMA channel

- ADC: A/D Converters
  - Up to 16 channel's Analog Inputs
  - 12-bit ADC0 x 2 and 10-bit ADC1
  - 4 x Op-amp for 12-bit ADC input level amplification
  - supports simultaneous sampling and conversion up to 2-input channels
  - Dedicated DMA channel

- OP amp
  - 5 ch OP amp
  - Can be operated with ADC
  - Edge detection function which is related with IMC

- LCDC: LCD Controller
  - 4 com x 40 segment
  - Static, 1/2 and 1/3 bias mode
  - External and internal resistor bias

- General Purpose IO (GPIO)
  - Disabling IO port enables the function of peripherals on pins
  - Output Open-drain / Push-pull configuration
  - Input Pull-up Resistor enable/disable configuration
  - GPIO Interrupt

- Two Low Power Modes
  - IDLE: Only CPU clock stops
  - STOP: Selected system clock and CPU clock stop
  - Fast wake-up with internal 8/16/20MHz oscillator (from STOP mode to normal mode)
  - Programmable external event/interrupt sources for Wake-up

- POR: Power-On Reset

- LVD: Low Voltage Detection
  - LVD for reset with configurable voltage levels
  - LVD for interrupt with configurable voltage levels

- PLL: Phase-Locked Loop
  - Input Frequency: 4 ~ 8 MHz
  - Output Frequency: 8 ~ 75MHz

- Operating Voltage Range
  - 2.7V ~ 5.5V

- Operating Frequency Range
  - 4 ~ 8 MHz by external main oscillator clock
  - 8/16/20MHz by internal main oscillator clock
  - 32.768KHz external/internal sub-oscillator clock
  - 8 ~ 75 MHz by PLL clock

- Operating Temperature Range
  - -40 ~ 85 °C

- Available in 128 ETQFP Package

1.4 Block Diagram

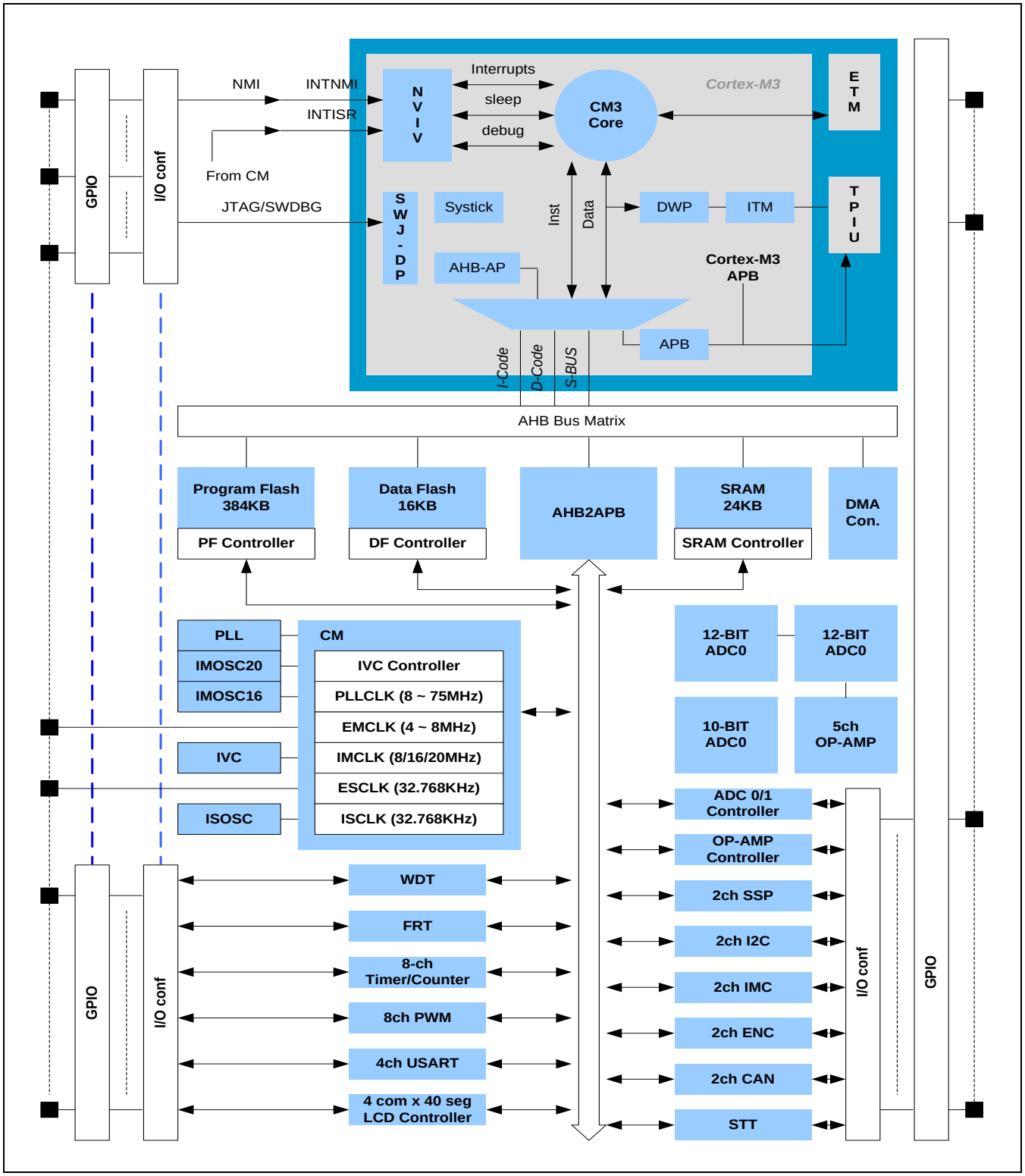


Figure 1-1 S3FM02G Block Diagram

2 PIN CONFIGURATION

2.1 Pin Configuration

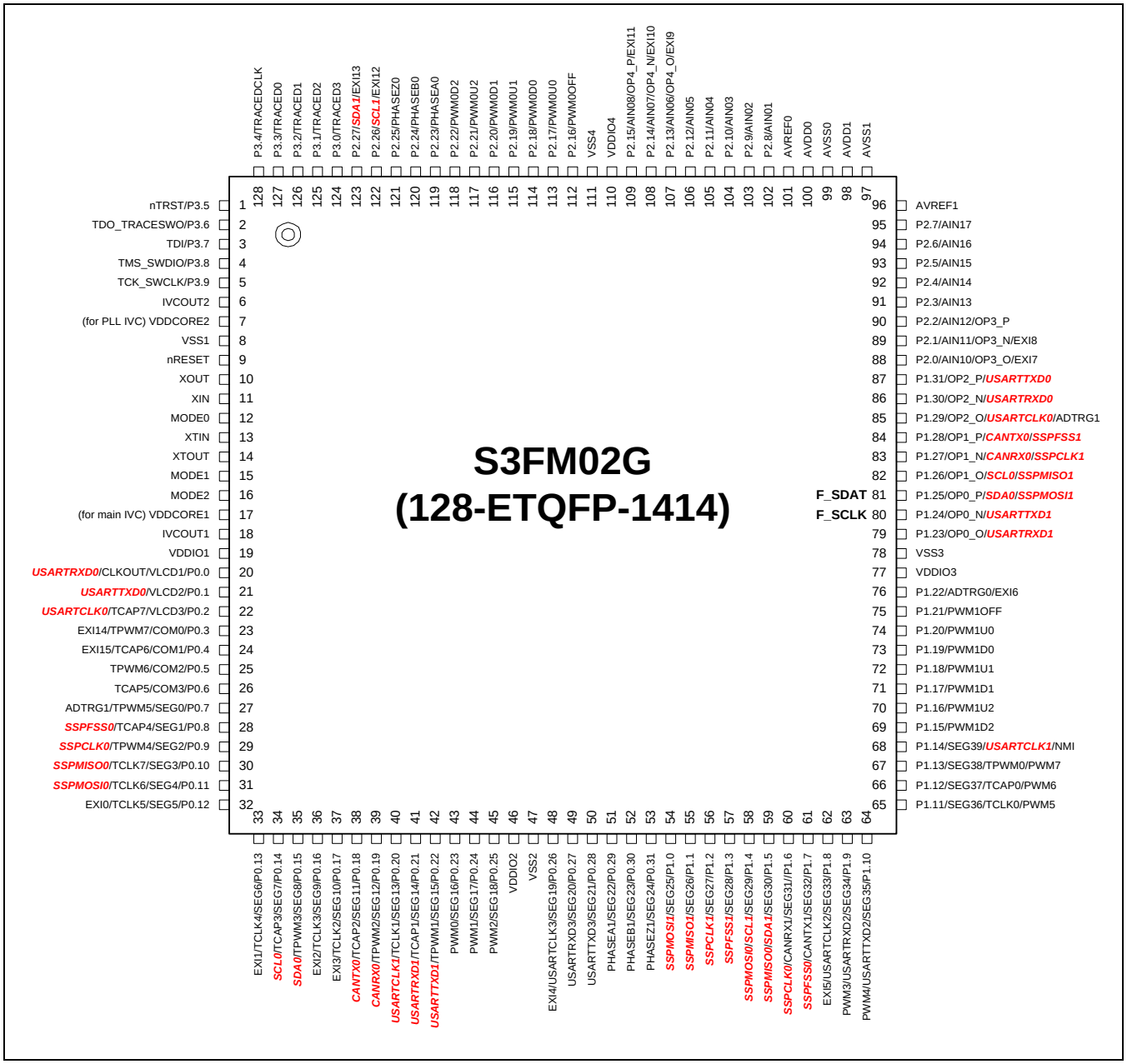


Figure 2-1 Pin Configuration

2.2 Pin Assignments

- D: Digital, A: Analog
- IO: Input and Output (Bi-direction), O: Output, I: Input, P: Power, G: Ground

Table 2-1 Pin Assignments – Pin Number Order

Num	PIN Name				Default @RESET	PULL up/dn @RESET	I/O state @RESET
	1st	2nd	3rd	4th			
1	P3.5	nTRST	–	–	nTRST	PULL-UP	I
2	P3.6	TDO/TRACESWO	–	–	TDO/ TRACESWO	–	O
3	P3.7	TDI	–	–	TDI	PULL-UP	I
4	P3.8	TMS/SWDIO	–	–	TMS/SWDIO	PULL-UP	I
5	P3.9	TCK/SWCLK	–	–	TCK/SWCLK	PULL-UP	I
6	IVCOUT2	IVCOUT2	IVCOUT2	IVCOUT2	IVCOUT2	–	O
7	VDDCORE2	VDDCORE2	VDDCORE2	VDDCORE2	VDDCORE2	–	P
8	VSS1	VSS1	VSS1	VSS1	VSS1	–	G
9	nRESET	nRESET	nRESET	nRESET	nRESET	PULL-UP	I
10	X_{OUT}	X_{OUT}	X_{OUT}	X_{OUT}	X_{OUT}	–	O
11	X_{IN}	X_{IN}	X_{IN}	X_{IN}	X_{IN}	–	I
12	MODE0	MODE0	MODE0	MODE0	MODE0	PULL-DN	I
13	X_{TIN}	X_{TIN}	X_{TIN}	X_{TIN}	X_{TIN}	–	I
14	X_{TOUT}	X_{TOUT}	X_{TOUT}	X_{TOUT}	X_{TOUT}	–	O
15	MODE1	MODE1	MODE1	MODE1	MODE1	PULL-DN	I
16	MODE2	MODE2	MODE2	MODE2	MODE2	PULL-DN	I
17	VDDCORE1	VDDCORE1	VDDCORE1	VDDCORE1	VDDCORE1	–	P
18	IVCOUT1	IVCOUT1	IVCOUT1	IVCOUT1	IVCOUT1	–	O
19	VDDIO1	VDDIO1	VDDIO1	VDDIO1	VDDIO1	–	P
20	P0.0	VLCD1	CLKOUT	***USARTRXD0***	P0.0	–	I
21	P0.1	VLCD2	–	***USARTTXD0***	P0.1	–	I
22	P0.2	VLCD3	TCAP7	***USARTCLK0***	P0.2	–	I
23	P0.3	COM0	TPWM7	EXI14	P0.3	–	I
24	P0.4	COM1	TCAP6	EXI15	P0.4	–	I
25	P0.5	COM2	TPWM6	–	P0.5	–	I
26	P0.6	COM3	TCAP5	–	P0.6	–	I
27	P0.7	SEG0	TPWM5	ADTRG1	P0.7	–	I
28	P0.8	SEG1	TCAP4	***SSPFSS0***	P0.8	–	I
29	P0.9	SEG2	TPWM4	***SSPCLK0***	P0.9	–	I

Num	PIN Name				Default @RESET	PULL up/dn @RESET	I/O state @RESET
	1st	2nd	3rd	4th			
30	P0.10	SEG3	TCLK7	***SSPMISO0***	P0.10	–	I
31	P0.11	SEG4	TCLK6	***SSPMOSI0***	P0.11	–	I
32	P0.12	SEG5	TCLK5	EXI0	P0.12	–	I
33	P0.13	SEG6	TCLK4	EXI1	P0.13	–	I
34	P0.14	SEG7	TCAP3	***SCL0***	P0.14	–	I
35	P0.15	SEG8	TPWM3	***SDA0***	P0.15	–	I
36	P0.16	SEG9	TCLK3	EXI2	P0.16	–	I
37	P0.17	SEG10	TCLK2	EXI3	P0.17	–	I
38	P0.18	SEG11	TCAP2	***CANTX0***	P0.18	–	I
39	P0.19	SEG12	TPWM2	***CANRX0***	P0.19	–	I
40	P0.20	SEG13	TCLK1	***USARTCLK1***	P0.20	–	I
41	P0.21	SEG14	TCAP1	***USARTRXD1***	P0.21	–	I
42	P0.22	SEG15	TPWM1	***USARTTXD1***	P0.22	–	I
43	P0.23	SEG16	PWM0	–	P0.23	–	I
44	P0.24	SEG17	PWM1	–	P0.24	–	I
45	P0.25	SEG18	PWM2	–	P0.25	–	I
46	VDDIO2	VDDIO2	VDDIO2	VDDIO2	VDDIO2	–	P
47	VSS2	VSS2	VSS2	VSS2	VSS2	–	G
48	P0.26	SEG19	USARTCLK3	EXI4	P0.26	–	I
49	P0.27	SEG20	USARTRXD3	–	P0.27	–	I
50	P0.28	SEG21	USARTTXD3	–	P0.28	–	I
51	P0.29	SEG22	PHASEA1	–	P0.29	–	I
52	P0.30	SEG23	PHASEB1	–	P0.30	–	I
53	P0.31	SEG24	PHASEZ1	–	P0.31	–	I
54	P1.0	SEG25	***SSPMOSI1***	–	P1.0	–	I
55	P1.1	SEG26	***SSPMISO1***	–	P1.1	–	I
56	P1.2	SEG27	***SSPCLK1***	–	P1.2	–	I
57	P1.3	SEG28	***SSPFSS1***	–	P1.3	–	I
58	P1.4	SEG29	***SCL1***	***SSPMOSI0***	P1.4	–	I
59	P1.5	SEG30	***SDA1***	***SSPMISO0***	P1.5	–	I
60	P1.6	SEG31	CANRX1	***SSPCLK0***	P1.6	–	I
61	P1.7	SEG32	CANTX1	***SSPFSS0***	P1.7	–	I
62	P1.8	SEG33	USARTCLK2	EXI5	P1.8	–	I
63	P1.9	SEG34	USARTRXD2	PWM3	P1.9	–	I
64	P1.10	SEG35	USARTTXD2	PWM4	P1.10	–	I

Num	PIN Name				Default @RESET	PULL up/dn @RESET	I/O state @RESET
	1st	2nd	3rd	4th			
65	P1.11	SEG36	TCLK0	PWM5	P1.11	–	I
66	P1.12	SEG37	TCAP0	PWM6	P1.12	–	I
67	P1.13	SEG38	TPWM0	PWM7	P1.13	–	I
68	P1.14	SEG39	***USARTCLK1***	NMI	P1.14	–	I
69	P1.15	PWM1D2	–	–	P1.15	–	I
70	P1.16	PWM1U2	–	–	P1.16	–	I
71	P1.17	PWM1D1	–	–	P1.17	–	I
72	P1.18	PWM1U1	–	–	P1.18	–	I
73	P1.19	PWM1D0	–	–	P1.19	–	I
74	P1.20	PWM1U0	–	–	P1.20	–	I
75	P1.21	PWM1OFF	–	–	P1.21	–	I
76	P1.22	ADTRG0	EXI6	–	P1.22	–	I
77	VDDIO3	VDDIO3	VDDIO3	VDDIO3	VDDIO3	–	P
78	VSS3	VSS3	VSS3	VSS3	VSS3	–	G
79	P1.23	OP0_O	***USARTRXD1***	–	P1.23	–	I
80	P1.24	OP0_N	***USARTTXD1***	–	P1.24	–	I
81	P1.25	OP0_P	***SDA0***	***SSPMOSI1***	P1.25	–	I
82	P1.26	OP1_O	***SCL0***	***SSPMISO1***	P1.26	–	I
83	P1.27	OP1_N	***CANRX0***	***SSPCLK1***	P1.27	–	I
84	P1.28	OP1_P	***CANTX0***	***SSPFSS1***	P1.28	–	I
85	P1.29	OP2_O	***USARTCLK0***	ADTRG1	P1.29	–	I
86	P1.30	OP2_N	***USARTRXD0***	–	P1.30	–	I
87	P1.31	OP2_P	***USARTXD0***	–	P1.31	–	I
88	P2.0	AIN10	OP3_O	EXI7	P2.0	–	I
89	P2.1	AIN11	OP3_N	EXI8	P2.1	–	I
90	P2.2	AIN12	OP3_P	–	P2.2	–	I
91	P2.3	AIN13	–	–	P2.3	–	I
92	P2.4	AIN14	–	–	P2.4	–	I
93	P2.5	AIN15	–	–	P2.5	–	I
94	P2.6	AIN16	–	–	P2.6	–	I
95	P2.7	AIN17	–	–	P2.7	–	I
96	AVREF1	AVREF1	AVREF1	AVREF1	AVREF1	–	I
97	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	–	G
98	AVDD1	AVDD1	AVDD1	AVDD1	AVDD1	–	P
99	AVSS0	AVSS0	AVSS0	AVSS0	AVSS0	–	G

Num	PIN Name				Default @RESET	PULL up/dn @RESET	I/O state @RESET
	1st	2nd	3rd	4th			
100	AVDD0	AVDD0	AVDD0	AVDD0	AVDD0	–	P
101	AVREF0	AVREF0	AVREF0	AVREF0	AVREF0	–	I
102	P2.8	AIN01	–	–	P2.8	–	I
103	P2.9	AIN02	–	–	P2.9	–	I
104	P2.10	AIN03	–	–	P2.10	–	I
105	P2.11	AIN04	–	–	P2.11	–	I
106	P2.12	AIN05	–	–	P2.12	–	I
107	P2.13	AIN06	OP4_O	EXI9	P2.13	–	I
108	P2.14	AIN07	OP4_N	EXI10	P2.14	–	I
109	P2.15	AIN08	OP4_P	EXI11	P2.15	–	I
110	VDDIO4	VDDIO4	VDDIO4	VDDIO4	VDDIO4	–	P
111	VSS4	VSS4	VSS4	VSS4	VSS4	–	G
112	P2.16	PWM0OFF	–	–	P2.16	–	I
113	P2.17	PWM0U0	–	–	P2.17	–	I
114	P2.18	PWM0D0	–	–	P2.18	–	I
115	P2.19	PWM0U1	–	–	P2.19	–	I
116	P2.20	PWM0D1	–	–	P2.20	–	I
117	P2.21	PWM0U2	–	–	P2.21	–	I
118	P2.22	PWM0D2	–	–	P2.22	–	I
119	P2.23	PHASEA0	–	–	P2.23	–	I
120	P2.24	PHASEB0	–	–	P2.24	–	I
121	P2.25	PHASEZ0	–	–	P2.25	–	I
122	P2.26	***SCL1***	EXI12	–	P2.26	–	I
123	P2.27	***SDA1***	EXI13	–	P2.27	–	I
124	P3.0	TRACED3	–	–	P3.0	–	I
125	P3.1	TRACED2	–	–	P3.1	–	I
126	P3.2	TRACED1	–	–	P3.2	–	I
127	P3.3	TRACED0	–	–	P3.3	–	I
128	P3.4	TRACECLK	–	–	P3.4	–	I

2.3 Pin Description

- D: Digital, A: Analog
- IO: Input and Output (Bi-direction), O: Output, I: Input, P: Power, G: Ground

2.3.1 Miscellaneous

Name	I/O	Description	D/A
nRESET	I	Chip Reset Signal (active “Low”) This nRESET pin contains an internal pull up resistor 250. Setting this pin to low level initialize the internal state of the device. Thereafter, setting the input to high release the reset status. The S3FM02G waits for the system clock to be stable, and the PC to the reset interrupt vector. Internal Reset is generated after clock stabilization.	D
MODE[2:0]	I	Factory test input pins. This pins should be connected to Ground	D

2.3.2 Clock Manager

Name	I/O	Description	D/A
X_{IN}	I	External Main Oscillator Input (4MHz ~ 8MHz)	A
X_{OUT}	O	External Main Oscillator Output	A
XT_{IN}	I	External Sub-Oscillator Input (32.768KHz)	A
XT_{OUT}	O	External Sub-Oscillator Output.	A
CLKOUT	O	Internal Clock Output signals.	D

2.3.3 External Interrupt

Name	I/O	Description	D/A
EXI0 ~ EXI15	I	External interrupt/wakeup input pins	D

2.3.4 DEBUG Interface

Name	I/O	Description	D/A
TCK/SWCLK	I	JTAG Test Clock/ Serial Wire Clock, Pull-up	D
TMS/SWDIO	I	JTAG Test Mode Select/ Serial Wire Data Input Output, Pull-up	D
TDI	I	JTAG Test Data Input, Pull-up	D
TDO/TRACESWO	O	JTAG Test Data Out / Trace Serial Wire Viewer Data	D
nTRST	I	JTAG Test nRESET, Pull-up	D
TRACECLK	O	Trace Clock	D
TRACED[3:0]	O	Trace Data	D

2.3.5 USART Interface

Name	I/O	Description	D/A
USARTCLK[3:0]	IO	External Clock Signal Input / Internal Clock Signal Output	D
USARTRXD[3:0]	I	Receive Data Input	D
USARTTXD[3:0]	O	Transmit Data Output	D

2.3.6 Encoder Interface

Name	I/O	Description	D/A
PHASEA[1:0]	I	Phase A input pin	D
PHASEB[1:0]	I	Phase B input pin	D
PHASEZ[1:0]	I	Phase Z input pin	D

2.3.7 IMC Interface

Name	I/O	Description	D/A
PWM[1:0]U[2:0]	O	PWM output for inverter motor	D
PWM[1:0]D[2:0]	O	PWM output for inverter motor	D
PWM[1:0]OFF	I	Input pin for PWM output off	D

2.3.8 TIMER Interface

Name	I/O	Description	D/A
TCLK[7:0]	I	External Clock Input	D
TCAP[7:0]	I	External Capture Input	D
TPWM[7:0]	O	PWM Output	D

2.3.9 PWM Interface

Name	I/O	Description	D/A
PWM[7:0]	O	Pulse width modulation output	D

2.3.10 I2C Interface

Name	I/O	Description	D/A
SCL[1:0]	IO	Serial Clock	D
SDA[1:0]	IO	Serial Data	D

2.3.11 CAN Interface

Name	I/O	Description	D/A
CANTX[1:0]	O	Transmit Data Output	D
CANRX[1:0]	I	Receive Data Input	D

2.3.12 SSP Interface

Name	I/O	Description	D/A
SSPCLK[1:0]	IO	SSP Master Clock Output / Slave Clock Input	D
SSPMISO[1:0]	IO	SSP Master Input / Slave Output	D
SSPMOSI[1:0]	IO	SSP Master Output / Slave Input	D
SSPFSS[1:0]	IO	SSP Master Chip Select Output / Slave Chip Select Input	D

2.3.13 LCD Controller Interface

Name	I/O	Description	D/A
VLCD[3:1]	P	LCD Power Supply	D
COM[3:0]	O	COM drive signal	D
SEG[39:0]	O	SEG drive signal	D

2.3.14 ADC Interface

Name	I/O	Description	D/A
AIN0[8:1]	I	Analog Input pins for 8-channels	A
AIN1[7:0]	I	Analog Input pins for 8-channels	A
ADTRG[1:0]	I	ADC External Trigger Input pin	D
AVREF[1:0]	I	ADC Reference Top Voltage.	A

2.3.15 OP-AMP Interface

Name	I/O	Description	D/A
OP[4:0]_O	O	OP-AMP Output	A
OP[4:0]_N	I	OP-AMP N Input	A
OP[4:0]_P	I	OP-AMP P Input	A

2.3.16 GPIOs

Name	I/O	Description	D/A
P0[31:0]	IO	General Purpose I/O port 0	D
P1[31:0]	IO	General Purpose I/O port 1	D
P2[27:0]	IO	General Purpose I/O port 2	D
P3[9:0]	IO	General Purpose I/O port 3	D

2.3.17 FLASH

Name	I/O	Description	D/A
F_SDAT	IO	Serial Data pin (Output when reading, Input when writing)	D
F_SCLK	I	Serial Clock	D

2.3.18 Power

Name	I/O	Description
VDDCORE[2:1]	P	Digital Power for interval IVC (2.7V ~ 5.5V)
VDDIO[4:1]	P	Digital IO Power 2.7 V ~ 5.5V
VSS[4:1]	G	Digital Ground
IVCOUT[2:1]	P	Cap Output port from internal Regulators (connect to GND through a 1uF capacitor)
AVDD[1:0]	P	Analog Power
AVSS[1:0]	G	Analog Ground

MODE2	MODE1	MODE0	Mode Description
0	0	0	User Normal/Debug Mode
0	0	1	User Flash Writing Tool Mode
0	1	0	User UART SPGM Tool Mode
1	0	1	SCAN Mode (Only for Test)

3 SYSTEM MEMORY MANAGEMENT

3.1 Default Memory Map

The S3FM02G has memory space allocation as below.

Table 3-1 Memory Map

Address	Memory
Reserved	Reserved
0xE00F_FFFF ~ 0xE000_0000	Cortex™-M3 Internal Peripheral Registers
Reserved	Reserved
0x8000_3FFF ~ 0x8000_0000	16 Kbytes Internal Data Flash Memory
Reserved	Reserved
0x400F_FFFF ~ 0x4000_0000	Special Function Registers
Reserved	Reserved
0x2000_5FFF ~ 0x2000_0000	24 Kbytes Internal SRAM Memory
Reserved	Reserved
0x0005_FFFF ~ 0x0000_0000	384 Kbytes Internal Program Flash Memory

3.2 Special Function Register Map

3.2.1 Core Special Function Register Map

Table 3-2 Core Special Function Register Map

Base Address	Peripheral	Description
0xE00F_F000	ROM Table	ROM memory table
0xE004_2000	External PPB	Private Peripheral Bus
0xE004_1000	ETM	Embedded Trace Macro Register
0xE004_0000	TPIU	Trace Port Interface
0xE000_F000	Reserved	–
0xE000_E000	SCS	System Control Space
0xE000_3000	Reserved	–
0xE000_2000	FPB	Flash Patch & Break Pint
0xE000_1000	DWT	Data Watch Point & Trace
0xE000_0000	ITM	Instrumentation Trace Macro-cell

3.2.2 Peripheral Special Function Register Map

Table 3-3 Peripheral Memory Map

Peripheral Group	Base Address	Peripheral	Description
DMAC	0x400F_0000	DMAC	Direct Memory Access Controller
CAN	0x400E_1000	CAN1	Controller Area Network 1
	0x400E_0000	CAN0	Controller Area Network 0
LCDC	0x400D_0000	LCDC	LCD Controller
ENC	0x400C_1000	ENC1	Encoder Counter 1
	0x400C_0000	ENC0	Encoder Counter 0
IMC	0x400B_1000	IMC1	Inverter Motor Controller1
	0x400B_0000	IMC0	Inverter Motor Controller0
I2C	0x400A_1000	I2C1	Inter-Integrated Circuit 1
	0x400A_0000	I2C0	Inter-Integrated Circuit 0
SSP	0x4009_1000	SSP1	Synchronous Serial Port 1
	0x4009_0000	SSP0	Synchronous Serial Port 0
USART	0x4008_3000	USART3	Universal Sync/Async Receiver/Transmitter 3
	0x4008_2000	USART2	Universal Sync/Async Receiver/Transmitter 2
	0x4008_1000	USART1	Universal Sync/Async Receiver/Transmitter 1
	0x4008_0000	USART0	Universal Sync/Async Receiver/Transmitter 0
STT	0x4007_8000	STT	Stamp Timer
PWM	0x4007_7000	PWM7	Pulse Width Modulation 7 (16bit)

Peripheral Group	Base Address	Peripheral	Description
	0x4007_6000	PWM6	Pulse Width Modulation 6 (16bit)
	0x4007_5000	PWM5	Pulse Width Modulation 5 (16bit)
	0x4007_4000	PWM4	Pulse Width Modulation 4 (16bit)
	0x4007_3000	PWM3	Pulse Width Modulation 3 (16bit)
	0x4007_2000	PWM2	Pulse Width Modulation 2 (16bit)
	0x4007_1000	PWM1	Pulse Width Modulation 1 (16bit)
	0x4007_0000	PWM0	Pulse Width Modulation 0 (16bit)
TIMER/ Counter	0x4006_7000	TC7	Timer/Counter 7 (16bit)
	0x4006_6000	TC6	Timer/Counter 6 (16bit)
	0x4006_5000	TC5	Timer/Counter 5 (16bit)
	0x4006_4000	TC4	Timer/Counter 4 (16bit)
	0x4006_3000	TC3	Timer/Counter 3 (16bit)
	0x4006_2000	TC2	Timer/Counter 2 (16bit)
	0x4006_1000	TC1	Timer/Counter 1 (16bit)
	0x4006_0000	TC0	Timer/Counter 0 (16bit)
GPIO	0x4005_8000	IOCONF	IO Configuration
	0x4005_3000	GPIO3	General Purpose IO Group 3
	0x4005_2000	GPIO2	General Purpose IO Group 2
	0x4005_1000	GPIO1	General Purpose IO Group 1
	0x4005_0000	GPIO0	General Purpose IO Group 0
OPAMP	0x4004_2000	OPAMP	OP-AMP
ADC	0x4004_1000	ADC1	Analog to Digital Converter 1 (10bit)
	0x4004_0000	ADC0	Analog to Digital Converter 0 (12bit)
FRT	0x4003_1000	FRT	Free Running Timer (32bit)
WDT	0x4003_0000	WDT	Watchdog Timer
SYSTEM	0x4002_0000	CM	System(Clock, Reset and Power) Manager
MEMORY	0x4001_1000	DFC	Data Flash Controller
	0x4001_0000	PFC	Program Flash Controller
SFM	0x4000_0000	–	Device information including Chip ID

4 ELECTRICAL DATA

4.1 Absolute Maximum Ratings

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. The functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
DC Supply Voltage for V_{DDCORE}	V_{DDCORE}	–	–0.3 to 6.0	V
DC Supply Voltage for V_{DDIO}	V_{DDIO}	–	–0.3 to 6.0	V
DC Supply Voltage for AV_{DD}	AV_{DD}	–	–0.3 to 6.0	V
DC Supply Voltage for AV_{REF}	AV_{REF}	–	–0.3 to 6.0	V
Digital I/O Input Voltage	V_{IN}	–	–0.3 to V_{DDIO}+0.3	V
Analog I/O Input Voltage	AV_{IN}	–	–0.3 to AV_{DD}+0.3	V
DC Digital Input Current	I_{IN_D}	All Input Pins	–	mA
	–	Per Pin	–	mA
DC Analog Input Current	I_{IN_A}	All Input Pins	–	mA
		Per Pin	–	mA
Output Current Low	I_{O_LOW}	All Output Pins	–	mA
	–	Per Pin	–	mA
Output Current High	I_{O_HIGH}	All Output Pins	–	mA
	–	Per Pin	–	mA
Output Voltage	V_O	All Output Pins	–0.3 to V_{DDIO}+0.3	V
Operating Temperature	T_A	–	–40 to 85	°C
Storage Temperature	T_{STG}	–	–65 to 155	°C

NOTE: The device is not guaranteed to operate properly above those listed in 'Absolute Maximum Ratings'.

4.2 Recommended Operation Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

Table 4-2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Rating	Unit
DC Supply Voltage for V_{DD} Core	V_{DDCORE}	–	2.7 to 5.5	V
DC Supply Voltage for I/O	V_{DDIO}	–	2.7 to 5.5	V
DC Supply Voltage for AV_{DD}	AV_{DD}	–	2.7 to 5.5	V
DC Supply Voltage for AV_{REF}	AV_{REF}	–	0.0 to 5.5	V
Operating Temperature	T_A	–	–40 to 85	°C

4.3 I/O D.C. Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	X_{IN} = 4MHz ~ 8MHz, PLLCLK = 75MHz	2.7	–	5.5	V
Input High Voltage	V_{IH1}	All input pins except V_{IH2}	$0.8V_{DD}$	–	V_{DD}	V
	V_{IH2}	X_{IN}, $XT_{IN,}$ MODE[2:0], nRESET	V_{DD} –0.3	–	V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}, $XT_{IN,}$ MODE[2:0], nRESET	–	–	0.3	
Output High Voltage	V_{OH1}	I_{OH} = –1.6mA, V_{DD}=5.0V	V_{DD} –0.4	–	–	V
	V_{OH2}	I_{OH}=-20mA, 12 IMC pads, V_{DD}=5.0V (PWM[1:0]U[2:0], PWM[1:0]D[2:0])	V_{DD} –1.0	–	–	V
Output Low Voltage	V_{OL1}	I_{OL} = 1.6mA , V_{DD}=5.0V	–	–	0.4	V
	V_{OL2}	I_{OL}=20mA, 12 IMC pads, V_{DD}=5.0V (PWM[1:0]U[2:0], PWM[1:0]D[2:0])	–	–	1.0	V
Input High Leakage Current	I_{LIH1}	V_{IN}=V_{DD}, All input pins except MODE[2:0] and I_{LIH2}	–	–	1	µA
	I_{LIH2}	V_{IN}=V_{DD}, X_{IN}, XT_{IN}	–	–	20	
Input Low Leakage Current	I_{LIL1}	V_{IN}=0V, All input pins except nRESET and I_{LIL2}	–	–	–1	µA
	I_{LIL2}	V_{IN}=0V, X_{IN}, XT_{IN}	–	–	–20	
Output High Leakage Current	I_{LOH}	V_{OUT}=V_{DD}, All output pins	–	–	3	µA
Output Low Leakage Current	ILOL	V_{OUT}=0V, All output pins	–	–	–3	µA
Pull-up Resistor	R_L	V_{IN}=0V, V_{DD}=5.0V All ports	16	30	60	kΩ

NOTE: All pins are schmitt trigger type

4.4 I/O Capacitance

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I/O Capacitance	C_{IO}	F = 1MHz, unmeasured pins are connected to V_{SS}	–	–	10	pF
Input Capacitance	C_{IN}		–	–	10	
Output Capacitance	C_{OUT}		–	–	10	

4.5 RESET Input Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pull-up Resistor	R_{NRST}	V_{IN}=0V, V_{DD}=5.0V	16	30	60	kΩ
Input Low Width	t_{RSL}	–	0.8	1.2	2	μs

NOTE: If the width of reset pulse is greater than minimum value, the pulse is always recognized as a valid pulse.

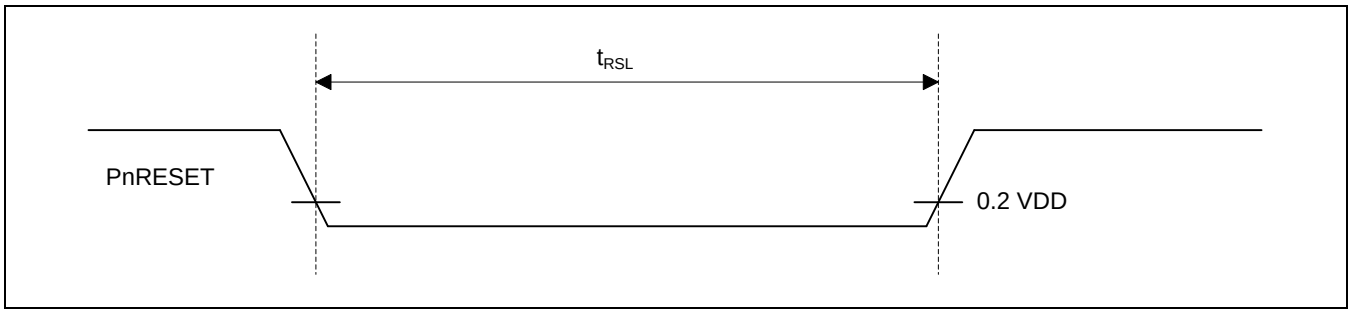


Figure 4-1 Input Timing for nRESET

4.6 External Interrupt Input Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input High Width	t_{INTH}	V_{DD}=5.0V	100	200	300	ns
Interrupt Input Low Width	t_{INTL}	V_{DD}=5.0V	100	200	300	ns

NOTE: If the width of interrupt pulse is greater than minimum value, the pulse is always recognized as a valid pulse.

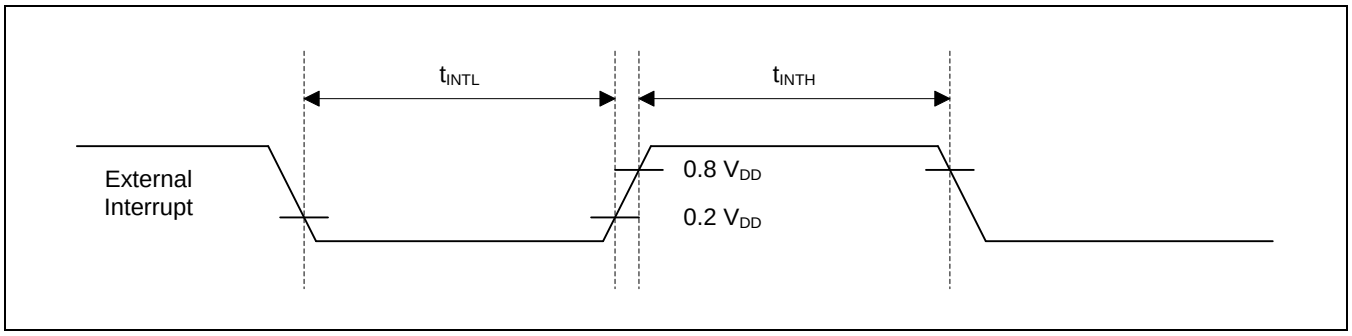
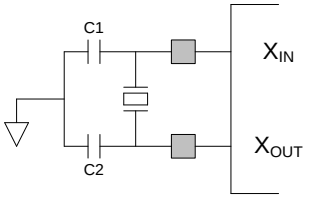
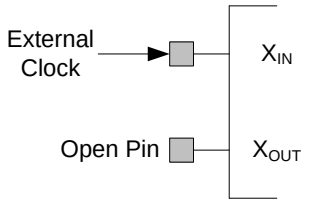


Figure 4-2 Input Timing for External Interrupt

4.7 Oscillator Characteristics

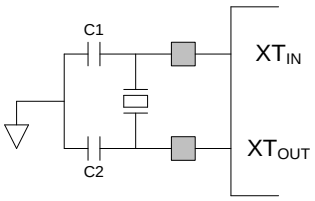
4.7.1 External Main Clock Oscillator Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Oscillator	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator frequency	EMCLK	–	4	–	8	MHz
Stabilization Time	T_{STA}	–	–	–	10	ms
Crystal/Resonator/ Ceramic	EMCLK		4	–	8	MHz
External Clock	EMCLK		4	–	8	MHz

4.7.2 External Sub Clock Oscillator Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Oscillator	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator frequency	ESCLK	–	–	32.768	–	KHz
Stabilization Time	T_{STA}	–	–	–	10	s
Crystal/Resonator/ Ceramic	ESCLK		–	32.768	–	KHz

4.7.3 Internal Main Clock Oscillator Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Oscillator	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator frequency	IMCLK16	V_{DD}=5.0V	–	8/16	–	MHz
	IMCLK20		–	20	–	MHz
Output clock duty ratio	–	V_{DD}=5.0V	40	–	60	%
Accuracy	–	V_{DD}=5.0V, $\mathbf{T_A}$ = 25'C	–	–	±1	%
	–	V_{DD}=2.7~5.5V, $\mathbf{T_A}$ = 0~70'C	–	–	±2	%
	–	V_{DD}=5.0V, $\mathbf{T_A}$ = –40~85'C	–	–	±3	%
	–	V_{DD}=2.7~5.5V, $\mathbf{T_A}$ = –40~85'C	–	–	±5	%
Stabilization Time	T_{STA}	–	–	–	2	ms

4.7.4 Internal Sub Clock Oscillator Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Oscillator	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator frequency	ISCLK	V_{DD}=5.0V	–	32.768	–	KHz
Output clock duty ratio	–	V_{DD}=5.0V	40	–	60	%
Accuracy	–	**T_A = –40 to 85 °C**	–	–	±50	%
Stabilization Time	T_{STA}	–	–	–	500	µs

4.7.5 PLL Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input frequency	F_{IN}	–	4	–	8	MHz
Output frequency	F_{OUT}		8	–	75	MHz
Clock Duty Ratio	T_{OD}		40	50	60	%
Locking Time	T_{LT}		–	–	200	µs

4.8 Current Consumption

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 5.5V)

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
Supply Current	I_{DD111}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK = 8MHz	Normal operating 11	–	13	26	mA
	I_{DD112} (3)	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK = 4MHz	Normal operating 11	–	10	20	mA
	I_{DD121} (3)	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK = 20MHz	Normal operating 12	–	20	40	mA
	I_{DD122} (3)	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK = 8MHz	Normal operating 12	–	10	20	mA
	I_{DD2}	Enable PLL Enable EMCLK, IMCLK, ESCLK, and ISCLK Run CPU by PLLCLK	High-speed operating	–	50	90	mA
	I_{DD31}	CPU stops in I_{DD11} Condition.	Normal idle 1	–	6	12	mA
	I_{DD32} (3)	CPU stops in I_{DD12} Condition.	Normal idle 2	–	6	12	mA
	I_{DD4}	CPU stops in I_{DD2} Condition.	High-speed idle	–	10	20	mA
	I_{DD51} (3)	Disable EMCLK, and IMCLK Enable ESCLK, and ISCLK Enable all peripherals Run CPU by ESCLK	Sub-operating 1	–	5	10	mA
	I_{DD52} (3)	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK Enable all peripherals	Sub-operating 2	–	5	10	mA

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
		Run CPU by ISCLK					
	I_{DD61} (3)	CPU stops in I_{DD51} Condition. LVD OFF, LCD OFF	Sub-idle 1	–	4	8	mA
	I_{DD62} (3)	CPU stops in I_{DD52} Condition. LVD OFF, LCD OFF	Sub-idle 2	–	4	8	mA
	I_{DD71}	Disable EMCLK, IMCLK, ESCLK, and ISCLK All peripherals stop. LVD OFF, LCD OFF	Stop 1	–	0.5	1	mA
	I_{DD72} (3)	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK, FRT LVD OFF, LCD OFF	Stop 2	–	0.6	1	mA

NOTE:

1. Supply Current does not include current drawn through internal pull-up resistor, LCD voltage dividing resistors, and external output current loads.
2. Above tables, the current is based on LVD-OFF condition.
3. These values are only characterization data, and not tested in the mass production.

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 3.3V) (3)

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
Supply Current	I_{DD111}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK = 8MHz	Normal operating 11	–	10	20	mA
	I_{DD112}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK = 4MHz	Normal operating 11	–	7	14	mA
	I_{DD121}	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK = 20MHz	Normal operating 12	–	17	34	mA
	I_{DD122}	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK = 8MHz	Normal operating 12	–	8	16	mA
	I_{DD2}	Enable PLL Enable EMCLK, IMCLK, ESCLK, and ISCLK Run CPU by PLLCLK	High-speed operating	–	45	85	mA
	I_{DD31}	CPU stops in I_{DD11} Condition.	Normal idle 1	–	3	6	mA
	I_{DD32}	CPU stops in I_{DD12} Condition.	Normal idle 2	–	3	6	mA
	I_{DD4}	CPU stops in I_{DD2} Condition.	High-speed idle	–	7	14	mA
	I_{DD51}	Disable EMCLK, and IMCLK Enable ESCLK, and ISCLK Enable all peripherals Run CPU by ESCLK	Sub-operating 1	–	3	6	mA
	I_{DD52}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK Enable all peripherals Run CPU by ISCLK	Sub-operating 2	–	3	6	mA
	I_{DD61}	CPU stops in I_{DD51} Condition. LVD OFF, LCD OFF	Sub-idle 1	–	2	4	mA
	I_{DD62}	CPU stops in I_{DD52} Condition. LVD OFF, LCD OFF	Sub-idle 2	–	2	4	mA
	I_{DD71}	Disable EMCLK, IMCLK, ESCLK, and ISCLK All peripherals stop.	Stop 1	–	0.5	1	mA

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
		LVD OFF, LCD OFF					
	I_{DD72}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK, FRT LVD OFF, LCD OFF	Stop 2	–	0.5	1	mA

NOTE:

1. Supply Current does not include current drawn through internal pull-up resistor, LCD voltage dividing resistors, and external output current loads.
2. Above tables, the current is based on LVD-OFF condition.
3. 3.3V data is only characteristic data. These values are not tested in the mass production

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V) (3)

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
Supply Current	I_{DD111}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK = 8MHz	Normal operating 11	–	9	18	mA
	I_{DD112}	Enable EMCLK, IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by EMCLK = 4MHz	Normal operating 11	–	6	12	mA
	I_{DD121}	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK = 20MHz	Normal operating 12	–	17	34	mA
	I_{DD122}	Disable EMCLK Enable IMCLK, ESCLK, and ISCLK Enable all peripherals Run CPU by IMCLK = 8MHz	Normal operating 12	–	8	16	mA
	I_{DD2}	Enable PLL Enable EMCLK, IMCLK, ESCLK, and ISCLK Run CPU by PLLCLK	High-speed operating	–	44	85	mA
	I_{DD31}	CPU stops in I_{DD11} Condition.	Normal idle 1	–	2	5	mA
	I_{DD32}	CPU stops in I_{DD12} Condition.	Normal idle 2	–	2	5	mA
	I_{DD4}	CPU stops in I_{DD2} Condition.	High-speed idle	–	7	14	mA
	I_{DD51}	Disable EMCLK, and IMCLK Enable ESCLK, and ISCLK Enable all peripherals Run CPU by ESCLK	Sub-operating 1	–	2	5	mA
	I_{DD52}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK Enable all peripherals Run CPU by ISCLK	Sub-operating 2	–	2	5	mA
	I_{DD61}	CPU stops in I_{DD51}	Sub-idle 1	–	1	3	mA

Parameter	Symbol	Condition	Mode	Min.	Typ.	Max.	Unit
		Condition. LVD OFF, LCD OFF					
	I_{DD62}	CPU stops in I_{DD52} Condition. LVD OFF, LCD OFF	Sub-idle 2	–	1	3	mA
	I_{DD71}	Disable EMCLK, IMCLK, ESCLK, and ISCLK All peripherals stop. LVD OFF, LCD OFF	Stop 1	–	0.5	1	mA
	I_{DD72}	Disable EMCLK, IMCLK, and ESCLK Enable ISCLK, FRT LVD OFF, LCD OFF	Stop 2	–	0.5	1	mA

NOTE:

1. Supply Current does not include current drawn through internal pull-up resistor, LCD voltage dividing resistors, and external output current loads.
2. Above tables, the current is based on LVD-OFF condition.
3. 2.7V data is only characteristic data. These values are not tested in the mass production

4.9 LVD Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Oscillator	Symbol	Conditions	Min	Typ	Max	Unit
LVD Detect Voltage	V_{LVD0}	Reset Default	2.5	2.6	2.7	V
	V_{LVD1}		2.6	2.8	3.0	
	V_{LVD2}		3.5	3.75	4.0	
	V_{LVD3}		4.0	4.25	4.5	
Hysteresis of V_{LVD} (Slew Rate of LVD)	ΔV	–	–	100	200	mV

NOTE: User can select the level for reset and interrupt voltage by LVDRL[2:0] and LVDIL[2:0] in CM_MR0 register

4.10 12-Bit ADC0 Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	–	–	–	12	–	Bit
Supply Voltage	AV_{DD0}	–	2.7	5	5.5	V
Reference Voltage	AV_{REF}	–	2.7	–	AV_{DD0}	V
Input Voltage Range	V_{AIN0}	–	0	–	AV_{REF}	V
Clock Frequency	F_{ADC0}	50% duty cycle	–	–	5	MHz
Maximum Conversion Time	t_{ADC0}	Max. F_{ADC0} AV_{DD0} = AV_{REF}	–	–	1	MSPS
Differential nonlinearity	DNL	AV_{DD0} = AV_{REF} AV_{SS0} = 0.0V	–	–	±1.5	LSB
Integral nonlinearity	INL	AV_{DD0} = AV_{REF} AV_{SS0} = 0.0V	–	–	±3.5	LSB
Offset Error (unadjusted)(1)	TOPOFF	AV_{REF} = 5.5V	–	–	AV_{REF} - 43	mV
		AV_{REF} = 2.7V	–	–	AV_{REF} - 22	mV
	BOTOFF	AV_{REF} = 5.5V	–	–	43	mV
		AV_{REF} = 2.7V	–	–	22	mV
Operation Current	I_{OP}	AV_{DD0} = AV_{REF} = 5.0V AV_{SS0} = 0.0V	–	7.5	10	mA
Power down Current	I_{PD}	AV_{DD0} = AV_{REF} = 5.0V AV_{SS0} = 0.0V	–	20	30	μA

NOTE: When Internal Calibration mode is set, the 1/4 and 3/4 values of V_{REF} are stored in ADC_OCR registers but these values can't be used for getting accurate compensation (calibration) because of the offset difference in the customer board environment. Therefore external calibration is better to be used for more accurate calibration. More detail information is shown in ADC0 section.

4.10.1 OP-AMP Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	$\|V_{IO}\|$	–	–	–	±9	mV
Input Voltage Range	V_I	Gain = 2.32 to 4.09	$0.04AV_{DD0}$	–	$0.36AV_{DD0}$	V
		Gain = 4.53 to 5.92	$0.02AV_{DD0}$	–	$0.18AV_{DD0}$	V
		Gain = 7.09, 8.86	$0.01AV_{DD0}$	–	$0.085AV_{DD0}$	V
Slew Rate	S_R	@CL = 10pF	10	15	-	V/μs
		@CL = 50pF	–	10	-	V/μs
Gain Error	G_E	Gain = 2.32 to 4.53, T_A = 25°C	–	±1.0	±2.0	%
		Gain = 5.04 to 8.86, T_A = 25°C	–	±1.5	±3.0	%
		Gain = 2.32 to 4.53, T_A = –40 to 85 °C	–	±2.0	±4.0	%
		Gain = 5.04 to 8.86, T_A = –40 to 85 °C	–	±3.0	±6.0	%

4.11 10-Bit ADC1 Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution	–	–	–	10	–	Bit
Supply Voltage	AV_{DD1}	–	2.7	5	5.5	V
Reference Voltage	AV_{REF}	–	2.7	–	AV_{DD1}	V
Input Voltage Range	V_{AIN1}	–	0	–	AV_{REF}	V
Clock Frequency	F_{ADC1}	50% duty cycle	–	–	700	㎑
Maximum Conversion Time	t_{ADC1}	Max. F_{ADC1} AV_{DD1} = AV_{REF}	–	–	50	KSPS
Differential nonlinearity	DNL	AV_{DD1} = AV_{REF} AV_{SS1} = 0.0V	–	–	±1	LSB
Integral nonlinearity	INL	AV_{DD1} = AV_{REF} AV_{SS1} = 0.0V	–	–	±1.5	LSB
Offset Error (unadjusted)	TOPOFF	AV_{REF} = 5.5V	–	–	AV_{REF} - 172	mV
		AV_{REF} = 2.7V	–	–	AV_{REF} - 85	mV
	BOTOFF	AV_{REF} = 5.5V	–	–	172	mV
		AV_{REF} = 2.7V	–	–	85	mV
Operation Current	I_{OP}	AV_{DD1} = AV_{REF} = 5.0V AV_{SS1} = 0.0V	–	0.2	1	mA
Power down Current	I_{PD}	AV_{DD1} = AV_{REF} = 5.0V AV_{SS1} = 0.0V	–	1	2	μA

4.12 LCD Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
LCD voltage dividing resistor	R_{LCD1}	–	LCDC_CR.17=0	40	60	80	kΩ
	R_{LCD2}		LCDC_CR.17=1	20	30	40	kΩ
$\|V_{LCD}$ - COMi$\|$ voltage drop (i=0 ~ 3)	V_{DC}	–15μA per common pin		–	–	120	mV
$\|V_{LCD}$ - SEGi$\|$ voltage drop (i=0 ~ 39)	V_{DS}	–15μA per common pin		–	–	120	mV
Middle Output Voltage	V_{LCD1}	–		$0.67V_{DD}$-0.2	–	$0.67V_{DD}$+0.2	V
	V_{LCD2}			$0.33V_{DD}$-0.2	–	$0.33V_{DD}$+0.2	V

4.13 Memory Characteristics

4.13.1 Program Flash Memory Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Total Size	F_{SIZE}	–	–	384	–	KB
Program Size	F_{WSIZE}	–	–	4	–	B
Page Size	F_{PSIZE}	–	–	1024	–	B
Sector Size	F_{SSIZE}	–	–	32	–	KB
Programming Time for 1 Word	F_{TW}	–	20	25	30	µs
Page Erase Time	F_{TPERA}	–	4	8	12	ms
Sector Erase Time	F_{TSERA}	–	12	20	28	ms
Chip Erase Time	F_{TCERA}	–	32	50	70	ms
Read Command to valid data	F_{RA}	–	–	–	50	ns
Endurance Number of writing/erasing	F_{NWE}	–	10,000	–	–	Times
Data Retention	F_{TDR}	–	10	–	–	Years

NOTE: Flash hardware operating times: Total flash operating (program/erase) time may depend upon the software

4.13.2 Data FLASH Memory Characteristics

(T_A = –40 to 85 °C, V_{DD} = V_{DDCORE} = V_{DDIO} = AV_{DD} = 2.7V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Total Size	F_{SIZE}	–	–	16	–	KB
Program Size	F_{WSIZE}	–	1	2	4	B
Page Size	F_{PSIZE}	–	–	256	–	B
Sector Size	F_{SSIZE}	–	–	1	–	KB
Programming Time for 1 Word	F_{TW}	–	20	25	30	µs
Page Erase Time	F_{TPERA}	–	4	8	12	ms
Sector Erase Time	F_{TSERA}	–	12	20	28	ms
Chip Erase Time	F_{TCERA}	–	32	50	70	ms
Read Command to valid data	F_{RA}	–	–	–	100	ns
Endurance Number of writing/erasing	F_{NWE}	–	100,000	–	–	Times
Data Retention	F_{TDR}	–	10	–	–	Years

NOTE: Flash hardware operating times: Total flash operating (program/erase) time may depend upon the software

4.14 ESD Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Electrostatic discharge	V_{ESD}	HBM	2000	–	–	V
		MM	200	–	–	V
		CDM	500	–	–	V

5 PACKAGE SPECIFICATION

5.1 Overview

This chapter describes the package information of S3FM02G. It is available in a 128-ETQFP-1414 package type.

Table 5-1 Absolute Maximum Ratings

Package Number	128-ETQFP-1414
Package Width / Package Length	14.0 / 14.0 mm
Mounting Height	1.20 mm MAX
Lead Pitch	0.40 mm

5.2 Package Dimension

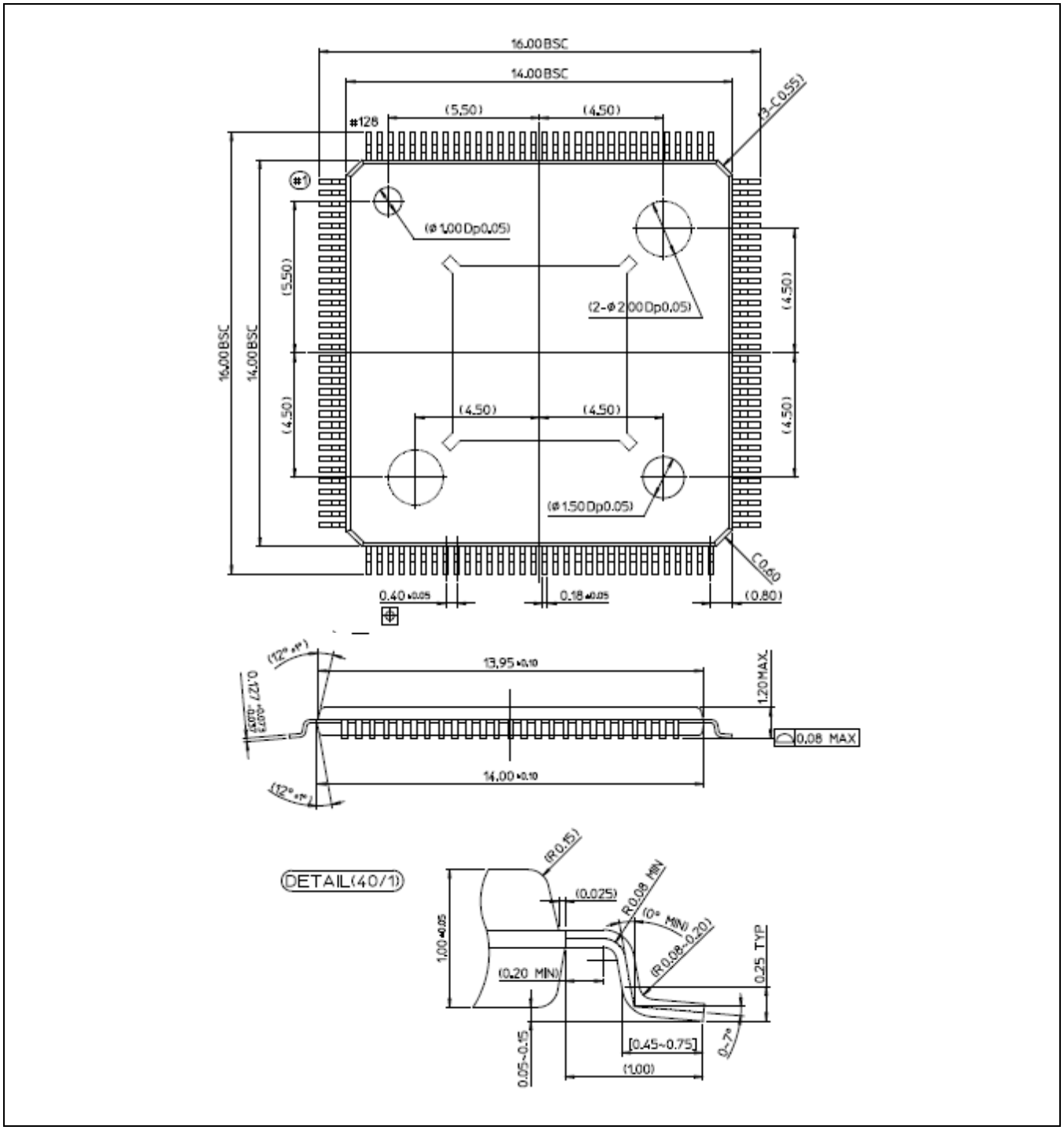


Figure 5-1 128ETQFP-1414 Package Dimension