TDA8028, TDA8008
Dual multiprotocol smart card coupler

Objective speci®cation v4.0 February 2000

FEATURES

- 8xC51 core with 16kBytes ROM (TDA8028) or EPROM (TDA8008), 256Bytes RAM, 512Bytes AUXRAM, Timer 0, 1, 2 and Enhanced UART
- Specific ISO7816 UART, accessible with MOVX instructions for automatic convention processing, variable baud rate through frequency or division ratio programming, error management at character level for T=0 protocol, extra guard time register
- Dual V_{CC} generation (5V+/-5% or 3V+/-5%), max current 60mA with controlled rise and fall times
- Dual Cards clock generation (up to 10MHz) with two times synchronous frequency doubling
- Cards clock STOP HIGH or LOW or 1.25MHz (from an integrated oscillator) for cards power reduction mode
- Automatic activation and deactivation sequences through independent sequencers
- Supports the asynchronous protocols T=0 and T=1 in accordance with ISO7816 and EMV
- Versatile 24Bits time-out counter for ATR and waiting times processing
- 22 ETU counter for Block Guard Time
- Supports synchronous cards
- Current limitations on cards contacts and emergency deactivation in case of overcosumption or overheating
- Special circuitry for killing spikes during power-on or off
- Supply supervisor for power on/off reset
- Step up converter (supply voltage from 2.7V to 5.5V @16MHz), doubler, tripler or follower according to V_{CC} and V_{DD}
- Speed up to 25MHz at V_{DD} = 5V
- Additional I/O pin allowing the use of the ISO7816 UART for an external card interface (IOAUX)
- Additional interrupt pin allowing detection of level toggling on an external signal (INTAUX)
- Fast and efficient swapping between the 3 cards due to separate buffering of parameters for each card
- Chip select input allowing use of several devices in parallel and memory space paging
- Enhanced ESD protections on cards contacts (6kV min)
- Software library for easy integration within the application
- Development tool with a TDA8007B and a regular emulator

APPLICATIONS

- Multiple smart card readers for multiprotocol applications (EMV Banking, Digital Pay TV, Access control, etc.)

GENERAL DESCRIPTION

The TDA8028/TDA8008 is a complete, one chip, low cost dual smart card coupler.

It can be used as the kernel of a multiple card reader. It takes care of all ISO7816, EMV and GSM11-11 requirements. The integrated ISO7816 UART and the time-out counters allow easy use even at high baudrates with no real time constraints. Due to its chip select and external I/O and interrupt features, it simplifies a lot the realization of any number of cards reader. It gives the cards and the set a very high level of security, due to its special hardware against ESD, short-circuiting, power failure, overheating. Its integrated step-up converter allows operation within a supply voltage range of 2.7V to 5.5V @16MHz.

The OTP version (TDA8008) allows fast and reliable software development, and fast product introduction waiting for the ROM version. ROM versions in smaller packages (LQFP64) are available.

A software library has been developed, taking care of all actions required for T=0, T=1 and synchronous protocols.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	VDDD = VDDA = VDDP	2.7	–	5.5	V
$I_{DD(pd)}$	supply current in power-down mode	V_{DD}=3.3V; cards inactive; 8xC51 Controller in Power-Down Mode	–	–	tbf	µA
$I_{DD(sm)}$	supply current in sleep mode	V_{DD}=3.3V; cards active at V_{CC}=5V; CLK stopped; 8xC51 Controller in IDLE Mode	–	–	tbf	mA
$I_{DD(om)}$	supply current in operating mode	V_{DD}=3.3V; f_{XTAL1}=20MHz VCC1=VCC2=5V; ICC1+ICC2=80mA	–	-	tbf	mA
V_{CC}	card supply voltage	including static loads (5V card)	4.75	5.0	5.25	V
		with 40nAs dynamic loads on 200nF capacitor (5V card)	4.6		5.4	V
		including static loads (3V card)	2.78		3.22	V
		with 40nAs dynamic loads on 200nF capacitor (3V card)	2.75		3.25	V
I_{CC}	card supply current	operating	–	–	65	mA
		overload detection	–	100		mA
ICC1 + ICC2	sum of both cards currents				80	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 300nF	0.05	0.16	0.22	V/µs
t_{de}	deactivation cycle duration		–	–	100	µs
t_{act}	activation cycle duration		–	–	130	µs
f_{xtal}	crystal frequency		3.5	–	25	MHz
f_{op}	operating frequency	external frequency applied on XTAL1	0		25	MHz
T_{amb}	operating ambient temperature		–25	–	+85	°C

Note

1. I_{DD} in all configurations include the current at pins VDDD, VDDA and VDDP.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8008HL	LQFP80	80 lead Plastic Quad Flat Pack; body 12 x 12 x 1.4 mm	SOT 315
TDA8028HL	LQFP80	80 lead Plastic Quad Flat Pack; body 12 x 12 x 1.4 mm	SOT 315
TDA8028AHL	LQFP64	64 lead Plastic Quad Flat Pack; body 10 x 10 x 1.4 mm	SOT 314

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *Quality Reference Handbook* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

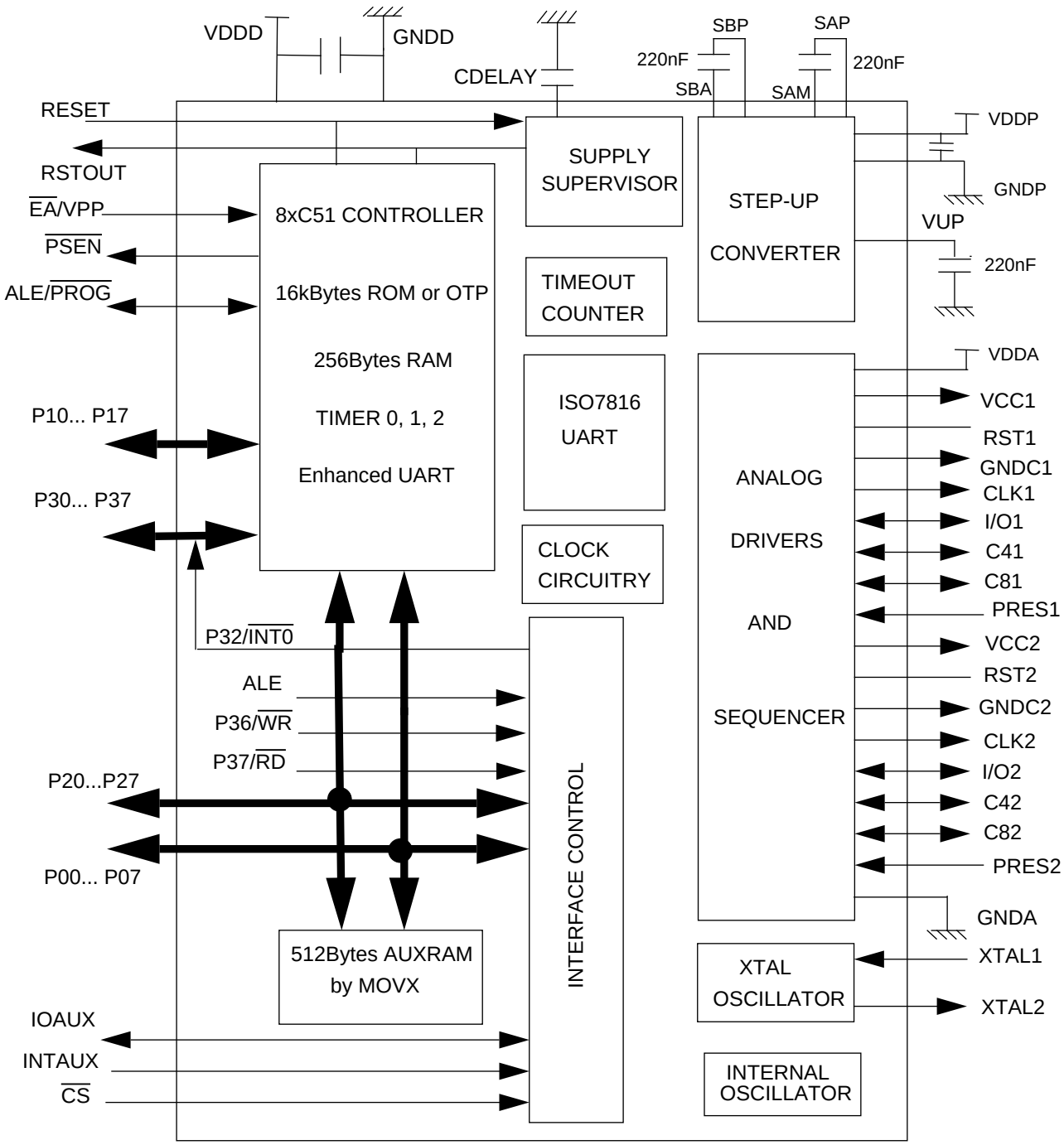


Fig.1 Block diagram

PINNING

SYMBOL	PIN		DESCRIPTION
	LQFP80	LQFP64	
P16	1	-	8xC51 general purpose I/O port
P17	2	-	8xC51 general purpose I/O port
RESET	3	1	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to GNDD permits a power-on reset using an external capacitor to VDDD.
VDDA	4	2	Analog Power Supply
GNDA	5	3	Analog Ground
CDELAY	6	4	Pin for an external delay capacitor
INHIB	7	-	Test pin (must be left open in the application)
PRES2	8	5	Card2 presence contact input (active HIGH or LOW by mask option)
IO2	9	6	Data line to/from card2 (ISO C7 contact)
C82	10	7	Auxiliary I/O for ISO C8 contact (synchronous cards for instance) for card2
C42	11	8	Auxiliary I/O for ISO C4 contact (synchronous cards for instance) for card2
RST2	12	9	Card2 reset output (ISO C2 contact)
VCC2	13	10	Card2 supply output voltage (ISO C1 contact)
CLK2	14	11	Clock output to card2 (ISO C3 contact)
GNDC2	15	12	Ground for card2
SAM	16	13	Contact 2 for the step-up converter (Connect a Low ESR 220nF capacitor between SAP and SAM)
GNDP	17	14	Ground connection for the step-up converter
SBM	18	15	contact 4 for the step-up converter (Connect a Low ESR 220nF capacitor between SBP and SBM)
VDDP	23	17	Positive supply voltage for the step-up converter
SBP	24	18	contact 3 for the step-up converter (Connect a Low ESR 220nF capacitor between SBP and SBM)
SAP	25	19	contact 1 for the step-up converter (Connect a Low ESR 220nF capacitor between SAP and SAM)
VUP	26	20	Output of the step-up converter
GNDC1	27	21	Ground for card1
CLK1	28	22	Clock output to card1 (ISO C3 contact)
VCC1	29	23	Card1 supply output voltage (ISO C1 contact)
RST1	30	24	Card1 reset output (ISO C2 contact)
C41	31	25	Auxiliary I/O for ISO C4 contact (synchronous cards for instance) for card1
PRES1	32	26	Card1 presence contact input (active HIGH or LOW by mask option)
C81	33	27	Auxiliary I/O for ISO C8 contact (synchronous cards for instance) for card1
IO1	34	28	Data line to/from card1 (ISO C7 contact)
INTAUX	35	29	Auxiliary interrupt input
TEST	36	-	Test pin (must be left open in the application)
IOAUX	37	-	Input or output for an I/O line issued of an auxiliary smart card interface
$\overline{CS}$	38	30	Chip select input (active low)

RSTOUT	39	31	Open drain output for resetting external chips
P30/RxD	41	32	8xC51 general purpose I/O port / serial input port
P31/TxD	42	33	8xC51 general purpose I/O port / serial output port
P32/$\overline{\text{INT0}}$	43	-	8xC51 general purpose I/O port / external interrupt 0
P33/$\overline{\text{INT1}}$	44	34	8xC51 general purpose I/O port / external interrupt 1
P34/T0	45	35?	8xC51 general purpose I/O port / Timer 0 external input
P35/T1	46	36?	8xC51 general purpose I/O port / Timer 1external input
P36/$\overline{\text{WR}}$	47	37	8xC51 general purpose I/O port / external data memory write strobe
P37/$\overline{\text{RD}}$	48	38	8xC51 general purpose I/O port / external data memory read strobe
XTAL2	49	39	Connection pin for an external crystal (output from the inverting oscillator ampli®er)
XTAL1	50	40	Connection pin for an external crystal, or input for an external clock signal (Input to the inverting oscillator ampli®er and input to the internal clock generator circuits)
VDDD	51	41	Digital Power Supply
GNDD	52	42	Digital Ground
P20/A8	53	43	8xC51 general purpose I/O port / address 8
P21/A9	54	44	8xC51 general purpose I/O port / address 9
P22/A10	55	45	8xC51 general purpose I/O port / address 10
P23/A11	56	46	8xC51 general purpose I/O port / address 11
P24/A12	57	47	8xC51 general purpose I/O port / address 12
P25/A13	60	48	8xC51 general purpose I/O port / address 13
P26/A14	61	49	8xC51 general purpose I/O port / address 14
P27/A15	62	50?	8xC51 general purpose I/O port / address 15
$\overline{\text{PSEN}}$	63	51	Program Store Enable: The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
ALE/$\overline{\text{PROG}}$	64	52	Address Latch Enable/Program Pulse: Output pulse for latching the low Byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR Auxiliary.0. With this Bit set, ALE will be active only during a MOVX instruction.
$\overline{\text{EA}}$/VPP	65	53	External Access Enable/Programming Supply Voltage: EAN must be externally held low to enable the device to fetch code from external program memory locations starting with 0000H. If EAN is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (16kBytes boundary). This pin also receives the 12.75V programming supply voltage (VPP) during EPROM programming. If security Bit 1 is programmed, EAN will be internally latched on Reset.
P07/AD7	67	55	8xC51 general purpose I/O port / address/data 7
P06/AD6	68	56	8xC51 general purpose I/O port / address/data 6
P05/AD5	69	57	8xC51 general purpose I/O port / address/data 5
P04/AD4	70	58	8xC51 general purpose I/O port / address/data 4

P03/AD3	71	59	8xC51 general purpose I/O port / address/data 3
P02/AD2	72	60	8xC51 general purpose I/O port / address/data 2
P01/AD1	73	61	8xC51 general purpose I/O port / address/data 1
P00/AD0	74	62	8xC51 general purpose I/O port / address/data 0
P10/T2	75	63?	8xC51 general purpose I/O port / Timer/Counter 2 external count input/Clockout (see Programmable Clock-Out)
P11/T2EX	76	64?	8xC51 general purpose I/O port / Timer/Counter 2 Reload/Capture/Direction Control
P12	77	-	8xC51 general purpose I/O port
P13	78	-	8xC51 general purpose I/O port
P14	79	-	8xC51 general purpose I/O port
P15	80	-	8xC51 general purpose I/O port

Notes

1. LQFP80: Pins 19 to 22, 40, 58, 59 and 66 are Not Connected.
2. LQFP64: Pins 16and 54 are Not Connected.
3. LQFP64: Pinning tbf.

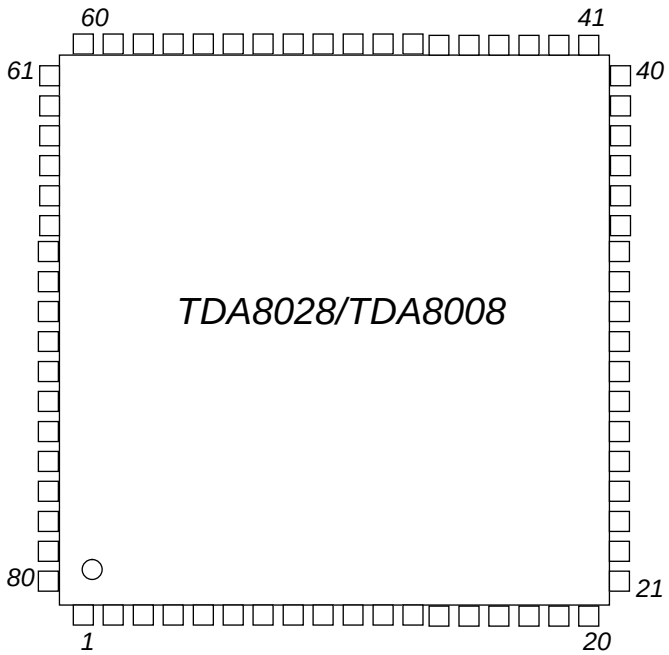


Fig.2 Pin configuration LQFP80

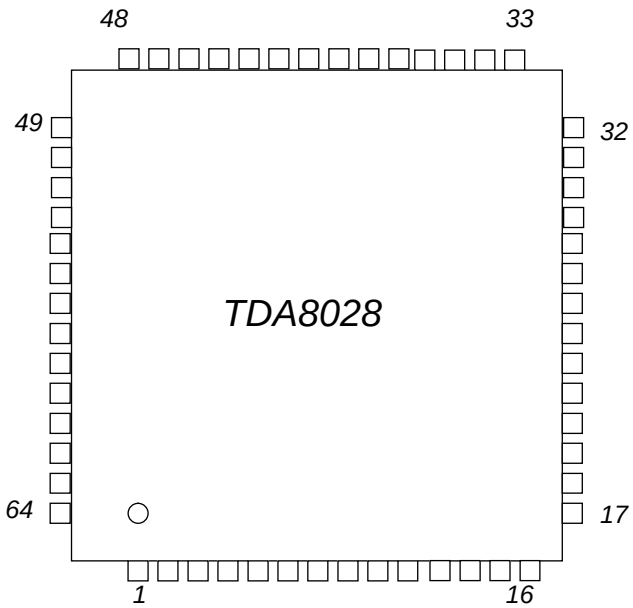


Fig.3 Pin configuration LQFP64

FUNCTIONAL DESCRIPTION

Throughout this specification, it is assumed that the reader is aware of ISO7816 norm terminology.

ISO7816 UART and ASSOCIATED LOGIC

In this section, the description is given of how the integrated ISO7816 UART works, how it may be programmed by means of its control registers and how it is internally interfaced to the embedded microcontroller.

Interface control

The ISO7816 UART may be controlled through an 8Bits parallel bus. This bus is directly, internally connected to the Port0 (P07..P00) of the embedded `C51 microcontroller.

The registers inside the ISO7816 UART may be written or read by using the standard `C51 **MOVX** instructions.

Note, that only if $\overline{CS}$ is LOW, the UART can be accessed.

When $\overline{CS}$ is LOW, the demultiplexing of address and data is done internally by means of the ALE signal. A low pulse on P37/$\overline{RD}$ allows read of the selected register, a low pulse on P36/$\overline{WR}$ allows write into the selected register.

The ISO UART interrupt line is directly, internally connected to the microcontrollers' External Interrupt0 input P32/$\overline{INT0}$. For that reason, the External Interrupt0 of the `C51 controller must be enabled to ensure a proper function.

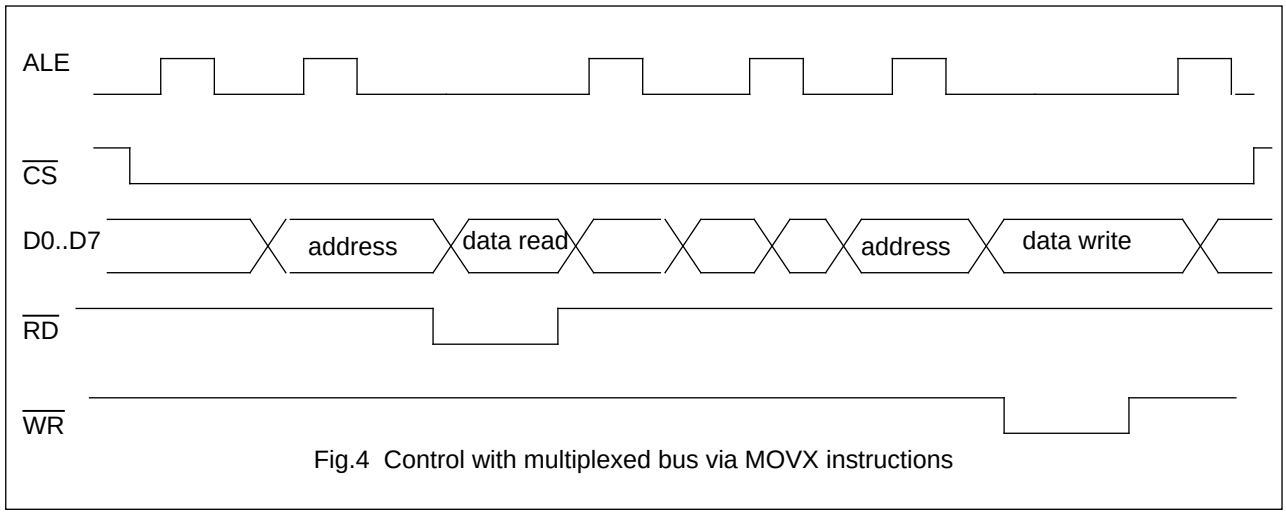


Fig.4 Control with multiplexed bus via MOVX instructions

CONTROL REGISTERS

The TDA8028/TDA8008 has 2 complete analog interfaces which can drive card1 and card2. The data to/from these 2 cards share the same ISO UART. The data to/from a third card (card3), externally interfaced (with a TDA8002 or TDA8003 for example), may also share the ISO UART.

Card 1, 2 and 3 have dedicated registers for setting the parameters of the ISO UART. (PDR: Programmable Divider Register, GTR: Guard Time Register, UCR1: Uart Configuration Register1, UCR2: Uart Configuration Register 2, CCR: Clock Configuration Register).

Cards 1 and 2 also have dedicated registers for controlling their power and their clock configuration. (PCR: Power Control Register) For card 3, these controls are done externally. PCR is also used for writing or reading on the auxiliary cards contacts C4 and C8.

Card1 or card2 or card3 may be selected through the card select register. (CSR) When one card is selected, the corresponding parameters are used by the ISO UART. CSR also contains a bit for resetting the ISO UART (Active LOW). This bit is reset after power on, and must be set to high before starting with anyone of the cards. It may be reset by software when necessary.

When the specific parameters of the cards have been programmed, the UART may be used with the following registers: Uart Receive and Uart Transmit Registers (URR and UTR), Uart Status Register (USR) and Mixed Status Register (MSR) . In reception mode, a FIFO of 1 to 8 characters may be used, and is configurated with the FIFO Control Rgister (FCR).

The Hardware Status Register HSR gives the status of the supply voltage, of the hardware protections and of the card movements.

HSR and USR give interrupts on INT when some of their bits have ben changed.

MSR does not give interrupts and may be used in polling mode for some operations; for this use, some of the interrupt sources within USR and HSR may be masked.

A 24 bits time out counter may be started for giving an interrupt after a number of ETU programmed in registers TOR1, TOR2 and TOR3. It will help the controller for processing different real time tasks (ATR, WWT, BWT etc...) mainly if controllers and cards clock are asynchronous.

This counter is configurated with a register (TOC, Time Out counter Configuration); It may be used as a 24 bits or as a 16bits + 8 bits . Each counter may be set for starting counting once data written, or on detection of a start bit on I/O, or as autoreload.

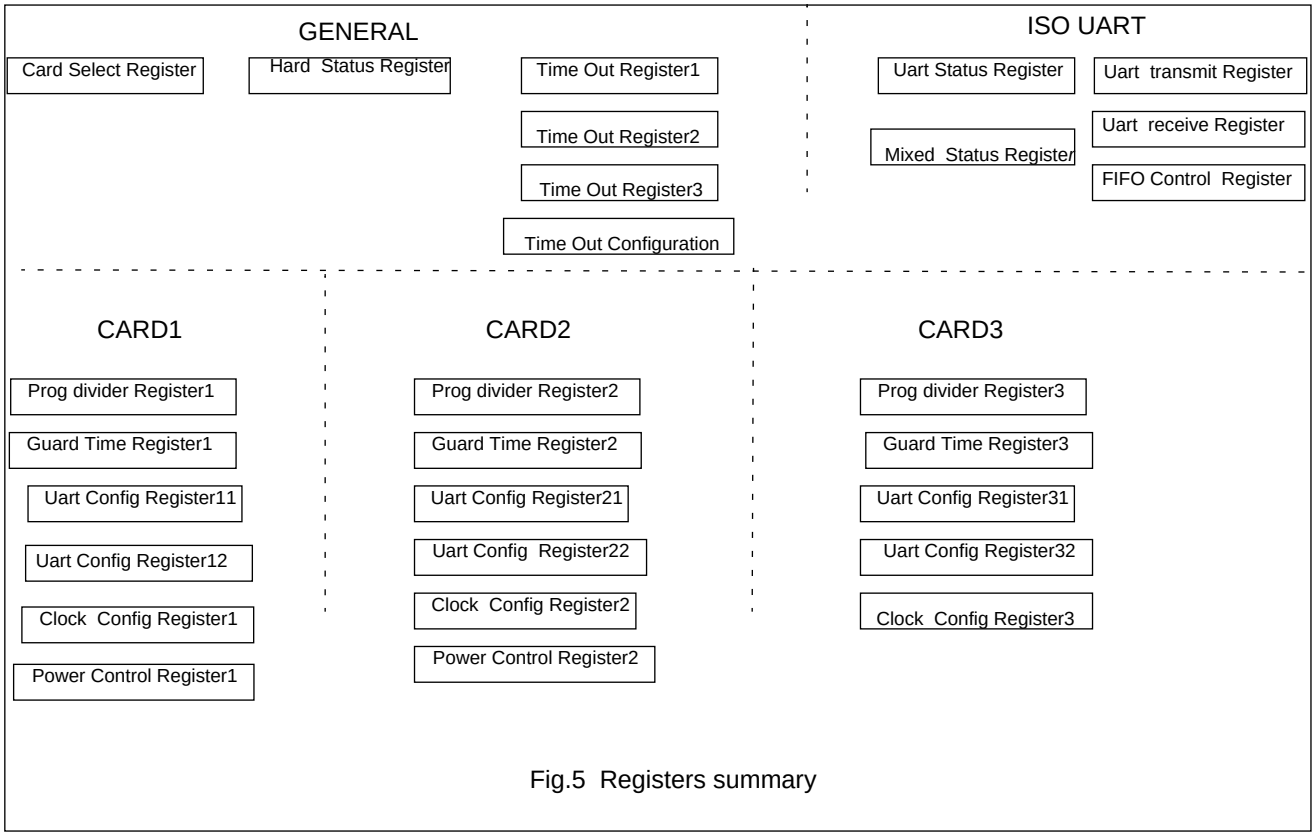


Fig.5 Registers summary

GENERAL REGISTERS

Card Select Register (CSR) (Write and read); Address: 0 (All signi®cant bits cleared after reset, except for SC1 which is set)

CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
nu	nu	nu	nu	$\overline{RIU}$	SC3	SC2	SC1

This register is used for selecting the card on which the UART will act, and also to reset the ISO UART.

If SC1=1, then card 1 is selected; if SC2=1, then card2 is selected, if SC3 is 1, then card3 is selected. Only one of these bits must be set at the same time. After reset, the card 1 is selected by default. The bit Reset Iso Uart ($\overline{RIU}$) must be set to 1 by software before any action on the UART. When reset, this bit resets all UART's registers to their initial value.

Hardware Status Register (HSR) (Read only); Address: F (All signi®cant bits cleared after reset except for SUPL which is set within the RSTOUT pulse)

HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
nu	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL

This register gives the status of the chip after an hardware problem has been signaled.

PRL1(Presence latch 1) and PRL2(Presence latch 2) are high when a change has occured on PR1 and PR2.

SUPL(Supervisor latch) is high when the supervisor has been active.

PRTL1 (Protection1) and PRTL2 (Protection2) are high when a default has been detected on card reader1 and 2. (PRTL is the OR of protection on VCC and on RST)

PTL is set if an overheating has occured.

INTAUXL is high if the level on INTAUX input has been changed.

When PRTL2 or PRTL1 or PRL2 or PRL1 or PTL is high, then INT is low. The bits having caused the interrupt are cleared when HSR has been readout. The same occurs with bit INTAUXL if not disabled.

At power on, or after a supply voltage dropout, then SUPL is set, and $\overline{\text{INT}}$ is LOW. $\overline{\text{INT}}$ will go back HIGH at the end of the alarm pulse on pin RSTOUT. SUPL will be reset only after a status register readout outside the ALARM pulse. (See Fig.)

In case of emergency deactivation (by PRTL1, PRTL2, SUPL, PRL2, PRL1, PTL), then the bit START is automatically reset by hardware.

Time Out Register 1 (TOR1) (Write only); Address: 9 (All bits cleared after reset)

TO17	**TO16**	**TO15**	**TO14**	**TO13**	**TO12**	**TO11**	**TO10**
TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0

Time Out Register 2 (TOR2) (Write only);Address: A (All bits cleared after reset)

TO27	**TO26**	**TO25**	**TO24**	**TO23**	**TO22**	**TO21**	**TO20**
TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8

Time Out Register 3 (TOR3) (Write only);Address: B (All bits cleared after reset)

TO37	**TO36**	**TO35**	**TO34**	**TO33**	**TO32**	**TO31**	**TO30**
TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16

***Time Out Con®guration Register (TOC) (Read and Write)*;Address: 8 (All bits cleared after reset)**

TOC7	**TOC6**	**TOC5**	**TOC4**	**TOC3**	**TOC2**	**TOC1**	**TOC0**
TOC7	*TOC6*	*TOC5*	*TOC4*	*TOC3*	*TOC2*	*TOC1*	*TOC0*

The three registers TOR1, TOR2, TOR3 form a programmable 24 bits ETU counter, or two independant counters (One 16 bits and one 8 bits).

The value to load in TOR1, 2, 3 is the number of etus to count.

The register TOC is used for setting different configurations of the time out counter according to following table. (All other configurations are undefined):

TOC	OPERATION MODE
00	All counters are stopped
61	Counter 1 is stopped, and counters 3 and 2 form a 16 bits counter starting counting the value TOR3 TOR2 when 61 is written in the TOC. An interrupt is given, and bit TO3 is set within USR when the terminal count is reached. The counter is stopped by writing 00 in the TOC.
65	Counter1 is an 8 bits autoreload counter, and counters 3 and 2 form a 16 bits counter. Counter 1 starts counting the content of TOR1 on the ®rst start bit (reception or transmission) detected on I/O after 65 is written in the TOC. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in USR is set, and the counter automatically restarts the same count until it is stopped. It is not allowed to change the content of TOR1 during a count. Counter 3 and 2 are wired as a single 16 bits counter starting counting the value TOR3 TOR2 when 65 is written in the TOC. When the counter reaches its terminal count, an interrupt is given and bit TO3 is set within USR. Both counters are stopped when 00 is written in the TOC.
68	Counters 3, 2 and 1 are wired as a single 24 bits counter, starting counting the value stored in TOR3, TOR2 and TOR1 when 68 is written in the TOC. The counter is stopped by writing 00 in the TOC. It is not allowed to change the content of TOR3, TOR2 and TOR1 within a count.
7C	Counters 3, 2 and 1 are wired as a single 24 bits counter, starting counting the value stored in TOR3, TOR2 and TOR1 on the ®rst start bit detected on I/O (reception or transmission) after the value has been written. It is possible to change the content of TOR3, TOR2, TOR1 during a count; the current count will not be affected, and the new count value will be taken into account at the next start bit. The counter is stopped by writing 00 in the TOC. In this con®guration, TOR3, TOR2 and TOR1 must not be all null.
E5	Same con®guration than TOC=65, except that counter1 will be stopped at the end of the 12th etu following the ®rst start bit detected after E5 has been written in the TOC.

This time out counter is very usefull for processing the CLK counting during ATR, or the Work Waiting Time, or the Waiting times defined in T=1 protocol. (Note: The 200 and 400 CLK counter used during ATR is done by hardware when Start Session is set, a specific hardware takes care of BGT in T=1 protocol, and a specific register is present for processing the extra guard time)

Possible use of the counters:

- ATR (Cold reset)
  - ± Before activation, TOR1=C0H, TOR2=6EH, TOR3=0. TOC=65.
    Once activated, timer2+3 will count 40920 CLK pulses before giving an interrupt
  - ± On interrupt, TOR2=76H, TOC=65.
    If a character comes from the card before the timeout, then it will start counter1. Counter1 will give one interrupt each 192 etus, so the software will count 100 times for checking that the ATR is finished before 19200 etu.
    The UART will give interrupt by bit Buffer Full at 10.5 etu after the start bit.
  - ± On interrupt,TOR3=25H, TOR2=80H, TOC=65
    Counter1 keeps on counting 100x192 etu, while Counter2+3 counts 9600 etu.

This sequence is repeated until the character before the last one of the ATR.

- *On interrupt, TOR3=25H, TOR2=80H, TOC=E5*
  Timer 1 will be automatically stopped at the end of the last character of the ATR, allowing count of 19200 etu.
- *On interrupt, TOC=00*

- *Work Waiting Time in T=0*
  Before sending the first command to the card, TOR1, TOR2, TOR3 should be loaded with the correct 960xWIxD value, and TOC=7C.
  Timer3+2+1 will count WWT between each start bit
- *Character Waiting Time and Block Waiting Time in T=1*
  Before sending the first block to the card, TOR3,2,1 should be loaded with CWT and TOC=7C.
  Timer 3+2+1 will count CWT between each start bit.
  Before the end of the block, TOR3,2,1 should be loaded with BWT.
  Timer 3+2+1 will count BWT from the last start bit of the sent block.
  After reception of the first character of the block from the card, TOR3,2,1 should be loaded with CWT.
  Timer 3+2+1 will count CWT between each received start bit.
  And so on...
- *Before and after CLOCK STOP (Exemple where etu=372 CLK)*
  After the last received on I/O, TOR3=0, TOR2=6, TOC=61.
  Timer 3+2 will start counting 2232 clk before giving an interrupt.
  On interrupt, the software may stop the clock to the card
  When it is needed to restart the clock, TOR3=0, TOR2=2, TOC=61. and restart the clock.
  Timer 3+2 gives an interrupt at 744 clk, and then the software can send the first command to the card.

ISO UART REGISTERS

Uart Transmit Register (UTR) (Write only); Address: D (All bits cleared after reset)

UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0
UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0

When the controller wants to transmit a character to the selected card, it writes the data in direct convention in this register. The transmission:

* starts at the end of this writing (On the rising edge of $\overline{WR}$) if the previous character has been transmitted and if the extra guard time has expired

* starts at the end of the extra guard time if this one has not expired

* does not start if the transmission of the previous character is not completed

In case of synchronous card (bit SAN within UCR2 set), D0 only is relevant, and is copied on I/O of the selected card.

Uart Receive Register (URR) (Read only); Address: D (All bits cleared after reset)

UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0
UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0

When the controller wants to read a data from the card, it reads it from this register in direct convention.

In case of synchronous card, only D0 is relevant and is a copy of the state of the selected card I/O.

When needed, this register may be tied to a FIFO whose length n is programmable between 1 and 8.

If n>1, then no interrupt is given until the FIFO is full, and the controller may empty the FIFO when it wants.

In protocol T=0:

In case of parity error, the received byte is not stored in the FIFO, and the error counter is incremented. The error counter is programmable between 1 and 8. When the programmed number is reached, then the bit PE is set in the status register USR and INT falls LOW. *The error counter must be reprogrammed to the desired value after its count has been reached*

In protocol T=1:

In case of parity error, the character is loaded in the FIFO, and the bit PE is set whatever the programmed value in parity error counter.

When the FIFO is full, then the bit RBF in the status register USR is set. This bit is reset when at least one character has been read from URR.

When the FIFO is empty, then the bit FE is set as long as no character has been received.

Mixed Status Register (MSR) (Read only); Address: C (Bits TBE/RBF, BGT cleared after reset; bit FE set after reset)

MS7	MS6	MS5	MS4	MS3	MS2	MS1	MS0
nu	FE	BGT	nu	PR2	PR1	INTAUX	TBE/RBF

This register relates the status of the pin INTAUX , the cards presence contacts PR1/PR2, the BGT counter, the FIFO empty indication and the transmit/receive ready indicator TBE/RBF.

The bit INTAUX is set when the level on pin INTAUX is high, reset when the level is low.

The bit BGT is linked with a 22 etu counter, which is started at every start bit on I/O. If the count is finished before the next start bit, then the bit BGT is set. This helps checking that the card has not answered before 22 etu after the last transmitted character, or not transmitting a character before 22 etu after the last received character.

PR1 (Presence1) is high when card1 is present, PR2 (Presence2) is high when card2 is present.

FE (FIFO Empty) is set when the reception FIFO is empty. It is reset when at least one character has been loaded in the FIFO.

Bit TBE/RBF (Transmit Buffer Empty/Receive Buffer Full) is set when:

* Changing from reception mode to transmission mode

* A character has been transmitted by the UART

* The reception FIFO is full

It is reset after power-on, or when the bit $\overline{\text{RIU}}$ is reset, or when a character has been written in UTR, or when at least one character has been read in the FIFO, or when changing from transmission mode to reception mode.

No bit within MSR act upon $\overline{\text{INT}}$.

FIFO Control Register (FCR) (Write only); Address: C (All relevant bits cleared after reset)

FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
nu	PEC2	PEC1	PEC0	nu	FL2	FL1	FL0

FL2, FL1, FL0 determine the depth of the FIFO: 000 means length 1, 111 means length 8.

PEC2, PEC1, PEC0 determine the number of parity errors before setting the bit PE within USR and pulling $\overline{INT}$ LOW; 000 means that if only one parity error has occured, the bit PE is set; 111 means that PE will be set after 8 parity errors

PEC2, PEC1, PEC0 need to be reprogrammed to the desired value after PE has been set.

In protocol T=0, if a correct character is received before the programmed error number is reached, then the error counter is reset. If the programmed number of allowed parity errors is reached, then the bit PE within USR is set as long as USR has not been read.

In protocol T=1, the error counter has no action. (PE is set at the first wrong received character)

Uart Status Register (USR) (Read only); Address: E (All bits cleared after reset)

US7	US6	US5	US4	US3	US2	US1	US0
TO3	*nu*	TO1	EA	PE	OVR	FER	TBE/RBF

This register is used by the controller to monitor the activity of the ISO UART and of the Time Out Counter

TBE (Transmission buffer empty) is high when the UART is in transmission mode, and when the controller may write the next character to transmit in UTR. It is reset when the controller has written a data in the Transmit Register, or when the bit T/R within UCR1 has been reset either automatically or by software.

RBF (Reception buffer full) is high when the FIFO is full. The controller may read some of the characters in URR, which clears the bit RBF. TBE and RBF share the same bit within USR. (When in transmission mode, the relevant one is TBE; when in reception, it is RBF)

FER (Framing Error) is high when I/O was not in high impedance state at 10.25 etu after a start bit. It is reset when USR has been readout.

OVR(Overrun) is high if the UART has received a new character whilst the FIFO was full. In this case, at least one character has been lost...

In T=0 protocol, PE (Parity error) is high if the UART has detected a number of received characters with parity error equal to the number written in *PEC2, PEC1, PEC0* or if a transmitted character has been NAKed by the card.

In T=0 protocol, a character received with a parity error is not stored in the FIFO. (The card is supposed to repeat this character). In T=1 protocol, a character with parity error is stored in the FIFO and the parity error counter is not operating.

EA (Early answer) is high if the first start bit on I/O during ATR has been detected between 200 and 384 CLK pulses (All activities on I/O during the 200 first CLK pulses with RST LOW or HIGH are not taken into account). *These 2 features are reinitialized at each toggling of RST.*

The bit TO1 is set when counter1 has reached its terminal count.

The bit TO3 is set when counter 3 has reached its terminal count.

If any of the status bits FER, OVR, PE, EA, TO1 or TO3 is set, then $\overline{INT}$ is LOW. The bit having caused the interrupt is reset at the end of a read operation of USR. If TBE/RBF is set, and if the mask bit DISTBE/RBF within USR2 is not set, then $\overline{INT}$ is also LOW. TBE/RBF is reset when a data has been written in UTR, or when a data has been read from URR, or when changing from transmission mode to reception mode.

CARDS REGISTERS

When cards 1 or 2 or 3 are selected, then the following registers may be used for programming some specific parameters:

Programmable Divider Register (PDR1, 2, 3) (Read and write); Address: 2 (All bits cleared after reset)

PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

This register is used for counting the cards clock cycles forming the ETU . It is an autoreload 8 bits counter decounting from the programmed value down to 0.

Uart Con®guration Register 2 (UCR21, 22, 23) (Read and write); Address: 3 (All relevant bits cleared after reset)

UC27	UC26	UC25	UC24	UC23	UC22	UC21	UC20
nu	DISTBE/RBF	DISAUX	PDWN	SAN	$\overline{\text{AUTOCONV}}$	CKU	PSC

If PSC is 1, then the prescaler value is 32. If PSC is 0, then the prescaler value is 31. One etu will last a number of cards clock cycles equal to prescaler x pdr. All baudrates specified in ISO 7816 norm are achievable with this configuration.

Table 1 Baud rates with a 3.58MHz cards clock frequency *(31; 12 means prescaler set to 31 and PDR set to 12*)

		F											
		0	1	2	3	4	5	6	9	10	11	12	13
D	1	31;12 9600	31;12 9600	31;18 6400	31;24 4800	31;36 3200	31;48 2400	31;60 1920	32;16	32;24	32;32	32;48	32;64
	2	31;6 19200	31;6 19200	31;9 12800	31;12 9600	31;18 6400	31;24 4800	31;30 3840	32;8	32;12	32;16	32;24	32;32
	3	31;3 38400	31;3 38400		31;6 19200	31;9 12800	31;12 9600	31;15 7680	32;4	32;6	32;8	32;12	32;16
	4				31;3 38400		31;6 19200		32;2	32;3	32;4	32;6	32;8
	5						31;3 38400		32;1		32;2	32;3	32;4
	6										32;1		32;2
	8	31;1 115200	31;1 115200		31;2 57600	31;3 38400	31;4 28800	31;5 23040		32;2		32;4	
	9							31;3 38400					

If the bit $\overline{\text{AUTOCONV}}$ is set, then the convention is set by software with the bit CONV in the UART Configuration Register. If it is reset, then the configuration is automatically detected on the first received character whilst the bit SS (Start Session) is set.

For other baud rates, there is the possibility to set bit CKU (Clock uart) to 1. In this case, the etu will last the half of the formula above.

SAN (Synchronous/$\overline{\text{Asynchronous}}$) is set by software if a synchronous card is expected. Then, the UART is bypassed, and only the bit 0 in URR and UTR is connected to I/O. In this case, CLK is controlled by the bit SC in CCR.

PDWN (Power Down Mode): To be fixedi:

If bit DISAUX within UCR2(Disable AUX interrupts) is set, then a change on INTAUX will not generate an interrupt. (But the bit INTAUXL within HSR will be set. *So it is necessary to read HSR before a DISAUX reset to avoid an interrupt by INTAUXL*).

If bit DISTBE/RBF (Disable TBE/RBF interrupts) is set, then reception or transmission of a character will not generate an interrupt. This feature is usefull for increasing communication speed with the card ; in this case, the copy of TBE/RBF bit within MSR must be polled, and not the original, in order not to loose prioritary interrupts which can occur in USR.

Guard Time Register (GTR1, 2, 3) (Read and write); Address: 5 (All bits cleared after reset)

GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0
GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0

This register is used for storing the number of guard etu given by the card during ATR. In transmission mode, the UART will wait this number of ETU before transmitting the character stored in UTR. In T=1 protocol, GTR=FF means operation at 11 ETU. In protocol T=0, GTR=FF means operation at 12 etu.

Uart Con®guration Register 1(UCR11, 12, 13) (Read and write); Address: 6 (All relevant bits cleared after reset)

UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0
nu	FIP	FC	PROT	T/R	LCT	SS	CONV

This register is used for setting the parameters of the ISO UART:

CONV (Convention) is set if the convention is direct. CONV is either automatically written by hardware according to the convention detected during ATR, or by software if the bit $\overline{\text{AUTOCONV}}$ is set.

SS (Start Session) is set before ATR for automatic convention detection and early answer detection. (must be reset by software after reception of a correct initial character)

LCT (Last character to transmit) is set by software before writing in UTR the last character to transmit. It allows automatic change to reception mode. Reset by hardware at the end of a successfull transmission.

T/R (Transmit/receive) is set by software for transmission mode. A change from 0 to 1 will set the bit TBE in USR. T/R is automatically reset by hardware if LCT has been used before transmitting the last character.

PROT (Protocol) is set if protocol type is asynchronous T=1. If PROT =0, the protocol is T=0.

FC (Flow control) is set if flow control is used (Not described in this specification)

If FIP (Force inverse parity) is set to high, then the UART will NACK a correct received character, and will transmit characters with wrong parity bit.

Clock Con®guration Register (CCR1, 2, 3) (Read and write); Address: 1 (All bits cleared after reset)

CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
nu	nu	SHL	CST	SC	AC2	AC1	AC0

For cards 1 and 2, this register defines the CLK to the selected card. For cards 1, 2 and 3 it defines the clock to the ISO UART. Note that if bit CKU in the Prescaler register of the selected card is set, then the ISO UART is clocked at twice the frequency to the card, which allows to reach baudrates not foreseen in ISO7816 norm.

In case of asynchronous card, the bit CST (Clock Stop) defines whether the clock to the card is stopped or not.

If CST is set, then CLK is stopped at LOW if SHL is 0, at HIGH if SHL is 1.

If CST is reset, then CLK is determined by bits AC0, AC1, AC2 according to the following table. All frequency changes are synchronous, ensuring that no spike or unwanted pulse width occurs during changes.

For switching from XTAL/n to Fint/2 and reverse, only the bit AC2 must be changed.(AC1 and AC0 must remain the same). For switching from XTAL/n or Fint/2 to CLK STOP and reverse, only bits CST and SHL must be changed.

When switching from XTAL/n to Fint/2 and reverse, a maximum delay of 200us can occur between the command and the effective frequency change on CLK. (The fastest switch is from XTAL/2 to Fint/2 and reverse, the best for duty cycle is from XTAL/8 to Fint/2 and reverse)

In case of synchronous card, then the CLK contact is the copy of the value written in SC. (Synchronous Clock). *In reception mode, the data from the card is available in UR0 after a read operation of URR*; in transmission mode, the data is written on the I/O line of the card when UTR has been written , and remains unchanged when an other card is selected.

Table 2 CLK value for an asynchronous card

AC2	AC1	AC0	CLK
0	*0*	*0*	*XTAL*
0	0	1	XTAL/2
0	1	0	XTAL/4
0	1	1	XTAL/8
1	0	0	Fint/2
1	0	1	Fint/2
1	1	0	Fint/2
1	1	1	Fint/2

In case of CLK=XTAL, the duty cycle must be ensured by the incoming clock signal on XTAL1.

The following control registers are only available for cards 1 or 2:

Power Control Register (PCR1, 2) (Read and write); Address: 7 (All relevant bits cleared after reset)

PCR7	PCR6	PCR5	PCR4	PCR3	PCR2	PCR1	PCR0
nu	nu	*C8*	*C4*	1V8	RSTIN	3V/5V	START

This register is used for starting or stopping card sessions, and also for reading or writing on auxiliary cards contacts C4 and C8.

If the controller sets START to 1, then the selected card is activated *(See further description of activation sequence)*. If the controller resets START to 0, then the card is deactivated*(See further description of deactivation sequence)*. START is automatically reset in case of emergency deactivation.

If 3V/5V is set to 1, then VCC is 3V. If 3V/5V is 0, then VCC is 5V.

When the card is activated, RST is the copy of the value written in RSTIN.

If 1V8 is set, then VCC=1.8V. Note that no specification is guaranted at this voltage.

When writing in PCR, C4 will output the value written in PCR4, and C8 the value written in PCR5. When reading from PCR, PCR4 will store the value on C4, and PCR5 the value on C8.

REGISTERS SUMMARY

NAME	ADDR	R/W	7	6	5	4	3	2	1	0	VALUE AT RESET
CSR	00	R/W	nu	nu	nu	nu	$\overline{\text{RIU}}$	SC3	SC2	SC1	*XXXX0000*
HSR	0F	R	nu	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL	X0010000
MSR	0C	R	nu	FE	BGT	nu	PR2	PR1	INTAUX	TBE/RBF	X10XXXX0
TOR1	09	W	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0	00000000
TOR2	0A	W	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8	00000000
TOR3	0B	W	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16	00000000
TOC	*08*	*R/W*	*TOC7*	*TOC6*	*TOC5*	*TOC4*	*TOC3*	*TOC2*	*TOC1*	*TOC0*	*00000000*
UTR	0D	W	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0	00000000
URR	0D	R	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	00000000
FCR	0C	W	nu	PEC2	PEC1	PEC0	nu	FL2	FL1	FL0	X000X000
USR	*0E*	*R*	*TO3*	*nu*	*TO1*	*EA*	*PE*	*OVR*	*FER*	*TBE/RBF*	*0X000000*
PDR	02	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00000000
UCR2	03	R/W	nu	DISTBE/RBF	DISAUX	PDWN	SAN	$\overline{\text{AUTOC}}$	CKU	PSC	X0000000
GTR	05	R/W	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0	00000000
UCR1	06	R/W	nu	FIP	FC	PROT	T/R	LCT	SS	CONV	X0000000
CCR	01	R/W	MC1	MC0	SHL	CST	SC	AC2	AC1	AC0	00000000
PCR	07	R/W	nu	nu	C8	C4	1V8	RSTIN	3V/$\overline{\text{5V}}$	START	*XX110000*

Supply

The circuit operates within a supply voltage range of *2.7* to 6 V. The supply pins are V_{DD}, V_{DDA}, GND, GNDA. Pins V_{DDA} and GNDA supply the analog drivers to the cards and have to be externally decoupled because of the large current spikes that the cards and the step-up converter can create. VDD and GND supply the rest of the chip. An integrated spike killer ensures the contacts to the cards remain inactive during power-up or power-down. An internal voltage reference is generated which is used within the step-up converter, the voltage supervisor, and the V_{CC} generators.

The voltage supervisor generates an alarm pulse, whose length is defined by an external capacitor tied to the DELAY pin, when V_{DD} is too low to ensure proper operation (1 ms per 1 nF typical). This pulse may be used as a RESET pulse by the system controller. (*Pin RSTOUT, active HIGH*) It is also used in order to either block any spurious on card contacts during controllers reset, or to force an automatic deactivation of the contacts in the event of supply drop-out (see ªActivation sequenceº and ªDeactivation sequenceº)

After power-on, or after a voltage drop, the bit SUPL is set within the Hardware Status Register (HSR) and remains set until HSR is readout outside the alarm pulse. As long as RSTOUT is active, $\overline{INT}$ is LOW.

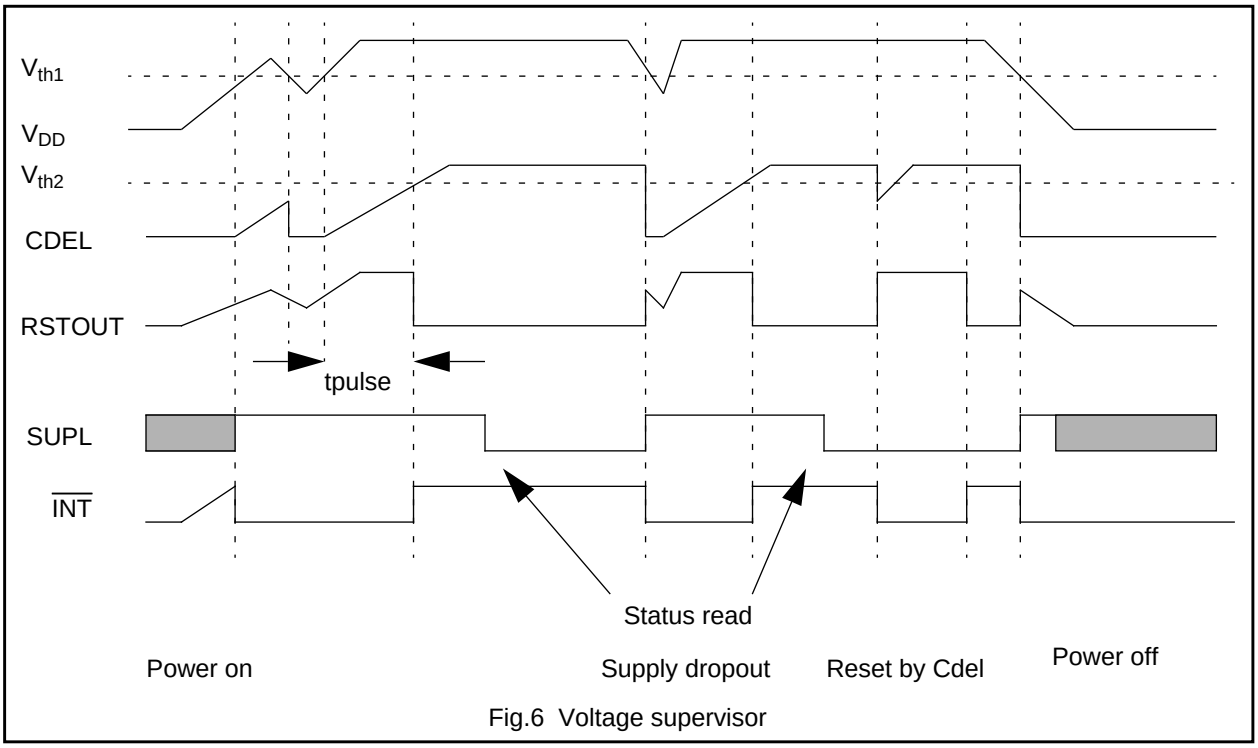


Fig.6 Voltage supervisor

If needed, a complete reset of the chip may be performed by uncharging the capacitor CDEL.

Step-up converter

Except for V_{CC} generator, and the other cards contacts buffers, the whole circuit is powered by V_{DD}, and V_{DDA}. If the supply voltage is 2.5 V , then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the controller, the sequencer first starts the step-up converter, which is a switched capacitors type, clocked by an internal oscillator at a frequency approximately 2.5 MHz.

Lets call VCC the maximum of VCC1 and VCC2. There are four possible situations:

- VDD=3V and VCC=3V: In this case the stepup is acting as a doubler with a regulation about *4.0V*.
- VDD=3V and VCC=5V: In this case, the stepup is acting as a tripler with a regulation about *5.5V*.

- VDD=5V and VCC=3V: In this case, the stepup is acting as a follower: VDD is applied on VUP.
- VDD=5V and VCC=5V. In this case, the stepup is acting as a doubler with a regulation about *5.5V*.

The recognition of the supply voltage is done by the TDA8007B at about *3.5V*.

The output voltage, V_{UP}, is fed to the V_{CC} generators. V_{CC} and GND are used as a reference for all other cards contacts. .

ISO 7816 security

The correct sequence during activation and deactivation of the cards is ensured through two specific sequencers, clocked by a division ratio of the internal oscillator.

Activation (START bit HIGH in PCR1 or PCR2) is only possible if the card is present*(PRESactive HIGH with an internal current source to GND*), and if the supply voltage is correct (Supervisor not active).

The presence of the cards is signalled to the controller by the Hardware Status Register HSR.

Bits PR1 or PR2 (in USR) are set if card1 or card2 is present. PRL1 or PRL2 are set if PR1 or PR2 has toggled.

During a session, the sequencer performs an automatic emergency deactivation on one card in the event of card take-off, or shortcircuit. Both cards are automatically deactivated in case of supply voltage drop, or overheating. The HSR register is updated and the $\overline{\text{INT}}$ line falls down, so the system controller is aware of what happened.

ISO 7816 security

The correct sequence during activation and deactivation of the cards is ensured through two specific sequencers, clocked by a division ratio of the internal oscillator.

Activation (START Bit HIGH in PCR1 or PCR2) is only possible if the card is present (PRES HIGH or LOW according to mask option), and if the supply voltage is correct (Supervisor not active).

The presence of the cards is signalled to the controller by the Hardware Status Register HSR.

Bits PR1 or PR2 (in USR) are set if card1 or card2 is present. PRL1 or PRL2 are set if PR1 or PR2 has toggled.

During a session, the sequencer performs an automatic emergency deactivation on one card in the event of card take-off, or short-circuit. Both cards are automatically deactivated in case of supply voltage drop, or overheating. The HSR (Hardware Status Register) is updated and the $\overline{\text{INT0}}$ line falls down, so the embedded controller may be aware of what happened.

Activation sequence

When the cards are inactive, VCC, CLK, RST, C4, C8 and I/O are LOW, with low impedance with respect to GNDC. The step-up converter is stopped.

When everything is satisfactory (voltage supply, card present, no hardware problems), the embedded controller may initiate an activation sequence of a present card.

After selecting the card and leaving the UART reset mode, and then configurating the necessary parameters for the counters and the UART, it may set the Bit START within PCR (t0).

- The step-up converter is started (t1). (If already one card was active, then the step-up converter was already on, and nothing more occurs at this step.)
- VCC starts rising from 0 to 5 V or 3V with a controlled rise time of 0.17V/µs typically (t2).
- I/O rises to VCC (t3); C4 and C8 also if Bits C4 and C8 within PCR have been set to 1 (Integrated 10k pull-ups to VCC).
- CLK is sent to the card and RST is enabled (t4).

After a number of CLK pulses that can be counted with the Time Out Counter, the Bit RSTIN within PCR may be set by software: then, RST rises to VCC.

The sequencer is clocked by $f_{INT}/64$ which leads to a time interval T of 25µs typical.

Thus t1 = 0 to T/64, t2 = t1 + 3T/2, t3 = t1 + 7T/2, and t4 = t1 + 4T.

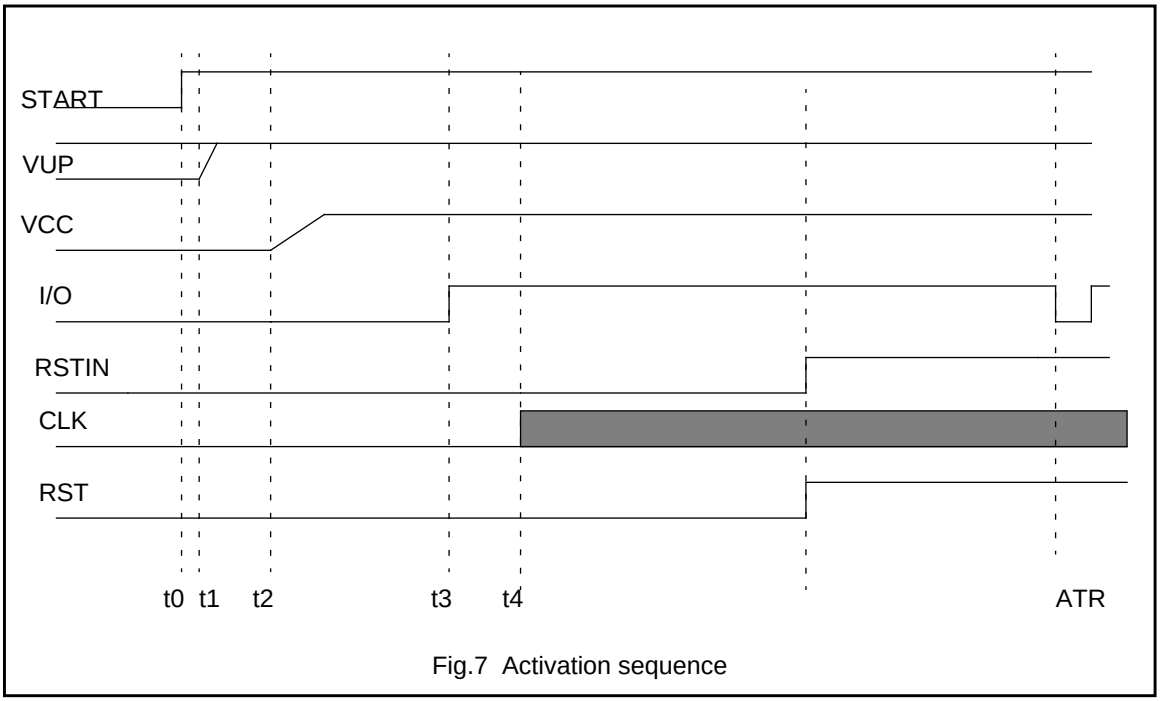


Fig.7 Activation sequence

Deactivation sequence

When the session is completed, the microcontroller resets th eBit START inside PCR (t10). The circuit then executes an automatic deactivation sequence

- Card reset (RST falls LOW) (t11)
- clock on CLK is stopped (t12)
- I/O, C4 and C8 fall to 0V (t13)
- VCC falls to 0V with typical 0.17 V/µs slew rate (t14)
- The step-up converter is stopped and CLK, RST, VCC and I/O become low impedance with th erespect to GNDC (t15) (If both cards are inactive.)

t11 = t10 + T/64, t12 = t11 + T/2, t13 = t11 + T, t14 = t11 + 3T/2, t15 = t11 + 7T/2.

t_{de} is the time that VCC needs for going down to less than 0.4V.

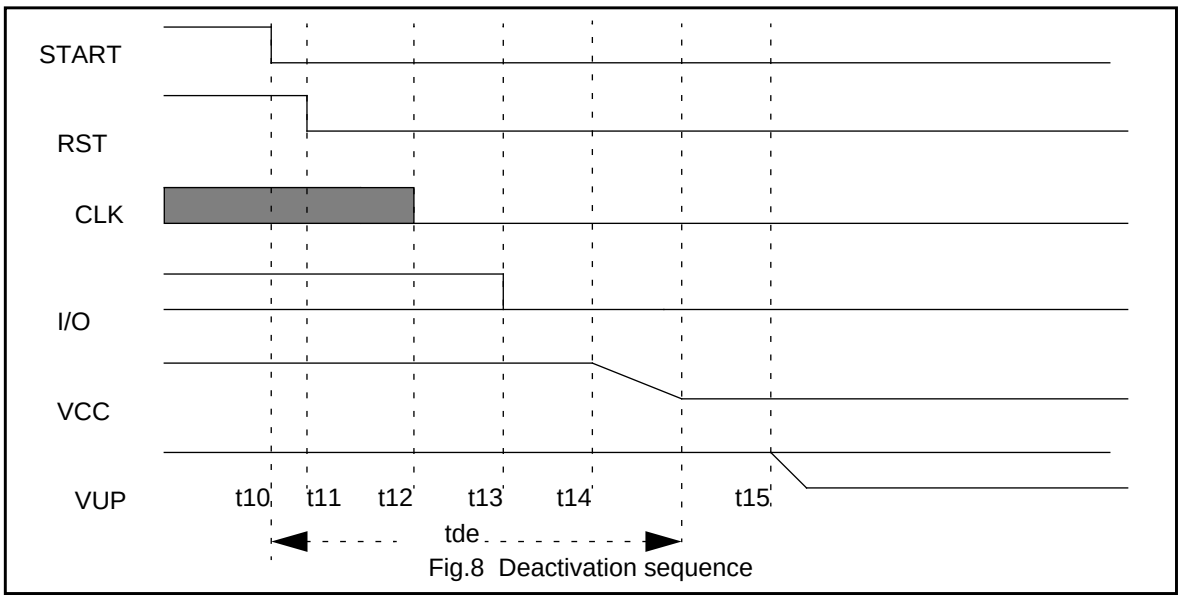


Fig.8 Deactivation sequence

Microcontroller

The Microcontroller core inside the TDA8028/TDA8008 basically behaves like a standard `C51 Microcontroller.

It has the same instruction set as the 80C51.

A general description as well as every added feature will be described in the following sections.

The added features to the 80C51 Controller are similar to the 8XC51RB+ Controller. Please refer for any further information to the published specification of the 8XC51RB+ in ªData Handbook IC20; 80C51-Based 8-Bit Microcontrollersº.

It has four 8-Bits I/O ports, three 16-Bits timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra memory capability up to 64kBytes, it can be expanded using standard TTL-compatible memories and logic.

- 80C51 Central Processing Unit
- Full static operation
- Security Bits: ROM - 2Bits / OTP - 3Bits
- Encryption array of 64Bytes
- RAM expandible up to 64kBytes
- 4 level priority structure
- 6 interrupt sources
- Four 8-Bits I/O ports
- Full-duplex enhanced UART with framing error detection and automatic address recognition
- Power control modes (Clock can be stopped and resumed / IDLE mode / Power Down mode)
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)

The table underneath gives a list of main features to get a better understanding of the differences between a standard 80C51, an 8XC51RB+ and the embedded Controller in the TDA8028/TDA8008:

Principal Blocks in 80C51, 8XC51RB+ and TDA8028/TDA8008

Feature	80C51	8XC51RB+	TDA8028/TDA8008
ROM / EPROM	4kBytes	16kBytes	16kBytes
RAM	128Bytes	256Bytes	256Bytes
ERAM (MOVX)	NO	256Bytes	512Bytes
PCA	NO	YES	NO
WDT	NO	YES	NO
T0	YES	YES	YES
T1	YES	YES	YES
T2	NO	YES	YES
		lowest interrupt priority-vector @ 002BH	
4 level priority interrupt	NO	YES	YES
enhanced UART	NO	YES	YES
programmable clock-out	NO	YES	YES

Embedded `C51 Controller Special Function Registers

Symbol	Description	@	Bit Address, Symbol or Alternative Port Function								RESET Value
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR#	Auxiliary	8EH	-	-					EXTRAM	AO	xxxxxx00B
AUXR1#	Auxiliary	A2H	-	-		LPEP[3]	GF	0	-	DPS	xxx000x0B
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
IE*	Interrupt Enable	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			AF	AE	AD	AC	AB	AA	A9	A8	
IP*	Interrupt Priority	B8H	-	-	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IPH#	Interrupt Priority High	B7H	-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx000000B
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			87	86	85	84	83	82	81	80	
P1*	Port 1	90H	-	-	-	-	-	-	T2EX	T2	FFH
			97	96	95	94	93	92	91	90	
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
PCON#[1]	Power Control	87H	SMOD1	SMOD0	-	POF[2]	GF1	GF0	PD	IDL	00xx0000B
SPW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	-	P	000000x0B
			D7	D6	D5	D4	D3	D2	D1	D0	
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SADDR#	Slave Address	A9H									00H
SADEN#	Slave Address Mask	B9H									00H
SBUF	Serial Data Buffer	99H									xxH
SCON*	Serial Control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00H
			9F	9E	9D	9C	9B	9A	99	98	
SP	Stack Pointer	81H									07H
TCON*	Timer Control	88H	TF1	TR1	TF0	TE0	IE1	IT1	IE0	IT0	00H
			8F	8E	8D	8C	8B	8A	89	88	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
			CF	CE	CD	CC	CB	CA	C9	C8	

Symbol	Description	@	Bit Address, Symbol or Alternative Port Function								RESET Value
T2MOD#	Timer 2 Mode Control	C9H	-	-	-	-	-	-	T2OE	DCEN	xxxxxx00B
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low1	8BH									00H
TL2#	Timer Low2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H

Notes

1. RESET Value depends on Reset source
2. Bit will not be affected by RESET
3. LPEP - Low Power OTP: TDA8008 only
4. * SFRs are Bit addressable
5. # SFRs are modified from or added to the 80C51 SFRs

PORTS CHARACTERISTICS

Port 0 (P0.7..P0.0): Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code Bytes during program verification and received code Bytes during EPROM programming. External pull-ups are required during program verification.

Port 1 (P1.7..P1.0): Port 1 is an 8-Bit bidirectional I/O -port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address Byte during program memory verification. Alternate functions for port 1 include:

T2 (P1.0): Timer/Counter 2 external count input / Clockout (see Programmable Clock-Out)

T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control

Port 2 (P2.7..P2.0): Port 2 is an 8-Bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address Byte during fetches from external program memory and during accesses to external data memory that use 16-Bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-Bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high order address Bits during EPROM programming and verification.

Port 3 (P3.7..P3.3, P3.1, P3.0): Port 3 is an 7-Bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. Port 3 also serves the special features of the 80C51 family, as listed:

RxD (P3.0): Serial input port

TxD (P3.1): Serial output port

$\overline{INT0}$ (P3.2): External interrupt 0

$\overline{INT1}$ (P3.3): External interrupt 1

T0 (P3.4): Timer 0 external input

T1 (P3.5): Timer 1external input

$\overline{WR}$ (P3.6): External data memory write strobe

$\overline{RD}$ (P3.7): External data memory read strobe

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RESET pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RESET pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{DDD}, V_{DDA}, V_{DDP} and RESET must come up at the same time for a proper start-up. Ports 1, 2, and 3 will asynchronously be driven to their reset condition when a voltage above V_{IH1} (min.) is applied to RESET.

LOW POWER MODES

Stop Clock Mode: The static design enables the clock speed to be reduced down to 0MHz (stopped). When the oscillator is stopped, the RAM and Special Function Registers retain their values. This mode allows step-by-step utilization and permits reduced system power consumption by lowering the clock frequency down to any value. For lowest power consumption the Power Down mode is suggested.

IDLE Mode: In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode: To save even more power, a Power Down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to the minimum supply voltage and care must be taken to return V_{DDD}, V_{DDA} and V_{DDP} to the minimum specified operating voltage before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{DDD}, V_{DDA} and V_{DDP} are restored to their normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Within the $\overline{INT0}$ interrupt service routine, the controller has to read out the Hardware Status Register (HSR @ 0FH) and/or the UART Status register (USR @ 0EH) by means of MOVX-instructions in order to know the exact interrupt reason and to reset the interrupt source. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power-Down.

External Pin Status during IDLE and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT2	PORT3
IDLE	Internal	1	1	Data	Data	Data	Data
IDLE	External	1	1	Float	Data	Address	Data
Power-Down	Internal	0	0	Data	Data	Data	Data
Power-Down	External	0	0	Float	Data	Data	Data

LPEP

The EPROM array contains some analog circuits that are not required when V_{DDD} is less than 4V, but are required for a V_{DDD} greater than 4V. The LPEP Bit (AUXR.4), when set, will power-down these analog circuits resulting in a reduced supply current. This Bit should be set ONLY for applications that operate at a V_{DDD} less than 4V.

POWER OFF FLAG

The Power Off Flag (POF) is set by on-chip circuitry when the V_{DDD} level rises from 0 to 5V. The POF Bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after power-down. The V_{DDD} level must remain above 3V for the POF to remain unaffected by the V_{DDD} level.

Design Consideration: When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhiBits access to internal RAM in this event, but access to the port pins is not inhiBited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

PROGRAMMABLE CLOCK-OUT

A 50% duty cycle clock can be programmed to come out on P1.0. This pin, besides being a regular I/O pin, has two alternate functions. It can be programmed:

1. to input the external clock for Timer/Counter 2, or

2. to output a 50% duty cycle clock ranging from 61Hz to 4MHz at a 16MHz operating frequency.

To configure the Timer/Counter 2 as a clock generator, Bit C/$\overline{T2}$ (in T2CON) must be cleared and Bit T20E in T2MOD must be set. Bit TR2 (T2CON.2) also must be set to start the timer.

The Clock-Out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers (RCAP2H, RCAP2L) as shown in this equation:

(1)

$$\frac{OscillatorFrequency}{4\times(65536\pm(RCAP2H,RCAP2L))}$$

Where (RCAP2H,RCAP2L) = the content of RCAP2H and RCAP2L taken as a 16-Bit unsigned integer.

In the Clock-Out mode Timer 2 roll-over will not generate an interrupt. This is similar to when it is used as a baud-rate generator. It is possible to use Timer 2 as a baud-rate generator and a clock generator simultaneously. Note, however, that the baud-rate and the Clock-Out frequency will be the same.

TIMER2 OPERATION

Timer2 is a 16-Bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C$\overline{T2}$ in the special function register T2CON. Timer 2 has three operating modes: Capture, Auto-reload (up or down counting), and Baud Rate Generator, which are selected by Bits in the T2CON.

Timer/Counter 2 (T2CON) Control Register

Register Name	Register Address	Bit	Symbol	Function
T2CON	C8H	T2CON.7	TF2	Timer 2 over¯ow ¯ag set by a Timer 2 over¯ow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
		T2CON.6	EXF2	Timer 2 external ¯ag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software. EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
		T2CON.5	RCLK	Receive clock ¯ag. When set, causes the serial port to use Timer 2 over¯ow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 over¯ow to be used for the receive clock.
		T2CON.4	TCLK	Transmit clock ¯ag. When set, causes the serial port to use Timer 2 over¯ow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 over¯ows to be used for the transmit clock.
		T2CON.3	EXEN2	Timer 2 external enable ¯ag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2=0 causes Timer 2 to ignore events at T2EX.
		T2CON.2	TR2	Start/stop control for Timer 2. A logic 1 starts the timer.
		T2CON.1	C/$\overline{T2}$	Timer or counter select. (Timer 2) 0 = Internal timer (f_{XTAL1}/12) 1 = External event counter (falling edge triggered).
		T2CON.0	CP/$\overline{RL2}$	Capture/Reload ¯ag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 over¯ows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this Bit is ignored and the timer is forced to auto-reload on Timer 2 over¯ow.

Timer 2 Operating Modes

MODE	RCLK + TCLK	CP/$\overline{RL2}$	TR2
16-Bit Auto-Reload	0	0	1
16-Bit Capture	0	1	1
Baud-Rate Generator	1	X	1
(off)	X	X	0

Capture Mode: In the capture mode there are two options which are selected by Bit EXEN2 in T2CON. If EXEN2=0, then timer2 is a 16-Bit timer or counter (as selected by C/$\overline{T2}$ in T2CON) which, upon overflowing sets Bit TF2, the timer2 overflow Bit. This Bit can be used to generate an interrupt (by enabling the Timer2 interrupt Bit in the IE register). If EXEN2= 1, Timer2 operates as described above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes Bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer2 overflow interrupt. The Timer2 interrupt service routine can

interrogate TF2 and EXF2 to determine which event caused the interrupt). There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.

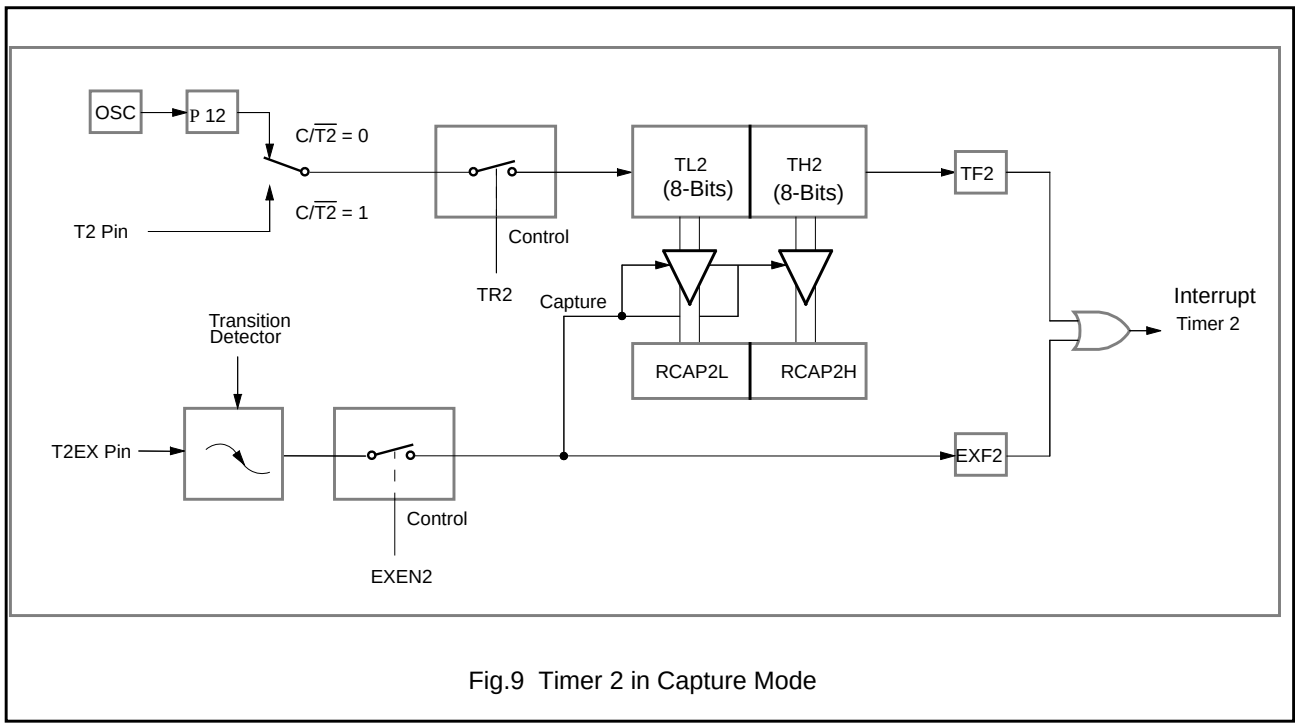


Fig.9 Timer 2 in Capture Mode

Auto-Reload Mode (Up or Down Counter): In the 16-Bit auto-reload mode, Timer2 can be configured (as either a timer or counter [C/$\overline{T2}$ in T2CON]) then programmed to count up or down. The counting direction is determined by Bit DCEN (Down Counter Enable) which is located in the T2MOD register. When reset is applied the DCEN=0 which means Timer2 will default to counting up. If DCEN Bit is set, Timer 2 can count up or down depending on the value of the T2EX pin.

Timer2 which will count up automatically since DCEN=0. In this mode there are two options selected by Bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) Bit upon overflow. This causes the Timer2 registers to be reloaded with the 16-Bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If EXEN2=1, then a 16-Bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 Bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

DCEN=1 enables Timer2 to count up or down. This mode allows pin T2EX to control the direction of count. When a logic 1 is applied at pin T2EX Timer2 will count up. Timer2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-Bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at pin T2EX this causes Timer2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer2 underflows or overflows. This EXF2 Bit can be used as a 17th Bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

Timer 2 (T2MOD) Control Register

Register Name	Register Address	Bit	Symbol	Function
T2MOD	C9H	T2MOD.7	-	Not implemented, reserved for future use.[1]
		T2MOD.6	-	Not implemented, reserved for future use.[1]
		T2MOD.5	-	Not implemented, reserved for future use.[1]
		T2MOD.4	-	Not implemented, reserved for future use.[1]
		T2MOD.3	-	Not implemented, reserved for future use.[1]
		T2MOD.2	-	Not implemented, reserved for future use.[1]
		T2MOD.1	T2OE	Timer 2 Output Enable Bit.
		T2MOD.0	DCEN	Down Count Enable Bit. When set, this allows Timer 2 to be con®gured as an up/down counter

Note

1. User software should not write 1s to reserved Bits. These Bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new Bit will be 0, and its active value will be 1. The value read from a reserved Bit is indeterminate.

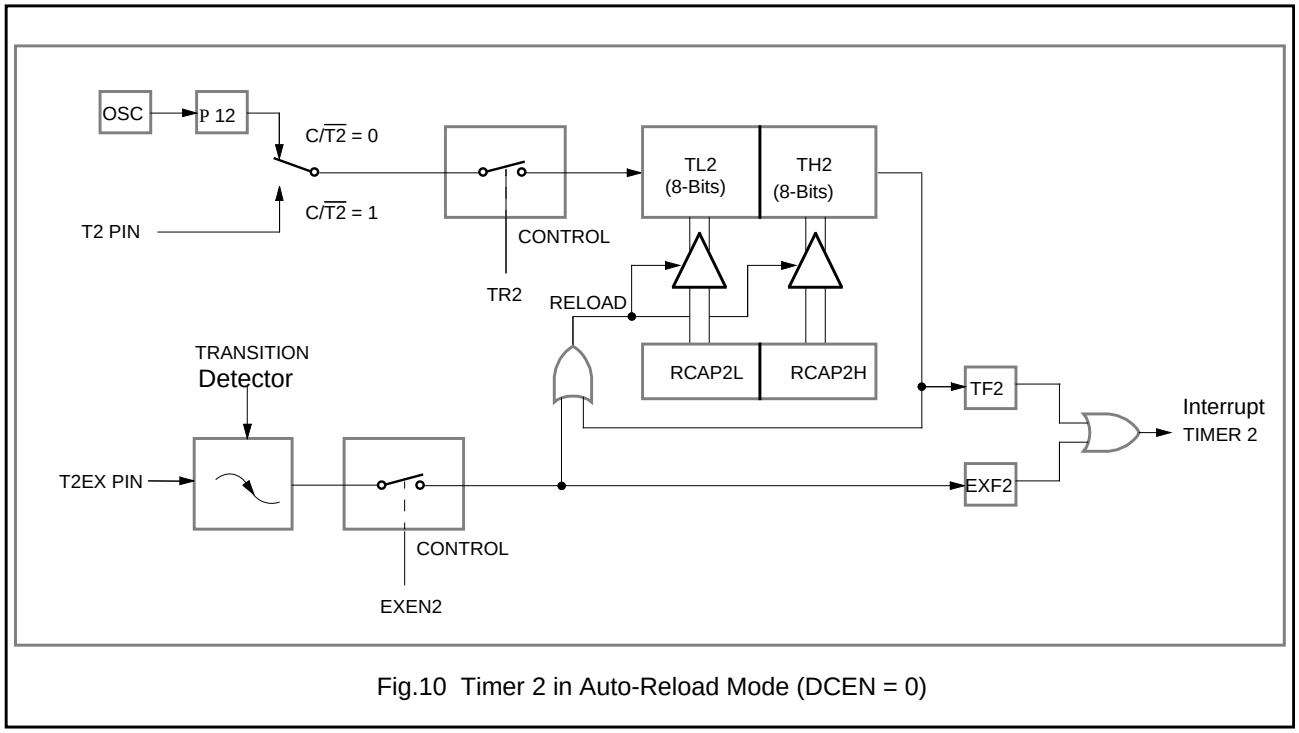


Fig.10 Timer 2 in Auto-Reload Mode (DCEN = 0)

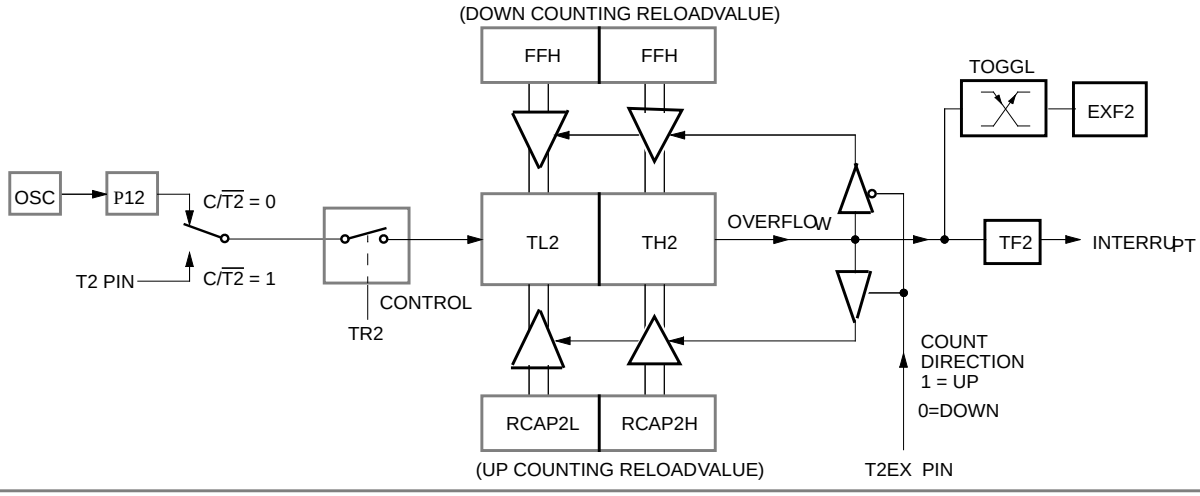


Fig.11 Timer 2 in Auto-Reload Mode (DCEN = 1)

Baud Rate Generator Mode: Bits TCLK and/or RCLK in T2CON allow the serial port transmit and receive baud rates to be derived from either Timer1 or Timer2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two Bits, the serial port can have different receive and transmit baud rates - one generated by Timer 1, the other by Timer2.

The baud rate generation mode is like the auto-reload mode, in that a rollover in TH2 causes the Timer2 registers to be reloaded with the 16-Bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

(2)

The timer can be configured for either ªtimerº or ªcounterº operation. In many applications, it is configured for ªtimerº operation (C/$\overline{T2}$=0). Timer operation is different for Timer2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the modes 1 and 3 baud rate formula is as follows:

(3)

$$\frac{}{\times}$$

Where: (RCAP2H, RCAP2L) = The content of RCAP2H and RCAP2L taken as a 16-Bit unsigned integer.

The Timer2 as a baud rate generator mode is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer2 interrupt does not have to be disabled when Timer2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2,TL2). Therefore when Timer2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer2 or RCAP2 registers.

Timer 2 Generated commonly used Baud Rates

BAUD RATE	XTAL OSCILLATOR FREQUENCY	TIMER	
		RCAP2H	RCAP2L
375k	12MHz	FFH	FFH
9.6k	12MHz	FFH	D9H
2.8k	12MHz	FFH	B2H
2.4k	12MHz	FFH	64H
1.2k	12MHz	FEH	C8H
300	12MHz	FBH	1EH
110	12MHz	F2H	AFH
300	6MHz	FDH	8FH
110	6MHz	F9H	57H

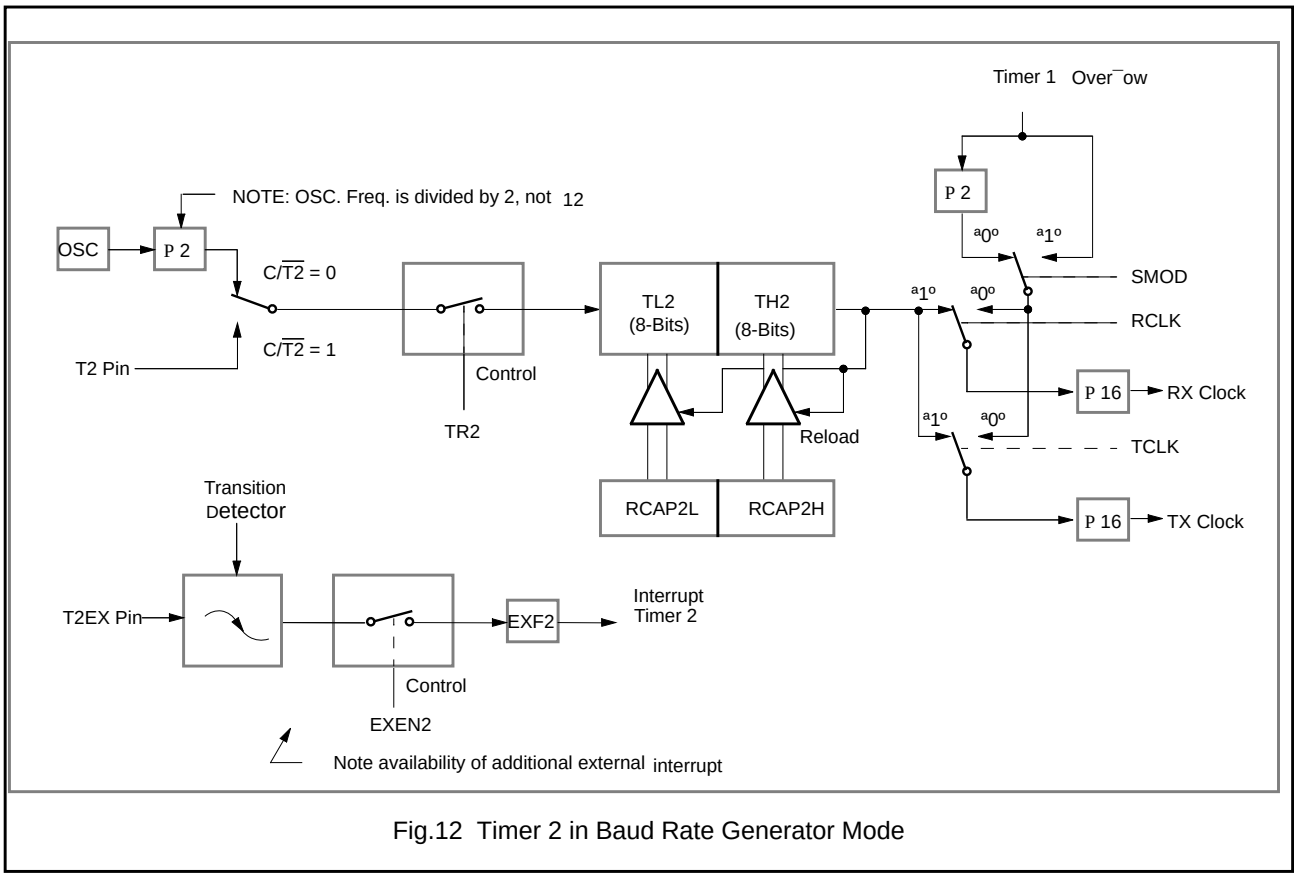


Fig.12 Timer 2 in Baud Rate Generator Mode

Summary of Baud Rate Equations: Timer2 is in baud rate generating mode. If Timer2 is being clocked through pin T2 (P1.0) the baud rate is:

(4)

$$\frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer2 is being clocked internally, the baud rate is:

(5)

$$\frac{\text{Oscillator Frequency}}{32 \times (65536 \pm (\text{RCAP2H, RCAP2L}))}$$

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

(6)

$$= \pm \frac{\quad}{\times}$$

Where f_{OSC} = Oscillator Frequency

Timer/Counter2 Set-up: Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 Bit. Therefore, Bit TR2 must be set, separately, to turn the timer on.

Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL[1]	EXTERNAL CONTROL[2]
16-Bit Auto-Reload	00H	08H
16-Bit Capture	01H	09H
Baud Rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Timer 2 as a Counter

MODE	T2MOD	
	INTERNAL CONTROL[1]	EXTERNAL CONTROL[2]
16-Bit	02H	04H
Auto-Reload	03H	0BH

Note

1. Capture/Reload occurs only on timer/counter overflow.
2. Capture/Reload on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer2 is used in the Baud Rate generator mode.

ENHANCED UART

The UART operates in all of the usual modes that are described in the first section of *Data Handbook IC20, 80C51-Based 8-Bit Microcontrollers*. In addition the UART can perform framing error detect by looking for missing stop Bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect the UART looks for missing stop Bits in the communication. A missing Bit will set the FE Bit in the SCON register. The FE Bit shares the SCON.7 Bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE SCON.7 can only be cleared by software.

SCON: Serial Port Control Register

Register Name	Register Address	Bit	Symbol	Function
SCON	98H	SCON.7	SM0/FE	**SM0:** Serial Port Mode Bit 0, (SMOD0[1] must = 0 to access Bit SM0) **FE:** Framing Error Bit. This Bit is set by the receiver when an invalid stop Bit is detected. The FE Bit is not cleared by valid frames but should be cleared by software. The SMOD0[1] Bit must be set to enable access to the FE Bit.
		SCON.6	SM1	Serial Port Mode Bit 1
		SCON.5	SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then Rl will not be set unless the received 9th data Bit (RB8) is 1, indicating an address, and the received Byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then Rl will not be activated unless a valid stop Bit was received, and the received Byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
		SCON.4	REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
		SCON.3	TB8	The 9th data Bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired. In Mode 0, RB8 is not used.
		SCON.2	RB8	In modes 2 and 3, the 9th data Bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop Bit that was received. In Mode 0, RB8 is not used.
		SCON.1	Tl	Transmit interrupt ¯ag. Set by hardware at the end of the 8th Bit time in Mode 0, or at the beginning of the stop Bit in the other modes, in any serial transmission. Must be cleared by software.
		SCON.0	Rl	Receive interrupt ¯ag. Set by hardware at the end of the 8th Bit time in Mode 0, or halfway through the stop Bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Note

1. SMOD0 is located at PCON.6.

Enhanced UART Modes

SM0	SM1	MODE	DESCRIPTION	BAUD-RATE
0	0	0	shift register	f/12
0	1	1	8-Bit UART	variable
1	0	2	9-Bit UART	$f_{XTAL1}/64$ or $f_{XTAL1}/32$
1	1	3	9-Bit UART	variable

Automatic Address Recognition: Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial Bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 Bit in SCON. In the 9 Bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received Byte contains either the ªGivenº address or the ªBroadcastº address. The 9-Bit mode requires that the 9th information Bit is a 1 to indicate that the received information is an address and not data.

The 8 Bit mode is called Mode1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop Bit following the 8 address Bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which Bits in the SADDR are to be used and which Bits are ªdon't careº. The SADEN mask can be logically ANDed with the SADDR to create the ªGivenº address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0

SADDR	1100 0000
SADEN	1111 1101
Given	1100 00X0

Slave 1

SADDR	1100 0000
SADEN	1111 1110
Given	1100 000X

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in Bit 0 and it ignores Bit 1. Slave 1 requires a 0 in Bit 1 and Bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in Bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in Bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has Bit 0 = 0 (for slave 0) and Bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0

SADDR	1100 0000
SADEN	1111 1001
Given	1100 0XX0

Slave 1

SADDR	1110 0000
SADEN	1111 1010
Given	1110 0X0X

Slave 2

SADDR	1110 0000
SADEN	1111 1100
Given	1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address Bits. Slave 0 requires that Bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that Bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that Bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make Bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FFH hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are leaded with 0s. This produces a given address of all ªdon't caresº as well as a Broadcast address of all ªdon't caresº. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51 type UART drivers which do not make use of this feature.

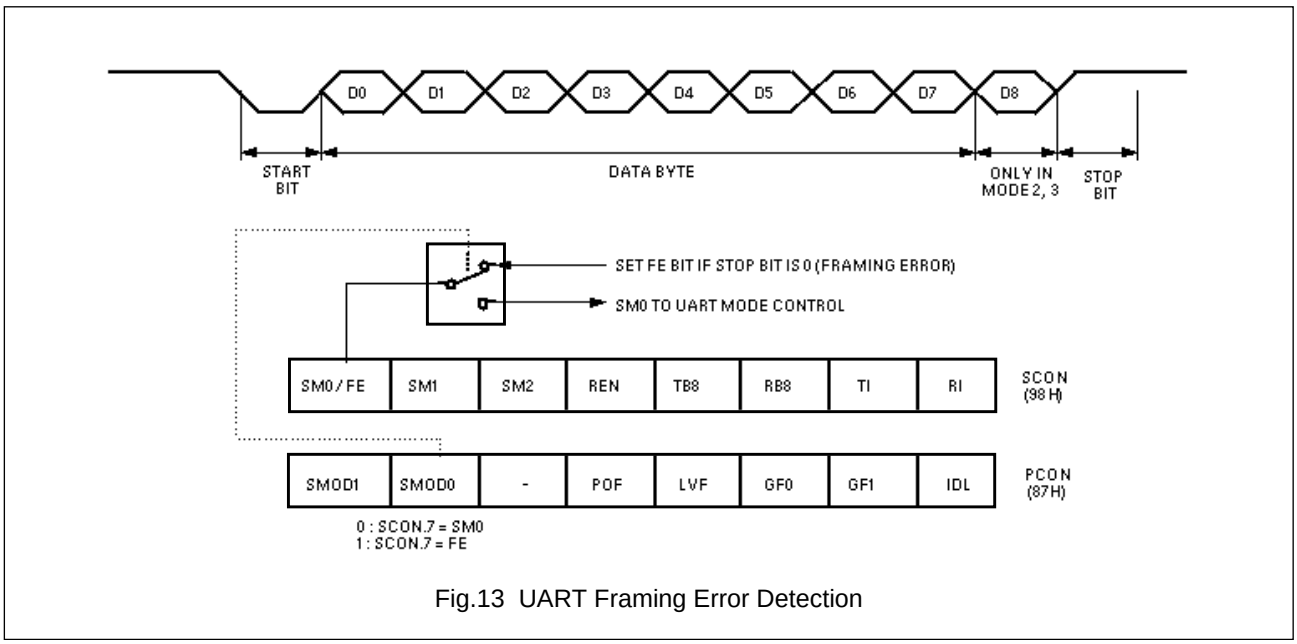


Fig.13 UART Framing Error Detection

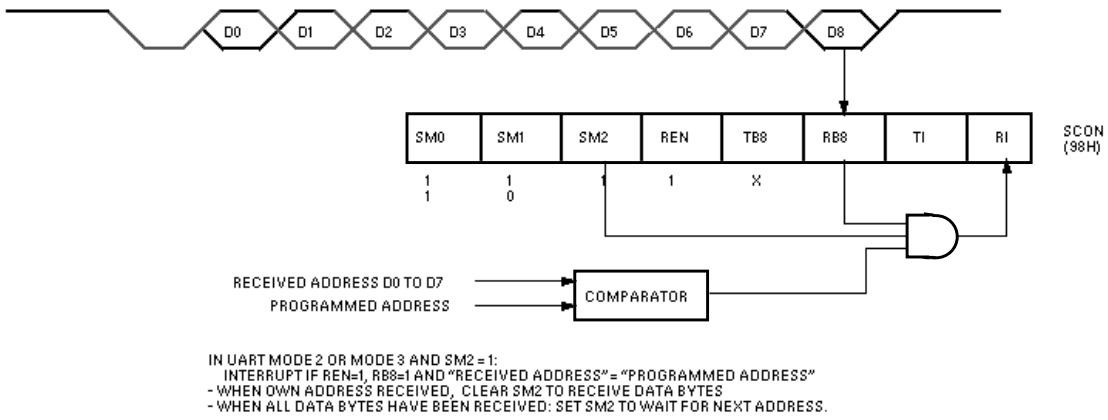


Fig.14 UART Multiprocessor Communication, Automatic Address Recognation

INTERRUPT PRIORITY STRUCTURE

The TDA8028/TDA8008 have a 6-source four-level interrupt structure.

There are 3 SFRs associated with the four-level interrupt. They are the IE, IP, and IPH. The IPH (Interrupt Priority High) register makes the four-level interrupt structure possible. The IPH is located at SFR address B7H.

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

Priority Bits

IPH.x	IP.x	INTERRUPT PRIORITY LEVEL
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Interrupt Table

SOURCE	Polling Priority	Request Bits	Hardware Clear?	Vector Address
X0	1	IE0	N[1], Y[2]	03H
T0	2	TF0	Y	0BH
X1	3	IE1	N[1], Y[2]	13H
T1	4	TF1	Y	1BH
SP	5	RI, TI	N	23H
T2	6	TF2, EXF2	N	2BH

Notes

1. Level activated
2. Transition activated

IE Register

Register Name	Register Address	Bit[1]	Symbol	Function
IE	A8H	IE.7	EA	Global disable Bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable Bit.
		IE.6	-	Not implemented, reserved for future use.[2]
		IE.5	ET2	Timer 2 interrupt enable Bit.
		IE.4	ES	Serial Port interrupt enable Bit.
		IE.3	ET1	Timer 1 interrupt enable Bit.
		IE.2	EX1	External interrupt 1 enable Bit.
		IE.1	ET0	Timer 0 interrupt enable Bit.
		IE.0	EX0	External interrupt 0 enable Bit.

Notes

1. Enable Bit = 1 enables the interrupt / Enable Bit = 0 disables it.
2. User software should not write 1s to reserved Bits. These Bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new Bit will be 0, and its active value will be 1. The value read from a reserved Bit is indeterminate.

IP Register

Register Name	Register Address	Bit[1]	Symbol	Function
IP	B8H	IP.7	-	Not implemented, reserved for future use.[2]
		IP.6	-	Not implemented, reserved for future use.[2]
		IP.5	PT2	Timer 2 interrupt priority Bit.
		IP.4	PS	Serial Port interrupt priority Bit.
		IP.3	PT1	Timer 1 interrupt priority Bit.
		IP.2	PX1	External interrupt 1 priority Bit.
		IP.1	PT0	Timer 0 interrupt priority Bit.
		IP.0	PX0	External interrupt 0 priority Bit.

Notes

1. Priority Bit = 1 assigns high priority / Priority Bit = 0 assigns low priority.
2. User software should not write 1s to reserved Bits. These Bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new Bit will be 0, and its active value will be 1. The value read from a reserved Bit is indeterminate.

IPH Register

Register Name	Register Address	Bit[1]	Symbol	Function
IPH	B7H	IPH.7	-	Not implemented, reserved for future use.[2]
		IPH.6	-	Not implemented, reserved for future use.[2]
		IPH.5	PT2H	Timer 2 interrupt priority Bit high.
		IPH.4	PSH	Serial Port interrupt priority Bit high.
		IPH.3	PT1H	Timer 1 interrupt priority Bit high.
		IPH.2	PX1H	External interrupt 1 priority Bit high.
		IPH.1	PT0H	Timer 0 interrupt priority Bit high.
		IPH.0	PX0H	External interrupt 0 priority Bit high.

Notes

1. Priority Bit High = 1 assigns higher priority / Priority Bit High = 0 assigns lower priority.
2. User software should not write 1s to reserved Bits. These Bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new Bit will be 0, and its active value will be 1. The value read from a reserved Bit is indeterminate.

REDUCED EMI MODE

The AO Bit (AUXR.0) in the AUXR register when set disables the ALE output.

DUAL DPTR

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-Bit DPTR registers that address the external memory, and a single Bit called DPS = AUXR1/Bit0 that allows the program code to switch between them.

The DPS Bit status should be saved by software when switching between DPTR0 and DPTR1.

The GF3 Bit is a general purpose user-defined flag. Note that Bit 2 is not writable and is always read as a zero. This allows the DPS Bit to be quickly toggled simply by executing an INC AUXR1 instruction without affecting the GF3 or LPEP Bits.

DPTR Instructions: The instructions that refer to DPTR refer to the data pointer that is currently selected using the Bit AUXR1. 0 in the AUXR1 register. The six instructions that use the DPTR are as follows:

DPTR Instructions

INC DPTR	Increments the data pointer by 1
MOV DPTR, #data16	Loads the DPTR with a 16-Bit constant
MOV A, @A+DPTR	Move code Byte relative to DPTR to ACC
MOVX A, @DPTR	Move external RAM (16-Bit address) to ACC
MOVX @DPTR, A	Move ACC to external RAM (16-Bit address)
JMP @A+DPTR	Jump indirect relative to DPTR

The data pointer can be accessed on a Byte-by-Byte basis by specifying the low or high Byte in an instruction which accesses the SFRs.

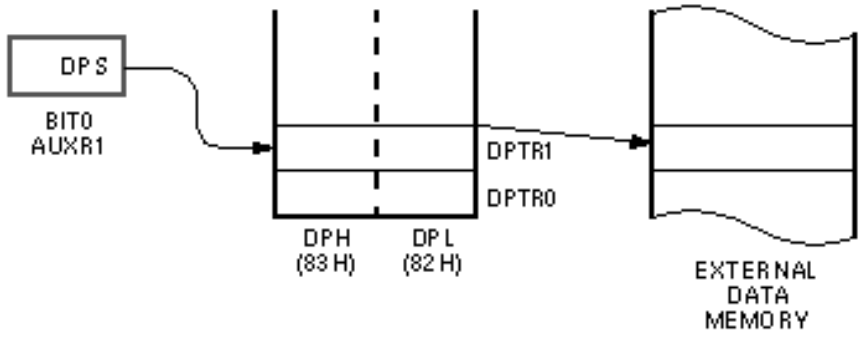


Fig.15 Dual DPTR

EXPANDED DATA RAM ADDRESSING

The TDA8028/TDA8008 have internal data memory that is mapped into four separate segments: the lower 128Bytes of RAM, upper 128Bytes of RAM, 128Bytes Special Function Register (SFR), and 512Bytes expanded RAM (EXTRAM).

The four segments are:

1. The Lower 128 Bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.

2. The Upper 128 Bytes of RAM (addresses 80H to FFH) are indirectly addressable only.

3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.

4. The 512Bytes expanded RAM (EXTRAM (512 Bytes) 00H-1FFH) and are indirectly accessed by move external instruction, MOVX, and with the EXTRAM Bit (AUXR.1) cleared.

The Lower 128 Bytes can be accessed by either direct or indirect addressing. The Upper 128 Bytes can be accessed by indirect addressing only. The Upper 128 Bytes occupy the same address space as the SFR. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 Bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example: ªMOV A0H, #dataº accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the Upper 128 Bytes of data RAM.

For example: ªMOV @R0,#dataº where R0 contains 0A0H, accesses the data Byte at address 0A0H, rather than P2 (whose address is 0A0H).

The EXTRAM can be accessed by indirect addressing, with EXTRAM Bit (AUXR.1) cleared and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 512 Bytes of external data memory.

With EXTRAM = 0, the EXTRAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to EXTRAM will not affect ports P0, P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$). P2 SFR is output during external addressing. For example, with EXTRAM = 0, ªMOVX @R0, Aº where R0 contains 0A0H, access the EXTRAM at address 0A0H rather than external memory. An access to external data memory locations higher than 1FFH (i.e., 0200H to FFFFH) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

With EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51. MOVX @Ri will provide an 8-Bit address multiplexed with data on Port0 and any output port pins can be used to output higher order address Bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-Bit address. Port2 outputs the

high-order eight address Bits (the contents of DPH) while Port0 multiplexes the low-order eight address Bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either read or write signals on P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$).

The stack pointer (SP) may be located anywhere in the 256 Bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the EXTRAM.

AUXR: Auxiliary Register

Register Name	Register Address	Bit	Symbol	Function
AUXR	8EH	AUXR.7	-	Not implemented, reserved for future use.[1]
		AUXR.6	-	Not implemented, reserved for future use.[1]
		AUXR.5	-	Not implemented, reserved for future use.[1]
		AUXR.4	-	Not implemented, reserved for future use.[1]
		AUXR.3	-	Not implemented, reserved for future use.[1]
		AUXR.2	-	Not implemented, reserved for future use.[1]
		AUXR.1	EXTRAM	Internal/External RAM access using MOVX @Ri/@DPTR EXTRAM=0: Internal ERAM (0000H-01FFH) access using MOVX @Ri/@DPTR EXTRAM=1: External data memory access.
		AUXR.0	AO	Disable/Enable ALE AO=0: ALE is emitted at a constant rate of 1/6 the XTAL-oscillator frequency. AO=1: ALE is active only during a MOVX or MOVC instruction.

Note

1. User software should not write 1s to reserved Bits. These Bits may be used in future 8051 family products to invoke new features. In that case, the reset or inactive value of the new Bit will be 0, and its active value will be 1. The value read from a reserved Bit is indeterminate.

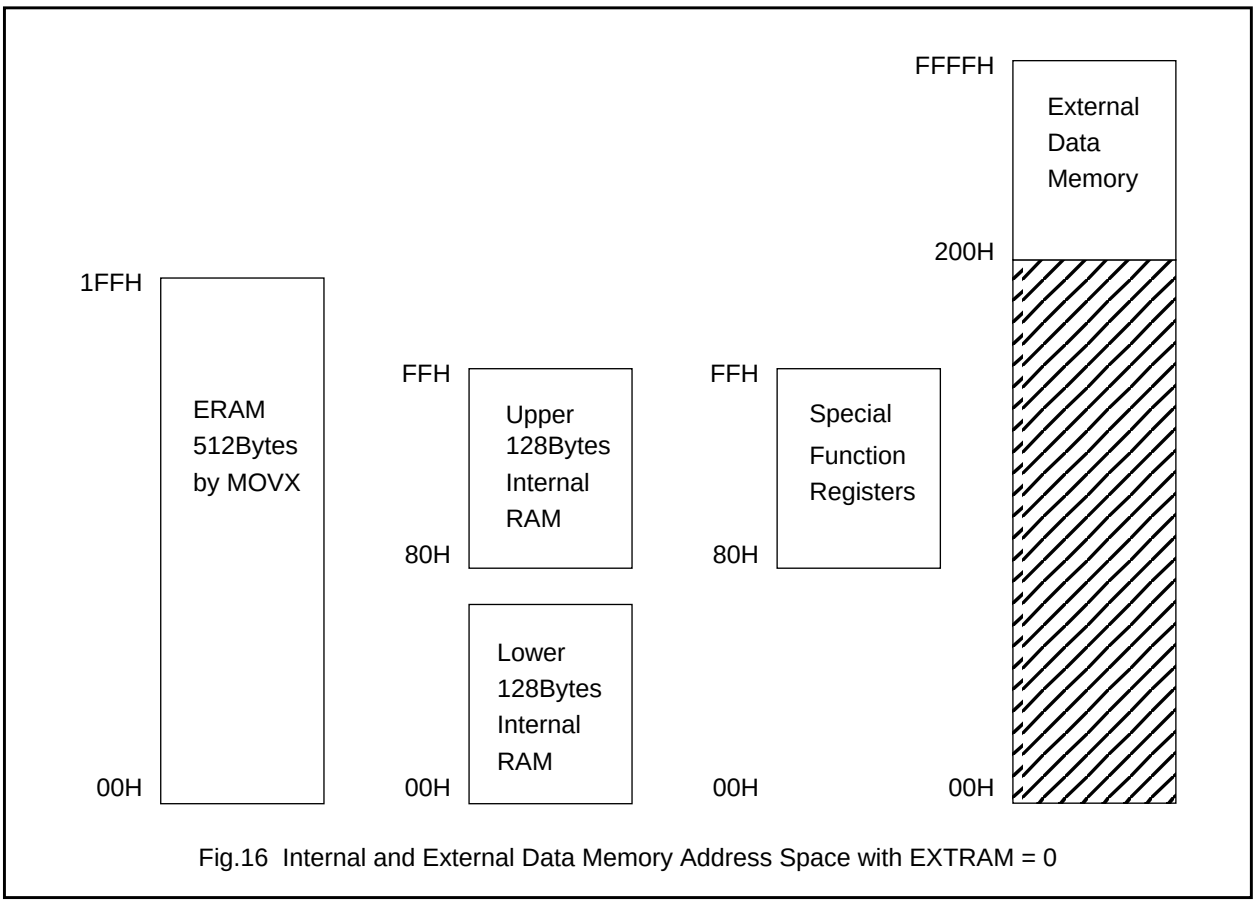


Fig.16 Internal and External Data Memory Address Space with EXTRAM = 0

EPROM CHARACTERISTICS

The OTP-device TDA8008 can be programmed by using a modified Improved Quick-Pulse Programming™ (Trademark phrase of Intel Corporation.) algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses. If commercial programmers are used, the 87C51RB+ algorithm has to be chosen.

The TDA8008 contains two signature Bytes that can be read and used by an EPROM programming system to identify the device. The signature Bytes identify the device as being manufactured by Philips.

Quick-Pulse Programming: Note that the device is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2. The code Byte to be programmed into that location is applied to port 0. RST, $\overline{PSEN}$ and pins of ports 2 and 3 are held at the ÁProgram Code Data' levels. The ALE/$\overline{PROG}$ is pulsed low 5 times 100µs +/-10µs with a delay of minimum 10µs between 2 programming pulses.

To program the encryption table, repeat the 5 pulse programming sequence for addresses 0 through 1FH, using the ÁPgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security Bits, repeat the 5 pulse programming sequence using the ÁPgm Security Bit' levels. After one security Bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security Bits can still be programmed.

Note that the $\overline{EA}/V_{PP}$ pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification: If security Bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2. The other pins are held at the ÁVerify Code Data' levels. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the 64 Byte encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program Byte with one of the encryption Bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes: The signature Bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = CBH indicates TDA8008

(060H) = NA

Security Bits: With none of the security Bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security Bit 1 is programmed, MOVC instructions executed from external program memory are disabled from fetching code Bytes from the internal memory, $\overline{EA}$ is latched on Reset and all further programming of the EPROM is disabled. When security Bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security Bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

Encryption Array: 64 Bytes of encryption array are initially unprogrammed (all 1s).

EPROM Programming Modes

MODE	RESET	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.7	P2.6	P3.7	P3.6
Read Signature	1	0	1	1	0	0	0	0
Program code data	1	0	0	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Program encryption table	1	0	0	V_{PP}	1	0	1	0
Program security Bit1	1	0	0	V_{PP}	1	1	1	1
Program security Bit2	1	0	0	V_{PP}	1	1	0	0
Program security Bit3	1	0	0	V_{PP}	0	1	0	1

Note

1. `0' = valid low for that pin, `1' = valid high for that pin.
2. V_{PP} = 12.75V+/-0.25V.
3. Supply voltage during programming and verification must be 5V+/-10%.
4. ALE/$\overline{PROG}$ receives 5 programming pulses for code data (also for user array; 5 pulses for encryption or security Bits) while V_{PP} is held at 12.75V. Each programming pulse is low for 100µs+/-10µs and high for a minimum of 10µs.

Program Security Bits for TDA8008

PROGRAM LOCK BITS[1,2]			PROTECTION DESCRIPTION
SB1	SB2	SB3	
U	U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
P	U	U	MOVC instructions executed from external program memory are disabled from fetching code Bytes from internal memory, $\overline{EA}$ is sampled and latched on reset and further programming of the EPROM is disabled.
P	P	U	Same as above, also verify is disabled.
P	P	P	Same as above and external execution is disabled.

Note

1. P - programmed. U - unprogrammed.
2. Any other combination of the security Bits is not defined.

ROM CODE SUBMISSION FOR 16K EPROM DEVICE TDA8008

When submitting ROM code for the 16K EPROM devices, the following must be specified:

1. 16k Byte user EPROM data

2. 64 Byte EPROM encryption key

3. EPROM security Bits.

MASK ROM DEVICES

Security Bits: With none of the security Bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security Bit 1 is programmed, MOVC instructions executed from external program memory are disabled from fetching code Bytes from the internal memory. When security Bits 1 and 2 are programmed, in addition to the above, verify mode is disabled.

Encryption Array: 64 Bytes of encryption array are initially unprogrammed (all 1s).

Program Security Bits for TDA8028

PROGRAM LOCK BITS[1,2]		PROTECTION DESCRIPTION
SB1	SB2	
U	U	No Program Security features enabled. (Code verify will still be encrypted by the Encryption Array if programmed.)
P	U	MOVC instructions executed from external program memory are disabled from fetching code Bytes from internal memory.
P	P	Same as above, also verify is disabled.

Note

1. P - programmed. U - unprogrammed.
2. Any other combination of the security Bits is not defined.

ROM CODE SUBMISSION FOR 16K ROM DEVICE TDA8028

When submitting ROM code for the 16K ROM devices, the following must be specified:

1. 16k Byte user ROM data
2. 64 Byte ROM encryption key
3. ROM security Bits.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.5	6.5	V
V_{DDD}	digital supply voltage		–0.5	6.5	V
V_{DDP}	power supply voltage for step-up converter		–0.5	6.5	V
V_n	all input voltage except SAM, SAP, SBM, SBP, VUP		–0.5	V_{DD} + 0.5	V
V_n	voltage on pins SAM, SAP, SBM, SBP, VUP		–0.5	7.5	V
I_{n1}	DC current into all pins except SAM, SAP, SBM, SBP, VUP		–5	5	mA
I_{n3}	DC current from or to SAM, SAP, SBM, SBP, VUP		-200	200	mA
P_{tot}	continuous total power dissipation LQFP80	T_{amb} = –20 to +85°C	–	tbf	mW
P_{tot}	continuous total power dissipation LQFP64	T_{amb} = –20 to +85°C	–	tbf	mW
T_{stg}	IC storage temperature		–55	+150	°C
T_j	operating junction temperature			+125	°C
V_{es}	electrostatic discharge	on pins I/O1, VCC1, RST1, CLK1, C41, C81, GNDC1, PRES1, I/O2, VCC2, RST2, CLK2, C42, C82, GNDC2 and PRES2	–6	+6	kV
		on other pins	–2	+2	kV

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air (LQFP80)	55	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{DD} = 3.3 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise speci®ed.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.7	–	6.0	V
$I_{DD(sm)}$	supply current sleep mode	both cards powered, but with CLK stopped	-	-	tbf	µA
$I_{DD(om)}$	supply current operating mode	ICC1=65mA; ICC2=15mA; f_{xtal} = 20MHz, f_{clk} = 10MHz; 5V cards; VDD=2.7V	-	-	300	mA
		ICC1=65mA; ICC2=15mA; f_{xtal} = 20MHz, f_{clk} = 10MHz; 3V cards; VDD=2.7V	-	-	200	mA
		ICC1=65mA; ICC2=15mA; f_{xtal} = 20MHz, f_{clk} = 10MHz; 3V cards; VDD=5V	-	-	100	mA
V_{th1}	threshold voltage on V_{DD} (falling)		2.25	–	2.50	V
V_{hys1}	hysteresis on V_{th1}		50	–	170	mV
V_{th2}	threshold voltage on DELAY		–	1.38	–	V
V_{DEL}	voltage on pin DELAY		–	–	V_{DD}+0.3	V
I_{DEL}	output current at DELAY	pin grounded (charge)	–	–2	–	µA
		V_{DEL} = V_{DD} (discharge)	–	2	–	mA
t_W	ALARM pulse width	C_{DEL} = 22nF	–	10	–	ms
RSTOUT (open drain active HIGH or LOW output)						
I_{OH}	HIGH level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW level output voltage	active LOW option; I_{OL} = 2 mA	-0.3	–	0.4	V
I_{OL}	LOW level output current	active HIGH option, V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH level output voltage	active HIGH option, I_{OH} = –1 mA	0.8VDD	–	VDD+0.3	V
Crystal oscillator						
f_{xtal}	crystal frequency		4	–	25	MHz
f_{EXT}	external frequency applied on XTAL1		0	–	25	MHz
Step-up converter						
f_{INT}	oscillation frequency		2	2.5	3	MHz
V_{UP}	voltage on VUP	at least one 5V card	–	5.7	–	V
V_{UP}	voltage on VUP	both cards 3V	–	4.1	–	V
V_{dt}	detection voltage for double/tripler selection		3.4	3.5	3.6	V
Reset output to the cards (RST1, RST2)						
$V_{inactive}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{inactive}$	current from RST when inactive and pin grounded		0	–	–1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200µA	0	–	0.3	V
V_{OH}	HIGH level output voltage	I_{OH} =-200µA	V_{CC} – 0.7	–	V_{CC}	V
t_r	rise time	C_L = 30pF	–	–	0.1	µs
t_f	fall time	C_L = 30pF	–	–	0.1	µs
Clock output to the cards (CLK1, CLK2)						
$V_{inactive}$	output voltage in inactive mode	no load	0	–	0.1	V
		$I_{inactive}$ = 1mA	0	–	0.3	V
$I_{inactive}$	current from CLK when inactive and pin grounded		0	–	–1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200µA	0	–	0.3	V
V_{OH}	HIGH level output voltage	I_{OH} = -200µA	VCC-0.5	–	V_{CC}	V
t_r	rise time	C_L = 30pF	–	–	8	ns
t_f	fall time	C_L = 30pF	–	–	8	ns
f_{clk}	clock frequency	1MHz Idle con®guration	1	–	1.5	MHz
		operational	0	–	10	MHz
δ	duty cycle	C_L = 30pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30pF	0.2			V/ns
Card supply voltage (V_{CC1},VCC2) (2 ceramic multi-layer capacitances with low ESR of minimum 100nF should be used in order to meet these specs)						
$V_{inactive}$	output voltage inactive	no load	0	–	0.1	V
		$I_{inactive}$ = 1mA	0	–	0.3	V
$I_{inactive}$	current from VCC when inactive and pin grounded		–	–	–1	mA
VCC	output voltage	active mode; ICC<65mA; 5V card	4.75	5	5.25	V
		active mode; ICC<65mA; 3V card	2.78	3	3.22	V
		active mode; current pulses of 40nAs with I<200mA, t<400ns, f<20MHz; 5V card	4.6		5.4	V
		active mode; current pulses of 24nAs with I<200mA, t<400ns, f<20MHz; 3V card	2.75		3.25	V
$-I_{CC}$	output current	from 0 t0 3 or 5V	–	–	65	mA
SR	slew rate	up or down (max capacitor=300 nF)	0.05	0.16	0.22	V/µs
ICC1+ICC2	sum of both cards current				80	mA
Data lines (I/O1, I/O2); Note: I/O1 has an integrated 10k pull-up at VCC1, I/O2 to VCC2						
$V_{inactive}$	output voltage inactive	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	–	–	0.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{inactive}$	current from I/O when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW level output voltage (I/O con®gured as an output)	I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH level output voltage (I/O con®gured as an output)	I/O con®gured as an output; I_{OH} <-40 µA	0.8VCC	–	V_{CC} + 0.25	V
V_{IL}	input voltage LOW (I/O con®gured as an input)		–0.3	–	0.8	V
V_{IH}	input voltage HIGH (I/O con®gured as an input)		1.5	–	V_{CC}	V
I_{IL}	input current LOW on I/O	V_{IL} =0			600	µA
I_{LIH}	input leakage current HIGH on I/O	V_{IH}=VCC			20	µA
t_r, t_f	input transition times	C_L = 30 pF	–	–	1	µs
t_r, t_f	output transition times	C_L = 30 pF	–	–	0.1	µs
R_{pu}	internal pull-up resistance between I/O and VCC		8k	10k	12k	Ω
Auxiliary cards contacts (C41, C81, C42, C82) Note: C41and C81 have integrated 10k pull-up at VCC1, C42 and C82 have integrated 20k pull-up at VCC2.						
$V_{inactive}$	output voltage inactive	no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	–	–	0.3	V
$I_{inactive}$	current from C4 or C8 when inactive and pin grounded		–	–	–1	mA
V_{OL}	LOW level output voltage (C4 or C8 con®gured as an output)	I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH level output voltage (C4 or C8 con®gured as an output)	I/O con®gured as an output; I_{OH} <-50 µA	0.8VCC	–	V_{CC} + 0.25	V
V_{IL}	input voltage LOW (C4 or C8 con®gured as an input)		–0.3	–	0.8	V
V_{IH}	input voltage HIGH (C4 or C8 con®gured as an input)		1.5	–	V_{CC}	V
I_{IL}	input current LOW on C4 or C8	V_{IL} =0			600	µA
I_{LIH}	input leakage current HIGH on C4 or C8	V_{IH}=VCC			20	µA
t_r, t_f	input transition times	C_L = 30 pF	–	–	1	µs
t_r, t_f	output transition times	C_L = 30 pF	–	–	0.1	µs
tedge	*width of active pull up pulse*			*200*		*ns*
R_{pu}	internal pull up resistance between C4/C8 and VCC		8k	10k	12k	Ω
$f_{(max)}$	max frequency on C4 or C8				1	MHz
Timings						

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{act}	activation sequence duration		–	–	130	µs
t_{de}	deactivation sequence duration		–	–	100	µs
Protections and limitations						
$I_{CC(sd)}$	shutdown and limitation current at VCC		-	-100	-	mA
$I_{I/O(lim)}$	limitation current on I/O		-10		+10	mA
$I_{CLK(lim)}$	limitation current on CLK		-70		+70	mA
$I_{RST(sd)}$	shutdown and limitation current on RST		-20		+20	mA
t_{sd}	*shutdown temoerature*			*150*		*°C*
Card presence input1s(PRES1, PRES2)						
V_{IL}	LOW level input voltage		–	–	0.3VDD	V
V_{IH}	HIGH level input voltage		0.7VDD	–	–	V
+/-I_{IL}	input leakage current low	VIN=0	–	–	20	µA
+/-I_{IH}	input leakage current high	VIN=VDD	–	–	20	µA
Logic inputs INTAUX, $\overline{CS}$						
VIL	LOW level input voltage		-0.3		0.3VDD	V
VIH	HIGH level input voltage		0.7VDD		VDD+0.3	V
+/-IIL	input leakage current low				20	uA
+/-IIH	input leakage current high				20	uA
C_{Load}	pin capacitance				10	pF
Auxiliary I/O I/OAUX						
VIL	LOW level input voltage		-0.3		0.3VDD	V
VIH	HIGH level input voltage		0.7VDD		VDD+0.3	V
+/-IIH	input leakage current high				20	uA
-IIL	input current low	VIL=0			600	uA
V_{OL}	output voltage LOW	I_{OL}=1mA			300	mV
V_{OH}	output voltage HIGH	*I_{OH}=40uA*	0.8VDD		VDD+.25	V
Rpu	internal pullup resistance between I/OAUX and VDD		8	10	12	k
tr, tf	input transition times	CL=30pF			1	us
t_r, t_f	output transition times	CL=30pF			0.1	us
f_{IOAUX}	max frequency on I/OAUX				1	MHz

APPLICATION INFORMATION

To be fixed.

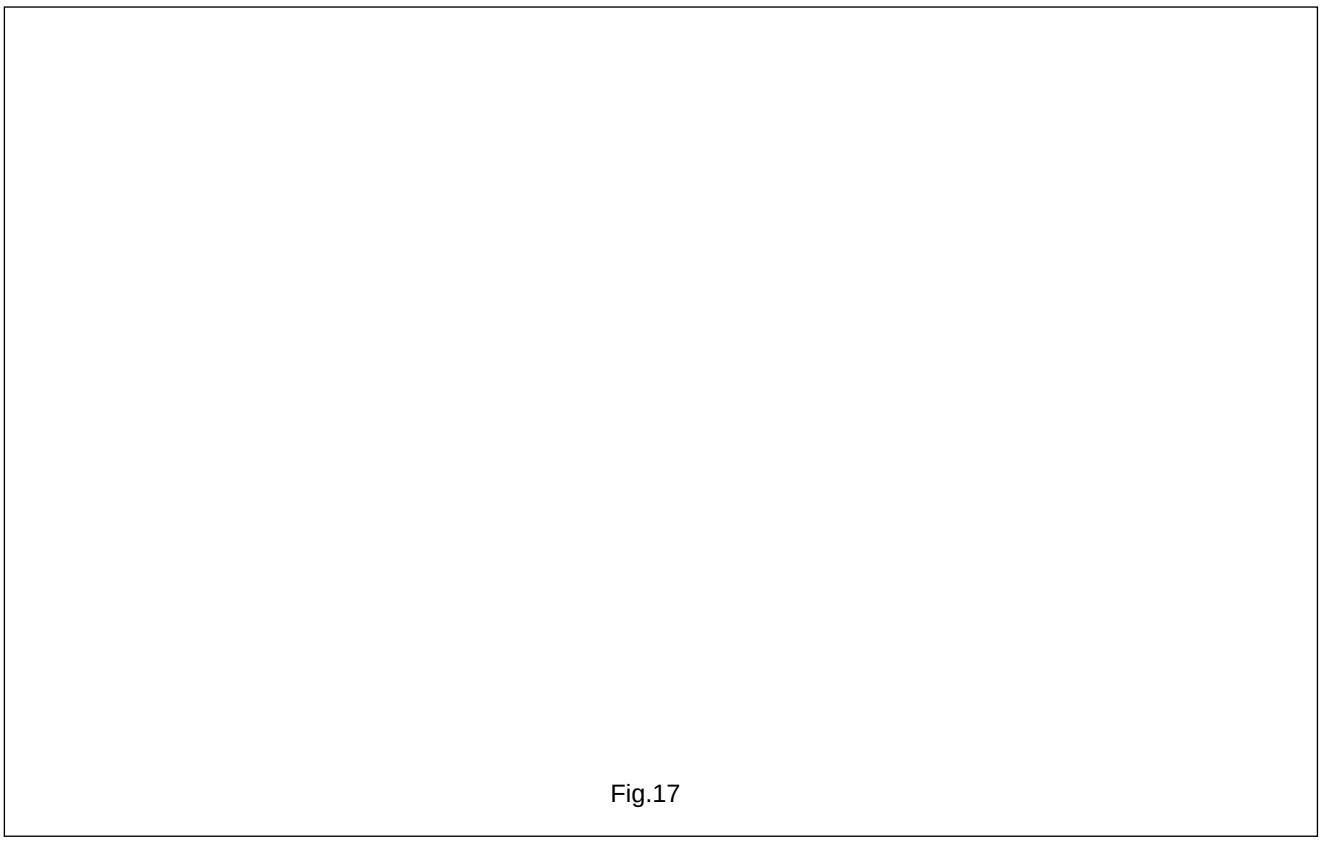
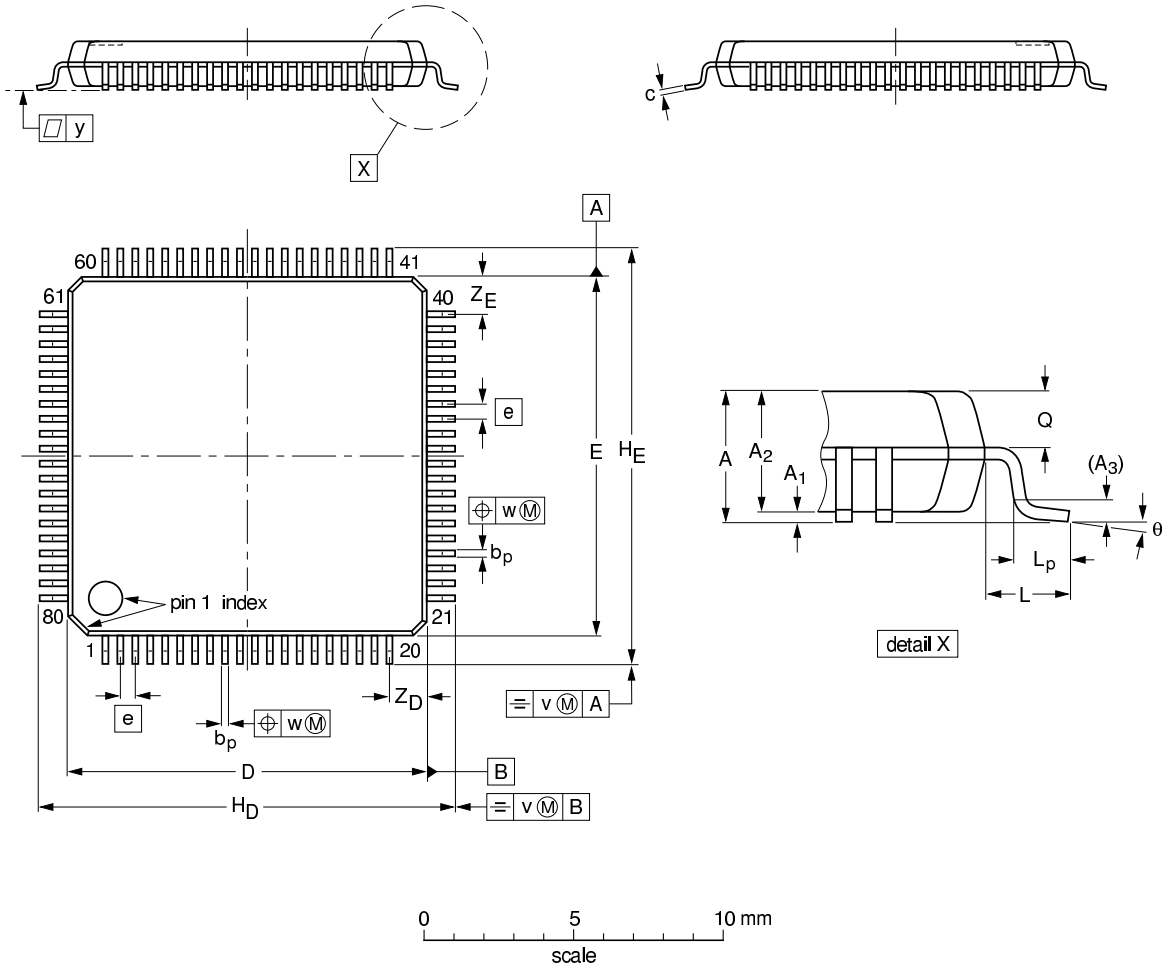


Fig.17

PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.25 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.7 0.3	0.70 0.58	0.2	0.15	0.1	1.45 1.05	1.45 1.05	4^o 0^o

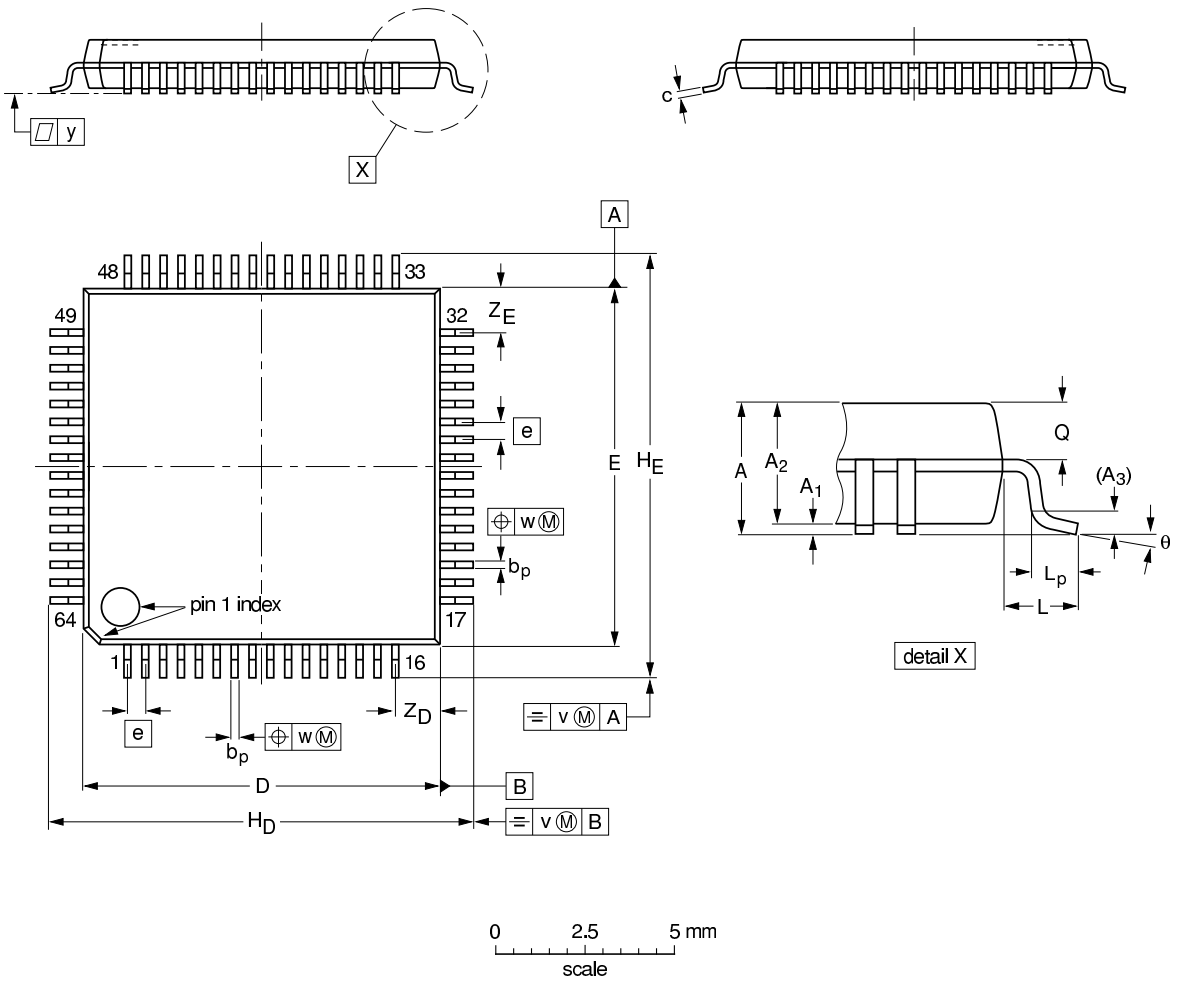
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~92-03-24~~ 95-12-19

PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~94-01-07~~ 95-02-25

SOLDERING

Plastic quad ¯at packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 ºC, and maximum duration of package immersion in solder bath is 10s, if allowed to cool to less than 150 ºC within 6 s. Typical dwell time is 4 s at 250 ºC.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective speci®cation	This data sheet contains target or goal speci®cations for product development.
Preliminary speci®cation	This data sheet contains preliminary data; supplementary data may be published later.
Product speci®cation	This data sheet contains ®nal product speci®cations.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the speci®cation is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the speci®cation.	

LIFE SUPPORT APPLICATIONS

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