DATA SHEET

TDA8008
Dual multiprotocol smart card coupler

Product specification
Supersedes data of 1999 Dec 14

2003 Jul 28

Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- 8xC51 core with 16 kbyte EPROM (OTP); 256 byte RAM; 512 byte AUXRAM; Timers 0, 1 and 2; enhanced UART
- Specific ISO 7816 UART; accessible with MOVX instructions for automatic convention processing; variable baud rate through frequency or division ratio programming, error management at character level for T = 0 protocol; extra guard time register
- FIFO register for 1 to 8 characters in reception mode
- Parity error counter in reception mode; also in transmission mode with automatic re-transmission
- Dual V_{CC} generation with controlled rise and fall times
  - 5 V ± 5%, 65 mA (max.) or
  - 3 V ± 8%, 50 mA (max.) or
  - 1.8 V ± 10%, 30 mA (max.)
- Dual cards clock generation (up to 10 MHz) with three-times synchronous frequency doubling (f_{XTAL}, $^1/_2 f_{XTAL}$, $^1/_4 f_{XTAL}$ and $^1/_8 f_{XTAL}$)
- Cards clock STOP HIGH or STOP LOW or 1.25 MHz (from an integrated oscillator) for cards power reduction mode
- Automatic activation and deactivation sequences through independent sequencers
- Supports the asynchronous protocols T = 0 and T = 1 in accordance with ISO 7816 and EMV 3.1.1
- Versatile 24-bit time-out counter for Answer To Reset (ATR) and waiting time processing
- Specific Elementary Time Unit (ETU) counter for Block Guard Time (BGT); 22 in T = 1 and 16 in T = 0
- Supports synchronous cards
- Current limitations in the event of a short-circuit on pins I/O1, I/O2, V_{CC1}, V_{CC2}, RST1 or RST2)
- Special circuitry for killing spikes during power-on or power-off
- Supply supervisor for power-on and power-off reset
- Step-up converter (supply voltage from 2.7 V to 6 V at 16 MHz), doubler, tripler or follower according to V_{CC} and V_{DD}
- Additional input/output (pin I/OAUX) allowing the use of the ISO 7816 UART for an external card interface
- Additional interrupt input (pin INTAUX) allowing detection of level toggling on an external signal
- Fast and efficient swapping between the three cards due to separate buffering of parameters for each card
- Chip select input allowing use of several devices in parallel and memory space paging
- Enhanced ESD protection on card side: 6 kV (min.)
- Software library for easy integration within the application
- Power-down mode for reduced current consumption when there is no activity.

2 APPLICATIONS

- Multiple smart card readers for multi protocol applications, for example, EMV Banking, digital pay TV and access control.

3 GENERAL DESCRIPTION

The TDA8008 is a complete, single-chip, cost-efficient dual smart card coupler.

Designed to be used as the kernel of a multiple card reader, it takes care of all ISO 7816, EMV 3.1.1 and GSM11-11 requirements. The integrated ISO 7816 UART and the time-out counters allow easy use with no real time constraints, even at high baud rates.

Due to the chip-select and external I/O and interrupt features, the TDA8008 greatly simplifies the realization of a reader for any number of cards. It gives the cards and the application a very high level of security through special hardware protection against ESD, short-circuiting, power failure and overheating.

The integrated step-up converter allows operation within a supply voltage range of 2.7 to 6 V at f_{XTAL} = 16 MHz.

A software library has been developed, taking care of all actions required for T = 0, T = 1 and synchronous protocols.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8008HLC2	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	$V_{DDD} = V_{DDA} = V_{DDP}$	2.7	–	6.0	V
$I_{DD(pd)}$	supply current in Power-down mode	V_{DD} = 3.3 V; both cards inactive; XTAL oscillator stopped; note 1	–	–	500	µA
$I_{DD(sm)}$	supply current in Sleep mode	V_{DD} = 3.3 V; both cards powered; clock stopped; note 1	–	–	6	mA
$I_{DD(oper)}$	supply current in operating mode	V_{DD} = 3.3 V; f_{XTAL1} = 20 MHz; $V_{CC1} = V_{CC2}$ = 5 V; $I_{CC1} + I_{CC2}$ = 80 mA; note 1	–	–	300	mA
V_{CC}	card supply output voltage	5 V card				
		including static loads	4.75	5.0	5.25	V
		with 40 nC dynamic loads; 200 nF capacitor	4.6	–	5.4	V
		3 V card				
		including static loads	2.78	3.0	3.22	V
		with 24 nC dynamic loads; 200 nF capacitor	2.75	–	3.25	V
		1.8 V card				
		including static loads	1.65	1.8	1.95	V
		with 12 nC dynamic loads; 200 nF capacitor	1.62	–	1.98	V
I_{CC}	card supply output current	5 V card; operating	–	–	65	mA
		3 V card; operating	–	–	50	mA
		1.8 V card; operating	–	–	30	mA
$I_{CC1} + I_{CC2}$	sum of currents for both cards		–	–	80	mA
$I_{CC(sd)}$	shutdown and limitation current at V_{CC}		–	100	–	mA
SR	slew rate on V_{CC}	voltage moving up or down; capacitance = 300 nF (max.)	0.05	0.16	0.22	V/µs
t_{act}	duration of activation sequence		–	–	130	µs
t_{deact}	duration of deactivation sequence		–	–	100	µs
f_{XTAL}	crystal frequency		4	–	20	MHz
f_{EXT}	external frequency applied on pin XTAL1		0	–	20	MHz
T_{amb}	ambient temperature		–30	–	+85	°C

Note

1. Includes currents at pins V_{DDD}, V_{DDA} and V_{DDP}.

6 BLOCK DIAGRAM

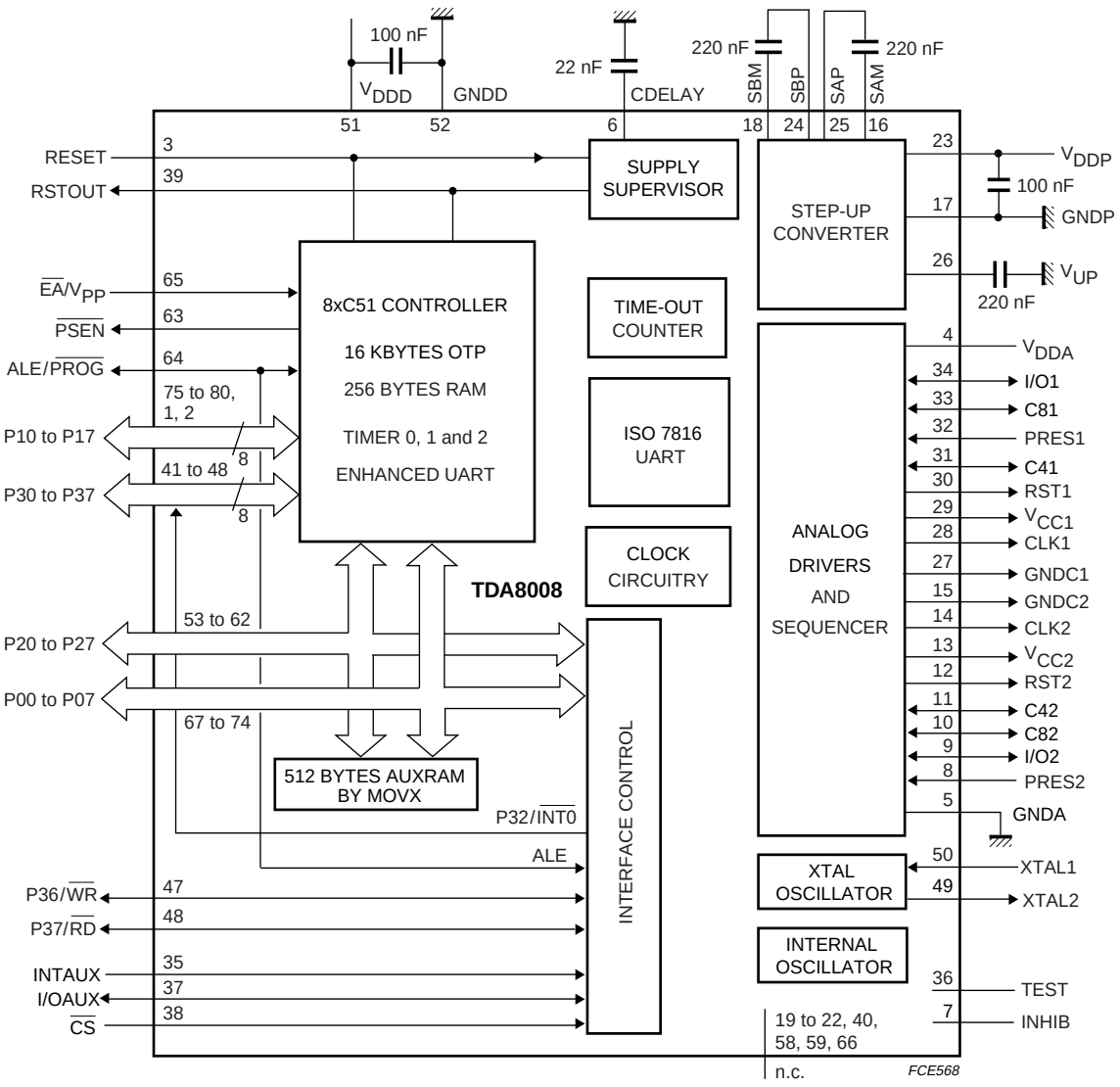


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
P16	1	8xC51 general purpose I/O port
P17	2	8xC51 general purpose I/O port
RESET	3	reset input; a HIGH-level sustained on this pin for two machine cycles while the oscillator is running resets the device; the Power-on reset is derived from an internal diffused resistor to GNDD coupled with an external capacitor to V_{DDD}
V_{DDA}	4	analog power supply voltage
GNDA	5	analog ground
CDELAY	6	pin for an external delay capacitor
INHIB	7	test pin; leave open-circuit in the application
PRES2	8	card 2 presence contact input; active HIGH
I/O2	9	data line to/from card 2 for ISO C7 contact
C82	10	auxiliary I/O for ISO C8 contact for card 2 (for example, for synchronous cards)
C42	11	auxiliary I/O for ISO C4 contact for card 2 (for example, for synchronous cards)
RST2	12	reset output to card 2 for ISO C2 contact
V_{CC2}	13	card 2 supply voltage output for ISO C1 contact (connect two low ESR 100 nF capacitors between V_{CC2} and GNDC2)
CLK2	14	clock output to card 2 for ISO C3 contact
GNDC2	15	ground connection for card 2 (connect to system ground)
SAM	16	contact 2 for the step-up converter (connect a low ESR 220 nF capacitor between pin SAP and pin SAM)
GNDP	17	ground connection for the step-up converter
SBM	18	contact 4 for the step-up converter (connect a low ESR 220 nF capacitor between pin SBP and pin SBM)
n.c.	19 to 22	not connected
V_{DDP}	23	positive supply voltage for the step-up converter
SBP	24	contact 3 for the step-up converter (connect a low ESR 220 nF capacitor between pin SBP and pin SBM)
SAP	25	contact 1 for the step-up converter (connect a low ESR 220 nF capacitor between pin SAP and pin SAM)
V_{UP}	26	output of the step-up converter (connect a low ESR 220 nF capacitor between pin V_{UP} and GNDP)
GNDC1	27	ground connection for card 1 (connect to system ground)
CLK1	28	clock output to card 1 for ISO C3 contact
V_{CC1}	29	card 1 supply output voltage for ISO C1 contact (connect two low ESR 100 nF capacitors between V_{CC1} and GNDC1)
RST1	30	reset output to card 1 for ISO C2 contact
C41	31	auxiliary I/O for ISO C4 contact for card 1 (for example, for synchronous cards)
PRES1	32	card 1 presence contact input; active HIGH
C81	33	auxiliary I/O for ISO C8 contact for card 1 (for example, for synchronous cards)
I/O1	34	data line to/from card 1 for ISO C7 contact
INTAUX	35	auxiliary interrupt input

SYMBOL	PIN	DESCRIPTION
TEST	36	test pin; leave open-circuit in the application
I/OAUX	37	input or output for an I/O line from an auxiliary smart card interface
$\overline{CS}$	38	chip select input; active LOW
RSTOUT	39	open-drain output for resetting external chips
n.c.	40	not connected
P30/RXD	41	8xC51 general purpose I/O port/serial input port
P31/TXD	42	8xC51 general purpose I/O port/serial output port
P32/$\overline{INT0}$	43	8xC51 general purpose I/O port/external interrupt 0
P33/$\overline{INT1}$	44	8xC51 general purpose I/O port/external interrupt 1
P34/T0	45	8xC51 general purpose I/O port/Timer 0 external input
P35/T1	46	8xC51 general purpose I/O port/Timer 1 external input
P36/$\overline{WR}$	47	8xC51 general purpose I/O port/external data memory write strobe
P37/$\overline{RD}$	48	8xC51 general purpose I/O port/external data memory read strobe
XTAL2	49	connection pin for an external crystal (output from the inverting oscillator amplifier)
XTAL1	50	connection pin for an external crystal, or input for an external clock signal (input to the inverting oscillator amplifier and to the internal clock generator circuits)
V_{DDD}	51	digital power supply voltage
GNDD	52	digital ground
P20/A8	53	8xC51 general purpose I/O port/address 8
P21/A9	54	8xC51 general purpose I/O port/address 9
P22/A10	55	8xC51 general purpose I/O port/address 10
P23/A11	56	8xC51 general purpose I/O port/address 11
P24/A12	57	8xC51 general purpose I/O port/address 12
n.c.	58, 59	not connected
P25/A13	60	8xC51 general purpose I/O port/address 13
P26/A14	61	8xC51 general purpose I/O port/address 14
P27/A15	62	8xC51 general purpose I/O port/address 15
$\overline{PSEN}$	63	program store enable output: the read strobe to external program memory; when executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory; PSEN is not activated during fetches from internal program memory
ALE/$\overline{PROG}$	64	address latch enable/program pulse: output pulse for latching the lower byte of the address during an access to external memory; in normal operation, ALE is emitted at a constant rate of $\frac{1}{6}$ the oscillator frequency and can be used for external timing or clocking; one ALE pulse is skipped during each access to external data memory; this pin is also the program pulse input (PROG) during EPROM programming; ALE can be disabled by setting auxiliary special function register AUXR bit AO; with this bit set, ALE will be active only during a MOVX instruction
$\overline{EA}/V_{PP}$	65	external access enable/programming supply voltage input: must be held LOW externally to enable the device to fetch code from external program memory locations starting with 0000H; if $\overline{EA}$ is held HIGH, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (16 kbytes boundary); this pin also receives the 12.75 V programming supply voltage (V_{PP}) during EPROM programming; if security bit 1 is programmed, $\overline{EA}$ will be latched internally on reset

SYMBOL	PIN	DESCRIPTION
n.c.	66	not connected
P07/AD7	67	8xC51 general purpose I/O port/address/data 7
P06/AD6	68	8xC51 general purpose I/O port/address/data 6
P05/AD5	69	8xC51 general purpose I/O port/address/data 5
P04/AD4	70	8xC51 general purpose I/O port/address/data 4
P03/AD3	71	8xC51 general purpose I/O port/address/data 3
P02/AD2	72	8xC51 general purpose I/O port/address/data 2
P01/AD1	73	8xC51 general purpose I/O port/address/data 1
P00/AD0	74	8xC51 general purpose I/O port/address/data 0
P10/T2	75	8xC51 general purpose I/O port/Timer/Counter 2 external count input/ clock-out (clock-out is programmable)
P11/T2EX	76	8xC51 general purpose I/O port/Timer/Counter 2 reload/capture/direction control
P12	77	8xC51 general purpose I/O port
P13	78	8xC51 general purpose I/O port
P14	79	8xC51 general purpose I/O port
P15	80	8xC51 general purpose I/O port

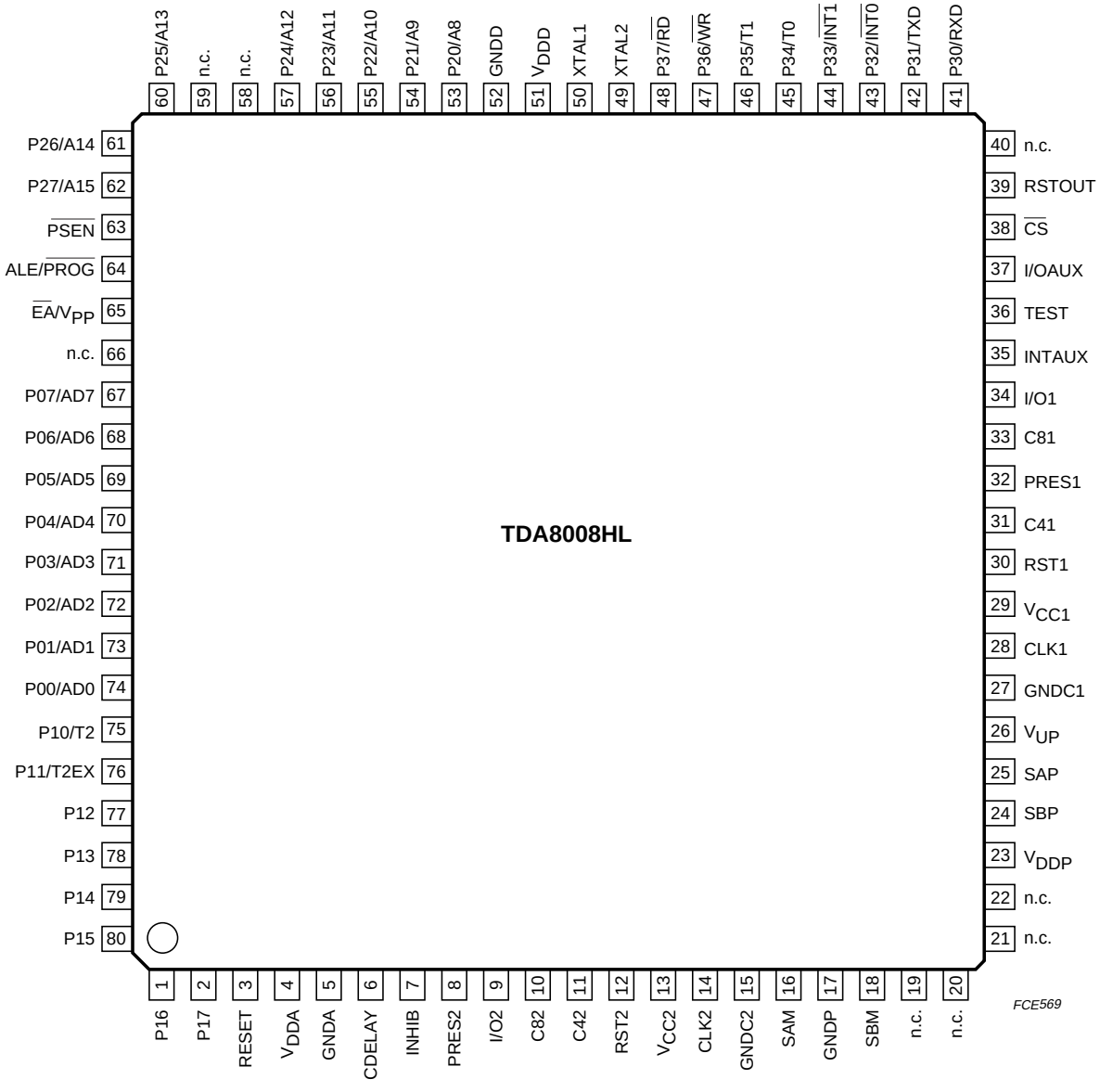


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

Throughout this specification it is assumed that the reader is aware of *"ISO 7816 norm"* terminology.

8.1 ISO 7816 UART and associated logic

In this section, the description is given of how the integrated ISO 7816 UART works, how it may be programmed by means of its control registers and how it is internally interfaced to the embedded microcontroller.

8.1.1 INTERFACE CONTROL

The ISO 7816 UART may be controlled through an 8-bit parallel bus. This bus is directly, internally connected to the Port 0 (P07 to P00) of the embedded microcontroller.

The registers inside the ISO 7816 UART may be written to or read from by using the standard 80C51 MOVX instructions (see Fig.3).

Note: the UART can be accessed only if $\overline{CS}$ is LOW.

When $\overline{CS}$ is LOW, the demultiplexing of address and data is done internally by means of the ALE signal. A low pulse on P37/$\overline{RD}$ allows reading of the selected register, a low pulse on P36/$\overline{WR}$ allows writing to the selected register.

The ISO 7816 UART interrupt line is directly, internally connected to the embedded microcontroller external interrupt 0 input P32/$\overline{INT0}$. For that reason, the external interrupt 0 of the microcontroller must be enabled to ensure a proper function.

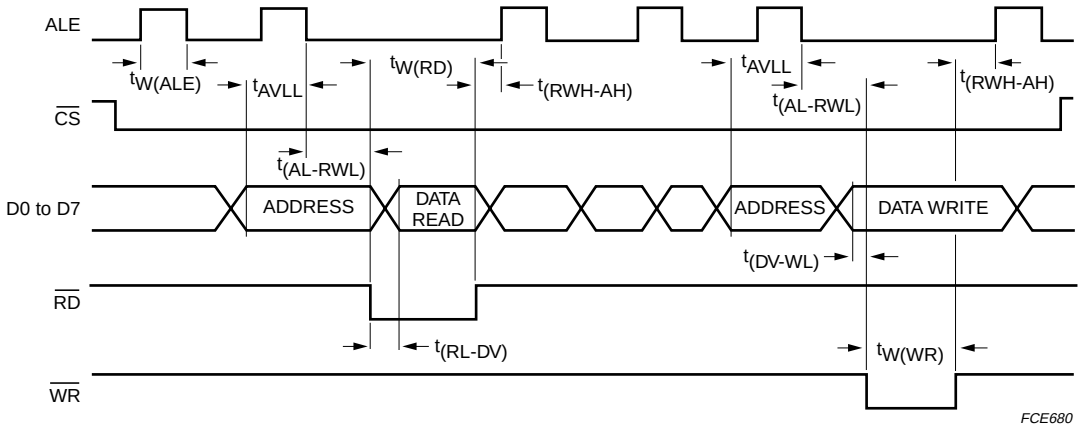


Fig.3 Control with multiplexed bus via MOVX instructions.

8.1.2 CONTROL REGISTERS

The TDA8008 has two complete analog interfaces which can drive card 1 and card 2. Data to and from the two cards share the same ISO 7816 UART. Data to and from a third card (card 3), externally interfaced with, for example, a TDA8002C or TDA8020, may also share the ISO 7816 UART. A summary of the registers is given in Fig.4

Cards 1, 2 and 3 have dedicated registers for setting the parameters of the ISO 7816 UART, namely:

- Programmable Divider Register (PDR)
- Guard Time Register (GTR)
- UART Configuration Register 1 (UCR1)
- UART Configuration Register 2 (UCR2)
- Clock Configuration Register (CCR).

Cards 1 and 2 also have dedicated registers for controlling their power and their clock configuration, namely:

- Power Control Register 1 (PCR1)
- Power Control Register 2 (PCR2).

Registers PCRx are also used for writing to or reading from the auxiliary cards contacts C4 and C8.

Power and clock controls for card 3 are performed externally.

Cards 1, 2 or 3 can be selected via the Card Select Register (CSR). When one card is selected, the corresponding parameters are used by the ISO 7816 UART. The CSR also contains one bit for resetting the ISO 7816 UART (active LOW). This bit is reset after power-on and must be set to HIGH before starting with any of the cards. It may be reset by software when necessary.

When the specific parameters of the cards have been programmed, the ISO 7816 UART may be used with the following registers:

- UART Receive Register (URR)
- UART Transmit Register (UTR)
- UART Status Register (USR)
- Mixed Status Register (MSR).

In reception mode, a FIFO of 1 to 8 characters may be used; this is configured with the FIFO Control Register (FCR). This register is also used for the automatic re-transmission of NAKed characters in transmission mode.

The Hardware Status Register (HSR) gives the status of the supply voltage, of the hardware protections and of the card movements.

Registers HSR and USR give interrupts on pin $\overline{INT0}$ when some of their bits have been changed.

Register MSR does not give interrupts and may be used in the polling mode for some operations; for this use some of the interrupt sources within the USR and HSR registers may be masked.

A 24-bit time-out counter may be started to give an interrupt after a number of ETU programmed into time-out registers TOR1, TOR2 and TOR3. This will help the embedded microcontroller in processing different real-time tasks (for example, ATR, WWT, BWT, etc.).

This counter is configured with the Time-Out counter Configuration register (TOC). The counter may be used as a 24-bit or as a 16 + 8 bits function. Each counter can be set to start counting once data has been written, or on detection of a START bit on the I/O, or as auto-reload.

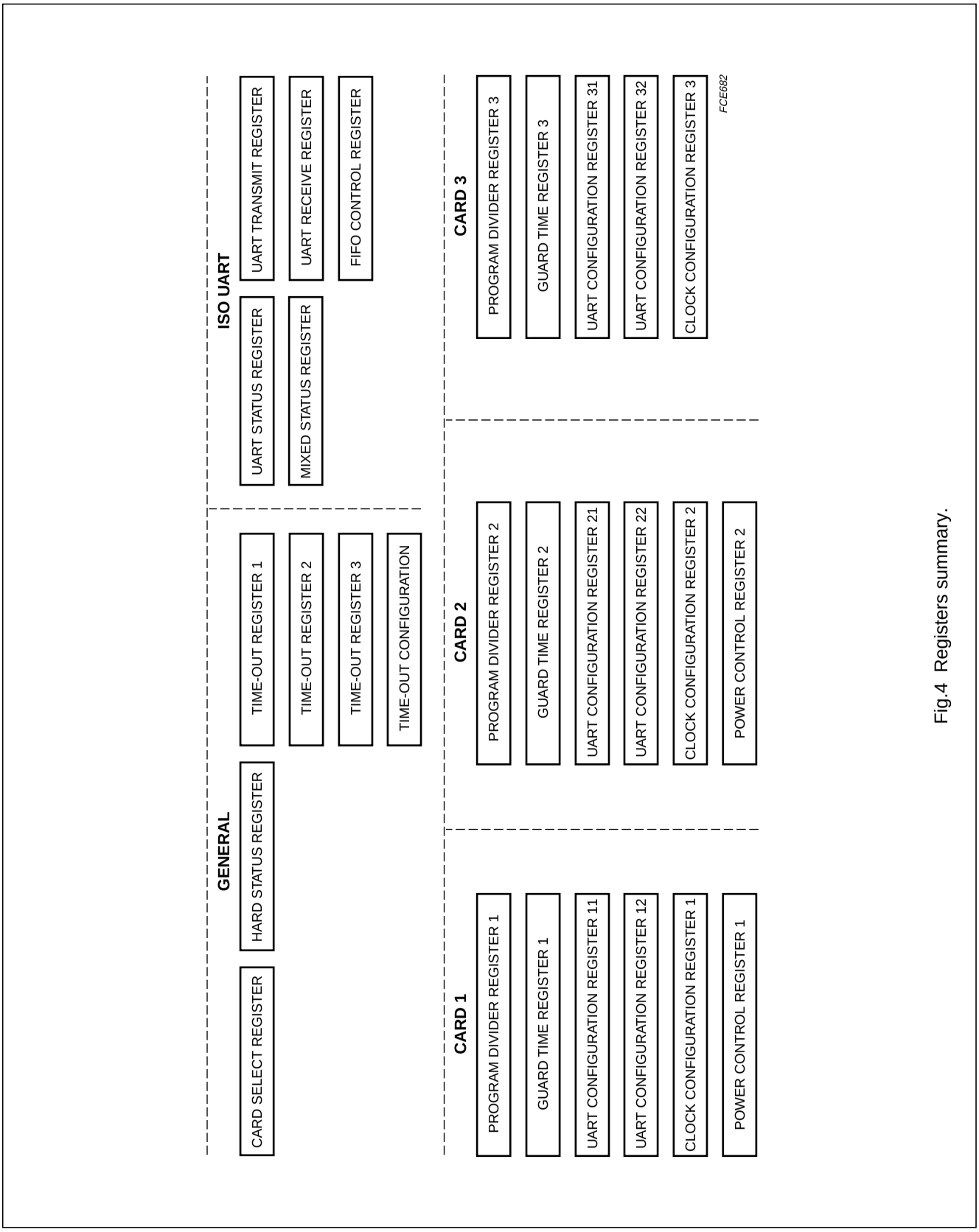


Fig.4 Registers summary.

8.1.3 General registers

8.1.3.1 Card select register

The Card Select Register (CSR) is used for selecting the card on which the ISO 7816 UART will act, and also to reset the ISO 7816 UART.

Table 1 Register CSR (address 00H; write and read); note 1

7	6	5	4	3	2	1	0
CS7	CS6	CS5	CS4	$\overline{\text{RIU}}$	SC3	SC2	SC1

Note

1. Register value at reset: all significant bits are cleared after reset, except bits CS7 to CS4 which are set to their default value.

Table 2 Description of CSR bits; note 1

BIT	SYMBOL	DESCRIPTION
7	CS7	**IC identification**. Default value: 0000.
6	CS6	
5	CS5	
4	CS4	
3	$\overline{\text{RIU}}$	**Reset ISO UART.** When reset, this bit resets a large part of the UART registers to their initial value. Bit $\overline{\text{RIU}}$ must be set to logic 1 by software before any action on the UART can take place. Bit $\overline{\text{RIU}}$ must be reset before any activation.
2	SC3	**Select card 3**. If bit SC3 = 1, then card 3 is selected.
1	SC2	**Select card 2**. If bit SC2 = 1, then card 2 is selected.
0	SC1	**Select card 1**. If bit SC1 = 1, then card 1 is selected.

Note

1. Bits SC1, SC2 and SC3 must be set one at a time. After reset, no card is selected by default.

8.1.3.2 Hardware status register

The Hardware Status Register (HSR) gives the status of the chip after a hardware problem has been detected.

Table 3 Register HSR (address 0FH; read only); note 1

7	6	5	4	3	2	1	0
HS7	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL

Note

1. Register value at reset: all significant bits are cleared after reset, except bit SUPL which is set within pulse RSTOUT.

Table 4 Description of HSR bits

BIT	SYMBOL	DESCRIPTION
7	HS7	not used
6	PRTL2	**Protection 2**. Bit PRTL2 = 1 when a fault has been detected on card reader 2. Bit PRTL 2 is the OR-function of the protection on pin V_{CC2} and pin RST2.
5	PRTL1	**Protection 1**. Bit PRTL1 = 1 when a fault has been detected on card reader 1. Bit PRTL 1 is the OR-function of the protection on pin V_{CC1} and pin RST1.
4	SUPL	**Supervisor latch**. Bit SUPL = 1 when the supervisor has been activated.
3	PRL2	**Presence latch 2**. Bit PRL2 = 1 when a level change has occurred on pin PRES2.
2	PRL1	**Presence latch 1**. Bit PRL1 = 1 when a level change has occurred on pin PRES1.
1	INTAUXL	**Auxiliary interrupt change**. Bit INTAUXL = 1 if the level on pin INTAUX has changed.
0	PTL	**Overheating**. Bit PTL = 1 if overheating has occurred.

When at least one of bits PRTL2, PRTL1, PRL2, PRL1 or PTL is HIGH, then pin INT0 is LOW. The bits having caused the interrupt are cleared when register HSR has been read-out. The same occurs with INTAUXL, if not disabled.

In case of emergency deactivation (by bits PRTL1, PRTL2, SUPL, PRL2, PRL1 or PTL), bit START (bit 0 in the PCR) is automatically reset by hardware.

At power-on, or after a supply voltage drop-out, bit SUPL is set and pin $\overline{INT0}$ is LOW. Pin $\overline{INT0}$ will return HIGH at the end of the ALARM pulse on pin RSTOUT. Bit SUPL will be reset only after a status register read-out outside the ALARM pulse (see Fig.9).

A minimum time of 2 µs is needed between two successive read operations of register HSR, as well as between the reading of register HSR and activation (write in PCR).

8.1.3.3 Time-out registers

The three Time-Out Registers (TOR1, TOR2 and TOR3) form a programmable 24-bit ETU counter, or two independant counters (one 16-bit and one 8-bit). The value to load in registers TOR1, TOR2 and TOR3 is the number of ETU to count. The time-out counters may only be used when a card is active with a running clock.

Table 5 Register TOR1 (address 09H; write only); note 1

7	6	5	4	3	2	1	0
TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0

Note

1. Register value at reset: all bits are cleared after reset.

Table 6 Register TOR2 (address 0AH; write only); note 1

7	6	5	4	3	2	1	0
TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8

Note

1. Register value at reset: all bits are cleared after reset

Table 7 Register TOR3 (address 0BH; write only); note 1

7	6	5	4	3	2	1	0
TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TOL16

Note

1. Register value at reset: all bits are cleared after reset

8.1.3.4 Time-out configuration register

The Time-Out Configuration (TOC) register is used for setting different configurations of the time-out counter as given in Table 9; all other configurations are undefined.

Table 8 Register TOC (address 08H; read and write); note 1

7	6	5	4	3	2	1	0
TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0

Note

1. Register value at reset: all bits are cleared after reset.

Table 9 Time-out counter configurations

TOC VALUE	OPERATING MODE
00H	All counters are stopped.
05H	Counters 2 and 3 are stopped; counter 1 continues to operate in auto-reload mode.
61H	Counter 1 is stopped, and counters 3 and 2 form a 16-bit counter. Counting the value stored in registers TOR3 and TOR2 is started after 61H is written in register TOC. An interrupt is given, and bit TO3 is set within register USR when the terminal count is reached. The counter is stopped by writing 00H in register TOC, and should be stopped before reloading new values in registers TOR2 and TOR3.
65H	Counter 1 is an 8-bit auto-reload counter, and counters 3 and 2 form a 16-bit counter. Counter 1 starts counting the content of register TOR1 on the first START bit (reception or transmission) detected on pin I/O after 65H is written in register TOC. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in register USR is set, and the counter automatically restarts the same count until it is stopped. It is not allowed to change the content of register TOR1 during a count. Counters 3 and 2 are wired as a single 16-bit counter and start counting the value in registers TOR3 and TOR2 when 65H is written in register TOC. When the counter reaches its terminal count, an interrupt is given and bit TO3 is set within register USR. Both counters are stopped when 00H is written in register TOC. Counters 3 and 2 shall be stopped by writing 05H in register TOC before reloading new values in registers TOR2 and TOR3.
68H	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in registers TOR3, TOR2 and TOR1 is started after 68H is written in register TOC. The counter is stopped by writing 00H in register TOC. It is not allowed to change the content of registers TOR3, TOR2 and TOR1 within a count.
71H	Counter 1 is stopped, and counters 3 and 2 form a 16-bit counter. Counting the value stored in registers TOR3 and TOR2 and is started on the first START bit detected on pin I/O (reception or transmission) after the value has been written, and then on each subsequent START bit. It is possible to change the content of registers TOR3 and TOR2 during a count; the current count will not be affected and the new count value will be taken into account at the next START bit. The counter is stopped by writing 00H in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.

TOC VALUE	OPERATING MODE
75H	Counter 1 is an 8-bit auto-reload counter, and counters 3 and 2 form a 16-bit counter. Counter 1 starts counting the content of register TOR1 on the first START bit (reception or transmission) detected on pin I/O after 75H is written in register TOC. When counter 1 reaches its terminal count, an interrupt is given, bit TO1 in register USR is set, and the counter automatically restarts the same count until it is stopped. Changing the content of register TOR1 during a count is not allowed. Counting the value stored in registers TOR3 and TOR2 is started on the first START bit detected on pin I/O (reception or transmission) after the value has been written, and then on each subsequent START bit. It is possible to change the content of registers TOR3 and TOR2 during a count; the current count will not be affected and the new count value will be taken into account at the next START bit. The counter is stopped by writing 00H in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.
7CH	Counters 3, 2 and 1 are wired as a single 24-bit counter. Counting the value stored in registers TOR3, TOR2 and TOR1 is started on the first START bit detected on pin I/O (reception or transmission) after the value has been written, and then on each subsequent START bit. It is possible to change the content of registers TOR3, TOR2 and TOR1 during a count; the current count will not be affected and the new count value will be taken into account at the next START bit. The counter is stopped by writing 00H in register TOC. In this configuration, registers TOR3, TOR2 and TOR1 must not be all zero.
85H	Same as value 05H, except that all the counters will be stopped at the end of the 12th ETU following the first received START bit detected after 85H has been written in register TOC.
E5H	Same configuration as value 65H, except that counter 1 will be stopped at the end of the 12th ETU following the first START bit detected after E5H has been written in register TOC.
F1H	Same configuration as value 71H, except that the 16-bit counter will be stopped at the end of the 12th ETU following the first START bit detected after F1H has been written in register TOC.
F5H	Same configuration as value 75H, except the two counters will be stopped at the end of the 12th ETU following the first START bit detected after F5H has been written in register TOC.

The time-out counter is very useful for processing the clock counting during ATR, the Work Waiting Time (WWT) or the waiting times defined in protocol T = 1. It should be noted that the 200 and 384 clock counter used during ATR is done by hardware when the start session is set, specific hardware controls the functionality of BGT in T = 1 and T = 0 protocols and a specific register is available for processing the extra guard time.

Writing to register TOC is not allowed as long as the card is not activated with a running clock.

Before restarting the 16-bit counter (counters 3 and 2) by writing 61H or 65H in the TOC; or the 24-bit counter (counters 3, 2 and 1) by writing 68H in the TOC; it is mandatory to stop them by writing 00H in the TOC.

Detailed examples of how to use these specific timers can be found in application note *“AN10125”*.

8.1.4 ISO 7816 UART REGISTERS

8.1.4.1 UART receive register

Table 10 Register URR (address 0DH; read only); note 1

7	6	5	4	3	2	1	0
UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0

Note

1. Register value at reset: all bits are cleared after reset.

When the microcontroller wants to read data from the card, it reads it from the UART Receive Register (URR) in direct convention:

- With a synchronous card, only D0 is relevant and this is a copy of the state of the selected card I/O
- When needed, this register may be tied to a FIFO whose length n is programmable between 1 and 8; if n > 1, no interrupt is given until the FIFO is full, then the controller may empty the FIFO when required
- When the FIFO is full, bit RBF in the status register USR is set; this bit is reset when at least one character has been read from URR
- When the FIFO is empty, bit FE is set in the status register MSR as long as no character has been received
- With a parity error:
  - In protocol T = 0; the received byte is not stored in the FIFO and the error counter is incremented. The error counter is programmable between 1 and 8. When the programmed number is reached, the bit PE is set in the status register USR and $\overline{INT0}$ falls LOW. The error counter must be reprogrammed to the desired value after its count has been reached
  - In protocol T = 1; the character is loaded in the FIFO and the bit PE is set, whatever the programmed value in parity error counter.

8.1.4.2 UART transmit register

Table 11 Register UTR (address 0DH; write only); note 1

7	6	5	4	3	2	1	0
UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0

Note

1. Register value at reset: all bits are cleared after reset.

When the microcontroller wants to transmit a character to the selected card, it writes the data in direct convention in the UART Transmit Register (UTR). The transmission:

- Starts at the end of writing (on the rising edge of signal $\overline{WR}$) if the previous character has been transmitted and if the extra guard time has expired
- Starts at the end of the extra guard time if this one has not expired
- Does not start if the transmission of the previous character is not completed
- With a synchronous card (bit SAN within register UCR2 is set), only signal D0 is relevant and is copied on pin I/O of the selected card.

8.1.4.3 Mixed status register

The Mixed Status Register (MSR) relates the status of pin INTAUX, the cards presence bits PR1 and PR2, the BGT counter, the FIFO empty indication and the transmit or receive ready indicator TBE/RBF.

Register MSR also gives useful indications when switching the clock to or from $^1/_2 f_{int}$ and for driving the ISO 7816 UART with the embedded controller.

No bits within register MSR act upon $\overline{INT0}$.

Table 12 Register MSR (address 0CH; read only); note 1

7	6	5	4	3	2	1	0
CLKSW	FE	BGT	CRED	PR2	PR1	INTAUX	TBE/RBF

Note

1. Register value at reset: bits TBE/RBF, BGT and CLKSW are cleared after reset; bits FE and CRED are set after reset.

Table 13 Description of MSR bits.

BIT	SYMBOL	DESCRIPTION
7	CLKSW	**Clock switch**. Bit CLKSW is set when the TDA8008 has performed a required clock switch from $\frac{1}{n}f_{XTAL}$ to $\frac{1}{2}f_{int}$, and is reset when the TDA8008 has performed a required clock switch from $\frac{1}{2}f_{int}$ to $\frac{1}{n}f_{XTAL}$; the application must wait until this bit is set or reset before sending a new command to the card; this bit is reset at power-on.
6	FE	**FIFO empty**. Bit FE is set when the reception FIFO is empty; it is reset when at least one character has been loaded in the FIFO.
5	BGT	**Block guard time**. In protocol T = 1, bit BGT is linked with a 22-ETU counter which is started at every START bit on pin I/O; bit BGT is set if the count is finished before the next START bit; this helps to verify that the card has not answered before 22 ETU after the last transmitted character, or that the reader is not transmitting a character before 22 ETU after the last received character. In protocol T = 0, bit BGT is linked with a 16-ETU counter which is started at every START bit on pin I/O; bit BGT is set if the count is finished before the next START bit; this helps to verify that the reader is not transmitting a character before 16 ETU after the last received character.
4	CRED	**Control ready**. The usage of bit CRED is optional; this bit may be used for driving the ISO 7816 UART with the embedded microcontroller of the TDA8008; before writing in registers TOC or UTR, or reading from register URR, check if bit CRED is set; if reset, it means that the writing or reading operation will not be correct because the controller is acting faster than the required time for this operation: • 3 clock cycles after rising edge $\overline{WR}$ for writing in register UTR: $t_{WR(UTR)} - t_{W(WR)}$ (see Fig.5) • 3 clock cycles after rising edge $\overline{RD}$ for reading from register URR: $t_{RD(URR)} - t_{W(RD)}$ (see Fig.6). • $\frac{3}{31}$ or $\frac{3}{32}$ ETU after rising edge $\overline{WR}$ for writing in register TOC: $t_{WR(TOC)} - t_{W(WR)}$ (see Fig.7). Bit CRED is set at power-on.
3	PR2	**Card 2 present**. Bit PR2 = 1 when card 2 is present.
2	PR1	**Card 1 present**. Bit PR1 = 1 when card 1 is present.
1	INTAUX	**Auxiliary interrupt**. Bit INTAUX is set when pin INTAUX = HIGH and it is reset when pin INTAUX = LOW.

BIT	SYMBOL	DESCRIPTION
0	TBE/RBF	**Transmit buffer empty/receive buffer full**. Bit TBE/RBF = 1 when: • Changing from reception mode to transmission mode • A character has been transmitted by the ISO 7816 UART • The reception FIFO is full. Bit TBE/RBF = 0 after power-on or after one of the following: • When bit $\overline{RIU}$ is reset • When a character has been written to register UTR • When at least one character has been read in the FIFO • When changing from transmission mode to reception mode.

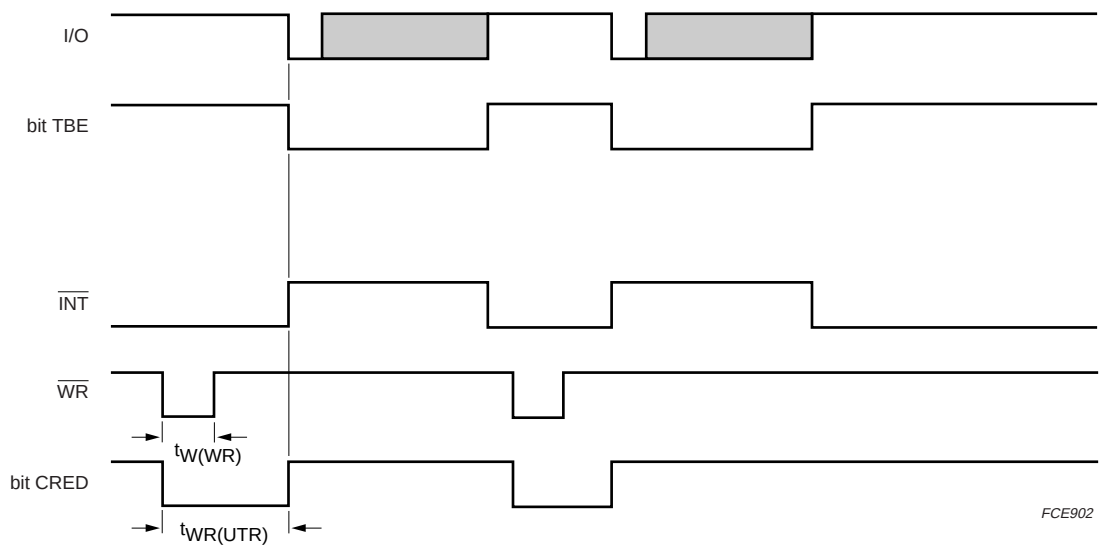


Fig.5 Minimum time between two write operations in UTR.

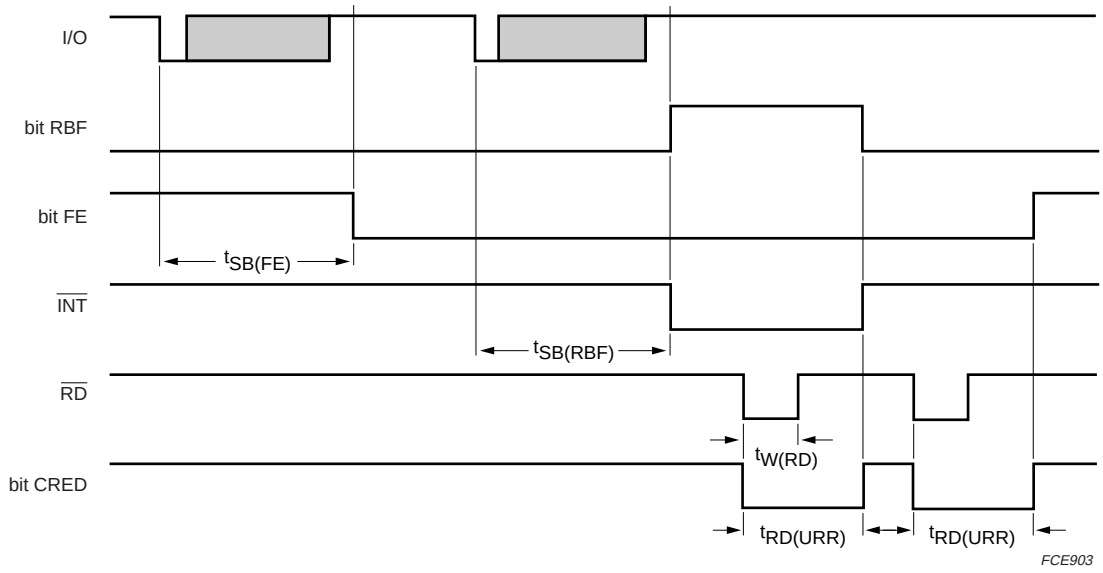


Fig.6 Minimum time between two read operations in URR.

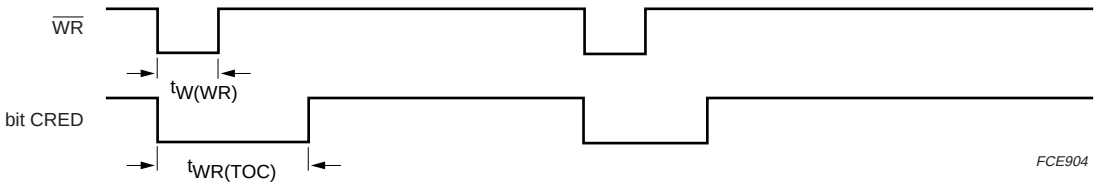


Fig.7 Minimum time between two write operations in TOC.

8.1.4.4 FIFO control register

The FIFO Control Register (FCR) relates the parity error count and the FIFO length.

Table 14 Register FCR (address 0CH; write only); note 1

7	6	5	4	3	2	1	0
FC7	PEC2	PEC1	PEC0	FC3	FL2	FL1	FL0

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 15 Description of FCR bits.

BIT	SYMBOL	DESCRIPTION
7	FC7	Not used.
6 to 4	PEC2 to 0	**Parity Error Count**. Bits PEC2, PEC1 and PEC0 determine the number of allowed repetitions in reception or in transmission before setting bit PE in register USR and pulling pin $\overline{INT0}$ to LOW level. The value 000 indicates that, if only one parity error has occurred, bit PE is set; the value 111 indicates that bit PE will be set after 8 parity errors. In protocol T = 0: • If a correct character is received before the programmed error number is reached, the error counter will be reset • If the programmed number of allowed parity errors is reached, bit PE in register USR will be set as long as register USR has not been read • If a transmitted character has been NAKed by the card, then the TDA8008 will automatically re-transmit it a number of times equal to the value programmed in bits PEC2, PEC1 and PEC0; the character will be present at 15 ETU • In transmission mode, if bits PEC2, PEC1 and PEC0 are logic 0, then the automatic re-transmission is invalidated; the character manually rewritten in register UTR will start at 13.5 ETU. In protocol T = 1: • The error counter has no action: bit PE is set at the first incorrectly received character.
3	FC3	Not used.
2 to 0	FL2 to 0	**FIFO length**. Bits FL2, FL1 and FL0 determine the depth of the FIFO: • 000 = length 1 • 111 = length 8.

8.1.4.5 UART status register

The UART Status Register (USR) is used by the embedded microcontroller to monitor the activity of the ISO 7816 UART and that of the time-out counter.

If any of the status bits FER, OVR, PE, EA, TO1, TO2 or TO3 are set then pin $\overline{INT0}$ will go LOW. The bit having caused the interrupt is reset 2 μs after the rising edge of $\overline{RD}$ during a read operation of register USR.

If bit TBE/RBF is set, and if the mask bit DISTBE/RBF within register UCR2 is not set, then pin $\overline{INT0}$ will also be LOW.

Bit TBE/RBF is reset 3 clock cycles after a data write to register UTR, or 3 clock cycles after a data read from register URR, or when changing from transmission mode to reception mode if the FIFO register had not been left full when going to transmission. In order to avoid counting these clock cycles, the bit CRED in register MSR may be used (see Table 12).

If bit LCT is used for transmitting the last character, then bit TBE is not set at the end of the transmission.

Table 16 Register USR (address 0EH; read only); note 1

7	6	5	4	3	2	1	0
TO3	TO2	TO1	EA	PE	OVR	FER	TBE/RBF

Note

1. Register value at reset: all bits are cleared after reset.

Table 17 Description of USR bits.

BIT	SYMBOL	DESCRIPTION
7	TO3	**Time-out counter 3.** Bit TO3 is set when counter 3 has reached its terminal count.
6	TO2	**Time-out counter 2.** Bit TO2 is set when counter 2 has reached its terminal count.
5	TO1	**Time-out counter 1.** Bit TO1 is set when counter 1 has reached its terminal count.
4	EA	**Early answer.** Bit EA = 1 if the first START bit on pin I/O during ATR has been detected between the first 200 and 384 clock pulses with RST LOW (all activities on pin I/O during the first 200 clock pulses with RST LOW are not taken into account) and before the first 384 clock pulses with RST HIGH. These two features are re-initialized at each toggling of RST.
3	PE	**Parity error.** In protocol T = 0, bit PE = 1 if the ISO 7816 UART has detected a number of received characters with parity errors equal to the number written in bits PEC2, PEC1 and PEC0, or if a transmitted character has been NAKed by the card a number of times equal to the value programmed in bits PEC2, PEC1 and PEC0. It is set at 10.5 ETU in the reception mode and at 11.5 ETU in the transmission mode. In protocol T = 0, a character received with a parity error is not stored in register FIFO (the card should repeat this character). In protocol T = 1, a character with a parity error is stored in the FIFO and the parity error counter is not active.
2	OVR	**Overrun.** Bit OVR = 1 if the UART has received a new character whilst register FIFO was full. In this case, at least one character has been lost.
1	FER	**Framing error.** Bit FER = 1 when pin I/O was not in the high-impedance state at 10.25 ETU after a START bit. It is reset when register USR has been read-out.

BIT	SYMBOL	DESCRIPTION
0	TBE/RBF	**Transmission buffer empty/reception buffer full.** Bits TBE and RBF share the same bit within register USR: when in transmission mode the relevant bit is TBE; when in reception mode it is RBF. Bit TBE = 1 when the ISO 7816 UART is in transmission mode and when the embedded microcontroller may write the next character to transmit in register UTR. It is reset when the embedded microcontroller has written data in the transmit register or when bit T/R within register UCR1 has been reset either automatically or by software. After detection of a parity error in transmission, it is necessary to wait 13.5 ETU before rewriting the character that has been NAKed by the card. (Manual mode, register FCR; see Table 29). Bit RBF = 1 when register FIFO is full. The embedded microcontroller may read some of the characters in register URR, which clears bit RBF.

8.1.5 CARD REGISTERS

When cards 1, 2 or 3 are selected, the following registers may be used for programming some specific parameters.

8.1.5.1 Programmable divider register

The Programmable Divider Registers (PDR1, PDR2 and PDR3) are used for counting the cards clock cycles forming the ETU (see Fig.8). These are auto-reload 8-bit counters that count from the programmed value down to 0.

Table 18 Registers PDR1, PDR2 and PDR3 (address 02H; read and write); note 1

7	6	5	4	3	2	1	0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Note

1. Register value at reset: all bits are cleared after reset.

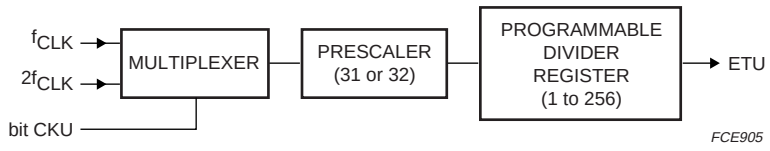


Fig.8 ETU generation.

8.1.5.2 UART configuration register 2

The UART Configuration Registers 2 (UCR12, UCR22 and UCR32) relate the UART configuration.

Table 19 Registers UCR12, UCR22 and UCR32 (address 03H; read and write); note 1

7	6	5	4	3	2	1	0
ENINT1	DISTBE/RBF	DISAUX	ENRX	SAN	$\overline{\text{AUTOCONV}}$	CKU	PSC

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 20 Description of UCR2 bits.

BIT	SYMBOL	DESCRIPTION
7	ENINT1	**Enable interrupt 1.** When not in the Power-down mode bit ENINT1 has no effect; if bit ENINT1 = 1, then a reception or a HIGH-to-LOW transition on pin $\overline{\text{INT1}}$ will wake-up the TDA8008 from the Power-down mode; in the case of reception of a character when in the Power-down mode, the start of the frame will be lost.
6	DISTBE/RBF	**Disable TBE/RBF interrupt bit**. If bit DISTBE/RBF = 1, then reception or transmission of a character will not generate an interrupt; this feature is useful for increasing communication speed with the card, in this case, a copy of bit TBE/RBF within register MSR must be polled (not the original) in order not to lose priority interrupts which can occur in register URR.
5	DISAUX	**Disable auxiliary interrupt**. If bit DISAUX in register UCR2 is set, then a change on pin INTAUX will not generate an interrupt, but bit INTAUXL will be set; it is necessary to read register HSR before bit DISAUX is to be reset to avoid an interrupt by bit INTAUXL; in order to avoid an interrupt during a change of card, it is better to set bit DISAUX in register UCR2 for all cards.
4	ENRX	**Enable reception**. When not in the Power-down mode bit ENRX has no effect; if bit ENRX = 1 then a reception or a HIGH-to-LOW transition on pin RX will wake-up the TDA8008 from the Power-down mode; in the case of reception of a character when in the Power-down mode, the start of the frame will be lost.
3	SAN	**Synchronous/asynchronous card**. Bit SAN = 1 is set by software if a synchronous card is expected; the ISO 7816 UART is then bypassed and only bit 0 in registers URR and UTR is connected to pin I/O; in this case the clock is controlled by bit SC in register CCR.
2	$\overline{\text{AUTOCONV}}$	**Auto convention**. If bit $\overline{\text{AUTOCONV}}$ = 1, then the convention is set by software using bit CONV in register UCR1; if the bit is reset, then the configuration is automatically detected on the first received character whilst the start session bit (bit SS) is set. Bit $\overline{\text{AUTOCONV}}$ must not be changed during a card session.
1	CKU	**Clock UART**. For baud rates other than those given in Table 21, there is the possibility to set bit CKU = 1; in this case the ETU will last half the number of card clock cycles equal to prescaler PDRx; bit CKU = 1 has no effect if $f_{CLK} = f_{XTAL}$, this means, for example, that 76800 baud is not possible when the card is clocked with a 3.58 MHz external frequency on pin XTAL1.
0	PSC	**PreScale Select**. If bit PSC = 1, then the prescaler value is 32; if bit PSC = 0, then the prescaler value is 31; one ETU will last a number of cards clock cycles equal to prescaler PDRx; all baud rates specified in the ISO 7816 norm are achievable with this configuration (see Table 21).

Table 21 Baud rate selection using values F and D; card clock frequency f_{CLK} = 3.58 MHz for PSC = 31 and f_{CLK} = 4.92 MHz for PSC = 32; for example, in the table '31;12' means 'prescaler set to 31 and PDR set to 12'

D	F											
	0	1	2	3	4	5	6	9	10	11	12	13
1	31;12 9600	31;12 9600	31;18 6400	31;24 4800	31;36 3200	31;48 2400	31;60 1920	32;16 9600	32;24 6400	32;32 4800	32;48 3200	32;64 2400
2	31;6 19200	31;6 19200	31;9 12800	31;12 9600	31;18 6400	31;24 4800	31;30 3840	32;8 19200	32;12 12800	32;16 9600	32;24 6400	32;32 4800
3	31;3 38400	31;3 38400		31;6 19200	31;9 12800	31;12 9600	31;15 7680	32;4 38400	32;6 25600	32;8 19200	32;12 12800	32;16 9600
4				31;3 38400		31;6 19200		32;2 76800	32;3 51300	32;4 38400	32;6 25600	32;8 19200
5						31;3 38400		32;1 153600		32;2 76800	32;3 51300	32;4 38400
6										32;1 153600		32;2 76800
8	31;1 115200	31;1 115200		31;2 57600	31;3 38400	31;4 28800	31;5 23040		32;2 76800		32;4 38400	
9							31;3 38400					

8.1.5.3 Guard time register

The Guard Time Register (GTR) is used for storing the number of guard ETU given by the card during ATR. In transmission mode, the UART will wait this number of ETU before transmitting the character stored in register UTR. In protocol T = 1, when register GTR = FF means operation at 11 ETU. In protocol T = 0, register GTRx = FF means operation at 12 ETU.

Table 22 Registers GTR1, GTR2 and GTR3 (address 05H; read and write); note 1

7	6	5	4	3	2	1	0
GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0

Note

1. Register value at reset: all bits are cleared after reset.

8.1.5.4 UART configuration register 1

The UART Configuration Register 1 (UCR) is used for setting the parameters of the ISO 7816 UART.

Table 23 Registers UCR11, UCR21 and UCR31 (address 06H; read and write); note 1

7	6	5	4	3	2	1	0
UC71	FIP	FC	PROT	T/R	LCT	SS	CONV

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 24 Description of UCR1 bits

BIT	SYMBOL	DESCRIPTION
7	UC7	not used
6	FIP	**Force inverse parity**. If bit FIP is set to logic 1, the ISO 7816 UART will NAK a correctly received character and will transmit characters with wrong parity bits.
5	FC	**Test**. Bit FC is a test bit, and must be left at logic 0.
4	PROT	**Protocol**. Bit PROT is set if the protocol is T = 1 (asynchronous) and bit PROT = 0 if the protocol is T = 0.
3	T/R	**Transmit/receive**. Bit T/R is set by software for transmission mode; a change from logic 0 to 1 will set bit TBE in register USR; bit T/R is automatically reset by hardware if bit LCT has been used before transmitting the last character.
2	LCT	**Last character to transmit**. Bit LCT is set by software before writing the last character to be transmitted in the UTR; it allows automatic change to reception mode; it is reset by hardware at the end of a successful transmission; when LCT is being reset, the bit T/R is also reset and the ISO 7816 UART is ready for receiving a character.
1	SS	**Software convention setting**. Bit SS is set by software before ATR for automatic convention detection and early answer detection; it is automatically reset by hardware at 10.5 ETU after reception of the initial character.
0	CONV	**Convention**. Bit CONV is set if the convention is direct; bit CONV is either automatically written by hardware according to the convention detected during ATR, or by software if the bit $\overline{\text{AUTOCONV}}$ in register UCR2X is set.

8.1.5.5 Clock configuration registers

The Clock Configuration Registers (CCR1, CCR2 and CCR3) relate the clock signals:

- For cards 1 and 2, register CCRx defines the clock for the selected card
- For cards 1, 2 and 3, register CCRx defines the clock to the ISO 7816 UART. If bit CKU in the prescaler register of the selected card (register UCRx2) is set, then the ISO 7816 UART is clocked at twice the frequency of the card, which allows baud rates not foreseen in the ISO 7816 norm to be reached.

Table 25 Registers CCR1, CCR2 and CCR3 (address 01H; read and write); note 1

7	6	5	4	3	2	1	0
CC7	CC6	SHL	CST	SC	AC2	AC1	AC0

Note

1. Register value at reset: all relevant bits are cleared after reset.

Table 26 Description of CCRx bits

<table>
<tr><th>BIT</th><th>SYMBOL</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td>7</td><td>CC7</td><td colspan="4">not used</td></tr>
<tr><td>6</td><td>CC6</td><td colspan="4">not used</td></tr>
<tr><td>5</td><td>SHL</td><td colspan="4">Stop HIGH or LOW. If bit CST = 1, then the clock is stopped at LOW level if bit SHL = 0, and at HIGH level if bit SHL = 1.</td></tr>
<tr><td>4</td><td>CST</td><td colspan="4">Clock stop. In the case of an asynchronous card, bit CST defines whether the clock to the card is stopped or not; if bit CST is reset, then the clock is determined by bits AC0, AC1 and AC2.</td></tr>
<tr><td>3</td><td>SC</td><td colspan="4">Synchronous clock. In the event of a synchronous card, then contact CLK is the copy of the value of bit SC; in reception mode, the data from the card is available to bit UR0 after a read operation of register URR; in transmission mode, the data is written on the I/O line of the card when register UTR has been written to and remains unchanged when another card is selected.</td></tr>
<tr><td rowspan="9">2 to 0</td><td rowspan="9">AC</td><td colspan="4">Alternating clock. All frequency changes are synchronous, thus ensuring that no spikes or unwanted pulse widths occur during changes.</td></tr>
<tr><td>AC2</td><td>AC1</td><td>AC0</td><td>CLOCK FREQUENCIES (ASYNCHRONOUS CARD)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>f_{XTAL}</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>$\frac{1}{2}f_{XTAL}$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>$\frac{1}{4}f_{XTAL}$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>$\frac{1}{8}f_{XTAL}$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td rowspan="4">$\frac{1}{2}f_{int}$</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td></tr>
</table>

Clock switching constraints:

- f_{int} is the frequency delivered by the internal oscillator
- In case of $f_{CLK} = f_{XTAL}$, the duty cycle must be ensured by the incoming clock signal on pin XTAL1
- When switching from $\frac{1}{n}f_{XTAL}$ to $\frac{1}{2}f_{int}$ or vice verse, only bit AC2 must be changed (bits AC1 and AC0 must remain the same). When switching from $\frac{1}{n}f_{XTAL}$ or $\frac{1}{2}f_{int}$ to clock stopped or vice verse, only bits CST and SHL must be changed
- When switching from $\frac{1}{n}f_{XTAL}$ to $\frac{1}{2}f_{int}$ or vice verse, a delay can occur between the command and the effective frequency change on CLK (the fastest switching time is from $\frac{1}{2}f_{XTAL}$ to $\frac{1}{2}f_{int}$ or vice verse, the best for duty cycle is from $\frac{1}{8}f_{XTAL}$ to $\frac{1}{2}f_{int}$ or vice verse)
- It is necessary to survey the bit CLKSW in register MSR before re-transmitting commands to the card.

8.1.5.6 Power control registers

The Power Control Registers (PCR1 and PCR2):

- Start or stop card sessions
- Read from or write to auxiliary card contacts C4 and C8
- Are available only for cards 1 or 2.

Table 27 Registers PCR1 and PCR2 (address 07H; read and write)

7	6	5	4	3	2	1	0
PCR7	PCR6	C8	C4	1V8	RSTIN	3V/5V	START

Register value at reset: all relevant bits are cleared after reset.

Table 28 Description of PCRx bits

BIT	SYMBOL	DESCRIPTION
7	PCR7	not used
6	PCR6	not used
5	C8	**Contact 8**. When writing to register PCR, pin C8 will output the value of bit C8; when reading from register PCR, bit C8 will store the value on pin C8.
4	C4	**Contact 4**. When writing to register PCR, pin C4 will output the value of bit C4; when reading from register PCR, bit C4 will store the value on pin C4.
3	1V8	**1.8 V cards**. If bit 1V8 is set, then V_{CC} = 1.8 V; no specification is guaranteed with this V_{CC} level when the supply voltage V_{DD} is inferior to 3 V.
2	RSTIN	**Reset bit**. When the card is activated, pin RST is the copy of the value written in bit RSTIN.
1	3V/5V	**3 or 5 V cards**. If bit 3V/5V = 1, then V_{CC} = 3 V; if bit 3V/5V = 0, then V_{CC} = 5 V.
0	START	**Start**. If the embedded microcontroller sets bit START = 1, then the selected card is activated (see Section 8.7); if the embedded microcontroller resets bit START = 0, then the card is deactivated (see Section 8.8); bit START is automatically reset in case of emergency deactivation.

8.1.5.7 Register Summary

Table 29 Register summary

ADDR	NAME	R/W	7	6	5	4	3	2	1	0	VALUE AT RESET	VALUE(1) WHEN $\overline{RIU}$ = 0
00	CSR	R/W	0	0	0	0	$\overline{RIU}$	SC3	SC2	SC1	0010 0000	0000 uuuu
01	CCR(2)	R/W	not used	not used	SHL	CST	SC	AC2	AC1	AC0	XX00 0000	XXuu uuuu
02	PDR(2)	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	0000 0000	uuuu uuuu
03	UCR2(2)	R/W	ENINT1	DISTBE/ RBF	DISAUX	ENRX	SAN	$\overline{AUTOCONV}$	CKU	PSC	0000 0000	uuuu uuuu
05	GTR(2)	R/W	GT7	GT6	GT5	GT4	GT3	GT2	GT1	GT0	0000 0000	uuuu uuuu
06	UCR1(2)	R/W	not used	FIP	FC	PROT	T/R	LCT	SS	CONV	X000 0000	Xuuu 00uu
07	PCR(2)	R/W	not used	not used	C8	C4	1V8	RSTIN	3V/5V	START	XX11 0000	XXuu uuuu
08	TOC	R/W	TOC7	TOC6	TOC5	TOC4	TOC3	TOC2	TOC1	TOC0	0000 0000	0000 0000
09	TOR1	W	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0	0000 0000	uuuu uuuu
0A	TOR2	W	TOL15	TOL14	TOL13	TOL12	TOL11	TOL10	TOL9	TOL8	0000 0000	uuuu uuuu
0B	TOR3	W	TOL23	TOL22	TOL21	TOL20	TOL19	TOL18	TOL17	TVOL16	0000 0000	uuuu uuuu
0C	FCR	W	not used	PEC2	PEC1	PEC0	not used	FL2	FL1	FL0	X000 X000	Xuuu Xuuu
0C	MSR	R	CLKSW	FE	BGT	CRED	PR2	PR1	INTAUX	TBE/RBF	0101 XXX0	u1u1 uuu0
0D	URR	R	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0	0000 0000	0000 0000
0D	UTR	W	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0	0000 0000	0000 0000
0E	USR	R	TO3	TO2	TO1	EA	PE	OVR	FER	TBE/RBF	0000 0000	0000 0000
0F	HSR	R	not used	PRTL2	PRTL1	SUPL	PRL2	PRL1	INTAUXL	PTL	X001 0000	Xuuu uuuu

Notes

1. X = undefined; u = no change.
2. PDR, GTR, UCR1, UCR2, CCR and PCR vary according to the card selected.

8.2 Supply and reset

The TDA8008 operates within a supply voltage range of 2.7 to 6 V. The supply pins are V_{DDD}, V_{DDA}, V_{DDP}, GNDP, GNDD and GNDA.

Pins V_{DDA} and GNDA supply the analog drivers to the cards and have to be decoupled externally because of the large current spikes that the cards and the step-up converter can create. V_{DDA} may be different from V_{DDD}.

The step-up converter is supplied via pins V_{DDP} and GNDP, and the rest of the chip is supplied via pins V_{DDD} and GNDD. An integrated spike killer ensures that the contacts to the cards remain inactive during power-up and power-down.

An internal voltage reference is generated for use within the step-up converter, the voltage supervisor and the V_{CC} generators.

The voltage supervisor generates an ALARM pulse when V_{DDA} is too low to ensure proper operation. The pulse length is defined by an external capacitor tied to pin CDELAY and is typically 1 ms per 2 nF. The ALARM pulse may be used as a reset pulse by the embedded microcontroller (pin RSTOUT = HIGH). It also can be used when V_{DDA} is too low to ensure proper operation can be used to block any spurious noise on card contacts during the embedded microcontroller reset, or to force an automatic deactivation of the contacts in the event of a supply drop-out (see Sections 8.7 and 8.8).

A HIGH-level on pin RESET may also be used to reset the whole chip as power-on is detected.

After power-on, or after a voltage drop, bit SUPL is set within register HSR and remains set until HSR is read-out outside the ALARM pulse. Signal $\overline{INT0}$ is LOW for the duration that RSTOUT is active.

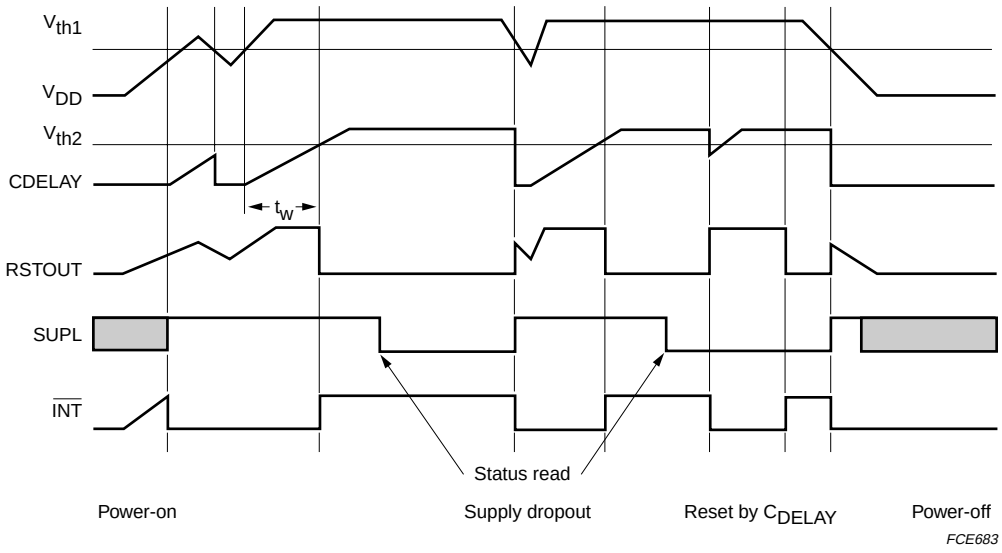


Fig.9 Voltage supervisor.

8.3 Step-up converter

Except for the V_{CC} generator and the other cards contact buffers, the whole circuit is powered by V_{DD} and V_{DDA}. If the supply voltage is 2.7 V, then a higher voltage is needed for the ISO contacts supply. When a card session is requested by the embedded microcontroller, the sequencer first enables the step-up converter (a switched capacitors type) which is clocked by an internal oscillator at a frequency of approximately 2.5 MHz.

Supposing that V_{CC} is the maximum of V_{CC1} and V_{CC2}, then the possible situations are:

- V_{CC} = 3 V
  - For V_{DD} = 3 V the step-up converter acts as a voltage doubler with regulation of V_{UP} at approximately 4.0 V
  - For V_{DD} = 5 V the step-up converter acts as a voltage follower and V_{DD} is applied to V_{UP}.
- V_{CC} = 5 V
  - For V_{DD} = 3 V the step-up converter acts as a voltage tripler with regulation of V_{UP} at approximately 5.5 V
  - For V_{DD} = 5 V the step-up converter acts as a voltage doubler with regulation of V_{UP} at approximately 5.5 V.
- V_{CC} = 1.8 V
  - The step-up converter acts as a voltage follower for any value of V_{DD}.

The recognition of the supply voltage is done by the TDA8008 at approximately 3.5 V.

Output voltage V_{UP} is fed to the V_{CC} generators. V_{CC} and GNDC are used as a reference for all other card contacts.

8.4 ISO 7816 security

The correct sequence during activation and deactivation of the cards is ensured by two specific sequencers, the clock is defined by a division ratio of the internal oscillator.

Activation (registers PCR1 or PCR2, bit START = HIGH) is only possible if the card is present (pin PRES is active HIGH with an internal current source to V_{DD}) and if the supply voltage is correct (voltage supervisor not active).

The presence of the cards is signalled to the embedded microcontroller by register HSR. Bits PR1 or PR2 (in register MSR) are set if card 1 or card 2 is present. Bits PRL1 or PRL2 are set if PRES1 or PRES2 have toggled.

During a session, the sequencer performs an automatic emergency deactivation on one card in the event of card take-off, or short-circuit. Both cards are automatically deactivated in the event of a supply voltage drop or overheating. Register HSR is updated and the $\overline{INT0}$ line falls, so that the embedded microcontroller is aware of what happened.

8.5 Power reduction modes

In addition to the standard 80C51 power reduction features, the TDA8008 has several power reduction modes that allow it to be used in portable equipment and to help in protecting the environment:

- Power-down mode
  - The device is in the Power-down mode and the card is deactivated; the bias currents in the chip and the frequency of the internal oscillator are reduced. In this mode, the consumption is less than 350 μA.
- Sleep mode
  - The embedded microcontroller is in the Power-down mode, the cards are activated but with the clock stopped HIGH or LOW; in this case, the cards should draw less than 3 mA from V_{CC}.

When in Power-down or Sleep mode, the following events will wake-up the chip:

- Card extraction or insertion
- Overcurrent on V_{CC}
- RST or RESET pin active HIGH.

The same occurs in case of a falling edge on pin RX if bit ENRX is set, or on pin $\overline{INT1}$ if bit ENINT1 is set and if interrupt INT1 is enabled within the 80C51.

If wake-up of the TDA8008 is only by INT1, then $\overline{INT1}$ must be enabled in the 80C51, and only ENINT1 should be set.

If RX should wake-up the TDA8008, then $\overline{INT1}$ must be enabled in the 80C51, and ENRX and ENINT1 should be set. Following a wake-up by RX, the first received characters may be lost; this depends on the baud rate of the serial link and is due to the 80C51 waiting for 1536 XTAL cycles before leaving Power-down mode.

For more details about the use of these modes, please refer to application note *“AN10124”*.

8.6 Protection and limitation

The TDA8008 has the following protection and limitation features:

- I_{CC} is limited to 100 mA, the card is deactivated when this limit is reached
- Current to and from pin RST is limited to 20 mA, the card is deactivated when this limit is reached
- The IC is deactivated if the temperature of the die exceeds 150 °C
- Current to and from pin I/O is limited to 10 mA
- Current to and from pin CLK is limited to 70 mA
- ESD protection on all cards contacts plus PRES is 6 kV (minimum); therefore, no need of extra components for protecting against ESD flash caused by a charged card being introduced in the slot
- Short-circuit between any card contacts can last any duration without damage.

8.7 Activation sequence

When the cards are inactive, pins V_{CC}, CLK, RST, C4, C8 and I/O are LOW and have low-impedance with respect to GNDC. The step-up converter is stopped.

When everything is satisfactory (voltage supply, card present and no hardware problems), the embedded microcontroller may initiate an activation sequence of a present card.

After selecting the card and leaving the UART reset mode ($\overline{RIU}$ = 1), and then configuring the necessary parameters for the counters and the UART, bit START may be set within register PCR at time t_0 (see Fig.10):

1. The step-up converter is started (time t_1); if one card was already active, then the step-up converter was already on and nothing more occurs at this step.
2. V_{CC} starts rising (time t_2) from 0 to 3 or 5 V with a controlled rise time of 0.17 V/µs (typical).
3. Pin I/O rises to V_{CC} (time t_3); pins C4 and C8 also rise if bits C4 and C8 within register PCR have been set to logic 1 (integrated 10kΩ pull-up resistors to V_{CC}).
4. Clock pulse CLK is sent to the card and pin RST is enabled (time t4).

After a number of clock pulses that can be counted with the time-out counter, the bit RSTIN within register PCR may be set by software: then, pin RST rises to V_{CC}.

The sequencer is clocked by $\frac{1}{64}f_{int}$ which leads to a time interval t = 25 µs (typical).

Thus:

t_1 = 0 to $\frac{1}{64}t$

$t_2 = t_1 + \frac{3}{2}t$

$t_3 = t_1 + \frac{7}{2}t$

$t_4 = t_1 + 4t$.

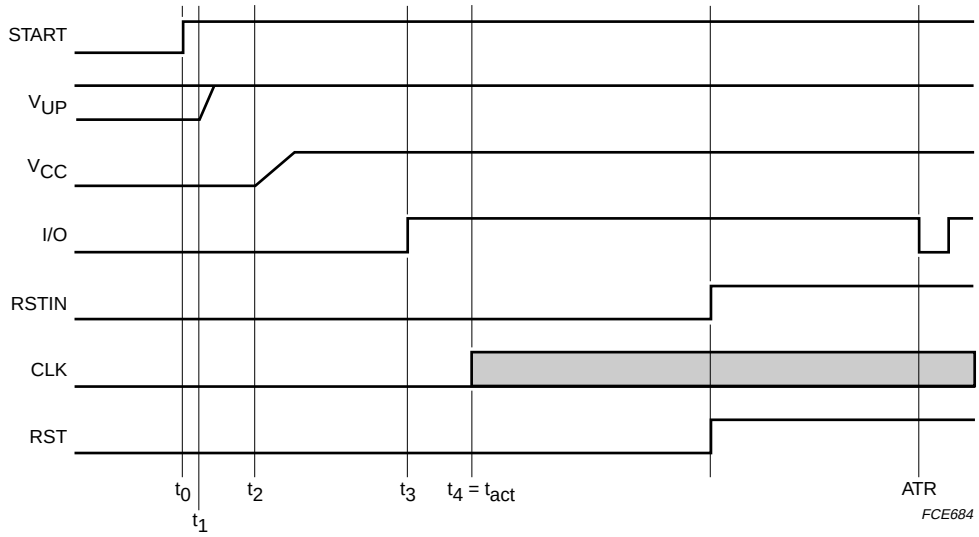


Fig.10 Activation sequence.

8.8 Deactivation sequence

When the session is completed, the embedded microcontroller resets the bit START within register PCR at time t_{10} (see Fig.11). The circuit then executes an automatic deactivation sequence.

1. The card is reset by signal RST = LOW (t_{11}).
2. Clock pulse CLK is stopped (t_{12}).
3. Pins I/O, C4 and C8 fall to 0 V (t_{13}).
4. V_{CC} falls to 0 V with typical 0.17 V/µs slew rate (t_{14}).
5. The step-up converter is stopped (t_{15}) and pins CLK, RST, V_{CC} and I/O become low-impedance to GNDC, if both cards are inactive.

Thus:

$t_{11} = t_{10} + 1/64t$

$t_{12} = t_{11} + 1/2t$

$t_{13} = t_{11} + t$

$t_{14} = t_{11} + 3/2t$

$t_{15} = t_{11} + 7/2t$

t_{de} = time that V_{CC} needs to decrease to less than 0.4 V.

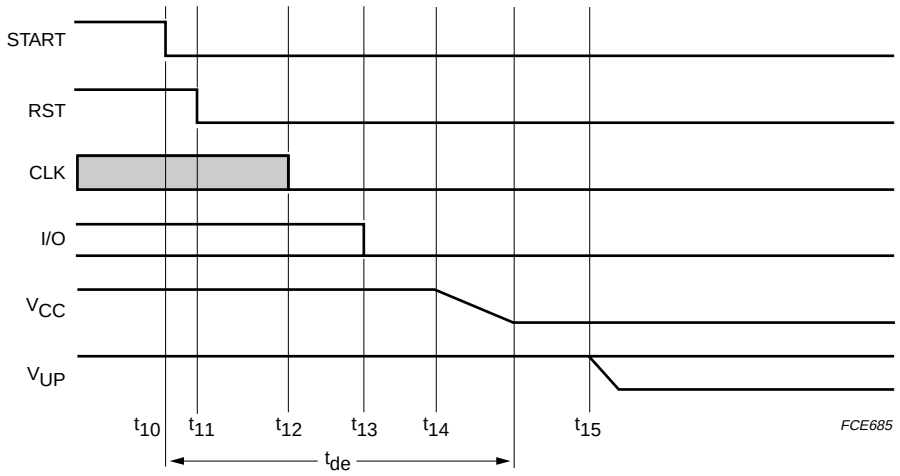


Fig.11 Deactivation sequence.

8.9 Embedded microcontroller

The microcontroller core inside the TDA8008 is like a standard ’C51 microcontroller and has the same instruction set as the 80C51.

Features added to the 80C51 microcontroller are similar to those of the 8xC51RB+ microcontroller. For further information refer to the published specifications for 8-bit, C51+ microcontrollers at *“http://www.semiconductors.philips.com/catalog/”*.

The embedded microcontroller has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source four priority level nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits. For systems that require extra memory capability, it can be expanded up to 64 kbytes using standard TTL-compatible memories and logic.

Features include:

- 80C51 central processing unit
- Full static operation
- Security bits: OTP 3 bits
- Encryption array of 64 bytes
- RAM expandible up to 64 kbytes
- Four level priority structure
- Six interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART with framing error detection and automatic address recognition
- Power control modes (clock can be stopped and resumed/Idle mode/Power-down mode)
- Wake-up from power-down by falling edge on $\overline{INT0}$, $\overline{INT1}$ and RX with an embedded delay counter
- Programmable clock output
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE).

Table 30 gives a list of main features to emphasise the differences between a standard 80C51, an 8xC51RB+ and the embedded microcontroller in the TDA8008.

Table 30 Principal blocks in 80C51, 8xC51RB+ and TDA8008

FEATURE	80C51	8xC51RB+	TDA8008
ROM/EPROM	4 kbytes	16 kbytes	16 kbytes
RAM	128 bytes	256 bytes	256 bytes
ERAM (MOVX)	no	256 bytes	512 bytes
PCA	no	yes	no
WDT	no	yes	no
Timer T0	yes	yes	yes
Timer T1	yes	yes	yes
Timer T2	no	yes	yes
		(lowest interrupt priority-vector at 002BH)	
4-level priority interrupt	no	yes	yes
Enhanced UART	no	yes	yes
Programmable clock-out	no	yes	yes
Delay counter	no	no	yes

Table 31 Embedded ’C51 microcontroller special function registers

SYMBOL	DESCRIPTION	REG ADDR	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE(1)
ACC(2)	accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
AUXR(3)	auxiliary	8EH	–	–	–	–	–	–	EXTRAM	AO	xxxxxx00B
AUXR1(3)	auxiliary	A2H	–	–	–	LPEP(4)	GF	0	–	DPS	xxx000x0B
B(2)	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPH	data pointer high	83H									00H
DPL	data pointer low	82H									00H
IE(2)	interrupt enable	A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
			AF	AE	AD	AC	AB	AA	A9	A8	
IP(2)	interrupt priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IPH(3)	interrupt priority high	B7H	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	xx000000B
P0(2)	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			87	86	85	84	83	82	81	80	
P1(2)	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			97	96	95	94	93	92	91	90	
P2(2)	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P3(2)	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TXD	RXD	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
PCON(3)(5)	power control	87H	SMOD1	SMOD0	–	POF(6)	GF1	GF0	PD	IDL	00xx0000B
SPW(2)	program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	000000x0B
			D7	D6	D5	D4	D3	D2	D1	D0	
RACAP2H(3)	Timer 2 capture high	CBH									00H
RACAP2L(3)	Timer 2 capture low	CAH									00H
SADDR(3)	slave address	A9H									00H
SADEN(3)	slave address mask	B9H									00H
SBUF	serial data buffer	99H									xxH
SCON(2)	serial control	98H	SM0/FER	SM1	SM2	REN	TB8	RB8	TI	RI	00H
			9F	9E	9D	9C	9B	9A	99	98	

SYMBOL	DESCRIPTION	REG ADDR	BIT ADDRESS, SYMBOL OR ALTERNATIVE PORT FUNCTION								RESET VALUE(1)
SP	stack pointer	81H									07H
TCON(2)	timer control	88H	TF1	TR1	TF0	TE0	IE1	IT1	IE0	IT0	00H
			8F	8E	8D	8C	8B	8A	89	88	
T2CON(2)	Timer 2 control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2MOD(3)	Timer 2 mode control	C9H	–	–	–	–	–	–	T2OE	DCEN	xxxxxx00B
TH0	Timer high 0	8CH									00H
TH1	Timer high 1	8DH									00H
TH2(3)	Timer high 2	CDH									00H
TL0	Timer low 0	8AH									00H
TL1	Timer low 1	8BH									00H
TL2(3)	Timer low 2	CCH									00H
TMOD	Timer mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H

Notes

1. x = undefined.
2. SFRs are bit-addressable.
3. SFRs are modified from, or added to, the 80C51 SFRs.
4. LPEP = low power OTP.
5. Reset value depends on reset source.
6. Bit will not be affected by reset.

8.9.1 PORT CHARACTERISTICS

8.9.1.1 Port 0

Port 0 (P07 to P00) is an open-drain, bidirectional I/O port. Port 0 pins that have logic 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting logic 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EPROM programming. External pull-ups are required during program verification.

8.9.1.2 Port 1

Port 1 (P17 to P10) is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are pulled LOW externally will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during program memory verification.

Alternative functions for Port 1 include:

T2 (P10): Timer/Counter 2 external count input/clock-out (see Section 8.9.7)

T2EX (P11): Timer/Counter 2 reload/capture/direction control.

8.9.1.3 Port 2

Port 2 (P27 to P20) is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are being pulled LOW externally will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX at DPTR). In this application it uses strong internal pull-ups when emitting logic 1s. During accesses to external data memory that use 8-bit addresses (MOV at Ri), Port 2 emits the contents of the P2 special function register. Some Port 2 pins receive the high-order address bits during EPROM programming and verification.

8.9.1.4 Port 3

Port 3 (P37 to P33, P31, P30) is a 7-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have logic 1s written to them are pulled HIGH by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are being pulled LOW externally will source current because of the pull-ups.

Port 3 also serves the following special features of the 80C51 family:

RXD (P30): serial input port

TXD (P31): serial output port

$\overline{\text{INT0}}$ (P32): external interrupt 0

$\overline{\text{INT1}}$ (P33): external interrupt 1

T0 (P34): Timer 0 external input

T1 (P35): Timer 1external input

$\overline{\text{WR}}$ (P36): external data memory write strobe

$\overline{\text{RD}}$ (P37): external data memory read strobe.

8.9.2 OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are, respectively, the input and output of an inverting amplifier. The pins can be configured for use as an on-chip oscillator. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum HIGH and LOW times specified in the data sheet must be observed.

8.9.3 RESET

A reset is accomplished by holding the RESET pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. To ensure a good Power-on reset, the RESET pin must be HIGH long enough to allow the oscillator time to start-up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on pins V_{DDD}, V_{DDA}, V_{DDP} and RESET must come up at the same time for a proper start-up. Ports 1, 2 and 3 will be driven to their reset condition asynchronously when a voltage above V_{IH1} (min.) is applied to RESET.

8.9.4 LOW POWER MODES

8.9.4.1 Stop clock mode

The static design enables the clock speed to be reduced down to 0 MHz (stopped). When the oscillator is stopped, the RAM and special function registers retain their values. This mode allows step-by-step utilization and permits reduced system Power consumption by lowering the clock frequency down to any value. For lowest power consumption the power-down mode is suggested.

8.9.4.2 Idle mode

In the Idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the Idle mode is the last instruction executed in the normal operating mode before the Idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the microcontroller in the same manner as a Power-on reset.

8.9.4.3 Power-down mode

To save even more power, a Power-down mode can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked power-down is the last instruction executed.

A hardware reset, an external interrupt or a signal received on pin RX can be used to exit from power-down. RESET redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

With $\overline{INT0}$, $\overline{INT1}$ or RX, the corresponding bits in the interrupt enable register must be enabled. Within the $\overline{INT0}$ interrupt service routine, the microcontroller must read the hardware status register (address 0FH) and/or the UART status register (address 0EH) by means of MOVX instructions in order to determine the cause of the interrupt and to reset the interrupt source.

For enabling a wake-up using $\overline{INT1}$, the bit ENINT1 within register UCR2 must be set.

For enabling a wake-up using RX, the bits ENINT1 and ENRX within register UCR2 must be set.

An integrated delay counter holds $\overline{INT0}$ and $\overline{INT1}$ LOW long enough to allow the oscillator to restart properly, so a falling edge on pins RX, $\overline{INT0}$ and $\overline{INT1}$ is enough to wake-up the whole circuit.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power-down mode.

Table 32 External pin status during Idle and Power-down modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	internal	1	1	data	data	data	data
	external	1	1	floating	data	address	data
Power-down	internal	0	0	data	data	data	data
	external	0	0	floating	data	data	data

8.9.5 Low power EPROM programming

The EPROM array contains some analog circuits that are not required when V_{DDD} is less than 4 V but are required for a V_{DDD} greater than 4 V. The Low power EPROM programming bit LPEP in register AUXR, when set, will power-down these analog circuits resulting in a reduced supply current. This bit should be set ONLY for applications that operate at a V_{DDD} less than 4 V.

8.9.6 Power-off flag

The Power-Off Flag (POF) is set by on-chip circuitry when the V_{DDD} level rises from 0 to 5 V. The POF bit can be set or cleared by software allowing a user to determine if the reset is the result of a power-on or a warm start after power-down. The V_{DDD} level must remain above 3 V for the POF to remain unaffected by the V_{DDD} level.

Design consideration. When the Idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off and it can be up to two machine cycles before the internal reset algorithm takes control. In this event, on-chip hardware inhibits access to the internal RAM but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle mode should not be one that writes to a port pin or to external memory.

8.9.7 Programmable clock-out

A 50% duty cycle clock can be programmed to be output on port P10.

Port 10, besides being a regular I/O pin, has two programmable alternative functions:

- To input the external clock for Timer/Counter 2, or
- To output a 50% duty cycle clock ranging from 61 Hz to 4 MHz at a 16 MHz operating frequency.

To configure Timer/Counter 2 as a clock generator, bit C/$\overline{T2}$ in register T2CON must be cleared and bit T20E in register T2MOD must be set. Bit TR2 in register T2CON.2 must also be set to start the timer.

The clock-out frequency depends on the oscillator frequency and the reload value of Timer 2 capture registers RCAP2H and RCAP2L as shown in the equation

$$\frac{f_{OSC}}{4 \times [65536 - (RCAP2H, RCAP2L)]}$$

where (RCAP2H, RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

In the clock-out mode, Timer 2 roll-over will not generate an interrupt. This is similar to when it is used as a baud rate generator. It is possible to use Timer 2 as a baud rate generator and a clock generator simultaneously, however the baud rate and the clock-out frequency will be the same.

8.9.8 Timer 2 operation

Timer 2 is a 16-bit Timer/Counter that can operate as an event timer or an event counter, as selected by C/$\overline{T2}$ in the special function register T2CON. Timer 2 has three operating modes selected by bits in the T2CON register. The modes are capture, auto-reload (up or down counting) and baud rate generator.

Table 33 Timer 2 control register T2CON (address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 34 Description of T2CON bits

BIT	SYMBOL	FUNCTION
7	TF2	**Timer 2 overflow flag.** Bit TF2 is set by a Timer 2 overflow and must be cleared by software; TF2 will not be set when either RCLK or TCLK = 1.
6	EXF2	**Timer 2 external flag.** Bit EXF2 is set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1; when Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine; EXF2 must be cleared by software; EXF2 does not cause an interrupt in up/down counter mode (DCEN = 1).
5	RCLK	**Receive clock flag.** When set, bit RCLK causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3; RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

BIT	SYMBOL	FUNCTION
4	TCLK	**Transmit clock flag.** When set, bit TCLK causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3; TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
3	EXEN2	**Timer 2 external enable flag.** When set, bit EXEN2 allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port; EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
2	TR2	**Start/stop control for Timer 2.** Bit TR2 = 1 starts the timer.
1	C/$\overline{T2}$	**Timer or counter select (Timer 2).** C/$\overline{T2}$ = 0: internal timer $\left(\frac{f_{XTAL1}}{12}\right)$ C/$\overline{T2}$ = 1: external event counter (falling edge triggered).
0	CP/$\overline{RL2}$	**Capture/reload flag.** When set, captures will occur on negative transitions at T2EX if EXEN2 = 1; when cleared, auto-reloads will occur either with Timer 2 overflows or with negative transitions at T2EX when EXEN2 = 1; when either RCLK = 1 or TCLK = 1 this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Table 35 Timer 2 control register T2MOD (address C9H)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	T2OE	DCEN

Table 36 Description of T2MOD bits

BIT	SYMBOL	FUNCTION
7 to 2	–	not implemented, reserved for future use; note 1
1	T2OE	**Timer 2 output enable.**
0	DCEN	**Down count enable.** When bit DCEN set, this allows Timer 2 to be configured as an up/down counter.

Note

1. User software should not write logic 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. It is possible that the reset or inactive value of the new bit will be logic 0 and its active value will be logic 1. The value read from a reserved bit is indeterminate.

Table 37 Timer 2 operating modes; note 1

MODE	RCLK + TCLK	CP/$\overline{RL2}$	TR2
16-bit auto-reload	0	0	1
16-bit capture	0	1	1
Baud rate generator	1	X	1
Timer 2 OFF	X	X	0

Note

1. X = don’t care.

8.9.8.1 Auto-reload mode (up or down counter)

In the 16-bit auto-reload mode, Timer 2 can be configured as a timer or a counter (bit C/$\overline{T2}$ in register T2CON) then programmed to count up or down. The counting direction is determined by bit DCEN (down counter enable) which is located in the T2MOD register. When reset is applied, bit DCEN = 0 which means Timer 2 will default to counting up. If bit DCEN is set, Timer 2 can count up or down as determined by the value on input T2EX.

In the configuration shown in Fig.12, Timer 2 will count up automatically since bit DCEN = 0. In this mode there are two options selected by bit EXEN2 in T2CON register. If bit EXEN2 = 0, then Timer 2 counts up to 0FFFFH and sets bit TF2 (overflow flag) upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H. The values in RCAP2L and RCAP2H are preset by software means.

If bit EXEN2 = 1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

Bit DCEN = 1 enables Timer 2 to count up or down. This mode allows input T2EX to control the direction of count (see Fig.13). When a logic 1 is applied at input T2EX, Timer 2 will count up. Timer 2 will overflow at 0FFFFH and set the TF2 flag, which can then generate an interrupt, if the interrupt is enabled. This timer overflow also causes the 16-bit value in RCAP2L and RCAP2H to be reloaded into the timer registers TL2 and TH2.

When a logic 0 is applied at input T2EX this causes Timer 2 to count down. The timer will underflow when TL2 and TH2 become equal to the value stored in RCAP2L and RCAP2H. Timer 2 underflow sets the TF2 flag and causes 0FFFFH to be reloaded into the timer registers TL2 and TH2.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

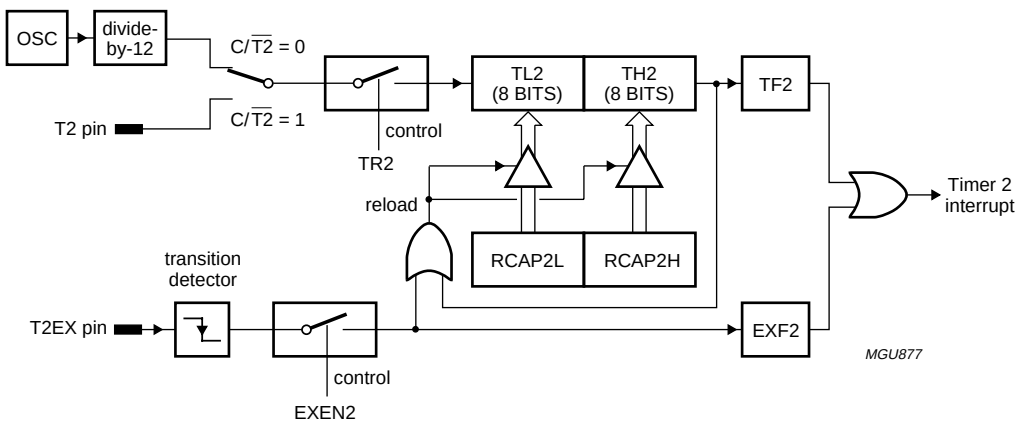


Fig.12 Timer 2 in auto-reload mode (DCEN = 0).

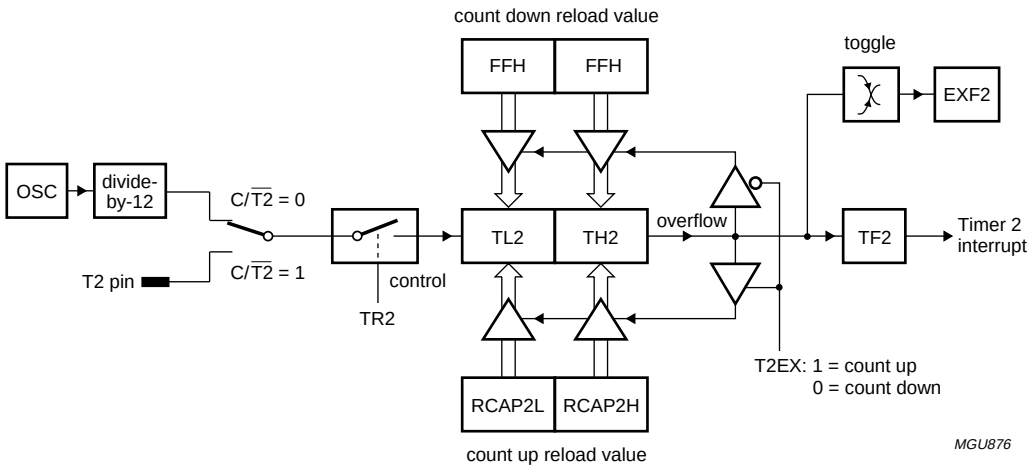


Fig.13 Timer 2 in auto-reload mode (DCEN = 1).

8.9.8.2 Capture mode

In the Capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter (as selected by C/$\overline{T2}$ in T2CON) which, upon overflowing sets the Timer 2 overflow bit TF2. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register). If EXEN2 = 1, Timer 2 operates as described above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt; the Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or $^{1}/_{12} \times f_{OSC}$ pulses.

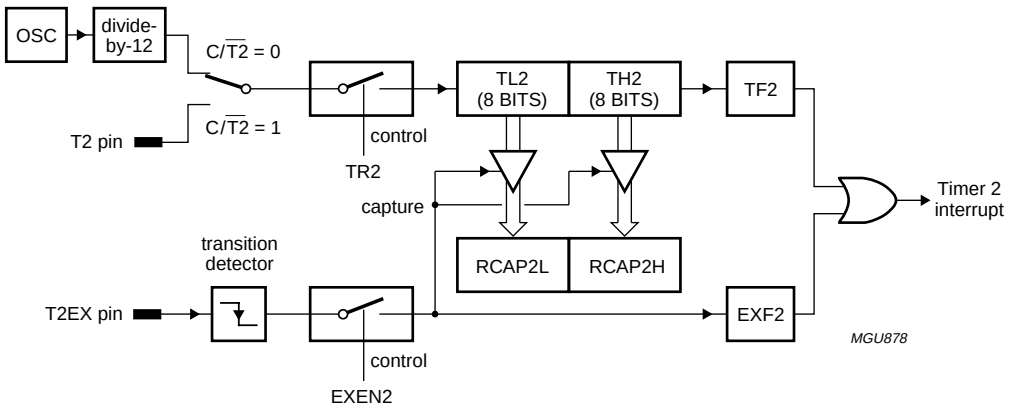
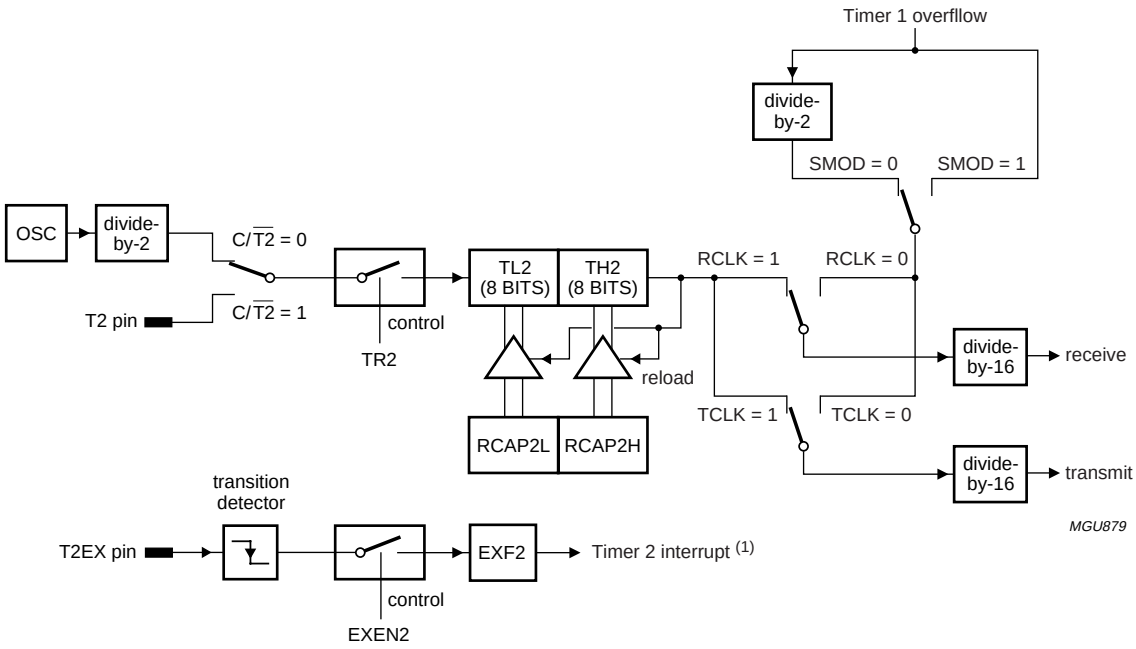


Fig.14 Timer 2 in capture mode.

8.9.8.3 Baud rate generator mode



(1) Additional external interrupt.

Fig.15 Timer 2 in Baud rate generator mode.

In the Baud rate generator mode (see Fig.15), bits TCLK and/or RCLK in register T2CON allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When bit TCLK = 0, Timer 1 is used as the serial port transmit baud rate generator; when bit TCLK = 1 it is Timer 2 that is used. Bit RCLK has the same effect for the serial port receive baud rate. With bits TCLK and RCLK the serial port can have different receive and transmit baud rates, one generated by Timer 1, the other by Timer 2.

The Baud rate generation mode is similar to the Auto-reload mode in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L (these are preset by software).

The baud rates in Auto-reload and Baud rate generation modes are related to Timer 2's overflow rate as follows:

$$\frac{\text{Timer 2 overflow rate}}{16}$$

The timer can be configured for timer or counter operation (bit C/$\overline{T2}$ in register T2CON). The operation of Timer 2 is modified when it is used as a baud rate generator.

As a timer, T2 would increment every machine cycle ($1/12 \times f_{OSC}$) but as a baud rate generator it increments every state time ($1/2 \times f_{OSC}$). Therefore the mode 1 and mode 3 baud rate formula is:

$$\frac{f_{OSC}}{32 \times [65536 - (RCAP2H, RCAP2L)]}$$

Where (RCAP2H, RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 baud rate generator mode is valid only if RCLK and/or TCLK = 1 in register T2CON.

A rollover in TH2 does not set TF2 and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/Counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Therefore when Timer 2 is in use as a baud rate generator, if needed, T2EX can be used as an additional external interrupt.

When Timer 2 is in the baud rate generator mode, no attempt should be made to read or write TH2 and TL2.

As a baud rate generator, Timer 2 is incremented every state time or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. Registers RCAP2 may be read from but should not be written to because a write may overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 38 Generated commonly-used baud rates

BAUD RATE	f_{XTAL} or f_{OSC} (MHz)	TIMER REGISTER	
		RCAP2H	RCAP2L
375000	12	FFH	FFH
9600	12	FFH	D9H
2800	12	FFH	B2H
2400	12	FFH	64H
1200	12	FEH	C8H
300	12	FBH	1EH
110	12	F2H	AFH
300	6	FDH	8FH
110	6	F9H	57H

8.9.8.4 Summary of baud rate equations

Timer 2 is in baud rate generating mode.

If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is:

$$\frac{\text{Timer 2 overflow rate}}{16}$$

If Timer 2 is being clocked internally, the baud rate is:

$$\frac{f_{OSC}}{32 \times (65536 - (RCAP2H, RCAP2L))}$$

To obtain the reload value for RCAP2H and RCAP2L, the equation can be rewritten as:

$$RCAP2H, RCAP2L = 65536 - \frac{f_{OSC}}{32 \times \text{baud rate}}$$

where f_{OSC} is the oscillator frequency.

8.9.8.5 Timer/Counter 2 set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately in order to turn the timer on; see Tables 39 and 40.

Table 39 Timer 2 as a timer

MODE	T2CON	
	INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
16-bit auto-reload	00H	08H
16-bit capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Notes

1. Capture/reload occurs only on Timer/Counter overflow.
2. Capture/reload on Timer/Counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

Table 40 Timer 2 as a counter

MODE	T2MOD	
	INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
16-bit	02H	04H
Auto-reload	03H	0BH

Notes

1. Capture/reload occurs only on Timer/Counter overflow.
2. Capture/reload on Timer/Counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

8.9.9 ENHANCED UART

The UART operates in all of the normal modes that are described in the published 8-bit, C51+ microcontroller family specifications (refer to *"http://www.semiconductors.philips.com/catalog/"*). In addition the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detection (see Fig.16), the UART looks for missing stop bits in the communication. A missing bit will set the FER bit in the SCON register. The FER bit shares bit 7 with SM0 and the bit function is determined by bit SMOD0 in register PCON; see Table 31.

If SMOD0 is set then SCON bit 7 functions as FER, or functions as SM0 when SMOD0 is cleared. When used as FER, SCON bit 7 can only be cleared by software.

Table 41 Enhanced UART modes

SM0	SM1	MODE	FUNCTION	BAUD RATE
0	0	0	shift register	$^1/_{12}f_{OSC}$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$^1/_{64}f_{XTAL1}$ or $^1/_{32}f_{XTAL1}$
1	1	3	9-bit UART	variable

Table 42 Serial port control register SCON (address 98H)

7	6	5	4	3	2	1	0
SM0/FER	SM1	SM2	REN	TB8	RB8	TI	RI

Table 43 Description of SCON bits

BIT	SYMBOL	FUNCTION
7	SM0/FER	**Serial port mode bit 0/framing error.** To access bit SM0, bit SMOD0(1) must = 0; to access bit FER, bit SMOD0 must = 1; bit FER is set by the receiver when an invalid stop bit is detected; bit FER is not cleared by valid frames but should be cleared by software.
6	SM1	**Serial port mode bit 1.**
5	SM2	**Serial port mode bit 2.** Bit SM2 enables the automatic address recognition feature in modes 2 or 3; if SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is logic 1 (indicating an address) and the received byte is a given or broadcast address; in mode 1, if SM2 = 1, then RI will not be activated unless a valid stop bit was received and the received byte is a given or broadcast address; in Mode 0, SM2 should be logic 0.
4	REN	**Receive enable.** Enables serial reception; bit REN is set by software to enable reception; clear by software to disable reception.
3	TB8	**Transmitted bit 8.** The 9th data bit that will be transmitted in Modes 2 and 3; set or clear by software as desired; in Mode 0, RB8 is not used.
2	RB8	**Received bit 8.** In modes 2 and 3, the 9th data bit that was received; in Mode 1, if SM2 = 0, RB8 is the stop bit that was received; in Mode 0, RB8 is not used.
1	TI	**Transmit interrupt flag.** Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes in any serial transmission; bit TI must be cleared by software.
0	RI	**Receive interrupt flag.** Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes in any serial reception (except see SM2); bit RI must be cleared by software.

Note

1. Bit SMOD0 is located in register PCON.

8.9.9.1 Automatic address recognition

Automatic address recognition is a feature that allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons (see Fig.17). This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. It is enabled by setting the bit SM2 in register SCON. In 9-bit UART Modes 2 and 3, the Receive Interrupt flag (RI) will be set automatically when the received byte contains either the “given” address or the “broadcast” address. The 9-bit mode requires that the 9th information bit is a logic 1 to indicate that the received information is an address and not data.

The 8-bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid STOP bit following the 8 address bits and the information is either a ‘given’ or a ‘broadcast’ address.

Mode 0 is the shift register mode and SM2 is ignored.

Using the automatic address recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the broadcast address. Special function registers are used to define the slave’s address (register SADDR) and the address mask (register SADEN). Register SADEN is used to define which bits in register SADDR are to be used and which bits are don’t care. The SADEN mask can be logically ANDed with register SADDR to create the given address which the master will use for addressing each of the slaves. Use of the given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme.

Table 44 Automatic addressing example 1

REGISTER	ADDRESS(1)
Slave 0	
SADDR	1100 0000
SADEN	1111 1101
Given address	1100 00X0
Slave 1	
SADDR	1100 0000
SADEN	1111 1110
Given address	1100 000X

Note

1. X = don’t care.

In the example shown in Table 44, SADDR is the same for both slaves and the SADEN data differentiates between them. Slave 0 requires a logic 0 in bit 0 and it ignores bit 1. Slave 1 requires a logic 0 in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a logic 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a logic 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = logic 0 for slave 0 and bit 1 = logic 0 for slave 1. Thus, both could be addressed with 1100 0000.

In a more complex system, the example shown in Table 45 could be used to select slaves 1 and 2 while excluding slave 0.

In this example, the differentiation between the three slaves is in the lower of the three address bits. Slave 0 requires that bit 0 = logic 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = logic 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = logic 0 and its unique address is 1110 0011. To select slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = logic 1 to exclude slave 2.

The broadcast address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are treated as don’t cares. In most cases, interpreting the don’t cares as logic 1s, the broadcast address will be FFH.

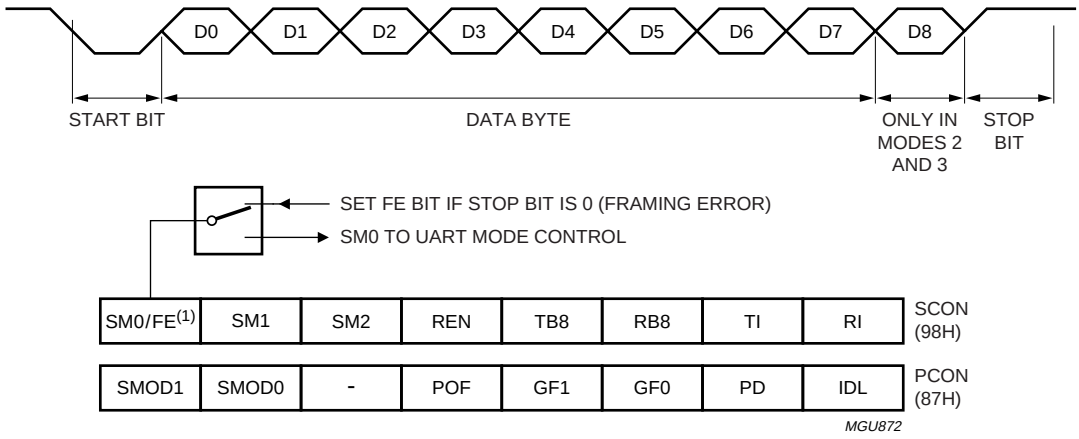
Table 45 Automatic addressing example 2

REGISTER	ADDRESS(1)
Slave 0	
SADDR	1100 0000
SADEN	1111 1001
Given address	1110 0XX0
Slave 1	
SADDR	1110 0000
SADEN	1111 1010
Given address	1110 0X0X
Slave 2	
SADDR	1110 0000
SADEN	1111 1100
Given address	1110 00XX

Note

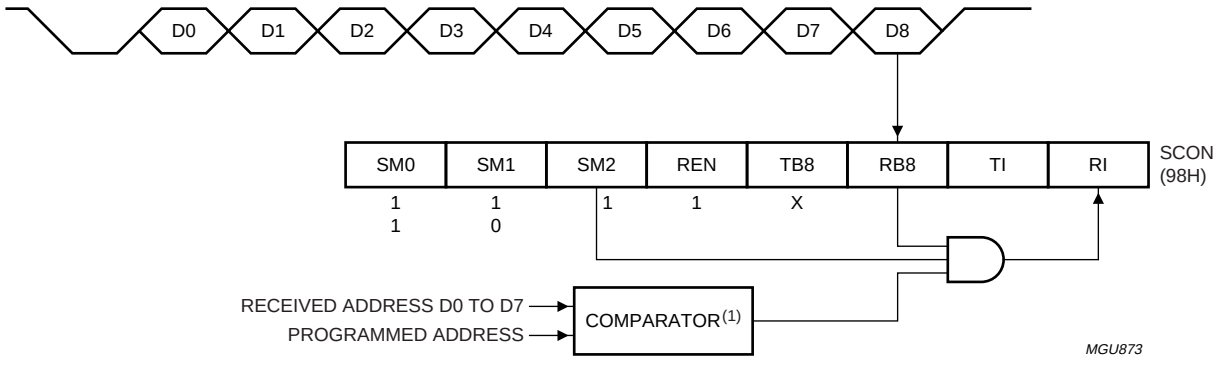
1. X = don’t care.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with logic 0s. This produces a given address of all ‘don’t cares’ as well as a broadcast address of all ‘don’t cares’. This effectively disables the automatic addressing mode and allows the microcontroller to use standard 80C51 type UART drivers that do not make use of this feature.



(1) SCON bit 7: 0 = SM0; 1 = FER.

Fig.16 UART framing error detection.



(1) In UART Mode 2 or Mode 3 and with SM2 = 1, an interrupt is generated if REN = 1, RB8 = 1 and received address = programmed address; when own address is received, clear SM2 to receive data bytes; when all data bytes have been received, set SM2 to wait for next address.

Fig.17 UART multiprocessor communication, automatic address recognition.

8.9.10 INTERRUPT PRIORITY STRUCTURE

The TDA8008 has a six-source, four-level interrupt structure. There are three special function registers associated with the four-level interrupt; registers IE, IP, and IPH. The Interrupt Priority High register (Register IPH) makes the four-level interrupt structure possible. Register IPH is located at SFR address B7H. The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt as shown in Table 46.

Table 46 Priority bits

IPH.x	IP.x	INTERRUPT PRIORITY LEVEL
0	0	level 0 (lowest priority)
0	1	level 1
1	0	level 2
1	1	level 3 (highest priority)

Table 47 Interrupt table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR	VECTOR ADDRESS
X0	1	IE0	no[1], yes[2]	03H
T0	2	TF0	yes	0BH
X1	3	IE1	no[1], yes[2]	13H
T1	4	TF1	yes	1BH
SP	5	RI, TI	no	23H
T2	6	TF2, EXF2	no	2BH

Notes

1. Level activated.
2. Transition activated.

Table 48 Interrupt enable register IE (address A8H)

7	6	5	4	3	2	1	0
EA	–	ET2	ES	ET1	EX1	ET0	EX0

Table 49 Description of IE bits (IE bit = 1 enables the interrupt; IE bit = 0 disables the interrupt)

BIT	SYMBOL	FUNCTION
7	EA	**Global disable.** If EA = 0, all interrupts are disabled; if EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
6	–	not implemented, reserved for future use; note 1
5	ET2	**Timer 2 interrupt enable.**
4	ES	**Serial port interrupt enable.**
3	ET1	**Timer 1 interrupt enable.**
2	EX1	**External interrupt 1 enable.**
1	ET0	**Timer 0 interrupt enable.**
0	EX0	**External interrupt 0 enable.**

Note

1. User software should not write logic 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. It is possible that the reset or inactive value of the new bit will be logic 0 and its active value will be logic 1. The value read from a reserved bit is indeterminate.

Table 50 Interrupt priority register IP (address B8H)

7	6	5	4	3	2	1	0
–	–	PT2	PS	PT1	PX1	PT0	PX0

Table 51 Description of IP bits (IP bit = 1 assigns high priority; IP bit = 0 assigns low priority)

BIT	SYMBOL	FUNCTION
7 and 6	–	not implemented, reserved for future use; note 1
5	PT2	**Timer 2 interrupt priority.**
4	PS	**Serial port interrupt priority.**
3	PT1	**Timer 1 interrupt priority.**
2	PX1	**External interrupt 1 priority.**
1	PT0	**Timer 0 interrupt priority.**
0	PX0	**External interrupt 0 priority.**

Note

1. User software should not write logic 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. It is possible that the reset or inactive value of the new bit will be logic 0 and its active value will be logic 1. The value read from a reserved bit is indeterminate.

Table 52 Interrupt priority high register IPH (address B7H)

7	6	5	4	3	2	1	0
–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Table 53 Description of IPH bits (IPH bit = 1 assigns higher priority; IP bit = 0 assigns lower priority)

BIT	SYMBOL	FUNCTION
7 and 6	–	not implemented, reserved for future use; note 1
5	PT2H	**Timer 2 interrupt priority high.**
4	PSH	**Serial port interrupt priority high.**
3	PT1H	**Timer 1 interrupt priority high.**
2	PX1H	**External interrupt 1 priority high.**
1	PT0H	**Timer 0 interrupt priority high.**
0	PX0H	**External interrupt 0 priority high.**

Note

1. User software should not write logic 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. It is possible that the reset or inactive value of the new bit will be logic 0 and its active value will be logic 1. The value read from a reserved bit is indeterminate.

8.9.11 Reduced EMI mode

When bit AO in register AUXR is set it disables the ALE output.

8.9.12 Dual DPTR

The dual data pointer (DPTR) structure is the means by which the TDA8008 specifies the address of an external data memory location (see Fig.18). There are two 16-bit DPTR registers that address the external memory and a single bit (register AUXR1, bit DPS) that allows the program code to switch between the DPTR registers (registers DPTR0 and DPTR1).

The status of the DPS bit should be saved by software when switching between the DPTR registers.
A user-defined flag (register AUXR1, bit GF) allows the DPS bit to be quickly toggled by executing an INC AUXR1 instruction without affecting the AUXR1 GF or LPEP bits.

Bit 2 of register AUXR1 is not writable and is always read as a logic 0.

The DPTR instructions refer to the data pointer that is currently selected using register AUXR1, bit DPS. The six DPTR instructions are described in Table 54.

The data pointer can be accessed on a byte-by-byte basis by specifying the low byte or high byte in an instruction which accesses the special function registers.

Table 54 DPTR instructions

INSTRUCTION	ACTION
INC DPTR	increments the data pointer by 1
MOV DPTR, #data16	loads the DPTR with a 16-bit constant
MOV A, at A + DPTR	move code byte relative to DPTR to ACC
MOVX A, at DPTR	move external RAM (16-bit address) to ACC
MOVX at DPTR, A	move ACC to external RAM (16-bit address)
JMP at A + DPTR	jump indirect relative to DPTR

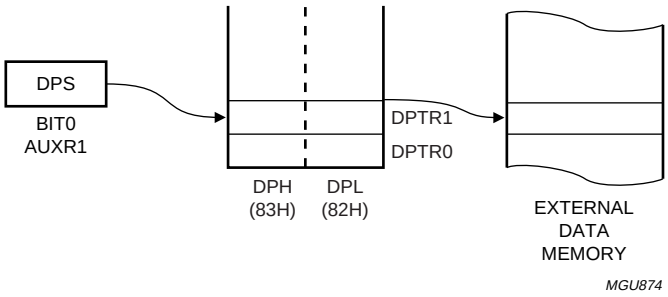


Fig.18 Dual DPTR.

8.9.13 Expanded data RAM addressing

The TDA8008 has an internal data memory that is mapped into four separate segments. These are the lower 128 bytes of RAM, the upper 128 bytes of RAM, 128 bytes from special function registers and 512 bytes of expanded RAM (EXTRAM) as shown in Fig.19.

The four segments are:

- The lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable
- The upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only
- The special function registers (addresses 80H to FFH) are directly addressable only
- The 512 bytes of EXTRAM (addresses 00H to 1FFH) are indirectly accessed by move external instruction MOVX, and with register AUXR, bit EXTRAM cleared.

The lower 128 bytes can be accessed by direct or indirect addressing. The upper 128 bytes can be accessed by indirect addressing only. The upper 128 bytes occupy the same address space as the SFR. This means they have the same address but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether to access the upper 128 bytes of data RAM or to access SFR space by the addressing mode used in the instruction.

Instructions that use direct addressing access SFR space; for example, ‘MOV A0H, #data’ accesses the SFR at location 0A0H (which is P2).

Instructions that use indirect addressing access the upper 128 bytes of data RAM; for example, ‘MOV @R0,#data’ where R0 contains 0A0H to access the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

The EXTRAM can be accessed by indirect addressing with register AUXR, bit EXTRAM cleared and with MOVX instructions. This part of the memory is physically located on-chip, and logically occupies the first 512 bytes of external data memory.

With bit EXTRAM = 0, the EXTRAM is indirectly addressed using the MOVX instruction in combination with any registers R0, R1 of the selected bank or DPTR. An access to the EXTRAM will not affect ports P0, P36 ($\overline{WR}$) and P37 ($\overline{RD}$). Port P2 (SFR) is output during external addressing. For example, with EXTRAM = 0, ‘MOVX @R0, A’ where R0 contains 0A0H, access to the EXTRAM is at address 0A0H rather than external memory. An access to external data memory locations higher than 1FFH (i.e., 0200H to FFFFH) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, that is with P0 and P2 as data/address bus, and P36 and P37 as WRITE and READ timing signals.

With bit EXTRAM = 1, instructions MOVX @Ri and MOVX @DPTR will be similar to the standard 80C51 instructions. MOVX @Ri will provide an 8-bit address multiplexed with data on Port 0 and any output port pins can be used to output higher-order address bits. This is to provide the external paging capability. MOVX @DPTR will generate a 16-bit address. Port 2 outputs the higher eight address bits (the contents of DPH) while Port 0 multiplexes the lower eight address bits (DPL) with data. MOVX @Ri and MOVX @DPTR will generate either READ or WRITE signals on P36 ($\overline{WR}$) and P37 ($\overline{RD}$).

The Stack Pointer (SP) may be located anywhere in the 256-byte RAM (lower and upper RAM) internal data memory. The stack may not be located in the EXTRAM.

Table 55 Auxiliary register AUXR (address 8EH)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	EXTRAM	AO

Table 56 Description of AUXR bits

BIT	SYMBOL	FUNCTION
7 to 2	–	not implemented, reserved for future use; note 1
1	EXTRAM	internal/external RAM access using MOVX @Ri/@DPTR EXTRAM = 0: internal ERAM (0000H-01FFH) access using MOVX @Ri/@DPTR EXTRAM = 1: external data memory access
0	AO	deactivation sequence disable/enable ALE AO = 0: ALE is emitted at a constant rate of $\frac{1}{6}$ the crystal or oscillator frequency AO = 1: ALE is active only during a MOVX or MOVC instruction

Note

1. User software should not write logic 1s to reserved bits. These bits may be used in future 8051 family products to invoke new features. It is possible that the reset or inactive value of the new bit will be logic 0 and its active value will be logic 1. The value read from a reserved bit is indeterminate.

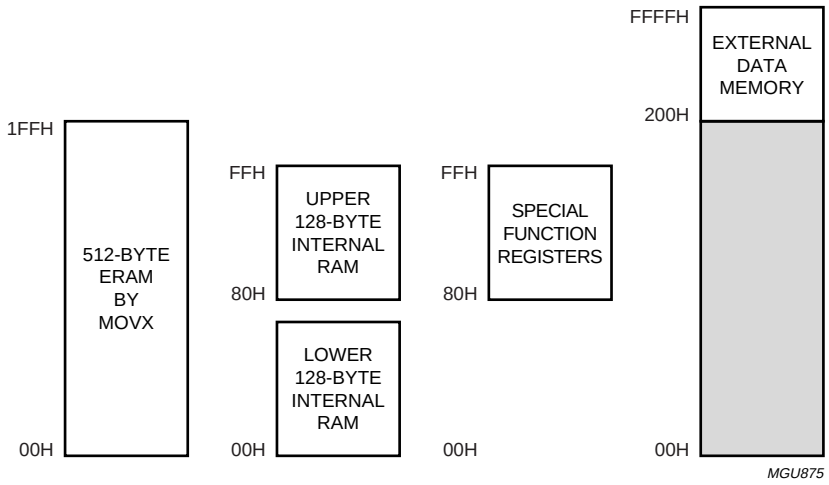


Fig.19 Internal and external data memory address space with EXTRAM = 0.

8.9.14 EPROM CHARACTERISTICS

The OTP-device TDA8008 can be programmed by using a modified Improved Quick-Pulse Programming™(1) algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/$\overline{PROG}$ pulses. If commercial programmers are used, the 87C51RB+ algorithm has to be chosen.

The TDA8008 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as being manufactured by Philips.

8.9.14.1 Quick-pulse programming

In quick-pulse programming, the device is running with a 4 to 6 MHz oscillator. The reason for the oscillator to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to Ports 1 and 2. The code byte to be programmed into that location is applied to Port 0. RST, $\overline{PSEN}$ and pins of Ports 2 and 3 are held at the 'program code data' levels. The ALE/$\overline{PROG}$ is pulsed LOW five times, each pulse is 100 μs ± 10 μs with a delay of minimum 10 μs between two programming pulses.

To program the encryption table, repeat the five-pulse programming sequence for addresses 0 through 1FH, using the 'Pgm encryption table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the security bits, repeat the five-pulse programming sequence using the 'Pgm security bit' levels. After one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bits can still be programmed.

Note that the $\overline{EA}$/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

8.9.14.2 Program verification

If security bits 2 and 3 have not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to Ports 1 and 2. The other pins are held at the 'verify code data' levels. The contents of the address location will be emitted on Port 0. External pull-ups are required on Port 0 for this operation.

If the 64-byte encryption table has been programmed, the data presented at Port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

8.9.14.3 Reading the signature bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P36 and P37 need to be pulled to a logic LOW. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = CBH indicates TDA8008

(060H) = NA.

8.9.14.4 Security bits

With none of the security bits programmed the code in the program memory can be verified. If the encryption table is programmed, the code will be encrypted when verified. When only security bit 1 is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory, $\overline{EA}$ is latched on reset and all further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled.

8.9.14.5 Encryption array

There are 64 bytes of encryption array and these are all initially unprogrammed (all at logic 1).

(1) Improved Quick-Pulse Programming is a trademark of the Intel Corporation.

8.9.14.6 EPROM programming modes

Table 57 EPROM programming

V_{PP} = 12.75 V ± 0.25 V; during programming and verification supply voltage V_{DD} = 5 V ± 10%

MODE	INPUTS FOR PROGRAMMING(1)							
	RESET	$\overline{PSEN}$	ALE/$\overline{PROG}$(2)	$\overline{EA}$/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Program encryption table	1	0	0	V_{PP}	1	0	1	0
Program security bit 1	1	0	0	V_{PP}	1	1	1	1
Program security bit 2	1	0	0	V_{PP}	1	1	0	0
Program security bit 3	1	0	0	V_{PP}	0	1	0	1

Notes

1. For each input, ‘0’ indicates valid LOW and ‘1’ indicates valid HIGH
2. ALE/$\overline{PROG}$ receives five programming pulses for code data (also for user array; five pulses for encryption or security bits) while V_{PP} is held at 12.75 V. Each programming pulse is LOW for 100 μs ± 10 μs and HIGH for a duration of 10 μs minimum.

Table 58 Security bit programming

SECURITY BITS(1)			PROGRAM PROTECTION
SB1	SB2	SB3	
U	U	U	no program security features are enabled (code verify will continue to be encrypted by the encryption array, if programmed)
P	U	U	MOVC instructions executed from external program memory are disabled by fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on RESET and further programming of the EPROM is disabled
P	P	U	MOVC instructions executed from external program memory are disabled by fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on RESET and further programming of the EPROM is disabled; code verify is disabled
P	P	P	MOVC instructions executed from external program memory are disabled by fetching code bytes from internal memory; $\overline{EA}$ is sampled and latched on RESET and further programming of the EPROM is disabled; external execution is disabled

Note

1. P = programmed; U = unprogrammed; any other combination of the security bits is not defined.

8.9.15 ROM CODE SUBMISSION FOR 16 kbyte EPROM DEVICE

When submitting ROM code for the 16 kbyte EPROM devices for TDA8008, the following must be specified:

- 16 kbyte user EPROM data
- 64 byte EPROM encryption key
- EPROM security bits.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.5	+6.5	V
V_{DDD}	digital supply voltage		–0.5	+6.5	V
V_{DDP}	supply voltage for DC-to-DC converter		–0.5	+6.5	V
V_n	input voltages on all pins except SAM, SAP, SBM, SBP and V_{UP}		–0.5	V_{DD} + 0.5	V
	voltage on pins SAM, SAP, SBM, SBP and V_{UP}		–0.5	+7.5	V
P_{tot}	continuous total power dissipation (LQFP80)	T_{amb} = –30 to +85 °C	–	650	mW
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	125	°C
V_{es}	electrostatic discharge voltage	HBM; note 1			
	on pins I/O1, V_{CC1}, RST1, CLK1, C41, C81, GNDC1, PRES1, I/O2, V_{CC2}, RST2, CLK2, C42, C82, GNDC2 and PRES2		–6	+6	kV
	on other pins except pin $\overline{EA}/V_{PP}$		–2	+2	kV
	on pin $\overline{EA}/V_{PP}$		–1	+1	kV

Note

1. Human body model as defined in JEDEC Standard JESD22-A114-B, dated June 2000.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	In free air	62	K/W

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *“Handling MOS devices”*).

12 CHARACTERISTICS

V_{DD} = 3.3 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.7	–	6.0	V
V_{DDP}	supply voltage for the DC-to-DC converter		V_{DD}	–	6.0	V
$I_{DD(pd)}$	supply current in Power-down mode	both cards inactive; XTAL oscillator stopped; note 1	–	–	500	µA
$I_{DD(sm)}$	supply current in Sleep mode	both cards powered; CLK stopped; note 1	–	–	6	mA
$I_{DD(oper)}$	supply current in operating mode	5 V card I_{CC1} = 65 mA; I_{CC2} = 15 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; V_{DD} = 2.7 V	–	–	300	mA
		3 V card I_{CC1} = 50 mA; I_{CC2} = 30 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; V_{DD} = 2.7 V	–	–	215	mA
		I_{CC1} = 50 mA; I_{CC2} = 30 mA; f_{XTAL} = 20 MHz; f_{CLK} = 10 MHz; V_{DD} = 5 V	–	–	100	mA
V_{th1}	threshold voltage on V_{DD} (falling)		2.1	–	2.35	V
V_{hys1}	hysteresis on V_{th1}		50	–	170	mV
V_{th2}	threshold voltage on pin CDELAY		–	1.3	–	V
V_{CDELAY}	voltage on pin CDELAY		–	–	V_{DD} + 0.3	V
I_{CDELAY}	output current at pin CDELAY	pin grounded (charge)	–	–3	–	µA
		V_{CDELAY} = V_{DD} (discharge)	–	2	–	mA
C_{CDELAY}	capacitance value		1	–	–	nF
$t_{W(ALARM)}$	ALARM pulse width	C_{CDELAY} = 22 nF	–	10	–	ms
External IC reset output (pin RSTOUT; open-drain active HIGH or LOW)						
I_{OH}	HIGH-level output current	active LOW option; V_{OH} = 5 V	–	–	10	µA
V_{OL}	LOW-level output voltage	active LOW option; I_{OL} = 2 mA	–0.3	–	+0.4	V
I_{OL}	LOW-level output current	active HIGH option, V_{OL} = 0 V	–	–	–10	µA
V_{OH}	HIGH-level output voltage	active HIGH option, I_{OH} = –1 mA	$0.8V_{DD}$	–	V_{DD} + 0.3	V
Crystal oscillator						
f_{XTAL}	crystal frequency		4	–	20	MHz
f_{EXT}	external frequency applied on pin XTAL1		0	–	20	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Step-up converter						
f_{int}	internal oscillator frequency		2	2.5	3	MHz
V_{VUP}	voltage on pin V_{UP}	at least one 5 V card	–	5.5	–	V
		both cards 3 V	–	5.0	–	V
$V_{det(dt)}$	detection voltage on V_{DD} for doubler/tripler selection		3.4	3.5	3.6	V
Reset output to the cards (pins RST1 and RST2)						
$V_{O(inactive)}$	output voltage (inactive)	cards inactive				
		no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{O(inactive)}$	output current (inactive)	cards inactive and pins RST grounded	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	0.1	μs
t_f	fall time	C_L = 30 pF	–	–	0.1	μs
f_{CLK}	clock frequency	1 MHz Idle mode configuration	1	–	1.85	MHz
		operational mode	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns
Clock output to the cards (pins CLK1 and CLK2)						
$V_{O(inactive)}$	output voltage (inactive)	cards inactive				
		no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{O(inactive)}$	output current (inactive)	cards inactive and pins CLK grounded	0	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 μA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 μA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF	–	–	8	ns
t_f	fall time	C_L = 30 pF	–	–	8	ns
f_{clk}	clock frequency	1 MHz Idle mode configuration	1	–	1.5	MHz
		operational	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%
SR	slew rate (rise and fall)	C_L = 30 pF	0.2	–	–	V/ns
Card supply voltage (pins V_{CC1} and V_{CC2}); note 2						
$V_{O(inactive)}$	output voltage (inactive)	cards inactive mode				
		no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	0	–	0.3	V
$I_{O(inactive)}$	output current (inactive)	cards inactive and pins V_{CC} grounded	–	–	–1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	card supply output voltage	5 V card				
		cards active mode; I_{CC} < 65 mA	4.75	5	5.25	V
		cards active mode; current pulses of 40 nC; I_p < 200 mA; t_p < 400 ns; f_p < 20 MHz	4.6	–	5.4	V
		3 V card				
		cards active mode; I_{CC} < 50 mA	2.78	3	3.22	V
		cards active mode; current pulses of 24 nC; I_p < 200 mA; t_p < 400 ns; f_p < 20 MHz	2.75	–	3.25	V
		1.8 V card				
		cards active mode; I_{CC} < 30 mA	1.65	1.8	1.95	V
		cards active mode; current pulses of 12 nC; I_p < 200 mA; t_p < 400 ns; f_p < 20 MHz	1.62	–	1.98	V
I_{CC}	card supply output current	5 V card; operating	–	–	65	mA
		3 V card; operating	–	–	50	mA
		1.8 V card; operating	–	–	30	mA
SR	slew rate on V_{CC}	voltage moving up or down; capacitance = 300 nF (max.)	0.05	0.16	0.22	V/µs
$I_{CC1} + I_{CC2}$	sum of currents for both cards		–	–	–80	mA
Data lines (pins I/O1 and I/O2); note 3						
$V_{O(inactive)}$	output voltage (inactive)	cards inactive				
		no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	–	–	0.3	V
$I_{O(inactive)}$	output current (inactive)	cards inactive and pins I/O grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	pin I/O configured as an output; I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	pin I/O configured as an output; I_{OH} < –20 µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
		pin I/O configured as an output; I_{OH} < –40 µA (5 and 3 V cards)	$0.75V_{CC}$	–	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	pin I/O configured as an input	–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage	pin I/O configured as an input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–600	µA
I_{LIH}	input leakage current HIGH	$V_{IH} = V_{CC}$	–	–	20	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{i(tr)}$, $t_{i(tf)}$	input transition times	C_L < = 30 pF	–	–	1.2	µs
$t_{o(tr)}$, $t_{o(tf)}$	output transition times	C_L < = 30 pF	–	–	0.1	µs
R_{pu}	internal pull-up resistance between pin I/O and V_{CC}		10.5	12.5	14.5	kΩ
Contacts for auxiliary cards (pins C41, C81, C42 and C82); note 4						
$V_{O(inactive)}$	output voltage (inactive)	cards inactive				
		no load	0	–	0.1	V
		$I_{inactive}$ = 1 mA	–	–	0.3	V
$I_{O(inactive)}$	output current (inactive)	cards inactive and pin grounded	–	–	–1	mA
V_{OL}	LOW-level output voltage	I/O configured as output; I_{OL} = 1 mA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I/O configured as an output; I_{OH} < –20 µA	$0.8V_{CC}$	–	V_{CC} + 0.25	V
		I/O configured as an output; I_{OH} < –40 µA (5 and 3 V cards)	$0.75V_{CC}$	–	V_{CC} + 0.25	V
V_{IL}	LOW-level input voltage	I/O configured as an input	–0.3	–	+0.8	V
V_{IH}	HIGH-level output voltage	I/O configured as an input	1.5	–	V_{CC}	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–600	µA
I_{LIH}	input leakage current HIGH	V_{IH} = V_{CC}	–	–	20	µA
$t_{i(tr)}$, $t_{i(tf)}$	input transition times	C_L = 30 pF	–	–	1.2	µs
$t_{o(tr)}$, $t_{o(tf)}$	output transition times	C_L = 30 pF	–	–	0.1	µs
$t_{W(pu)}$	width of active pull-up pulse		–	200	–	ns
$R_{int(pu)}$	internal pull up resistance between pins C41, C81, C42, C82 and V_{CC}		8	10	12	kΩ
$f_{(max)}$	maximum frequency on pins C41, C81, C42, C82		–	–	1	MHz
Timing						
t_{act}	duration of activation sequence		–	–	130	µs
t_{deact}	duration of deactivation sequence		–	–	100	µs
Protection and limitation						
$I_{CC(sd)}$	shutdown and limitation current at V_{CC}		–	–100	–	mA
$I_{I/O(lim)}$	limitation current on the I/O		–10	–	+10	mA
$I_{CLK(lim)}$	limitation current on pin CLK		–70	–	+70	mA
$I_{RST(sd)}$	shutdown current on RST		–	–20	–	mA
$I_{RST(lim)}$	limitation current on RST		–20		+20	mA
T_{sd}	shutdown temperature		–	150	–	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card presence inputs (pins PRES1, PRES2)						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	–	V
$I_{IL(L)}$	input leakage current LOW	V_{IN} = 0	–10	–	+10	µA
$I_{IL(H)}$	input leakage current HIGH	$V_{IN} = V_{DD}$	–10	–	+10	µA
Logic inputs (pins INTAUX and $\overline{CS}$)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
$I_{IL(L)}$	input leakage current LOW		–20	–	+20	µA
$I_{IL(H)}$	input leakage current HIGH		–20	–	+20	µA
C_L	load capacitance		–	–	10	pF
Auxiliary I/O (pin I/OAUX); note 5						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
$I_{IL(H)}$	input leakage current HIGH		–20	–	+20	µA
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	–	–600	µA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–	–	300	mV
V_{OH}	HIGH-level output voltage	I_{OH} = 40 µA	$0.75V_{DD}$	–	V_{DD} + 0.25	V
$R_{int(pu)}$	internal pull-up resistance between I/OAUX and V_{DD}		8	10	12	kΩ
$t_{i(tr)}$, $t_{i(tf)}$	input transition time	C_L = 30 pF	–	–	1.2	µs
$t_{o(tr)}$, $t_{o(tf)}$	output transition time	C_L = 30 pF	–	–	0.1	µs
$f_{I/OAUX(max)}$	maximum frequency on pin I/OAUX		–	–	1	MHz
I/O ports: general purpose (pins P10 to P17, P20, P27 and P34 to P37), interrupts (pins $\overline{INT0}$ and $\overline{INT1}$) and serial links (pins RX and TX)						
V_{IL}	LOW-level input voltage	$4.0 < V_{DD} < 6.0$ V	–0.5	–	$0.2V_{DD}$ – 0.1	V
		$2.7 < V_{DD} < 4.0$ V	–0.5	–	0.7	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD}$ + 0.9	–	V_{DD} + 0.5	V
V_{OL}	LOW-level output voltage	V_{DD} = 2.7 V; I_{OL} = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	V_{DD} = 2.7 V; I_{OL} = –20 µA	V_{DD} – 0.7	–	–	V
		V_{DD} = 2.7 V; I_{OL} = –30 µA	V_{DD} – 0.7	–	–	V
I_{IL}	logic 0 input current	V_{IN} = 0.4 V	–1	–	–50	µA
I_{TL}	logic 1-to-0 transition current	V_{IN} = 2 V	–	–	–650	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General purpose I/O ports (pins P00 to P07)						
V_{IL}	LOW-level input voltage	$4.0 < V_{DD} < 6.0$ V	–0.5	–	$0.2V_{DD} - 0.1$	V
		$2.7 < V_{DD} < 4.0$ V	–0.5	–	0.7	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.5$	V
V_{OL}	LOW-level output voltage	V_{DD} = 2.7 V; I_{OL} = 3.2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	V_{DD} = 2.7 V; I_{OH} = –3.2 mA	$V_{DD} - 0.7$	–	–	V
I_{LI}	input leakage current	$0.45 < V_{IN} < V_{DD} - 0.3$	–	–	±10	μA
Input pin $\overline{EA}/V_{PP}$						
V_{IL}	LOW-level input voltage	$4.0 < V_{DD} < 6.0$V	–0.5	–	$0.2V_{DD} - 0.1$	V
		$2.7 < V_{DD} < 4.0$V	–0.5	–	0.7	V
V_{IH}	HIGH-level input voltage		$0.2V_{DD} + 0.9$	–	$V_{DD} + 0.5$	V
Output pins ALE and $\overline{PSEN}$						
V_{OL}	LOW-level output voltage	V_{DD} = 2.7 V; I_{OL} = 3.2 mA	–	–	0.4	V
V_{OH}	HIGH-level output voltage	V_{DD} = 2.7 V; I_{OH} = –3.2 mA	$V_{DD} - 0.7$	–	–	V
Input pins RESET (active HIGH) and XTAL1						
V_{IL}	LOW-level input voltage	$4.0 < V_{DD} < 6.0$V	–0.5	–	$0.2V_{DD} - 0.1$	V
		$2.7 < V_{DD} < 4.0$V	–0.5	–	0.7	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	$V_{DD} + 0.5$	V
$R_{int(reset)}$	Internal pull-down resistor on pin RESET		40	–	225	kΩ
Timing for bit CRED; see Figs 5, 6 and 7						
$t_{WR(UTR)}$	$\overline{WR}$ LOW to I/O LOW		$t_{WR} + 2t_{CLK}$	–	$t_{WR} + 3t_{CLK}$	ns
$t_{RD(URR)}$	$\overline{RD}$ LOW to CRED HIGH		$t_{RD} + 2t_{CLK}$	–	$t_{RD} + 3t_{CLK}$	ns
$t_{WR(TOC)}$	$\overline{WR}$ LOW to CRED HIGH		$\frac{1}{PSC}$	–	$\frac{2}{PSC}$	ETU

Notes

1. Includes currents at pins V_{DDD}, V_{DDA} and V_{DDP}.
2. Two ceramic multilayer capacitors with minimum 100 nF and low ESR should be used in order to meet these specifications.
3. Pin I/O1 has an integrated 14 kΩ pull-up resistor to V_{CC1}; pin I/O2 has an integrated 14 kΩ pull-up resistor to V_{CC2}.
4. Pins C41 and C81 have an integrated 10 kΩ pull-up resistor to V_{CC1}; pins C42 and C82 have an integrated 10 kΩ pull-up resistor to V_{CC2}.
5. Pin I/OAUX has a 14 kΩ pull-up resistor to V_{DD}.

13 APPLICATION INFORMATION

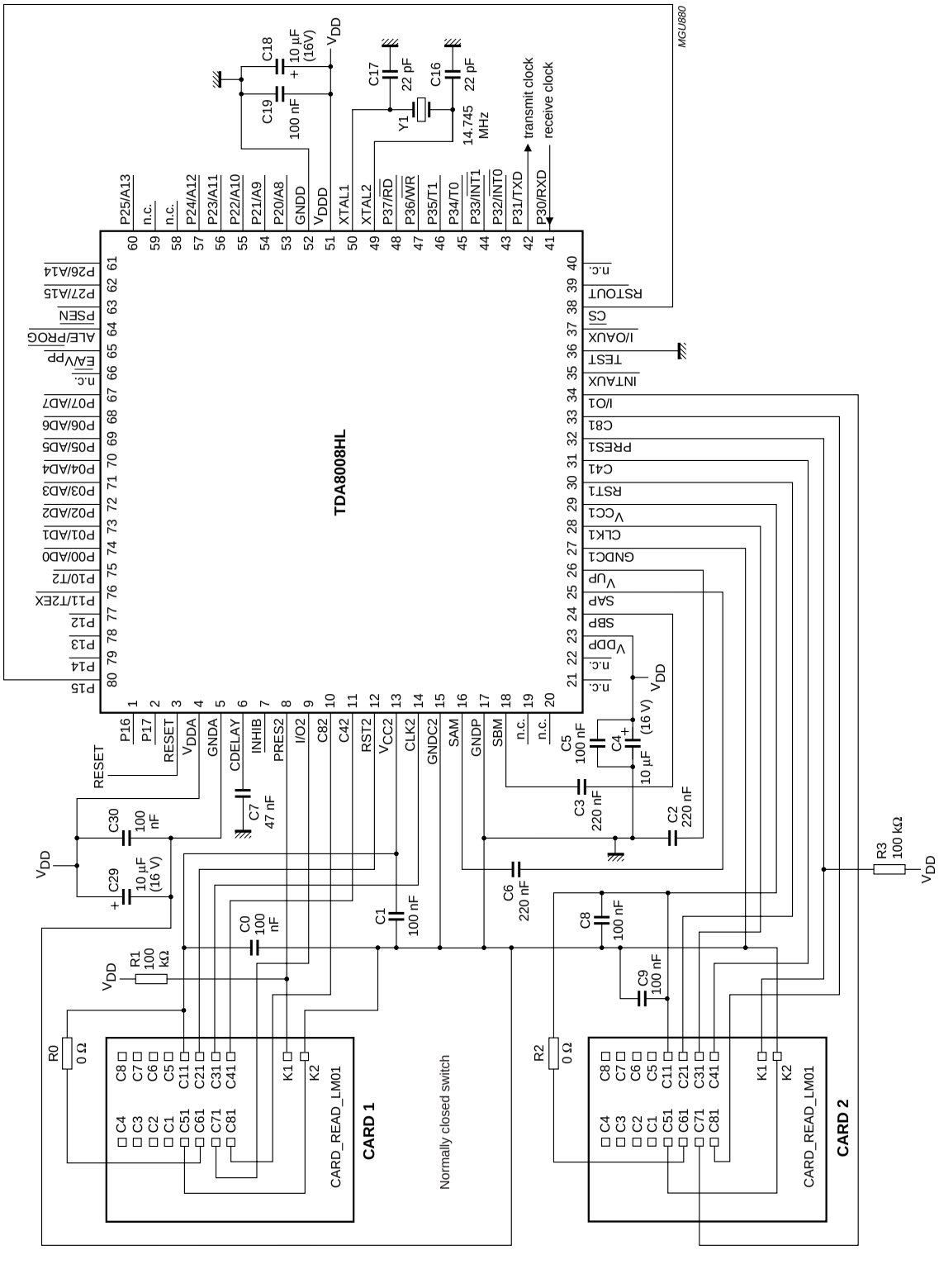
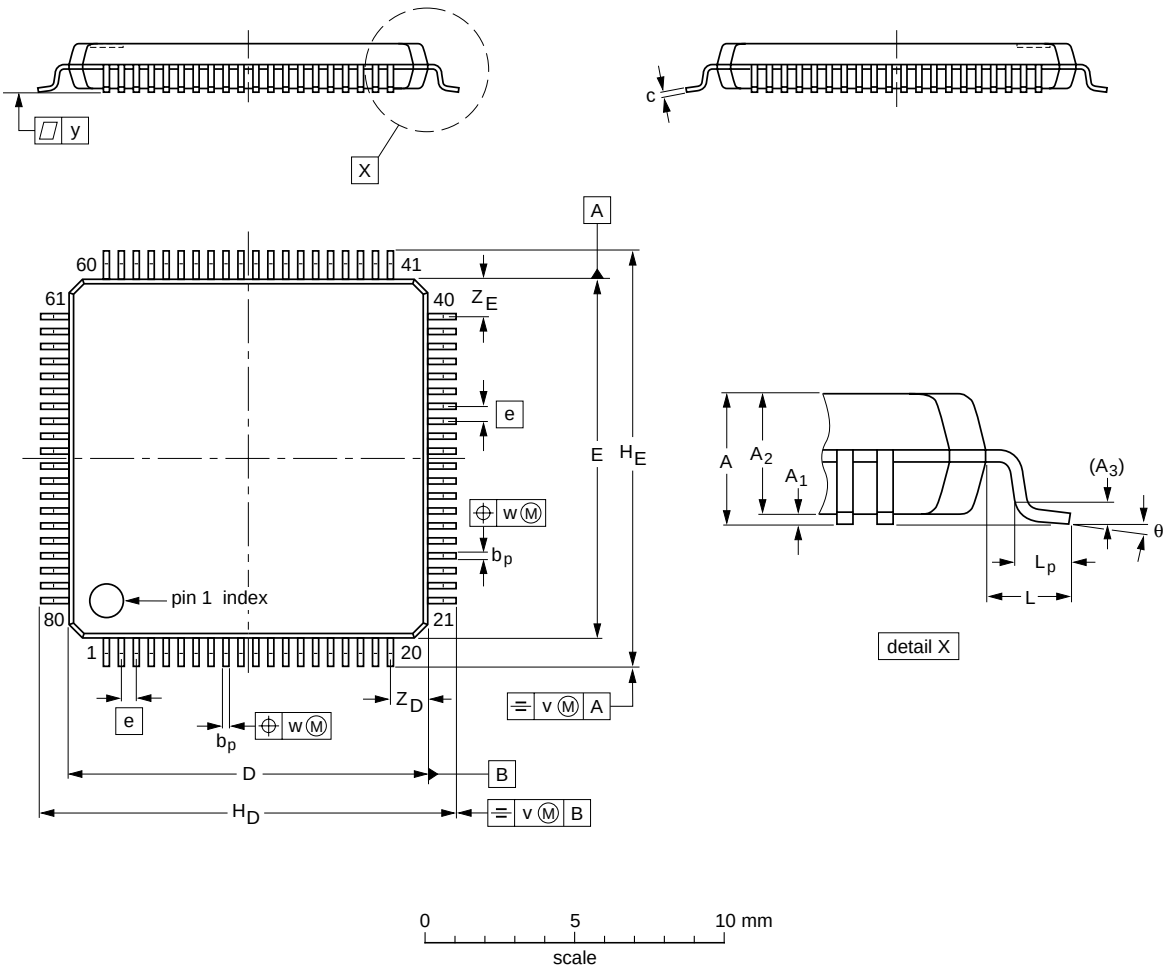


Fig.20 Application example.

14 PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
PMFP[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Hot bar or manual soldering is suitable for PMFP packages.

16 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

18 DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands 753504/03/pp67 Date of release: 2003 Jul 28 Document order number: 9397 750 11704

Let's make things better.

Philips
Semiconductors

PHILIPS