



Vehicle body and gateway controller SJA2010

Controlling the body

The SJA2010 is a 32-bit ARM7-based microcontroller for automotive body control and gateway applications. Featuring scalable Flash memory, dedicated in-vehicle network interfaces and a compelling peripheral set in a range of package options, the SJA2010 provides designers with the highest level of flexibility for implementing and customizing the on-chip peripherals.

Features

- ▶ 32-bit ARM7, running at up to 60 MHz
- ▶ 512/768 Kbytes embedded Flash with source code protection and 4 Mbits/s fast programming capability
- ▶ 40 Kbytes SRAM
- ▶ CAN 2.0B compliant with FullCAN receive mode and triple transmit buffers
- ▶ 6 CAN controllers and 8 LIN 2.0 master controllers
- ▶ 2 UARTS and 3 full-duplex SPI channels
- ▶ Real time clock with on-chip 32 kHz crystal oscillator and battery supply
- ▶ 4 x 32-bit timers, each with four capture and compare registers
- ▶ 18 level-sensitive external interrupt pins
- ▶ 32 analog input pins
- ▶ 24 PWM outputs, suitable for light dimming and brushless DC motor control
- ▶ Up to 160 general purpose I/Os
- ▶ Internal programmable ringoscillator for power saving mode
- ▶ LQFP144/LQFP208
- ▶ LQFP176 on request
- ▶ Automotive AEC Q100 qualified
- ▶ Temperature range: -40 + 105° ambient

The 32-bit ARM7 microcontroller SJA2010 includes dedicated hardware for IVN communication, making it the ideal solution for high-performance automotive body control and gateway systems as well as combined body control and gateway applications.

It supports specific hardware for 6 CAN channels and 8 dedicated LIN 2.0 master controllers, enabling high performance network communication with minimal CPU load.

Furthermore the SJA2010 features 4 versatile PWM modules with 6 outputs each, useful for applications such as light dimming. Direct coupling between the PWM modules and the A/D converters also makes the SJA2010 ideal for brushless DC motor control.

Benefits

- ▶ Powerful, flexible solution with extensive functionality and I/Os
- ▶ Hardware support for CAN and LIN
- ▶ Same microcontroller can be used for multiple applications

Applications

- ▶ Body control
- ▶ Light dimming
- ▶ Combined body control/gateways
- ▶ Dashboard and comfort systems
- ▶ Brushless DC motor control

Employing NXP's reuse design approach, including all software and hardware gateway functionality, provides designers with the highest level of flexibility in terms of implementation and customization of the gateway. All CAN channels are CAN 2.0B compliant with FullCAN receive mode and triple transmit buffers. A unique global acceptance filter services all CAN controllers with a scanning algorithm, ensuring extremely short transfer latency times. Three state-of-the-art SPI interfaces and an external bus interface allow fast access to multimedia networks such as MOST or IDB-1394.

Universal functionality

The SJA2010 microcontroller is ideal for automotive applications requiring 32-bit processing power and large pin count. Up to 160 general purpose I/O's, 32 analog input pins, 24 PWM outputs together with 3 full-duplex SPI channels, 6 CAN controller and 8 LIN 2.0 master controllers make it a universal solution. The SJA2010 is available in packages with 144 up to 208 pins so that the same microcontroller can be used for different application areas.

ARM7TDMI-S embedded processor core

The ARM7TDMI-S is a general-purpose 32-bit microprocessor, which offers high performance and very low power consumption. Based on reduced instruction set computer (RISC) principles, the instruction set and related decode mechanism are much simpler than those of micro programmed complex instruction set computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Clocked by an on-chip PLL that allows CPU operation up to 60 MHz, the 32-bit RISC architecture of the ARM7 core also features a 16-bit thumb mode resulting in higher code density due to a reduced instruction set. The SJA2010 contains a

very flexible Vectored Interrupt Controller (VIC) with up to 16 priority levels to interrupt the ARM processor on request. The software development is facilitated by the standard ARM Test/Debug interface with Real-Time In-Circuit Emulator.

6 CAN Global Acceptance Filter FullCAN receive mode Triple Transmit buffers	32bit ARM7 60MHz VIC with 16 priority levels & 12 external interrupts	512/768kB Flash with Source Code Protection, programmable at 4Mb/s
8 LIN 2.0 Masters Message buffers LIN message optimized		
3 SPI 16bit, Tx/Rx FIFOs	WatchDog 32bit, with timer change protection	40kB SRAM
2 UARTs with local message buffers	Ringoscillator for power saving modes	4 PWM 6 channels each, 16bit
Bus Interface 8, 16 or 32bit data, 26bit address, up to 8 memory banks	Real Time Clock with separate supply	3 ADCs 16/8/8 channels, 10bit
	4 timers 32bit, 4 cap/match register each	
up to 160 GPIO		

SJA2010 block diagram