DATA SHEET

P80CL580; P83CL580
Low voltage 8-bit microcontrollers with UART, I^2C-bus and ADC

Product specification
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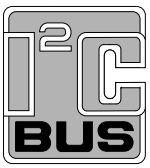
CONTENTS



1 FEATURES

- Full static 80C51 Central Processing Unit
- 8-bit CPU, ROM, RAM, I/O in a 56-lead VSO or 64-lead QFP package
- 256 bytes on-chip RAM Data Memory
- 6 kbytes on-chip ROM Program Memory for P83CL580
- External memory expandable up to 128 kbytes: RAM up to 64 kbytes and ROM up to 64 kbytes
- Five 8-bit ports; 40 I/O lines
- Three 16-bit Timers/Event counters
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector, nested interrupt structure with two priority levels
- Full duplex serial port (UART)
- I²C-bus interface for serial transfer on two lines
- Analog-to-digital converter (ADC) with Power-down mode; 4 input channels and 8-bit ADC
- Pulse Width Modulated (PWM) output (8-bit resolution)
- Watchdog Timer
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four 8-byte RAM register banks
  - stack depth limited only by available internal RAM (maximum 256 bytes)
  - multiply, divide, subtract and compare instructions
- Reduced power consumption through Power-down and Idle modes
- Wake-up via external interrupts at Port 1
- Frequency range: 0 to 12 MHz. For ADC operation minimum 250 kHz at 2.7 V
- Supply voltage: 2.5 to 6.0 V
- Very low current consumption: typically 4.5 mA at 2.5 V and 8 MHz
- Operating ambient temperature range: –40 to +85 °C.

2 GENERAL DESCRIPTION

The P80CL580; P83CL580 (hereafter generally referred to as P8xCL580) is manufactured in an advanced CMOS technology. The P8xCL580 has the same instruction set as the 80C51, consisting of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte. The device operates over a wide range of supply voltages and has low power consumption; there are two software selectable modes for power reduction: Idle and Power-down. For emulation purposes, the P85CL580 (piggy-back version) with 256 bytes of RAM is recommended.

This data sheet details the specific properties of the P80CL580; P83CL580. For details of the 80C51 core and the I²C-bus see *"Data Handbook IC20"*.

2.1 ROMless version: P80CL580

The P80CL580 is the ROMless version of the P83CL580. The mask options on the P80CL580 are fixed as follows:

- All ports have option '1S' (standard port, HIGH after reset), except ports P1.6 and P1.7 which have option '2S' (open-drain, HIGH after reset)
- Oscillator option: Oscillator 3
- Power-on-reset option: off.

3 APPLICATIONS

The P8xCL580 is an 8-bit general purpose microcontroller especially suited for cordless telephone and mobile communication applications. The P8xCL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities.

4 ORDERING INFORMATION

TYPE NUMBER(1)	PACKAGE		
	NAME	DESCRIPTION	VERSION
P8xCL580HFT	VSO56	plastic very small outline package; 56 leads	SOT190-1
P8xCL580HFH	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm	SOT319-2

Note

1. 'x' = 0 or 3. Refer to the Order Entry Form (OEF) for this device for the full type number, including options/program.

5 BLOCK DIAGRAM

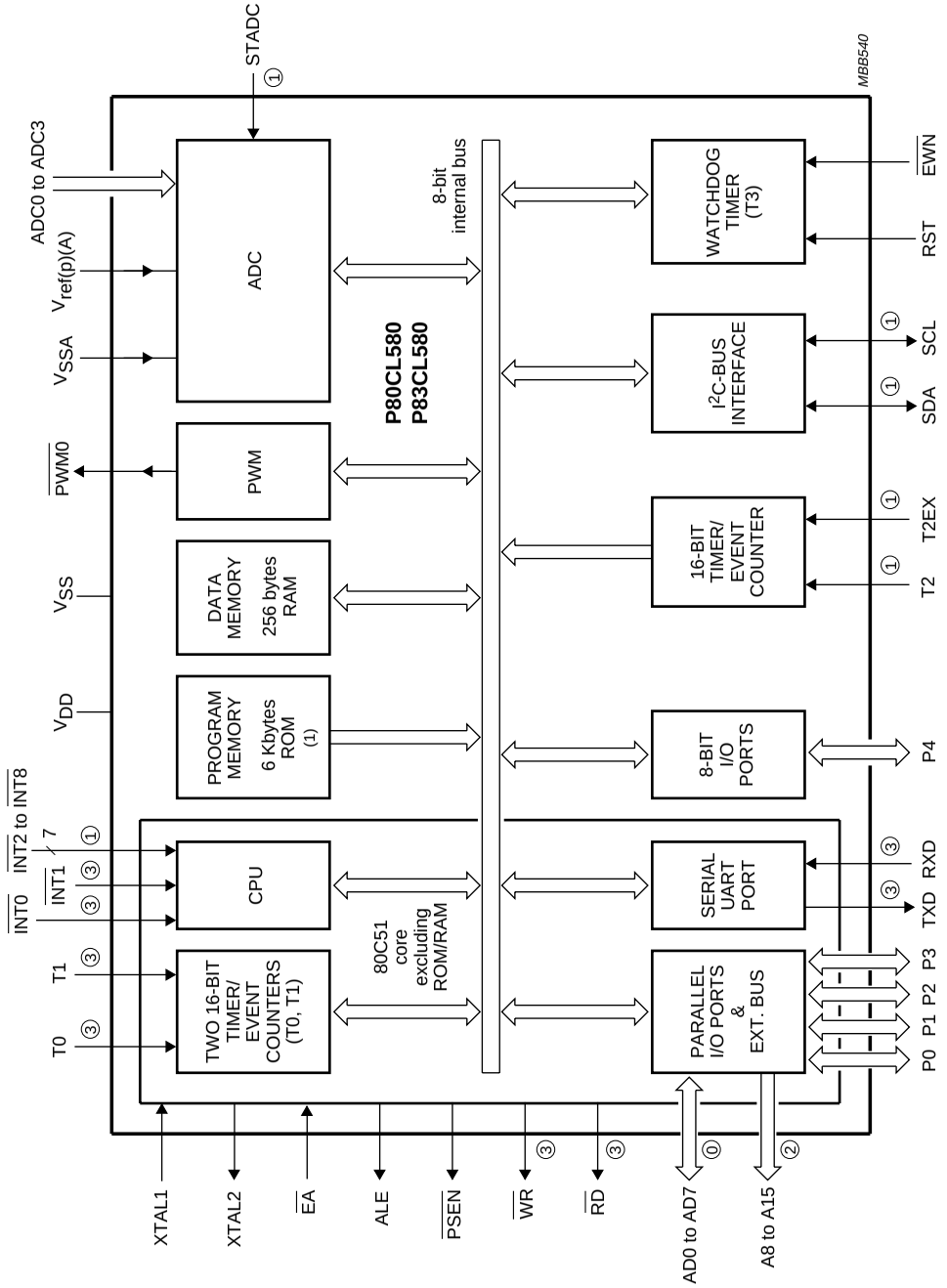


Fig.1 Block diagram.

6 FUNCTIONAL DIAGRAM

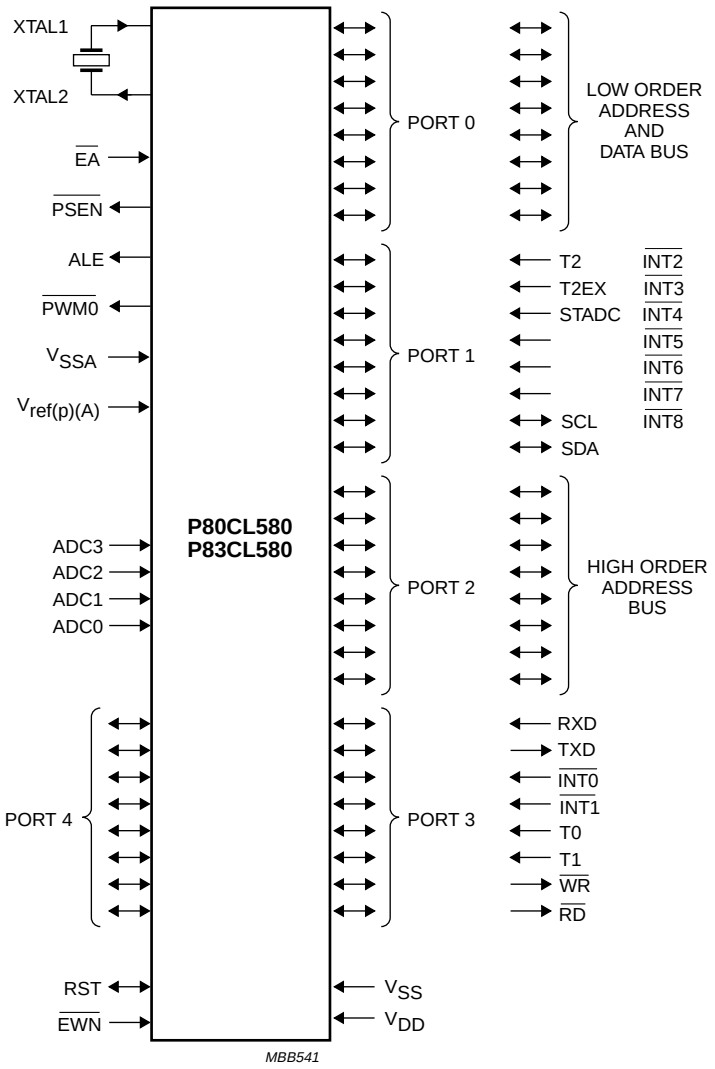


Fig.2 Functional diagram.

7 PINNING INFORMATION

7.1 Pinning

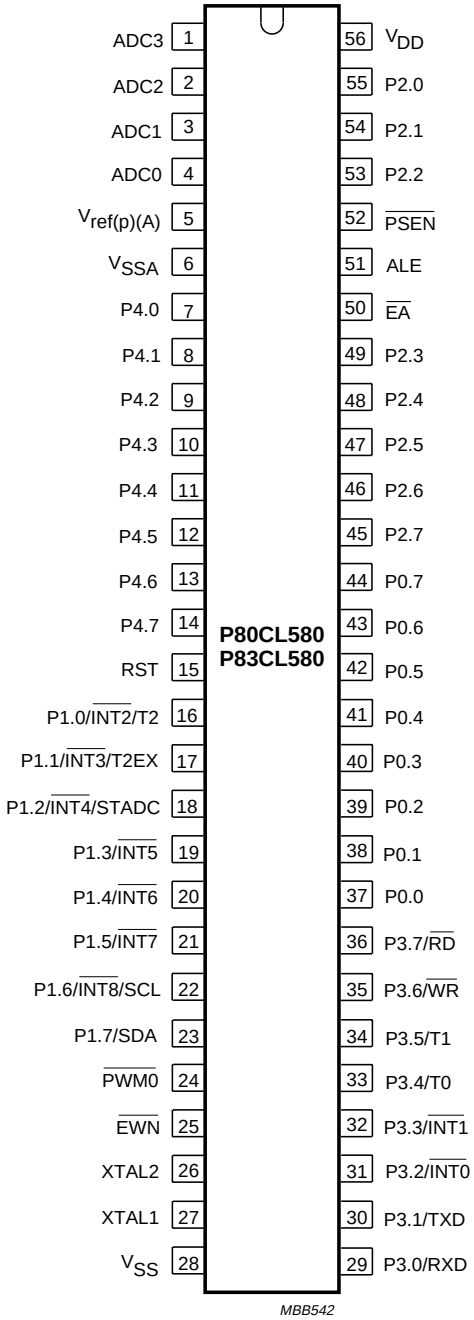


Fig.3 Pin configuration for VSO56 package.

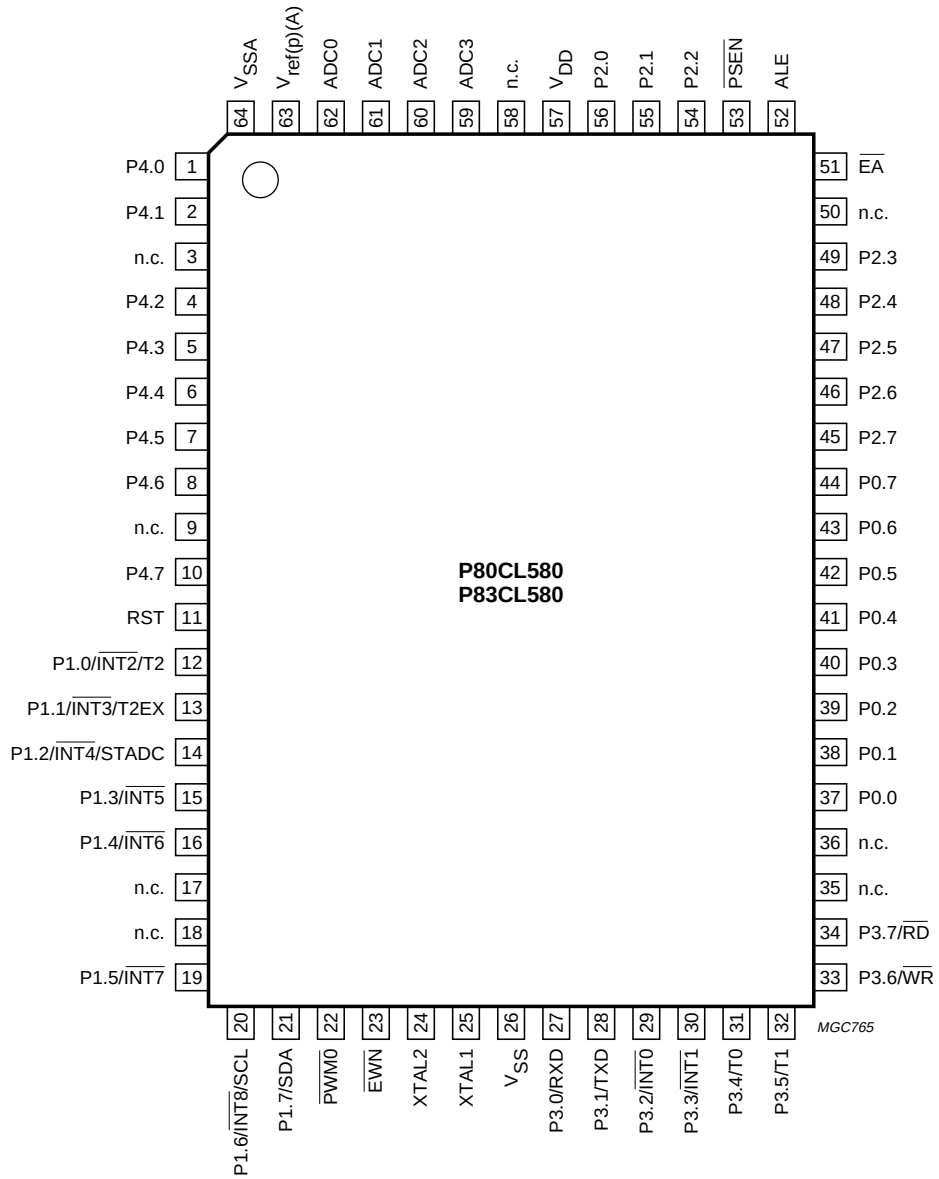


Fig.4 Pin configuration for QFP64 package.

7.2 Pin description

Table 1 Pin description for VSO56 (SOT190-1) and QFP64 (SOT319-2)
For more extensive description of the port pins see Chapter 10 “I/O facilities”.

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
ADC3 to ADC0	1 to 4	59 to 62	4 input channels to the ADC.
$V_{ref(p)(A)}$	5	63	Positive potential of analog-to-digital conversion reference resistor.
V_{SSA}	6	64	Analog part ground.
P4.0 to P4.7	7 to 14	1, 2, 4 to 8, 10	**Port 4**: 8-bit bidirectional I/O port. (P4.0 to P4.7). Port pins that have logic 1s written to them are pulled HIGH by internal pull-ups, and in this state can be used as inputs. As inputs, Port 4 pins that are externally pulled LOW will source current (I_{IL}, see Chapter 23) due to the internal pull-ups. Port 4 output buffers can sink/source 4 LS TTL loads.
RST	15	11	**Reset**: a HIGH level on this pin for two machine cycles while the oscillator is running resets the device.
P1.0/$\overline{\text{INT2}}$/T2	16	12	• **Port 1:** 8-bit bidirectional I/O port (P1.0 to P1.7). Same characteristics as Port 4, but note that P1.6 and P1.7 are open-drain only. • **Alternative functions:** – INT2 to INT8 are external interrupt inputs – STADC is the external trigger of the analog-to-digital converter – T2 and T2EX are the Timer/event counter 2 inputs – SCL and SDA are the I²C-bus clock and data lines.
P1.1/$\overline{\text{INT3}}$/T2EX	17	13	
P1.2/$\overline{\text{INT4}}$/STADC	18	14	
P1.3/$\overline{\text{INT5}}$	19	15	
P1.4/$\overline{\text{INT6}}$	20	16	
P1.5/$\overline{\text{INT7}}$	21	19	
P1.6/$\overline{\text{INT8}}$/SCL	22	20	
P1.7/SDA	23	21	
$\overline{\text{PWM0}}$	24	22	**Pulse Width Modulation output 0**.
$\overline{\text{EWN}}$	25	23	**Enable Watchdog Timer**: enable for Watchdog Timer and enable Power-down mode.
XTAL2	26	24	**Crystal oscillator output**: output of the inverting amplifier of the oscillator. Left open when external clock is used.
XTAL1	27	25	**Crystal oscillator input**: input to the inverting amplifier of the oscillator, also the input for an externally generated clock source.
V_{SS}	28	26	Ground: circuit ground potential.

SYMBOL	PIN		DESCRIPTION
	VSO56	QFP64	
P3.0/RXD P3.1/TXD P3.2/$\overline{\text{INT0}}$ P3.3/$\overline{\text{INT1}}$ P3.4/T0 P3.5/T1 P3.6/$\overline{\text{WR}}$ P3.7/$\overline{\text{RD}}$	29 30 31 32 33 34 35 36	27 28 29 30 31 32 33 34	• **Port 3:** 8-bit bidirectional I/O port (P3.0 to P3.7). Same characteristics as Port 4 • **Alternative functions:** – RXD is the UART serial data input (asynchronous) or data input/output (synchronous) – TXD is the UART serial data output (asynchronous) or clock output (synchronous) – $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ are external interrupts 0 and 1 – T0 and T1 are external inputs for timers 0 and 1. – $\overline{\text{WR}}$ is the external Data Memory write strobe – $\overline{\text{RD}}$ is the external Data Memory read strobe
P0.0 to P0.7	37 to 44	37 to 44	• **Port 0**: 8-bit open-drain bidirectional I/O port. As an open-drain output port it can sink 8 LS TTL loads. Port 0 pins that have logic 1s written to them float, and in that state will function as high impedance inputs. • **Low-order addressing**: Port 0 is also the multiplexed low-order address and data bus during access to external memory. The strong internal pull-ups are used while emitting logic 1s within the low order address.
P2.0 to P2.7	55 to 53, 49 to 45	56 to 54, 49 to 45	• **Port 2**: 8-bit bidirectional I/O port with internal pull-ups. Same characteristics as Port 4. • **High-order addressing**: Port 2 emits the high-order address byte during accesses to external memory that use 16-bit addresses (MOVX @DPTR). In this application it uses the strong internal pull-ups when emitting logic 1s. During accesses to external memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.
$\overline{\text{EA}}$	50	51	**External Access**. When $\overline{\text{EA}}$ is held HIGH the CPU executes out of internal Program Memory (unless the program counter exceeds 17FFH). Holding $\overline{\text{EA}}$ LOW forces the CPU to execute out of external memory regardless of the value of the Program Counter.
ALE	51	52	**Address Latch Enable**. Output pulse for latching the low byte of the address during access to external memory. ALE is emitted at a constant rate of $\frac{1}{6} \times f_{osc}$, and may be used for external timing or clocking purposes (assuming MOVX instructions are not used).
$\overline{\text{PSEN}}$	52	53	**Program Store Enable**. Output read strobe to external Program Memory. When executing code out of external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle. However, during each access to external Data Memory two $\overline{\text{PSEN}}$ activations are skipped.
V_{DD}	56	57	Power supply.
n.c.	–	3, 9, 17, 18, 35, 36, 50 and 58	Not connected.

8 FUNCTIONAL DESCRIPTION OVERVIEW

This chapter gives a brief overview of the device. The detailed functional description is in the following chapters:

Chapter 9 “Memory organization”

Chapter 10 “I/O facilities”

Chapter 11 “Timers/event counters”

Chapter 12 “Pulse Width Modulated output”

Chapter 13 “Analog-to-digital converter (ADC)”

Chapter 14 “Reduced power modes”

Chapter 15 “I²C-bus serial I/O”

Chapter 16 “Standard serial interface SIO0: UART”

Chapter 17 “Interrupt system”

Chapter 18 “Oscillator circuitry”

Chapter 19 “Reset”.

8.1 General

The P8xCL580 is a stand-alone high-performance CMOS microcontroller designed for use in real-time applications such as cordless telephone and mobile communications, instrumentation, industrial control, intelligent computer peripherals and consumer products.

The device provides hardware features, architectural enhancements and new instructions to function as a controller for applications requiring up to 64 kbytes of Program Memory and/or up to 64 kbytes of Data Memory.

The P8xCL580 contains a 6 kbytes Program Memory (ROM; P83CL580); a static 256 bytes Data Memory (RAM); 40 I/O lines; three 16-bit timer/event counters; a fifteen-source two priority-level, nested interrupt structure and on-chip oscillator and timing circuit, 4-channel 8-bit A/D converter, Watchdog Timer and Pulse Width Modulation output.

The device has two software-selectable modes of reduced activity for power reduction:

- **Idle mode**; freezes the CPU while allowing the derivative functions (timers, serial I/O, ADC, PWM) and interrupt system to continue functioning.
- **Power-down mode**; saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

In addition, two serial interfaces are provided on-chip:

- A standard UART serial interface, and
- A standard I²C-bus serial interface. The I²C-bus serial interface has byte-oriented master and slave functions allowing communication with the whole family of I²C-bus compatible devices.

8.2 CPU timing

A machine cycle consists of a sequence of 6 states. Each state lasts for two oscillator periods, thus a machine cycle takes 12 oscillator periods or 1 μs if the oscillator frequency (f_{osc}) is 12 MHz.

9 MEMORY ORGANIZATION

The P8xCL580 has 6 kbytes of Program Memory (ROM; P83CL580 only) plus 256 bytes of Data Memory (RAM) on board.The device has separate address spaces for Program and Data Memory (see Fig.6). Using Port latches P0 and P2, the P8xCL580 can address up to 128 kbytes of external memory. The CPU generates both read ($\overline{RD}$) and write ($\overline{WR}$) signals for external Data Memory accesses, and the read strobe ($\overline{PSEN}$) for external Program Memory.

9.1 Program Memory

The P83CL580 contains 6 kbytes of internal ROM. After reset the CPU begins execution at location 0000H. The lower 6 kbytes of Program Memory can be implemented in either on-chip ROM or external Program Memory.

If the $\overline{EA}$ pin is tied to V_{DD}, then Program Memory fetches from addresses 0000H to 17FFH are directed to the internal ROM. Fetches from addresses 1800H to FFFFH are directed to external ROM. Program Counter values greater than 17FFH are automatically addressed to external memory regardless of the state of the $\overline{EA}$ pin.

9.2 Data Memory

The P8xCL580 contains 256 bytes of internal RAM and 40 Special Function Registers (SFRs). Figure 6 shows the internal Data Memory space divided into the lower 128 bytes, the upper 128 bytes, and the SFRs space. Internal RAM locations 0 to 127 are directly and indirectly addressable. Internal RAM locations 128 to 255 are only indirectly addressable. The Special Function Register locations 128 to 255 bytes are only directly addressable.

9.3 Special Function Registers (SFRs)

The upper 128 bytes are the address locations of the SFRs. Figures 7 and 8 show the Special Function Registers space. The SFRs include the port latches, timers, peripheral control, serial I/O registers, etc. These registers can only be accessed by direct addressing. There are 128 directly addressable locations in the SFR address space. Bit addressable SFRs are those that end in 000B.

9.4 Addressing

The P8xCL580 has five methods for addressing source operands:

- Register
- Direct
- Register-indirect
- Immediate
- Base-register plus index-register-indirect.

The first three methods can be used for addressing destination operands. Most instructions have a ‘destination/source’ field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

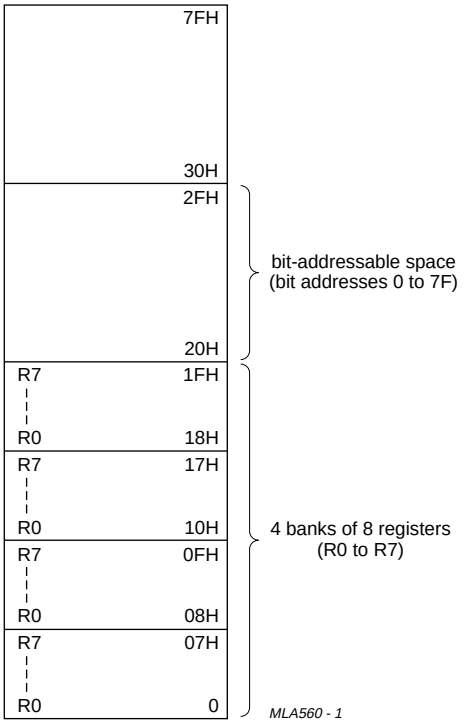


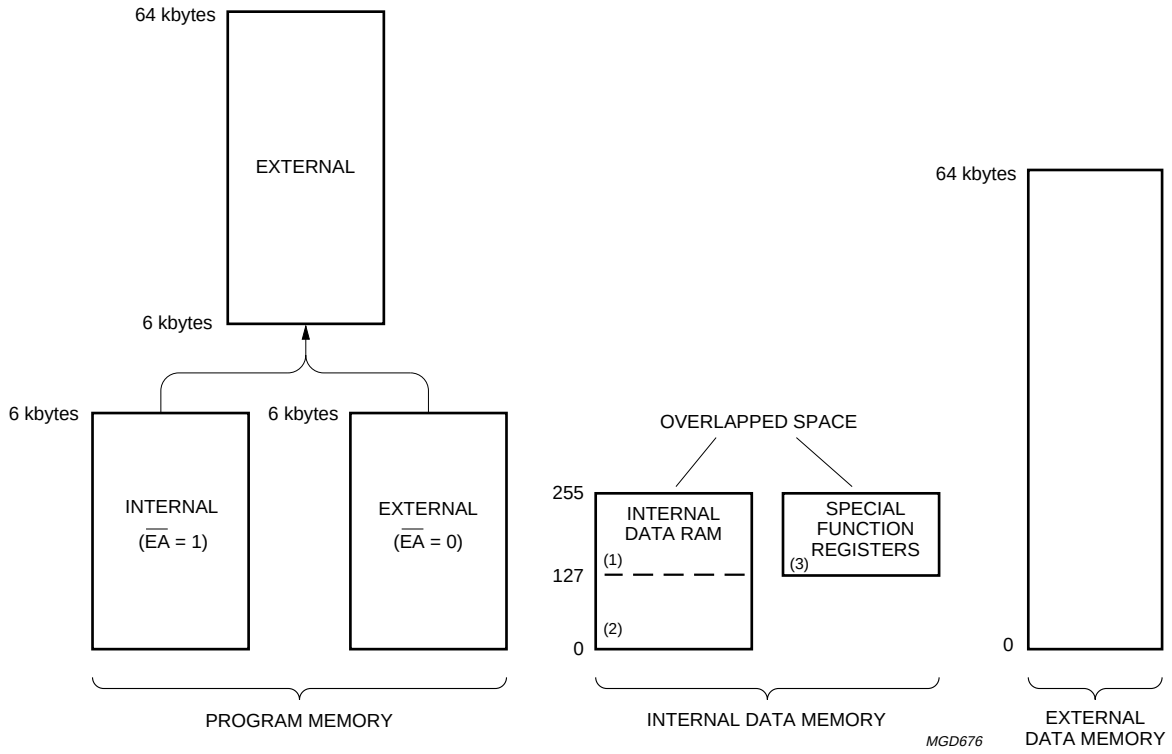
Fig.5 The lower 128 bytes of internal RAM.

Access to memory addressing is as follows:

- Registers in one of the four register banks through register, direct or register-indirect
- Lower 128 bytes of internal RAM through direct or register-indirect; upper 128 bytes of internal RAM through direct
- Special Function Registers through direct
- External Data Memory through register-indirect
- Program Memory look-up tables through base-register plus index-register-indirect.

The P8xCL580 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers, Arithmetic Logic Unit and external data bus are all 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.



(1) Accessible via indirect addressing only.
(2) Accessible via direct and indirect addressing.
(3) Accessible via direct addressing.

Fig.6 Memory map.

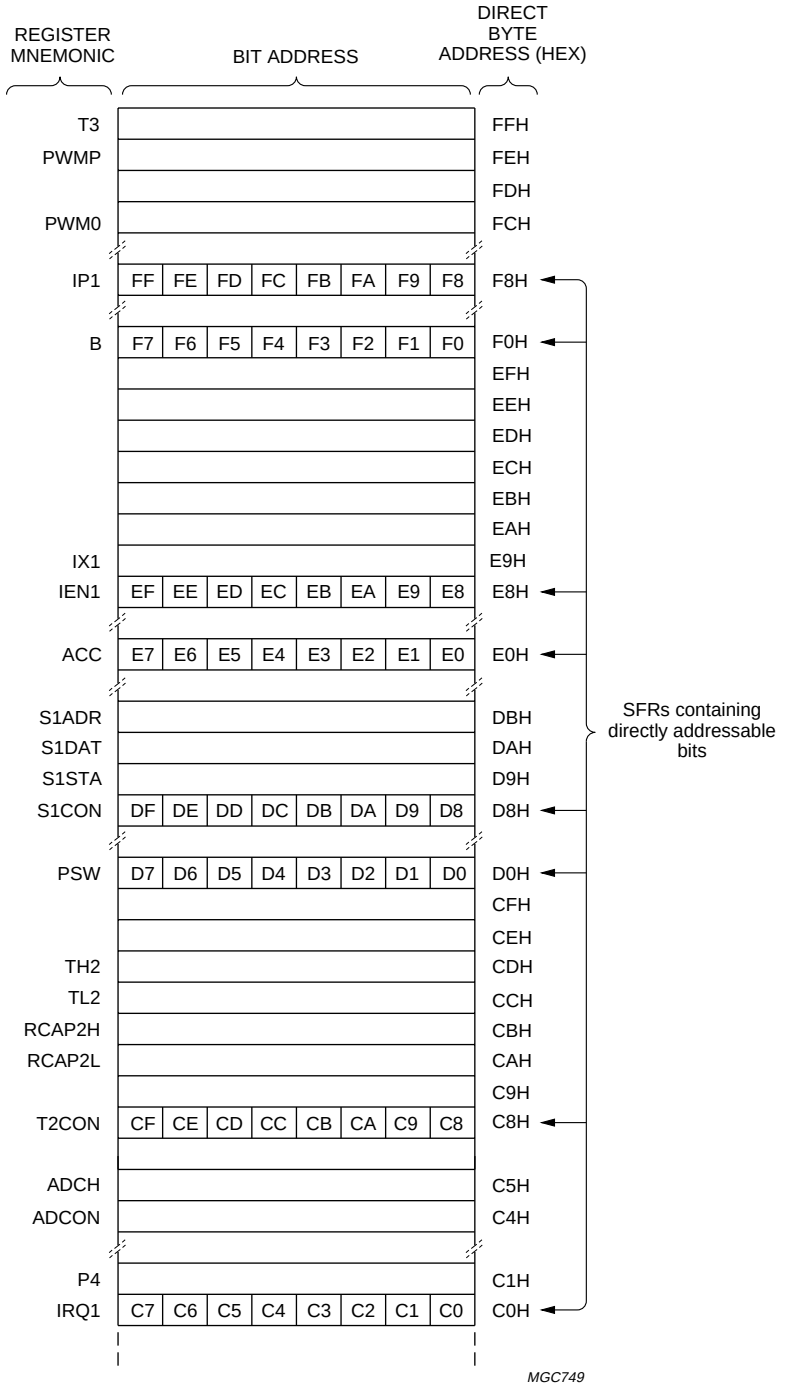


Fig.7 Special Function Register memory map (continued in Fig.8).

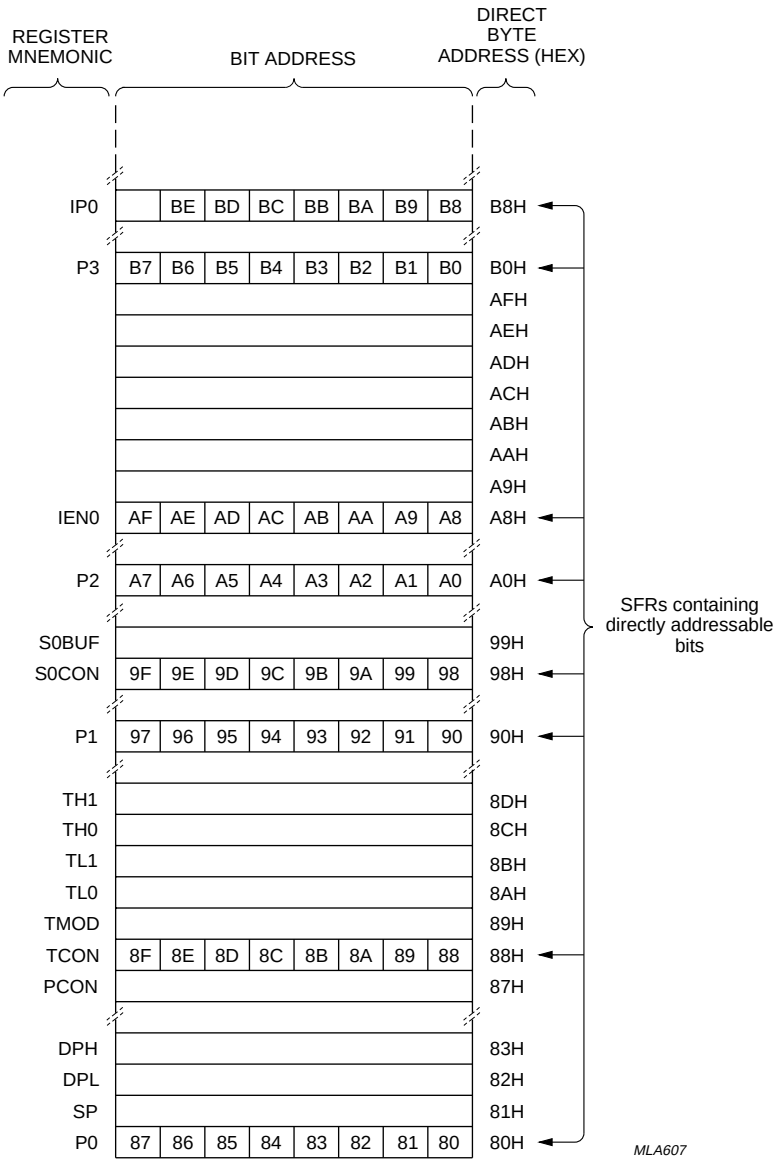


Fig.8 Special Function Register memory map (continued from Fig.7).

10 I/O FACILITIES

10.1 Ports

The P8xCL580 has 40 I/O lines treated as one 8-bit port plus 32 individually addressable bits or as five parallel 8-bit addressable ports.

Port 4 has no alternative functions. To enable a port pin alternative function for Ports 0, 1, 2 and 3, the port bit latch in its SFR must contain a logic 1. The alternative functions are detailed below:

Port 0 Provides the multiplexed low-order address and data bus for expanding the device with standard memories and peripherals.

Port 1 Used for a number of special functions:

- Provides the inputs for the external interrupts: $\overline{INT2}$ to $\overline{INT8}$.
- External activation of Timer 2: T2.
- External trigger of the ADC: STADC.
- The I²C-bus interface: SCL and SDA.

Port 2 Provides the high-order address when expanding the device with external Program or Data Memory.

Port 3 Pins can be configured individually to provide:

- External interrupt request inputs: $\overline{INT1}$ and $\overline{INT0}$.
- Counter input: T1 and T0.
- Control signals to read and write to external memories: $\overline{RD}$ and $\overline{WR}$.
- UART input and output: RXD and TXD.

Each port consists of a latch (SFRs P0 to P4), an output driver and input buffer. Ports 1, 2, 3 and 4 have internal pull-ups (except P1.6 and P1.7). Figure 9(a) shows that the strong transistor ‘p1’ is turned on for only 2 oscillator periods after a LOW-to-HIGH transition in the port latch. When on, it turns on ‘p3’ (a weak pull-up) through the inverter. This inverter and ‘p3’ form a latch which holds the logic 1. In Port 0 the pull-up ‘p1’ is only on when emitting logic 1s for external memory access. Writing a logic 1 to a Port 0 bit latch leaves both output transistors switched off so that the pin can be used as an high-impedance input.

10.2 Port options

38 of the 40 port pins (excluding P1.6 and P1.7 with option 2S only) may be individually configured with one of the following options. These options are also shown in Fig.9.

Option 1 **Standard Port**; quasi-bidirectional I/O with pull-up. The strong booster pull-up ‘p1’ is turned on for two oscillator periods after a LOW-to-HIGH transition in the port latch; Fig.9(a).

Option 2 **Open-drain**; quasi-bidirectional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor; see Fig.9(b).

Option 3 **Push-pull**; output with drive capability in both polarities. Under this option, pins can only be used as outputs; see Fig.9(c).

10.3 Port 0 options

The definition of port options for Port 0 is slightly different. Two cases are considered. First, access to external memory ($\overline{EA}$ = 0 or access above the built-in memory boundary) and second, I/O accesses.

10.3.1 External memory accesses

Option 1 True logic 0 and logic 1 are written as address to the external memory (strong pull-up to be used).

Option 2 An external pull-up resistor is required for external accesses.

Option 3 Not allowed for external memory accesses as the port can only be used as output.

10.3.2 I/O Accesses

Option 1 When writing a logic 1 to the port latch, the strong pull-up ‘p1’ will be on for 2 oscillator periods. No weak pull-up exists. Without an external pull-up, this option can be used as a high-impedance input.

Option 2 Open-drain; quasi-directional I/O with n-channel open-drain output. Use as an output requires the connection of an external pull-up resistor. See Fig.9(b).

Option 3 Push-Pull; output with drive capability in both polarities. Under this option pins can only be used as outputs. See Fig.9(c).

10.4 SET/RESET options

Individual mask selection of the post-reset state is available with any of the above pins. The selection is made by appending ‘S’ or ‘R’ to Options 1, 2, or 3 above.

Option R RESET, at reset this pin will be initialized LOW.

Option S SET, at reset this pin will be initialized HIGH.

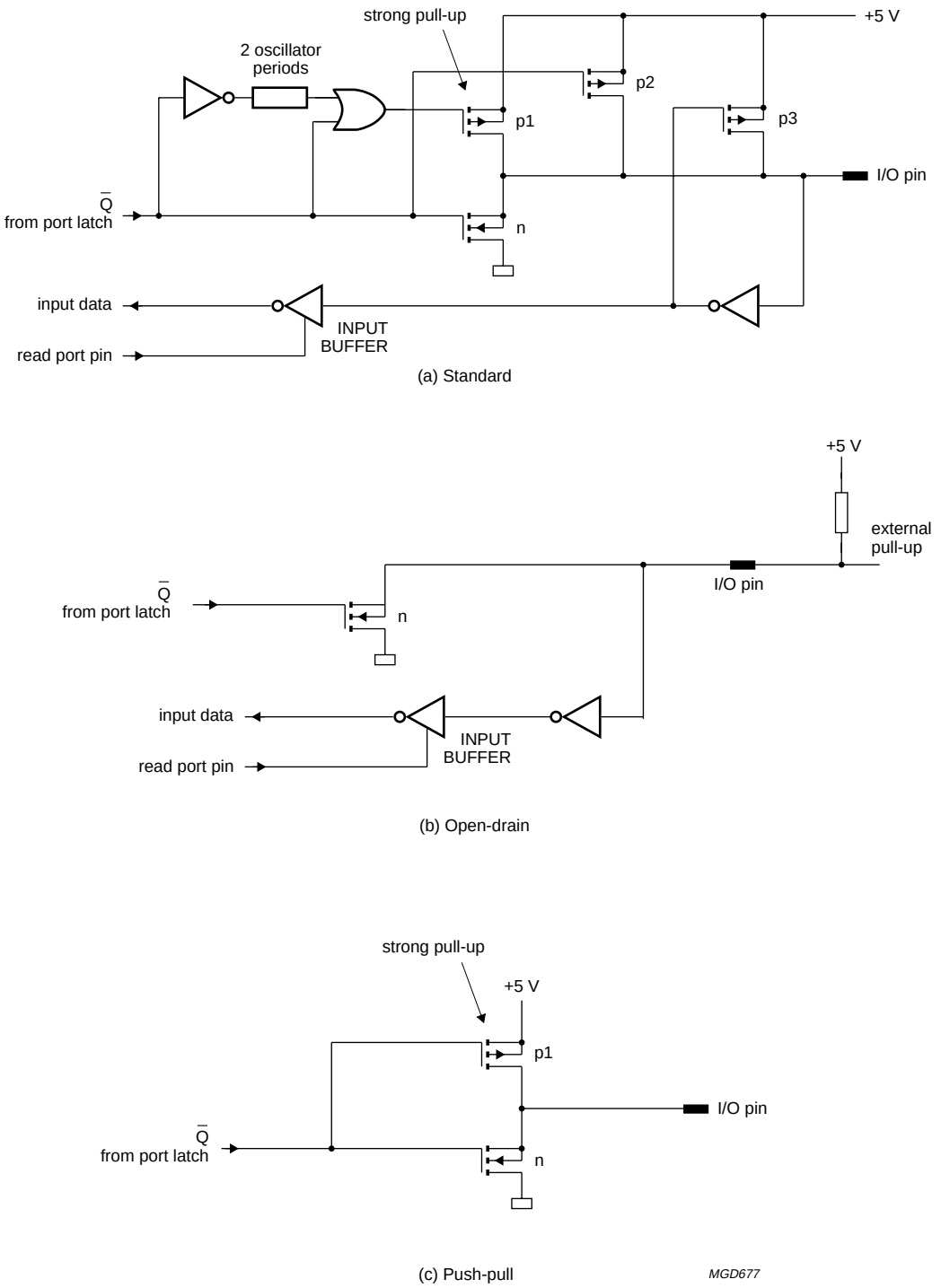


Fig.9 Port configuration options.

11 TIMERS/EVENT COUNTERS

The P8xCL580 contains three 16-bit timer/event counter registers; Timer 0, Timer 1 and Timer 2 which can perform the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

In the 'Timer' operating mode the register is incremented every machine cycle. Since a machine cycle consists of 12 oscillator periods, the count rate is $\frac{1}{12} \times f_{osc}$.

In the 'Counter' operating mode, the register is incremented in response to a HIGH-to-LOW transition. Since it takes 2 machine cycles (24 oscillator periods) to recognize a HIGH-to-LOW transition, the maximum count rate is $\frac{1}{24} \times f_{osc}$. To ensure a given level is sampled, it should be held for at least one complete machine cycle.

11.1 Timer 0 and Timer 1

Timer 0 and Timer 1 can be programmed independently to operate in four modes:

Mode 0 8-bit timer or 8-bit counter each with divide-by-32 prescaler.

Mode 1 16-bit time-interval or event counter.

Mode 2 8-bit time-interval or event counter with automatic reload upon overflow.

Mode 3 Timer 0 establishes TL0 and TH0 as two separate counters.

11.2 Timer T2

Timer T2 is a 16-bit timer/counter that can operate (like Timer 0 and 1) either as a timer or as an event counter. These functions are selected by the state of the C/$\overline{T2}$ bit in the T2CON register; see Tables 2 and 3.

Three operating modes are available Capture, Auto-reload and Baud Rate Generator, which also are selected via the T2CON register; see Table 4.

11.2.1 CAPTURE MODE

Figure 10 shows the Capture mode. Two options in this mode, may be selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets the Timer 2 overflow bit TF2, this may then be used to generate an interrupt.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX causes the current value in TL2 and TH2 to be captured into registers RCAP2L and RCAP2H respectively. In addition, the transition at T2EX causes the EXF2 bit in T2CON to be set; this may also be used to generate an interrupt.

11.2.2 AUTO-RELOAD MODE

Figure 11 shows the Auto-reload mode. Also two options in this mode are selected by the EXEN2 bit in T2CON:

- If EXEN2 = 0, then when Timer 2 rolls over, it sets the TF2 bit but also causes the Timer 2 registers to be reloaded with the 16-bit value held in registers RCAP2L and RCAP2H. The 16-bit value held in these registers is preset by software.
- If EXEN2 = 1, Timer 2 operates as described above but with the additional feature that a HIGH-to-LOW transition at external input T2EX will also trigger the 16-bit reload and set the EXF2 bit.

11.2.3 BAUD RATE GENERATOR MODE

The Baud Rate Generator mode is selected when RTCLK = 1. It will be described in conjunction with the serial port (UART); see Section 16.3.2.

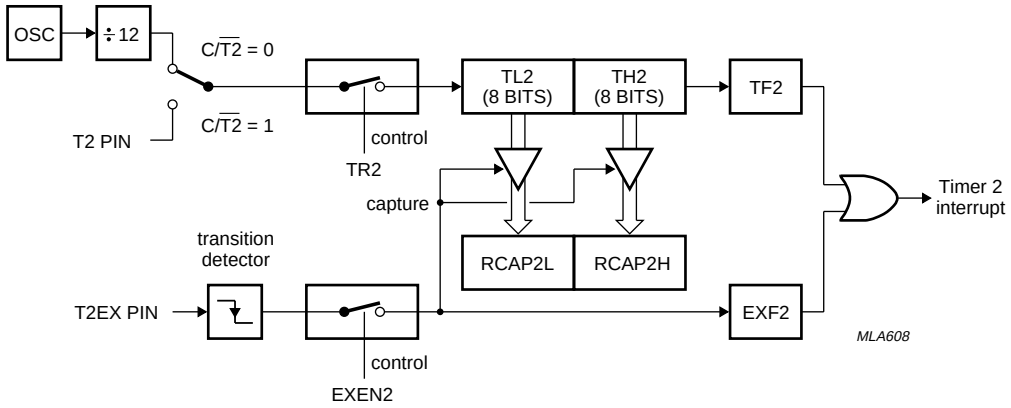


Fig.10 Timer 2 in Capture mode.

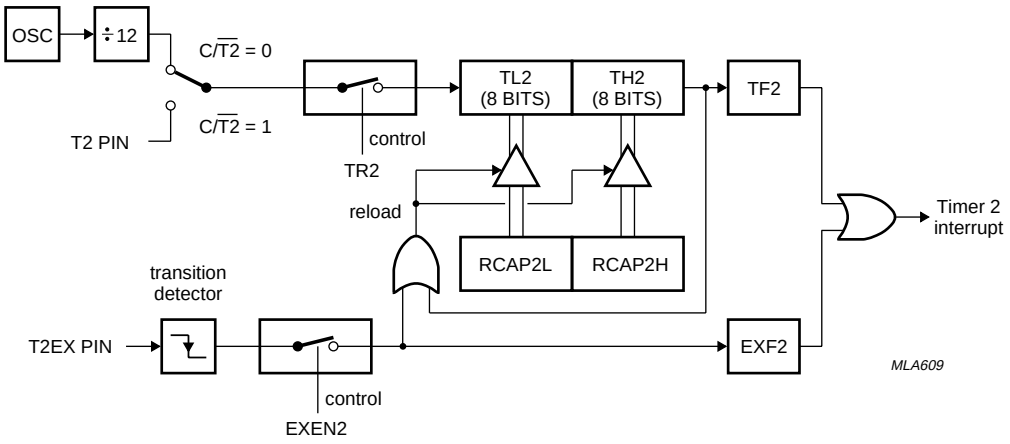


Fig.11 Timer 2 in Auto-Reload mode.

11.3 Timer/Counter 2 Control Register (T2CON)

Table 2 Timer/Counter 2 Control Register (SFR address C8H)

7	6	5	4	3	2	1	0
TF2	EXF2	GF2	RTCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Table 3 Description of T2CON bits.

BIT	SYMBOL	DESCRIPTION
7	TF2	**Timer 2 overflow flag**. Set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when RTCLK = 1.
6	EXF2	**Timer 2 external flag.** Set when either a capture or reload is caused by a negative transition on T2EX and when EXEN2 = 1. When Timer T2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to Timer 2 interrupt routine. EXF2 must be cleared by software.
5	GF2	**General purpose flag** bit.
4	RTCLK	**Receive/transmit clock flag**. When set, causes the UART serial port to use Timer 2 overflow pulses for its receive and transmit clock in Modes 1 and 3. RTCLK = 0 causes Timer 1 overflows to be used for the receive and transmit clock.
3	EXEN2	**Timer 2 external enable flag**. When set, allows a capture or reload to occur as a result of a negative transition on T2EX, if Timer 2 is not being used to clock the serial port. EXEN2 = 0, causes Timer 2 to ignore events at T2EX.
2	TR2	**Start/stop control for Timer 2**. TR2 = 1 starts the timer.
1	C/$\overline{T2}$	**Timer or counter select for Timer 2**. C/$\overline{T2}$ = 0 selects the internal timer with a clock frequency of $^1/_{12} \times f_{osc}$. C/$\overline{T2}$ = 1 selects the external event counter; negative edge triggered.
0	CP/$\overline{RL2}$	**Capture/Reload flag**. When set, captures will occur on negative transitions at T2EX, if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When RTCLK = 1, this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

Table 4 Timer 2 operating modes; X = don't care.

RTCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud Rate Generator
X	X	0	Off

11.4 Watchdog Timer

In addition to Timer T2 and the standard timers, a Watchdog Timer (consisting of an 11-bit prescaler and an 8-bit timer) is also incorporated.

The Watchdog Timer is controlled by the Watchdog Enable pin ($\overline{EWN}$). When $\overline{EWN}$ = 0, the timer is enabled and the Power-down mode is disabled. When $\overline{EWN}$ = 1, the timer is disabled and the Power-down mode is enabled. In the Idle mode the Watchdog Timer and reset circuitry remain active.

The Watchdog Timer is shown in Fig. 12.

The timer frequency is derived from the oscillator frequency using the following formula:

$$f_{timer} = \frac{f_{osc}}{(12 \times 2048)}$$

When a timer overflow occurs, the microcontroller is reset and a reset output pulse is generated at the RST pin. To prevent a system reset the timer must be reloaded in time by the application software. If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The Watchdog Timer can only be reloaded if the condition flag WLE (PCON.4) has been previously set by software. At the moment the counter is loaded the condition flag is automatically cleared.

The time interval between the timer reloading and the occurrence of a reset is dependent upon the reloaded value. For example, this time period may range from 2 ms to 500 ms when using an oscillator frequency f_{osc} = 12 MHz.

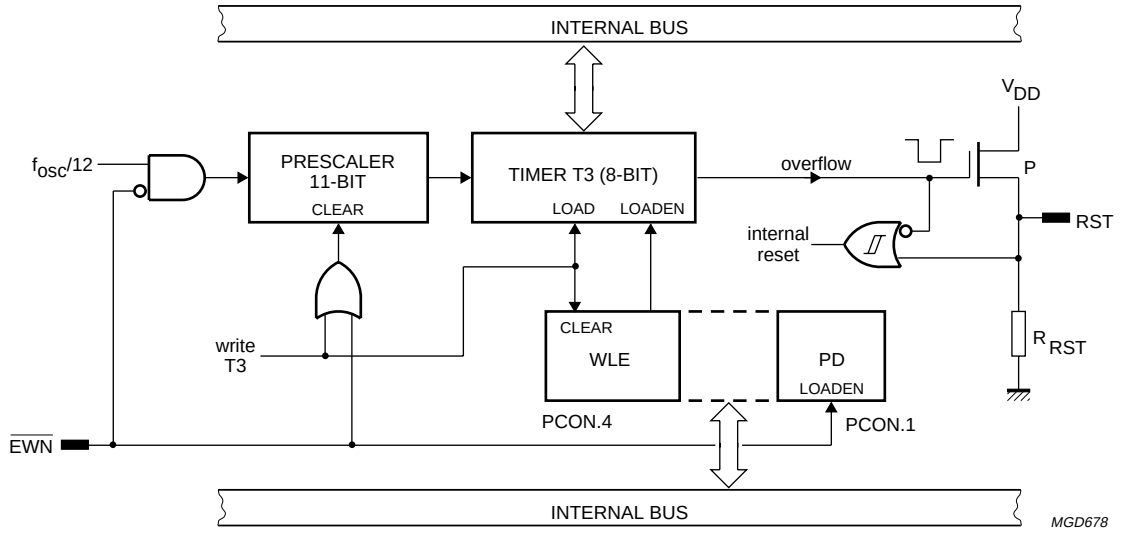


Fig.12 Functional diagram of the T3 Watchdog Timer.

12 PULSE WIDTH MODULATED OUTPUT

One Pulse Width Modulated output channel ($\overline{PWM0}$) is provided which outputs pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler (PWMP) that generates the clock for the counter. The 8-bit counter counts modulo 255, i.e. from 0 to 254 inclusive. The value held in the 8-bit counter is compared to the contents of the register PWM0.

Provided the contents of this register are greater than the counter value, the $\overline{PWM0}$ output is set LOW. If the contents of register $\overline{PWM0}$ are equal to, or less than the counter value, the $\overline{PWM0}$ output is set HIGH.
The pulse-width-ratio is therefore defined by the contents of register PWM0. The pulse-width-ratio will be in the range 0 to $^{255}/_{255}$ and may be programmed in increments of $^{1}/_{255}$.

The repetition frequency (f_{PWM}) at the $\overline{PWM0}$ output is given by:

$$f_{PWM} = \frac{f_{osc}}{\{2 \times (1 + PWMP) \times 255\}}$$

For f_{osc} = 12 MHz the above formula gives a repetition frequency range of 92 Hz to 23.5 kHz.

By loading the PWM0 register with either 00H or FFH, the $\overline{PWM0}$ output can be retained at a constant HIGH or LOW level respectively. When loading FFH into the PWM0 register, the 8-bit counter will never actually reach this value.

The $\overline{PWM0}$ output pin is driven by push-pull drivers and is not shared with any other function.

12.1 Prescaler Frequency Control Register (PWMP)

Table 5 Prescaler Frequency Control Register (address FEH)

7	6	5	4	3	2	1	0
PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Table 6 Description of PWMP bits

BIT	SYMBOL	DESCRIPTION
7 to 1	PWMP.7 to PWMP.0	Prescaler division factor = (PWMP) + 1.

12.2 Pulse Width Register (PWM0)

Table 7 Pulse Width Register (address FCH)

7	6	5	4	3	2	1	0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Table 8 Description of PWM0 bits

BIT	SYMBOL	DESCRIPTION
7 to 1	PWM0.7 to PWM0.0	LOW/HIGH ratio of $\overline{PWM0}$ signal $= \frac{(PWM0)}{\{255 - (PWM0)\}}$

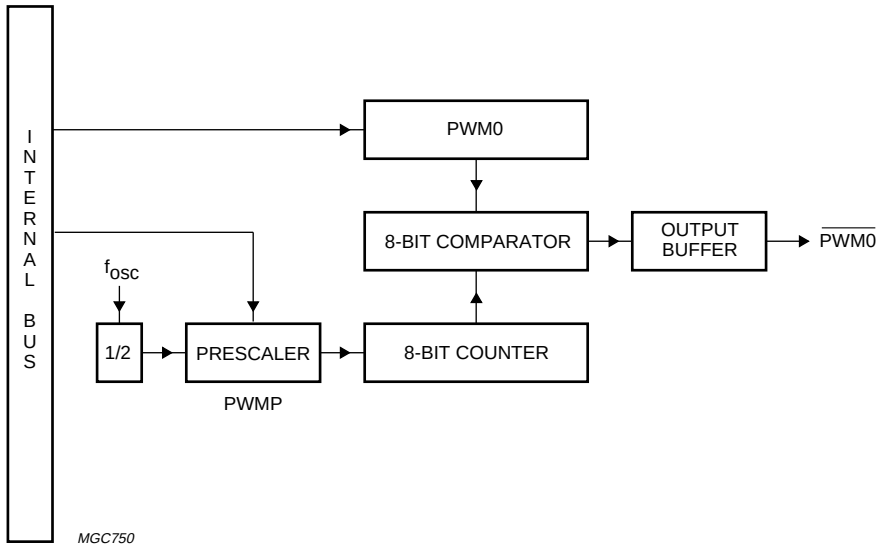


Fig.13 Functional diagram of Pulse Width Modulated output ($\overline{PWM0}$).

13 ANALOG-TO-DIGITAL CONVERTER (ADC)

The analog input circuitry consists of a 4-bit analog multiplexer and an ADC with 8-bit resolution. The analog reference voltage ($V_{ref(p)(A)}$) and analog ground (V_{SSA}) are connected via separate input pins. The conversion is selectable from 24 machine cycles (24 µs at f_{osc} = 12 MHz) to 48 machine cycles. The functional diagram of the ADC is shown in Fig. 14.

The ADC is controlled using the ADC Control Register (ADCON). Input channels are selected by the analog multiplexer via the ADCON register bits AADR0 and AADR1. The completion of the 8-bit ADC conversion is flagged by ADCI in the ADCON register and the result is stored in the Special Function Register ADCH (address C5H).

An ADC conversion in progress is unaffected by an external software ADC start.

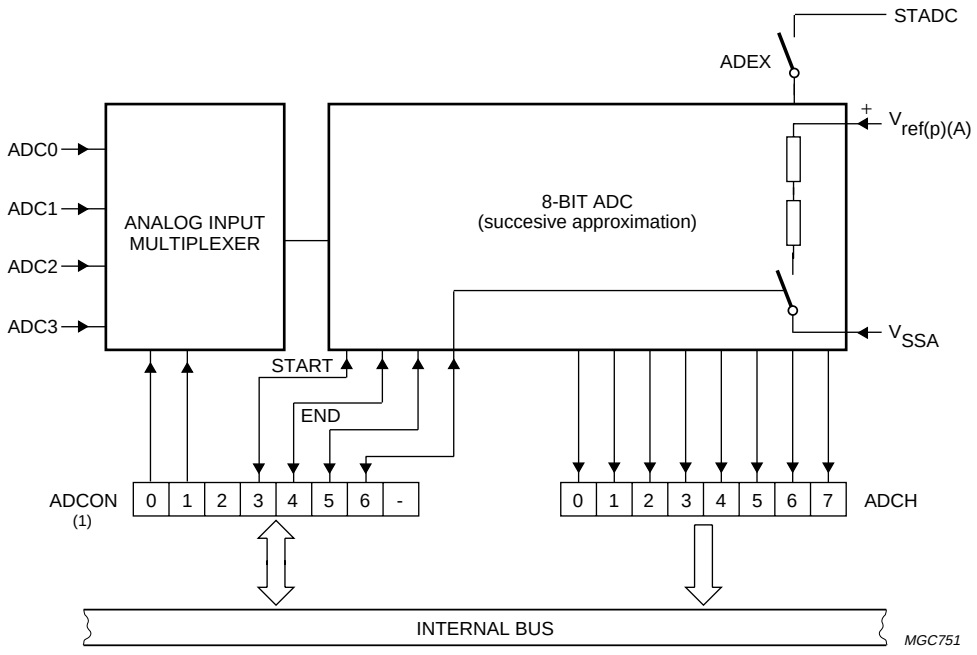
The result of a completed conversion remains unaffected provided ADCI = 1. While ADCS = 1 or ADCI = 1, a new ADC start will be blocked and consequently lost.

An ADC conversion already in progress is aborted when the Power-down mode is entered. The result of a completed conversion (ADCI = 1) remains unaffected when entering the Idle or Power-down mode.

The analog-to-digital conversion can be started in 3 ways:

- Start in operating mode, continue in operating mode
- Start in operating mode, by setting the ADCS bit, then go to Idle mode
- Set the ADEX bit, go to the Idle mode and start conversion externally via the STADC pin.

For the three cases mentioned above the internal flag ADCI is set upon completion of the conversion.



(1) For the descriptions of ADCON bits see Table 10.

Fig.14 Functional diagram of analog input.

13.1 ADC Control Register (ADCON)

Table 9 ADC Control Register (address C4H)

7	6	5	4	3	2	1	0
–	ADPD	ADEX	ADCI	ADCS	CKDIV	AADR1	AADR0

Table 10 Description of ADCON bits

BIT	SYMBOL	DESCRIPTION
7	–	Reserved.
6	ADPD	**Power-down.** This bit switches off the resistor reference to save power even when the CPU is operating.
5	ADEX	**Enable external start of conversion**. This bit determines whether a conversion can be started using the external pin STADC. When ADEX = 0, a conversion cannot be started externally using STADC. When ADEX = 1, a conversion can be started externally using STADC.
4	ADCI	**ADC interrupt flag**. This flag is set when an ADC conversion result is ready to be read. An interrupt is invoked if this is enabled. This flag must be cleared by software (it cannot be set by software); see Table 11.
3	ADCS	**ADC start and status flag**. When this bit is set an ADC conversion is started. ADCS may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion ADCS is reset and after that the interrupt flag ADCI is set. ADCS cannot be reset by software; see Table 11.
2	CKDIV	This bit selects the conversion time, in terms of instruction cycles. This allows the CPU to be run at the maximum frequency (12 MHz) yet keeping the ADC timing at low frequency. When CKDIV = 0, the conversion time is equivalent to 24 instruction cycles. When CKDIV = 1, the conversion time is equivalent to 48 instruction cycles. The conversion time includes a sampling time of 6 cycles.
1	AADR1	**Analog input select**. These bits are used to select one of the four analog inputs; see Table 12. They only can be changed when ADCI and ADCS are both LOW.
0	AADR0	

Table 11 Analog-to-digital operation

ADCI	ADCS	OPERATION
0	0	ADC not busy; a conversion can be started.
0	1	ADC busy; start of a new conversion is blocked.
1	0	Conversion completed; start of a new conversion is blocked.
1	1	Intermediate status for a maximum of one machine cycle before conversion is completed (ADCI = 1, ADCS = 0).

Table 12 Selection of analog input channel

AADR1	AADR0	SELECTED CHANNEL
0	0	AD0
0	1	AD1
1	0	AD2
1	1	AD3

14 REDUCED POWER MODES

There are two software selectable modes of reduced activity for further power reduction: Idle and Power-down.

14.1 Idle mode

Idle mode operation permits the interrupt, serial ports, timer blocks, PWM and ADC to continue to function while the clock to the CPU is halted.

Idle mode is entered by setting the IDL bit in the Power Control Register (PCON.0, see Table 14). The instruction that sets IDL is the last instruction executed in the normal operating mode before the Idle mode is activated

Once in Idle mode, the CPU status is preserved along with the Stack Pointer, Program Counter, Program Status Word and Accumulator. The RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 13.

The following functions remain active during the Idle mode:

- Timer 0, Timer 1, Timer 2 and Timer 3
- UART, I²C-bus interface
- External interrupt
- $\overline{\text{PWM0}}$ (reset; output = HIGH)
- ADC.

These functions may generate an interrupt or reset; thus ending the Idle mode.

There are two ways to terminate the Idle mode:

1. Activation of any enabled interrupt will cause IDL (PCON.0) to be cleared by hardware thus terminating the Idle mode. The interrupt is serviced, and following the RETI instruction, the next instruction to be executed will be the one following the instruction that put the device in the Idle mode. The flag bits GF0 (PCON.2) and GF1 (PCON.3) may be used to determine whether the interrupt was received during normal execution or during the Idle mode.
   For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When the Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
2. The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T2. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation. Reset redefines all SFRs but does not affect the on-chip RAM.

14.2 Power-down mode

Operation in Power-down mode freezes the oscillator. The internal connections which link both Idle and Power-down signals to the clock generation circuit are shown in Fig.15.

Power-down mode is entered by setting the PD bit in the Power Control Register (PCON.1, see Table 14).
The instruction that sets PD is the last executed prior to going into the Power-down mode.

Once in the Power-down mode, the oscillator is stopped. The contents of the on-chip RAM and the SFRs are preserved. The port pins output the value held by their respective SFRs. ALE and $\overline{\text{PSEN}}$ are held LOW.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The supply voltage must not be reduced until the Power-down mode is entered, and must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

14.3 Wake-up from Power-down mode

When in Power-down mode the controller can be woken-up with either the external interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT8}}$, or a reset operation. The wake-up operation has two basic approaches as explained in Section 14.3.1; 14.3.2 and illustrated in Fig.16.

14.3.1 WAKE-UP USING $\overline{\text{INT2}}$ TO $\overline{\text{INT8}}$

If any of the interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT8}}$ are enabled, the device can be woken-up from the Power-down mode with the external interrupts. To ensure that the oscillator is stable before the controller restarts, the internal clock will remain inactive for 1536 oscillator periods. This is controlled by an on-chip delay counter.

14.3.2 WAKE-UP USING RST

To wake-up the P8xCL580, the RST pin must be kept HIGH for a minimum of 24 periods. The on-chip delay counter is inactive. The user must ensure that the oscillator is stable before any operation is attempted.

14.4 Status of external pins

The status of the external pins during Idle and Power-down mode is shown in Table 13. If the Power-down mode is activated whilst accessing external Program Memory, the port data that is held in the Special Function Register P2 is restored to Port 2.

If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor ‘p1’; see Fig.9(a).

Table 13 Status of external pins during Idle and Power-down modes

MODE	MEMORY	ALE	$\overline{\text{PSEN}}$	$\overline{\text{PWM0}}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4
Idle	internal	1	1	active	port data	port data	port data	port data	port data
	external	1	1	active	floating	port data	address	port data	port data
Power-down	internal	0	0	HIGH	port data	port data	port data	port data	port data
	external	0	0	HIGH	floating	port data	port data	port data	port data

14.5 Power Control Register (PCON)

Idle and Power-down modes are activated by software using this SFR. PCON is not bit addressable, the reset value of PCON is 0XX00000B.

Table 14 Power Control Register (address 87H)

7	6	5	4	3	2	1	0
SMOD	–	–	WLE	GF1	GF0	PD	IDL

Table 15 Description of PCON bits

BIT	SYMBOL	DESCRIPTION
7	SMOD	**Double Baud rate bit**. When set to a logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3.
6 and 5	–	Reserved.
4	WLE	**Watchdog Load Enable**. This flag must be set by software prior to loading the Watchdog Timer (T3). It is cleared when T3 is loaded.
3 and 2	GF1 and GF0	**General purpose flag bits**.
1	PD	**Power-down bit**. Setting this bit activates the Power-down mode. This bit can only be set if input $\overline{\text{EWN}}$ is HIGH. If a logic 1 is written to both PD and IDL at the same time, PD takes precedence.
0	IDL	**Idle mode bit**. Setting this bit activates the Idle mode.

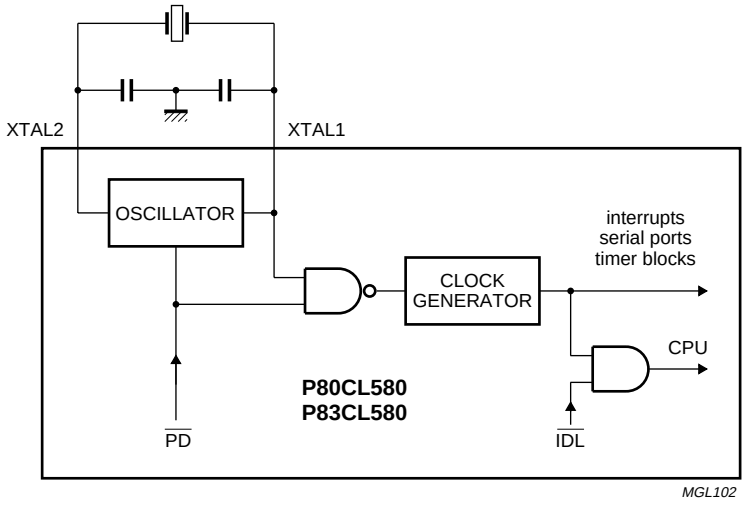


Fig.15 Internal clock control in Idle and Power-down modes.

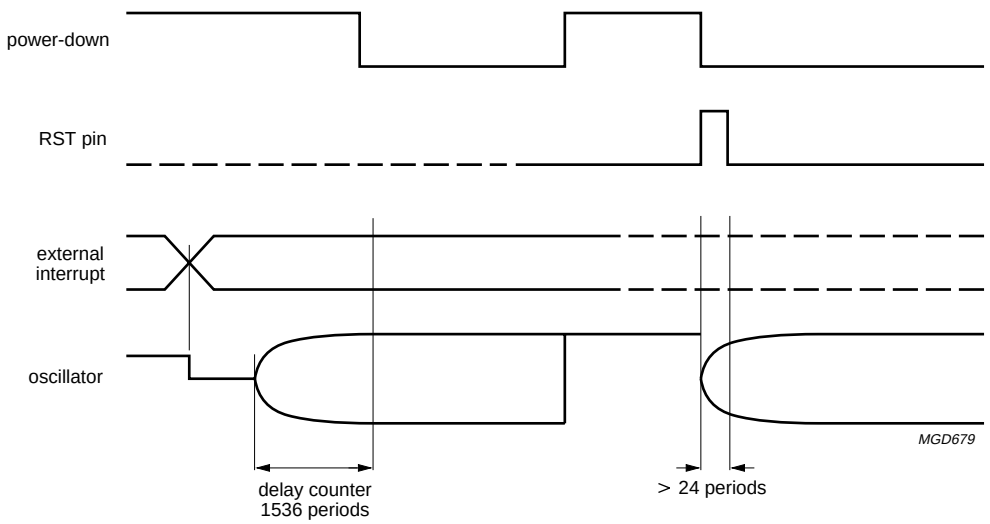


Fig.16 Wake-up operation.

15 I²C-BUS SERIAL I/O

The serial port supports the twin line I²C-bus, which consists of a serial data line (SDA) and a serial clock line (SCL). These lines also function as the I/O port lines P1.7 and P1.6 respectively.

The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

The I²C-bus serial I/O has complete autonomy in byte handling and operates in 4 modes:

- Master transmitter
- Master receiver
- Slave transmitter
- Slave receiver.

These functions are controlled by the Serial Control Register S1CON. S1STA is the Status Register whose contents may also be used as a vector to various service routines. S1DAT is the Data Shift Register and S1ADR is the Slave Address Register. Slave address recognition is performed by on-chip hardware.

Figure 17 is the block diagram of the I²C-bus serial I/O.

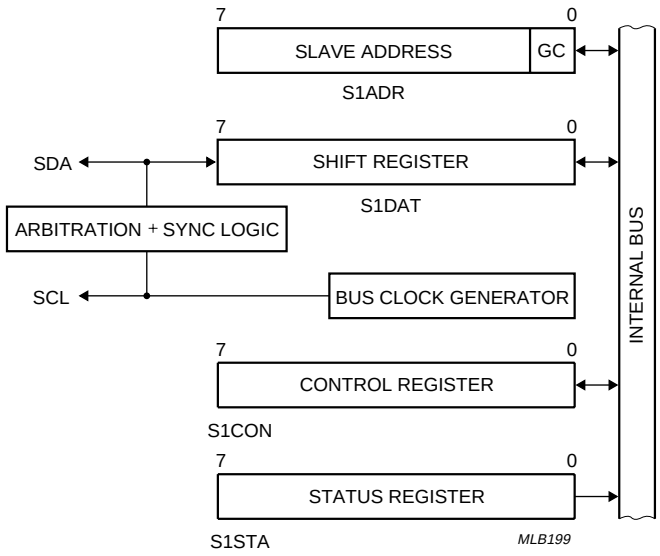


Fig.17 Block diagram of I²C-bus serial I/O.

15.1 Serial Control Register (S1CON)

Table 16 Serial Control Register (SFR address D8H)

7	6	5	4	3	2	1	0
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Table 17 Description of S1CON bits

BIT	SYMBOL	DESCRIPTION
7	CR2	This bit along with bits CR1 (S1CON.1) and CR0 (S1CON.0) determines the serial clock frequency when SIO is in the Master mode. See Table 18.
6	ENS1	**ENABLE serial I/O**. When ENS1 = 0, the serial I/O is disabled. SDA and SCL outputs are in the high impedance state; P1.6 and P1.7 function as open-drain ports. When ENS1 = 1, the serial I/O is enabled. Output port latches P1.6 and P1.7 must be set to logic 1.
5	STA	**START flag**. When this bit is set in Slave mode, the SIO hardware checks the status of the I²C-bus and generates a START condition if the bus is free or after the bus becomes free. If STA is set while the SIO is in Master mode, SIO will generate a repeated START condition.
4	STO	**STOP flag**. With this bit set while in Master mode a STOP condition is generated. When a STOP condition is detected on the I²C-bus, the SIO hardware clears the STO flag. STO may also be set in Slave mode in order to recover from an error condition. In this case no STOP condition is transmitted to the I²C-bus. However, the SIO hardware behaves as if a STOP condition has been received and releases the SDA and SCL. The SIO then switches to the not addressed slave receiver mode. The STOP flag is cleared by the hardware.
3	SI	**SIO interrupt flag**. This flag is set, and an interrupt is generated, after any of the following events occur: • A start condition is generated in Master mode • Own slave address has been received during AA = 1 • The general call address has been received while GC (S1ADR.0) = 1 and AA = 1 • A data byte has been received or transmitted in Master mode (even if arbitration is lost) • A data byte has been received or transmitted as selected slave • A Stop or Start condition is received as selected slave receiver or transmitter.
2	AA	**Assert Acknowledge**. When this bit is set, an acknowledge (low level to SDA) is returned during the acknowledge clock pulse on the SCL line when: • Own slave address is received • General call address is received; GC (S1ADR.0) = 1 • A data byte is received while the device is programmed to be a Master Receiver • A data byte is received while the device is a selected Slave Receiver. When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own slave address or general call address is received.
1	CR1	These two bits along with the CR2 (S1CON.7) bit determine the serial clock frequency when SIO is in the Master mode. See Table 18.
0	CR0	

Table 18 Selection of the serial clock frequency SCL in a Master mode of operation

CR2	CR1	CR0	f_{osc} DIVISOR	BIT RATE(kHz) AT f_{osc}		
				3.58 MHz	6 MHz	12 MHz
0	0	0	256	14.0	23.4	46.9
0	0	1	224	16.0	26.8	53.6
0	1	0	192	18.6	31.3	62.5
0	1	1	160	22.4	37.5	75.0
1	0	0	960	3.73	6.25	12.5
1	0	1	120	29.8	50.0	100.0
1	1	0	60	59.7	100.0	–
1	1	1	not allowed	–	–	–

15.2 Serial Status Register (S1STA)

S1STA is a read-only register.The contents of this register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus. The status codes for all possible modes of the I²C-bus interface are given in Tables 21 to 25.

Table 19 Serial Status Register (address D9H)

7	6	5	4	3	2	1	0
SC4	SC3	SC2	SC1	SC0	0	0	0

Table 20 Description of S1STA bits

BIT	SYMBOL	DESCRIPTION
3 to 7	SC4 to SC0	5-bit status code.
0 to 2	–	These three bits are always zero.

Table 21 MST/TRX mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
18H	SLA and W have been transmitted, ACK has been received.
20H	SLA and W have been transmitted, $\overline{\text{ACK}}$ received.
28H	DATA of S1DAT has been transmitted, ACK received.
30H	DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received.
38H	Arbitration lost in SLA, R/W or DATA.

Table 22 MST/REC mode

S1STA VALUE	DESCRIPTION
08H	A START condition has been transmitted.
10H	A repeated START condition has been transmitted.
38H	Arbitration lost while returning $\overline{ACK}$.
40H	SLA and R have been transmitted, ACK received.
48H	SLA and R have been transmitted, $\overline{ACK}$ received.
50H	DATA has been received, ACK returned.
58H	DATA has been received, $\overline{ACK}$ returned.

Table 23 SLV/REC mode

S1STA VALUE	DESCRIPTION
60H	Own SLA and W have been received, ACK returned.
68H	Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned.
70H	General CALL has been received, ACK returned.
78H	Arbitration lost in SLA, R/W as MST. General CALL has been received.
80H	Previously addressed with own SLA. DATA byte received, ACK returned.
88H	Previously addressed with own SLA. DATA byte received, $\overline{ACK}$ returned.
90H	Previously addressed with general CALL. DATA byte has been received, ACK has been returned.
98H	Previously addressed with general CALL. DATA byte has been received, $\overline{ACK}$ has been returned.
A0H	A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

Table 24 SLV/TRX mode

S1STA VALUE	DESCRIPTION
A8H	Own SLA and R have been received, ACK returned.
B0H	Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned.
B8H	DATA byte has been transmitted, ACK received.
C0H	DATA byte has been transmitted, $\overline{ACK}$ received.
C8H	Last DATA byte has been transmitted (AA = 0), ACK received.

Table 25 Miscellaneous.

S1STA VALUE	DESCRIPTION
00H	Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition.
F8H	No relevant state information available, SI = 0.

Table 26 Symbols used in Tables 21 to 25

SYMBOL	DESCRIPTION
SLA	7-bit slave address
R	Read bit
W	Write bit
ACK	Acknowledgement (acknowledge bit is logic 0)
$\overline{\text{ACK}}$	No acknowledgement (acknowledge bit is logic 1)
DATA	8-bit data byte to or from I²C-bus
MST	Master
SLV	Slave
TRX	Transmitter
REC	Receiver

15.3 Data Shift Register (S1DAT)

S1DAT contains the serial data to be transmitted or data which has just been received. The MSB (bit 7) is transmitted or received first; i.e. data shifted from right to left.

Table 27 Data Shift Register (SFR address DAH)

7	6	5	4	3	2	1	0
S1DAT.7	S1DAT.6	S1DAT.5	S1DAT.4	S1DAT.3	S1DAT.2	S1DAT.1	S1DAT.0

15.4 Address Register (S1ADR)

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter.

Table 28 Address Register (SFR address DBH)

7	6	5	4	3	2	1	0
SLA6	SLA5	SLA4	SLA3	SLA2	SLA1	SLA0	GC

Table 29 Description of S1ADR bits

BIT	SYMBOL	DESCRIPTION
7 to 1	SLA6 to SLA0	Own slave address.
0	GC	This bit is used to determine whether the general call address is recognized. When GC = 0, the general call address is not recognized; when GC = 1, the general call address is recognized.

16 STANDARD SERIAL INTERFACE SIO0: UART

This serial port is full duplex which means that it can transmit and receive simultaneously. It is also receive-buffered and can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte has not been read by the time the reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed via the Special Function Register S0BUF. Writing to S0BUF loads the transmit register and reading S0BUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0 Serial data enters and exits through RXD. TXD outputs the shift clock. Eight bits are transmitted/received (LSB first). The baud rate is fixed at $\frac{1}{12} \times f_{osc}$. See Figs 19 and 20.

Mode 1 10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). On receive, the stop bit goes into RB8 in Special Function Register S0CON. The baud rate is variable. See Figs 21 and 22.

Mode 2 11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of a logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in S0CON, while the stop bit is ignored. The baud rate is programmable to either $\frac{1}{32}$ or $\frac{1}{64} \times f_{osc}$. See Figs 23 and 24.

Mode 3 11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable. See Figs 25 and 26.

In all four modes, transmission is initiated by any instruction that uses S0BUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

16.1 Multiprocessor communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th bit goes into RB8. The following bit is the stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated, but only if RB8 = 1. This feature is enabled by setting bit SM2 in S0CON. One use of this feature, in multiprocessor systems, is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is HIGH in an address byte and LOW in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be sent. The slaves that were not being addressed leave their SM2 bits set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

16.2 Serial Port Control and Status Register (S0CON)

The Serial Port Control and Status Register is the Special Function Register S0CON. The register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Table 30 Serial Port Control Register (address 98H)

7	6	5	4	3	2	1	0
SMO	SM1	SM2	REN	TB8	RB8	TI	RI

Table 31 Description of S0CON bits

BIT	SYMBOL	DESCRIPTION
7	SM0	These bits are used to select the serial port mode; see Table 32.
6	SM1	
5	SM2	Enables the multiprocessor communication feature in Modes 2 and 3. In these modes, if SM2 = 1, then RI will not be activated if the received 9th data bit (RB8) is a logic 0. In Mode 1, if SM2 = 1, then RI will not be activated unless a valid stop bit was received. In Mode 0, SM2 should be a logic 0.
4	REN	Enables serial reception and is set by software to enable reception, and cleared by software to disable reception.
3	TB8	Is the 9th data bit that will be transmitted in Modes 2 and 3. Set or cleared by software as desired.
2	RB8	In Modes 2 and 3, is the 9th data bit received. In Mode 1, if SM2 = 0 then RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
1	TI	**The transmit interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit time in the other modes, in any serial transmission. Must be cleared by software.
0	RI	**The receive interrupt flag**. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial transmission (except see SM2). Must be cleared by software.

Table 32 Selection of the serial port modes

SMO	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	Mode 0	Shift register	$1/12 \times f_{osc}$
0	1	Mode 1	8-bit UART	variable
1	0	Mode 2	9-bit UART	$1/32$ or $1/64 \times f_{osc}$
1	1	Mode 3	9-bit UART	variable

16.3 Baud rates

The baud rate in Mode 0 is fixed and may be calculated as:

$$\text{Baud Rate} = \frac{f_{osc}}{12}$$

The baud rate in Mode 2 depends on the value of the SMOD bit in Special Function Register PCON and may be calculated as:

$$\text{Baud Rate} = \frac{2^{SMOD}}{64} \times f_{osc}$$

- If SMOD = 0 (value on reset), the baud rate is $1/64 \times f_{osc}$
- If SMOD = 1, the baud rate is $1/32 \times f_{osc}$

The baud rates in Modes 1 and 3 are determined by the Timer 1 or Timer 2 overflow rate.

16.3.1 Using Timer 1 to generate baud rates

When Timer 1 is used as the Baud Rate Generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD bit as follows:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \text{Timer 1 Overflow Rate.}$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either ‘timer’ or ‘counter’ operation in any of its 3 running modes. In most typical applications, it is configured for ‘timer’ operation, in the Auto-reload mode (high nibble of TMOD = 0010B). In this case the baud rate is given by the formula:

$$\text{Baud Rate} = \frac{2^{SMOD}}{32} \times \frac{f_{osc}}{\{12 \times (256 - TH1)\}}$$

By configuring Timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rates can be achieved. Table 33 lists commonly used baud rates and how they can be obtained from Timer 1.

Table 33 Commonly used baud rates generated by Timer 1

BAUD RATE(kb/s)	f_{osc} (MHz)	SMOD	C/T	TIMER 1 MODE	RELOAD VALUE
1000.0[1]	12.000	X[2]	X	X	X
375.0[3]	12.000	1	X	X	X
62.5[4]	12.000	1	0	Mode 2	FFH
19.2	11.059	1	0	Mode 2	FDH
9.6	11.059	0	0	Mode 2	FDH
4.8	11.059	0	0	Mode 2	FAH
2.4	11.059	0	0	Mode 2	F4H
1.2	11.059	0	0	Mode 2	E8H
137.5	11.986	0	0	Mode 2	1DH
110.0	6.000	0	0	Mode 2	72H
110.0	12.000	0	0	Mode 1	FEEBH

Notes

1. Maximum in Mode 0.
2. X = don’t care.
3. Maximum in Mode 2.
4. Maximum in Modes 1 and 3.

16.3.2 USING TIMER 2 TO GENERATE BAUD RATES

Timer 2 is selected as a Baud Rate Generator by setting the RTCLK bit in T2CON. The Baud Rate Generator mode is similar to the Auto-reload mode, in that a roll-over in TH2 causes Timer 2 registers to be reloaded with the 16-bit value held in the registers RCAP2H and RCAP2L, which are preset by software. Baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as specified below.

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The Timer 2 can be configured for either 'timer' or 'counter' operation. In the most typical applications, it is configured for 'timer' operation ($C/\overline{T2} = 0$). 'Timer' operation is slightly different for Timer 2 when it is being used as a Baud Rate Generator. Normally, as a timer it would increment every machine cycle at a frequency of $\frac{1}{12} \times f_{osc}$. However, as a Baud Rate Generator it increments every state time at a frequency of $\frac{1}{2} \times f_{osc}$. In this case the baud rate in Modes 1 and 3 is determined as:

$$\text{Baud Rate} = \frac{f_{osc}}{32 \times \{65536 - (\text{RCAP2H; RCAP2L})\}}$$

Where (RCAP2H; RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Baud Rate Generator mode for Timer 2 is shown in Fig.18. This figure is only valid if RTCLK = 1. At roll-over TH2 does not set the TF2 bit in T2CON and therefore, will not generate an interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the Baud Rate Generator mode. If EXEN2 is set, a HIGH-to-LOW transition on T2EX will set the EXF2 bit, also in T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2, TL2). Therefore, in this mode T2EX may be used as an additional external interrupt.

When Timer 2 is operating as a timer (TR2 = 1), in the Baud Rate Generator mode, registers TH2 and TL2 should not be accessed (read or write). Under these conditions the timer is being incremented every state time and therefore the results of a read or write may not be accurate. The registers RCAP2H and RCAP2L however, may be read but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required, Timer 2 or RCAP2H/RCAP2L should first be turned off by clearing the TR2 bit.

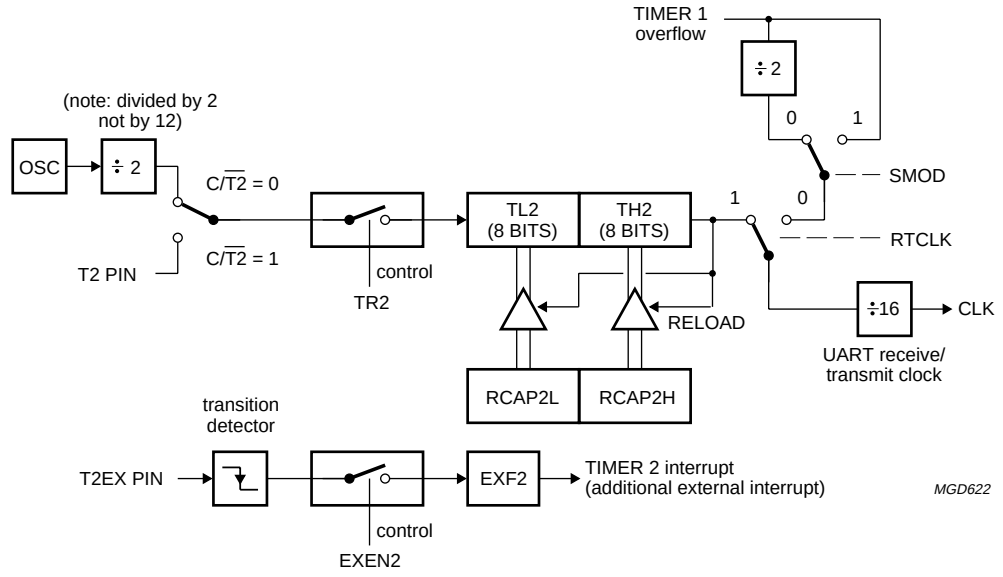


Fig.18 Timer 2 in Baud Rate Generator mode.

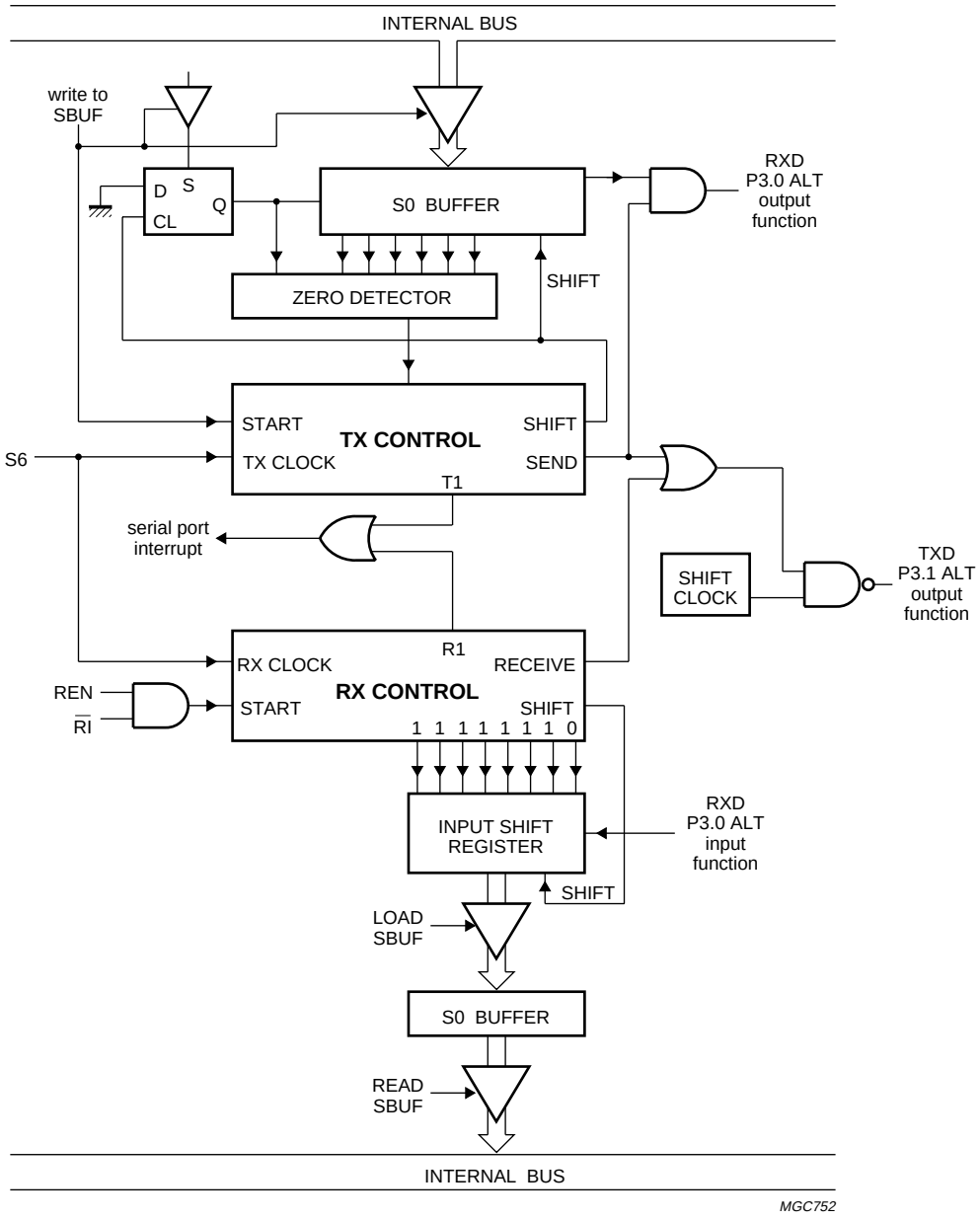


Fig.19 Serial port Mode 0.

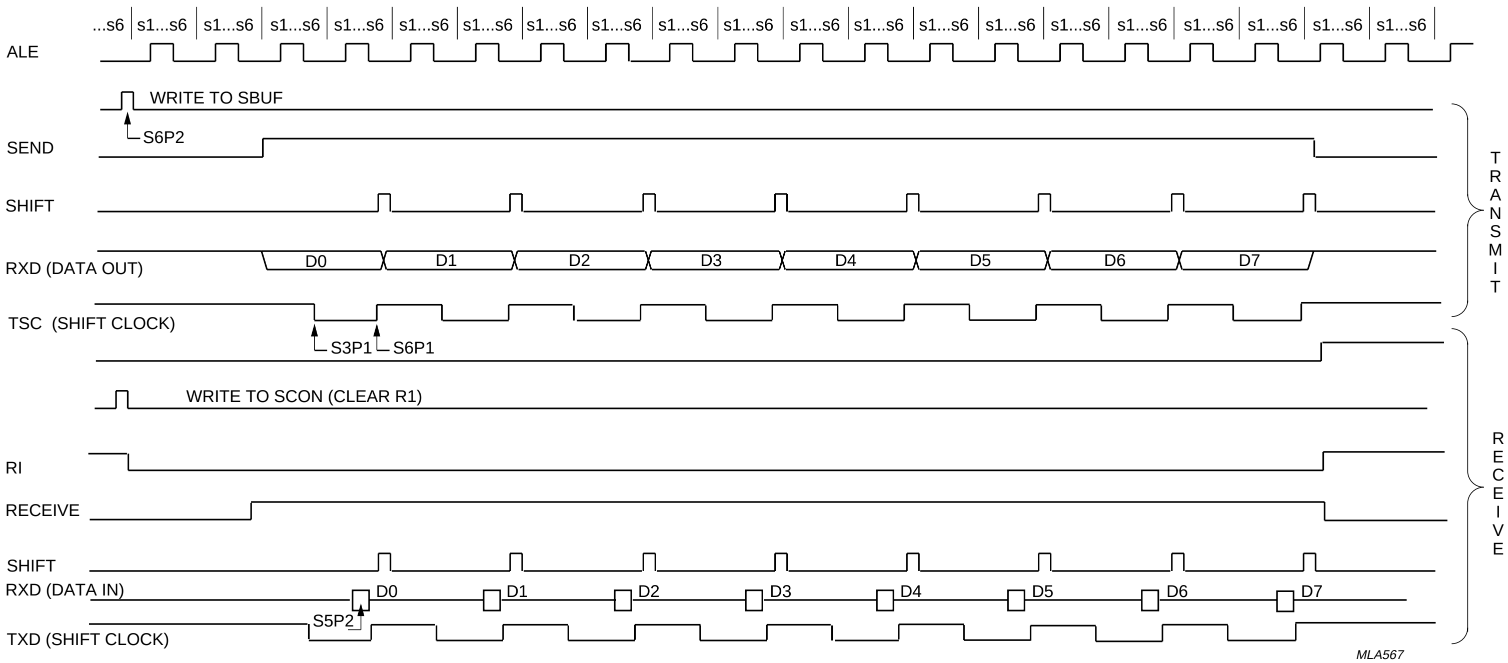


Fig.20 Serial port Mode 0 timing.

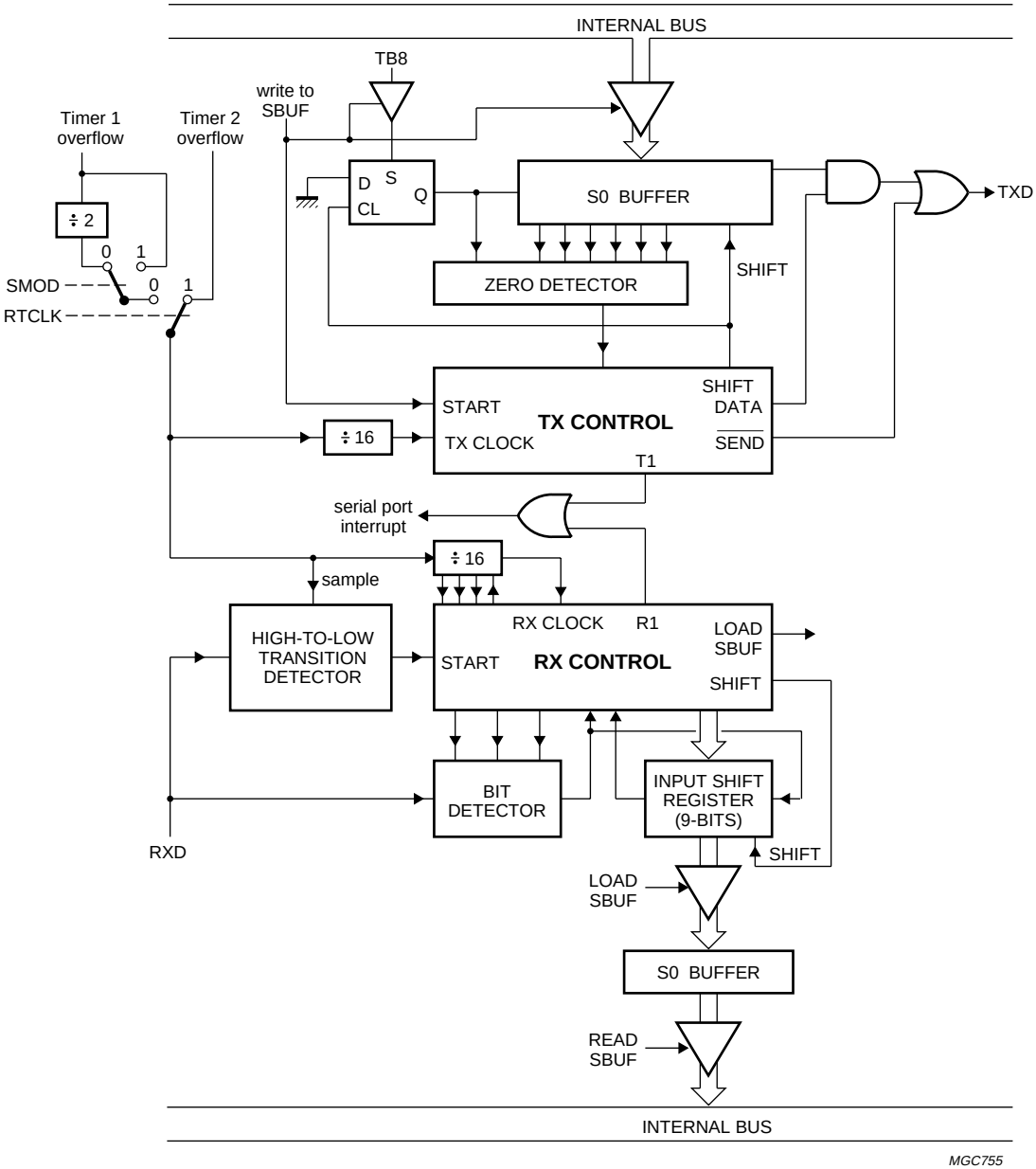


Fig.21 Serial port Mode 1.

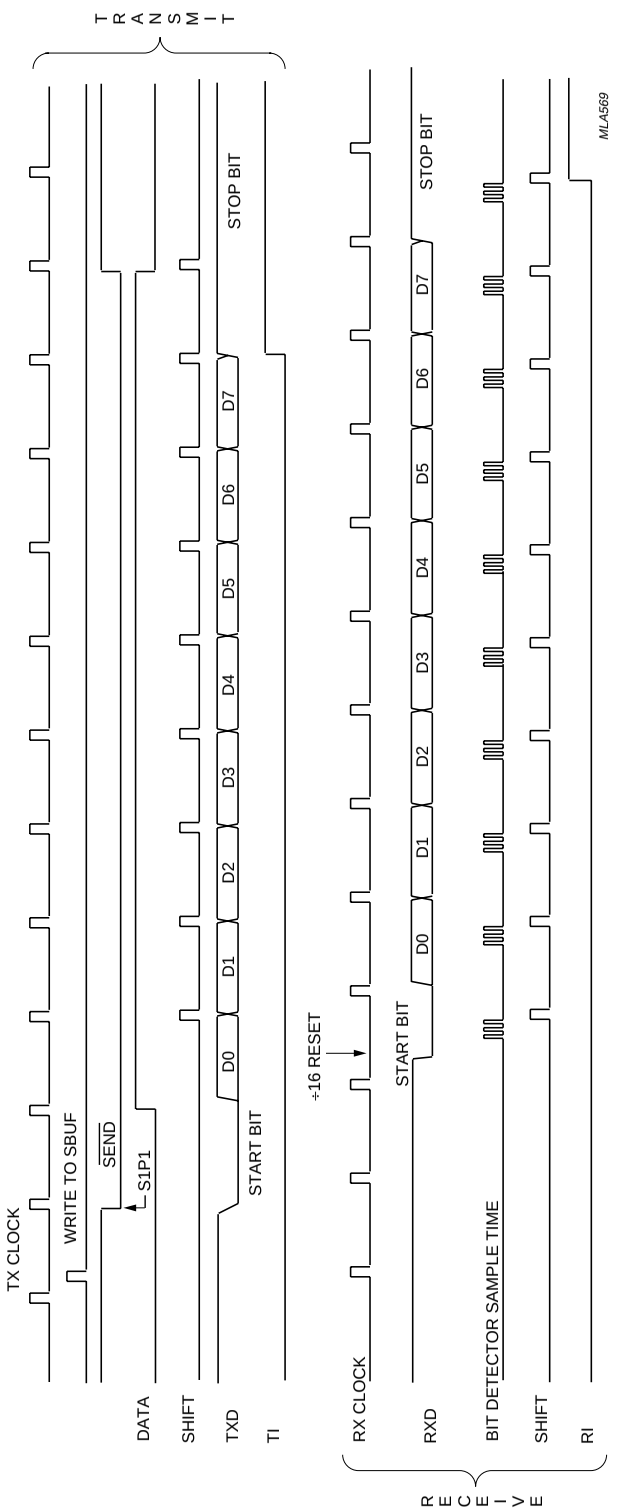


Fig.22 Serial port Mode 1 timing.

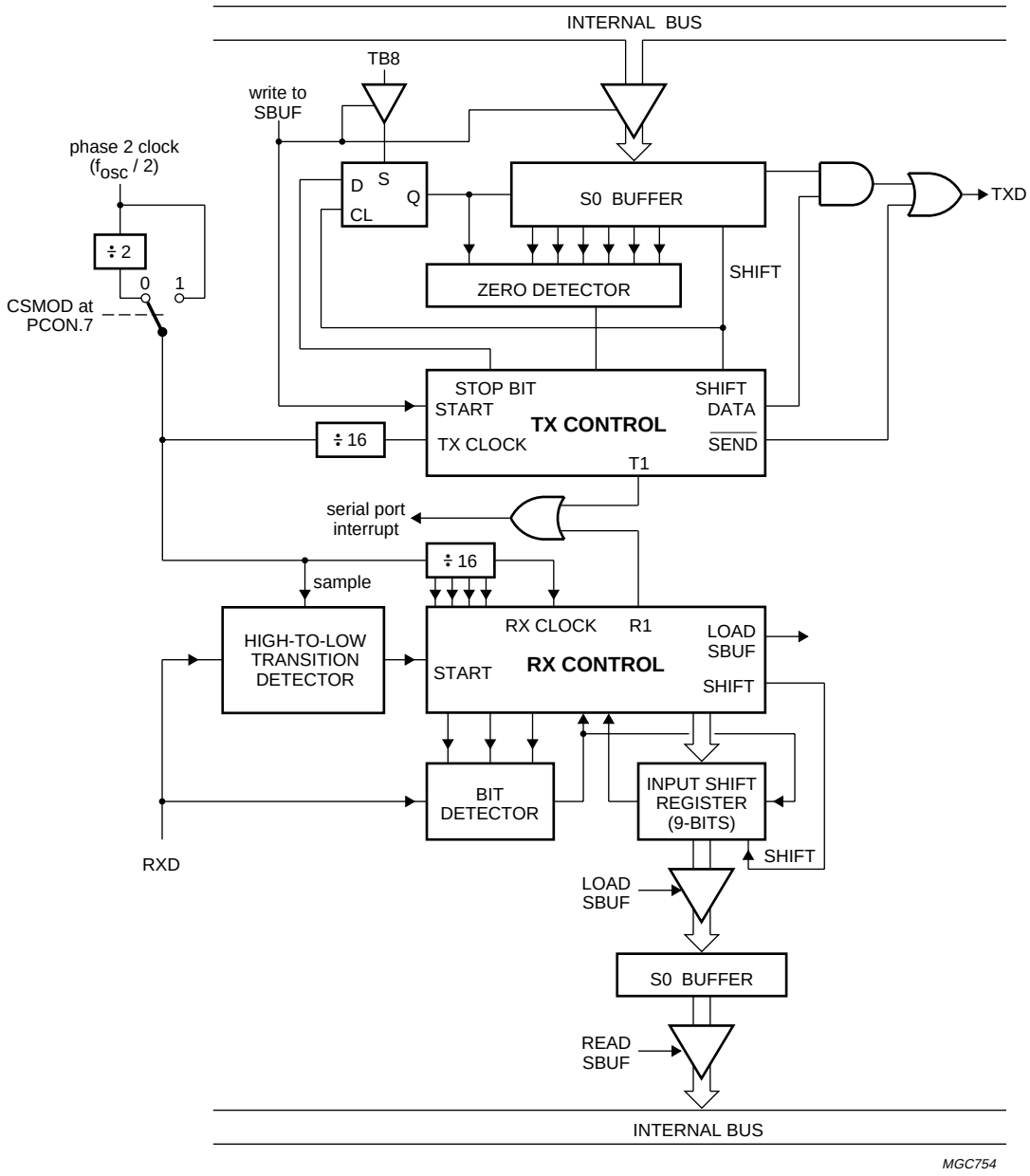


Fig.23 Serial port Mode 2.

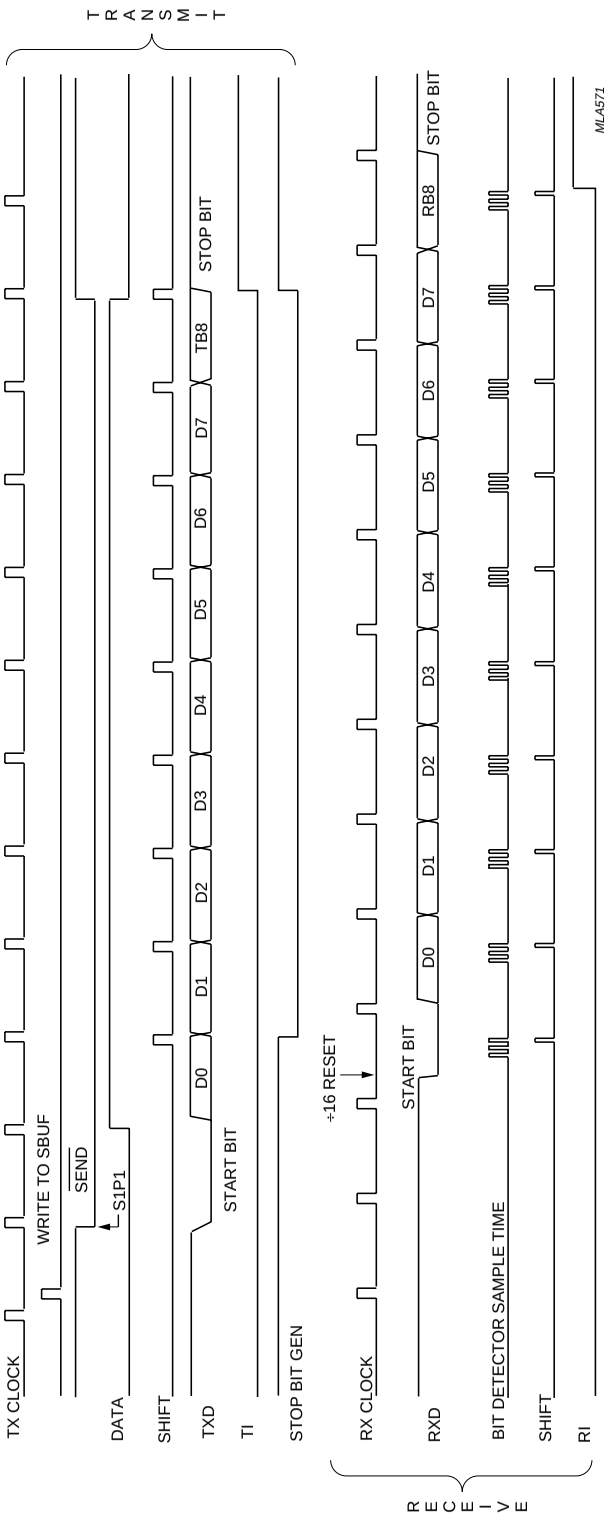


Fig.24 Serial port Mode 2 timing.

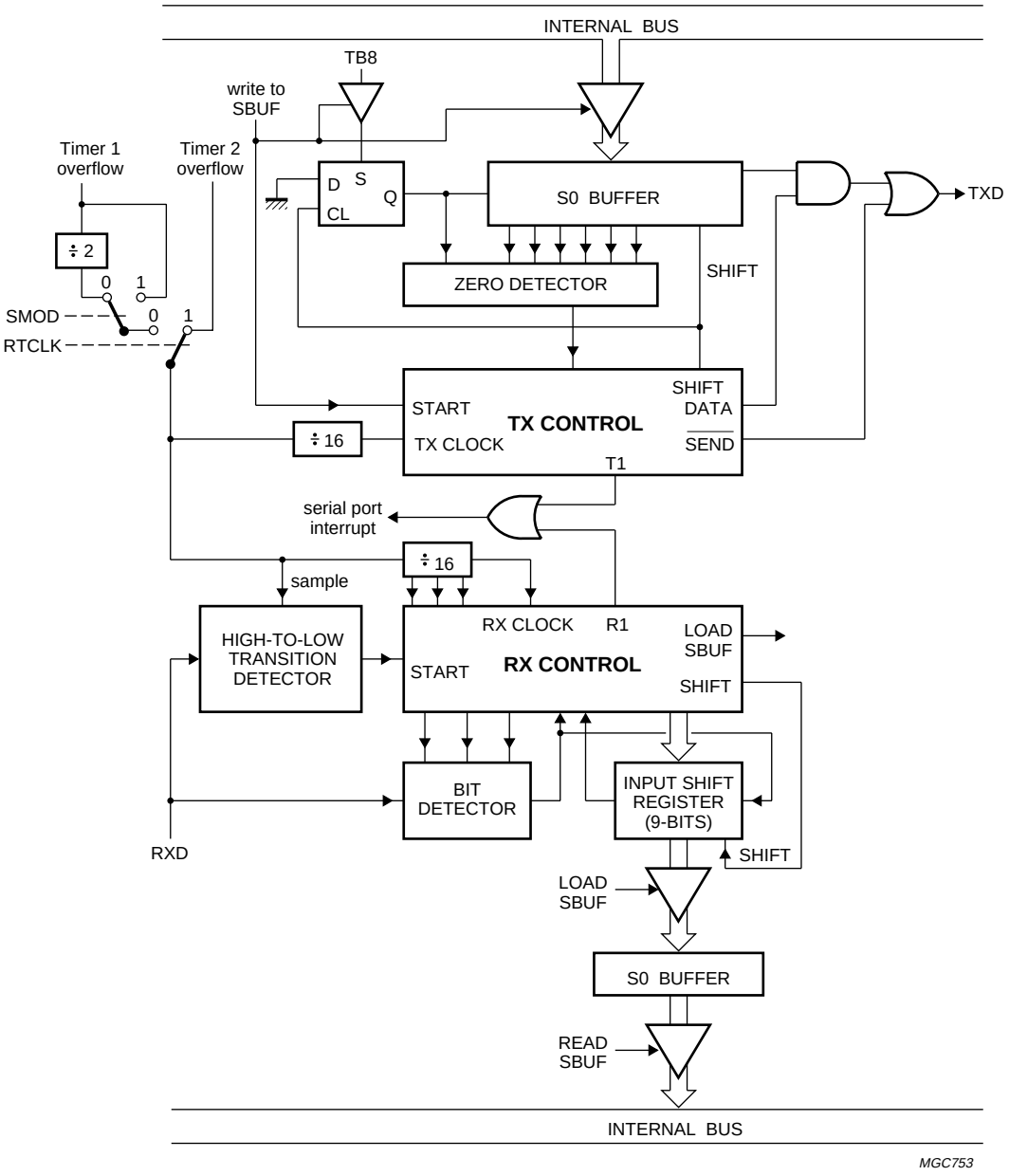


Fig.25 Serial port Mode 3.

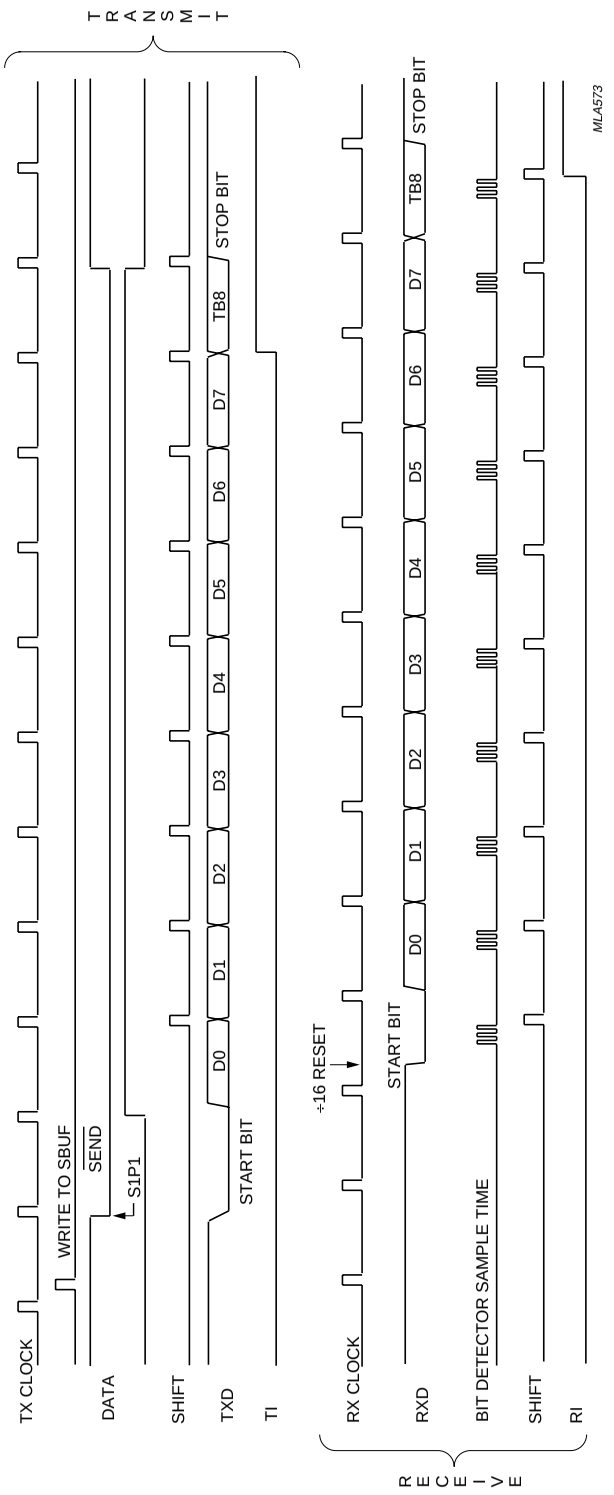


Fig.26 Serial port Mode 3 timing.

17 INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU at unpredictable times. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. The system is shown in Fig.27. The P8xCL580 acknowledges interrupt requests from fifteen sources as follows:

- $\overline{\text{INT0}}$ to $\overline{\text{INT8}}$
- Timer 0, Timer 1 and Timer 2
- I²C-bus serial I/O
- UART
- ADC.

Each interrupt vectors to a separate location in Program Memory for its service routine. Each source can be individually enabled or disabled by corresponding bits in the Interrupt Enable Registers (IEN0 and IEN1). The priority level is selected via the Interrupt Priority Registers (IP0 and IP1). All enabled sources can be globally disabled or enabled. Figure 27 shows the interrupt system.

17.1 External interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT8}}$

Port 1 lines serve an alternative purpose as seven additional interrupts $\overline{\text{INT2}}$ to $\overline{\text{INT8}}$. When enabled, each of these lines may wake-up the device from the Power-down mode. Using the Interrupt Polarity Register (IX1), each pin may be initialized to be either active HIGH or active LOW. IRQ1 is the Interrupt Request Flag Register. If the interrupt is enabled, each flag will be set on an interrupt request but must be cleared by software, i.e. via the interrupt software or when the interrupt is disabled.

Port 1 interrupts are level sensitive. A Port 1 interrupt will be recognized when a level (HIGH or LOW depending on the Interrupt Polarity Register) on P1.n is held active for at least one machine cycle. The interrupt request is not serviced until the next machine cycle. Figure 28 shows the external interrupt system.

17.2 Interrupt priority

Each interrupt source can be set to either a high priority or to a low priority. If a low priority interrupt is received simultaneously with a high priority interrupt, the high priority interrupt will be dealt with first.

If interrupts of the same priority are requested simultaneously, the processor will branch to the interrupt polled first, according to the sequence shown in Table 34 and in Fig.27. The ‘vector address’ is the ROM location where the appropriate interrupt service routine starts.

Table 34 Interrupt vector polling sequence

SYMBOL	VECTOR ADDRESS (HEX)	SOURCE
X0 (first)	0003	External 0
S1	002B	I²C port
X5	0053	External 5
T0	000B	Timer 0
T2	0033	Timer 2
X6	005B	External 6
X1	0013	External 1
X2	003B	External 2
X7	0063	External 7
T1	001B	Timer 1
X3	0043	External 3
X8	006B	External 8
SO	0023	UART
X4	004B	External 4
ADC (last)	0073	ADC

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine cannot be interrupted.

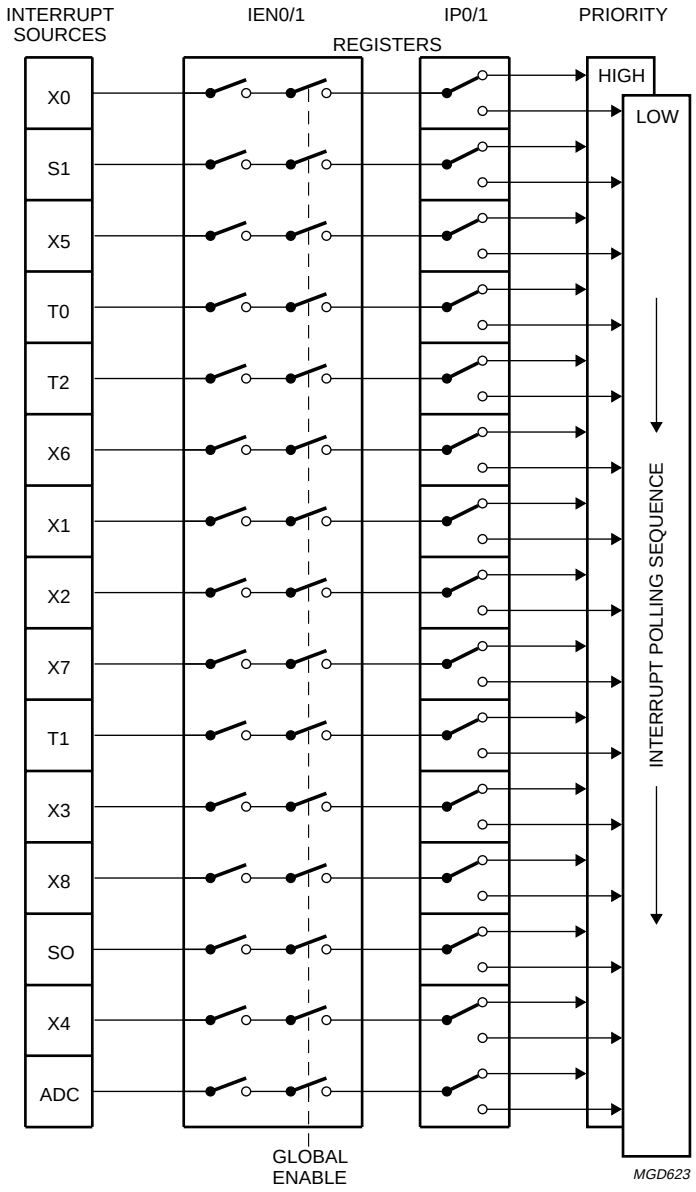


Fig.27 Interrupt system.

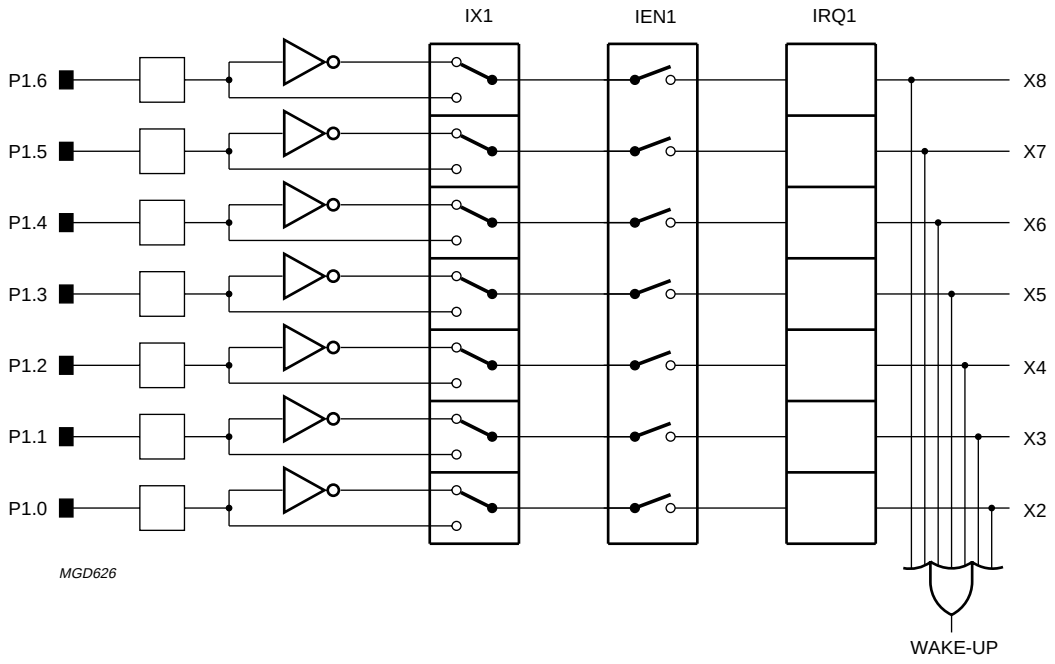


Fig.28 External interrupt configuration.

17.3 Interrupt registers

The registers used in the interrupt system are listed in Table 35. Tables 36 to 47 describe the contents of these registers.

Table 35 Special Function Registers related to the interrupt system

ADDRESS	REGISTER	DESCRIPTION
A8H	IEN0	Interrupt Enable Register
E8H	IEN1	Interrupt Enable Register ($\overline{INT2}$ to $\overline{INT8}$)
B8H	IP0	Interrupt Priority Register
F8H	IP1	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT8}$, ADC)
E9H	IX1	Interrupt Polarity Register
C0H	IRQ1	Interrupt Request Flag Register

17.3.1 Interrupt Enable Register (IEN0)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 36 Interrupt Enable Register (SFR address A8H)

7	6	5	4	3	2	1	0
EA	ET2	ES1	ES0	ET1	EX1	ET0	EX0

Table 37 Description of IEN0 bits

BIT	SYMBOL	DESCRIPTION
7	EA	General enable/disable control. If EA = 0, no interrupt is enabled. If EA = 1, any individually enabled interrupt will be accepted.
6	ET2	enable T2 interrupt
5	ES1	enable I²C interrupt
4	ES0	enable UART SIO interrupt
3	ET1	enable Timer 1 interrupt (T1)
2	EX1	enable external interrupt 1
1	ET0	enable Timer 0 interrupt (T0)
0	EX0	enable external interrupt 0

17.3.2 Interrupt Enable Register (IEN1)

Bit values: 0 = interrupt disabled; 1 = interrupt enabled.

Table 38 Interrupt Enable Register (SFR address E8H)

7	6	5	4	3	2	1	0
EAD	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Table 39 Description of IEN1 bits

BIT	SYMBOL	DESCRIPTION
7	EAD	Enable ADC interrupt.
6	EX8	enable external interrupt 8
5	EX7	enable external interrupt 7
4	EX7	enable external interrupt 6
3	EX5	enable external interrupt 5
2	EX4	enable external interrupt 4
1	EX3	enable external interrupt 3
0	EX2	enable external interrupt 2

17.3.3 Interrupt Priority Register (IP0)

Bit values: 0 = low priority; 1 = high priority.

Table 40 Interrupt Priority Register (SFR address B8H)

7	6	5	4	3	2	1	0
–	PT2	PS1	PS0	PT1	PX1	PT0	PX0

Table 41 Description of IP0 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	PT2	Timer 2 interrupt priority level
5	PS1	I²C interrupt priority level
4	PS0	UART SIO interrupt priority level
3	PT1	Timer 1 interrupt priority level
2	PX1	external interrupt 1 priority level
1	PT0	Timer 0 interrupt priority level
0	PX0	external interrupt 0 priority level

17.3.4 Interrupt Priority Register (IP1)

Bit values: 0 = low priority; 1 = high priority.

Table 42 Interrupt Priority Register (SFR address F8H)

7	6	5	4	3	2	1	0
PADC	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Table 43 Description of IP1 bits

BIT	SYMBOL	DESCRIPTION
7	PADC	ADC interrupt priority level
6	PX8	external interrupt 8 priority level
5	PX7	external interrupt 7 priority level
4	PX6	external interrupt 6 priority level
3	PX5	external interrupt 5 priority level
2	PX4	external interrupt 4 priority level
1	PX3	external interrupt 3 priority level
0	PX2	external interrupt 2 priority level

17.3.5 Interrupt Polarity Register (IX1)

Writing either a logic 1 or logic 0 to any Interrupt Polarity Register bit sets the polarity level of the corresponding external interrupt to an active HIGH or active LOW respectively.

Table 44 Interrupt Polarity Register (SFR address E9H)

7	6	5	4	3	2	1	0
–	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Table 45 Description of IX1 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	IL8	external interrupt 8 polarity level
5	IL7	external interrupt 7 polarity level
4	IL6	external interrupt 6 polarity level
3	IL5	external interrupt 5 polarity level
2	IL4	external interrupt 4 polarity level
1	IL3	external interrupt 3 polarity level
0	IL2	external interrupt 2 polarity level

17.3.6 Interrupt Request Flag Register (IRQ1)

Table 46 Interrupt Request Flag Register (SFR address C0H)

7	6	5	4	3	2	1	0
–	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Table 47 Description of IRQ1 bits

BIT	SYMBOL	DESCRIPTION
7	–	reserved
6	IQ8	external interrupt 8 request flag
5	IQ7	external interrupt 7 request flag
4	IQ6	external interrupt 6 request flag
3	IQ5	external interrupt 5 request flag
2	IQ4	external interrupt 4 request flag
1	IQ3	external interrupt 3 request flag
0	IQ2	external interrupt 2 request flag

18 OSCILLATOR CIRCUITRY

The on-chip oscillator circuitry of the P8xCL580 is a single-stage inverting amplifier biased by an internal feedback resistor. The oscillator circuit is shown in Fig.30. For operation as a standard quartz oscillator, no external components are needed, except for the 32 kHz option. When using external capacitors, ceramic resonators, coils and RC networks to drive the oscillator, five different configurations are supported (see Table 48 and Fig.29).

In the Power-down mode the oscillator is stopped and XTAL1 is pulled HIGH. The oscillator invertor is switched off to ensure no current will flow regardless of the voltage at XTAL1, for configurations (a), (b), (c), (d), (e) and (g) of Fig.29.

To drive the device with an external clock source, apply the external clock signal to XTAL1, and leave XTAL2 to float, as shown in Fig.29(f). There are no requirements on the duty cycle of the external clock, since the input to the internal clocking circuitry is buffered by a flip-flop.

Various oscillator options are provided for optimum on-chip oscillator performance; these are specified in Table 48 and shown in Fig.29. The required option should be stated when ordering.

Table 48 Oscillator options

OPTION	APPLICATION
Oscillator 1	For 32 kHz clock applications with external trimmer for frequency adjustment. A 4.7 MΩ bias resistor is needed for use in parallel with the crystal; see Fig.29(c).
Oscillator 2	Low-power, low-frequency operations using LC components; see Fig.29(e).
Oscillator 3	Medium frequency range applications.
Oscillator 4	High frequency range applications.
RC oscillator	RC oscillator configuration; see Figs 29(g) and 31.

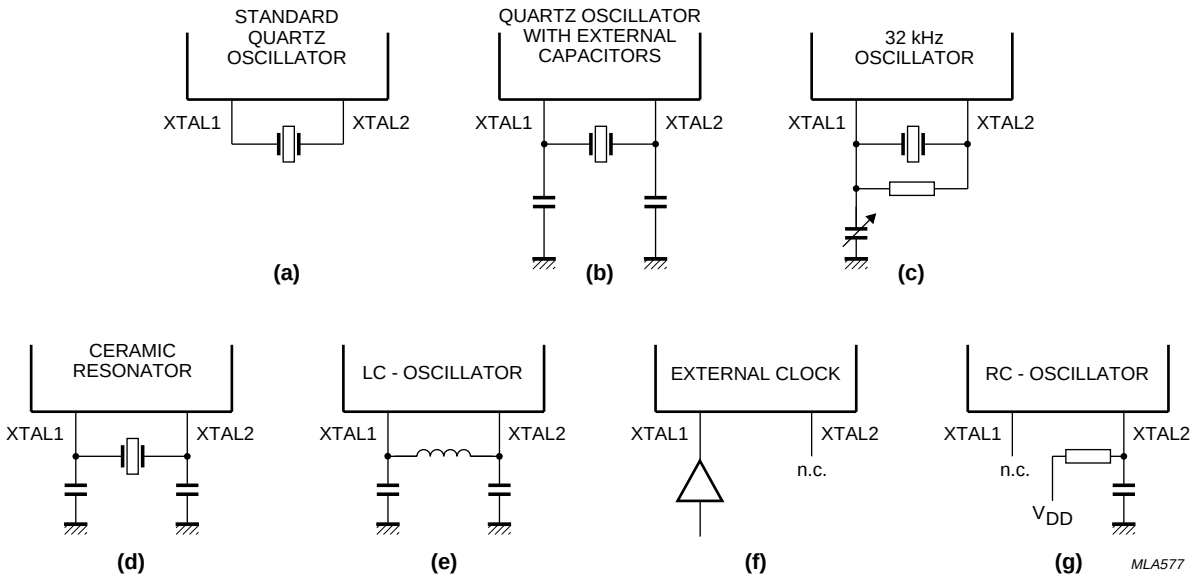


Fig.29 Oscillator configurations.

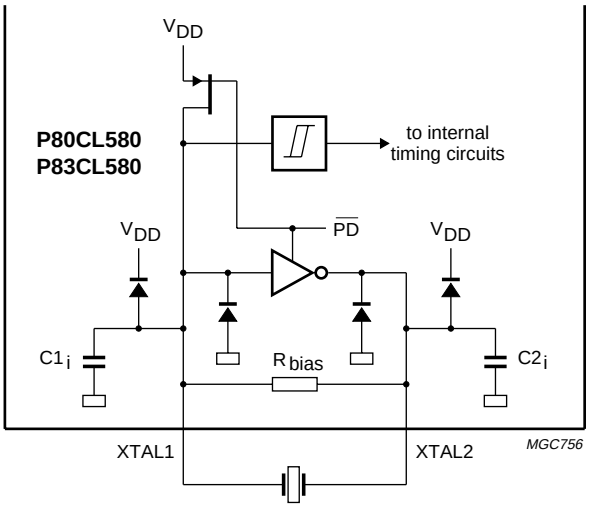
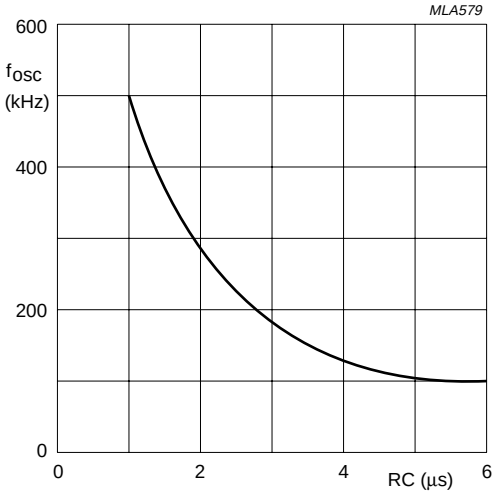


Fig.30 Standard oscillator.



RC oscillator frequency is externally adjustable; 100 kHz ≤ f_{osc} ≤ 500 kHz.

Fig.31 RC oscillator; frequency as a function of RC.

Table 49 Oscillator type selection guide

RESONATOR	FREQUENCY (MHz)	OPTION (see Table 48)	C1 EXT. (pF)		C2 EXT. (pF)		RESONATOR MAX. SERIES RESISTANCE
			MIN.	MAX.	MIN.	MAX.	
Quartz	0.032	Oscillator 1	0	0	5	15	15 kΩ; note 1
	1.0	Oscillator 2	0	30	0	30	600 Ω
	3.58		0	15	0	15	100 Ω
	4.0		0	20	0	20	75 Ω
	6.0	Oscillator 3	0	10	0	10	60 Ω
	10.0	Oscillator 4	0	15	0	15	60 Ω
	12.0		0	10	0	10	40Ω
	16.0		0	15	0	15	20 Ω
PXE	0.455	Oscillator 2	40	50	40	50	10 Ω
	1.0		15	50	15	50	100 Ω
	3.58		0	40	0	40	10 Ω
	4.0		0	40	0	40	10 Ω
	6.0		0	20	0	20	5 Ω
	10.0	Oscillator 3	0	15	0	15	6 Ω
	12.0	Oscillator 4	10	40	10	40	6 Ω
LC		Oscillator 2	20	90	20	90	10 μH = 1 Ω 100 μH = 5 Ω 1 mH = 75 Ω

Note

1. 32 kHz quartz crystals with a series resistance >15 kΩ will reduce the guaranteed supply voltage range to 2.5 to 3.5 V.

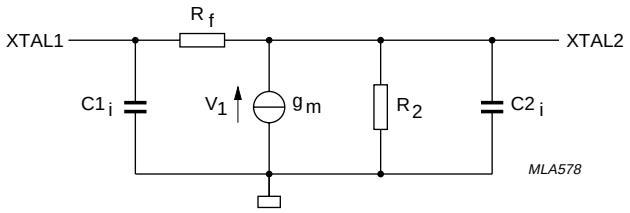


Fig.32 Oscillator equivalent circuit diagram.

Table 50 Oscillator equivalent circuit parameters

The equivalent circuit data of the internal oscillator compares with that of matched crystals.

SYMBOL	PARAMETER	OPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
g_m	transconductance	Oscillator 1; 32 kHz	T_{amb} = +25 °C; V_{DD} = 4.5 V	–	15	–	µS
		Oscillator 2		200	600	1000	µS
		Oscillator 3		400	1 500	4000	µS
		Oscillator 4		1000	4000	10000	µS
$C1_i$	input capacitance	Oscillator 1; 32 kHz		–	3.0	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
$C2_i$	output capacitance	Oscillator 1; 32 kHz		–	23	–	pF
		Oscillator 2		–	8.0	–	pF
		Oscillator 3		–	8.0	–	pF
		Oscillator 4		–	8.0	–	pF
R2	output resistance	Oscillator 1; 32 kHz		–	3800	–	kΩ
		Oscillator 2		–	65	–	kΩ
		Oscillator 3		–	18	–	kΩ
		Oscillator 4		–	5.0	–	kΩ

19 RESET

To initialize the P8xCL580 a reset is performed by either of three methods:

- Applying an external signal to the RST pin
- Via Power-on-reset circuitry
- Watchdog Timer.

A reset leaves the internal registers as shown in Chapter 20. The reset state of the port pins is mask-programmable and can be defined by the user.

19.1 External reset using the RST pin

The reset input for the P8xCL580 is RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle. A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. Port pins adopt their reset state immediately after the RST goes HIGH. During reset, ALE and $\overline{PSEN}$ are held HIGH.

The external reset is asynchronous to the internal clock. The RST pin is sampled during state 5, phase 2 of every machine cycle. After a HIGH is detected at the RST pin, an internal reset is repeated until RST goes LOW. The reset circuitry is also affected by the Watchdog timer; see Section 11.4. The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM contents are indeterminate.

19.2 Power-on-reset

The device contains on-chip circuitry which switches the port pins to the customer defined logic level as soon as V_{DD} exceeds 1.3 V; if the mask option 'ON' has been chosen. As soon as the minimum supply voltage is reached, the oscillator will start up. However, to ensure that the oscillator is stable before the controller starts, the clock signals are gated away from the CPU for a further 1536 oscillator periods. During that time the CPU is held in a reset state. A hysteresis of approximately 50 mV at a typical power-on switching level of 1.3 V will ensure correct operation (see Fig.35).

The on-chip Power-on reset circuitry can also be switched off via the mask option 'OFF'. This option reduces the Power-down current to typically 800 nA and can be chosen if external reset circuitry is used. For applications not requiring the internal reset, option 'OFF' should be chosen.

An automatic reset can be obtained by connecting the RST pin to V_{DD} via a 10 µF capacitor. At power-on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles. The Power-on-reset circuitry is shown in Fig.34.

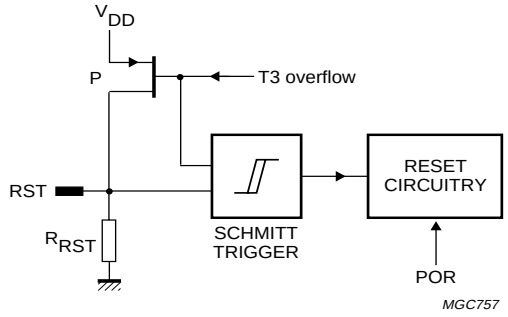


Fig.33 Reset configuration.

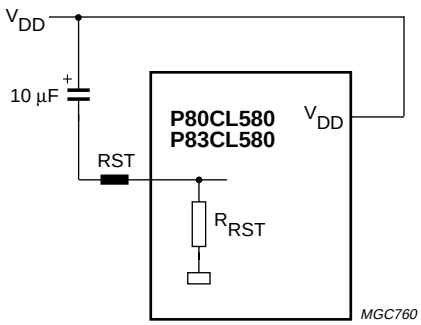


Fig.34 Recommended Power-on-reset circuitry.

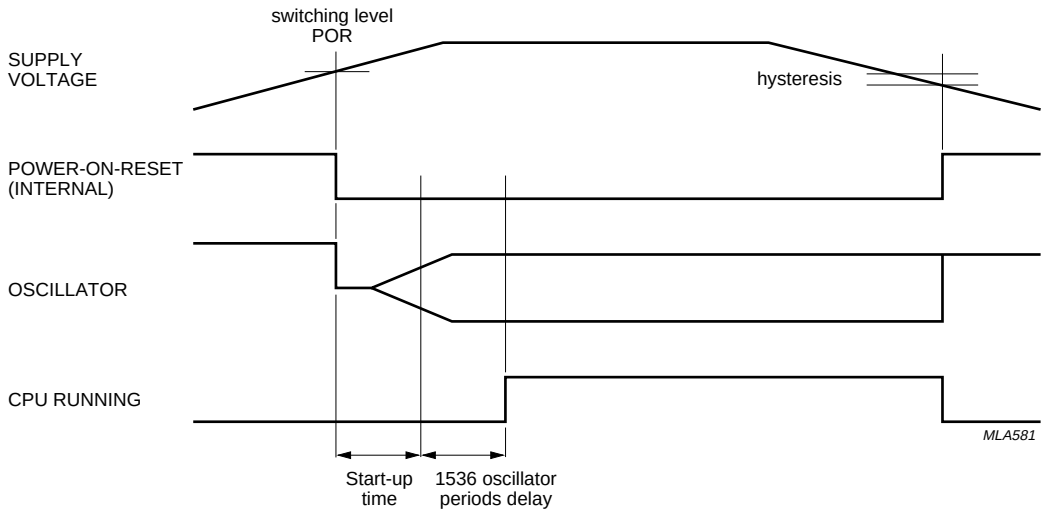


Fig.35 Power-on-reset switching level.

20 SPECIAL FUNCTION REGISTERS_OVERVIEW

The P8xCL580 has 40 SFRs available to the user.

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
FF	T3	00000000	Watchdog Timer
FE	PWMP	00000000	Prescaler Frequency Control Register
FC	PWM0	00000000	Pulse Width Register 0
F8	IP1	00000000	Interrupt Priority Register ($\overline{INT2}$ to $\overline{INT8}$, ADC)
F0	B(1)	00000000	B Register
E9	IX1	00000000	Interrupt Polarity Register
E8	IEN1(1)	00000000	Interrupt Enable Register 1
E0	ACC(1)	00000000	Accumulator
DB	S1ADR	00000000	I²C-bus Slave Address Register
DA	S1DAT	00000000	I²C-bus Data Shift Register
D9	S1STA	11111000	I²C-bus Serial Status Register
D8	S1CON(1)	00000000	I²C-bus Serial Control Register
D0	PSW(1)	00000000	Program Status Word
CD	TH2	00000000	Timer 2 High byte
CC	TL2	00000000	Timer 2 Low byte
CB	RCAP2H	00000000	Timer 2 Reload/Capture Register High byte
CA	RCAP2L	00000000	Timer 2 Reload/Capture Register Low byte
C8	T2CON(1)	00000000	Timer/Counter 2 Control Register
C5	ADCH	11111111	ADC Result Register
C4	ADCON	X0000000	ADC Control Register
C1	P4	XXXXXXXX(2)	Digital I/O Port Register 4
C0	IRQ1(1)	00000000	Interrupt Request Flag Register

ADDRESS (HEX)	NAME	RESET VALUE (B)	FUNCTION
B8	IP0[1]	X0000000	Interrupt Priority Register 0
B0	P3[1]	XXXXXXXX[2]	Digital I/O Port Register 3
A8	IEN0[1]	00000000	Interrupt Enable Register
A0	P2[1]	XXXXXXXX[2]	Digital I/O Port Register 2
99	S0BUF	XXXXXXXX	Serial Data Buffer Register 0
98	S0CON[1]	00000000	Serial Port Control Register 0
90	P1[1]	XXXXXXXX[2]	Digital I/O Port Register 1
8D	TH1	00000000	Timer 1 High byte
8C	TH0	00000000	Timer 0 High byte
8B	TL1	00000000	Timer 1 Low byte
8A	TL0	00000000	Timer 0 Low byte
89	TMOD	00000000	Timer 0 and 1 Mode Control Register
88	TCON[1]	00000000	Timer 0 and 1 Control/External Interrupt Control Register
87	PCON	0XX00000	Power Control Register
83	DPH	00000000	Data Pointer High byte
82	DPL	00000000	Data Pointer Low byte
81	SP	00000111	Stack Pointer
80	P0[1]	XXXXXXXX[2]	Digital I/O Port Register 0

Notes

1. Bit addressable register.
2. Port reset state determined by the customer.

21 INSTRUCTION SET

The P8xCL580 uses a powerful instruction set which permits the expansion of on-chip CPU peripherals and optimizes byte efficiency and execution speed. Assigned opcodes add new high-power operation and permit new addressing modes. The instruction set consists of 49 single-byte, 46 two-byte and 16 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

For the description of the **Data Addressing modes** and **Hexadecimal opcode cross-reference** see Table 55.

Table 51 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A and B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

Table 52 Instruction set description: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 53 Instruction set description: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 54 Instruction set description: Boolean variable manipulation, Program and machine control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	•1
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	♦1
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Table 55 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	111-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

Table 56 Instruction map

First hexadecimal character of opcode ↓	← Second hexadecimal character of opcode → 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	INC @Ri 1	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	DEC @Ri 1	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	ADD A,@Ri 1	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	ADDC A,@Ri 1	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	ORL A,@Ri 1	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	ANL A,@Ri 1	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	XRL A,@Ri 1	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	MOV @Ri,#data 1	MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	MOV direct,@Ri 1	MOV direct,Rr 0	MOV direct,Rr 1	MOV direct,Rr 2	MOV direct,Rr 3	MOV direct,Rr 4	MOV direct,Rr 5	MOV direct,Rr 6	MOV direct,Rr 7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	SUBB A,@Ri 1	SUB A,Rr 0	SUB A,Rr 1	SUB A,Rr 2	SUB A,Rr 3	SUB A,Rr 4	SUB A,Rr 5	SUB A,Rr 6	SUB A,Rr 7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	MOV @Ri,direct 1	MOV Rr,direct 0	MOV Rr,direct 1	MOV Rr,direct 2	MOV Rr,direct 3	MOV Rr,direct 4	MOV Rr,direct 5	MOV Rr,direct 6	MOV Rr,direct 7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	CJNE @Ri,#data,rel 1	CJNE Rr,#data,rel 0	CJNE Rr,#data,rel 1	CJNE Rr,#data,rel 2	CJNE Rr,#data,rel 3	CJNE Rr,#data,rel 4	CJNE Rr,#data,rel 5	CJNE Rr,#data,rel 6	CJNE Rr,#data,rel 7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	XCH A,@Ri 1	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	XCHD A,@Ri 1	DJNZ Rr,rel 0	DJNZ Rr,rel 1	DJNZ Rr,rel 2	DJNZ Rr,rel 3	DJNZ Rr,rel 4	DJNZ Rr,rel 5	DJNZ Rr,rel 6	DJNZ Rr,rel 7
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0	MOVX A,@Ri 1	CLR A	MOV A,direct (1)	MOV A,@Ri 0	MOV A,@Ri 1	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0	MOVX @Ri,A 1	CPL A	MOV direct,A	MOV @Ri,A 0	MOV @Ri,A 1	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7

Note

1. MOV A, ACC is not a valid instruction.

22 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+6.5	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.5	V_{DD} + 0.5	V
I_I	DC current on any input	–5.0	+5.0	mA
I_O	DC current on any output	–5.0	+5.0	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
T_j	operating junction temperature	–	+125	°C

23 DC CHARACTERISTICS

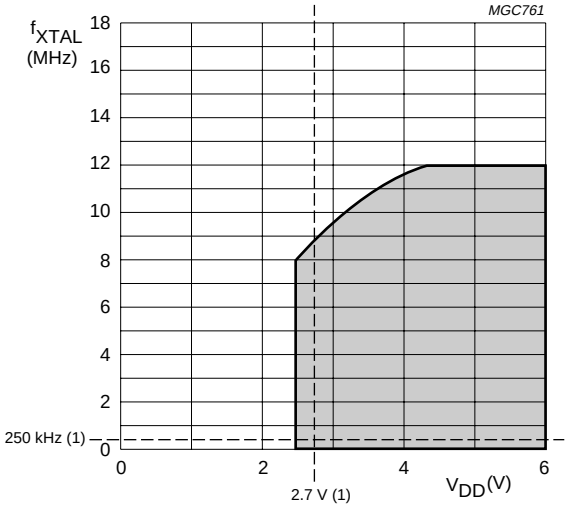
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +55 °C; see notes 1 and 2; all voltages with respect to V_{SS} unless specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	operating		2.5	–	6.0	V
	RAM retention voltage in Power-down mode		1.0	–	6.0	V
I_{DD}	supply current operating	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 3	–	–	27.0	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 3	–	–	5.0	mA
$I_{DD(idle)}$	supply current Idle mode	V_{DD} = 5 V; f_{CLK} = 12 MHz; note 4	–	–	10.0	mA
		V_{DD} = 3 V; f_{CLK} = 3.58 MHz; note 4	–	–	3.0	mA
$I_{DD(pd)}$	Power-down current	V_{DD} = 1.8 V; T_{amb} = 25°C; note 5	–	–	10	µA
Inputs (note 6)						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current (Port 0; $\overline{EA}$)	$V_{SS} < V_I < V_{DD}$	–	–	±10	µA
Outputs						
I_{OL}	LOW level output current (except SDA; SCL)	V_{DD} = 5 V; V_{OL} = 0.4 V	1.6	–	–	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	0.7	–	–	mA
	LOW level output current SDA; SCL	V_{DD} = 5 V; V_{OL} = 0.4 V	3.0	–	–	mA
	LOW level output current $\overline{PWM0}$	V_{DD} = 5 V; V_{OL} = 0.4 V	3.2	–	–	mA
		V_{DD} = 2.5 V; V_{OL} = 0.4 V	1.6	–	–	mA
I_{OH}	HIGH level output current $\overline{PWM0}$	V_{DD} = 5 V; V_{OH} = V_{DD} – 0.4 V	–3.2	–	–	mA
		V_{DD} = 2.5 V; V_{OH} = V_{DD} – 0.4 V	–1.6	–	–	mA
I_{OH}	HIGH level output current (push-pull options only)	V_{DD} = 5 V; V_{OH} = V_{DD} – 0.4 V	–1.6	–	–	mA
		V_{DD} = 2.5 V; V_{OH} = V_{DD} – 0.4 V	–0.7	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	input current logic 0	V_{DD} = 5 V; V_{IN} = 0.4 V	–	–	–100	µA
		V_{DD} = 2.5 V; V_{IN} = 0.4 V	–	–	–50	µA
I_{ITL}	input current logic 0; HIGH-to-LOW transition	V_{DD} = 5 V; V_{IN} = 0.5V_{DD}	–	–	–1.0	mA
		V_{DD} = 2.5 V; V_{IN} = 0.5V_{DD}	–	–	–500	µA
R_{RST}	RST pull-down resistor		10	–	200	kΩ
Analog inputs (note 7)						
$V_{IN(A)}$	analog input voltage		V_{SSA}	–	V_{DD}	mA
$V_{ref(p)(A)}$	reference voltage		2.7	–	V_{DD}	mA
R_{ref}	resistance between $V_{ref(p)(A)}$ and V_{SSA}		25	–	100	kΩ
C_{AIN}	analog on-chip input capacitance		–	3	–	pF
A_e	absolute error (note 8)		–	–	±1	LSB
OS_e	zero-offset error (note 9)		–	–	±1	LSB
DL_e	differential non-linearity (note 10)		–	–	±1	LSB
M_{ctc}	channel-to-channel matching (note 11)		–	–	±½	LSB

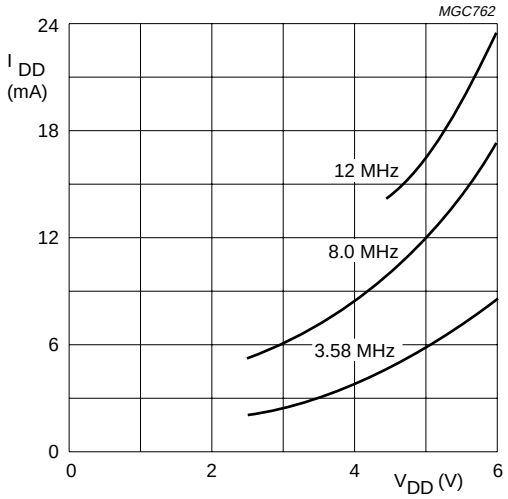
Notes to the DC characteristics

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3 pins when these make a HIGH-to-LOW transition during bus operations. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make HIGH-to-LOW transitions during bus operations. In the most adverse conditions (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such events it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger strobe input.
2. Capacitive loading on Ports 0 and 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9V_{DD} specification when the address bits are stabilizing.
3. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}.
4. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}.
5. The power-down current is measured with all output pins disconnected; XTAL1 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
6. The input threshold voltage of P1.6/SCL and P1.7/SDA meet the I²C-bus specification. Therefore, an input voltage below 0.3V_{DD} will be recognized as a logic 0 and an input voltage above 0.7V_{DD} will be recognized as a logic 1.
7. V_{DD} = 2.7 to 6 V; V_{SS} = 0 V; V_{SSA} = 0 V; $V_{ref(p)(A)} = V_{DD}$; T_{amb} = –40 to +85 °C, unless otherwise specified. $f_{xtal(min)}$ = 250 kHz.
8. Absolute error: the maximum difference between actual and ideal code transitions. Absolute error accounts for all deviations of an actual converter from an ideal converter.
9. Zero-offset error: the difference between the actual and ideal input voltage corresponding to the first actual code transition.
10. Differential non-linearity: the difference between the actual and ideal code widths.
11. Channel-to-channel matching: the difference between corresponding code transitions of actual characteristics taken from different channels under the same temperature, voltage and frequency conditions. Not tested, but verified on sampling basis.



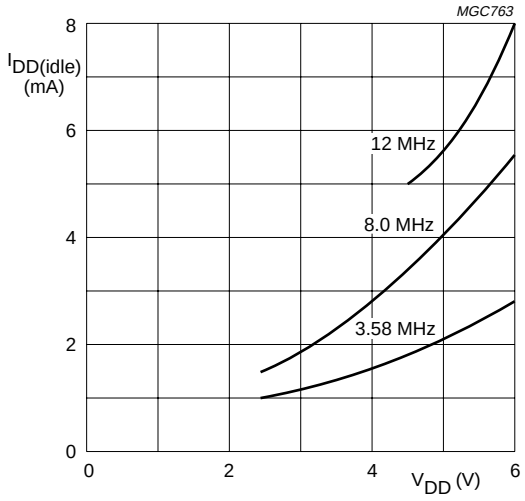
(1) The area above the dotted lines give the ADC operating area.

Fig.36 Frequency operating range.



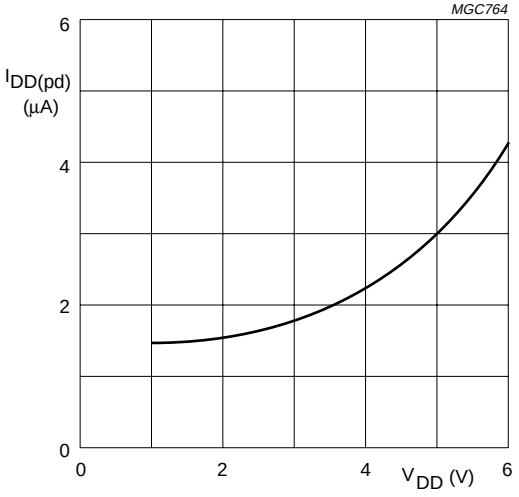
T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.37 Typical operating current as a function of frequency and V_{DD}.



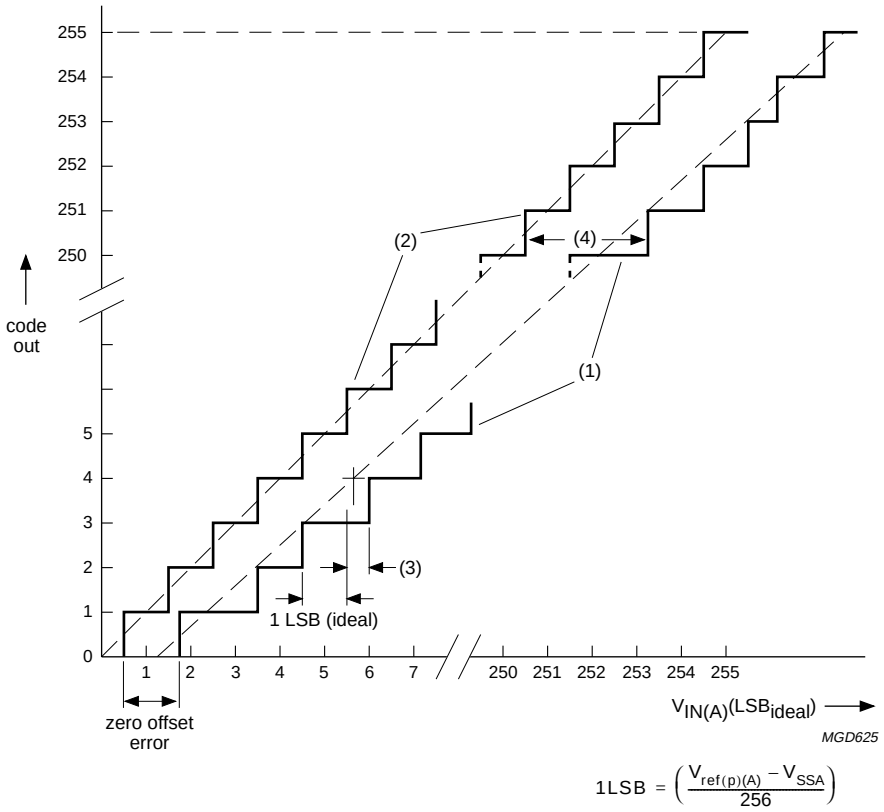
T_{amb} = 25 °C.
Oscillator option = Oscillator 3.

Fig.38 Typical Idle current as a function of frequency and V_{DD}.



T_{amb} = 25 °C.

Fig.39 Typical Power-down current as a function of V_{DD}.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity (DL_e).
(4) Absolute error.

Fig.40 Analog-to-digital conversion characteristics.

24 AC CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; C_L = 50 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 40 pF for all other outputs unless specified; $t_{CLK} = 1/f_{CLK}$.

SYMBOL	PARAMETER	f_{osc} = 12 MHz		f_{osc} = VARIABLE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Program Memory (Fig.41)						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLK} - 40$	–	ns
t_{AVLL}	address valid to ALE LOW	43	–	$t_{CLK} - 40$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{LLIV}	ALE LOW to valid instruction in	–	233	–	$4t_{CLK} - 100$	ns
t_{LLPL}	ALE LOW to $\overline{PSEN}$ LOW	58	–	$t_{CLK} - 25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLK} - 35$	–	ns
t_{PLIV}	$\overline{PSEN}$ LOW to valid instruction in	–	125	–	$3t_{CLK} - 125$	ns
t_{PXIX}	input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}	input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLK} - 20$	ns
t_{PXAV}	$\overline{PSEN}$ to address valid	75	–	$t_{CLK} - 8$	–	ns
t_{AVIV}	address to valid instruction in	–	302	–	$5t_{CLK} - 115$	ns
t_{PLAZ}	$\overline{PSEN}$ LOW to address float	12	–	0	–	ns
External Data Memory (Figs 42 and 43)						
t_{RLRH}	$\overline{RD}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLK} - 100$	–	ns
t_{LLAX}	address hold after ALE LOW	48	–	$t_{CLK} - 35$	–	ns
t_{RLDV}	$\overline{RD}$ LOW to valid data in	–	150	–	$5t_{CLK} - 165$	ns
t_{RHDZ}	data float after $\overline{RD}$	–	97	–	$2t_{CLK} - 70$	ns
t_{LLDV}	ALE LOW to valid data in	–	517		$8t_{CLK} - 150$	ns
t_{AVDV}	address to valid data in	–	585	–	$9t_{CLK} - 165$	ns
t_{LLWL}	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	200	300	$3t_{CLK} - 50$	$3t_{CLK} + 50$	ns
t_{AVWL}	address valid to $\overline{RD}$ or $\overline{WR}$ LOW	203	–	4	–	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	43	123	$t_{CLK} - 40$	$t_{CLK} + 40$	ns
t_{QVWX}	data valid to $\overline{WR}$ transition	23	–	$t_{CLK} - 60$	–	ns
t_{QVWH}	data valid time $\overline{WR}$ HIGH	433	–	$7t_{CLK} - 150$	–	ns
t_{WHQX}	data hold after $\overline{WR}$	33	–	$t_{CLK} - 50$	–	ns
t_{RLAZ}	$\overline{RD}$ LOW to address float	–	12	–	12	ns

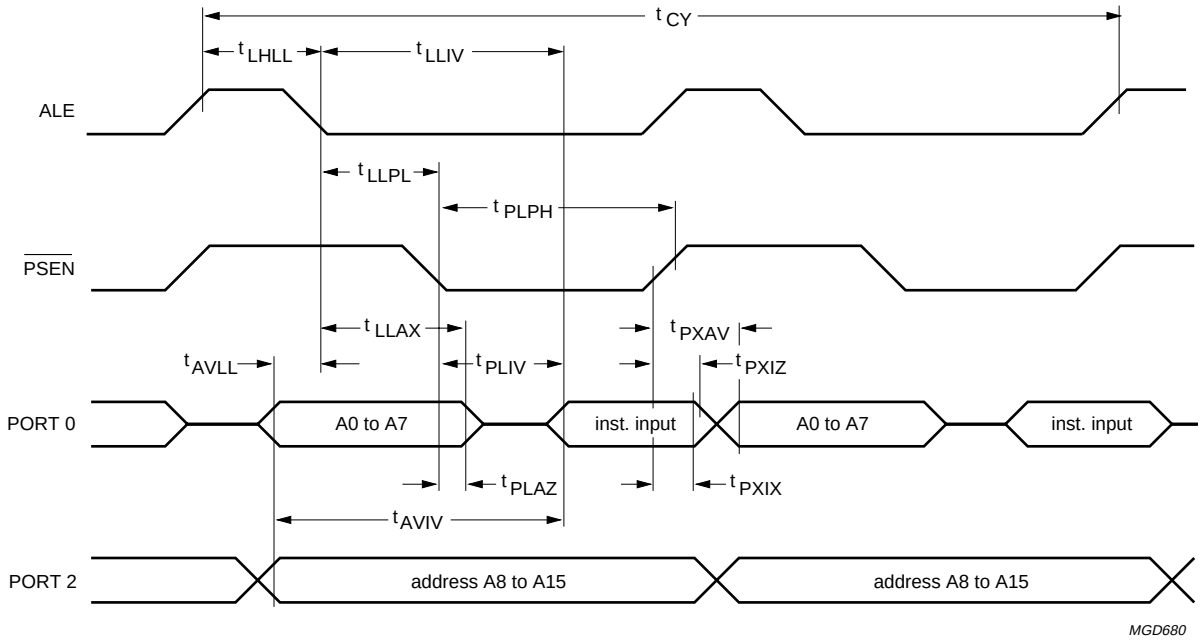


Fig.41 Read from Program Memory.

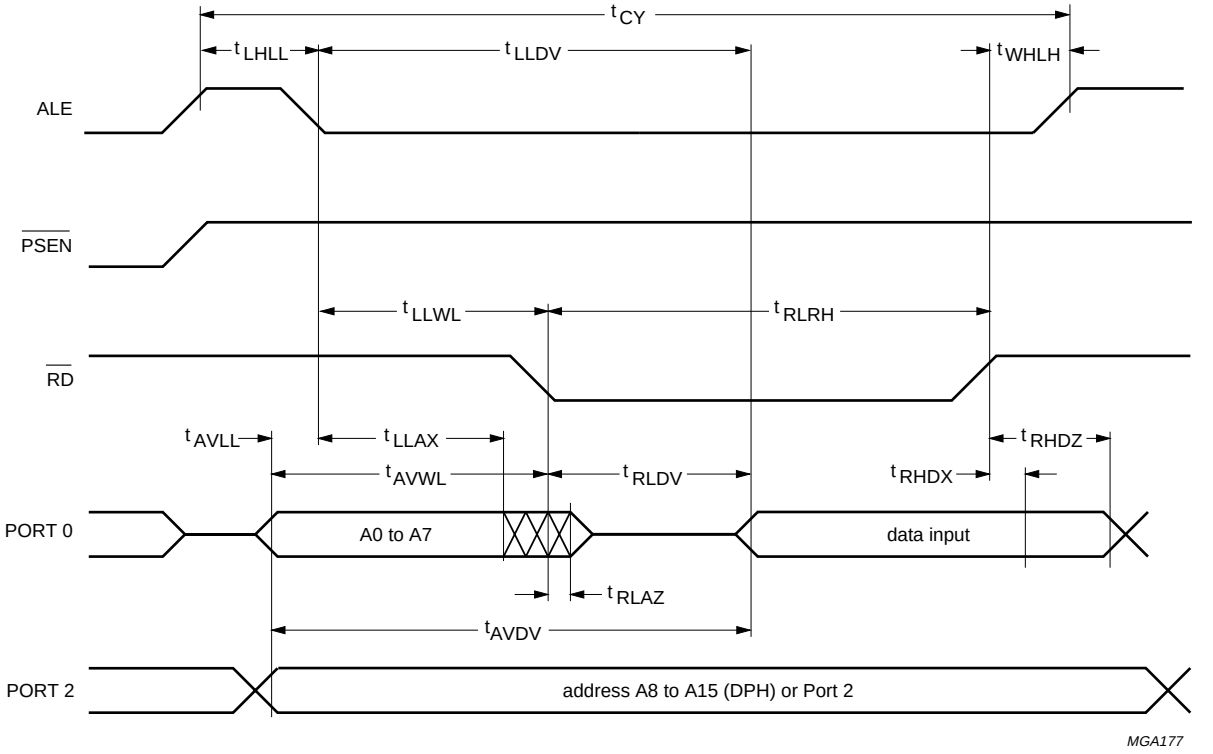


Fig.42 Read from Data Memory.

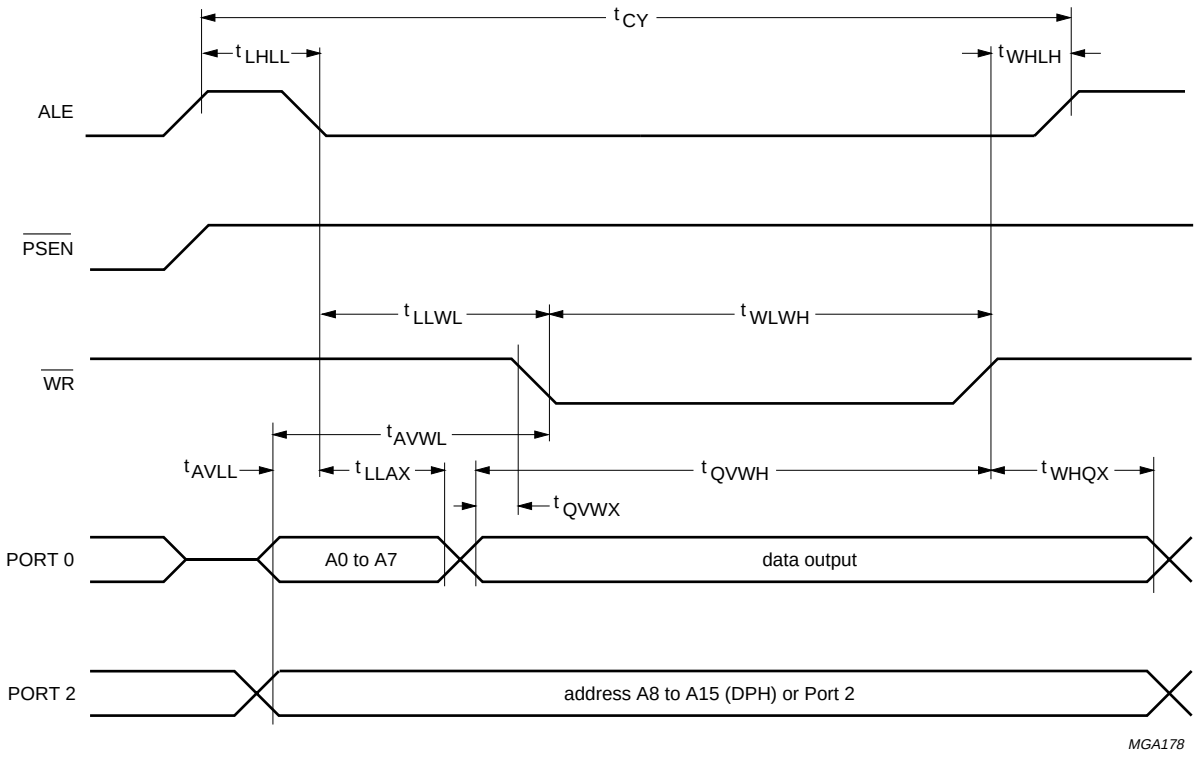


Fig.43 Write to Data Memory.

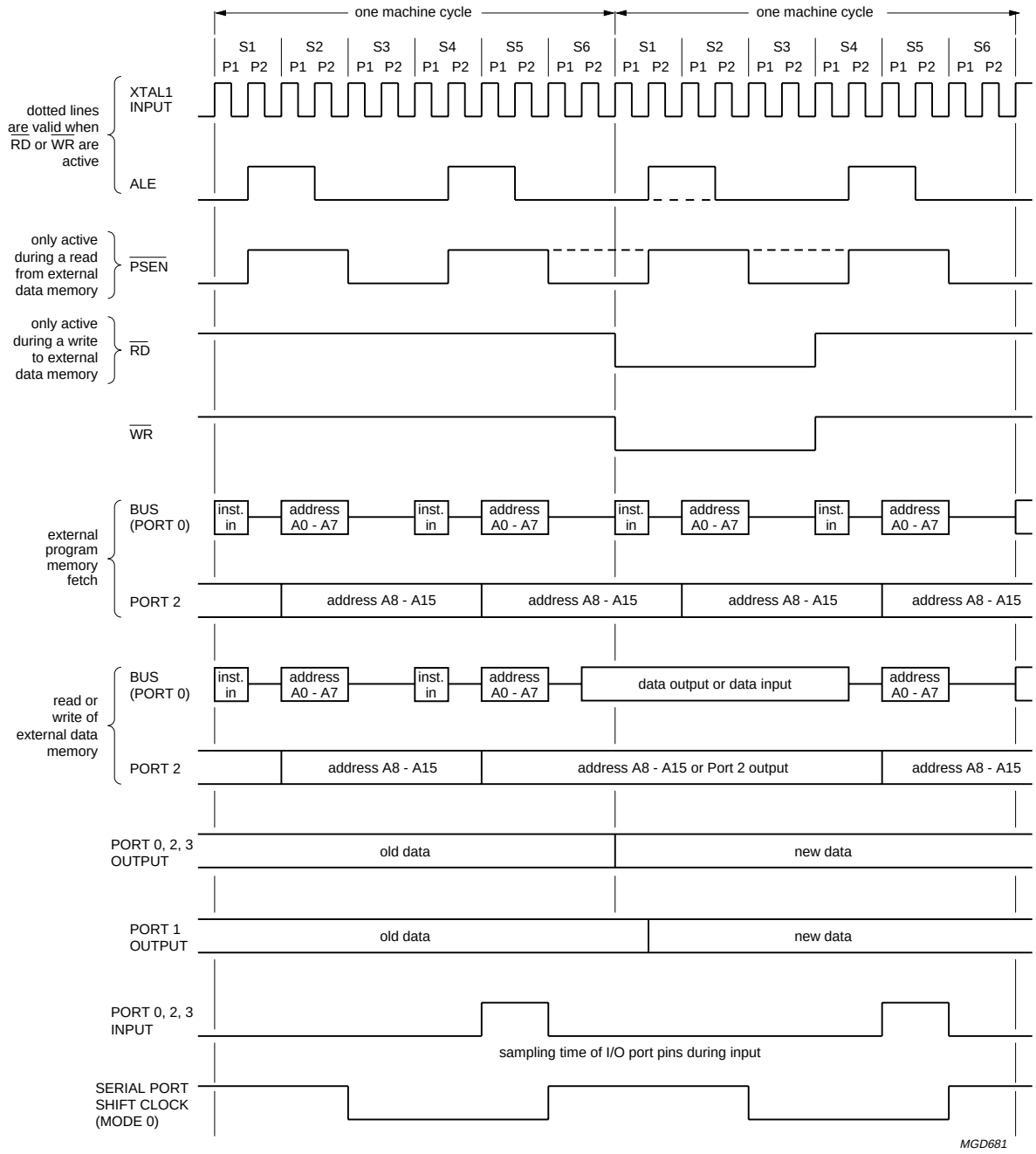


Fig.44 Instruction cycle timing.

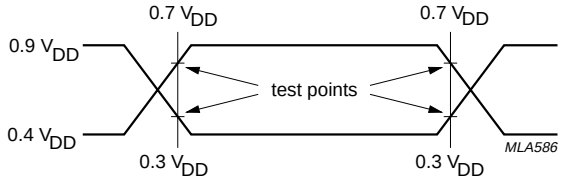


Fig.45 AC testing input waveform.

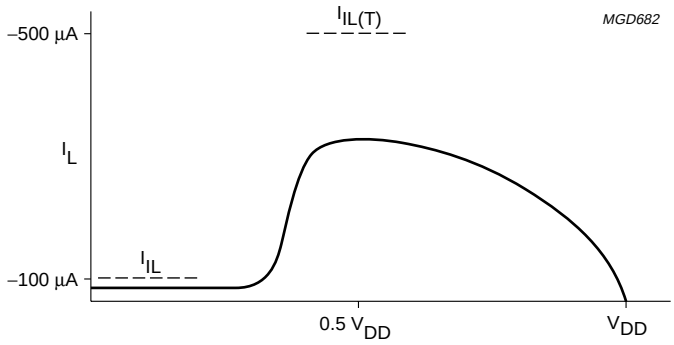
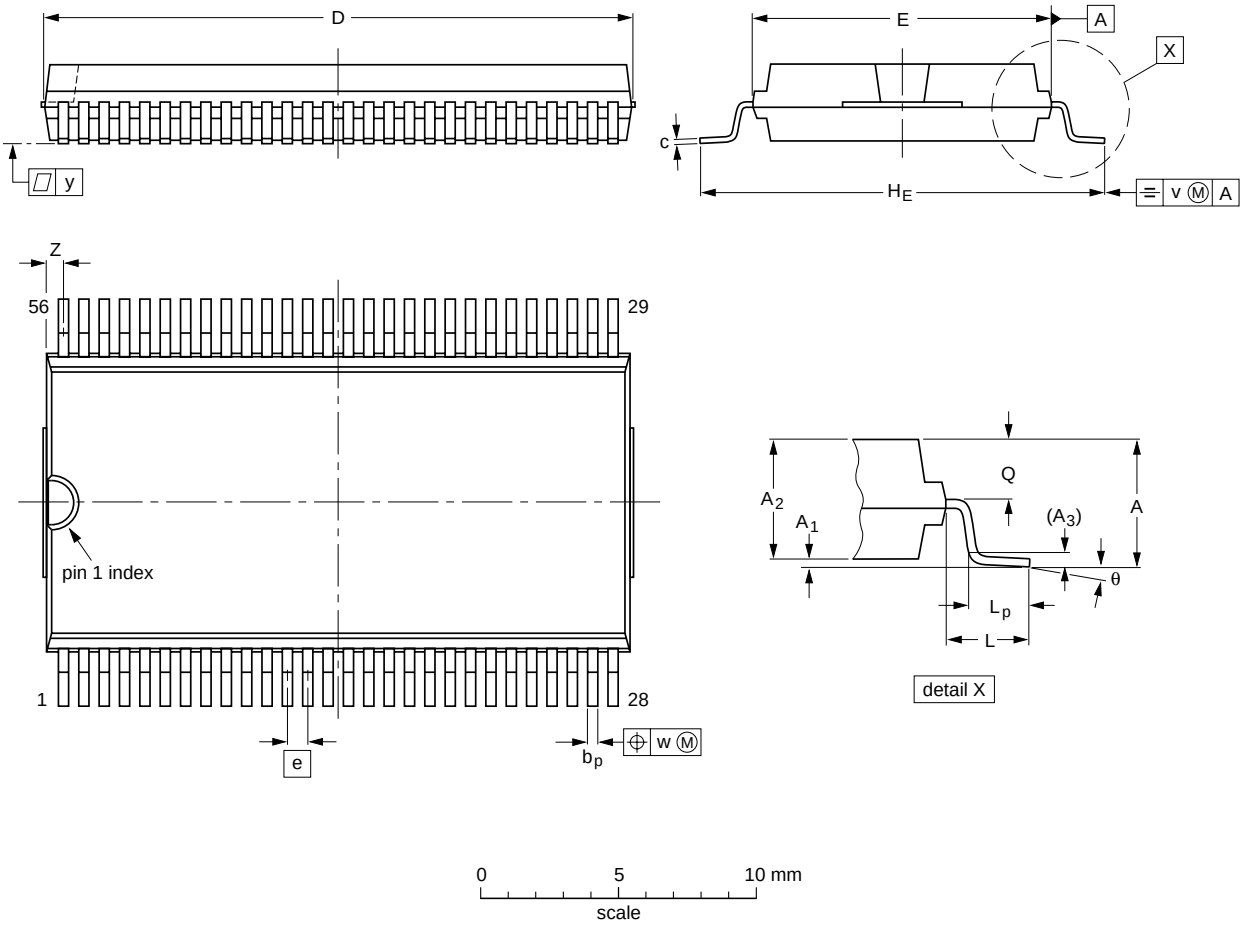


Fig.46 Input current.

25 PACKAGE OUTLINES

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

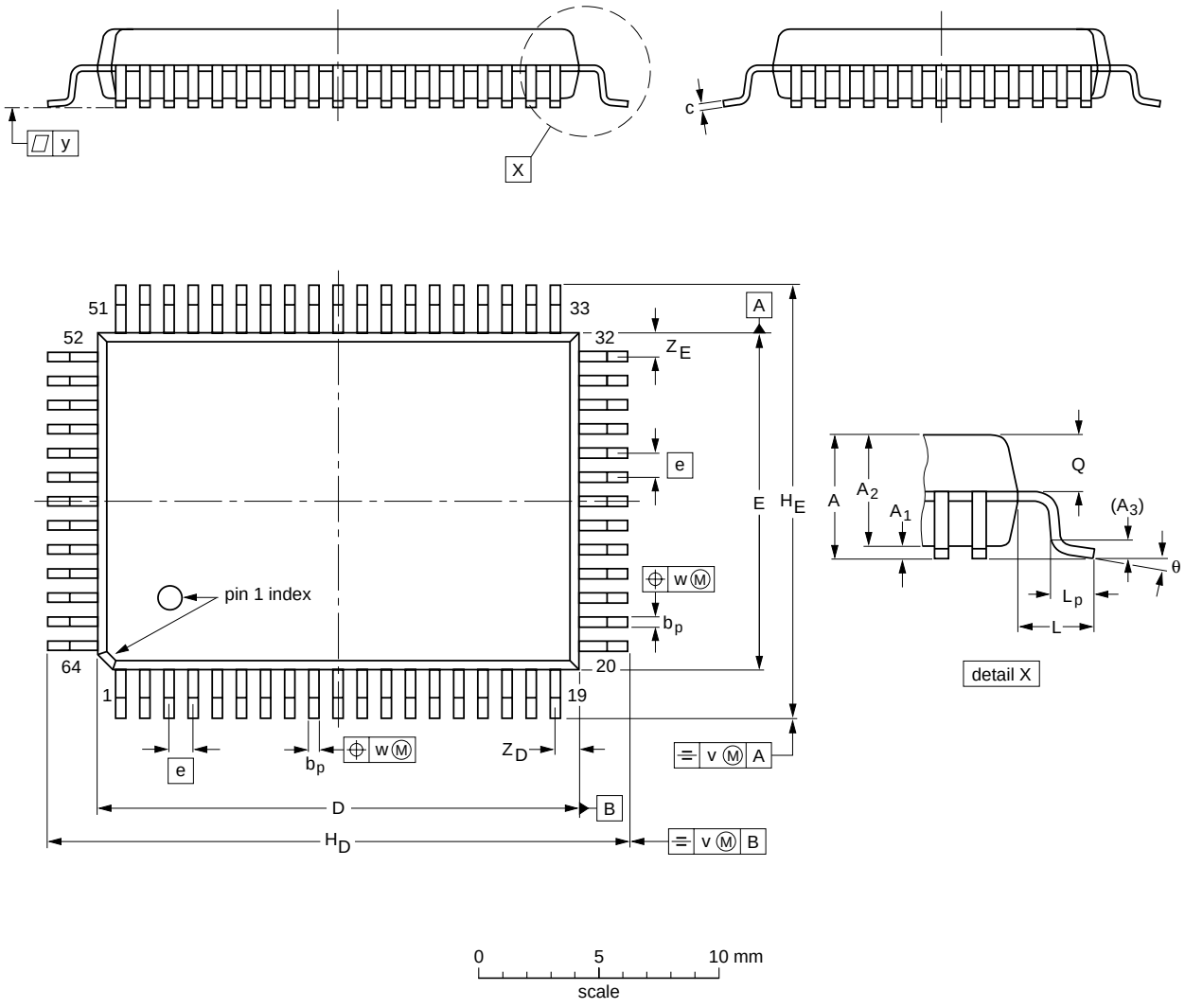
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7^o 0^o
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.03	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~92-11-17~~ 96-04-02

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	1.4 1.2	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~92-11-17~~ 95-02-04

26 SOLDERING

26.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

26.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP and VSO packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Manual"* (order code 9398 510 63011).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

26.3 Wave soldering

26.3.1 QFP

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

26.3.2 VSO

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

26.3.3 METHOD (QFP AND VSO)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

26.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

27 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

28 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

29 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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