ERRATA SHEET

Date: **2009 May 29**
Document Release: **Version 1.0**
Device Affected: **P89LPC9361**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

NXP
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Identification:

The typical P89LPC9361 devices have the following top-side marking:

P89LPC9361 x x

xxxxxxx xx

xxYYWW R

The last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC9361:

Revision Identifier (R)	Comment
-	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	occurs in revision	added
ADC.1	Single Step mode multi channel boundary interrupt	-	v1.0
DIVM.1	Using DIVM in power-down mode	-	v1.0
PGA.1	PGA0 enabled by setting PGATRIM0 bit	-	v1.0

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	occurs in revision	added
-	-	-	v1.0

Errata Notes

Note	Short Description	occurs in revision	added
-	-	-	v1.0

Functional Deviations of P89LPC9361

ADC.1: Single Step mode multi channel boundary interrupt

Introduction: The ADC on the LPC9361 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

Problem: When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. This applies to both ADC0 and ADC1 on the LPC9361.

Workarounds:
1) Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
2) Use the default boundary channel, not clear BNDI bit until all channels are converted.

DIVM.1: Using DIVM in power-down mode

Introduction: The LPC9361 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem: When DIVM is used in active mode and power-down mode is then entered the LPC9361 can not be woken up from power down mode.

Workaround: Before entering powerdown mode set DIVM back to 0x00. This way the LPC9361 will be operating full speed for one instruction before entering power-down mode. After the LPC9361 has been woken up DIVM can be set back to its original value.

PGA.1: PGA0 enabled by setting PGATRIM0 bit

Introduction: Register PGACON0 and PGACON0B are used for PGA0 configuration. In register PGACON0, ENPGA0 bit is used to enable PGA0. PGATRIM0 bit is used to enable PGA0 trim. If set, PGA0 is grounded for calibration mode.

Problem: PGA0 is also enabled by setting PGATRIM0 bit. When disable PGA0 by clear ENPGA0 bit, PGA0 still functions. When enter into power down mode or total power down mode, PGA module does not enter into power down mode and will continue consume power.

Workaround: Make sure to clear both PGATRIM0 bit and ENPGA0 bit before enter into power down mode or total power down mode. To disable PGA0, also make sure to clear both PGATRIM0 bit and ENPGA0 bit.

Electrical and Timing Specification Deviations of P89LPC9361

No known errata