ERRATA SHEET

Date: **November 7, 2008**
Document Release: **Version 0.09 Pre-release**
Device Affected: **LPC3220**

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Document revision history

Rev	Date	Description
1.0	<TBD>	First Release

November 7, 2008

NXP
Semiconductors

founded by Philips

Identification:

The LPC3220 devices typically have the following top-side marking:

LPC3220FET296

xxxxxxx

xxYYWWR

The last letter in the last line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC3220:

Revision Identifier (R)	Comment
‘-’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Occurs in Device Revision	Scheduled for fix in next major revision
RTC.1	An RTC match doesn't drive the ONSW pin active (high).	-	Y
INT.1	GPI_08 does not generate in interrupt signal.	-	Y

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Occurs in Device Revision	Scheduled for fix in next major revision
ESD.1	Weak ESD Protection on Reset_N Pin (pin M14)	-	Y

Errata Notes

Note	Short Description

Functional Problem Detail

RTC.1 An RTC match doesn't drive the ONSW pin active (high).

Introduction: An ONSW output pin (M15) is included in the LPC3220 to assist in waking up the chip after power is removed from all functions except the RTC and Battery RAM. When there is an active match condition the RTC will drive the ONSW pin high. The RTC only drives the ONSW pin while the match is active, and after 1 second of active match, if the software has not accessed the RTC block, the ONSW pin will go low when the match is no longer active.

Problem: When power is removed from all functions except the RTC and Battery RAM, the RTC does NOT drive the ONSW pin high when there is an active match condition.

Work-around: There is no work-around for this problem.

Schedule for Fix: Next Revision

INT.1 GPI_08 does not generate an Interrupt signal.

Introduction: The LPC3220 contains 12 pins (GPI_00 - GPI_09, GPI_19, GPI_28) that function as dedicated General Purpose Inputs. Each of these pins can generate an individual interrupt for the input pin. Sub Interrupt Controller Register 1 (SIC1_ER) and Sub Interrupt Controller Register 2 (SIC2_ER) contains bits that allow enabling or disabling the interrupt for the associated pin

Problem: When bit nine is set to one in the Sub Interrupt Controller 2 Enable register (SIC2_ER[9]) it does not enable the interrupt for the GPI_08 pin. All other General Purpose Input pins (GPI_00 - GPI_07, GPI_09, GPI_19, GPI_28) interrupts work correctly.

Work-around: There is no work-around for this problem.

Schedule for Fix: Next Revision.

AC/DC Deviation Detail

ESD.1 Weak ESD Protection on Reset_N Pad

Introduction: The LPC3220 was designed to withstand electrostatic discharges up to 2000 V using the Human Body Model.

Problem: The RESET_N pad (pin M14) does not pass ESD tests above 800V.

Work-around: Observe proper ESD handling precautions for the RESET_N pin

Schedule for Fix: Next Revision