ERRATA SHEET

Date: 2009 August 12
Document Release: Version 1.0
Device Affected: LPC313x

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2009 Aug 12

NXP
Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
1.0	2009 Aug 12	First version

Identification

The typical LPC313x devices have the following top-side marking:

LPC313xxxxxxx

xxxxxxx

xxYYWW R[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC3130, LPC3131:

Revision Identifier (R)	Comment
‘-’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
BOOTROM.1	Booting from 1.8 V NAND flash timing issue	'-'

Functional Problems of LPC313x

BOOTROM.1 Booting from 1.8 V NAND flash timing issue

Introduction: The LPC313x family of devices have an internal BootROM which supports booting from multiple sources, including SPI Flash, NOR Flash, UART, USB, SD Card, and NAND Flash.

Problem: The BootROM's default read timing for the NAND Flash interface with a 12 MHz input signal will only work for Flash devices with a maximum Trea (Ready Access) time of 27ns or faster. This can be a problem for 1.8V NAND devices, preventing successful boot-up from 1.8V NAND Flash.

Work-around: Option 1: Ensure that the maximum Ready Access Time of the NAND device is 27ns or faster when using a 12MHz input signal.

Option 2: Use 3.3V NAND Flash rather than 1.8V NAND Flash since 3.3V NAND devices generally meet this timing restriction. Note that since the NAND Flash interface shares pins with the SDRAM interface, the SDRAM must also be 3.3V

Option 2: Boot from another supported interface (for example: a small SPI Flash device) and set the proper timing configuration for the 1.8V NAND Flash device(s) in the system before accessing 1.8V NAND Flash devices.

Schedule for Fix:Next Revision