# LPC2292/LPC2294

## 16-bit/32-bit ARM microcontrollers; 256 kB ISP/IAP flash with CAN, 10-bit ADC and external memory interface

**Rev. 03 — 26 September 2005**  **Product data sheet**

## 1. General description

The LPC2292/LPC2294 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, together with 256 kB of embedded high-speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

With their 144-pin package, low power consumption, various 32-bit timers, 8-channel 10-bit ADC, 2/4 (LPC2292/LPC2294) advanced CAN channels, PWM channels and up to nine external interrupt pins these microcontrollers are particularly suitable for automotive and industrial control applications as well as medical systems and fault-tolerant maintenance buses. The number of available GPIOs ranges from 76 (with external memory) through 112 (single-chip). With a wide range of additional serial communications interfaces, they are also suited for communication gateways and protocol converters as well as many other general-purpose applications.

## 2. Features

### 2.1 Key features

- 16-bit/32-bit ARM7TDMI-S microcontroller in a LQFP144 package.
- 16 kB on-chip static RAM and 256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip boot-loader software. Single flash sector or full chip erase in 400 ms and programming of 256 bytes in 1 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software as well as high-speed real-time tracing of instruction execution.
- Two/four (LPC2292/2294) interconnected CAN interfaces with advanced acceptance filters. Additional serial interfaces include two UARTs (16C550), Fast I$^2$C-bus (400 kbits/s) and two SPIs.
- Eight channel 10-bit ADC with conversion time as low as 2.44 $\mu$s.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC) and watchdog.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8-bit/16-bit/32-bit data width.

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- Up to 112 general purpose I/O pins (5 V tolerant). Up to nine edge/level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 $\mu$s.
- On-chip crystal oscillator with an operating range of 1 MHz to 30 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V $\pm$ 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V $\pm$ 10 %) with 5 V tolerant I/O pads.

# 3. Ordering information

**Table 1:    Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | **Name** | **Description** | **Version** |
| LPC2292FBD144 | LQFP144 | plastic low profile quad flat package; 144 leads; body 20 $\times$ 20 $\times$ 1.4 mm | SOT486-1 |
| LPC2292FET144 | TFBGA144 | plastic thin fine-pitch ball grid array package; 144 balls; body 12 $\times$ 12 $\times$ 0.8 mm | SOT569-1 |
| LPC2294HBD144 | LQFP144 | plastic low profile quad flat package; 144 leads; body 20 $\times$ 20 $\times$ 1.4 mm | SOT486-1 |

## 3.1  Ordering options

**Table 2:    Ordering options**

| Type number | Flash memory | RAM | CAN | Temperature range ($^\circ$C) |
|---|---|---|---|---|
| LPC2292FBD144 | 256 kB | 16 kB | 2 channels | −40 to +85 |
| LPC2292FET144 | 256 kB | 16 kB | 2 channels | −40 to +85 |
| LPC2294HBD144 | 256 kB | 16 kB | 4 channels | −40 to +125 |

# 4. Block diagram
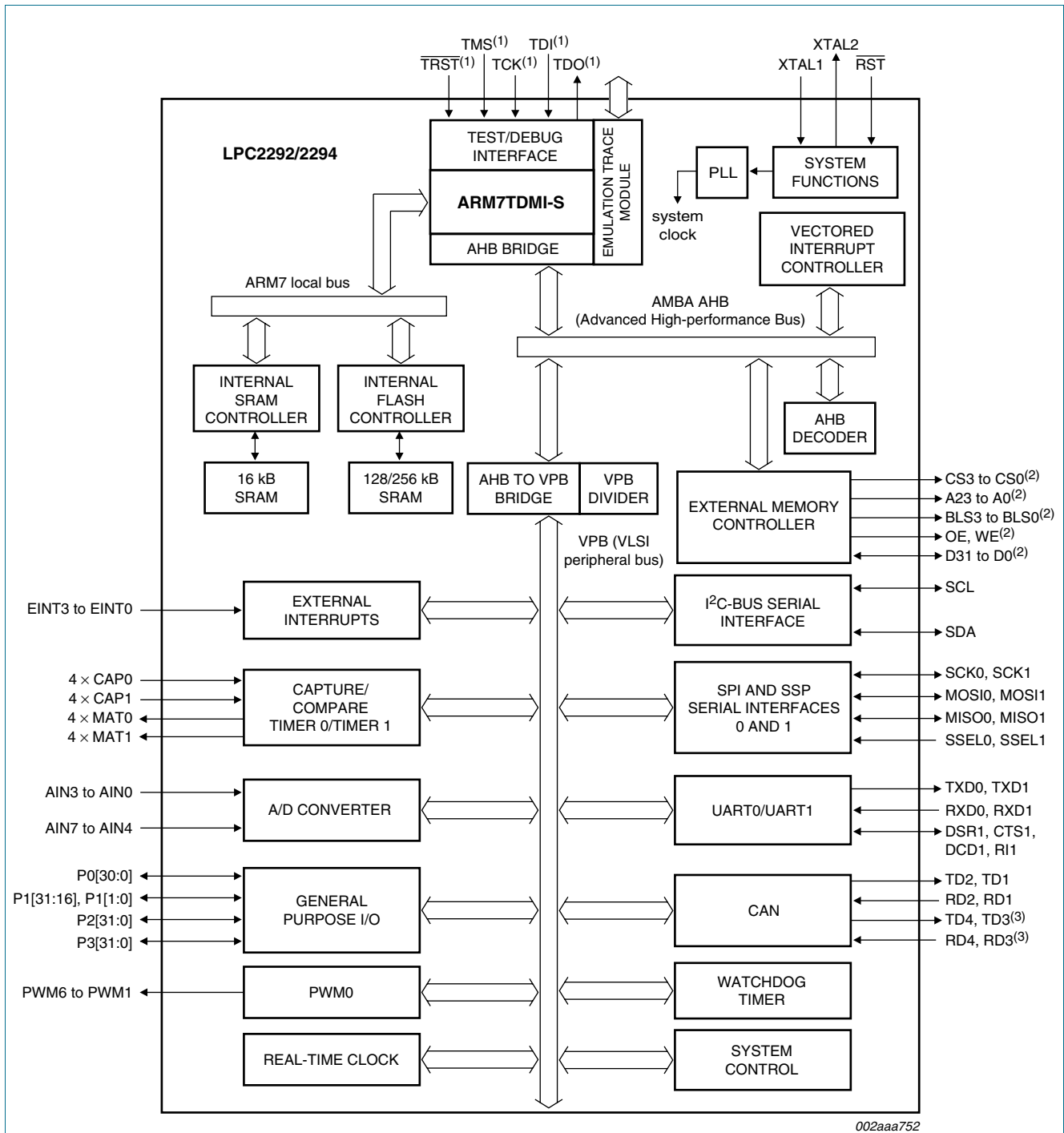


(1) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(2) Pins shared with GPIO.

(3) Available in LPC2294 only.

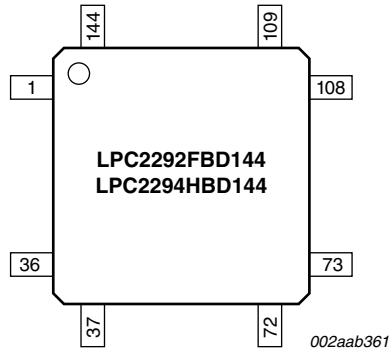**Fig 1. Block diagram**

# 5. Pinning information
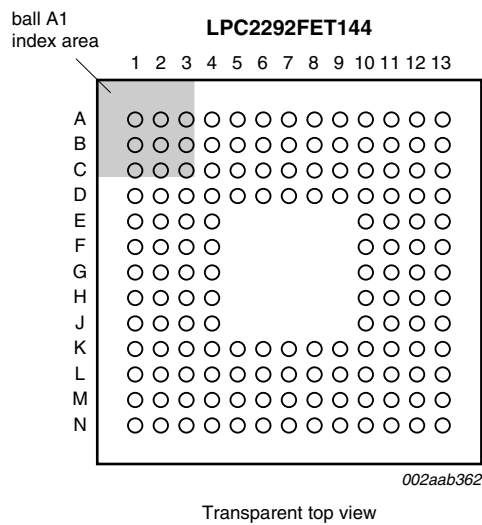
## 5.1 Pinning



**Fig 2.   LQFP144 pinning**



**Fig 3.   TFBGA144 pinning**

**Table 3:    Ball allocation**

| Row | Column 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | P2.22/ D22 | $V_{DDA(1V8)}$ | P1.28/ TDI | P2.21/ D21 | P2.18/ D18 | P2.14/ D14 | P1.29/ TCK | P2.11/ D11 | P2.10/ D10 | P2.7/D7 | $V_{DD(3V3)}$ | $V_{DD(1V8)}$ | P2.4/D4 |
| B | $V_{DD(3V3)}$ | P1.27/ TDO | XTAL2 | $V_{SSA(PLL)}$ | P2.19/ D19 | P2.15/ D15 | P2.12/ D12 | P0.20/ MAT1.3/ SSEL1/ EINT3 | $V_{DD(3V3)}$ | P2.6/D6 | $V_{SS}$ | P2.3/D3 | $V_{SS}$ |
| C | P0.21/ PWM5/ CAP1.3 | $V_{SS}$ | XTAL1 | $V_{SSA}$ | $\overline{RESET}$ | P2.16/ D16 | P2.13/ D13 | P0.19/ MAT1.2/ MOSI1/ CAP1.2 | P2.9/D9 | P2.5/D5 | P2.2/D2 | P2.1/D1 | $V_{DD(3V3)}$ |
| D | P0.24/ TD2 | P1.19/ TRACEP KT3 | P0.23/ RD2 | P0.22/ CAP0.0/ MAT0.0 | P2.20/ D20 | P2.17/ D17 | $V_{SS}$ | P0.18/ CAP1.3/ MISO1/ MAT1.3 | P2.8/D8 | P1.30/ TMS | $V_{SS}$ | P1.20/ TRACES YNC | P0.17/ CAP1.2/ SCK1/ MAT1.2 |
| E | P2.25/ D25 | P2.24/ D24 | P2.23 | $V_{SS}$ | | | | | | P0.16/ EINT0/ MAT0.2/ CAP0.2 | P0.15/ RI1/ EINT2 | P2.0/D0 | P3.30/ BLS1 |
| F | P2.27/ D27/ BOOT1 | P1.18/ TRACEP KT2 | $V_{DDA(3V3)}$ | P2.26/ D26/ BOOT0 | | | | | | P3.31/ BLS0 | P1.21/ PIPESTAT 0 | $V_{DD(3V3)}$ | $V_{SS}$ |
| G | P2.29/ D29 | P2.28/ D28 | P2.30/ D30/AIN4 | P2.31/ D31/AIN5 | | | | | | P0.14/ DCD1/ EINT1 | P1.0/CS0 | P3.0/A0 | P1.1/OE |
| H | P0.25/ RD1 | TD1 | P0.27/ AIN0/ CAP0.1/ MAT0.1 | P1.17/ TRACEP KT1 | | | | | | P0.13/ DTR1/ MAT1.1 | P1.22/ PIPESTAT 1 | P3.2/A2 | P3.1/A1 |
| J | P0.28/ AIN1/ CAP0.2/ MAT0.2 | $V_{SS}$ | P3.29/ BLS2/ AIN6 | P3.28/ BLS3/ AIN7 | | | | | | P3.3/A3 | P1.23/ PIPESTAT 2 | P0.11/ CTS1/ CAP1.1 | P0.12/ DSR1/ MAT1.0 |
| K | P3.27/WE | P3.26/ CS1 | $V_{DD(3V3)}$ | P3.22/ A22 | P3.20/ A20 | P0.1/ RXD0/ PWM3/ EINT0 | P3.14/ A14 | P1.25/ EXTIN0 | P3.11/ A11 | $V_{DD(3V3)}$ | P0.10/ RTS1/ CAP1.0 | $V_{SS}$ | P3.4/A4 |

**Table 3:    Ball allocation** *…continued*

| Row | Column | | | | | | | | | | | | |
|-----|--------|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
| L | P0.29/ AIN2/ CAP0.3/ MAT0.3 | P0.30/ AIN3/ EINT3/ CAP0.0 | P1.16/ TRACEPKT0 | P0.0/ TXD0/ PWM1 | P3.19/ A19 | P0.2/ SCL/ CAP0.0 | P3.15/ A15 | P0.4/ SCK0/ CAP0.1 | P3.12/ A12 | V$_{SS}$ | P1.24/ TRACECLK | P0.8/ TXD1/ PWM4 | P0.9/ RXD1/ PWM6/ EINT3 |
| M | P3.25/ CS2 | P3.24/ CS3 | V$_{DD(3V3)}$ | P1.31/ $\overline{TRST}$ | P3.18/ A18 | V$_{DD(3V3)}$ | P3.16/ A16 | P0.3/ SDA/ MAT0.0/ EINT1 | P3.13/ A13 | P3.9/A9 | P0.7/ SSEL0/ PWM2/ EINT2 | P3.7/A7 | P3.5/A5 |
| N | V$_{DD(1V8)}$ | V$_{SS}$ | P3.23/ A23/ XCLK | P3.21/ A21 | P3.17/ A17 | P1.26/ RTCK | V$_{SS}$ | V$_{DD(3V3)}$ | P0.5/ MISO0/ MAT0.1 | P3.10/ A10 | P0.6/ MOSI0/ CAP0.2 | P3.8/A8 | P3.6/A6 |

## 5.2 Pin description

**Table 4:     Pin description**

| Symbol | Pin (LQFP) | Pin (TFBGA) [1] | Type | Description |
|---|---|---|---|---|
| P0.0 to P0.31 | | | I/O | **Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block.<br><br>Pins 26 and 31 of port 0 are not available. |
| P0.0/TXD0/ PWM1 | 42 [2] | L4 [2] | O | **TXD0** — Transmitter output for UART0. |
| | | | O | **PWM1** — Pulse Width Modulator output 1. |
| P0.1/RXD0/ PWM3/EINT0 | 49 [3] | K6 [3] | I | **RXD0** — Receiver input for UART0. |
| | | | O | **PWM3** — Pulse Width Modulator output 3. |
| | | | I | **EINT0** — External interrupt 0 input |
| P0.2/SCL/ CAP0.0 | 50 [4] | L6 [4] | I/O | **SCL** — I2C-bus clock input/output. Open-drain output (for I2C-bus compliance). |
| | | | I | **CAP0.0** — Capture input for Timer 0, channel 0. |
| P0.3/SDA/ MAT0.0/EINT1 | 58 [4] | M8 [4] | I/O | **SDA** — I2C-bus data input/output. Open-drain output (for I2C-bus compliance). |
| | | | O | **MAT0.0** — Match output for Timer 0, channel 0. |
| | | | I | **EINT1** — External interrupt 1 input. |
| P0.4/SCK0/ CAP0.1 | 59 [2] | L8 [2] | I/O | **SCK0** — Serial clock for SPI0. SPI clock output from master or input to slave. |
| | | | I | **CAP0.1** — Capture input for Timer 0, channel 1. |
| P0.5/MISO0/ MAT0.1 | 61 [2] | N9 [2] | I/O | **MISO0** — Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave. |
| | | | O | **MAT0.1** — Match output for Timer 0, channel 1. |
| P0.6/MOSI0/ CAP0.2 | 68 [2] | N11 [2] | I/O | **MOSI0** — Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave. |
| | | | I | **CAP0.2** — Capture input for Timer 0, channel 2. |
| P0.7/SSEL0/ PWM2/EINT2 | 69 [3] | M11 [3] | I | **SSEL0** — Slave Select for SPI0. Selects the SPI interface as a slave. |
| | | | O | **PWM2** — Pulse Width Modulator output 2. |
| | | | I | **EINT2** — External interrupt 2 input. |
| P0.8/TXD1/ PWM4 | 75 [2] | L12 [2] | O | **TXD1** — Transmitter output for UART1. |
| | | | O | **PWM4** — Pulse Width Modulator output 4. |
| P0.9/RXD1/ PWM6/EINT3 | 76 [3] | L13 [3] | I | **RXD1** — Receiver input for UART1. |
| | | | O | **PWM6** — Pulse Width Modulator output 6. |
| | | | I | **EINT3** — External interrupt 3 input. |
| P0.10/RTS1/ CAP1.0 | 78 [2] | K11 [2] | O | **RTS1** — Request to Send output for UART1. |
| | | | I | **CAP1.0** — Capture input for Timer 1, channel 0. |
| P0.11/CTS1/ CAP1.1 | 83 [2] | J12 [2] | I | **CTS1** — Clear to Send input for UART1. |
| | | | I | **CAP1.1** — Capture input for Timer 1, channel 1. |

**Table 4:**    **Pin description** …continued

| Symbol | Pin (LQFP) | Pin (TFBGA) [1] | Type | Description |
|---|---|---|---|---|
| P0.12/DSR1/ MAT1.0/RD4 | 84 [2] | J13 [2] | I | **DSR1 —** Data Set Ready input for UART1. |
| | | | O | **MAT1.0 —** Match output for Timer 1, channel 0. |
| | | | I | **RD4 —** CAN4 receiver input (LPC2294 only). |
| P0.13/DTR1/ MAT1.1/TD4 | 85 [2] | H10 [2] | O | **DTR1 —** Data Terminal Ready output for UART1. |
| | | | O | **MAT1.1 —** Match output for Timer 1, channel 1. |
| | | | O | **TD4 —** CAN4 transmitter output (LPC2294 only). |
| P0.14/DCD1/ EINT1 | 92 [3] | G10 [3] | I | **DCD1 —** Data Carrier Detect input for UART1. |
| | | | I | **EINT1 —** External interrupt 1 input. |
| | | | | **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip boot-loader to take over control of the part after reset. |
| P0.15/RI1/ EINT2 | 99 [3] | E11 [3] | I | **RI1 —** Ring Indicator input for UART1. |
| | | | I | **EINT2 —** External interrupt 2 input. |
| P0.16/EINT0/ MAT0.2/CAP0.2 | 100 [3] | E10 [3] | I | **EINT0 —** External interrupt 0 input. |
| | | | O | **MAT0.2 —** Match output for Timer 0, channel 2. |
| | | | I | **CAP0.2 —** Capture input for Timer 0, channel 2. |
| P0.17/CAP1.2/ SCK1/MAT1.2 | 101 [2] | D13 [2] | I | **CAP1.2 —** Capture input for Timer 1, channel 2. |
| | | | I/O | **SCK1 —** Serial Clock for SPI1. SPI clock output from master or input to slave. |
| | | | O | **MAT1.2 —** Match output for Timer 1, channel 2. |
| P0.18/CAP1.3/ MISO1/MAT1.3 | 121 [2] | D8 [2] | I | **CAP1.3 —** Capture input for Timer 1, channel 3. |
| | | | I/O | **MISO1 —** Master In Slave Out for SPI1. Data input to SPI master or data output from SPI slave. |
| | | | O | **MAT1.3 —** Match output for Timer 1, channel 3. |
| P0.19/MAT1.2/ MOSI1/CAP1.2 | 122 [2] | C8 [2] | O | **MAT1.2 —** Match output for Timer 1, channel 2. |
| | | | I/O | **MOSI1 —** Master Out Slave In for SPI1. Data output from SPI master or data input to SPI slave. |
| | | | I | **CAP1.2 —** Capture input for Timer 1, channel 2. |
| P0.20/MAT1.3/ SSEL1/ EINT3 | 123 [3] | B8 [3] | O | **MAT1.3 —** Match output for Timer 1, channel 3. |
| | | | I | **SSEL1 —** Slave Select for SPI1. Selects the SPI interface as a slave. |
| | | | I | **EINT3 —** External interrupt 3 input. |
| P0.21/PWM5/ RD3/CAP1.3 | 4 [2] | C1 [2] | O | **PWM5 —** Pulse Width Modulator output 5. |
| | | | I | **RD3 —** CAN3 receiver input (LPC2294 only). |
| | | | I | **CAP1.3 —** Capture input for Timer 1, channel 3. |
| P0.22/CAP0.0/ MAT0.0 | 5 [2] | D4 [2] | O | **TD3 —** CAN3 transmitter output (LPC2294 only). |
| | | | I | **CAP0.0 —** Capture input for Timer 0, channel 0. |
| | | | O | **MAT0.0 —** Match output for Timer 0, channel 0. |
| P0.23/RD2 | 6 [2] | D3 [2] | I | **RD2 —** CAN2 receiver input. |
| P0.24/TD2 | 8 [2] | D1 [2] | O | **TD2 —** CAN2 transmitter output. |
| P0.25 | 21 [2] | H1 [2] | I | **RD1 —** CAN1 receiver input. |

**Table 4:** **Pin description** …*continued*

| Symbol | Pin (LQFP) | Pin (TFBGA) [1] | Type | Description |
|---|---|---|---|---|
| P0.27/AIN0/ CAP0.1/MAT0.1 | 23 [5] | H3 [5] | I | **AIN0** — ADC, input 0. This analog input is always connected to its pin. |
| | | | I | **CAP0.1** — Capture input for Timer 0, channel 1. |
| | | | O | **MAT0.1** — Match output for Timer 0, channel 1. |
| P0.28/AIN1/ CAP0.2/MAT0.2 | 25 [5] | J1 [5] | I | **AIN1** — ADC, input 1. This analog input is always connected to its pin. |
| | | | I | **CAP0.2** — Capture input for Timer 0, channel 2. |
| | | | O | **MAT0.2** — Match output for Timer 0, channel 2. |
| P0.29/AIN2/ CAP0.3/MAT0.3 | 32 [5] | L1 [5] | I | **AIN2** — ADC, input 2. This analog input is always connected to its pin. |
| | | | I | **CAP0.3** — Capture input for Timer 0, Channel 3. |
| | | | O | **MAT0.3** — Match output for Timer 0, channel 3. |
| P0.30/AIN3/ EINT3/CAP0.0 | 33 [5] | L2 [5] | I | **AIN3** — ADC, input 3. This analog input is always connected to its pin. |
| | | | I | **EINT3** — External interrupt 3 input. |
| | | | I | **CAP0.0** — Capture input for Timer 0, channel 0. |
| P1.0 to P1.31 | | | I/O | **Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available. |
| P1.0/CS0 | 91 [6] | G11 [6] | O | **CS0** — LOW-active Chip Select 0 signal. (Bank 0 addresses range 8000 0000 to 80FF FFFF) |
| P1.1/OE | 90 [6] | G13 [6] | O | **OE** — LOW-active Output Enable signal. |
| P1.16/ TRACEPKT0 | 34 [6] | L3 [6] | O | **TRACEPKT0** — Trace Packet, bit 0. Standard I/O port with internal pull-up. |
| P1.17/ TRACEPKT1 | 24 [6] | H4 [6] | O | **TRACEPKT1** — Trace Packet, bit 1. Standard I/O port with internal pull-up. |
| P1.18/ TRACEPKT2 | 15 [6] | F2 [6] | O | **TRACEPKT2** — Trace Packet, bit 2. Standard I/O port with internal pull-up. |
| P1.19/ TRACEPKT3 | 7 [6] | D2 [6] | O | **TRACEPKT3** — Trace Packet, bit 3. Standard I/O port with internal pull-up. |
| P1.20/ TRACESYNC | 102 [6] | D12 [6] | O | **TRACESYNC** — Trace Synchronization. Standard I/O port with internal pull-up. **Note:** LOW on this pin while $\overline{RESET}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset. |
| P1.21/ PIPESTAT0 | 95 [6] | F11 [6] | O | **PIPESTAT0** — Pipeline Status, bit 0. Standard I/O port with internal pull-up. |
| P1.22/ PIPESTAT1 | 86 [6] | H11 [6] | O | **PIPESTAT1** — Pipeline Status, bit 1. Standard I/O port with internal pull-up. |
| P1.23/ PIPESTAT2 | 82 [6] | J11 [6] | O | **PIPESTAT2** — Pipeline Status, bit 2. Standard I/O port with internal pull-up. |
| P1.24/ TRACECLK | 70 [6] | L11 [6] | O | **TRACECLK** — Trace Clock. Standard I/O port with internal pull-up. |

**Table 4:** **Pin description** …*continued*

| Symbol | Pin (LQFP) | Pin (TFBGA) [1] | Type | Description |
|---|---|---|---|---|
| P1.25/EXTIN0 | 60 [6] | K8 [6] | I | **EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up. |
| P1.26/RTCK | 52 [6] | N6 [6] | I/O | **RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up.<br>**Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset. |
| P1.27/TDO | 144 [6] | B2 [6] | O | **TDO —** Test Data out for JTAG interface. |
| P1.28/TDI | 140 [6] | A3 [6] | I | **TDI —** Test Data in for JTAG interface. |
| P1.29/TCK | 126 [6] | A7 [6] | I | **TCK —** Test Clock for JTAG interface. |
| P1.30/TMS | 113 [6] | D10 [6] | I | **TMS —** Test Mode Select for JTAG interface. |
| P1.31/$\overline{\text{TRST}}$ | 43 [6] | M4 [6] | I | **$\overline{\text{TRST}}$ —** Test Reset for JTAG interface. |
| P2.0 to P2.31 | | | I/O | **Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block. |
| P2.0/D0 | 98 [6] | E12 [6] | I/O | **D0 —** External memory data line 0. |
| P2.1/D1 | 105 [6] | C12 [6] | I/O | **D1 —** External memory data line 1. |
| P2.2/D2 | 106 [6] | C11 [6] | I/O | **D2 —** External memory data line 2. |
| P2.3/D3 | 108 [6] | B12 [6] | I/O | **D3 —** External memory data line 3. |
| P2.4/D4 | 109 [6] | A13 [6] | I/O | **D4 —** External memory data line 4. |
| P2.5/D5 | 114 [6] | C10 [6] | I/O | **D5 —** External memory data line 5. |
| P2.6/D6 | 115 [6] | B10 [6] | I/O | **D6 —** External memory data line 6. |
| P2.7/D7 | 116 [6] | A10 [6] | I/O | **D7 —** External memory data line 7. |
| P2.8/D8 | 117 [6] | D9 [6] | I/O | **D8 —** External memory data line 8. |
| P2.9/D9 | 118 [6] | C9 [6] | I/O | **D9 —** External memory data line 9. |
| P2.10/D10 | 120 [6] | A9 [6] | I/O | **D10 —** External memory data line 10. |
| P2.11/D11 | 124 [6] | A8 [6] | I/O | **D11 —** External memory data line 11. |
| P2.12/D12 | 125 [6] | B7 [6] | I/O | **D12 —** External memory data line 12. |
| P2.13/D13 | 127 [6] | C7 [6] | I/O | **D13 —** External memory data line 13. |
| P2.14/D14 | 129 [6] | A6 [6] | I/O | **D14 —** External memory data line 14. |
| P2.15/D15 | 130 [6] | B6 [6] | I/O | **D15 —** External memory data line 15. |
| P2.16/D16 | 131 [6] | C6 [6] | I/O | **D16 —** External memory data line 16. |
| P2.17/D17 | 132 [6] | D6 [6] | I/O | **D17 —** External memory data line 17. |
| P2.18/D18 | 133 [6] | A5 [6] | I/O | **D18 —** External memory data line 18. |
| P2.19/D19 | 134 [6] | B5 [6] | I/O | **D19 —** External memory data line 19. |
| P2.20/D20 | 136 [6] | D5 [6] | I/O | **D20 —** External memory data line 20. |
| P2.21/D21 | 137 [6] | A4 [6] | I/O | **D21 —** External memory data line 21. |
| P2.22/D22 | 1 [6] | A1 [6] | I/O | **D22 —** External memory data line 22. |
| P2.23/D23 | 10 [6] | E3 [6] | I/O | **D23 —** External memory data line 23. |
| P2.24/D24 | 11 [6] | E2 [6] | I/O | **D24 —** External memory data line 24. |

**Table 4:** **Pin description** …*continued*

| Symbol | Pin (LQFP) | Pin (TFBGA) [1] | Type | Description |
|---|---|---|---|---|
| P2.25/D25 | 12 [6] | E1 [6] | I/O | **D25 —** External memory data line 25. |
| P2.26/D26/ BOOT0 | 13 [6] | F4 [6] | I/O | **D26 —** External memory data line 26. |
| | | | I | **BOOT0 —** While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. |
| P2.27/D27/ BOOT1 | 16 [6] | F1 [6] | I/O | **D27 —** External memory data line 27. |
| | | | I | **BOOT1 —** While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. |
| | | | | BOOT1:0 = 00 selects 8-bit memory on CS0 for boot. |
| | | | | BOOT1:0 = 01 selects 16-bit memory on CS0 for boot. |
| | | | | BOOT1:0 = 10 selects 32-bit memory on CS0 for boot. |
| | | | | BOOT1:0 = 11 selects internal flash memory. |
| P2.28/D28 | 17 [6] | G2 [6] | I/O | **D28 —** External memory data line 28. |
| P2.29/D29 | 18 [6] | G1 [6] | I/O | **D29 —** External memory data line 29. |
| P2.30/D30/ AIN4 | 19 [3] | G3 [3] | I/O | **D30 —** External memory data line 30. |
| | | | I | **AIN4 —** ADC, input 4. This analog input is always connected to its pin. |
| P2.31/D31/ AIN5 | 20 [3] | G4 [3] | I/O | **D31 —** External memory data line 31. |
| | | | I | **AIN5 —** ADC, input 5. This analog input is always connected to its pin. |
| P3.0 to P3.31 | | | I/O | **Port 3 —** Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block. |
| P3.0/A0 | 89 [6] | G12 [6] | O | **A0 —** External memory address line 0. |
| P3.1/A1 | 88 [6] | H13 [6] | O | **A1 —** External memory address line 1. |
| P3.2/A2 | 87 [6] | H12 [6] | O | **A2 —** External memory address line 2. |
| P3.3/A3 | 81 [6] | J10 [6] | O | **A3 —** External memory address line 3. |
| P3.4/A4 | 80 [6] | K13 [6] | O | **A4 —** External memory address line 4. |
| P3.5/A5 | 74 [6] | M13 [6] | O | **A5 —** External memory address line 5. |
| P3.6/A6 | 73 [6] | N13 [6] | O | **A6 —** External memory address line 6. |
| P3.7/A7 | 72 [6] | M12 [6] | O | **A7 —** External memory address line 7. |
| P3.8/A8 | 71 [6] | N12 [6] | O | **A8 —** External memory address line 8. |
| P3.9/A9 | 66 [6] | M10 [6] | O | **A9 —** External memory address line 9. |
| P3.10/A10 | 65 [6] | N10 [6] | O | **A10 —** External memory address line 10. |
| P3.11/A11 | 64 [6] | K9 [6] | O | **A11 —** External memory address line 11. |
| P3.12/A12 | 63 [6] | L9 [6] | O | **A12 —** External memory address line 12. |
| P3.13/A13 | 62 [6] | M9 [6] | O | **A13 —** External memory address line 13. |
| P3.14/A14 | 56 [6] | K7 [6] | O | **A14 —** External memory address line 14. |
| P3.15/A15 | 55 [6] | L7 [6] | O | **A15 —** External memory address line 15. |
| P3.16/A16 | 53 [6] | M7 [6] | O | **A16 —** External memory address line 16. |
| P3.17/A17 | 48 [6] | N5 [6] | O | **A17 —** External memory address line 17. |

**Table 4:** **Pin description** …continued

| Symbol | Pin (LQFP) | Pin (TFBGA) [1] | Type | Description |
|---|---|---|---|---|
| P3.18/A18 | 47 [6] | M5 [6] | O | **A18 —** External memory address line 18. |
| P3.19/A19 | 46 [6] | L5 [6] | O | **A19 —** External memory address line 19. |
| P3.20/A20 | 45 [6] | K5 [6] | O | **A20 —** External memory address line 20. |
| P3.21/A21 | 44 [6] | N4 [6] | O | **A21 —** External memory address line 21. |
| P3.22/A22 | 41 [6] | K4 [6] | O | **A22 —** External memory address line 22. |
| P3.23/A23/ XCLK | 40 [6] | N3 [6] | I/O | **A23 —** External memory address line 23. |
|  |  |  | O | **XCLK —** Clock output. |
| P3.24/CS3 | 36 [6] | M2 [6] | O | **CS3 —** LOW-active Chip Select 3 signal. |
|  |  |  |  | (Bank 3 addresses range 8300 0000 to 83FF FFFF) |
| P3.25/CS2 | 35 [6] | M1 [6] | O | **CS2 —** LOW-active Chip Select 2signal. |
|  |  |  |  | (Bank 2 addresses range 8200 0000 to 82FF FFFF) |
| P3.26/CS1 | 30 [6] | K2 [6] | O | **CS1 —** LOW-active Chip Select 1 signal. |
|  |  |  |  | (Bank 1 addresses range 8100 0000 to 81FF FFFF) |
| P3.27/WE | 29 [6] | K1 [6] | O | **WE —** LOW-active Write enable signal. |
| P3.28/BLS3/ AIN7 | 28 [3] | J4 [3] | O | **BLS3 —** LOW-active Byte Lane Select signal (Bank 3). |
|  |  |  | I | **AIN7 —** ADC, input 7. This analog input is always connected to its pin. |
| P3.29/BLS2/ AIN6 | 27 [5] | J3 [5] | O | **BLS2 —** LOW-active Byte Lane Select signal (Bank 2). |
|  |  |  | I | **AIN6 —** ADC, input 6. This analog input is always connected to its pin. |
| P3.30/BLS1 | 97 [5] | E13 [5] | O | **BLS1 —** LOW-active Byte Lane Select signal (Bank 1). |
| P3.31/BLS0 | 96 [5] | F10 [5] | O | **BLS0 —** LOW-active Byte Lane Select signal (Bank 0). |
| TD1 | 22 [6] | H2 [6] | O | **TD1:** CAN1 transmitter output. |
| RESET | 135 [7] | C5 [7] | I | **External Reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant. |
| XTAL1 | 142 [8] | C3 [8] | I | Input to the oscillator circuit and internal clock generator circuits. |
| XTAL2 | 141 [8] | B3 [8] | O | Output from the oscillator amplifier. |
| $V_{SS}$ | 3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128 | C2, E4, J2, N2, N7, L10, K12, F13, D11, B13, B11, D7 | I | **Ground:** 0 V reference. |
| $V_{SSA}$ | 139 | C4 | I | **Analog ground:** 0 V reference. This should nominally be the same voltage as $V_{SS}$, but should be isolated to minimize noise and error. |
| $V_{SSA(PLL)}$ | 138 | B4 | I | **PLL analog ground:** 0 V reference. This should nominally be the same voltage as $V_{SS}$, but should be isolated to minimize noise and error. |
| $V_{DD(1V8)}$ | 37, 110 | N1, A12 | I | **1.8 V core power supply:** This is the power supply voltage for internal circuitry. |

**Table 4:** **Pin description** …continued

| Symbol | Pin (LQFP) | Pin (TFBGA) [1] | Type | Description |
|---|---|---|---|---|
| $V_{DDA(1V8)}$ | 143 | A2 | I | **Analog 1.8 V core power supply:** This is the power supply voltage for internal circuitry. This should be nominally the same voltage as $V_{DD(1V8)}$ but should be isolated to minimize noise and error. |
| $V_{DD(3V3)}$ | 2, 31, 39, 51, 57, 77, 94, 104, 112, 119 | B1, K3, M3, M6, N8, K10, F12, C13, A11, B9 | I | **3.3 V pad power supply:** This is the power supply voltage for the I/O ports. |
| $V_{DDA(3V3)}$ | 14 | F3 | I | **Analog 3.3 V pad power supply:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. |

[1] LPC2294 only.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[3] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[4] Open drain 5 V tolerant digital I/O I$^2$C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[5] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for a digital input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value ranges from 60 k$\Omega$ to 300 k$\Omega$.

[7] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[8] Pad provides special analog functionality.

# 6. Functional description

## 6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISC. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.

- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

## 6.2 On-chip flash program memory

The LPC2292/LPC2294 incorporate a 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When the on-chip boot loader is used, 248 kB of flash memory is available for user code.

The LPC2292/LPC2294 flash memory provides a minimum of 100,000 erase/write cycles and 20 years of data retention.

On-chip boot loader (as of revision 1.60) provides Code Read Protection (CRP) for the LPC2292/LPC2294 on-chip flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip RAM or flash memory are disabled. However, the ISP flash erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

## 6.3 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8-bits, 16-bits, and 32-bits. The LPC2292/LPC2294 provide 16 kB of SRAM.

## 6.4 Memory map

The LPC2292/LPC2294 memory maps incorporate several distinct regions, as shown in Figure 4.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.21 "System control".
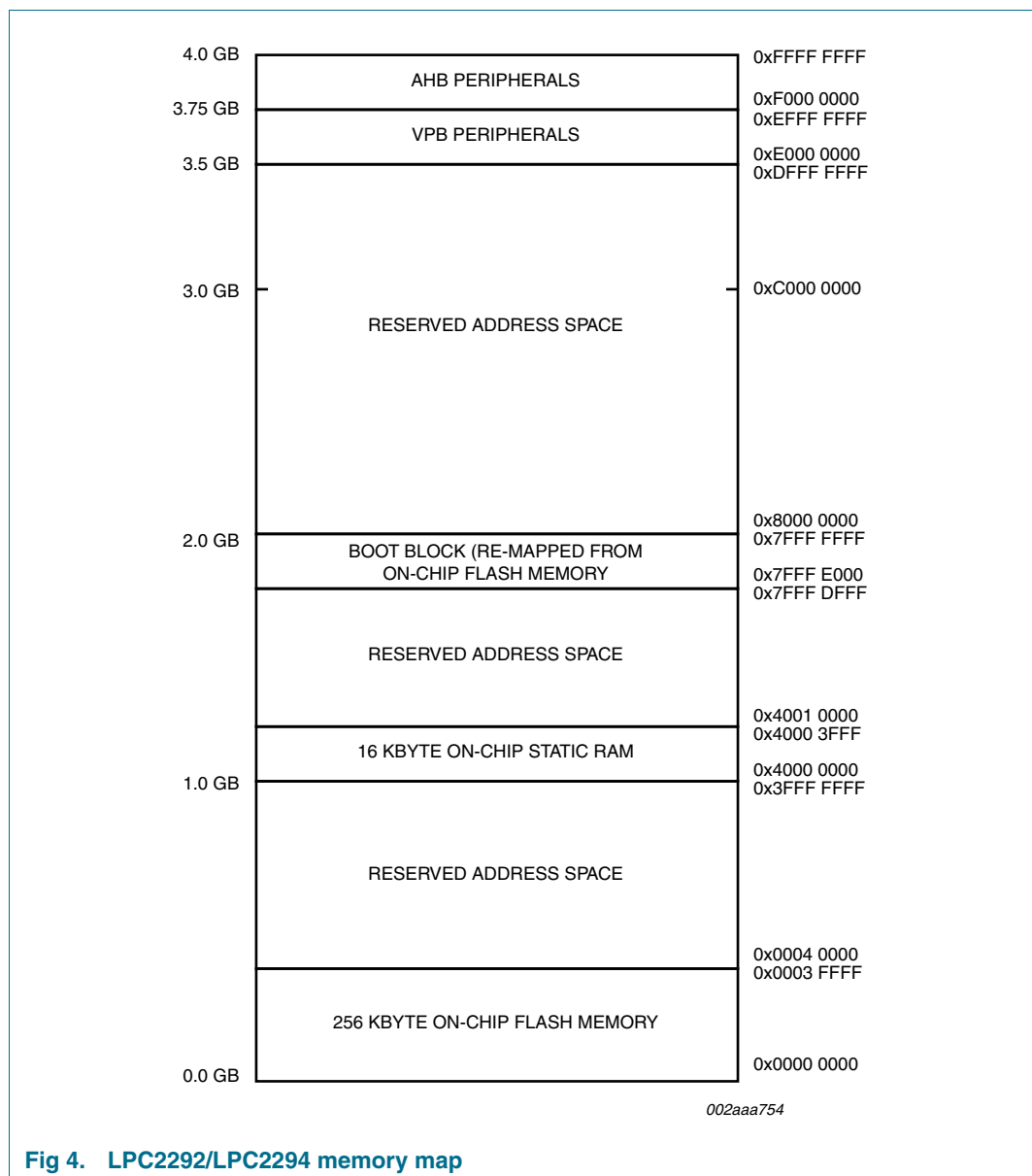


**Fig 4.** **LPC2292/LPC2294 memory map**

## 6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as FIQ, vectored IRQ, and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Fast Interrupt reQuest (FIQ) has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

### 6.5.1 Interrupt sources

Table 5 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

**Table 5:** **Interrupt sources**

| Block | Flag(s) | VIC channel # |
|---|---|---|
| WDT | Watchdog Interrupt (WDINT) | 0 |
| - | Reserved for software interrupts only | 1 |
| ARM Core | EmbeddedICE, DbgCommRx | 2 |
| ARM Core | EmbeddedICE, DbgCommTx | 3 |
| Timer 0 | Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3) | 4 |
| Timer 1 | Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3) | 5 |
| UART0 | RX Line Status (RLS) Transmit Holding Register empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) | 6 |

**Table 5:** **Interrupt sources** *…continued*

| Block | Flag(s) | VIC channel # |
|---|---|---|
| UART1 | RX Line Status (RLS) | 7 |
| | Transmit Holding Register empty (THRE) | |
| | RX Data Available (RDA) | |
| | Character Time-out Indicator (CTI) | |
| | Modem Status Interrupt (MSI) | |
| PWM0 | Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6) | 8 |
| I2C | SI (state change) | 9 |
| SPI0 | SPIF, MODF | 10 |
| SPI1 | SPIF, MODF | 11 |
| PLL | PLL Lock (PLOCK) | 12 |
| RTC | RTCCIF (Counter Increment), RTCALF (Alarm) | 13 |
| System Control | External Interrupt 0 (EINT0) | 14 |
| | External Interrupt 1 (EINT1) | 15 |
| | External Interrupt 2 (EINT2) | 16 |
| | External Interrupt 3 (EINT3) | 17 |
| A/D | ADC | 18 |
| CAN | 1 ORed CAN Acceptance Filter | 19 |
| | CAN1 (TX int, RX int) | 20, 21 |
| | CAN2 (TX int, RX int) | 22, 23 |
| | CAN3 (TX int, RX int) - LPC2294 only | 24, 25 |
| | CAN4 (TX int, RX int) - LPC2294 only | 26, 27 |

## 6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The pin control module contains three registers as shown in Table 6.

**Table 6:** **Pin control module registers**

| Address | Name | Description | Access |
|---|---|---|---|
| 0xE002 C000 | PINSEL0 | pin function select register 0 | read/write |
| 0xE002 C004 | PINSEL1 | pin function select register 1 | read/write |
| 0xE002 C014 | PINSEL2 | pin function select register 2 | read/write |

## 6.7 Pin function select register 0 (PINSEL0 - 0xE002 C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in Table 7. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically. Settings other than those shown in Table 7 are reserved, and should not be used

**Table 7:** **Pin function select register 0 (PINSEL0 - 0xE002 C000)**

| PINSEL0 | Pin name | Value | | Function | Value after reset |
|---|---|---|---|---|---|
| 1:0 | P0.0 | 0 | 0 | GPIO Port 0.0 | 0 |
| | | 0 | 1 | TXD (UART0) | |
| | | 1 | 0 | PWM1 | |
| | | 1 | 1 | reserved | |
| 3:2 | P0.1 | 0 | 0 | GPIO Port 0.1 | 0 |
| | | 0 | 1 | RXD (UART0) | |
| | | 1 | 0 | PWM3 | |
| | | 1 | 1 | EINT0 | |
| 5:4 | P0.2 | 0 | 0 | GPIO Port 0.2 | 0 |
| | | 0 | 1 | SCL (I$^2$C-bus) | |
| | | 1 | 0 | Capture 0.0 (Timer 0) | |
| | | 1 | 1 | reserved | |
| 7:6 | P0.3 | 0 | 0 | GPIO Port 0.3 | 0 |
| | | 0 | 1 | SDA (I$^2$C-bus) | |
| | | 1 | 0 | Match 0.0 (Timer 0) | |
| | | 1 | 1 | EINT1 | |
| 9:8 | P0.4 | 0 | 0 | GPIO Port 0.4 | 0 |
| | | 0 | 1 | SCK (SPI0) | |
| | | 1 | 0 | Capture 0.1 (Timer 0) | |
| | | 1 | 1 | reserved | |
| 11:10 | P0.5 | 0 | 0 | GPIO Port 0.5 | 0 |
| | | 0 | 1 | MISO (SPI0) | |
| | | 1 | 0 | Match 0.1 (Timer 0) | |
| | | 1 | 1 | reserved | |
| 13:12 | P0.6 | 0 | 0 | GPIO Port 0.6 | 0 |
| | | 0 | 1 | MOSI (SPI0) | |
| | | 1 | 0 | Capture 0.2 (Timer 0) | |
| | | 1 | 1 | reserved | |
| 15:14 | P0.7 | 0 | 0 | GPIO Port 0.7 | 0 |
| | | 0 | 1 | SSEL (SPI0) | |
| | | 1 | 0 | PWM2 | |
| | | 1 | 1 | EINT2 | |
| 17:16 | P0.8 | 0 | 0 | GPIO Port 0.8 | 0 |
| | | 0 | 1 | TXD UART1 | |
| | | 1 | 0 | PWM4 | |
| | | 1 | 1 | reserved | |
| 19:18 | P0.9 | 0 | 0 | GPIO Port 0.9 | 0 |
| | | 0 | 1 | RXD (UART1) | |
| | | 1 | 0 | PWM6 | |
| | | 1 | 1 | EINT3 | |

**Table 7:    Pin function select register 0 (PINSEL0 - 0xE002 C000)** *...continued*

| PINSEL0 | Pin name | Value | | Function | Value after reset |
|---------|----------|-------|---|----------|-------------------|
| 21:20 | P0.10 | 0 | 0 | GPIO Port 0.10 | 0 |
| | | 0 | 1 | RTS (UART1) | |
| | | 1 | 0 | Capture 1.0 (Timer 1) | |
| | | 1 | 1 | reserved | |
| 23:22 | P0.11 | 0 | 0 | GPIO Port 0.11 | 0 |
| | | 0 | 1 | CTS (UART1) | |
| | | 1 | 0 | Capture 1.1 (Timer 1) | |
| | | 1 | 1 | reserved | |
| 25:24 | P0.12 | 0 | 0 | GPIO Port 0.12 | 0 |
| | | 0 | 1 | DSR (UART1) | |
| | | 1 | 0 | Match 1.0 (Timer 1) | |
| | | 1 | 1 | RD4 [1] (CAN Controller 4) | |
| 27:26 | P0.13 | 0 | 0 | GPIO Port 0.13 | 0 |
| | | 0 | 1 | DTR (UART1) | |
| | | 1 | 0 | Match 1.1 (Timer 1) | |
| | | 1 | 1 | TD4 [1] (CAN Controller 4) | |
| 29:28 | P0.14 | 0 | 0 | GPIO Port 0.14 | 0 |
| | | 0 | 1 | DCD (UART1) | |
| | | 1 | 0 | EINT1 | |
| | | 1 | 1 | reserved | |
| 31:30 | P0.15 | 0 | 0 | GPIO Port 0.15 | 0 |
| | | 0 | 1 | RI (UART1) | |
| | | 1 | 0 | EINT2 | |
| | | 1 | 1 | reserved | |

[1]    CAN controller 4 is available in LPC2294 only. Fields in Table 7 related to CAN4 have a reserved value for LPC2292.

## 6.8  Pin function select register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 8. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in Table 8 are reserved, and should not be used.

**Table 8:    Pin function select register 1 (PINSEL1 - 0xE002 C004)**

| PINSEL1 | Pin Name | Value | | Function | Value after reset |
|---------|----------|-------|---|----------|-------------------|
| 1:0 | P0.16 | 0 | 0 | GPIO Port 0.16 | 0 |
| | | 0 | 1 | EINT0 | |
| | | 1 | 0 | Match 0.2 (Timer 0) | |
| | | 1 | 1 | reserved | |

**Table 8:** **Pin function select register 1 (PINSEL1 - 0xE002 C004)** *…continued*

| PINSEL1 | Pin Name | Value | | Function | Value after reset |
|---------|----------|-------|---|----------|-------------------|
| 3:2 | P0.17 | 0 | 0 | GPIO Port 0.17 | 0 |
| | | 0 | 1 | Capture 1.2 (Timer 1) | |
| | | 1 | 0 | SCK (SPI1) | |
| | | 1 | 1 | Match 1.2 (Timer 1) | |
| 5:4 | P0.18 | 0 | 0 | GPIO Port 0.18 | 0 |
| | | 0 | 1 | Capture 1.3 (Timer 1) | |
| | | 1 | 0 | MISO (SPI1) | |
| | | 1 | 1 | Match 1.3 (Timer 1) | |
| 7:6 | P0.19 | 0 | 0 | GPIO Port 0.19 | 0 |
| | | 0 | 1 | Match 1.2 (Timer 1) | |
| | | 1 | 0 | MOSI (SPI1) | |
| | | 1 | 1 | Match 1.3 (Timer 1) | |
| 9:8 | P0.20 | 0 | 0 | GPIO Port 0.20 | 0 |
| | | 0 | 1 | Match 1.3 (Timer 1) | |
| | | 1 | 0 | SSEL (SPI1) | |
| | | 1 | 1 | EINT3 | |
| 11:10 | P0.21 | 0 | 0 | GPIO Port 0.21 | 0 |
| | | 0 | 1 | PWM5 | |
| | | 1 | 0 | RD3[1] (CAN Controller 3) | |
| | | 1 | 1 | Capture 1.3 (Timer 1) | |
| 13:12 | P0.22 | 0 | 0 | GPIO Port 0.22 | 0 |
| | | 0 | 1 | TD3[1] (CAN Controller 3) | |
| | | 1 | 0 | Capture 0.0 (Timer 0) | |
| | | 1 | 1 | Match 0.0 (Timer 0) | |
| 15:14 | P0.23 | 0 | 0 | GPIO Port 0.23 | 0 |
| | | 0 | 1 | RD2 (CAN Controller 2) | |
| | | 1 | 0 | reserved | |
| | | 1 | 1 | reserved | |
| 17:16 | P0.24 | 0 | 0 | GPIO Port 0.24 | 0 |
| | | 0 | 1 | TD2 (CAN Controller 2) | |
| | | 1 | 0 | reserved | |
| | | 1 | 1 | reserved | |
| 19:18 | P0.25 | 0 | 0 | GPIO Port 0.25 | 0 |
| | | 0 | 1 | RD1 (CAN Controller 1) | |
| | | 1 | 0 | reserved | |
| | | 1 | 1 | reserved | |
| 21:20 | P0.26 | 0 | 0 | reserved | 0 |
| | | 0 | 1 | reserved | |
| | | 1 | 0 | reserved | |
| | | 1 | 1 | reserved | |

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**Table 8:** Pin function select register 1 (PINSEL1 - 0xE002 C004) ...continued

| PINSEL1 | Pin Name | Value | | Function | Value after reset |
|---------|----------|-------|---|----------|-------------------|
| 23:22 | P0.27 | 0 | 0 | GPIO Port 0.27 | 1 |
| | | 0 | 1 | AIN0 (ADC) | |
| | | 1 | 0 | Capture 0.1 (Timer 0) | |
| | | 1 | 1 | Match 0.1 (Timer 0) | |
| 25:24 | P0.28 | 0 | 0 | GPIO Port 0.28 | 1 |
| | | 0 | 1 | AIN1 (ADC) | |
| | | 1 | 0 | Capture 0.2 (Timer 0) | |
| | | 1 | 1 | Match 0.2 (Timer 0) | |
| 27:26 | P0.29 | 0 | 0 | GPIO Port 0.29 | 1 |
| | | 0 | 1 | AIN2 (ADC) | |
| | | 1 | 0 | Capture 0.3 (Timer 0) | |
| | | 1 | 1 | Match 0.3 (Timer 0) | |
| 29:28 | P0.30 | 0 | 0 | GPIO Port 0.30 | 1 |
| | | 0 | 1 | AIN3 (ADC) | |
| | | 1 | 0 | EINT3 | |
| | | 1 | 1 | Capture 0.0 (Timer 0) | |
| 31:30 | P0.31 | 0 | 0 | reserved | 0 |
| | | 0 | 1 | reserved | |
| | | 1 | 0 | reserved | |
| | | 1 | 1 | reserved | |

[1] CAN controller 3 is available in LPC2294 only. Fields in Table 8 related to CAN3 have a reserved value for LPC2292.

## 6.9 Pin function select register 2 (PINSEL2 - 0xE002 C014)

The PINSEL2 register controls the functions of the pins as per the settings listed in Table 9. The direction control bit in the IODIR register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically. Settings other than those shown in Table 9 are reserved, and should not be used.

**Table 9:** Pin function select register 2 (PINSEL2 - 0xE002 C014)

| PINSEL2 bits | Description | Reset value |
|--------------|-------------|-------------|
| 1:0 | reserved | - |
| 2 | When 0, pins P1[36:26] are used as GPIO pins. When 1, P1[31:26] are used as a Debug port. | $\overline{\text{P1.26/RTCK}}$ |
| 3 | When 0, pins P1[25:16] are used as GPIO pins. When 1, P1[25:16] are used as a Trace port. | $\overline{\text{P1.20/}}$ $\overline{\text{TRACESYNC}}$ |

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**Table 9:** **Pin function select register 2 (PINSEL2 - 0xE002 C014)** *…continued*

| PINSEL2 bits | Description | | | Reset value |
|---|---|---|---|---|
| 5:4 | Controls the use of the data bus and strobe pins: | | | BOOT1:0 |
| | Pins P2[7:0] | 11 = P2[7:0] | 0x or 10 = D7 to D0 | |
| | Pin P1.0 | 11 = P1.0 | 0x or 10 = CS0 | |
| | Pin P1.1 | 11 = P1.1 | 0x or 10 = OE | |
| | Pin P3.31 | 11 = P3.31 | 0x or 10 = BLS0 | |
| | Pins P2[15:8] | 00 or 11 = P2[15:8] | 01 or 10 = D15 to D8 | |
| | Pin P3.30 | 00 or 11 = P3.30 | 01 or 10 = BLS1 | |
| | Pins P2[27:16] | 0x or 11 = P2[27:16] | 10 = D27 to D16 | |
| | Pins P2[29:28] | 0x or 11 = P2[29:28] or reserved | 10 = D29, D28 | |
| | Pins P2[31:30] | 0x or 11 = P2[31:30] or AIN5 to AIN4 | 10 = D31, D30 | |
| | Pins P3[29:28] | 0x or 11 = P3[29:28] or AIN7 to AIN6 | 10 = BLS2, BLS3 | |
| 6 | If bits 5:4 are not 10, controls the use of pin P3.29: 0 enables P3.29, 1 enables AIN6. | | | 1 |
| 7 | If bits 5:4 are not 10, controls the use of pin P3.28: 0 enables P3.28, 1 enables AIN7. | | | 1 |
| 8 | Controls the use of pin P3.27: 0 enables P3.27, 1 enables WE. | | | 0 |
| 10:9 | reserved | | | - |
| 11 | Controls the use of pin P3.26: 0 enables P3.26, 1 enables CS1. | | | 0 |
| 12 | reserved | | | - |
| 13 | If bits 25:23 are not 111, controls the use of pin P3.23/A23/XCLK: 0 enables P3.23, 1 enables XCLK. | | | 0 |
| 15:14 | Controls the use of pin P3.25: 00 enables P3.25, 01 enables CS2, 10 and 11 are reserved values. | | | 00 |
| 17:16 | Controls the use of pin P3.24: 00 enables P3.24, 01 enables CS3, 10 and 11 are reserved values. | | | 00 |
| 19:18 | reserved | | | - |
| 20 | If bits 5:4 are not 10, controls the use of pin P2[29:28]: 0 enables P2[29:28], 1 is reserved | | | 0 |
| 21 | If bits 5:4 are not 10, controls the use of pin P2.30: 0 enables P2.30, 1 enables AIN4. | | | 1 |
| 22 | If bits 5:4 are not 10, controls the use of pin P2.31: 0 enables P2.31, 1 enables AIN5. | | | 1 |
| 23 | Controls whether P3.0/A0 is a port pin (0) or an address line (1). | | | 1 if BOOT1:0 = 00 at $\overline{RESET}$ = 0, 0 otherwise |
| 24 | Controls whether P3.1/A1 is a port pin (0) or an address line (1). | | | $\overline{BOOT1}$ during reset |

**Table 9:** **Pin function select register 2 (PINSEL2 - 0xE002 C014)** ...*continued*

| PINSEL2 bits | Description | | Reset value |
|---|---|---|---|
| 27:25 | Controls the number of pins among P3.23/A23/XCLK and P3[22:2]/A2[22:2] that are address lines: | | 000 if BOOT1:0 = 11 at reset, 111 otherwise |
| | 000 = None | 100 = A11 to A2 are address lines. | |
| | 001 = A3 to A2 are address lines. | 101 = A15 to A2 are address lines. | |
| | 010 = A5 to A2 are address lines. | 110 = A19 to A2 are address lines. | |
| | 011 = A7 to A2 are address lines. | 111 = A23 to A2 are address lines. | |
| 31:28 | reserved | | |

## 6.10 External memory controller

The external Static Memory Controller is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8, 16, or 32-bits wide.

## 6.11 General purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

### 6.11.1 Features

- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

## 6.12 10-bit ADC

The LPC2292/LPC2294 each contain single 10-bit successive approximation ADC with eight multiplexed channels.

### 6.12.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400,000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

## 6.13 CAN controllers and acceptance filter

The LPC2292/LPC2294 each contain two/four CAN controllers. The CAN is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

### 6.13.1 Features

- Data rates up to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with CAN specification 2.0B, ISO 11898-1.
- Global Acceptance Filter recognizes 11-bit and 29-bit RX identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard identifiers.

## 6.14 UARTs

The LPC2292/LPC2294 each contain two UARTs. One UART provides a full modem control handshake interface, the other provides only transmit and receive data lines.

### 6.14.1 Features

- 16 byte Receive and Transmit FIFOs.
- Register locations conform to '550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes
- Built-in baud rate generator.
- Standard modem interface signals included on UART1.

## 6.15 I$^2$C-bus serial I/O controller

The I$^2$C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I$^2$C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I$^2$C-bus implemented in LPC2292/LPC2294 supports bit rate up to 400 kbit/s (Fast I$^2$C-bus).

### 6.15.1 Features

- Compliant with standard I$^2$C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.

- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.

- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

- The I$^2$C-bus may be used for test and diagnostic purposes.

## 6.16 SPI serial I/O controller

The LPC2292/LPC2294 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

### 6.16.1 Features

- Compliant with SPI specification.

- Synchronous, serial, full duplex, communication.

- Combined SPI master and slave.

- Maximum data bit rate of one eighth of the input clock rate.

## 6.17 General purpose timers

The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

### 6.17.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.

- Four 32-bit match registers that allow:
  – Continuous operation with optional interrupt generation on match.
  – Stop timer on match with optional interrupt generation.
  – Reset timer on match with optional interrupt generation.

- Four external outputs per timer corresponding to match registers, with the following capabilities:
  – Set LOW on match.
  – Set HIGH on match.
  – Toggle on match.

– Do nothing on match.

## 6.18 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

### 6.18.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from $(t_{pclk} \times 256 \times 4)$ to $(t_{pclk} \times 2^{32} \times 4)$ in multiples of $t_{pclk} \times 4$.

## 6.19 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

### 6.19.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable Reference Clock Divider allows adjustment of the RTC to match various crystal frequencies.

## 6.20 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2292/LPC2294. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

### 6.20.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.

- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.

- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.

- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.

- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.

- May be used as a standard timer if the PWM mode is not enabled.

- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

## 6.21 System control

### 6.21.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 30 MHz. The oscillator output frequency is called $f_{osc}$ and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. $f_{osc}$ and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.21.2 "PLL" for additional information.

### 6.21.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

### 6.21.3 Reset and wake-up timer

Reset has two sources on the LPC2292/LPC2294: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD}$ ramp (in the case of power-on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

### 6.21.4 External interrupt inputs

The LPC2292/LPC2294 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

### 6.21.5 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

### 6.21.6 Power control

The LPC2292/LPC2294 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

### 6.21.7 VPB bus

The VPB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The VPB divider serves two purposes. The first is to provide peripherals with the desired PCLK via VPB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the VPB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the VPB bus must work properly at power-up (and its timing cannot be altered if it does not work since the VPB divider control registers reside on the VPB bus), the default condition at reset is for the VPB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the VPB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the VPB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

## 6.22 Emulation and debugging

The LPC2292/LPC2294 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

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### 6.22.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the remote debug protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

### 6.22.2 Embedded trace

Since the LPC2292/LPC2294 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

### 6.22.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2292/LPC2294 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

# 7. Limiting values

**Table 10:    Limiting values**
*In accordance with the Absolute Maximum Rating System (IEC 60134). [1]*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD(1V8)}$ | supply voltage (1.8 V) [2] | | | −0.5 | +2.5 | V |
| $V_{DD(3V3)}$ | supply voltage (3.3 V) [3] | | | −0.5 | +3.6 | V |
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | | | −0.5 | 4.6 | V |
| $V_{ia}$ | analog input voltage | | | −0.5 | 5.1 | V |
| $V_I$ | input voltage | 5 V tolerant I/O pins | [4] [5] | −0.5 | 6.0 | V |
| | | other I/O pins | [4] | −0.5 | $V_{DD(3V3)}$ + 0.5 [6] | V |
| $I_{DD}$ | DC supply current [7] | | | - | 100 [8] | mA |
| $I_{SS}$ | DC ground current [9] | | | - | 100 [8] | mA |
| $T_{stg}$ | storage temperature [10] | | | −65 | 150 | °C |
| $P_{tot(pack)}$ | package total power dissipation | based on package heat transfer, not device power consumption | | - | 1.5 | W |

[1]    The following applies to Table 10:

    a)  This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

    b)  Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to $V_{SS}$ unless otherwise noted.

[2]    Internal rail.

[3]    External rail.

[4]    Including voltage on outputs in 3-state mode.

[5]    Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6]    Not to exceed 4.6 V.

[7]    Per supply pin.

[8]    The peak current is limited to 25 times the corresponding maximum current.

[9]    Per ground pin.

[10]  Dependent on package type.

# 8. Static characteristics

**Table 11:    Static characteristics**

$T_{amb} = -40$ °C to +125 °C for commercial, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD(1V8)}$ | supply voltage (1.8 V) [2] | | 1.65 | 1.8 | 1.95 | V |
| $V_{DD(3V3)}$ | supply voltage (3.3 V) [3] | | 3.0 | 3.3 | 3.6 | V |
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | | 2.5 | 3.3 | 3.6 | V |
| **Standard port pins, RESET, RTCK** | | | | | | |
| $I_{IL}$ | LOW-state input current | $V_I = 0$ V; no pull-up | - | - | 3 | µA |
| $I_{IH}$ | HIGH-state input current | $V_I = V_{DD(3V3)}$; no pull-down | - | - | 3 | µA |
| $I_{OZ}$ | OFF-state output current | $V_O = 0$ V, $V_O = V_{DD(3V3)}$; no pull-up/down | - | - | 3 | µA |
| $I_{latch}$ | I/O latch-up current | $-(0.5V_{DD(3V3)}) < V < (1.5V_{DD(3V3)})$ $T_j < 125$ °C | 100 | - | - | mA |
| $V_I$ | input voltage | [4] [5] [6] | 0 | - | 5.5 | V |
| $V_O$ | output voltage | output active | 0 | - | $V_{DD(3V3)}$ | V |
| $V_{IH}$ | HIGH-state input voltage | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-state input voltage | | - | - | 0.8 | V |
| $V_{hys}$ | hysteresis voltage | | - | 0.4 | - | V |
| $V_{OH}$ | HIGH-state output voltage [7] | $I_{OH} = -4$ mA | $V_{DD(3V3)} - 0.4$ | - | - | V |
| $V_{OL}$ | LOW-state output voltage [7] | $I_{OL} = -4$ mA | - | - | 0.4 | V |
| $I_{OH}$ | HIGH-state output current [7] | $V_{OH} = V_{DD(3V3)} - 0.4$ V | −4 | - | - | mA |
| $I_{OL}$ | LOW-state output current [7] | $V_{OL} = 0.4$ V | 4 | - | - | mA |
| $I_{OHS}$ | HIGH-state short-circuit current [9] | $V_{OH} = 0$ V | - | - | −45 | mA |
| $I_{OLS}$ | LOW-state short-circuit current [9] | $V_{OL} = V_{DD(3V3)}$ | - | - | 50 | mA |
| $I_{pd}$ | pull-down current | $V_I = 5$ V [10] | 10 | 50 | 150 | µA |
| $I_{pu}$ | pull-up current [11] | $V_I = 0$ V | −15 | −50 | −85 | µA |
| | | $V_{DD(3V3)} < V_I < 5$ V [10] | 0 | 0 | 0 | µA |
| $I_{DD(act)1V8}$ | Active mode supply current (1.8 V) | $V_{DD(1V8)} = 1.8$ V, CCLK = 60 MHz, $T_{amb} = 25$ °C, code `while(1){}` executed from flash, no active peripherals | - | 50 | - | mA |

**Table 11:** Static characteristics *…continued*

$T_{amb} = -40\ °C\ to\ +125\ °C$ for commercial, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD(pd)}$ | Power-down mode supply current | $V_{DD(1V8)}$ = 1.8 V, $T_{amb}$ = +25 °C, | - | 10 | - | µA |
| | | $V_{DD(1V8)}$ = 1.8 V, $T_{amb}$ = +85 °C | - | 110 | 500 | µA |
| | | $V_{DD(1V8)}$ = 1.8 V, $T_{amb}$ = +125 °C | - | 300 | 1000 | µA |
| **I²C-bus pins** | | | | | | |
| $V_{IH}$ | HIGH-state input voltage | | $0.7V_{DD(3V3)}$ | - | - | V |
| $V_{IL}$ | LOW-state input voltage | | - | - | $0.3V_{DD(3V3)}$ | V |
| $V_{hys}$ | hysteresis voltage | | - | $0.5V_{DD(3V3)}$ | - | V |
| $V_{OL}$ | LOW-state output voltage | $I_{OLS}$ = 3 mA [7] | - | - | 0.4 | V |
| $I_{LI}$ | input leakage current [8] | $V_I = V_{DD(3V3)}$ | - | 2 | 4 | µA |
| | | $V_I$ = 5 V | - | 10 | 22 | µA |
| **Oscillator pins** | | | | | | |
| $V_{i(XTAL1)}$ | input voltage on pin XTAL1 | | 0 | - | 1.8 | V |
| $V_{o(XTAL2)}$ | output voltage on pin XTAL2 | | 0 | - | 1.8 | V |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] To $V_{SS}$.

[9] Only allowed for a short time period.

[10] Minimum condition for $V_I$ = 4.5 V, maximum condition for $V_I$ = 5.5 V.

[11] Applies to P1[25:16].

**Table 12:  ADC static characteristics**

$V_{DDA}$ = 2.5 V to 3.6 V; $T_{amb}$ = −40 ℃ to +125 ℃ unless otherwise specified. ADC frequency 4.5 MHz.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ia}$ | analog input voltage | | 0 | - | $V_{DDA}$ | V |
| $C_{ia}$ | analog input capacitance | | - | - | 1 | pF |
| $E_D$ | differential linearity error | [1] [2] [3] | - | - | ±1 | LSB |
| $E_{L(adj)}$ | integral non-linearity | [1] [4] | - | - | ±2 | LSB |
| $E_O$ | offset error | [1] [5] | - | - | ±3 | LSB |
| $E_G$ | gain error | [1] [6] | - | - | ±0.5 | % |
| $E_T$ | absolute error | [1] [7] | - | - | ±4 | LSB |

[1]  Conditions: $V_{SSA}$ = 0 V, $V_{DDA}$ = 3.3 V.

[2]  The ADC is monotonic, there are no missing codes.

[3]  The differential linearity error ($E_D$) is the difference between the actual step width and the ideal step width. See Figure 5.

[4]  The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5]  The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6]  The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7]  The absolute voltage error ($E_T$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.
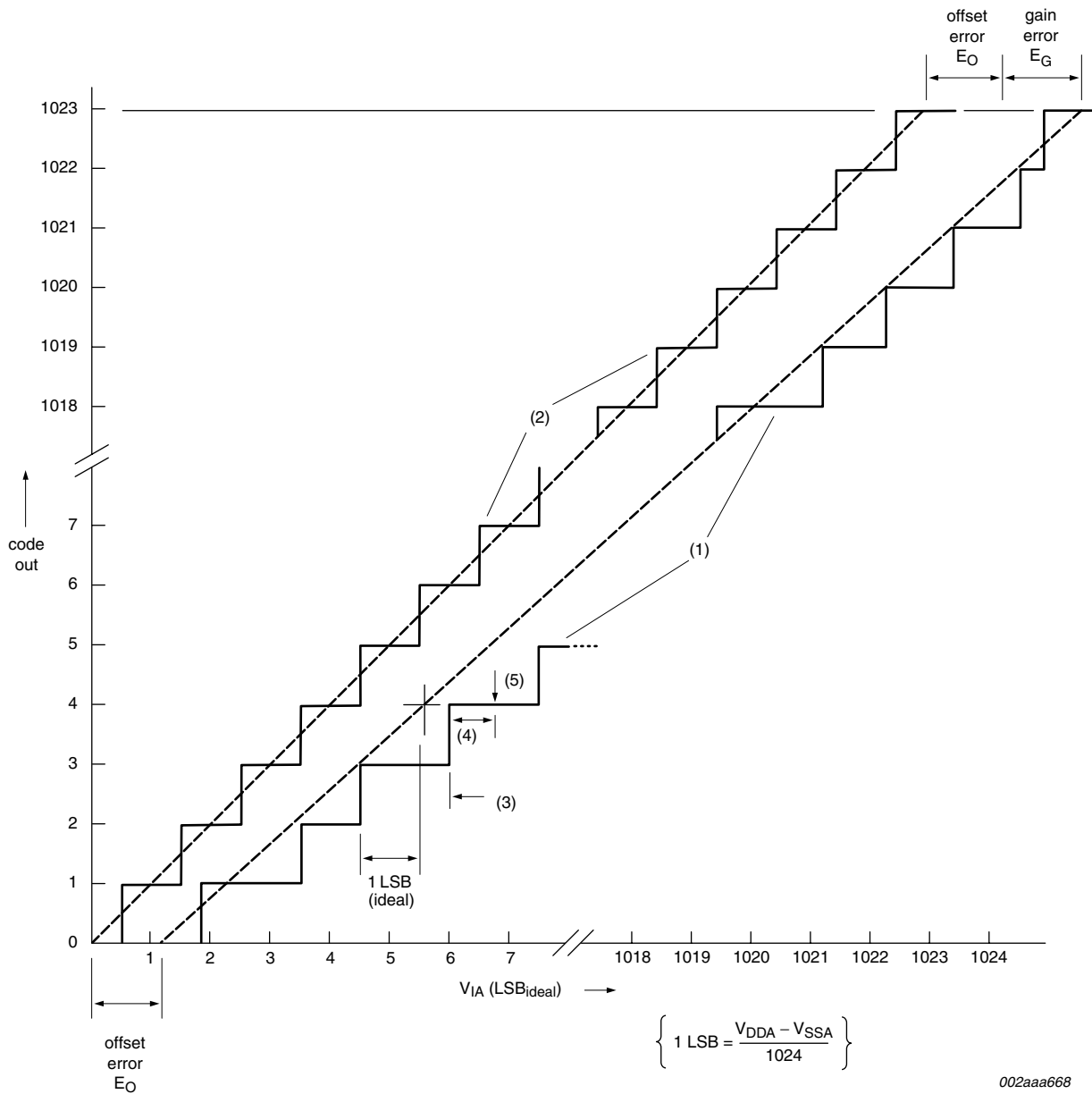
(1)  Example of an actual transfer curve.

(2)  The ideal transfer curve.

(3)  Differential linearity error ($E_D$).

(4)  Integral non-linearity ($E_{L(adj)}$).

(5)  Center of a step of the actual transfer curve.

**Fig 5.   ADC characteristics**

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# 9. Dynamic characteristics

**Table 13: Dynamic characteristics**

$T_{amb} = -40\ °C$ to $+125\ °C$, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges [1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **External clock** | | | | | | |
| $f_{osc}$ | oscillator frequency | supplied by an external oscillator (signal generator) | 1 | - | 50 | MHz |
| | | external clock frequency supplied by an external crystal oscillator | 1 | - | 30 | MHz |
| | | external clock frequency if on-chip PLL is used | 10 | - | 25 | MHz |
| | | external clock frequency if on-chip boot-loader is used for initial code download | 10 | - | 25 | MHz |
| $T_{cy(CLK)}$ | clock cycle time | | 20 | - | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | | $T_{cy(CLK)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | | $T_{cy(CLK)} \times 0.4$ | - | - | ns |
| $t_{CLCH}$ | clock rise time | | - | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | | - | - | 5 | ns |
| **Port pins (except P0.2 and P0.3)** | | | | | | |
| $t_r$ | rise time | | - | 10 | - | ns |
| $t_f$ | fall time | | - | 10 | - | ns |
| **I²C-bus pins (P0.2 and P0.3)** | | | | | | |
| $t_f$ | fall time | $V_{IH}$ to $V_{IL}$ | [2] $20 + 0.1 \times C_b$ | - | - | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance $C_b$ in pF, from 10 pF to 400 pF.

**Table 14: External memory interface dynamic characteristics**

$C_L = 25\ pF$, $T_{amb} = 40\ °C$

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Common to read and write cycles** | | | | | | |
| $t_{CHAV}$ | XCLK HIGH to address valid time | | - | - | 10 | ns |
| $t_{CHCSL}$ | XCLK HIGH to CS LOW time | | - | - | 10 | ns |
| $t_{CHCSH}$ | XCLK HIGH to CS HIGH time | | - | - | 10 | ns |
| $t_{CHANV}$ | XCLK HIGH to address invalid time | | - | - | 10 | ns |
| **Read cycle parameters** | | | | | | |
| $t_{CSLAV}$ | CS LOW to address valid time | [1] | −5 | - | 10 | ns |
| $t_{OELAV}$ | OE LOW to address valid time | [1] | −5 | - | 10 | ns |
| $t_{CSLOEL}$ | CS LOW to OE LOW time | | −5 | - | 5 | ns |
| $t_{am}$ | memory access time | [2] | $(T_{cy(CCLK)} \times (2 + WST1)) + (−20)$ | - | - | ns |

**Table 14:** **External memory interface dynamic characteristics** ...continued
$C_L = 25\ pF$, $T_{amb} = 40\ °C$

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{am(ibr)}$ | memory access time (initial burst-ROM) | [2] | $(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$ | - | - | ns |
| $t_{am(sbr)}$ | memory access time (subsequent burst-ROM) | [3] | $T_{cy(CCLK)} + (-20)$ | - | - | ns |
| $t_{h(D)}$ | data hold time | [4] | 0 | - | - | ns |
| $t_{CSHOEH}$ | CS HIGH to OE HIGH time | | −5 | - | 5 | ns |
| $t_{OEHANV}$ | OE HIGH to address invalid time | | −5 | - | 5 | ns |
| $t_{CHOEL}$ | XCLK HIGH to OE LOW time | | −5 | - | 5 | ns |
| $t_{CHOEH}$ | XCLK HIGH to OE HIGH time | | −5 | - | 5 | ns |
| **Write cycle parameters** | | | | | | |
| $t_{AVCSL}$ | address valid to CS LOW time | [1] | $T_{cy(CCLK)} - 10$ | - | - | ns |
| $t_{CSLDV}$ | CS LOW to data valid time | | −5 | - | 5 | ns |
| $t_{CSLWEL}$ | CS LOW to WE LOW time | | −5 | - | 5 | ns |
| $t_{CSLBLSL}$ | CS LOW to BLS LOW time | | −5 | - | 5 | ns |
| $t_{WELDV}$ | WE LOW to data valid time | | −5 | - | 5 | ns |
| $t_{CSLDV}$ | CS LOW to data valid time | | −5 | - | 5 | ns |
| $t_{WELWEH}$ | WE LOW to WE HIGH time | [5] | $T_{cy(CCLK)} \times (1 + WST2) - 5$ | - | $T_{cy(CCLK)} \times (1 + WST2) + 5$ | ns |
| $t_{BLSLBLSH}$ | BLS LOW to BLS HIGH time | [5] | $T_{cy(CCLK)} \times (1 + WST2) - 5$ | - | $T_{cy(CCLK)} \times (1 + WST2) + 5$ | ns |
| $t_{WEHANV}$ | WE HIGH to address invalid time | [5] | $T_{cy(CCLK)} - 5$ | - | $T_{cy(CCLK)} + 5$ | ns |
| $t_{WEHDNV}$ | WE HIGH to data invalid time | [5] | $(2 \times T_{cy(CCLK)}) - 5$ | - | $(2 \times T_{cy(CCLK)}) + 5$ | ns |
| $t_{BLSHANV}$ | BLS HIGH to address invalid time | [5] | $T_{cy(CCLK)} - 5$ | - | $T_{cclk} + 5$ | ns |
| $t_{BLSHDNV}$ | BLS HIGH to data invalid time | [5] | $(2 \times T_{cy(CCLK)}) - 5$ | - | $(2 \times T_{cy(CCLK)}) + 5$ | ns |
| $t_{CHDV}$ | XCLK HIGH to data valid time | | - | - | 10 | ns |
| $t_{CHWEL}$ | XCLK HIGH to WE LOW time | | - | - | 10 | ns |
| $t_{CHBLSL}$ | XCLK HIGH to BLS LOW time | | - | - | 10 | ns |
| $t_{CHWEH}$ | XCLK HIGH to WE HIGH time | | - | - | 10 | ns |
| $t_{CHBLSH}$ | XCLK HIGH to BLS HIGH time | | - | - | 10 | ns |
| $t_{CHDNV}$ | XCLK HIGH to data invalid time | | - | - | 10 | ns |

[1]   Except on initial access, in which case the address is set up $T_{cy(CCLK)}$ earlier.

[2]   Latest of address valid, CS LOW, OE LOW to data valid.

[3]   Address valid to data valid.

[4]   Earliest of CS HIGH, OE HIGH, address change to data invalid.

[5]   $T_{cy(CCLK)} = \frac{1}{CCLK}$.

**Table 15:   Standard read access specifications**

| Access cycle | Max frequency | WST setting<br>WST $\geq$ 0; round up to integer | Memory access time requirement |
|---|---|---|---|
| standard read | $f_{MAX} \leq \dfrac{2 + WST1}{t_{RAM} + 20\ ns}$ | $WST1 \geq \dfrac{t_{RAM} + 20\ ns}{t_{CYC}} - 2$ | $t_{RAM} \leq t_{CYC} \times (2 + WST1) - 20\ ns$ |
| standard write | $f_{MAX} \leq \dfrac{1 + WST2}{t_{WRITE} + 5\ ns}$ | $WST2 \geq \dfrac{t_{WRITE} - t_{CYC} + 5}{t_{CYC}}$ | $t_{WRITE} \leq t_{CYC} \times (1 + WST2) - 5\ ns$ |
| burst read - initial | $f_{MAX} \leq \dfrac{2 + WST1}{t_{INIT} + 20\ ns}$ | $WST1 \geq \dfrac{t_{INIT} + 20\ ns}{t_{CYC}} - 2$ | $t_{INIT} \leq t_{CYC} \times (2 + WST1) - 20\ ns$ |
| burst read - subsequent 3× | $f_{MAX} \leq \dfrac{1}{t_{ROM} + 20\ ns}$ | N/A | $t_{ROM} \leq t_{CYC} - 20\ ns$ |

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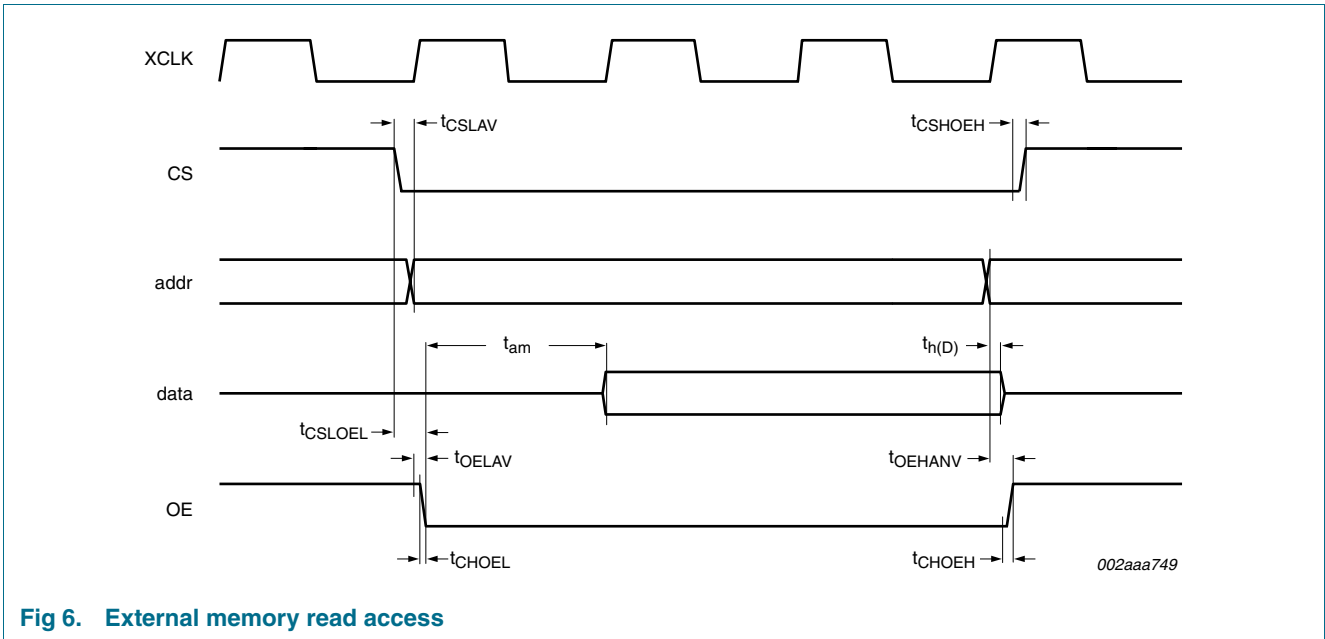
## 9.1 Timing



**Fig 6.  External memory read access**
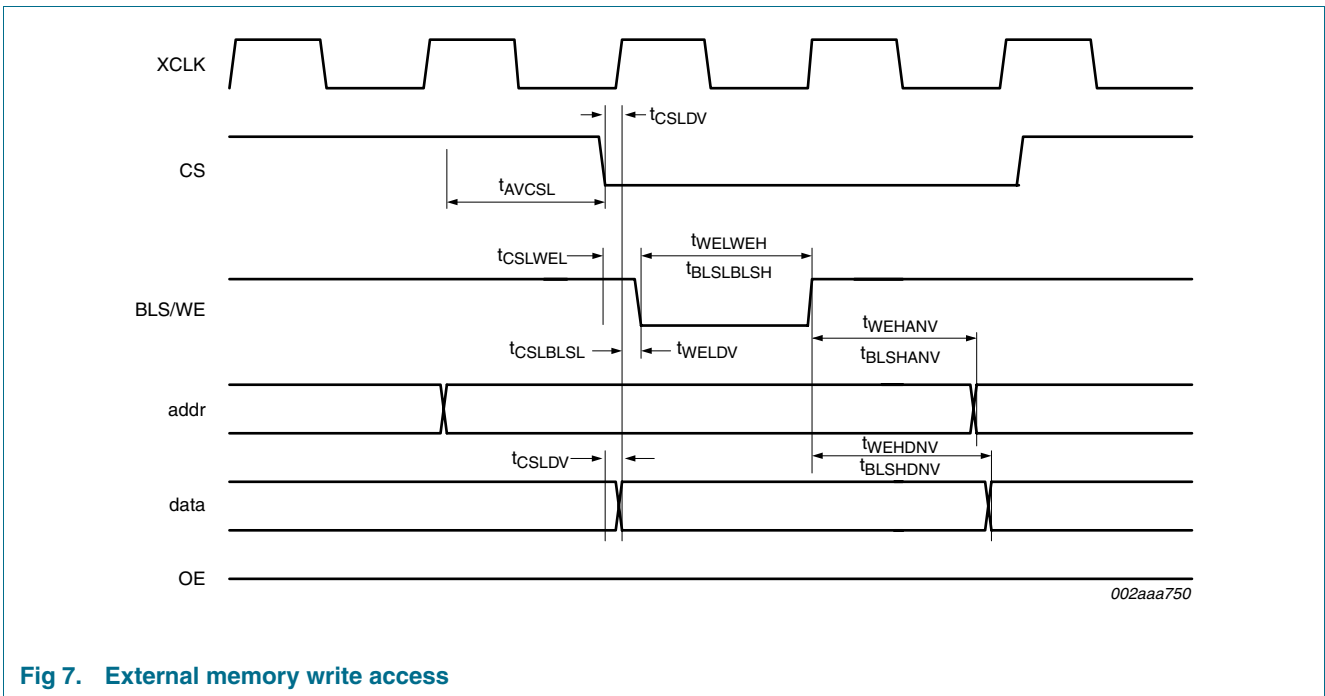


**Fig 7.  External memory write access**
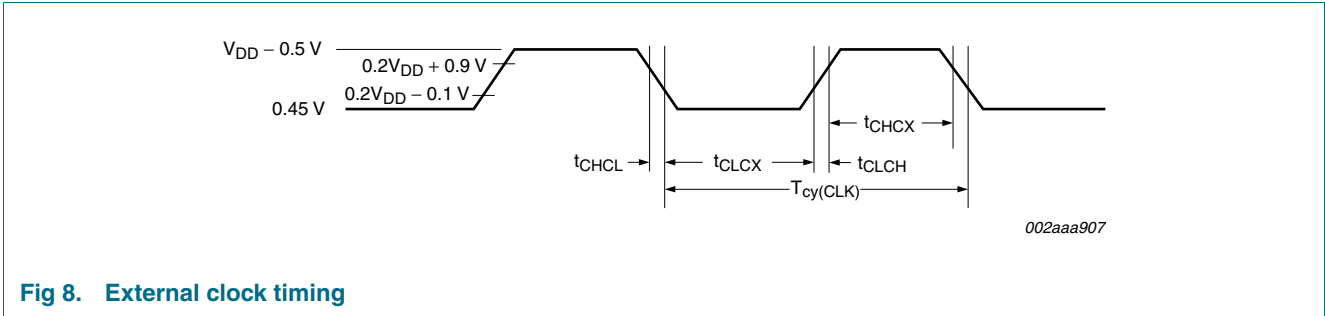
**Fig 8.   External clock timing**

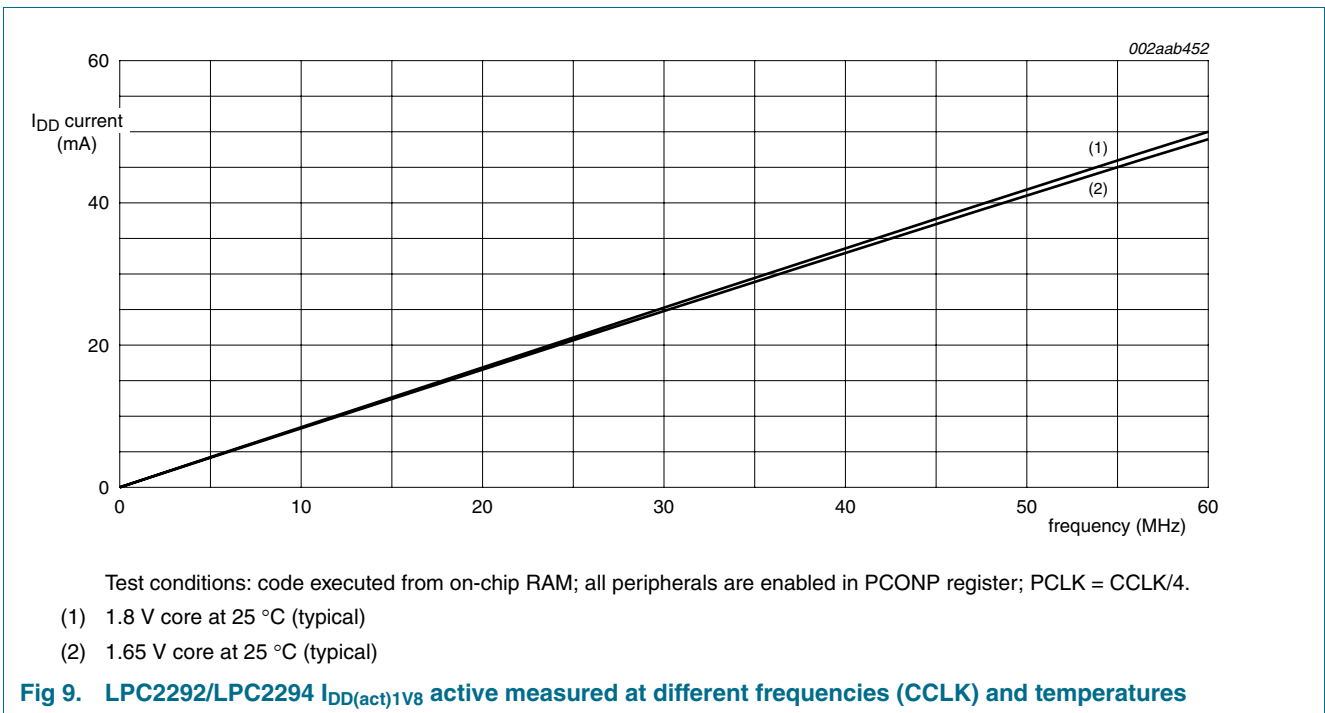## 9.2   LPC2292/LPC2294 power consumption measurements



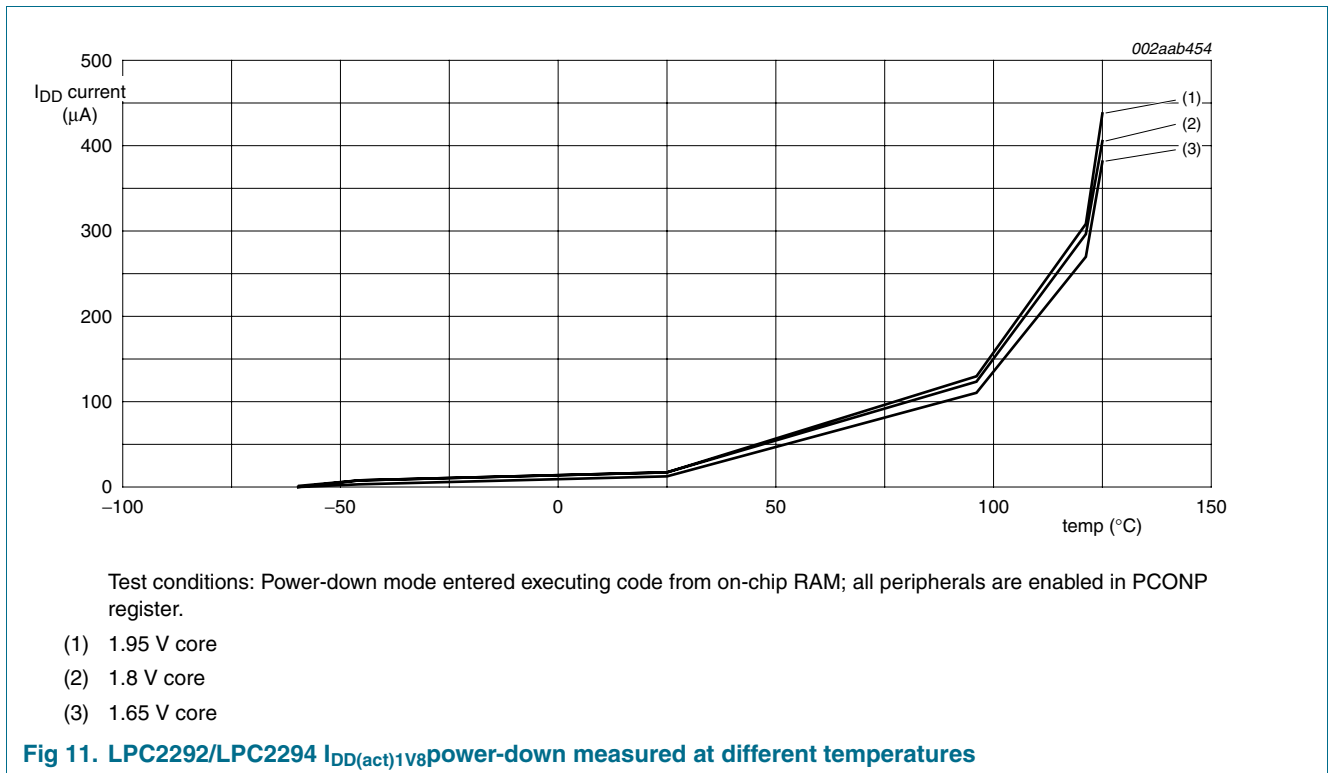Test conditions: code executed from on-chip RAM; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1)   1.8 V core at 25 °C (typical)

(2)   1.65 V core at 25 °C (typical)

**Fig 9.   LPC2292/LPC2294 $I_{DD(act)1V8}$ active measured at different frequencies (CCLK) and temperatures**

*002aab453*

Test conditions: Idle mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register; PCLK = CCLK/4.

(1)   1.8 V core at 25 °C (typical)

(2)   1.65 V core at 25 °C (typical)

**Fig 10.  LPC2292/LPC2294 I$_{DD(act)1V8}$ idle measured at different frequencies (CCLK) and temperatures**



*002aab454*

Test conditions: Power-down mode entered executing code from on-chip RAM; all peripherals are enabled in PCONP register.

(1)   1.95 V core

(2)   1.8 V core

(3)   1.65 V core

**Fig 11.  LPC2292/LPC2294 I$_{DD(act)1V8}$ power-down measured at different temperatures**

# 10. Package outline

**LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm**     **SOT486-1**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | b$_p$ | c | D$^{(1)}$ | E$^{(1)}$ | e | H$_D$ | H$_E$ | L | L$_p$ | v | w | y | Z$_D$$^{(1)}$ | Z$_E$$^{(1)}$ | θ |
|------|--------|-----|-----|-----|-------|-----|-----------|-----------|-----|-------|-------|-----|-------|-----|------|------|----------|----------|-----|
| mm | 1.6 | 0.15 0.05 | 1.45 1.35 | 0.25 | 0.27 0.17 | 0.20 0.09 | 20.1 19.9 | 20.1 19.9 | 0.5 | 22.15 21.85 | 22.15 21.85 | 1 | 0.75 0.45 | 0.2 | 0.08 | 0.08 | 1.4 1.1 | 1.4 1.1 | 7° 0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------|-------|-------|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT486-1 | 136E23 | MS-026 | | | | ~~00-03-14~~ 03-02-20 |

**Fig 12. Package outline SOT486-1 (LQFP144)**

**TFBGA144: plastic thin fine-pitch ball grid array package; 144 balls; body 12 x 12 x 0.8 mm**   **SOT569-1**



ball A1 index area

detail X

ball A1 index area

shape optional (4×)

**N M L K J H G F E D C B A**

**1 2 3 4 5 6 7 8 9 10 11 12 13**

0    5    10 mm

scale

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A$_1$ | A$_2$ | b | D | D$_1$ | E | E$_1$ | e | e$_1$ | e$_2$ | v | w | y | y$_1$ |
|------|--------|-------|-------|-----|------|------|------|------|-----|------|------|------|------|-----|------|
| mm | 1.2 | 0.36 0.24 | 0.84 0.74 | 0.53 0.43 | 12.2 11.8 | 11.9 11.7 | 12.2 11.8 | 11.9 11.7 | 0.8 | 9.6 | 9.6 | 0.15 | 0.08 | 0.1 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|-------|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT569-1 | | MO-216 | | | | ~~03-07-09~~ 05-09-14 |

**Fig 13. Package outline SOT569-1 (TFBGA144)**

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# 11. Abbreviations

**Table 16:    Acronym list**

| Acronym | Description |
|---------|-------------|
| ADC | Analog-to-Digital Converter |
| CAN | Controller Area Network |
| CISC | Complex Instruction Set Computer |
| CPU | Central Processing Unit |
| FIFO | First In, First Out |
| GPIO | General Purpose Input/Output |
| PLL | Phase-Locked Loop |
| PWM | Pulse Width Modulator |
| RAM | Random Access Memory |
| RISC | Reduced Instruction Set Computer |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| SSP | Synchronous Serial Port |
| UART | Universal Asynchronous Receiver/Transmitter |
| VPB | VLSI Peripheral Bus |

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## 12. Revision history

**Table 17: Revision history**

| Document ID | Release date | Data sheet status | Change notice | Doc. number | Supersedes |
|---|---|---|---|---|---|
| LPC2292_2294_3 | **<tbd>** | Product data sheet | - | - | LPC2292_2294-02 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. <br>• Added new device LPC22292FET144. <br>• Updated temperature range throughout data sheet. | | | | |
| LPC2292_2294-02 | 20041223 | Product data | - | 9397 750 13152 | LPC2292_2294-01 |

# 13. Data sheet status

| Level | Data sheet status [1] | Product status [2] [3] | Definition |
|---|---|---|---|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
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[2]   The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3]   For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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# 18. Contents