Oki Semiconductor

advantage™ microcontrollers

ML696201 / ML69Q6203

32-Bit ARM946E™ RISC Based Microcontroller

General Purpose

DESCRIPTION

The Oki ML696201/ML69Q6203 microcontrollers are system LSI suitable for portable USB high-speed storage devices based on the ARM946E™, ARM's proprietary 32-bit RISC CPU core.

The ML696201/ML69Q6203 devices provide a 120-Mhz ARM-9 CPU along with 128-KB of SRAM, a high-speed USB interface with PHY, an Ultra DMA hard-drive controller (ATA), and a Smart Media controller. These devices contain a memory controller that can connect to External FLASH, SRAM, and SDRAM. The ML69Q6203 also contains 512-KB of built-in FLASH ROM.

FEATURES

- ARM946E-S RISC CPU
  - 8-KB instruction Cache
  - 8-KB Data Cache
  - JTAG debug function
- Internal Memory
  - 128-KB SRAM, zero wait state
  - 16-KB Boot-loader ROM
  - 512-KB Flash ROM (ML69Q6203 only)
- USB High Speed controller
  - Contains integrated PHY
  - High Speed (480 Mbps) or Full Speed (12 Mbps)
- IDE (ATA) controller
  - DMA / Ultra DMA support
  - Up to 60-MHz operation
- NAND Flash memory controller
  - Smart Media 2000 Compliant
  - Built in ECC circuit
  - Supports ANAND Flash
  - 8 MB ~ 128 MB support
- 28 Interrupt Sources
  - 23 Internal IRQs
  - 4 External IRQs
  - One FIQ (Fast Interrupt Request)
- DMA Controller – 4-Channel
- A/D Converter – Four, 10-bit Channels
- PWM – 16-bit x 1-Channel
- Four 16-bit auto-reload timers
- 16-bit Watchdog Timer
- Interrupt or Reset control
- I^2S Transceiver
  - 16-bit Data
  - 8/11.025/12/16/22.05/24/32/ 44.1/ 48-kHz sample rates
- RTC Clock Generation
- Serial Interfaces
  - Two SSIO
  - UART/SIO
  - I^2C
- General Purpose I/O – 87 Programmable pins
- External Memory Controller supports:
  - Flash
  - SRAM
  - SDRAM
  - Supports external wait input – XWAIT
- Package – 272-pin LFBGA, 15 mm x 15 mm, 0.65 mm pitch

TYICAL APPLICATIONS

- USB High-Speed Storage Devices

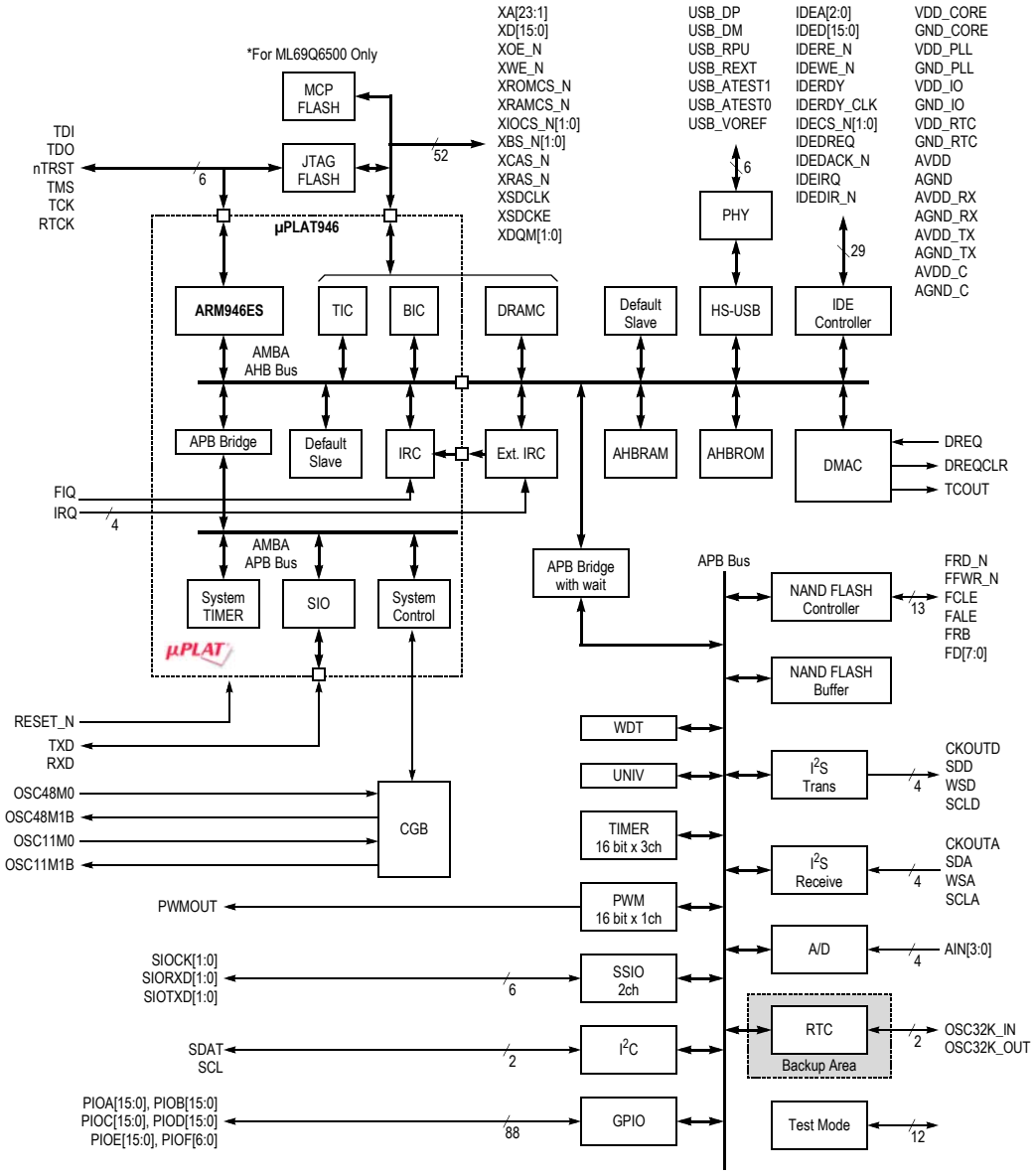
Product Selector

Part Number	Clock Frequency	Built-in Flash ROM	Package
ML696201LA	120 MHz	n/a	272-pin LFBGA 0.65 mm pitch
ML69Q6203LA	120 MHz	512 KB	272-pin LFBGA 0.65 mm pitch

January 2005, Rev 1.1

Data Sheet

Block Diagram



FUNCTIONAL DESCRIPTION

- CPU
  - 32-bit RISC CPU (ARM946E)
  - Built-in 8-KB instruction cache and 8-KB data cache
  - Little-endian format
  - Maximum operating frequency of 120 MHz
  - Instruction structure – Highly dense 32-bit long instructions and their subset 16-bit long instructions with high object code efficiency can be executed by switching between them.
  - 31 General-purpose registers x 32 bits
  - Built-in barrel shifter – The operations of the ALU and barrel shift can be executed by one instruction.
  - Built-in multiplier (32 bits x 16 bits)
  - Built-in debug function (JTAG)
  - Built-in memory protection unit (MPU)
- Cache memory
  - 8-KB Instruction and 8 KB Data cache memory
  - 4-Way set associative, 1 line, 16 bytes
- Internal memory
  - Built-in 128-KB SRAM (32 KWords x 32 bits)
  - AHB bus connection
  - Built-in boot ROM accommodates in-circuit Flash ROM reprogramming and field-updates via the USB port
- Flash
  - ML69Q6203: (256-K x 16-bit) Flash ROM is embedded in the MCP (Multi-chip Package)
  - ML696201: Version without Flash ROM
- μPLAT external memory controller (16-bit devices)
  - ROM (Flash) access function
    Supports 16- bit devices.
    Supports asynchronous type ROMs.
    Supports FLASH memories.
    In models equipped with MCP Flash, the access to Flash is controlled.
  - SRAM access function
    Supports 16- bit devices
    Supports asynchronous type SRAMs
    Allows setting of access timing
  - SDRAM access function – supports distributed CBR
    Supports 16- bit devices
    Supports distributed CBR
    Allows setting of access timing
  - External I/O access function
    two banks of I/O space with two chip select pins for each bank
    Supports 16- bit devices
    Supports external wait input inputs
    Allows setting of access timing for each bank
- μPLAT interrupt controller / extended-interrupt controller
  - FIQ – One source (external source)
  - 27 IRQ sources (23 internal sources and 4 external sources)
  - Eight interrupt priority levels can be set for each interrupt source
  - Release of STANDBY mode – A clock stop cancellation request is generated when the clock is stopped.
- μPLAT system timer
  - 16-bit auto reload timer x 1 channel
  - Cycle is 2.133 μs to 139.5 ms
- μPLAT-SIO (UART)
  - Full-duplex start-stop synchronization method
  - Built-in baud-rate generator
- DMA controller
  - Four channels
  - Fixed mode or round-robin mode priority can be selected
  - The cycle-steal mode or burst-mode bus access privilege can be selected
  - Software requests and external requests are supported as DMA transfer requests
  - A maskable interrupt request is issued to the CPU for each channel after the specified number of DMA transfers is complete or after an error occurs
  - Maximum transfer count is 65,536 (64K)
  - Data transfer sizes are 8, 16, or 32 bits
- High speed USB Port
  - Connectable to High Speed (480 Mbps) or Full Speed (12 Mbps)
  - The internal bus is connected to the AHB bus.
  - Built in PHY
  - Supports six programmable endpoints.
  - Supports 4-KB multi-configurable FIFO memory
  - DMA supported
- IDE Controller
  - Maximum frequency is 60 MHz
  - DMA and Ultra DMA are supported.
  - Switchable to NAND Flash + GPIO using the IDEMODE pin
- PWM
  - PWM x 1 channel (16-bit resolution)
- Watchdog timer
  - 16-bit timer
  - Interval-mode or watchdog-mode can be selected
  - An interrupt or a reset can be generated
  - Cycles can be set to 8.7, 35.0, 140.0 or 559.2 ms
- Analog-to-digital converter
  - 10-bit successive approximation type x 4 channels
  - Sample / hold function
  - Shortest conversion time is 6.7 μs
- I^2C Bus Controller
  - I^2C bus single-channel master-mode compliant controller
  - Communication speed is 100/400 kbps
  - Supports 7-bit and 10-bit addressing
  - Communication voltage is 2.7V to 3.3V
- Timer
  - 16-bit auto reload timer x 3 channels
  - A different clock can be set for each channel.
  - One-shot mode or interval mode can be set for each channel.
  - Cycle can be set from 0.133 μs to 2.237 s
- Synchronous Serial I/O (SSIO)
  - 8-bit clock synchronous serial port x 2 channels
  - Maximum transfer rate: 15 Mbps
  - 1/1, 1/2, 1/4, 1/16, 1/32 or 1/128 of the frequency of CCLK, or timer overflow clock can be selected.
  - LSB first or MSB first selectable
  - Master or slave mode selectable
  - Transmit/receive interrupt, transmit/receive buffer empty interrupt
  - Rollback test function
  - DMA supported

- Universal Registers
  - Four 8-bit general-purpose internal status/setup registers
- NAND Flash memory controller
  - SmartMedia Standard 2000 compliant (512-Bytes/sector)
  - Supporting SmartMedia of 8 MB to 128 MB
  - Supports ANAND devices
  - Built-in ECC circuit
  - 512-Byte/2048-Byte auto write/read function
  - Switchable to the IDE controller using the IDEMODE pin
- RTC
  - 1-second clock generation function from 32.768 kHz
  - Built-in 32-bit 1-second clock counter
  - 32-bit compare interrupt function
- GPIO
  - Built-in GPIO of 16 pin x 5 channels (GPIOA, GPIOB, GPIOC, GPIOD, GPIOE) and 7 pin x 1 channel (GPIOF)
  - Input/output can be set in units of bits
  - GPIOA[15:00], GPIOB[15:00] and GPIOC[15:00] can be set to an external bus by setting the EXTBUS pin
  - GPIOD[15:00] can be used to select a secondary function in units of bits.
  - GPIOE[15:12] can be used as external interrupts.
  - Only GPIOE[15] is 5-V tolerant input
  - GPIOF[6:0] function as IDE data, when the IDE controller mode is set using the IDEMODE pin.
- I^2S transmission/reception
  - Sampling frequencies of 32, 44.1, and 48 kHz, as well as 1/2 and 1/4 of these frequencies are supported
  - System clock is 256 times the sampling rate
  - Channel data length is 16 bits
  - Data buffer is 9,216 bytes (shared by transmission and reception)
  - With or without 1-bit delay, left/right reversible
- Clocks
  - Can connect a 48-MHz crystal oscillator and input an external clock directly.
  - The RTC section can connect a 32.768-kHz crystal oscillator.
  - Can connect an 11.2896-MHz crystal oscillator for audio and input an external clock directly.
- Power Management
  - Power down mode – The power supply can be disabled to all sections, except for the Real-time Clock section.
  - Stop mode – Software disables clock supply to the main section including the processor
  - Halt mode – Partially disables clock supply
  - Clock gear – Software can dynamically change clock to 1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of the clock input frequency
  - Clock control – Software can stop clock supply for each function
- Package
  - 272-pin LFBGA, 0.65 mm ball pitch

Pin Configuration

21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
NC	NC	NC	FIQ_N	NC	NC	PIOD[0]/ SCLD	PIOD[1]/ WSD	PIOD[3]/ CKOUTD	PIOD[6]/ SDA	PIOD[8]/ SSIOTXD [0]	PIOD[11]/ SSIOTXD [1]	PIOD[12]/ SSIORXD [1]	PIOD[14]/ UP_TXD	PWMOUT	TMODE[2]	TMODE[0]	BOOT[1]	GND_ CORE	GND_IO	GND_IO	AA
NC	NC	NC	NC	GND_IO	NC	GND_IO	VDD_ CORE	PIOD[2]/ SDD	PIOD[4]/ SCLA/SCL	VDD_FLA	PIOD[9]/ SSIORXD [0]	PIOD[13] SSIOCK[1]	SCL	TEST_ RSV	TMODE[1]	EXTBUS	BOOT[0]	GND_ CORE	GND_IO	TDO	Y
NC	NC	NC	NC	GND_IO	RESET_N	GND_IO	VDD_ CORE	VDD_ CORE	PIOD[5]/ WSA	PIOD[7]/ CKOUTA/ CLKOUT	PIOD[10]/ SSIOCK[0]	PIOD[15]/ UP_RXD	SDAT	PLL BYPASS	TMODE[3]	IDEMODE	GND_ CORE	GND_IO	FD[0]/ IDED[0]	VSSFLA	W
NC	NC	NC	NC	GND_IO	GND_IO	GND_IO	VDD_ CORE	VDD_IO	VDD_IO	GND_ CORE	GND_ CORE	VDD_IO	VDD_IO	VDD_ CORE	VDD_IO	VDD_IO	GND_IO	nTRST	FD[2]/ IDED[2]	FD[1]/ IDED[1]	V
NC	NC	ADIN[1]	AVDD														GND_IO	RTCK	FD[6]/ IDED[6]	FD[4]/ IDED[4]	U
NC	ADIN[2]	ADIN[3]	GND_ CORE														VDD_IO	TCK	PIOF[0]/ IDED[8]	FD[7]/ IDED[7]	T
ADIN[0]	AGND	VSSFLA	VDD_IO														VDD_IO	TMS	PIOF[3]/ IDED[11]	PIOF[2]/ IDED[10]	R
VDD_PLL	OSC48M0	OSC48M1B	VDD_ CORE														VDD_ CORE	TDI	PIOF[5]/ IDED[13]	PIOF[4]/ IDED[12]	P
USB_ VOREF	USB_ ATEST[0]	VDD_PLL	OSC11M0														VDD_ CORE	FD3/ IDED[3]	IDED[15]	PIOF[6]/ IDED[14]	N
USB_ REXT	AVDDC	GND_PLL	OSC11M1B														GND_ CORE	FD[5]/I DED[5]	OSC32K1B	GND_RTC	M
AVDDRX	AGND_C	USB_ ATEST[1]	GND_PLL														VDD_IO	PIOF[1]/ IDED[9]	RTC_ TESTMODE	OSC32K [0]	L
USB_DP	AGND_TX	DREQCLR	TCOUT														VDD_IO	32K_ TESTMODE	IDE NPCBRID	IDEIRQ	K
USB_DM	AGND_TX	XDQM[0]	DREQ														VDD_IO	VDDRTC	IDEDACK_ N	IDEDREQ	J
AVDDTX	AGND_RX	XSDCKE	XDQM[1]														VDD_IO	FCLE/ IDECS_N [0]	FRB/ IDERDY	FALE/ IDECS_N [1]	H
XCAS_N	XRAS_N	VDD_IO	XSYSCLK														VDD_ CORE	IDERST_N	FRD_N/ IDERE_N	FWR_N/ IDEWR_N	G
PIOC[1]/ XWAIT [1]	XSDCS_N	PIOC[0]/ XWAIT [0]	XSDCLK														VDD_ CORE	IDEA[1]	IDEA[2]	IDEA[0]	F
PIOC[2]/ XBS_N [0]	PIOC[4]/ XIOCS_N [0]	PIOC[3]/ XBS_N [1]	VDD_IO														GND_ CORE	GND_ CORE	PIOE[1]	PIOE[0]	E
GND_IO	GND_IO	VDD_IO	GND_IO	GND_ CORE	GND_ CORE	GND_ CORE	VDD_IO	VDD_IO	VDD_IO	VDD_ CORE	GND_ CORE	VDD_IO	VDD_IO	VDD_ CORE	VDD_ CORE	GND_IO	GND_IO	PIOE[5]	PIOE[3]	PIOE[2]	D
PIOC[9]/ XROMCS_ N	PIOC[10]/ XWE_N	GND_IO	PIOC[6]/ XIOCS_N [10]	PIOC[5]/ XIOCS_N [1]	PIOC[7]/ XIOCS_N [11]	PIOC[8]/ XRAMCS_N	PIOB[5]/ XD[5]	PIOB[9]/ XD[9]	PIOB[13]/ XD[13]	PIOA[3]/ XA[4]	PIOA[7]/ XA[8]	PIOA[10]/ XA[11]	PIOC[12]/ XA[17]	XA[21]	PIOE[15]	PIOE[6]	PIOE[4]	GND_IO	PIOE[8]	PIOE[7]	C
PIOC[11]/ XOE_N	GND_IO	PIOB[0]/ XD[0]	PIOB[2]/ XD[2]	PIOB[7]/ XD[7]	PIOB[10]/ XD[10]	PIOB[12]/ XD[12]	PIOA[0]/ XA[1]	PIOB[15]/ XD[15]	PIOA[1]/ XA[2]	PIOA[5]/ XA[6]	PIOA[9]/ XA[10]	PIOA[12]/ XA[13]	PIOA[15]/ XA[16]	PIOC[14]/ XA[19]	XA[23]	PIOE[12]	PIOE[13]	PIOE[10]	GND_IO	PIOE[9]	B
GND_IO	PIOB[1]/ XD[1]	PIOB[3]/ XD[3]	PIOB[4]/ XD[4]	PIOB[6]/ XD[6]	PIOB[8]/ XD[8]	PIOB[11]/ XD[11]	PIOB[14]/ XD[14]	PIOA[2]/ XA[3]	PIOA[4]/ XA[5]	PIOA[6]/ XA[7]	PIOA[8]/ XA[9]	PIOA[11]/ XA[12]	PIOA[13]/ XA[14]	PIOA[14]/ XA[15]	PIOC[13]/ XA[18]	PIOC[15]/ XA[20]	XA[22]	PIOE[14]	PIOE[11]	GND_IO	A
21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ML696201 / ML69Q6203
272-Pin LFBGA
(TOP VIEW)

NOTES:

1. For pins that have multiple functions, the signals are noted by their primary / secondary functions.
2. NC balls can be connected to VDD_IO or GND.

Pin Assignment Definitions and Functions

Pin Definitions	
Pin Name/Function	**Description**
A/B	A = Primary Function / B = Secondary Function
A/-	A = Primary Function / *No Secondary Function*
-/B	*No Primary Function* / B = Secondary Function
_N	Active-Low Input or Output

List of Pins

BGA Pin	Symbol	BGA Pin	Symbol	BGA Pin	Symbol	BGA Pin	Symbol
A1	GNDIO	**B1**	PIOE09/-	**C1**	PIOE07/-	**D1**	PIOE02/-
A2	PIOE11/-	B2	GNDIO	C2	PIOE08/-	D2	PIOE03/-
A3	PIOE14/-	B3	PIOE10/-	C3	GNDIO	D3	PIOE05/-
A4	-/XA22	B4	PIOE13/-	C4	PIOE04/-	D4	GNDIO
A5	PIOC15/XA20	B5	PIOE12/-	C5	PIOE06/-	D5	GNDIO
A6	PIOC13/XA18	B6	-/XA23	C6	PIOE15/-	D6	VDDCORE
A7	PIOA14/XA15	B7	PIOC14/XA19	C7	-/XA21	D7	VDDCORE
A8	PIOA13/XA14	B8	PIOA15/XA16	C8	PIOC12/XA17	D8	VDDIO
A9	PIOA11/XA12	B9	PIOA12/XA13	C9	PIOA10/XA11	D9	VDDIO
A10	PIOA08/XA09	B10	PIOA09/XA10	C10	PIOA07/XA08	D10	GNDCORE
A11	PIOA06/XA07	B11	PIOA05/XA06	C11	PIOA03/XA04	D11	VDDCORE
A12	PIOA04/XA05	B12	PIOA01/XA02	C12	PIOB13/XD13	D12	VDDIO
A13	PIOA02/XA03	B13	PIOB15/XD15	C13	PIOB09/XD09	D13	VDDIO
A14	PIOB14/XD14	B14	PIOA00/XA01	C14	PIOB05/XD05	D14	VDDIO
A15	PIOB11/XD11	B15	PIOB12/XD12	C15	PIOC08/XRAMCS_N	D15	GNDCORE
A16	PIOB08/XD08	B16	PIOB10/XD10	C16	PIOC07/XIOCS11_N	D16	GNDCORE
A17	PIOB06/XD06	B17	PIOB07/XD07	C17	PIOC05/XIOCS01_N	D17	GNDCORE
A18	PIOB04/XD04	B18	PIOB02/XD02	C18	PIOC06/XIOCS10_N	D18	GNDIO
A19	PIOB03/XD03	B19	PIOB00/XD00	C19	GNDIO	D19	VDDIO
A20	PIOB01/XD01	B20	GNDIO	C20	PIOC10/XWE_N	D20	GNDIO
A21	GNDIO	B21	PIOC11/XOE_N	C21	PIOC09/XROMCS_N	D21	GNDIO

E1	PIOE00/-	**F1**	-/IDEA0	**G1**	FWR_N/IDEWR_N	**H1**	FALE/IDECS1_N
E2	PIOE01/-	F2	-/IDEA2	G2	FRD_N/IDERE_N	H2	FRB/IDERDY
E3	GNDCORE	F3	-/IDEA1	G3	-/IDERST_N	H3	FCLE/IDECS0_N
E4	GNDCORE	F4	VDDCORE	G4	VDDCORE	H4	VDDIO
E18	VDDIO	F18	-/XSDCLK	G18	-/XSYSCLK	H18	-/XDQM1
E19	PIOC03/XBS1_N	F19	PIOC00/XWAIT0	G19	VDDIO	H19	-/XSDCKE
E20	PIOC04/XIOCS00_N	F20	-/XSDCS_N	G20	-/XRAS_N	H20	AGNDRX/-
E21	PIOC02/XBS0_N	F21	PIOC01/XWAIT1	G21	-/XCAS_N	H21	AVDDTX/-

J1	-/IDEDREQ	**K1**	-/IDEIRQ	**L1**	OSC32K0/-	**M1**	GNDRTC/-
J2	-/IDEDACK_N	K2	-/IDENPCBRID	L2	RTC_TESTMODE/-	M2	OSC32K1B/-
J3	VDDRTC/-	K3	32K_TESTMODE/-	L3	PIOF01/IDED09	M3	FD5/IDED05
J4	VDDIO	K4	VDDIO	L4	VDDIO	M4	GNDCORE
J18	-/DREQ	K18	-/TCOUT	L18	GNDPLL/-	M18	OSC11M1B/-
J19	-/XDQM0	K19	-/DREQCLR	L19	USB_ATEST1/-	M19	GNDPLL/-

List of Pins (Cont.)

BGA Pin	Symbol	BGA Pin	Symbol	BGA Pin	Symbol	BGA Pin	Symbol
J20	AGNDTX/-	K20	AGNDTX/-	L20	AGNDC/-	M20	AVDDC/-
J21	USB_DM/-	K21	USB_DP/-	L21	AVDDRX/-	M21	USB_REXT/-

N1	PIOF06/IDED14	**P1**	PIOF04/IDED12	**R1**	PIOF02/IDED10	**T1**	FD7/IDED07
N2	-/IDED15	P2	PIOF05/IDED13	R2	PIOF03/IDED11	T2	PIOF00/IDED08
N3	FD3/IDED03	P3	TDI/-	R3	TMS/-	T3	TCK/-
N4	VDDCORE	P4	VDDCORE	R4	VDDIO	T4	VDDIO
N18	OSC11M0/-	P18	VDDCORE	R18	VDDIO	T18	GNDCORE
N19	VDDPLL/-	P19	OSC48M1B/-	R19	VSSFLA	T19	ADIN3/-
N20	USB_ATEST0/-	P20	OSC48M0/-	R20	AGND/-	T20	ADIN2/-
N21	USB_VOREF/-	P21	VDDPLL/-	R21	ADIN0/-	T21	NC

U1	FD4/IDED04
U2	FD6/IDED06
U3	RTCK/-
U4	GNDIO
U18	AVDD/-
U19	ADIN1/-
U20	NC
U21	NC

V1	FD1/IDED01	**W1**	VSSFLA	**Y1**	TDO/-	**AA1**	GNDIO
V2	FD2/IDED02	W2	FD0/IDED00	Y2	GNDIO	AA2	GNDIO
V3	nTRST/-	W3	GNDIO	Y3	GNDCORE	AA3	GNDCORE
V4	GNDIO	W4	GNDCORE	Y4	BOOT0/-	AA4	BOOT1/-
V5	VDDIO	W5	IDEMODE/-	Y5	EXTBUS/-	AA5	TMODE0/-
V6	VDDIO	W6	TMODE3/-	Y6	TMODE1/-	AA6	TMODE2/-
V7	VDDCORE	W7	PLLBYPASS/-	Y7	TEST_RSV/-	AA7	PWMOUT/-
V8	VDDIO	W8	SDAT/-	Y8	SCL/-	AA8	PIOD14/UP_TXD
V9	VDDIO	W9	PIOD15/UP_RXD	Y9	PIOD13/SSIOCK1	AA9	PIOD12/SSIORXD1
V10	GNDCORE	W10	PIOD10/SSIOCK0	Y10	PIOD09/SSIORXD0	AA10	PIOD11/SSIOTXD1
V11	GNDCORE	W11	PIOD07/CKOUTA/ CLKOUT	Y11	VDDFLA	AA11	PIOD08/SSIOTXD0
V12	VDDIO	W12	PIOD05/WSA	Y12	PIOD04/SCLA/SCL	AA12	PIOD06/SDA
V13	VDDIO	W13	VDDCORE	Y13	PIOD02/SDD	AA13	PIOD03/CKOUTD
V14	VDDCORE	W14	VDDCORE	Y14	VDDCORE	AA14	PIOD01/WSD
V15	GNDIO	W15	GNDIO	Y15	GNDIO	AA15	PIOD00/SCLD
V16	GNDIO	W16	RESET_N/-	Y16	NC	AA16	NC
V17	GNDIO	W17	GNDIO	Y17	GNDIO	AA17	NC
V18	NC	W18	NC	Y18	NC	AA18	FIQ_N
V19	NC	W19	NC	Y19	NC	AA19	NC
V20	NC	W20	NC	Y20	NC	AA20	NC
V21	NC	W21	NC	Y21	NC	AA21	NC

Pin Description

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th><th>Primary/
Secondary</th></tr>
<tr><td colspan="4">System</td></tr>
<tr><td>OSC32K0</td><td>I</td><td>32-kHz oscillation input</td><td>—</td></tr>
<tr><td>OSC32K1B</td><td>O</td><td>32-kHz oscillation output</td><td>—</td></tr>
<tr><td>OSC48M0</td><td>I</td><td>48-MHz oscillation input</td><td>—</td></tr>
<tr><td>OSC48M1B</td><td>O</td><td>48-MHz oscillation output</td><td>—</td></tr>
<tr><td>OSC11M0</td><td>I</td><td>11-MHz oscillation input</td><td>—</td></tr>
<tr><td>OSC11M1B</td><td>O</td><td>11-MHz oscillation output</td><td>—</td></tr>
<tr><td>RESET_N</td><td>I</td><td>System Reset (Active-Low)</td><td>—</td></tr>
<tr><td colspan="4">Mode</td></tr>
<tr><td>BOOT[1:0]</td><td>I</td><td>Controls boot devices
<table>
<tr><th>BOOT[1]</th><th>BOOT[0]</th><th>Boot device</th></tr>
<tr><td>0</td><td>0</td><td>MCP Flash</td></tr>
<tr><td>0</td><td>1</td><td>External Flash</td></tr>
<tr><td>1</td><td>0</td><td>AHBROM</td></tr>
<tr><td>1</td><td>1</td><td>AHBROM</td></tr>
</table></td><td>—</td></tr>
<tr><td>EXTBUS</td><td>I</td><td>Switches between external bus pin and GPIO.
<table>
<tr><th>EXTBUS</th><th>GPIO/External bus</th></tr>
<tr><td>0</td><td>GPIO0</td></tr>
<tr><td>1</td><td>External Bus</td></tr>
</table></td><td>—</td></tr>
<tr><td>IDEMODE</td><td>I</td><td>Switches between IDE and NAND Flash pin
<table>
<tr><th>IDEMODE</th><th>NAND Flash/IDE controller</th></tr>
<tr><td>0</td><td>NAND Flash</td></tr>
<tr><td>1</td><td>IDE controller</td></tr>
</table></td><td>—</td></tr>
<tr><td>PLLBYPASS</td><td>I</td><td>Sets PLL bypass mode
<table>
<tr><th>PLLBYPASS</th><th>PLL Mode</th></tr>
<tr><td>0</td><td>Use PLL</td></tr>
<tr><td>1</td><td>Bypass PLL – connect to GND</td></tr>
</table></td><td>—</td></tr>
<tr><td>TEST_BS</td><td></td><td>Sets Boundary Scan mode – The TEST_BS pin can be set to active only when boundary scan is used.
<table>
<tr><th>TEST_BS</th><th>Boundary SCAN mode</th></tr>
<tr><td>0</td><td>Normal Mode</td></tr>
<tr><td>1</td><td>Boundary SCAN mode</td></tr>
</table></td><td>—</td></tr>
<tr><td>TMODE [3:0]</td><td>I</td><td>These pins are used to switch test modes such as SCAN, TIC, JTAG-Flash, AUDIO A/D and D/A, and PLL.
Always set TMODE to GND level.</td><td>—</td></tr>
<tr><td>RTC_TESTMODE</td><td>I</td><td>This pin switches the Scan mode pin of the RTC section.</td><td>—</td></tr>
<tr><td>32K_TESTMODE</td><td>I</td><td>This pin switches the test mode pin of a 32-kHz oscillator circuit.</td><td>—</td></tr>
<tr><td colspan="4">Debug Support</td></tr>
<tr><td>TCK</td><td>I</td><td>This pin is used during debugging. Normally connect this pin to GND.</td><td>—</td></tr>
<tr><td>TMS</td><td>I</td><td>This pin is used during debugging. Normally set this input High</td><td>—</td></tr>
</table>

Pin Description (Cont.)

Symbol	I/O	Description	Primary/ Secondary
nTRST	I	This pin is used during debugging. Normally connect this pin to GND. (n = Active Low)	—
TDI	I	This pin is used during debugging. Normally set this input High	—
TDO	O	This pin is used during debugging. Normally, do not connect this pin to any trace	—
RTCK	O	This pin is used during debugging. Normally, do not connect this pin to any trace	—
External Bus Address and Data			
XA [23:1]	O	Address of the bus that connects external RAM, external ROM, external IO and external DRAM	Secondary
XD [15:0]	I/O	Data bus that connects external RAM, external ROM, external IO and external DRAM	Secondary
External Bus Controls Signal			
XOE_N	O	External memory access read enable, Active-Low	Secondary
XWE_N	O	External memory access write enable, Active-Low	Secondary
XROMCS_N	O	External ROM chip select, Active-Low	Secondary
XRAMCS_N	O	External RAM chip select, Active-Low	Secondary
XBS1_N	O	External memory byte select (MSB), Active-Low	Secondary
XBS0_N	O	External memory byte select (LSB), Active-Low	Secondary
XIOCS11_N	O	I/O bank 1, chip select 1, Active-Low	Secondary
XIOCS10_N	O	I/O bank 1, chip select 0, Active-Low	Secondary
XIOCS01_N	O	I/O bank 0, chip select 1, Active-Low	Secondary
XIOCS00_N	O	I/O bank 0, chip select 0, Active-Low	Secondary
XWAIT [1:0]	I	Wait signal for I/O bank 0/1. A device slower than the register set value can be connected by inputting this signal (wait when 1).	Secondary
XSYSCLK	O	AHB clock for external bus	Secondary
External Bus Control Signals (DRAM)			
XSDCS_N	O	SDRAM chip select, Active-Low	Secondary
XCAS_N	O	Column address strobe (SDRAM), Active-Low	Secondary
XRAS_N	O	Row address strobe (SDRAM), Active-Low	Secondary
XSDCLK	O	Clock for SDRAM	Secondary
XSDCKE	O	Clock enable (SDRAM)	Secondary
XDQM1	O	Input/output mask (MSB)	Secondary
XDQM0	O	Input/output mask (LSB)	Secondary
DMA Control			
DREQ	I	DMA request signal. This signal is used if the DREQ type is set by the DMA controller.	Secondary
DREQCLR	O	DREQ signal clear request. The DMA device turns off the DREQ signal when this signal is output.	Secondary
TCOUT	O	This signal notifies the DAM device that the last transfer has been started.	Secondary
General-purpose I/O Port			
PIOA[15:0]	I/O	This is a general-purpose port. – Because this port has a secondary function, it cannot be used as a port if its secondary function is used.	Primary
PIOB[15:0]	I/O	This is a general-purpose port. – Because this port has a secondary function, it cannot be used as a port if its secondary function is used.	Primary
PIOC[15:0]	I/O	This is a general-purpose port.. – Because this port has a secondary function, it cannot be used as a port if its secondary function is used.	Primary

Pin Description (Cont.)

Symbol	I/O	Description	Primary/ Secondary
PIOD [15:0]	I/O	This is a general-purpose port.. – Because this port has a secondary function, it cannot be used as a port if its secondary function is used.	Primary
PIOE[15:0]	I/O	This is a general-purpose port. PIOE[15] is 5-V tolerant. PIOE[15:12] can be used as IRQ (interrupt requests)	Primary
PIOF[6:0]	I/O	This is a general-purpose port.. – Because this port has a secondary function, it cannot be used as a port if its secondary function is used.	Primary
μPLAT-SIO/UART			
UP_RXD	I	μPLAT SIO (UART) receive data	Secondary
UP_TXD	O	μPLAT SIO (UART) transmit data	Secondary
IDE			
IDEA [2:0]	O	IDE controller address	Secondary
IDED [15:0]	I/O	IDE controller data	Secondary
IDERE_N	O	IDE controller read enable, Active-Low	Secondary
IDEWR_N	O	IDE controller write enable, Active-Low	Secondary
IDERDY	I	This allows the IDE controller's I/O cycle extension.	Secondary
IDERST_N	O	Reset signal, Active-Low	Secondary
IDECS1_N	O	IDE controller status/control select signal, Active-Low	Secondary
IDECS0_N	O	IDE controller data/command select signal, Active-Low	Secondary
IDEDREQ	I	IDE controller DMA request	Secondary
IDEDACK_N	O	IDE controller, DMA acknowledge, Active-Low	Secondary
IDEIRQ	I	IDE controller interrupt input	Secondary
IDENPCBRID	I	This detects the IDE primary cable ID.	Secondary
Flash			
FD[7:0]	I/O	NAND Flash data	Primary
FRD_N	O	NAND Flash read enable, Active-Low	Primary
FWR_N	O	NAND Flash write enable, Active-Low	Primary
FRB	I	NAND Flash ready/busy (1 = ready, 0 = busy)	Primary
FALE	O	NAND Flash address latch enable	Primary
FCLE	O	NAND Flash command latch enable	Primary
USB			
USB_DP	I/O	USB DP input/output	Primary
USB_DM	I/O	USB DM input/output	Primary
USB_REXT	I	USB REXT pin	Primary
USB_VOREF	O	VoRef pin for USB TEST	Primary
USB_ATEST [1:0]	O	USB ANALOG TEST pin 1-0	Primary
I^2S Reception			
ICLKOUTA/CLKOUT	O	I^2S receive system clock	Secondary
SDA	I	I^2S receive data	Secondary
WSA	I/O	I^2S receive channel select	Secondary
SCLA/SCL	I/O	I^2S receive transfer clock	Secondary
I^2S Transmission			

Pin Description (Cont.)

Symbol	I/O	Description	Primary/ Secondary
CKOUTD	O	I^2S transmit system clock	Secondary
SDD	O	I^2S transmit data	Secondary
WSD	I/O	I^2S transmit channel select	Secondary
SCLD	I/O	I^2S transmit transfer clock	Secondary
I^2C			
SDAT	I/O	I^2C transmit/receive data	Primary
SCL	O	I^2C clock output	Primary
SSIO			
SSIOCK [1:0]	I/O	SSIO clock pins 0 and 1	Secondary
SSIORXD [1:0]	I	SSIO receive data input 1	Secondary
SSIOTXD [1:0]	O	SSIO transmit data output 1	Secondary
PWM			
PWMOUT	O	PWM output	Primary
A/D Converter			
ADIN [3:0]	I	ADC input (CH3/2/1/0)	Primary
Interrupt			
FIQ_N	O	Fast interrupt request	Primary
Power Supply			
VDD_CORE		Core logic power supply pin 1	—
GND_CORE		Core logic GND pin 1	—
VDD_PLL		PLL power supply pin 1(core level)	—
GND_PLL		PLL GND pin 1	—
VDD_IO		IO power supply pin 1	—
GND_IO		IO GND pin 1	—
AVDD		Power supply for 10-bit A/D C (IO level)	—
AGND		GND for 10-bit A/D C	—
VDD_RTC		Power supply for RTC (core level)	—
GND_RTC		GND for RTC	—
AVDD_RX		Power supply for USB (IO level)	—
AGND_RX		GND for USB	—
AVDD_TX		Power supply for USB (IO level)	—
AGND_TX		GND for USB	—
AVDD_C		Power supply for USB (IO level)	—
AGND_C		GND for USB	—
VDD_FLA		Power supply for FLASH (IO level)	—
GND_FLA		GND for FLASH	—

Electrical Characteristics

Absolute Maximum Ratings

(Exceeding these maximum ratings could cause damage or lead to permanent deterioration of the device)

Item	Symbol	Conditions	Rating	Unit
Digital power supply voltage (core) [1]	V_{DD_CORE}	All GND = 0V T_A = 25°C	-0.3 to +2.0	V
Digital power supply voltage (I/O) [2]	V_{DD_IO}		-0.3 to +4.6	
PLL power supply voltage [3]	V_{DD_PLL}		-0.3 to +2.0	
RTC power supply voltage [4]	V_{DD_RTC}		-0.3 to +2.0	
USB power supply voltage [5]	V_{DD_USB}		-0.3 to +4.6	
Analog power supply voltage [6]	AV_{DD}		-0.3 to +4.6	
Input Voltage	V_I		-0.3 to V_{DD_IO}+0.3	
Output Voltage	V_0		-0.3 to V_{DD_IO}+0.3	
Analog input voltage	V_{AI}		-0.3 to AV_{DD}	
Power dissipation	P_D	T_A = 70°C	*tbd*	mW
Storage temperature	T_{STG}	–	-50 to +150	°C

1. V_{DD_CORE}, V_{DD_PLL}
2. V_{DD_IO}
3. V_{DD_AC}, V_{DD_ADC}, V_{DD_HP}, V_{DD_CODEC}
4. V_{DD_RTC}
5. AV_{DD_RX}, AV_{DD_TX}, AV_{DD_C}
6. AV_{DD}

Recommended Operating Conditions (GND = 0 V

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
Digital power supply voltage (core)	V_{DD_CORE}	$V_{DD\_IO} \geq V_{DD\_CORE}$	1.35	1.5	1.65	V
Digital power supply voltage (I/O)	V_{DD_IO}		2.7	3.3	3.6	
PLL power supply voltage	V_{DD_PLL}		1.35	1.5	1.65	
RTC power supply voltage	V_{DD_RTC}		1.35	1.5	1.65	
USB power supply voltage	V_{DD_USB}		3.0	3.3	3.6	
Analog power supply voltage	AV_{DD}	$AV_{DD} = V_{DD\_IO}$	2.7	3.3	3.6	
CPU operating frequency	f_{OSC}		*tbd*	–	120	MHz
OSC11M oscillating frequency	f_{C11}		–	11.2896	–	MHz
OSC32k oscillating frequency	f_{C32}		–	32.768	–	kHz
Temperature of operation	T_A		-30	25	70	°C

DC Characteristics (V_{DD_CORE} = 1.35 to 1.65 V, V_{DD_IO} = 2.7 to 3.6 V, T_A = 0 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage *1	V_{IH1}		2.2	—	V_{DD_IO}+0.3	V
"L" input voltage *1	V_{IL1}		–0.3	—	0.6	
"H" input voltage *2	V_{IH2}		2.2	—	5.5	
"H" input voltage *3	V_{IH3}		0.8×V_{DD_RTC}	—	V_{DD_RTC}+0.3	
"L" input voltage *3	V_{IL3}		–0.3	—	0.2×V_{DD_RTC}	
"H" input voltage *4	V_{IH4}		0.8×V_{DD_IO}	—	V_{DD_IO}+0.3	
"L" input voltage *4	V_{IL4}		–0.3	—	0.2×V_{DD_IO}	
"H" output voltage *1	V_{OH1}	I_{OH} = –2 mA/–4 mA/–6 mA *5	2.2	—	—	
"H" output voltage *6	V_{OH2}	V_{DD_IO} = 3.0 to 3.6 V	2.2	—	—	
"L" output voltage *1	V_{OL1}	I_{OL} = –2 mA/–4 mA/–6 mA *5		—	0.4	
"H" output voltage *7	V_{OH3}		0.8×V_{DD_RTC}	—	—	
"L" output voltage *7	V_{OL3}			—	0.2×V_{DD_RTC}	
"H" output voltage *8	V_{OH4}		0.8×V_{DD_IO}	—	—	
"L" output voltage *8	V_{OL4}			—	0.2×V_{DD_IO}	
Input leakage current *9	I_{IL1}	V_I = 0V / V_{DD_IO}	–10	—	10	µA
Input leakage current *10	I_{IL2}	V_I = 0V / 5.5 V	–10	—	10	
Input leakage current *11	I_{IL3}	V_I = 0V	–200	–66	–10	
Input leakage current *11	I_{IL4}	V_I = V_{DD_IO}	–10	—	10	
Input leakage current *12	I_{IL5}	V_I = 0V	–10	—	10	
Input leakage current *12	I_{IL6}	V_I = V_{DD_IO}	10	66	200	
Input leakage current *8	I_{IL7}	V_I = 0V / V_{DD_IO}	–1	—	1	
Input leakage current *7	I_{IL8}	V_O = 0V / V_{DD_IO}	–0. 15	—	0.15	
Supply current (RTC section)	I_{DD_RTC}	V_{DD_RTC} = 2.5V (Only the RTC section is powered on)	—	—	50	µA
Supply current (Core section)	I_{DD_CORE}		—	—	200	mA

Notes

*1 Normal pins (including pulled-up and pulled-down pins)

*2 5-V tolerant pins

*3 OSC32K0, RTC_TESTMODE, and 32K_TESTMODE pins

*4 OSC48M0 and OSC11M0 pins

*5 Dependent on drive currents of pins

*6 IDE related pins

*7 Pins for 32-kHz oscillator

*8 Pins for 48-MHz and 11-MHz oscillators

*9 Normal pins

*10 Normal pins

*11 Pulled-up pins

*12 Pulled-down pins

A/D Converter Characteristics (VDD_CORE = 1.35 to 1.65 V, VDD_IO = 2.7 to 3.6 V, T_A = –30 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bit
Linearity error	E_L	Analog input source impedance Ri ≤TBD kΩ	—	*tbd*	—	LSB
Differential linearity error	E_D		—	*tbd*	—	
Zero-scale error	E_{ZS}		—	*tbd*	—	
Full-scale error	E_{FS}		—	*tbd*	—	
Conversion time	t_{CONV}	—	6.7	—	—	µs
Throughput rate		—	10	—	200	kHz

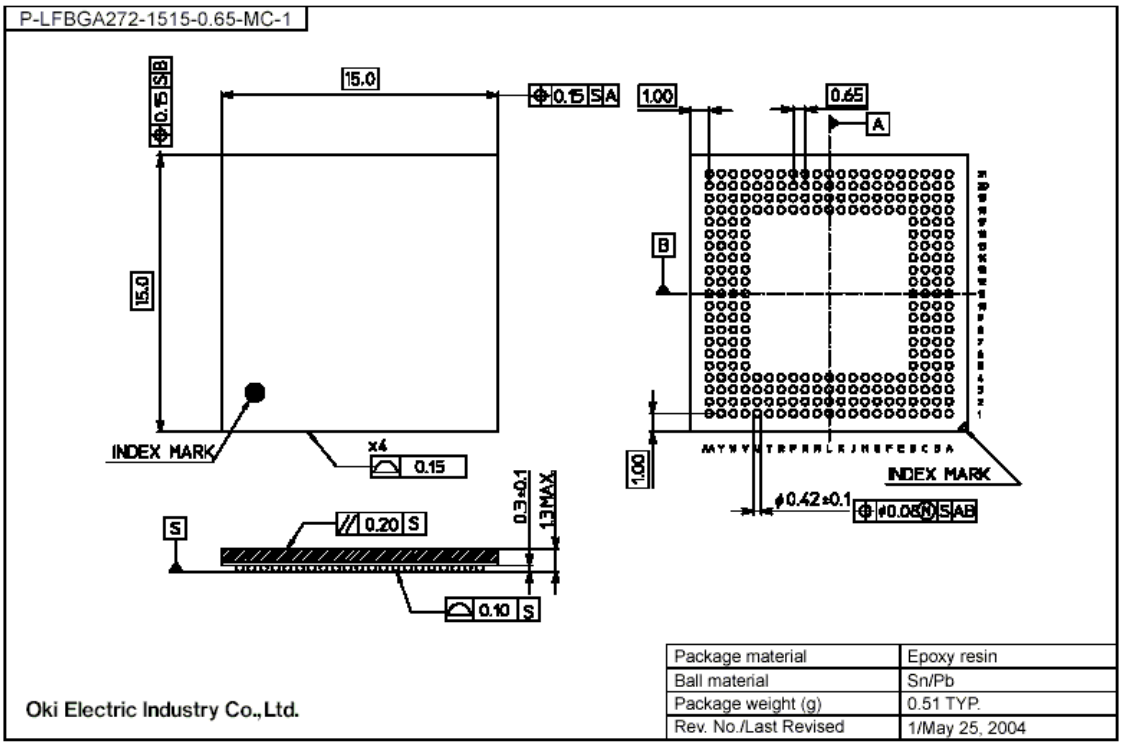
Definition of Terms:

1. Resolution Minimum input analog value that can be discriminated

   In a 10-bit converter, the number of discrete steps is equal to 2^{10} (= 1024), where 10 is the resolution of the converter, so the voltage from V_{REF} to AGND can be divided with 1024.
2. Linearity error is the deviation between the ideal conversion characteristic and the actual conversion characteristic of a 10-bit analog-to-digital converter (not including quantization error).

   The ideal conversion characteristic can be obtained by dividing the voltage from V_{REF} to AGND into 1024 equal steps.
3. Differential linearity error indicates the smoothness of conversion characteristics. The range of the analog input voltage that corresponds to one converted bit of digital output is ideally 1 LSB = (V_{REF} - AGND) /1024. The differential linearity error is the deviation between this ideal bit size and the bit size at an arbitrary point in the conversion range.
4. Zero-scale error is the deviation between the ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from “000h” to “001h”.
5. Full-scale error is the deviation between the ideal conversion characteristics and actual conversion characteristics at the point where the digital output changes from “3FEh” to “3FFh”.

PACKAGE DIMENSIONS



- Notes for Mounting the Surface Mount Type Package

  The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Related Oki Documents for the ML696201 and ML69Q6203

Document	Date

Related ARM Documents for the ML696201 and ML69Q6203

Document
ARM946E™ Technical Reference Manual
ARM Architecture Reference Manual

Revision History

Revision Number	Date	Changes from Previous Revision
Revision 1.0	October, 2004	Preliminary release of the document
Revision 1.1	January, 2005	Feature list modified, FIQ and IREQ signals added to Block Diagram. Part Numbers modified.

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Please make sure before using the product that the information you are referring to is up-to-date.

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January 2005, Rev 1.1

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