8-BIT MICROCONTROLLER

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1 GENERAL DESCRIPTION

The N79E342 series are an 8-bit 4T-8051 microcontroller which has Flash EPROM which is programmable by ICP (In Circuit Program) or by hardware writer. The instruction set of the N79E342 series are fully compatible with the standard 8052. The N79E342 series contain 2K bytes of main Flash EPROM; 128 bytes of RAM; two 16-bit timer/counters; 5 KBI inputs; 4-channel multiplexed 10-bit A/D convert. The N79E342 series supports 128 bytes NVM Data Flash EPROM. These peripherals are supported by 8 sources four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the N79E342 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security. This product series consist of on-chip internal oscillator that runs at 455KHz to provide better power saving.

2 FEATURES

- Fully static design 8-bit 4T-8051 CMOS microcontroller
  - VDD = 3.0V to 5.5V @12MHz
  - VDD = 2.4V to 5.5V @6MHz
- Instruction-set compatible with MSC-51.
- CPU clock source configurable by config bit and software:
  - External oscillator: upto 12MHz.
  - External crystal: 4MHz~12MHz or 32KHz ~1MHz, selectable by Config0 option bit.
  - On-chip oscillator: internal 455KHz RC oscillator, Only N79E342R supports with ±2% accuracy, at fixed voltage and temperature condition.
  - CPU clock source from external or on-chip oscillator is selectable by software.
- 2K bytes of AP Flash EPROM, with ICP and external writer programmable mode.
- 128 bytes of on-chip RAM.
- 128 bytes NVM Data Flash EPROM.
- Up to 14 I/O pins.
- Eight interrupts source with four levels of priority.
- The 4 outputs mode and TTL/Schmitt trigger selectable Port.
- Four-channel multiplexed with 10-bits A/D converter.
- Low Voltage Detect interrupt and reset.
- Two 16-bit timer/counters.
- Programmable Watchdog Timer (clock source supported by internal 20KHz RC oscillator and upto 12MHz external crystal, selectable by option bit).
- Five-keypad interrupt inputs.
- Internal square wave generator for buzzer output.
- LED drive capability on all port pins. Sink 18mA; Drive: -18mA @push-pull mode.
- Packages:

  - Lead Free (RoHS) DIP 16: N79E342AKG
  - Lead Free (RoHS) SOP 16: N79E342ASG
  - Lead Free (RoHS) DIP 16: N79E342RAKG
  - Lead Free (RoHS) SOP 16: N79E342RASG

3 PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

PART NO.	PROGRAM FLASH EPROM	RAM	DATA FLASH EPROM	INTERNAL RC [1] OSCILLATOR ACCURACY	PACKAGE
N79E342AKG	2K	128B	128B	±30%	DIP 16
N79E342ASG	2K	128B	128B	±30%	SOP 16
N79E342RAKG	2K	128B	128B	±2%	DIP 16
N79E342RASG	2K	128B	128B	±2%	SOP 16

Note: 1. Test conditions are V_{DD} = 3.3V, TA = 25°C

Table 3-1: Lead Free (RoHS) Parts information list

4 PIN CONFIGURATION

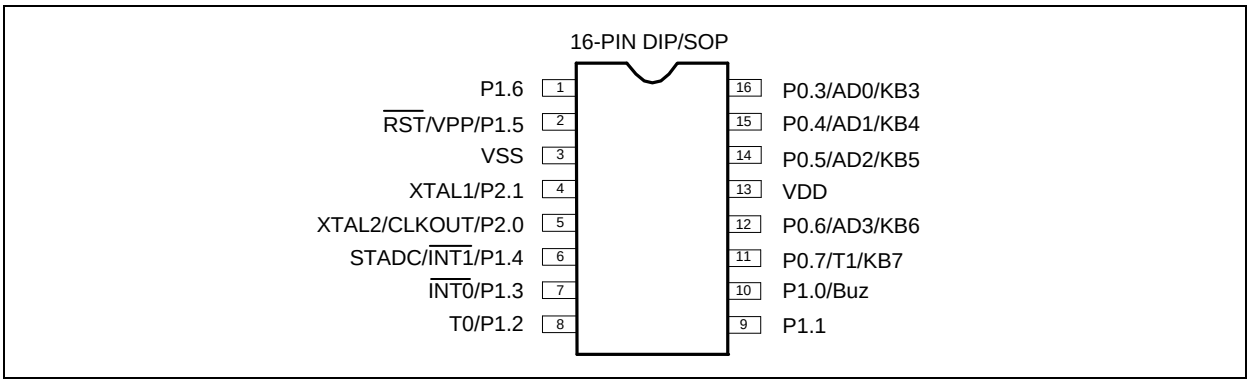


Figure 4-1: Pin Configuration

5 PIN DESCRIPTIONS

Symbol	Alternate Function 1	Alternate Function 2	Alternate Function 3	Alternate Function 4 (ICP mode)	Type	Descriptions
VDD					P	POWER SUPPLY: Supply voltage for operation.
VSS					P	GROUND: Ground potential.
P0.3	AD0	/KB3			I/O	Port0: Support 4 output modes and TTL/Schmitt trigger. Multifunction pins for T1, AD0-3, /KB3-7, Data and Clock (for ICP).
P0.4	AD1	/KB4		Data	I/O	
P0.5	AD2	/KB5		Clock	I/O	
P0.6	AD3	/KB6			I/O	
P0.7		/KB7	T1		I/O	
P1.0	BUZ				I/O	Port1: Support 4 output modes and TTL/Schmitt trigger (except for P1.5 input only). Multifunction pins for /RST, T0, /INT0-1, BUZ, STADC, and VPP (for ICP).
P1.1					I/O	
P1.2			T0		I/O	
P1.3		/INT0			I/O	
P1.4	STADC	/INT1			I/O	
P1.5	$\overline{\text{RST}}$			VPP	I	
P1.6					I/O	
P2.0	XTAL2/CLKOUT				I/O	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin. When operating as i/o, it supports 4 output modes and TTL/Schmitt trigger.
P2.1	XTAL1				I/O	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock or configurable i/o pin. When operating as i/o, it supports 4 output modes and TTL/Schmitt trigger.

* **TYPE:** P: power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open-drain**.**

Table 5-1: Pin Descriptions

Note:

On power-on-reset, all port pins will be tri-stated.

After power-on-reset, all port pins state will follow CONFIG0.PRHI bit definition.

6 FUNCTIONAL DESCRIPTION

The N79E342 series architecture consist of a 4T 8051 core controller surrounded by various registers, 2K bytes Flash EPROM, 128 bytes of RAM, up to 14 general purpose I/O ports, two timer/counters, 5 KBI inputs, 4-channel multiplexed with 10-bit ADC analog input, Flash EPROM program by Writer and ICP. N79E342 series supports 128 bytes NVM Data Flash EPROM.

6.1 On-Chip Flash EPROM

The N79E342 series include one 2K bytes of main Flash EPROM for application program. A Writer or ICP programming board is required to program the Flash EPROM or NVM Data Flash EPROM.

This ICP (In-Circuit Programming) feature makes the job easy and efficient when the application's firmware needs to be updated frequently. In some applications, the in-circuit programming feature makes it possible for the end-user to easily update the system firmware without opening the chassis.

6.2 I/O Ports

The N79E342 series have up to 14 I/O pins using on-chip oscillator & /RST is input only by reset options. All ports can be used as four outputs mode when it may set by PxM1.y and PxM2.y SFR's registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Timers

The N79E342 series have two 16-bit timers that are functionally and similar to the timers of the 8052 family. When used as timers, the user has a choice of 12 or 4 clocks per count that emulates the timing of the original 8052.

6.4 Interrupts

The Interrupt structure in the N79E342 series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.5 Data Pointers

The data pointer of N79E342 series is same as standard 8052 that has 16-bit Data Pointer (DPTR).

6.6 Architecture

The N79E342 series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.6.1 ALU

The ALU is the heart of the N79E342 series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.6.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the N79E342 series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.6.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.6.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.6.5 Scratch-pad RAM

The N79E342 series have a 128 bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.6.6 Stack Pointer

The N79E342 series have an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the N79E342 series. Hence the size of the stack is limited by the size of this RAM.

6.7 Power Management

Power Management like the standard 8052, the N79E342 series also have the IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU is stopped while the timers, serial ports and interrupt block continue to operate. In the POWER DOWN mode, all clocks are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

7 MEMORY ORGANIZATION

The N79E342 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

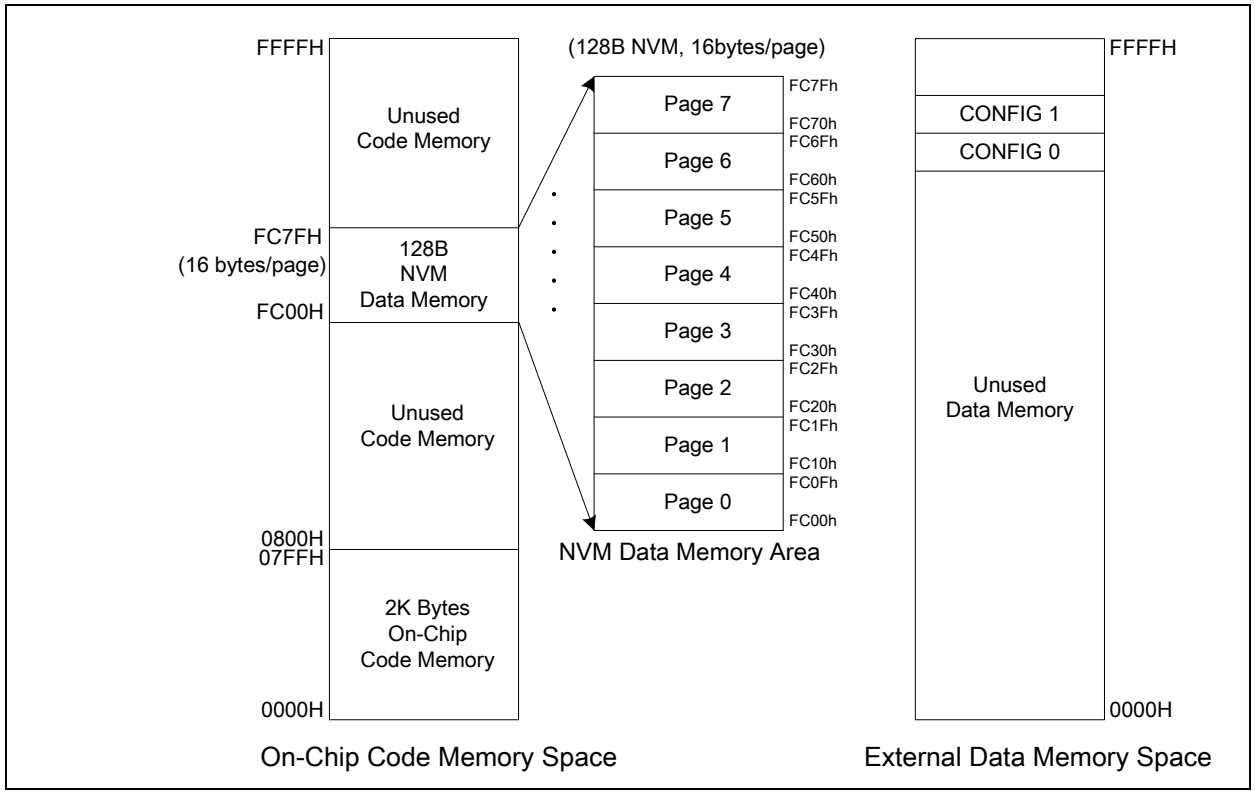


Figure 7-1: Memory map

7.1 Program Memory (on-chip Flash)

The Program Memory on the N79E342 series can be up to 2K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

For N79E342 series, NVM Data Memory of Flash EPROM is fixed at 128 bytes long with page size 16 bytes.

7.3 Data Memory (Accessed by MOVX)

Not available in this product series.

7.4 Scratch-pad RAM and Register Map

As mentioned before the N79E342 series have separate Program and Data Memory areas. The on-chip 128 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

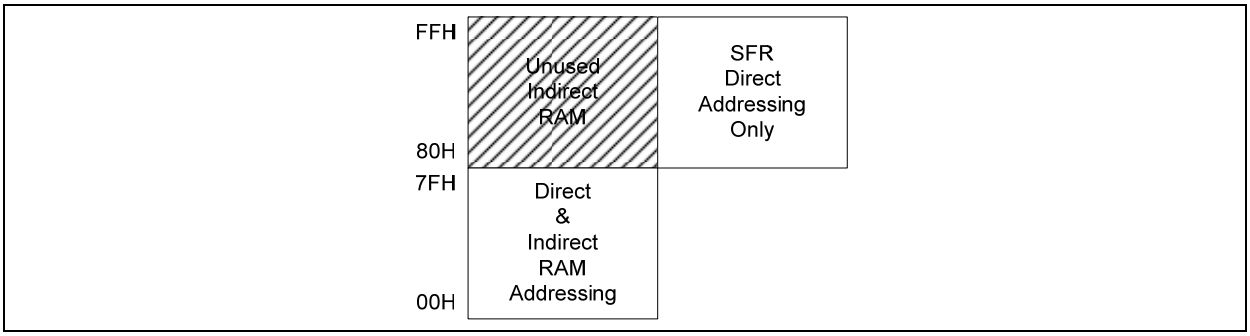


Figure 7-2: RAM and SFR memory map

Since the scratch-pad RAM is only 128 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are described as follows.

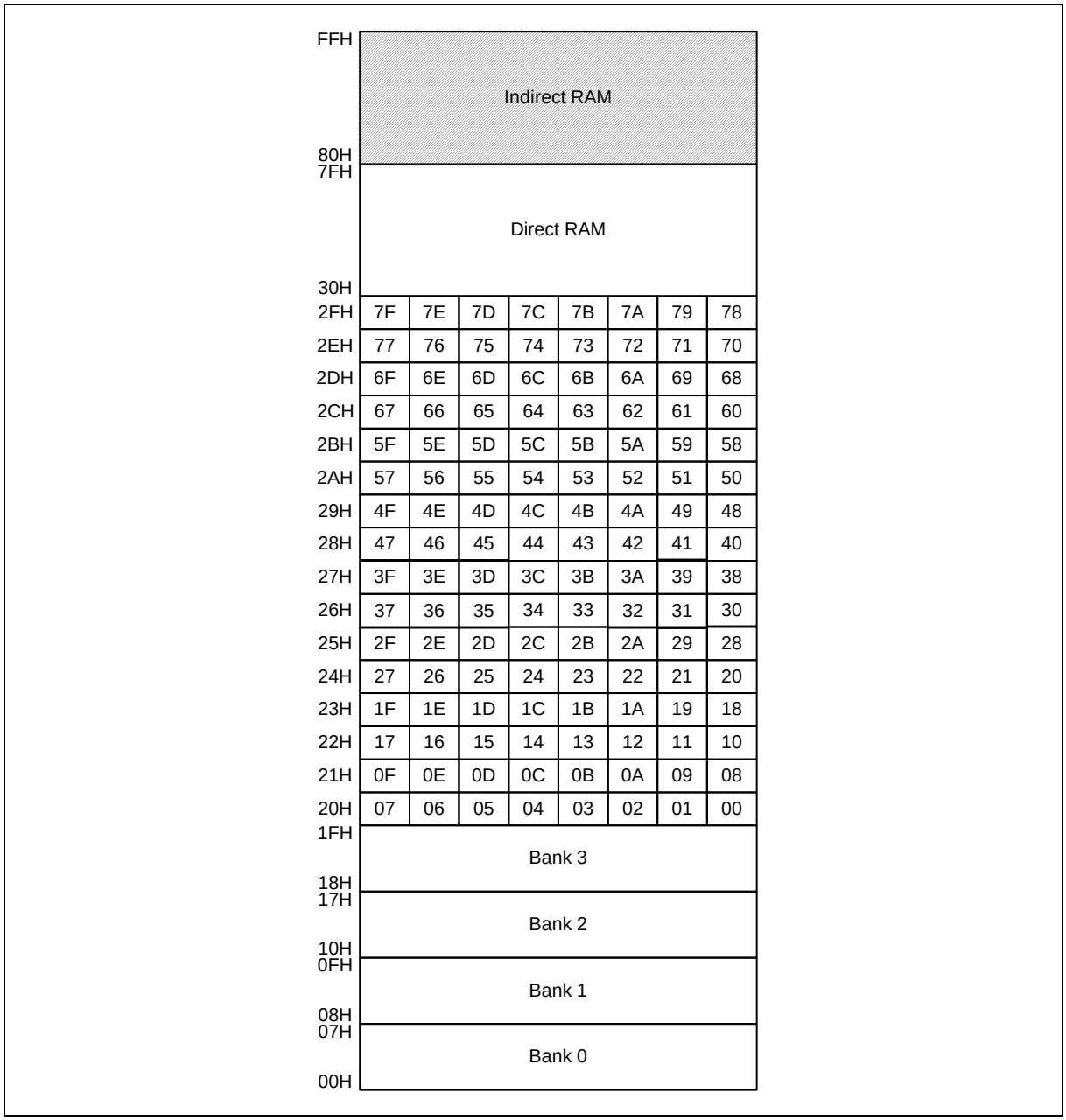


Figure 7-3: Scratch pad RAM

7.4.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the N79E342 series can work with only one particular bank. The bank selection is done by

setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

7.4.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

7.4.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8 SPECIAL FUNCTION REGISTERS

The N79E342 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The N79E342 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

F8	IP1	BUZCON						
F0	B						PADIDS	IP1H
E8	EIE							
E0	ACC	ADCCON	ADCH	ADCCON1				
D8	WDCON							
D0	PSW							
C8							NVMCON	NVMDATA
C0							NVMADDRL	TA
B8	IP0							
B0		P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	IE							
A0	P2	KBI	AUXR1					
98								
90	P1					DIVM		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	CKCON1
80	P0	SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

Note: 1. The SFRs in the column with dark borders are bit-addressable

2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

SYMBOL	DEFINITION	ADDRESS	MSB			BIT_ADDRESS, SYMBOL				LSB	RESET
BUZCON	Buzzer control register	F9H	BUZDIV.7	BUZDIV.6	BUZDIV.5	BUZDIV.4	BUZDIV.3	BUZDIV.2	BUZDIV.1	BUZDIV.0	00000000B
IP1	Interrupt priority 1	F8H	(FF) -	(FE) -	(FD) -	(FC) PWDI	(FB) -	(FA) -	(F9) PKB	(F8) -	xxx0xx0xB
IP1H	Interrupt high priority 1	F7H	-	-	-	PWDIH	-	-	PKBH	-	xxx0xx0xB
PADIDS	Port ADC Digital Input Disable	F6H	-	PADIDS.6	PADIDS.5	PADIDS.4	PADIDS.3	-	-	-	x0000xxxB
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) -	(EE) -	(ED) -	(EC) EWDI	(EB) -	(EA) -	(E9) EKB	(E8) -	xxx0xx0xB
ADCCON1	ADC control register 1	E3H	ADCLK.1	ADCLK.0	-	-	-	-	-	-	00xxxxxxB
ADCH	ADC converter result high register	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	00000000B
ADCCON	ADC control register	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0	00000000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0000B Watchdog reset: 0x00 0100B Power on reset 0x000000B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-	-	00000000B
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDRL	NVM low byte address	C6H	-	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	00000000B
IP0	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) -	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x00x0000B
IP0H	Interrupt high priority	B7H	-	PADCH	PBOH	-	PT1H	PX1H	PT0H	PX0H	x00x0000B
P2M2	Port 2 output mode 2	B6H	-	-	-	-	-	-	P2M2.1	P2M2.0	xxxxxx00B
P2M1	Port 2 output mode 1	B5H	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0	00000000B
P1M2	Port 1 output mode 2	B4H	-	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	x0x00000B
P1M1	Port 1 output mode 1	B3H	-	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	x0x00000B
P0M2	Port 0 output mode 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	-	-	-	00000xxxB
P0M1	Port 0 output mode 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	-	-	-	00000xxxB
IE	Interrupt enable	A8H	(AF) EA	(AE) EADC	(AD) EBO	(AC) -	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	000x0000B
AUXR1	AUX function register	A2H	KBF	BOD	BOI	LPBOV	SRST	ADCEN	BUZE	-	000x000xB
KBI	Keyboard Interrupt	A1H	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	-	-	-	00000xxxB
P2	Port 2	A0H	(A7) -	(A6) -	(A5) -	(A4) -	(A3) -	(A2) -	(A1) XTAL1	(A0) XTAL2 CLKOUT	xxxxxx11B
DIVM	uC clock divide register	95H									00000000B
P1	Port 1	90H	(97) -	(96)	(95) /RST VPP	(94) /INT1 STADC	(93) /INT0	(92) T0	(91)	(90) Buz	x1111111B
CKCON1	Clock control 1	8FH	-	-	-	-	-	-	CLKSRC.1	CLKSRC.0	**All reset: Bit1-0 = CONFIG0.1-0**
CKCON	Clock control	8EH	-	-	-	T1M	T0M	-	-	-	xxx00xxxB
TH1	Timer high 1	8DH									00000000B
TH0	Timer high 0	8CH									00000000B

TL1	Timer low 1	8BH									00000000B
TL0	Timer low 0	8AH									00000000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00000000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	00000000B
PCON	Power control	87H	-	-	BOF	POR	GF1	GF0	PD	IDL	xxxx0000B
DPH	Data pointer high	83H									00000000B
DPL	Data pointer low	82H									00000000B
SP	Stack pointer	81H									00000111B
P0	Port 0	80H	(87) T1	(86) AD3	(85) AD2	(84) AD1	(83) AD0	(82) -	(81) -	(80) -	11111xxxB

Table 8-2: Special Function Registers

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	-	-	-

Mnemonic: P0 Address: 80h

P0.7-0.3: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P0.7	Timer 1 pin or KB7 pin of keypad input by alternative.
6	P0.6	AD3 or KB6 pin of keypad input by alternative.
5	P0.5	AD2 or KB5 pin of keypad input by alternative.
4	P0.4	AD1 or KB4 pin of keypad input by alternative.
3	P0.3	AD0 or KB3 pin of keypad input by alternative.
2-0	-	Reserved.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer.

		This is the high byte of the DPTR 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	-	Reserved.
6	-	Reserved.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on

		$\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 13-bits timer/counter; THx 8 bits and TLx 5 bits which serve as pre-scalar.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits.

		(Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.

4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks.
2-0	-	Reserved.

CLOCK CONTROL 1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	CLKSRC.1	CLKSRC.0

Mnemonic: CKCON1 Address: 8Fh

BIT	NAME	FUNCTION
7-2	-	Reserved.
1-0	CLKSRC.[1:0]	Clock source selectors (TA protected bits): 00: 4MHz to 12MHz external crystal. 01: Internal 455KHz RC oscillator. 10: 32KHz to 1MHz external crystal. 11: External oscillator in XTAL1. Note that upon power-on-reset, the content of CONFIG0.1-0 will map to these bits. However, user is able to re-configure these CLKSRC bits after reset. These bits will have priority over CONFIG0.Fosc1 and Fosc0 bits.

PORT 1

Bit:	7	6	5	4	3	2	1	0
	-	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.6-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	-	
6	P1.6	Dedicated GPIO pin (for 16L package only).
5	P1.5	/RST Pin or VPP pin by alternative.
4	P1.4	INT1 interrupt or STADC pin by alternative.
3	P1.3	INT0 interrupt.
2	P1.2	Timer 0.
1	P1.1	Dedicated GPIO pin.

0	P1.0	Buz pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

DIVIDER CLOCK

Bit:	7	6	5	4	3	2	1	0
	DIVM.7	DIVM.6	DIVM.5	DIVM.4	DIVM.3	DIVM.2	DIVM.1	DIVM.0

Mnemonic: DIVM Address: 95h

BIT	NAME	FUNCTION
7-0	DIVM.[7:0]	The DIVM register is clock divider of uC. Refer OSCILLATOR chapter.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7-2	-	Reserved
1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

KEYBOARD INTERRUPT

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	-	-	-

Mnemonic: KBI Address: A1h

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt (for 16L package only).
2-0	-	Reserved.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	ADCEN	BUZE	-

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power Down mode. 1: When BOD is enable, the Brown Out detect circuit is turned on by Power Down mode. This control can help save 15/16 of the Brownout circuit power. When uC is in Power Down mode, the BOD will enable internal RC OSC (455KHZ)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	BUZE	Square-wave enable bit: When set, the square wave is output to the BUZ (P1.0) pin.
0	-	Reserved.

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	-	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	-	Reserved.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.

1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

PORT 0 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	-	-	-

Mnemonic: P0M1 Address: B1h

BIT	NAME	FUNCTION
7-3	P0M1.[7:3]	To control the output configuration of P0 bits [7:3].
2-0	-	Reserved.

PORT 0 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	-	-	-

Mnemonic: P0M2 Address: B2h

BIT	NAME	FUNCTION
7-3	P0M2.[7:3]	To control the output configuration of P0 bits [7:3]
2-0	-	Reserved.

PORT 1 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	-	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

BIT	NAME	FUNCTION
7	-	Reserved.
6	P1M1.6	To control the output configuration of P1.6.
5	-	Reserved.
4-0	P1M1.4-0	To control the output configuration of P1.4-1.0.

PORT 1 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	-	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

BIT	NAME	FUNCTION
7	-	Reserved.
6	P1M2.6	To control the output configuration of P1.6.

5	-	Reserved.
4-0	P1M2.[4:0]	To control the output configuration of P1 bits [4:0]

PORT 2 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0

Mnemonic: P2M1 Address: B5h

BIT	NAME	FUNCTION
7	P2S	0: Disable Schmitt trigger inputs on port 2 and enable TTL inputs on port 2. 1: Enables Schmitt trigger inputs on Port 2.
6	P1S	0: Disable Schmitt trigger inputs on port 1 and enable TTL inputs on port 1. 1: Enables Schmitt trigger inputs on Port 1.
5	P0S	0: Disable Schmitt trigger inputs on port 0 and enable TTL inputs on port 0 1: Enables Schmitt trigger inputs on Port 0.
4	ENCLK	1: Enabled clock output to XTAL2 pin (P2.0).
3	T1OE	1: The P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
2	T0OE	1: The P1.2 pin is toggled whenever Timer 0 overflows. The output frequency is therefore one half of the Timer 0 overflow rate.
1	P2M1.1	To control the output configuration of P2.1.
0	P2M1.0	To control the output configuration of P2.0.

PORT 2 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2M2.1	P2M2.0

Mnemonic: P2M2 Address: B6h

BIT	NAME	FUNCTION
7-2	-	Reserved.
1-0	P2M2.[1:0]	To control the output configuration of P2 bits [1:0]

Port Output Configuration Settings:

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

INTERRUPT HIGH PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	PADCH	PBOH	-	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PADCH	1: To set interrupt high priority of ADC is highest priority level.
5	PBOH	1: To set interrupt high priority of Brown Out Detector is highest priority level.
4	-	Reserved.
3	PT1H	1: To set interrupt high priority of Timer 1 is highest priority level.
2	PX1H	1: To set interrupt high priority of External interrupt 1 is highest priority level.
1	PT0H	1: To set interrupt high priority of Timer 0 is highest priority level.
0	PX0H	1: To set interrupt high priority of External interrupt 0 is highest priority level.

INTERRUPT PRIORITY 0

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PBO	-	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PADC	1: To set interrupt priority of ADC is higher priority level.
5	PBO	1: To set interrupt priority of Brown Out Detector is higher priority level.
4	-	Reserved.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

NVM LOW BYTE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	-	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0

Mnemonic: NVMADDRL Address: C6h

BIT	NAME	FUNCTION
7	-	Please Keep it at 0.

6~0	NVMADDR.[6:0]	The NVM low byte address: The register indicates NVM data memory of low byte address on On-Chip code memory space.

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	-	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit: 0: Without erase NVM page(n). 1: Set this bit to erase page(n) of NVM. The NVM has 8 pages and each page have 16 bytes data memory. Initiate page select by programming NVMADDL registers, which will automaticly enable page area. When user set this bit, the page erase process will begin and program counter will halt at this instruction. After the erase process is completed, program counter will continue executing next instruction.
6	EWR	NVM data write bit: 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5-0	-	Reserved

NVM DATA

Bit:	7	6	5	4	3	2	1	0
	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA3	NVMDATA.2	NVMDATA.1	NVMDATA.0

Mnemonic: NVMDATA Address: CFh

BIT	NAME	FUNCTION
7~0	NVMDATA.[7:0]	The NVM data write register. The read NVM data is by MOVC instruction.

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4~3	RS1~RS0	Register bank select bits.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.
5	WD1	Watchdog Timer Time-out Select bits. These bits determine the time-out period

4	WD0	of the watchdog timer. The reset time-out period is 512 clocks longer than the watchdog time-out. WD1 / WD0 / Interrupt time-out / Reset time-out 0 / 0 / 2^6 / 2^6 + 512 0 / 1 / 2^9 / 2^9 + 512 1 / 0 / 2^{13} / 2^{13} + 512 1 / 1 / 2^{15} / 2^{15} + 512
3	WDIF	Watchdog Timer Interrupt Flag 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.
2	WTRF	Watchdog Timer Reset Flag 1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.
1	EWRST	0: Disable Watchdog Timer Reset. 1: Enable Watchdog Timer Reset.
0	WDCLR	Reset Watchdog Timer This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt, if EWDI (EIE.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWRST is set. This bit is self-clearing by hardware.

The WDCON SFR is set to 0x000000B on a reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on a Power-on reset, reset pin reset, and Watch Dog Timer reset.

All the bits in this SFR have unrestricted read access. WDRUN, WD0, WD1, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```
TA      REG     C7H
WDCON   REG     D8H
MOV     TA, #AAH            ; To access protected bits
MOV     TA, #55H
SETB    WDCON.0             ; Reset watchdog timer
ORL     WDCON, #00110000B   ; Select 26 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #00000010B   ; Enable watchdog reset
```

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

BIT	NAME	FUNCTION
7-0	ACC.[7:0]	The A or ACC register is the standard 8052 accumulator

ADC CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

BIT	NAME	FUNCTION
7-6	ADC.1-0	2 LSB of 10-bit A/D conversion result.
5	ADCEX	Enable STADC-triggered conversion 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.4).
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. *Note:* ***1.*** *It is recommended to clear ADCI before ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.* ***2.*** *Software clearing of ADCS will abort conversion in progress.* ***3.*** ADC cannot start a new conversion while ADCS is high.
2	RCCLK	0: The CPU clock is used as ADC clock source. 1: The internal RC 455KHz clock is used as ADC clock source. *Note:* ***1.*** *This bit can only be set/cleared when ADCEN=0.* ***2.*** *The ADC clock source will goes through pre-scalar of /1, /2, /4 or /8, selectable by ADCLK bits (SFR ADCCON1.6-7).*
1	AADR1	The ADC input select. See table below.
0	AADR0	The ADC input select. See table below.

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

AADR1, AADR0: ADC Analog Input Channel select bits:

AADR1	AADR0	SELECTED ANALOG INPUT CHANNEL
0	0	AD0 (P0.3)
0	1	AD1 (P0.4)
1	0	AD2 (P0.5)
1	1	AD3 (P0.6)

(These bits can only be changed when ADCI and ADCS are both zero.)

ADC CONVERTER RESULT HIGH REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: E2h

BIT	NAME	FUNCTION
7-0	ADC.[9:2]	8 MSB of 10-bit A/D conversion result.

ADC CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	ADCLK.1	ADCLK.0	-	-	-	-	-	-

Mnemonic: ADCCON1 Address: E3h

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>7-6</td><td>ADCLK.1~0</td><td>ADC Clock Prescaler:
The 10-bit ADC needs a clock to drive the converting and the clock frequency need to be within 200KHz to 5MHz. ADCLK[1:0] controls the frequency of the clock to ADC block as below table.
<table>
<tr><td>ADCLK.1</td><td>ADCLK.0</td><td>ADC Clock Frequency</td></tr>
<tr><td>0</td><td>0</td><td>ADCCLK/1 (default)</td></tr>
<tr><td>0</td><td>1</td><td>ADCCLK/2</td></tr>
<tr><td>1</td><td>0</td><td>ADCCLK/4</td></tr>
<tr><td>1</td><td>1</td><td>ADCCLK/8</td></tr>
</table>
Note: User required to clear ADCEN (ADCEN = 0) when re-configure the ADC clock prescaler.</td></tr>
<tr><td>5-0</td><td>-</td><td>Reserved.</td></tr>
</table>

INTERRUPT ENABLE REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	-	-	EKB	-

Mnemonic: EIE Address: E8h

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	EWDI	0: Disable Watchdog Timer Interrupt. 1: Enable Watchdog Timer Interrupt.
3-2	-	Reserved.
1	EKB	0: Disable Keypad Interrupt. 1: Enable Keypad Interrupt.
0	-	Reserved.

B REGISTER

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

BIT	NAME	FUNCTION
7-0	B.[7:0]	The B register is the standard 8052 register that serves as a second accumulator.

PORT ADC DIGITAL INPUT DISABLE

Bit:	7	6	5	4	3	2	1	0
	-	PADIDS.6	PADIDS.5	PADIDS.4	PADIDS.3	-	-	-

Mnemonic: PADIDS Address: F6h

BIT	NAME	FUNCTION
7	-	Reserved.
6	PADIDS.6	P0.6 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 3.
5	PADIDS.5	P0.5 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 2.
4	PADIDS.4	P0.4 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 1.

3	PADIDS.3	P0.3 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 0.
2-0	-	Reserved.

INTERRUPT HIGH PRIORITY 1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWDIH	-	-	PKBH	-

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3-2	-	Reserved.
1	PKBH	1: To set interrupt high priority of Keypad is highest priority level.
0	-	Reserved.

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWDI	-	-	PKB	-

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3-2	-	Reserved.
1	PKB	1: To set interrupt priority of Keypad is higher priority level.
0	-	Reserved.

BUZZER CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	BUZDIV.7	BUZDIV.6	BUZDIV.5	BUZDIV.4	BUZDIV.3	BUZDIV.2	BUZDIV.1	BUZDIV.0

Mnemonic: BUZCON Address: F9h

BIT	NAME	FUNCTION
7-0	BUZDIV	Buzzer division select bits: These bits are division selector. User may configure these bits to further divide the cpu clock in order to generate the desired buzzer output frequency. The following shows the equation for the buzzer output rate; Fbuz = Fcpu x 1/[(16)x(BUZDIV + 1)]

9 INSTRUCTION SET

The N79E342 series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly the same. However, the timing of these instructions is different in two ways. Firstly, the machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Secondly, it can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can fetch twice per machine cycle (i.e., six clocks per fetch).

The timing differences create an advantage for the N79E342 series. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the N79E342 series reduces the number of dummy fetches and wasted cycles, and therefore improves overall efficiency, compared to the standard 8051/52.

Op-code	HEX Code	Bytes	N79E342 series Machine Cycle	N79E342 series Clock cycles	8032 Clock cycles	N79E342 series vs. 8032 Speed Ratio
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3

ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3

DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
DEC DPTR	A5	1	2	8	24	3
MUL AB	A4	1	5	20	48	2.4
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3
ANL A, R6	5E	1	1	4	12	3
ANL A, R7	5F	1	1	4	12	3
ANL A, @R0	56	1	1	4	12	3
ANL A, @R1	57	1	1	4	12	3
ANL A, direct	55	2	2	8	12	1.5
ANL A, #data	54	2	2	8	12	1.5
ANL direct, A	52	2	2	8	12	1.5
ANL direct, #data	53	3	3	12	24	2
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3
ORL A, @R1	47	1	1	4	12	3
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3

XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3

MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5

MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	6	24	3
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
MOV C, bit	A2	2	2	8	12	1.5

MOV bit, C	92	2	2	8	24	3
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
LCALL addr16	12	3	4	16	24	1.5
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
LJMP addr16	02	3	4	16	24	1.5
JMP @A+DPTR	73	1	2	6	24	3
SJMP rel	80	2	3	12	24	2
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2

DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

Table 9-1: Instruction Set for N79E342

9.1 Instruction Timing

This section is important because some applications use software instructions to generate timing delays. It also provides more information about timing differences between the N79E342 series and the standard 8051/52.

In N79E342 series, each machine cycle is four clock periods long. Each clock period is called a state, and each machine cycle consists of four states: C1, C2 C3 and C4, in order. Both clock edges are used for internal timing, so the duty cycle of the clock should be as close to 50% as possible to avoid timing conflicts.

The N79E342 series does one op-code fetch per machine cycle, so, in most instructions, the number of machine cycles required is equal to the number of bytes in the instruction. There are 256 available op-codes. 128 of them are single-cycle instructions, so many op-codes are executed in just four clocks period. Some of the other op-codes are two-cycle instructions, and most of these have two-byte op-codes. However, there are some instructions that have one-byte instructions yet take two cycles to execute. One important example is the MOVX instruction.

In the standard 8052, the MOVX instruction is always two machine cycles long. However, in the N79E342 series each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8052. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8052 in terms of clock periods.

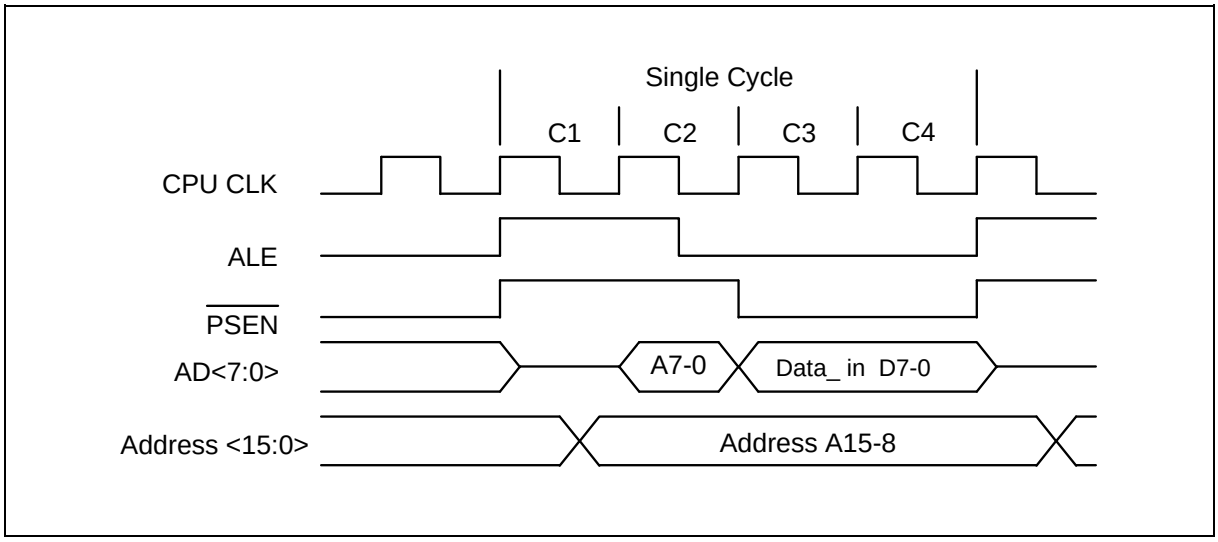


Figure 9-1: Single Cycle Instruction Timing

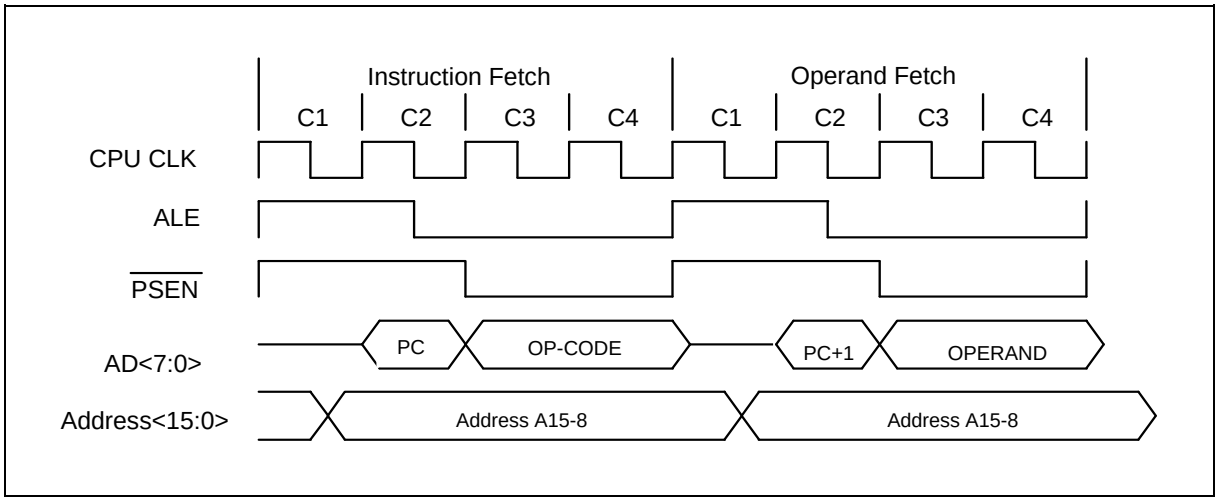


Figure 9-2: Two Cycles Instruction Timing

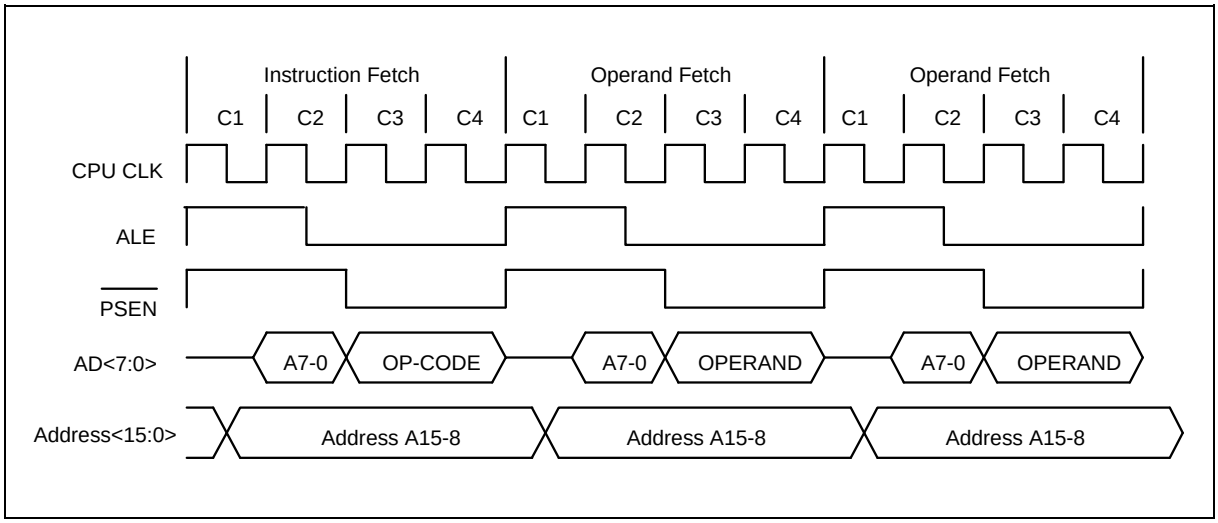


Figure 9-3: Three Cycles Instruction Timing

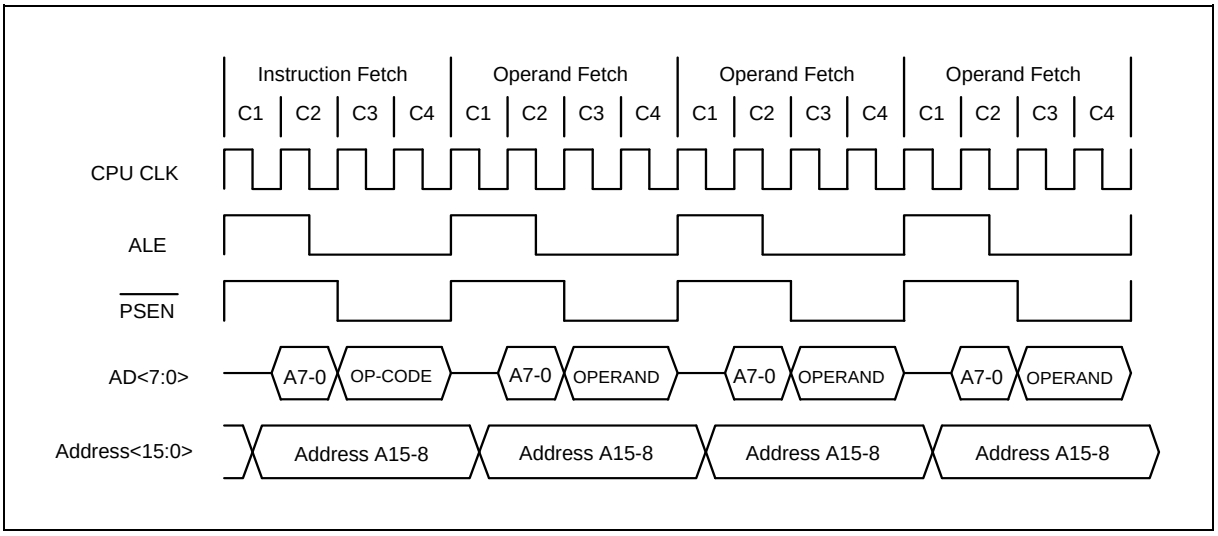


Figure 9-4: Four Cycles Instruction Timing

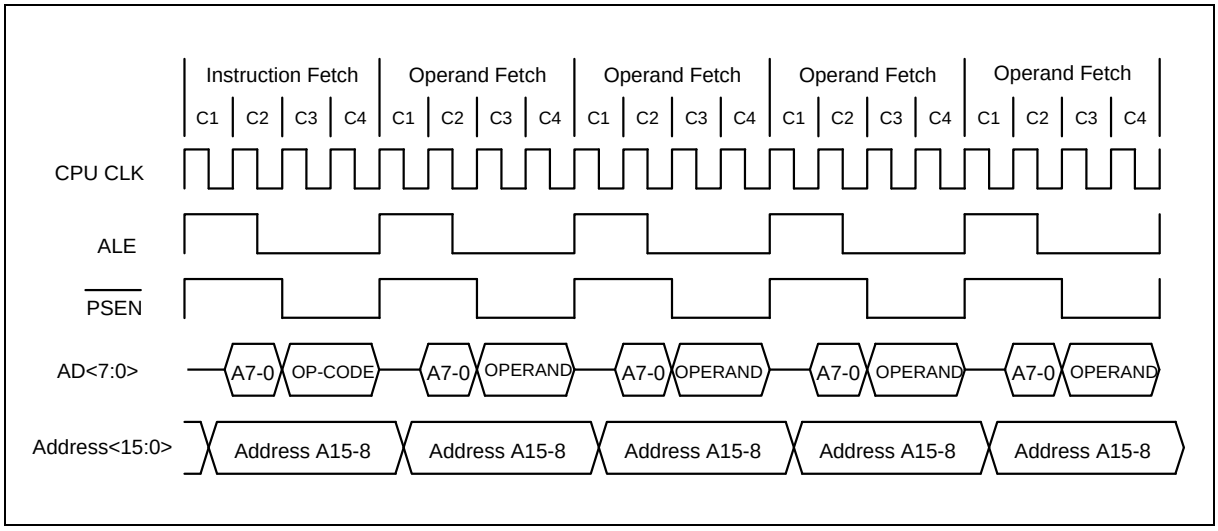


Figure 9-5: Five Cycles Instruction Timing

10 POWER MANAGEMENT

The N79E342 series has several features that help the user to control the power consumption of the device. These modes are discussed in the next two sections.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer and Watchdog timer blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle Mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a low on the external /RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held low for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the N79E342 series are exiting from an Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

10.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The N79E342 series will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detected. An external reset can be used to exit the Power down state. The low on /RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power down mode are external interrupts, keyboard interrupt (KBI), brownout reset (BOR), watchdog timer interrupt (if WDTCK = 0) and ADC. Note that for ADC waking up from powerdown, the device need to run on internal rc and software perform start ADC prior to powerdown.

The N79E342 series can be waken up from the Power Down mode by forcing an external interrupt pin activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then either a low-level or a falling-edge at external interrupt pin will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

11 RESET CONDITIONS

The user has several hardware related options for placing the N79E342 series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 Sources of reset

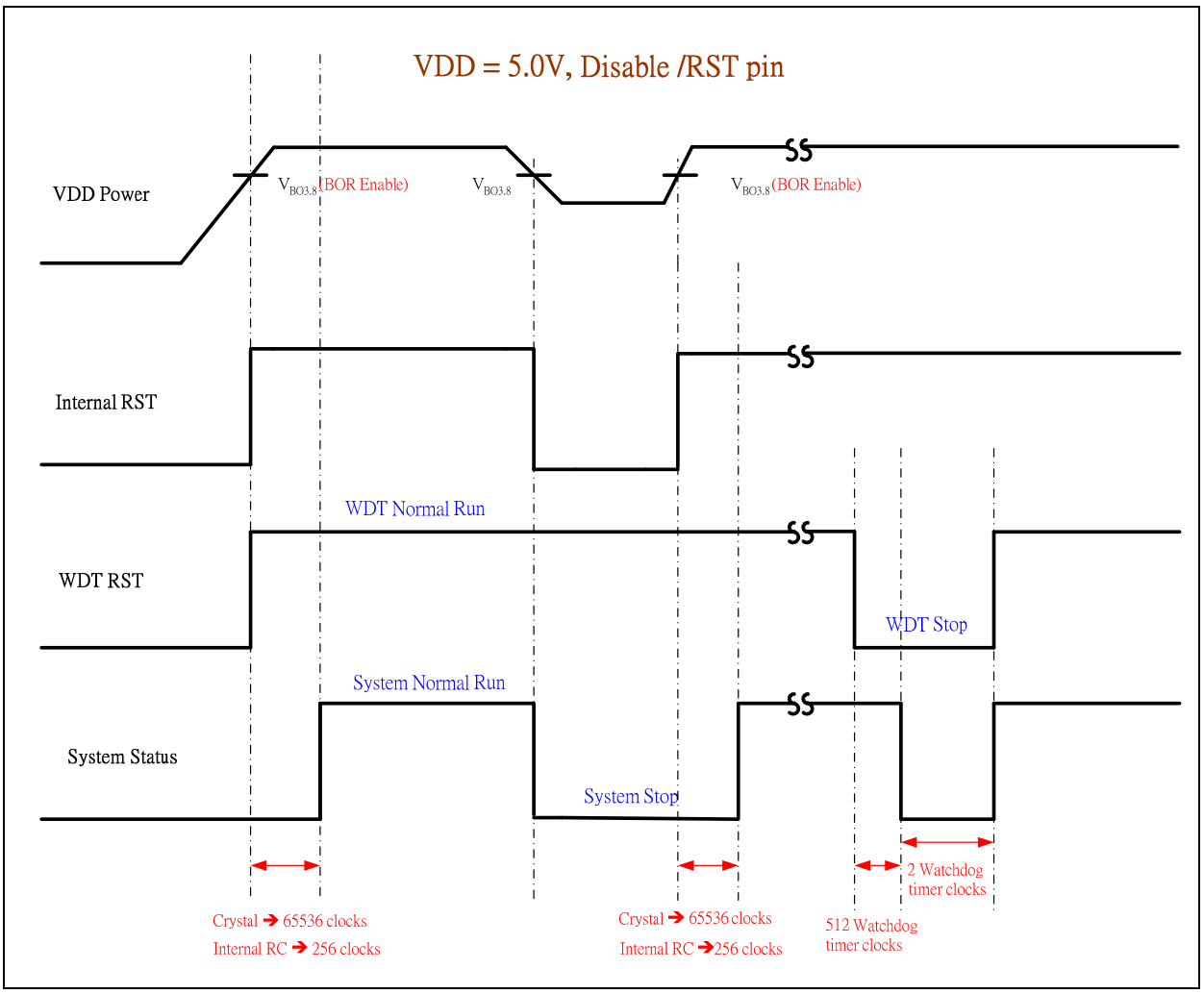


Figure 11-1: Reset and Vdd monitor timing diagram, disable /RST pin.

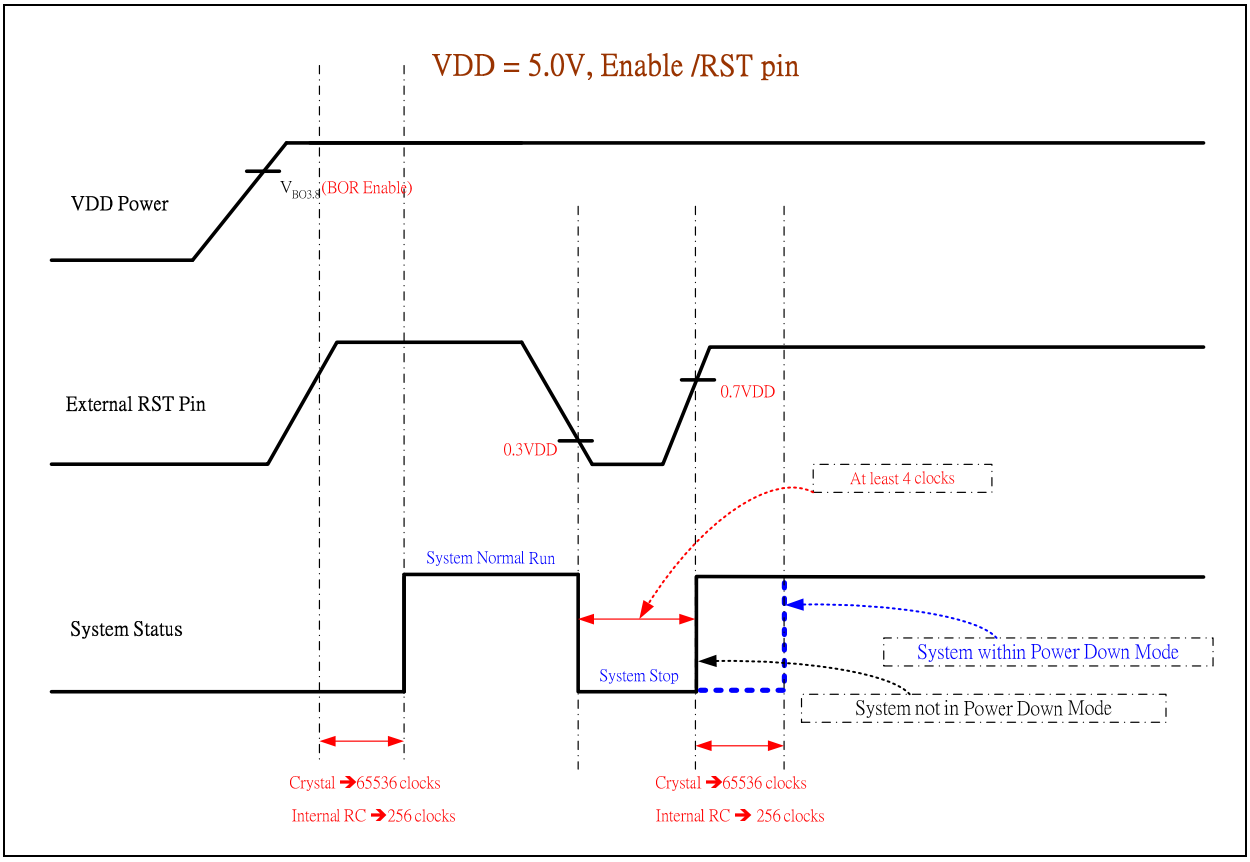


Figure 11-2: Reset and Vdd monitor timing diagram, enable /RST pin.

11.1.1 External Reset

The device samples the /RST pin every machine cycle during state C4. The /RST pin must be held low for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as /RST is low and remains low up to two machine cycles after /RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

11.1.2 Power-On Reset (POR)

When the power supply rises to proper level, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets. During power-on-reset, all port pins will be tri-stated. After power-on-reset, the port pins state will determined by PRHI value.

11.1.3 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the

Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

11.2 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state. The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2V, the minimum operating voltage for the RAM. If VDD falls below 2V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset. The WDCON SFR is set to a 0x00 0000B on the reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by external reset. EWRST (WDCON.1) is cleared by any reset. Software or any reset will clear WDIF (WDCON.3) bit.

Some of the bits in the WDCON SFR (WDRUN, WDCLR, EWRST, WDIF, WD0 and WD1) have un-restricted read access which required Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

For all SFR reset state values, please refer to Table 8-2: Special Function Registers.

12 INTERRUPTS

The N79E342 series have four priority level interrupts structure with 8 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

12.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

The ADC can generate interrupt after finished ADC converter. There is one interrupt source, which is obtained by the ADCI bit in the ADCCON SFR. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

Keyboard interrupt is generated when any of the keypad connected to P0 (P0.3-P0.7) pins is pressed. Each keypad interrupt can be individually enabled or disabled. User will have to software clear the flag bit.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBO (IE.5) and global interrupt enable are set.

All the bits that generate interrupts can be set or reset by software, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all interrupts.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being execute.
3. The current instruction does not involve a write to IE, EIE, IP0, IP0H, IP1 or IPH1 registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met,

the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as follows:

VECTOR LOCATIONS FOR INTERRUPT SOURCES

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
-	0023h	Brownout Interrupt	002Bh
-	0033h	KBI Interrupt	003Bh
-	0043h	-	004Bh
Watchdog Timer	0053h	ADC Interrupt	005Bh
-	0063h	-	006Bh
-	0073h	-	007Bh

Table 12-1: Vector locations for interrupt sources

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

12.2 Priority Level Structure

The N79E342 series uses a four priority level interrupt structure (highest, high, low and lowest) and supports up to **8 i**nterrupt sources. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as table below. This allows great flexibility in controlling and handling many interrupt sources.

Priority Bits		Interrupt Priority Level
IPXH	IPX	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 12-2: Four-level interrupt priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

As below Table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Interrupt Enable Bits	Interrupt Priority	Flag cleared by	Arbitration Ranking	Power Down Wakeup
External Interrupt 0	IE0	0003H	EX0 (IE0.0)	IP0H.0, IP0.0	Hardware, Follow the inverse of pin	1(highest)	Yes
Brownout Detect	BOF	002BH	EBO (IE.5)	IP0H.5, IP0.5	Software	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (EIE.4)	IP1H.4, IP1.4	Software	3	Yes(1)
Timer 0 Interrupt	TF0	000BH	ET0 (IE.1)	IP0H.1, IP0.1	Hardware, software	4	No
ADC Converter	ADCI	005BH	EAD (IE.6)	IP0H.6, IP0.6	Hardware	5	Yes(1)
External Interrupt 1	IE1	0013H	EX1 (IE.2)	IP0H.2, IP0.2	Hardware, Follow the inverse of pin	6	Yes
KBI Interrupt	KBF	003BH	EKB (EIE.1)	IP1H.1, IP1.1	Software	7	Yes
Timer 1 Interrupt	TF1	001BH	ET1 (IE.3)	IP0H.3, IP0.3	Hardware, software	8	No

Note: 1. The Watchdog Timer and ADC Converter can wake up Power Down Mode when its clock source is from internal RC.

Table 12-3: Vector location for Interrupt sources and power down wakeup

12.3 Response Time

The response time for each interrupt source depends on several factors, such as the nature of the

interrupt and the instruction underway. In the case of external interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the N79E342 series are performing a write to IE, EIE, IP0, IP0H, IP1 or IP1H and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, EIE, IP0, IP0H, IP1 or IP1H access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycles is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

12.4 Interrupt Inputs

The N79E342 series have total 8 interrupt sources with two individual interrupt inputs sources. They are IE0, IE1, BOF, KBF, WDT, TF0, TF1 and ADC. Two interrupt inputs are identical to those present on the standard 80C51 microcontroller as show in below figures.

If an external interrupt is enabled when the N79E342 series are put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation.

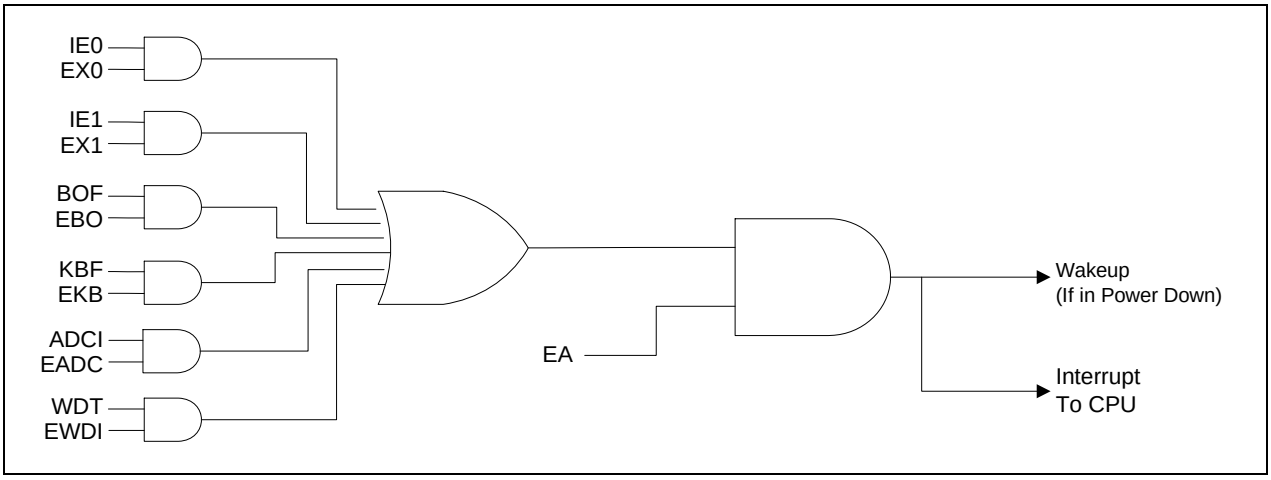


Figure 12-1: Interrupt Sources that can wake up from Power Down Mode

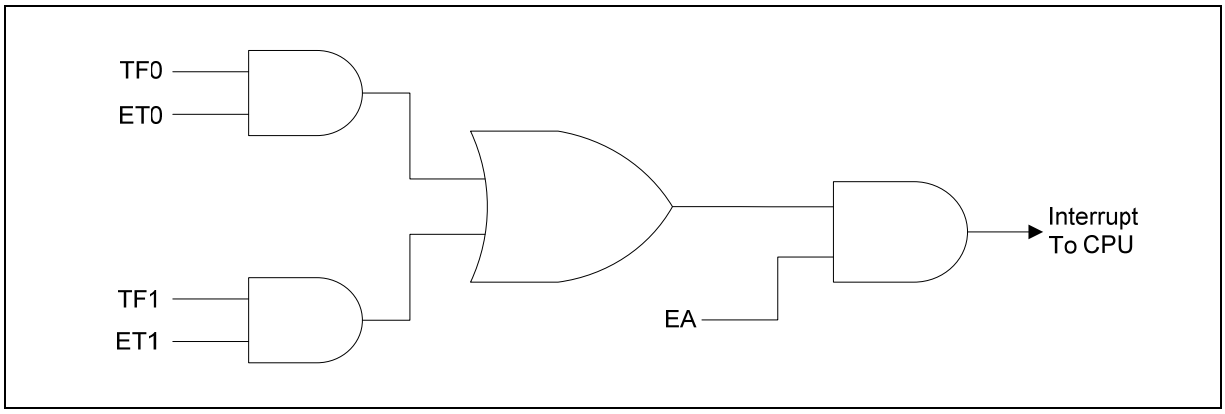


Figure 12-2: Interrupt Sources that cannot wake up from Power-down Mode

13 PROGRAMMABLE TIMERS/COUNTERS

The N79E342 series have two 16-bit programmable timer/counters and one programmable Watchdog Timer. The Watchdog Timer is operationally quite different from the other two timers. Its' timer/counters have additional timer 0 or timer 1 overflow toggle output enable feature as compare to conventional timer/counters. This timer overflow toggle output can be configured to automatically toggle T0 or T1 pin output whenever a timer overflow occurs.

13.1 Timer/Counters 0 & 1

The N79E342 series have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 for Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/8 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

13.1.1 Time-Base Selection

The N79E342 series can operate like the standard 8051/52 family, counting at the rate of 1/12 of the clock speed, or in turbo mode, counting at the rate of 1/4 clock speed. The speed is controlled by the T0M and T1M bits in CKCON, and the default value is zero, which uses the standard 8051/52 speed.

13.1.2 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (P1.2 for Timer 0) or T1 (P0.7 for Timer 1). For clock cycles, the time base may be 1/12 or 1/4 clock speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated in next figure below.

In “Timer” mode, if output toggled enable bit of P2M1.T0OE or P2M1.T1OE is enable, T0 or T1 output pin will toggle whenever a timer overflow occurs.

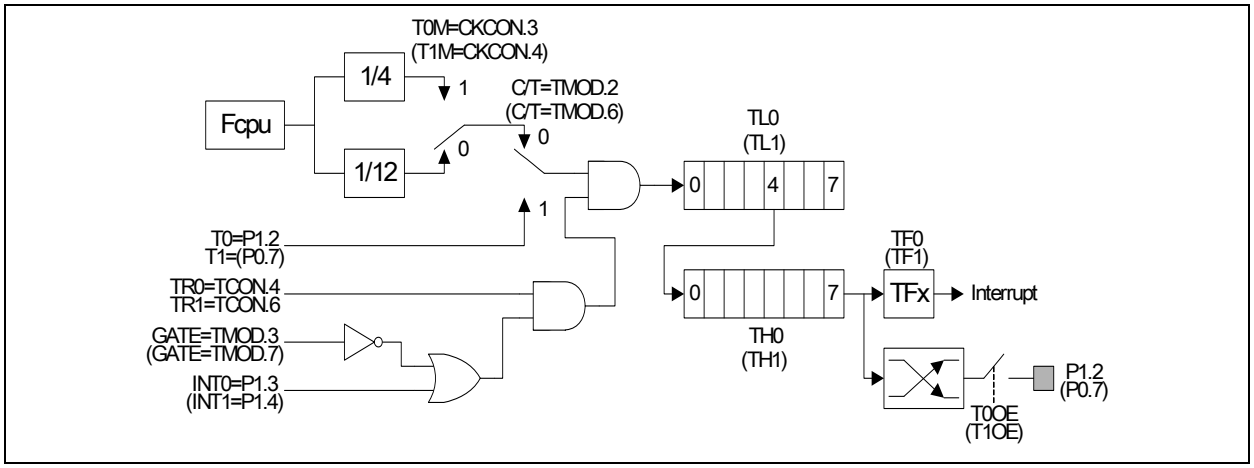


Figure 13-1: Timer/Counters 0 & 1 in Mode 0

13.1.3 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

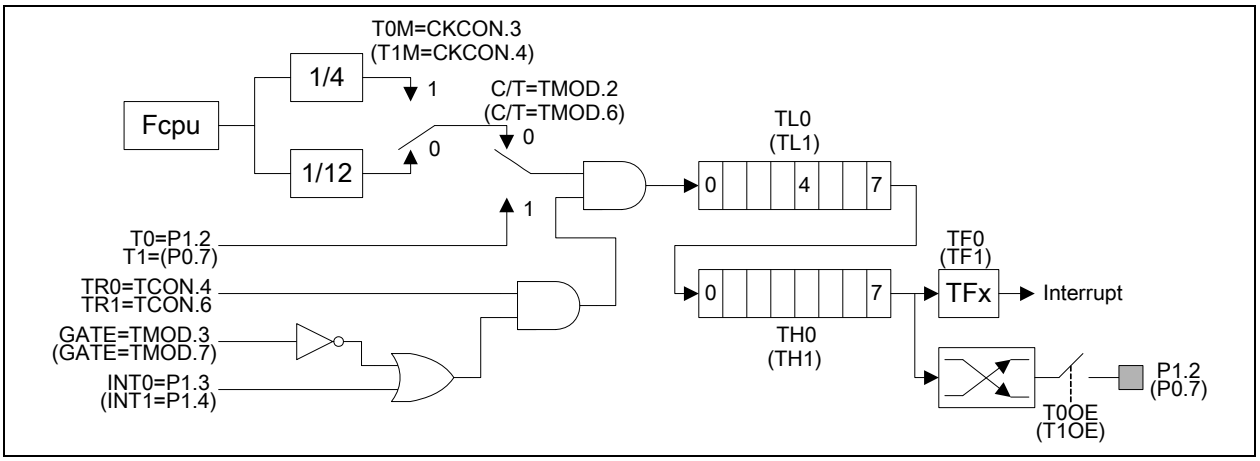


Figure 13-2: Timer/Counters 0 & 1 in Mode 1

13.1.4 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{\text{INTx}}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

In “Timer” mode, if output toggled enable bit of P2M1.T0OE or P2M1.T1OE is enable, T0 or T1 output pin will toggle whenever a timer overflow occurs.

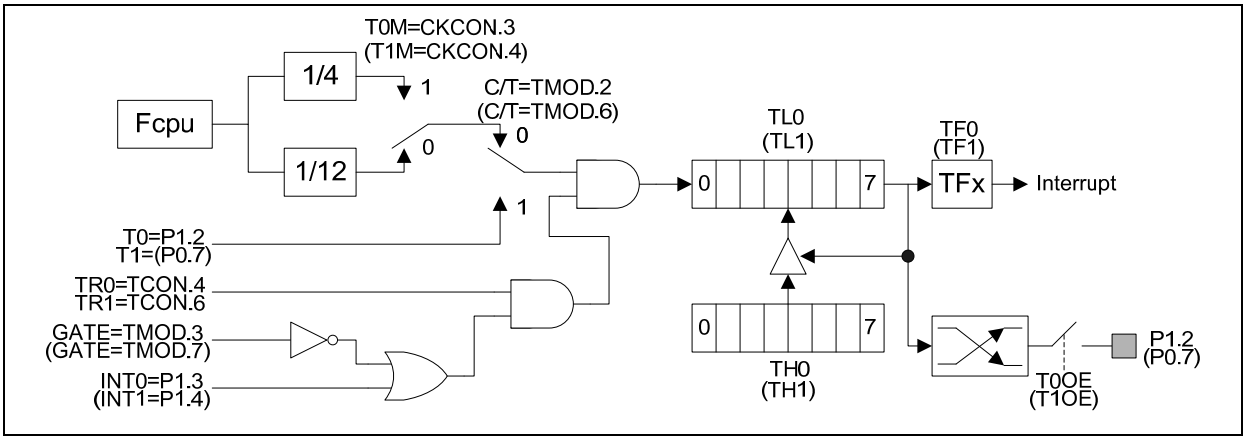


Figure 13-3: Timer/Counter 0 & 1 in Mode 2

13.1.5 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

In “Timer” mode, if output toggled enable bit of P2M1.T0OE or P2M1.T1OE is enable, T0 or T1 output pin will toggle whenever a timer overflow occurs.

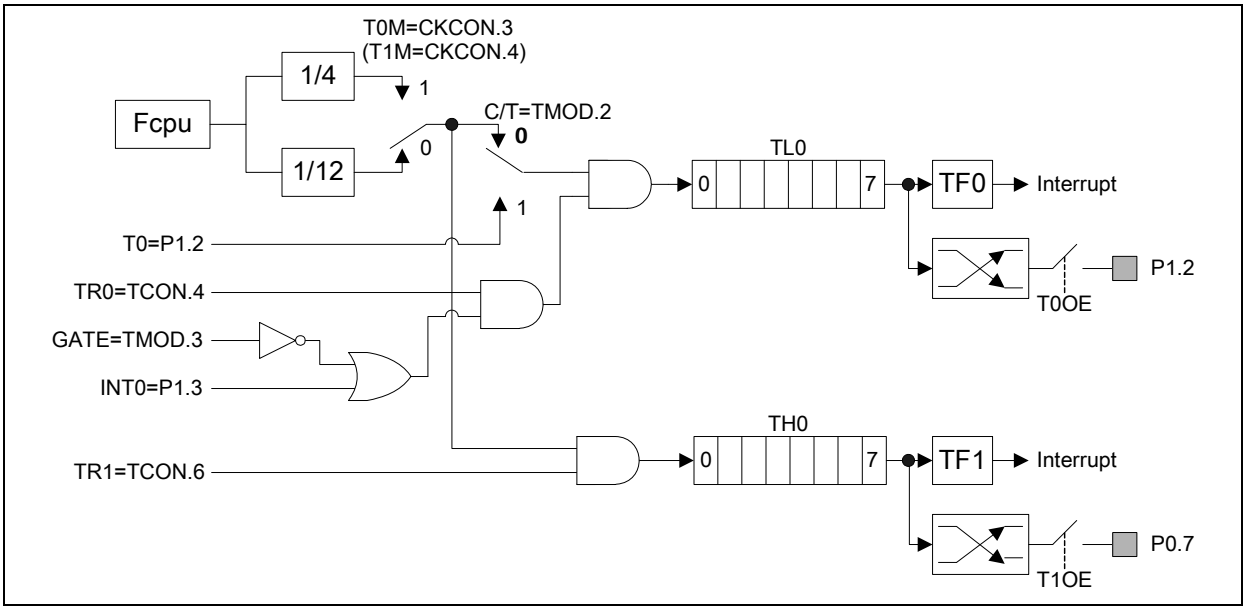


Figure 13-4: Timer/Counter Mode 3

14 NVM MEMORY

The N79E342 series has NVM data memory of 128 bytes of 8 pages and each page of 16 bytes.

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVC A,@A+DPTR instruction, and write data is by SFR of NVMADDRL, NVMDATA and NVMCON. Before write data to NVM memory, the page must be erased by providing page address on NVMADDRL, which address of On-Chip Code Memory space will decode, then set EER of NVMCON.7. This will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

For writing data to NVM memory, user must set address and data NVMADDRL and NVMDATA, then set EWR of NVMCON.6 to initiate nvm data write. The uC will hold program code and PC Counter, and then write data to mapping address. Upon write completion, the EWR bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.

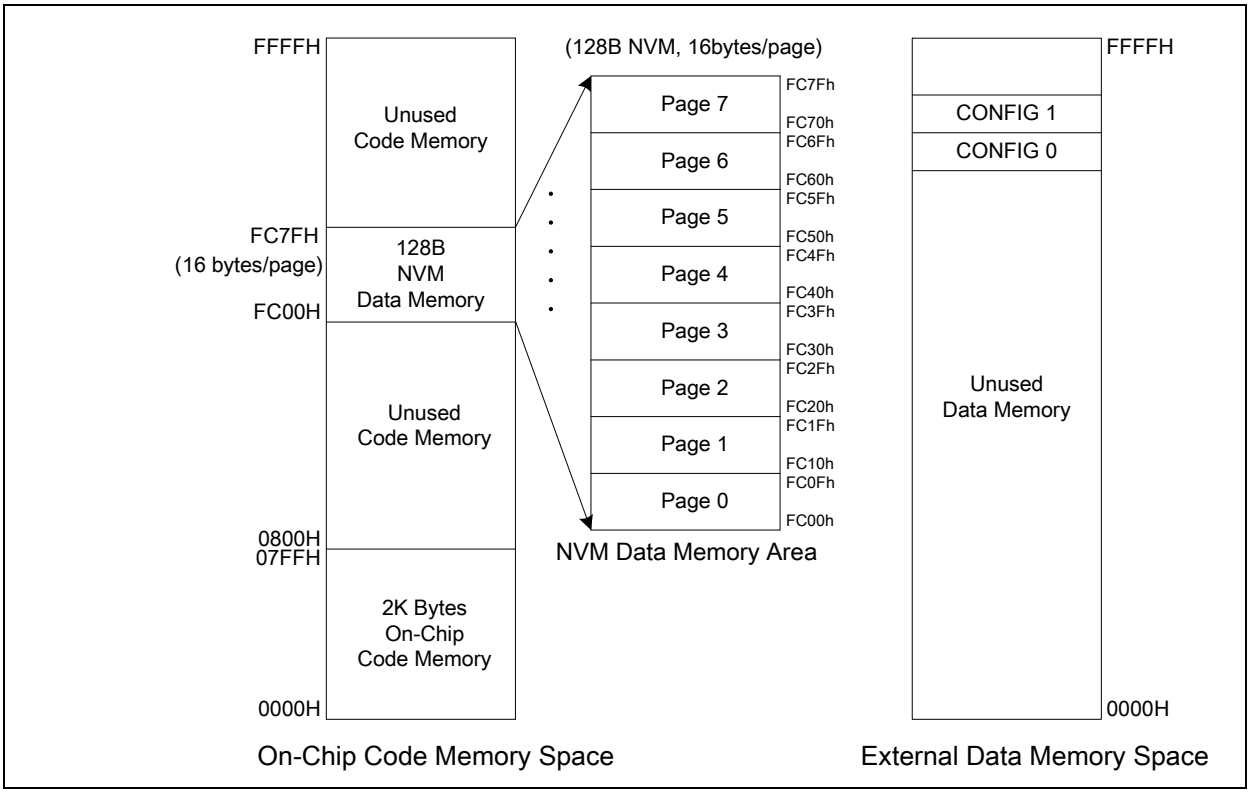


Figure 14-1: Memory map

15 WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

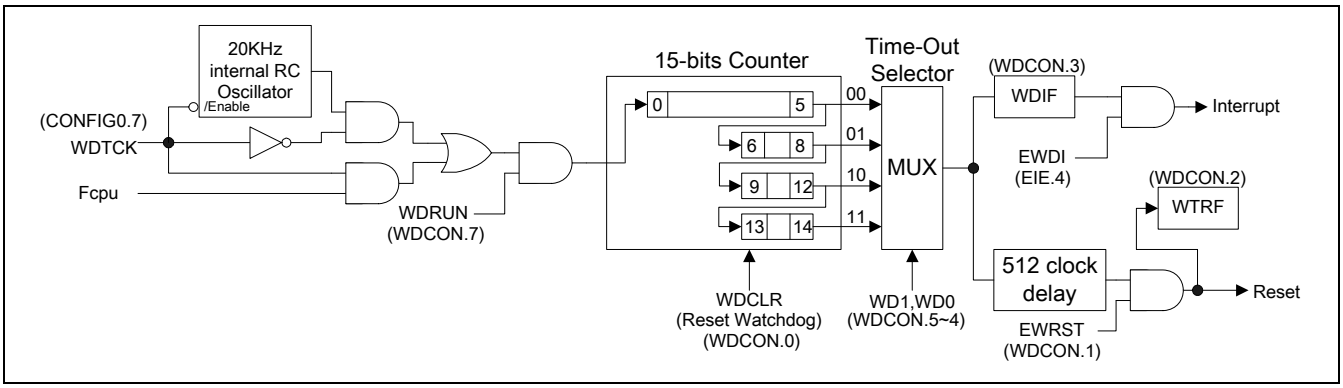


Figure 15-1: Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is

executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock speed. The reset, when enabled, will occur when 512 clocks after time-out has occurred.

WD1	WD0	Interrupt time-out	Reset time-out	Number of Clocks	Time @ 20 KHz
0	0	2^6	2^6 + 512	64	3.2 mS
0	1	2^9	2^9 + 512	512	25.6 mS
1	0	2^{13}	2^{13} + 512	8192	409.6 mS
1	1	2^{15}	2^{15} + 512	32768	1638.4 mS

Table 15-1: Time-out values for the Watchdog Timer

The Watchdog Timer will be disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state. The control bits that support the Watchdog Timer are discussed below.

15.1 WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWRST = 0, then this bit will not be affected by the Watchdog Timer.

EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

15.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^6 clocks, which is the shortest time-out period. The WDRUN, WD0, WD1, EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The WDTCK bit is located at bit 7 of CONFIG0 register. This bit is user to configure the clock source of watchdog timer either it is from the internal RC or from the uC clock.

When WDTCK bit is cleared and 20KHz clock is used to run the watchdog timer, there is a chance that

the watchdog timer would hang as the counter does not increment. This problem arises when the watchdog is set to run, (WDCON.7, WDRUN), the WDCLR bit (WDCON.0) is set to clear the watchdog timer and the next instruction is to set the PCON register for CPU to go into idle or power-down state. The reason this happens because the setting/clearing of WDCLR bit and the watchdog counter are running on different clock domains, CPU clock and internal RC clock respectively. When WDCLR bit is set, to reset it, the counter must be non-zero. Since the counter is running off a much slower clock, the counter may not have time to increment before the CPU clock halts as it entered the idle/power-down mode. This results in the WDCLR bit is always set & the watchdog counter remaining at zero. The solution to this problem is to monitor the WDCLR bit, ensuring that it's cleared before issue the instruction for the CPU to go into idle/power-down mode.

16 TIME ACCESS PROCTECTION

The N79E342 series have a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the N79E342 series have a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is;

```
TA      REG     0C7h            ; Define new register TA, @0C7h
        MOV     TA, #0AAh
        MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
        MOV     TA, #0AAh       ; 3 M/C Note: M/C = Machine Cycles
        MOV     TA, #055h       ; 3 M/C
        MOV     WDCON, #00h     ; 3 M/C
```

Example 2: Valid access

```
        MOV     TA, #0AAh       ; 3 M/C
        MOV     TA, #055h       ; 3 M/C
        NOP                     ; 1 M/C
        SETB    EWRST           ; 2 M/C
```

Example 3: Valid access

```
        MOV     TA, #0AAh       ; 3 M/C
        MOV     TA, #055h       ; 3 M/C
        ORL     WDCON, #00000010B ; 3M/C
```

Example 4: Invalid access

```
        MOV     TA, #0AAh       ; 3 M/C
        MOV     TA, #055h       ; 3 M/C
        NOP                     ; 1 M/C
        NOP                     ; 1 M/C
```

```
        CLR     EWT                     ; 2 M/C
Example 5: Invalid Access
        MOV     TA, #0AAh               ; 3 M/C
        NOP                             ; 1 M/C
        MOV     TA, #055h               ; 3 M/C
        SETB    EWT                     ; 2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

17 KEYBOARD INTERRUPT (KBI)

The N79E342 series are provided 5 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the N79E342 series, as shown below Figure. This interrupt may be used to wake up the CPU from Idle or Power Down modes, after chip is in Power Down or Idle Mode.

Keyboard function is supported through Port 0 (P0.3-P0.7). It can allow any or all supported pins of Port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits of KBI3 ~ KBI7 in the KBI register, as shown below Figure. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active, and the low pulse must be more than 1 machine cycle, an interrupt will be generated if it has been enabled. The KBF bit set by hardware and must be cleared by software. In order to determine which key was pressed, the KBI will allow the interrupt service routine to poll port 0.

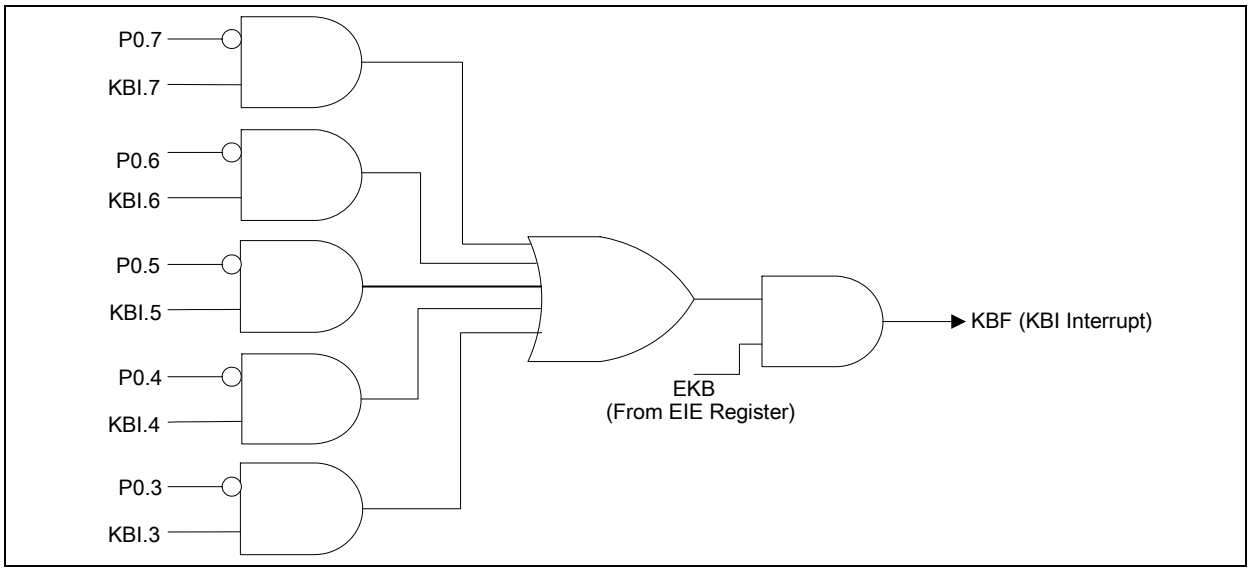


Figure 17-1: Keyboard Interrupt

18 I/O PORT CONFIGURATION

The N79E342 series have three I/O ports, port 0, port 1 and port 2. All pins of I/O ports can be configured to one of four types by software except P1.5 is only input pin. When P1.5 is configured reset pin by RPD=0 in the CONFIG 1 register, the N79E342 series can support 11 pins by use Crystal. If used on-chip RC oscillator the P1.5 is configured input pin, the N79E342 series can be supported up to 14 pins. The I/O ports configuration setting as below table.

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

Table 18-1: I/O port Configuration Table

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG0 register. During power-on-reset, all port pins will be tri-stated. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.5 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by T0OE and T1OE on P2M1 register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

Each I/O port of the N79E342 series may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P2M1 register, where n is 0, 1 or 2. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The P2.0 (XTAL2) can be configured clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

Note: During power-on-reset, all port pins will be tri-stated.

18.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports output are this mode, and output is common with the 8051. This mode can be used as both an input and output without the need to reconfigure the port.

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

The “weak” pull-up is turned on when the input port pin is logic “1” level or itself is logic “1”, and it provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

If port pin is low, it can drives large sink current for output, and it is similar with push-pull and open drain on sink current output.

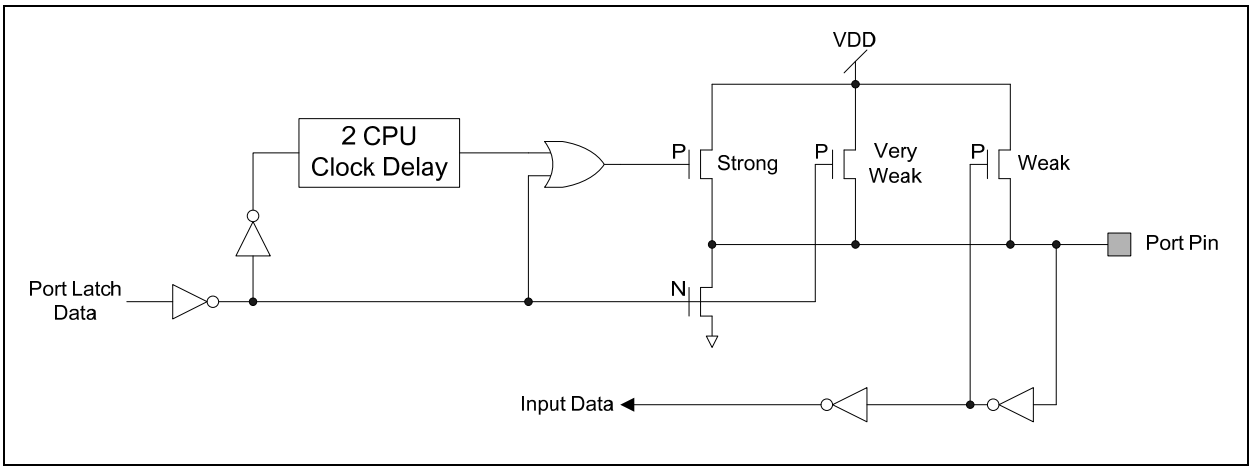


Figure 18-1: Quasi-Bidirectional Output

18.2 Open Drain Output Configuration

To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

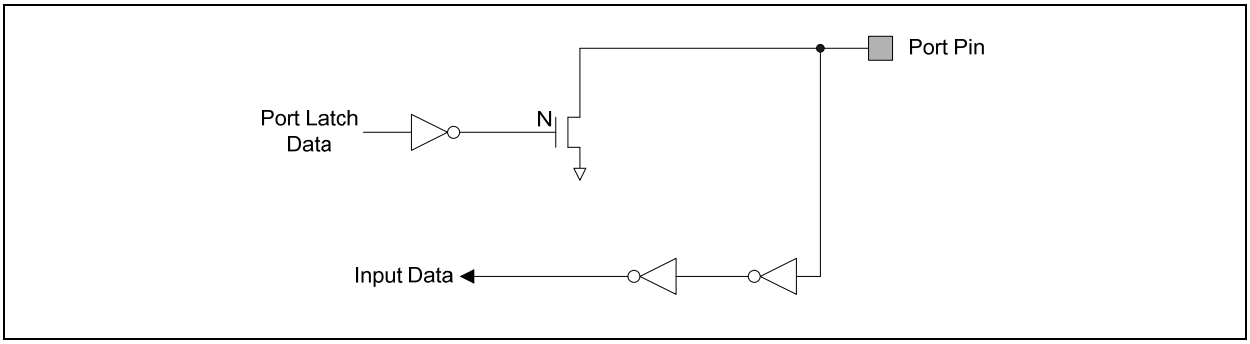


Figure 18-2: Open Drain Output

18.3 Push-Pull Output Configuration

The push-pull output mode has two strong pull-up and pull-down structure that support large source and sink current output. It removes “weak” pull-up and “very weak” pull-up resister and remain “strong pull-up resister on quasi-bidirectional output mode. The “strong” pull-up is always turns on when port latch is logic “1” to support source current. The push-pull port configuration is shown in below Figure.

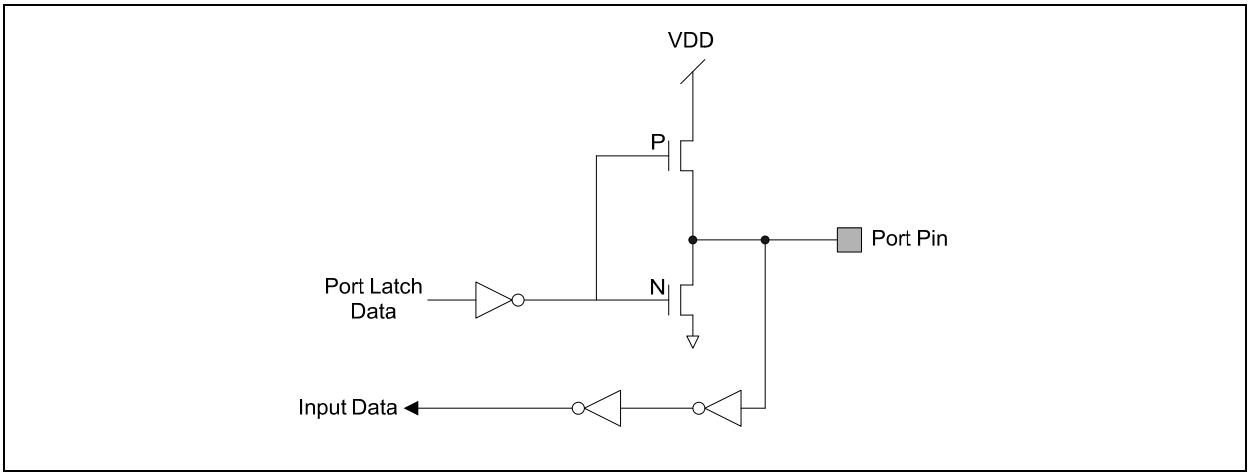


Figure 18-3: Push-Pull Output

18.4 Input Only Configuration

By configure this mode, the ports are only digital input and disable digital output. The N79E342 series can select input pin to Schmitt trigger or TTL level input by PxM1.y and PxM2.y registers.

19 OSCILLATOR

The N79E342 series provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported are 32KHz to 1MHz, and 4MHz to 12MHz, and without capacitor or resister.

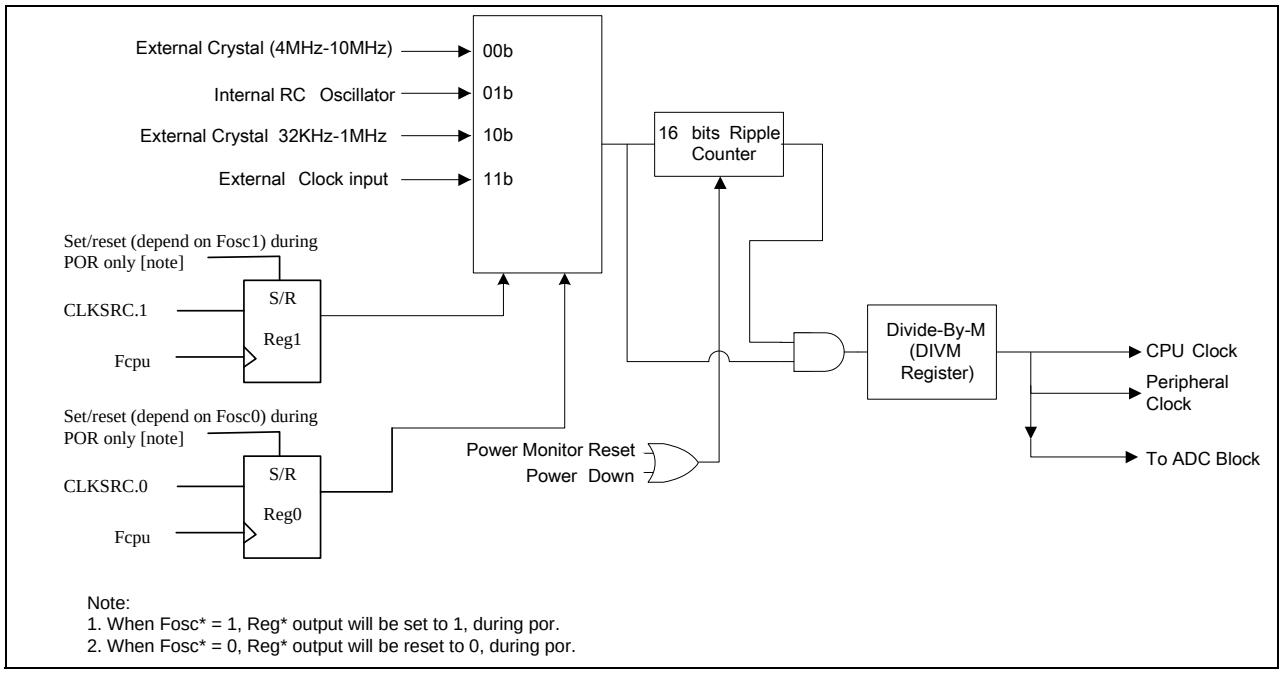


Figure 19-1: Oscillator

19.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is fixed at 455KHz +/- 2% frequency to support clock source. When FOSC1, FOSC0 = 01b, the On-Chip RC Oscillator is enabled. A clock output on P2.0 (XTAL2) may be enabled when On-Chip RC oscillator is used.

19.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is form 0Hz up to 12MHz. A clock output on P2.0 (XTAL2) may be enabled when External Clock Input is used.

The N79E342 series supports a clock output function when either the on-chip RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the N79E342 serial. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode, saving additional power. The clock output may also be enabled when the external clock input option is selected.

19.3 CPU Clock Rate select

The CPU clock of N79E342 series may be selected by the DIVM register. If DIVM = 00H, the CPU clock is running at 4 CPU clock pre machine cycle, and without any division from source clock (Fosc). When the DIVM register is set to N value, the CPU clock is divided by 2(DVIM+1), so CPU clock frequency division is from 4 to 512. The user may use this feature to set CPU at a lower speed rate for reducing power consumption. This is very similar to the situation when CPU has entered Idle mode. In addition this frequency division function affect all peripheral timings as they are all sourcing from the CPU clock(Fcpu).

19.4 Clock Source Control

The N79E342 series has added CKCON1 SFR that allows user application to control clock source above. The SFR consists of clock source selection bits (CLKSRC.1-0), where user can switch the clock source. For precaution reason, these SFR bits are TA protected. For information related to TA, please refer to section TIME ACCESS PROCTECTION.

With this clock source control, this device support clock switching from external rc to internal rc or internal rc to external rc by user application. However, for clock switching from internal rc to external rc, the device requires some amount of warm-up period for external rc to be stable. Duration of the warm-up period differs for different clock source conditions (see table below). During this warm-up period, the core clock is halted.

Clock Source	Warm-up period (due to power-on-reset and clock switching) [unit: clocks]
External Crystal (4MHz-12MHz)	65538
Internal RC (455KHz)	4
External Crystal (32KHz-1MHz)	4098
External Oscillator	258

Table 19-1: Warm-up period

20 BUZZER OUTPUT

The N79E342 series support square wave output capability. The square wave is output through P1.0 (BUZ) pin. The square wave can be enabled through bit BUZE (SFR AUXR1.1). Depending on Fcpu clock input to the buzzer output block, user is able to control the output frequency by configure the 8-bit Divider through BUZDIV bits in BUZCON SFR. The following shows the block diagram of square wave output generator.

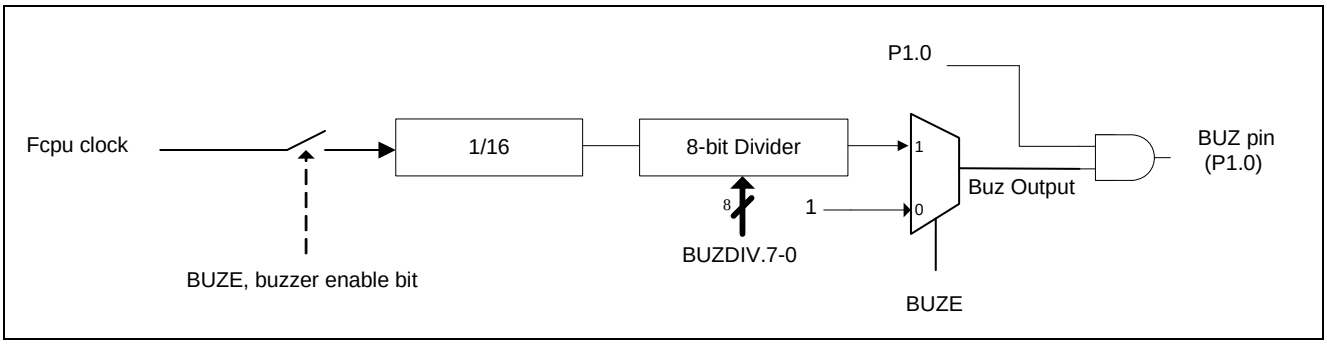


Figure 20-1: Square wave output

Buzzer output frequency equation:

Fbuz = Fcpu x 1/[16x(BUZDIV+1)]

The following table tabulates examples of the BUZDIV setting needed in order to generate buzzer output at rate close to 2KHz and 4KHz, for each cpu clock frequency.

		Frequency, Fcpu (Hz)			
	Division	455000	4000000	6000000	8000000
	/16	28437	250000	375000	5000000
BUZDIV + 1	1				
	.				
	4				
	5				
	6				
	7	4062.429			
	8				
	9				
	10				
	11				
	12				
	13				
	14	2031.214			
	15				
	16				
	17				
	18				
	19				
	64		3906.25		
	.				
	96			3906.25	
	.				
	128		1953.125		3906.25
	.				
	192			1953.125	
	256				1953.125

For supporting active low buzzer, this buzzer output is implemented with an off-state of high. The following pseudo code shows the operating procedure when working with active high and low buzzer;

(Assume PRHI=1):

1) During power on, P1.0/BUZ will be high;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low
                        ; at the top of s/w code to avoid initial beep sound.
<For active low buzzer>
No action needed.
```

2) To turn-on buzzer;

```
<For active high buzzer>
Set BUZE bit
Set SFR P1.0 bit        ; to push out the buzout.
<For active low buzzer>
Set BUZE bit
```

3) To turn-off buzzer;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low.
Clear BUZE bit
<For active low buzzer>
Set BUZE bit
```

21 POWER MONITORING FUNCTION

Power-On Detect and Brownout are two additional power monitoring functions implemented in N79E342 series to prevent incorrect operation during power up and power drop or loss.

21.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

21.2 Brownout Detect

The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. The N79E342 series have two brownout voltage levels to select by BOV (CONFIG0.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.

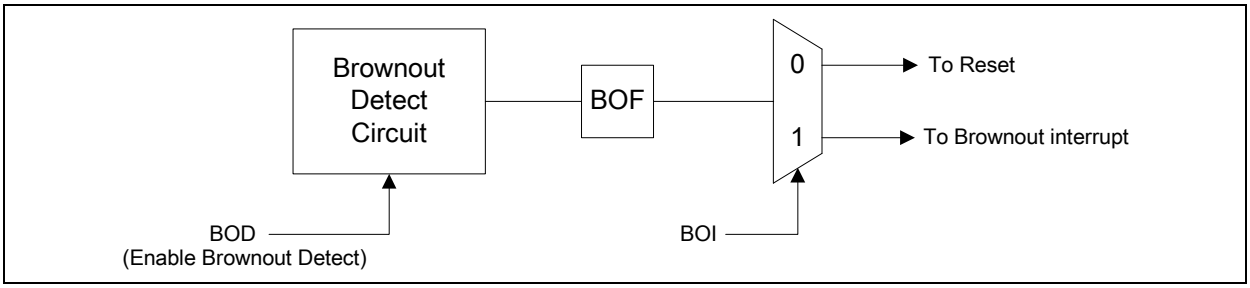


Figure 21-1: Brownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set and brownout reset will occur. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set. BOF is cleared by software.

In order to guarantee a correct detection of Brownout, The VDD fall time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.

22 ANALOG-TO-DIGITAL CONVERTER

The ADC contains a DAC which converts the contents of a successive approximation register to a voltage (VDAC) which is compared to the analog input voltage (Vin). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. A conversion is initiated by setting ADCS in the ADCCON register. There are two triggering methods by ADC to start conversion, either by purely software start or external pin STADC triggering.

The software start mode is used to trigger ADC conversion regardless of ADCCON.5 (ADCEX) bit is set or cleared. A conversion will start simply by setting the ADCCON.3 (ADCS) bit. As for the external STADC pin triggering mode, ADCCON.5 (ADCEX) bit has to be set and a rise edge pulse has to apply to STADC pin to trigger the ADC conversion. For the rising edge triggering method, a minimum of at least 2 machine cycles symmetrical pulse is required.

The low-to-high transition of STADC is recognized at the end of a machine cycle, and the conversion commences at the beginning of the next cycle. When a conversion is initiated by software, the conversion starts at the beginning of the machine cycle which follows the instruction that sets ADCS. ADCS is actually implemented with tpw flip-flops: a command flip-flop which is affected by set operations, and a status flag which is accessed during read operations.

The next two machine cycles are used to initiate the converter. At the end of the first cycle, the ADCS status flag is set end a value of “1” will be returned if the ADCS flag is read while the conversion is in progress. Sampling of the analog input commences at the end of the second cycle.

During the next eight machine cycles, the voltage at the previously selected pin of one of analog input pin is sampled, and this input voltage should be stable in order to obtain a useful sample. In any event, the input voltage slew rate must be less than 10V/ms in order to prevent an undefined result.

The successive approximation control logic first sets the most significant bit and clears all other bits in the successive approximation register (10 0000 0000b). The output of the DAC (50% full scale) is compared to the input voltage Vin. If the input voltage is greater than VDAC, then the bit remains set; otherwise if is cleared.

The successive approximation control logic now sets the next most significant bit (11 0000 0000b or 01 0000 0000b, depending on the previous result), and the VDAC is compared to Vin again. If the input voltage is greater then VDAC, then the bit remains set; otherwise it is cleared. This process is repeated until all ten bits have been tested, at which stage the result of the conversion is held in the successive approximation register. The conversion takes four machine cycles per bit.

The end of the 10-bit conversion is flagged by control bit ADCCON.4 (ADCI). The upper 8 bits of the result are held in special function register ADCH, and the two remaining bits are held in ADCCON.7 (ADC.1) and ADCCON.6 (ADC.0). The user may ignore the two least significant bits in ADCCON and use the ADC as an 8-bit converter (8 upper bits in ADCH). In any event, the total actual conversion time is 52 ADC clock cycles. ADCI will be set and the ADCS status flag will be reset 52 cycles after the ADCS is set. Control bits ADCCON.0 and ADCCON.1 are used to control an analog multiplexer which selects one of 4 analog channels. An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1; a new ADC conversion already in progress is aborted when the idle or power down mode is entered.

The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode.

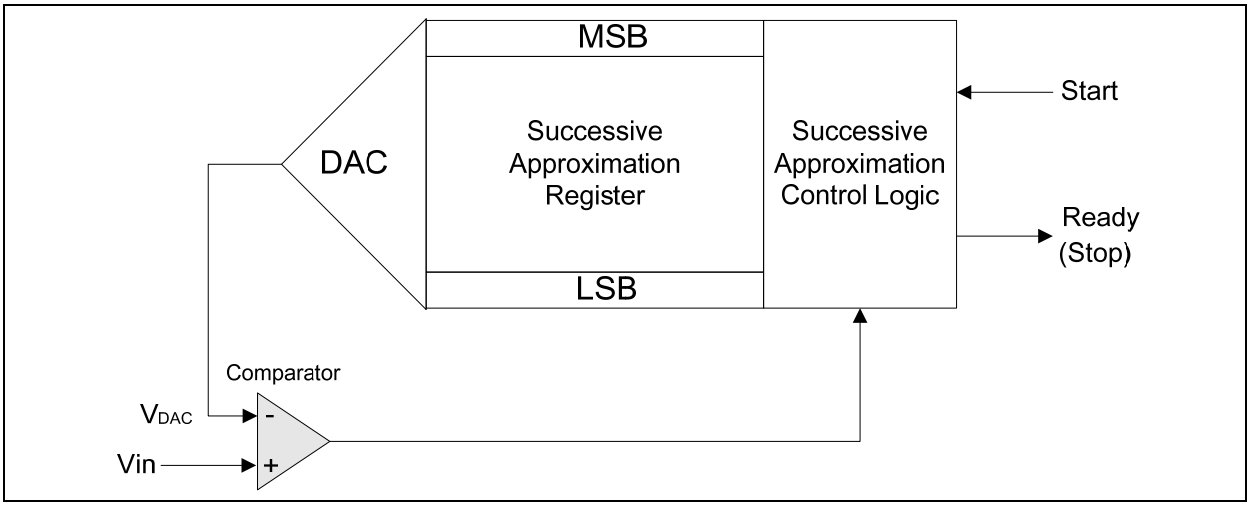


Figure 22-1: Successive Approximation ADC

22.1 ADC Resolution and Analog Supply:

The ADC circuit has its own supply pins (AVDD and AVSS) and one pins (Vref+) connected to each end of the DAC's resistance-ladder that the AVDD and Vref+ are connected to VDD and AVSS is connected to VSS. The ladder has 1023 equally spaced taps, separated by a resistance of "R". The first tap is located 0.5×R above AVSS, and the last tap is located 0.5×R below Vref+. This gives a total ladder resistance of 1024×R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between VSS and [(Vref+) + ½ LSB], the 10-bit result of an A/D conversion will be 0000000000B = 000H. For input voltages between [(Vref+) – 3/2 LSB] and Vref+, the result of a conversion will be 1111111111B = 3FFH. Vref+ and AVSS may be between AVDD + 0.2V and VSS – 0.2 V. Vref+ should be positive with respect to VSS, and the input voltage (Vin) should be between Vref+ and VSS.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{\text{Vin}}{\text{Vref}+} \quad \text{or Result} = 1024 \times \frac{\text{Vin}}{\text{VDD}}$$

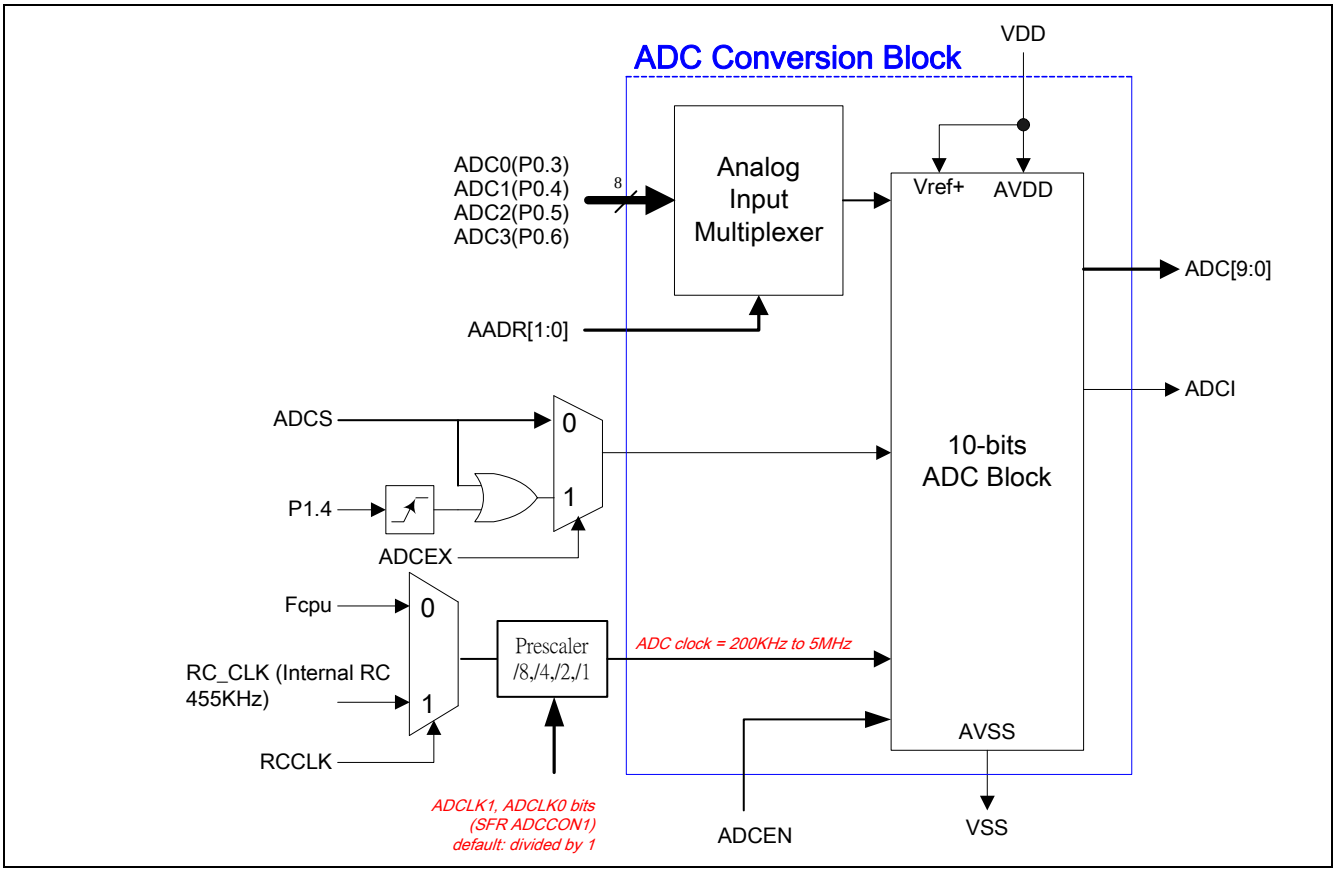
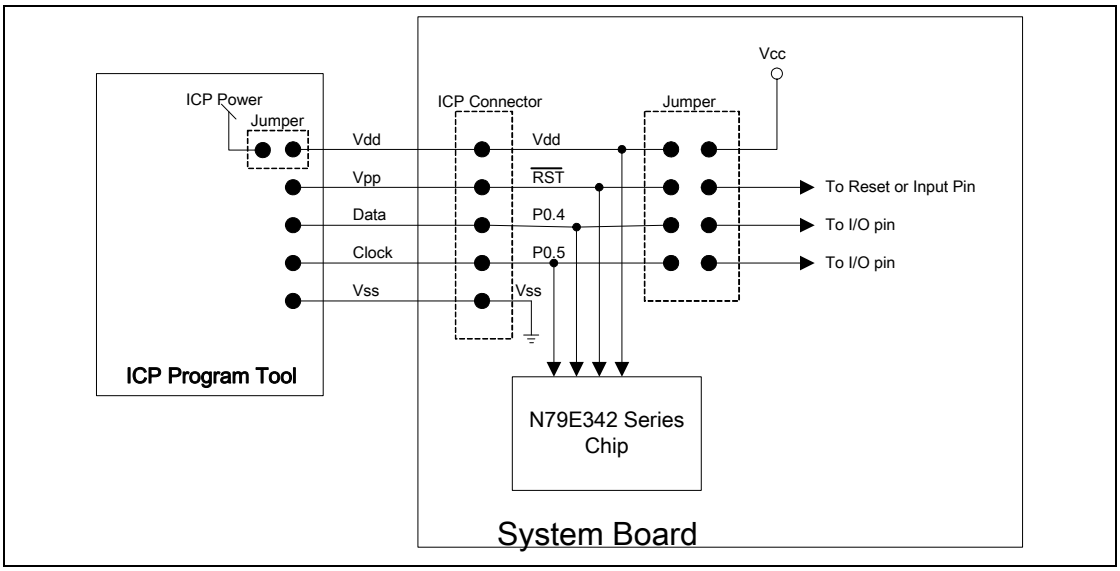


Figure 22-2: The ADC Block Diagram

23 ICP (IN-CIRCUIT PROGRAM) FLASH PROGRAM

The contexts of flash in N79E342 series are empty by default. At the first use, you must program the flash EPROM by external Writer device or by ICP (In-Circuit Program) tool.



Note:

1. When use ICP to upgrade code, the P1.5 (/RST), P0.4 and P0.5 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.
3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.

24 CONFIG BITS

The N79E342 has two CONFIG bits that must be defined at power up and can not be set the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below. The data of these bytes may be read by the MOVX instruction at the addresses.

24.1 CONFIG0

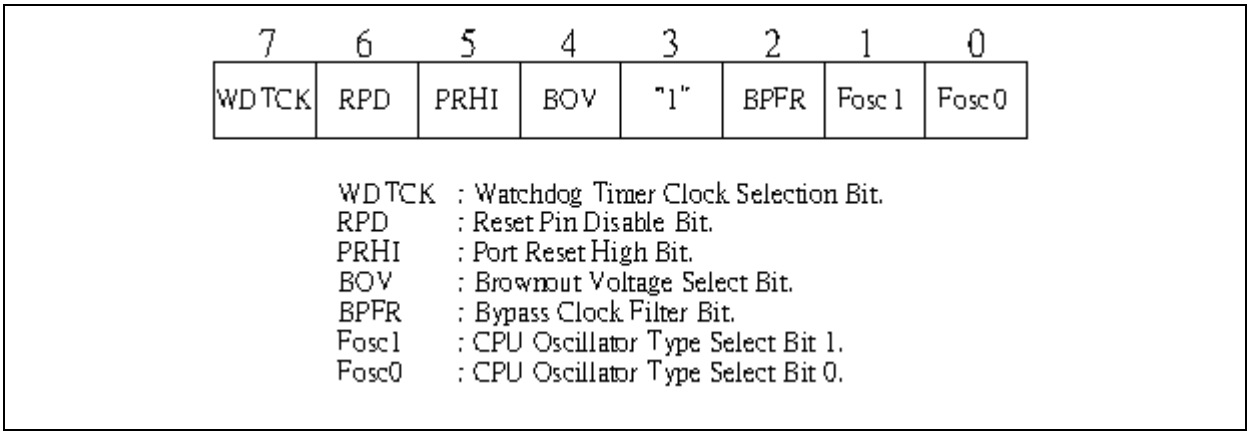


Figure 24-1: Config0 register bits

Bit	Name	Function
7	WDTCK	Watchdog Timer Clock Select bit: 0: The internal 20KHz RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.5. 1: Disable Reset function of Pin 1.5, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4	BOV	Brownout Voltage Select bit: 0: Brownout detect voltage is 3.8V. 1: Brownout detect voltage is 2.5V.
3	-	***Must be "1"***
2	BPFR	Bypass Clock Filter. 0: Disable Clock Filter. 1: Enable Clock Filter.

1	Fosc1	CPU Oscillator Type Select bit 1.
0	Fosc0	CPU Oscillator Type Select bit 0.

Oscillator Configuration bits:

Fosc1	Fosc0	OSC source
0	0	4MHz ~ 12MHz crystal
0	1	Internal 455KHz RC Oscillator
1	0	32KHz-1MHz crystal
1	1	External Oscillator in XTAL1

24.2 CONFIG1

7	6	5	4	3	2	1	0
C7	C6	"1"	"1"	"1"	"1"	"1"	"1"

Bit7: C7 : 2K byte Flash EPROM Code Lock Bit
Bit6: C6 : 128 byte NVM Data Lock Bit
Bit5~0: : Must be "1"

Figure 24-2: Config1 register bits

C7: 2K byte Flash EPROM Lock bit

This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.

C6: 128 byte NVM Data Lock bit

This bit is used to protect the customer's 128 bytes of data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the 128 bytes of Flash EPROM data and CONFIG Registers can not be accessed again.

Bit 7	Bit 6	Function Description
1	1	Both security of 2KB program code and 128 Bytes data area are not locked. They can be erased, programmed or read by Writer or ICP.
0	1	The 2KB program code area is locked. It can't be read by Writer or ICP. The 128 Bytes data area can be program or read. The bank erase is invalid.
1	0	Not supported.

0	0	Both security of 2KB program code and 128 Bytes data area are locked. They can't be read by Writer or ICP.

25 ELECTRICAL CHARACTERISTICS

25.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current suck by a I/O pin			25	mA
Maximum Current sourced by a I/O pin			25	mA
Maximum Current suck by total I/O pins			75	mA
Maximum Current sourced by total I/O pins			75	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

25.2 DC ELECTRICAL CHARACTERISTICS

(VDD–VSS = 2.4~5.5V, TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD1}	2.4	-	5.5	V	V_{DD}=3.0V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 6MHz
	V_{DD2}	3.0	-	5.5		NVM program and erase operation.
Operating Current (Internal RC 455KHz)	I_{DD1}	-	540	750	uA	No load, /RST = VDD, VDD = 5.0V, BOR disabled, RUN NOP
	I_{DD2}	-	170	230		No load, /RST = VDD, VDD = 3.3V, BOR disabled, RUN NOP
	I_{DD3}	-	90	120		No load, /RST = VDD, VDD = 2.4V, BOR disabled, RUN NOP
Operating Current (12MHz)	I_{DD4}	-	6.4	8.5	mA	No load, /RST = VDD, VDD = 5.0V, BOR disabled, RUN NOP
	I_{DD5}	-	3.3	4.2		No load, /RST = VDD, VDD = 3.3V, BOR disabled, RUN NOP
Idle Current (Internal RC 455KHz)	I_{IDLE1}	-	160	220	uA	No load, /RST = VDD, VDD = 5.0V, BOR disabled.
	I_{IDLE2}	-	80	110		No load, /RST = VDD, VDD = 3.3V, BOR disabled.
	I_{IDLE3}	-	42	55		No load, /RST = VDD, VDD = 2.4V, BOR disabled.
Idle Current (12MHz)	I_{IDLE4}	-	2.6	3.5	mA	No load, /RST = VDD, VDD = 5.0V, BOR disabled.
	I_{IDLE5}	-	1.4	1.8		No load, /RST = VDD, VDD = 3.3V, BOR disabled.
Power Down Current	I_{PWDN1}	-	1	10	uA	No load, V_{DD} = 5.5V @ Disable BOR function
	I_{PWDN2}	-	1	10	uA	No load, V_{DD} = 3.0V @ Disable BOR function
Input / Output						
Input Current P0, P1, P2	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current P1.5(RST pin)[*1]	I_{IN2}	-30	-45	-55	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P0, P1, P2 (Open Drain)	I_{LK}	-10	0.1	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2	I_{TL} [*2]	-200	-	-500	µA	V_{DD} = 5.5V, V_{IN}<2.0V
		-50	-	-100		V_{DD} = 2.4V, V_{IN}<1.3V
Input Low Voltage P0, P1, P2 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6		V_{DD} = 2.4V
Input High Voltage P0, P1, P2 (TTL input)	V_{IH1}	2.4	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =2.4V

Input Low Voltage XTAL1[*3]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*3]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	V_{DD} = 2.4V~5.5V
Positive going threshold (Schmitt input)	V_{IHS}	$0.7V_{DD}$	-	V_{DD}+0.5	V	V_{DD} = 2.4V~5.5V
Hysteresis voltage	V_{HY}	-	$0.2V_{DD}$	-	V	
Source Current P0, P1, P2 (PUSH-PULL Mode)	I_{SR1}	-12	-18	-	mA	V_{DD} = 4.5V, V_S = 2.4V
		-2	-4	-		V_{DD} =2.4V, V_S = 2.0V
Source Current P0, P1, P2 (Quasi-bidirectional Mode)	I_{SR2}	-150	-210	-360	μA	V_{DD} = 4.5V, V_S = 2.4V
		-20	-30	-50	μA	V_{DD} =2.4V, V_S = 2.0V
Sink Current P0, P1, P2 (Quasi-bidirectional and PUSH-PULL Mode)	I_{SK1}	12	18	-	mA	V_{DD} = 4.5V, V_S = 0.45V
		7	11	-	mA	V_{DD} = 2.4V, V_S = 0.45V
Brownout voltage with BOV=1	$V_{BO2.5}$	2.4	-	2.9	V	TA = -0 to 70°C
Brownout voltage with BOV=0	$V_{BO3.8}$	3.5	-	4.1	V	TA = -0 to 70°C
Brownout voltage detect current (BOR enable)	I_{BOD}	-	1.2	1.6	mA	V_{DD} = 5.0V
		-	1.0	1.3	mA	V_{DD} = 3.0V
ADC current (Additional power consumption if ADC converter is enabled)	I_{ADC}	-	500	800	uA	V_{DD} = 5.0V, ADCCLK =4MHz
		-	330	500	uA	V_{DD} = 3.3V, ADCCLK =4MHz
		-	350	600	uA	V_{DD} = 5.0V, ADCCLK =455KHz
		-	250	400	uA	V_{DD} = 3.3V, ADCCLK =455KHz

*1. /RST pin is a Schmitt trigger input.

*2. Pins of P0, P1 and P2 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V (V_{DD}=5.5V) or 1.3V (V_{DD}=2.4V).

*3. XTAL1 is a CMOS input.

25.3 The ADC Converter DC ELECTRICAL CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fosc = 4MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Analog input	AVin	V_{SS}-0.2		V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz	-	5MHz	Hz	ADC block circuit input clock
Conversion time	t_C		$52t_{ADC}$[1]		us	
Differential non-linearity	DNL	-1	-	+1	LSB	
Integral non-linearity	INL	-2	-	+2	LSB	
Offset error	Ofe	-1	-	+2	LSB	
Gain error	Ge	-1	-	+1	%	
Absolute voltage error	Ae	-3	-	+3	LSB	

Notes:

1. tADC: The period time of ADC input clock.

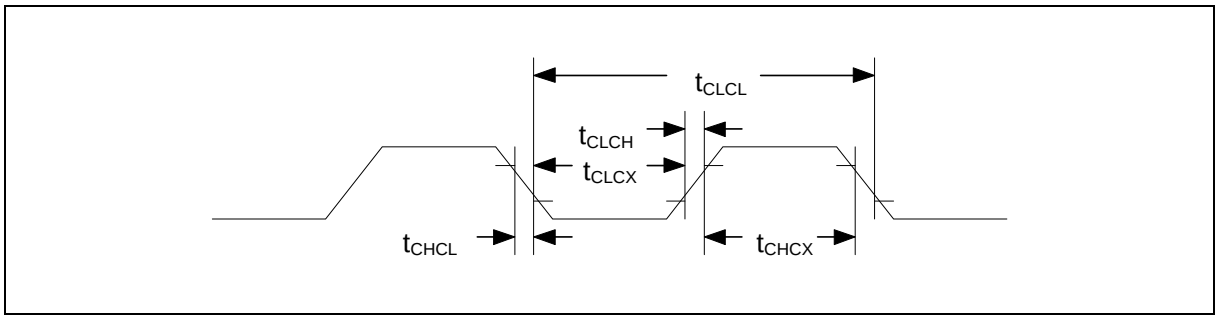
25.4 INTERNAL RC OSC DC ELECTRICAL CHARACTERISTICS

Parameter	Specification				Test Conditions
	Min.	Typ.	Max.	Unit	
N79E342 Frequency accuracy of On-chip 455KHz RC oscillator (Without calibration)	-	±30%	-	%	V_{DD}=3.3V, TA = 25°C
N79E342R On-chip 455KHz RC oscillator with calibration[1] (with factory calibration)	-2	-	2	%	V_{DD}=3.3V, TA = 25°C
	-5	-	5	%	V_{DD}=2.4V~5.5V, TA = 0~50°C
	-5		9	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-9		9	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-11	-	9	%	V_{DD}=2.7V~5.5V, TA = -40~85°C

Note:

1. These values are for design guidance only and are not tested.

25.5 AC ELECTRICAL CHARACTERISTICS



Note: Duty cycle is 50%.

25.6 EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	30	-	-	nS	
Clock Low Time	t_{CLCX}	30	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

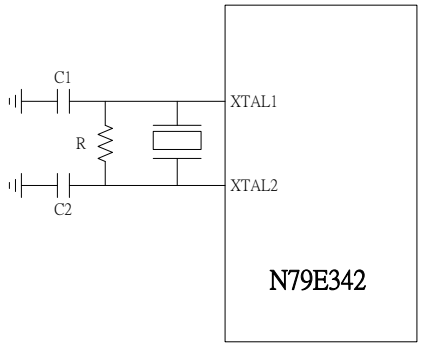
25.7 AC SPECIFICATION

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	12	MHz

25.8 TYPICAL APPLICATION CIRCUITS

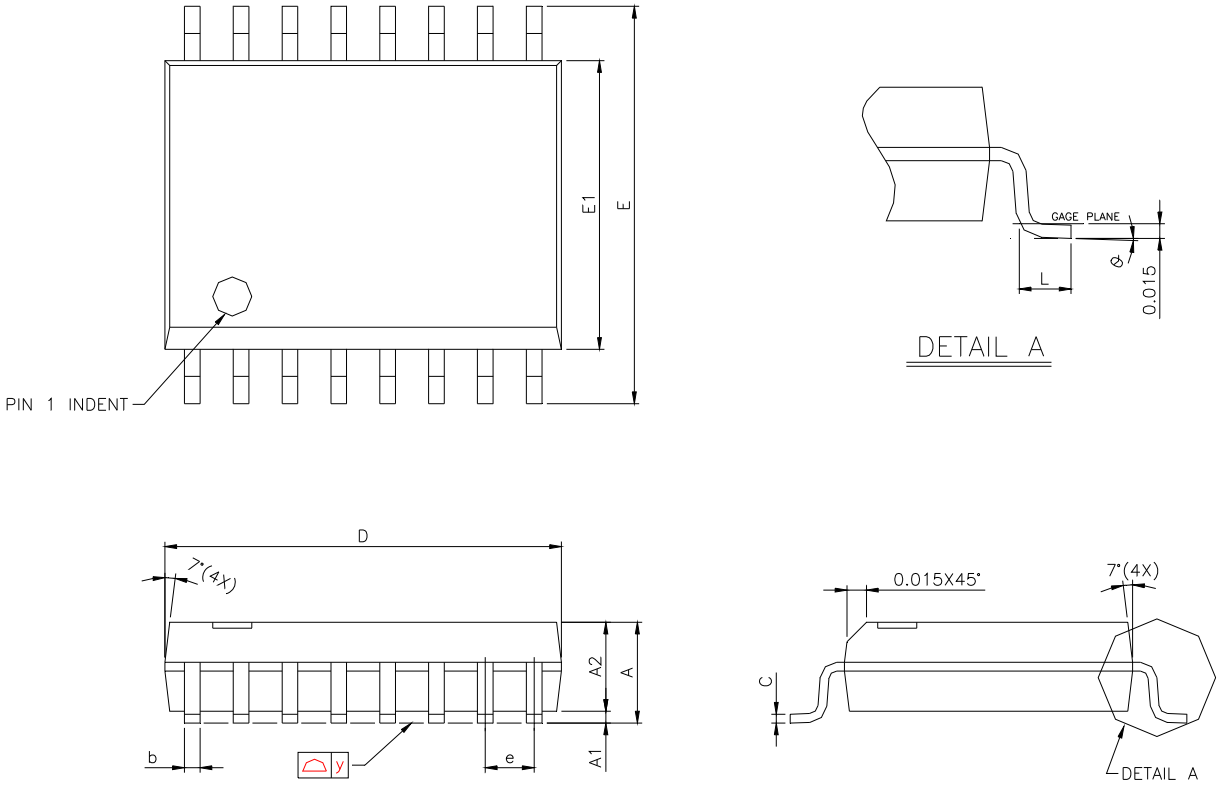
CRYSTAL	CONFIG0.FOSC1	CONFIG0.FOSC0	C1	C2	R
4MHz ~ 12MHz	0	0	without	without	without
1MHz	1	0	without	without	without
455KHz	1	0	without	without	without
32.768KHz	1	0	150pF	150pF	without

The above table shows the reference values for crystal applications.



26 PACKAGE DIMENSIONS

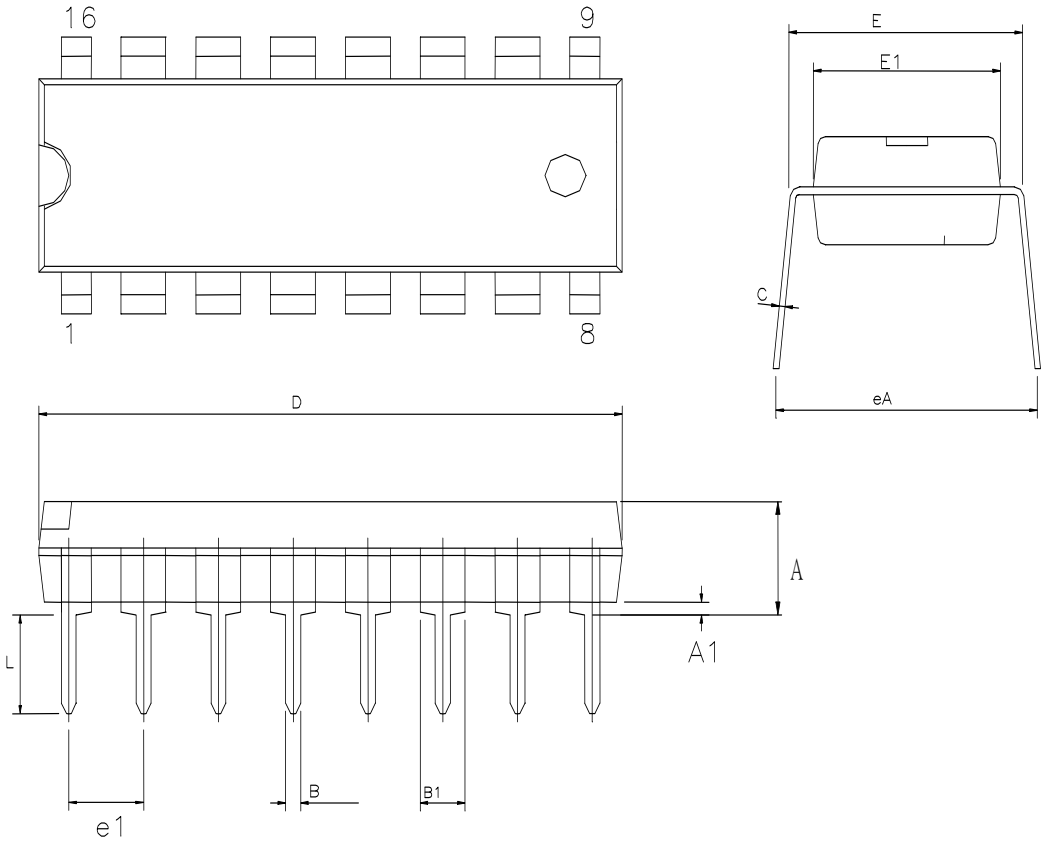
26.1 16-pin SOP



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	——	0.30	0.004	——	0.012
A2	——	2.31	——	——	0.091	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	——	1.27	——	——	0.050	——
L	0.38	0.81	1.27	0.015	0.032	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

Figure 26-1: 16-pin SOP 300mil

26.2 16-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	–	–	0.210	–	–	0.5334
A1	0.015	–	–	0.381	–	–
B	0.016	0.018	0.020	0.406	0.457	0.508
B1	0.055	0.060	0.065	1.397	1.524	1.651
c	–	0.010	–	–	0.25	–
D	0.740	0.750	0.760	18.796	19.05	19.304
E	0.300	0.312	0.324	7.62	7.925	8.230
E1	0.246	0.250	0.254	6.25	6.35	6.45
e1	0.1BSC			2.54BSC		
L	0.115	–	–	2.921	–	–
eA	0.330	0.350	0.370	8.382	8.89	9.398

Figure 26-2: 16-pin DIP 300mil

27 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	September 19, 2008	-	Initial Issued
A2	Dec 21, 2009	79 80	Add defaule value for the reserved bit of CONFIG0 Add defaule value for the reserved bit of CONFIG1

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