MX10FMAXD

SINGLE-CHIP 8-BIT MICROCONTROLLER

FEATURE

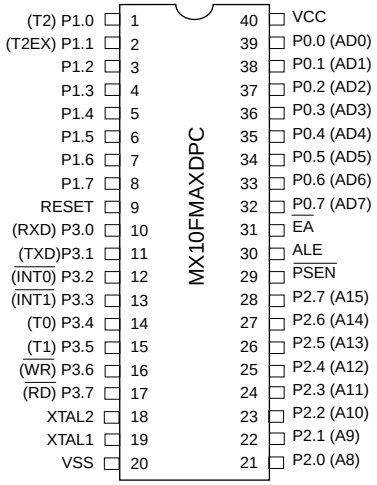
- High performance CMOS MTP ROM CPU
- Operation Voltage 5V
- Up to 40MHz operation (3.5MHz to 40MHz)
- Three 16-bit timer/counters
- 256 Bytes of on-chip data RAM
- 64 Kbytes on-chip Flash memory
- 32 Programmable I/O lines
- 6 interrupt Sources
- Code protection
- Two priority levels
- Power saving Idle and power down modes
- 64 K external program memory space
- 64 K external data memory space
- Four 8-bit I/O ports
- Full-duplex enhanced UART compatible with the standard 80C51 and the 80C52
- MX10FMAXDPC(PDIP)
- MX10FMAXDQC(PLCC)
- MX10FMAXDFC(PQFP)

GENERAL DESCRIPTION

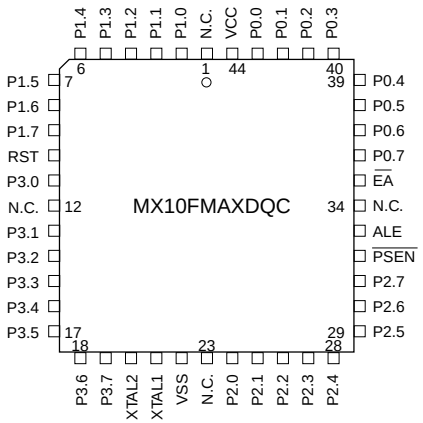
The single-chip 8-bit microcontroller is manufactured in MXIC's advanced CMOS process. This device uses the same powerful instruction set, has the same architecture, and is pin-to-pin compatible with the existing 80C51. The added features make it an even more powerful microcontroller for applications that require clock output, and up/down counting capabilities such as motor control. It also has a more versatile serial channel that facilitates multi-processor communications.

PIN CONFIGURATIONS

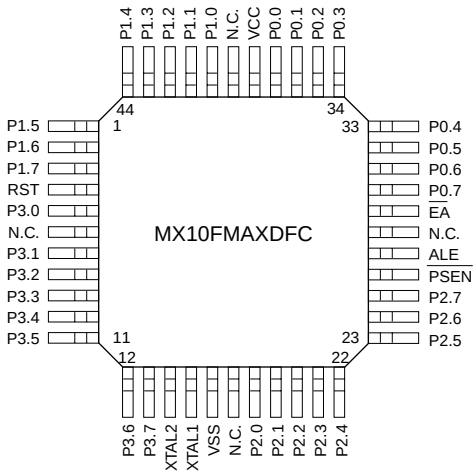
40 PDIP



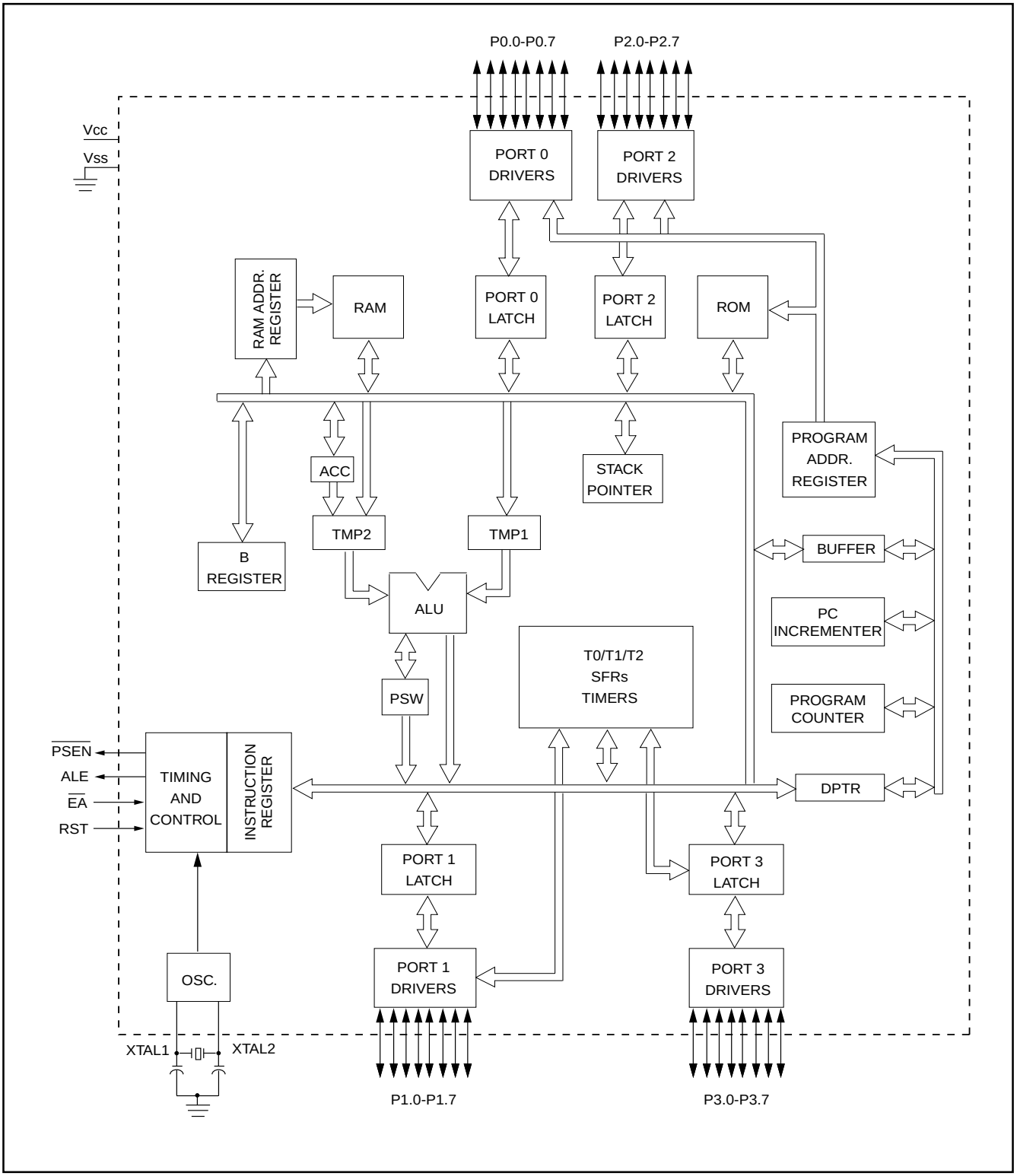
44 PLCC



44 PQFP



BLOCK DIAGRAM



PROCESS INFORMATION

This device is manufactured on a MXIC CMOS process.

PIN DESCRIPTIONS

VCC : Supply voltage.

VSS : Circuit ground.

Port 0 : Port 0 is an 8-bit, open drain, bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's, and can source and sink serveral LS TTL inputs.

Port 1 : Port 1 is an 8-bit bidirectional I/O port with internal pullups. The port 1 output buffers can drive LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (IIL, on the data sheet) because of the internal pullups.

In additional, Port 1 serves the functions of the following special features of the MX10FMAXD :

Port Pin	Alternate Function
P1.0	T2 (External Count Input to Timer/ Counter 2), Clock-Out
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger and Direction Control)

Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pullups. The port 2 output buffers can drive LS TTL inputs. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3 : Port 3 is an 8-bit bidirectional I/O port with internal pullups. The port 3 output buffers can drive LS TTL inputs. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 3 also serves the function of various special features of the 8051 Family, as listed below :

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	WR (external data memory write sttobe)
P3.7	RD (external data memory read strobe)

RST : Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum VIHI voltage is applied whether the oscillator is running or not. An internal pulldown resistor permits a power-on reset with only a capacitor connected to VCC.

ALE : Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 5 of SFR location 87H (PCON). With this bit set, the pin is weakly pulled high. However, the ALE disable feature will be suspended during a MOVX or MOVC instruction, idle mode, power down mode. The ALE disable feature will be terminated by reset. When the ALE disable feature is suspended or terminated, the ALE pin will no longer be pulled up weakly. Setting the ALE-disable bit has no affect if the micrcontroller is in external execution mode.

Throughout the remainder of this data sheet, ALE will refer to the signal coming out of the ALE pin, and the pin will be referred to as the ALE pin.

$\overline{PSEN}$: Program Store Enable is the read strobe to external Program Memory.

When the MX10FMAXD is executing code from external Program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data memory.

$\overline{EA}$/VPP : Extrernal Access enable. EA must be strapped to VSS in order to enable the twiceto fetch code from external Program Memory locations 0000H to 0FFFFH. $\overline{EA}$ will be internally latched on reset.

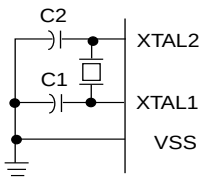
$\overline{EA}$ should be strapped to VCC for internal program executions.

XTAL1 : Input to the inverting oscillator amplifier.

XTAL2 : Output from the inverting oscillator amplifier.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of a inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used.



C1, C2 = 30 pF is equal to or less than 10 pF for Crystal
For Ceramic Resonators,contact resonator manufacture.

Figure 3. Oscillator Connections

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 floats, as shown in Figure 4. There are no requirememts on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifer and its feedback capacitance. Once the external signal meets the VIL and VIH specifications the capacitance will not exceed 20 pF.

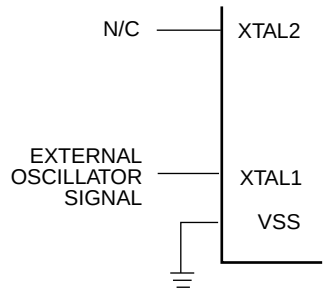


Figure 4. External Clock Drive Configuration

IDLE MODE

The user's software can invoke the Idle Mode. When the microcontroller is in this mode, power consumption is reduced. The Special Function Registers and the onboard RAM retain their values during Idle, but the processor stops executing instructions. Idle Mode will be exited if the chip is reset or if an enabled interrupt occurs.

ABSOLUTE MAXIMUM RATING*

Ambient Temperature Under Bias	0℃ to 70℃
Storage Temperature	-65℃ to +150℃
Voltage on Any Other Pin to VSS	-0.5V to +6.5V
IOL Per I/O Pin	15mA
Power Dissipation	1.5W

(Based on PACKAGE heat transfer limitations, not device consumption)

Table 2. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

POWER DOWN MODE

To save even more power, a Power Down mode can be invoked by software. If this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

On the MX10FMAXD either a hardware reset or an external interrupt can cause an exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and on-chip RAM to retain their values.

To properly terminate Power Down, the reset or external interrupt should not be executed before VCC is restored to its normal operating level, and must be held active long enough for the oscillator to restart and stabilize (normally less than 10 ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Program Memory

MX10FMAXD internal program can be protected by 3 Program Lock Bits. The following table is the meaning for 3 protection levels:

Table 3 3 level ROM code protection

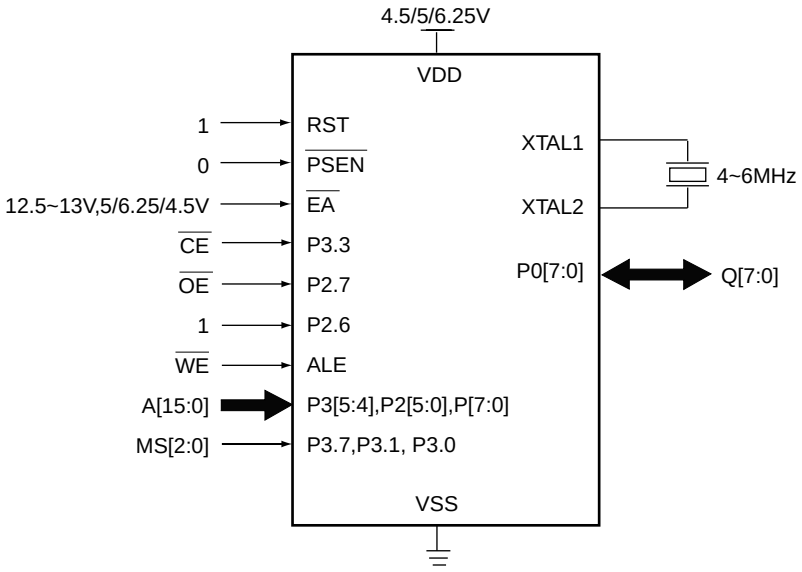
LEVEL	LOCK1	LOCK2	LOCK3	PROTECTION DESCRIPTION
0	U	U	U	No Program Lock feature enabled
1	P	U	U	extrnal MOVC is disabled
2	P	P	U	Same as 1, plus normal read, program-verify and erase-verify are all disabled
3	P	P	P	Same as 2, plus all instructions will be fetched only from internal ROM

Note
1. Program Lock Bits can be reset only by chip erase operation

5. PROGRAMMING SPECIFICATION

5.1 Parallel Programming Mode

The Following is the setting for parallel programming mode.



PIN NAME	SYMBOL	FUNCTION
P1.0 ~ P1.7	A0 ~A7	Input low order address bits
P2.0 ~ P2.5, P3.4 ~ P3.5	A8 ~ A13, A14 ~A15	Input high order address bits
P0.0 ~ P0.7	Q0 ~ Q7	Data Input/Output
P3.3	$\overline{CE}$	Chip Enable Input
P2.7	$\overline{OE}$	Output Enable Input
ALE	$\overline{WE}$	Write Enable Input
$\overline{EA}$	Vpp	Program Supply Voltage, 12.5 ~13Volts
P3.7, P3.1, P3.0	MS2 ~ MS0	Flash Mode Selection
VDD	VDD	Power Supply Voltage (+5V)
GND	GND	Ground Pin

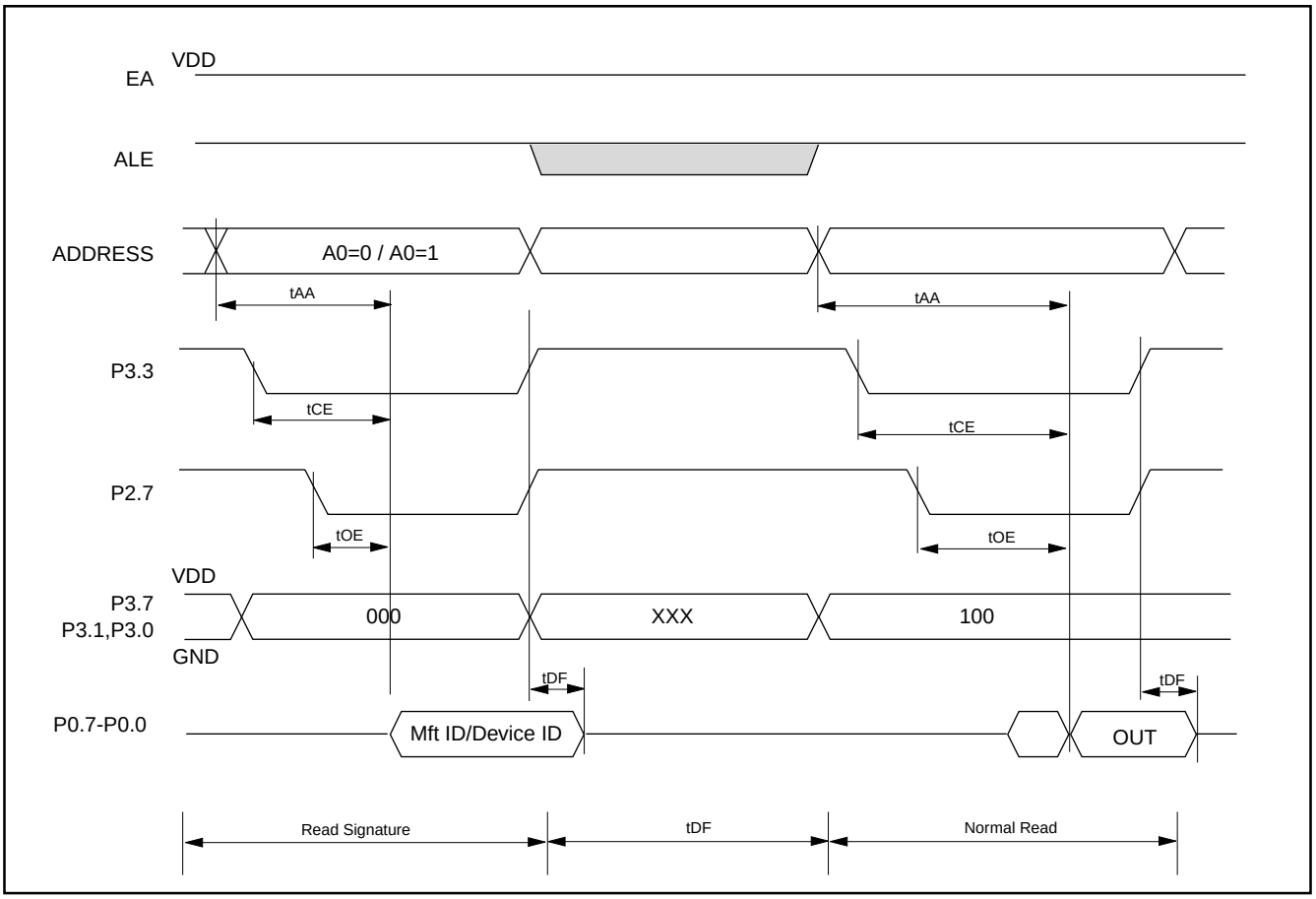
Notice for speed progamming

5.1.1 Table of parallel programming modes

External Pin	EA	VDD	P3.3	P2.7	ALE	P3[5:4], P2[5:0], P1[7:0]	P3.7, P3.1, P3.0	P0[7:0]
Standby	X	5V	1	X	X	X	X	Z
Read Signature	5V	5V	0	0	1	P1.0=0 P1.0=1	000	MftID=C2H DID=F0H
Program	12.5~13V	6.25V	0	1	100us pulses	address	011	DATA
Program Verify	12.5~13V	6.25V	0	0	1	address	010	DATA
Pgm Lock bit #1	12.5~13V	6.25V	0	1	100us pulses	X	111	X
Pgm Lock bit #2	12.5~13V	6.25V	0	1	100us pulses	X	110	X
Pgm Lock bit #3	12.5~13V	6.25V	0	1	100us pulses	X	100	X
Pgm verify Lock bits	6.25V	6.25V	0	0	1	X	101	P0[3:1]= LOCK[3:1]
Erase verify LOCK bits	4.5V	4.5V	0	0	1	X	101	P0[3:1]= LOCK[3:1]
Chip Erase	12.5~13V	6.25V	0	1	0.5sec pulse	X	010	X
Erase Verify	12.5~13V	4.5V	0	0	1	address	011	DATA
Normal Read	**X**	5V	0	0	1	address	100	DATA

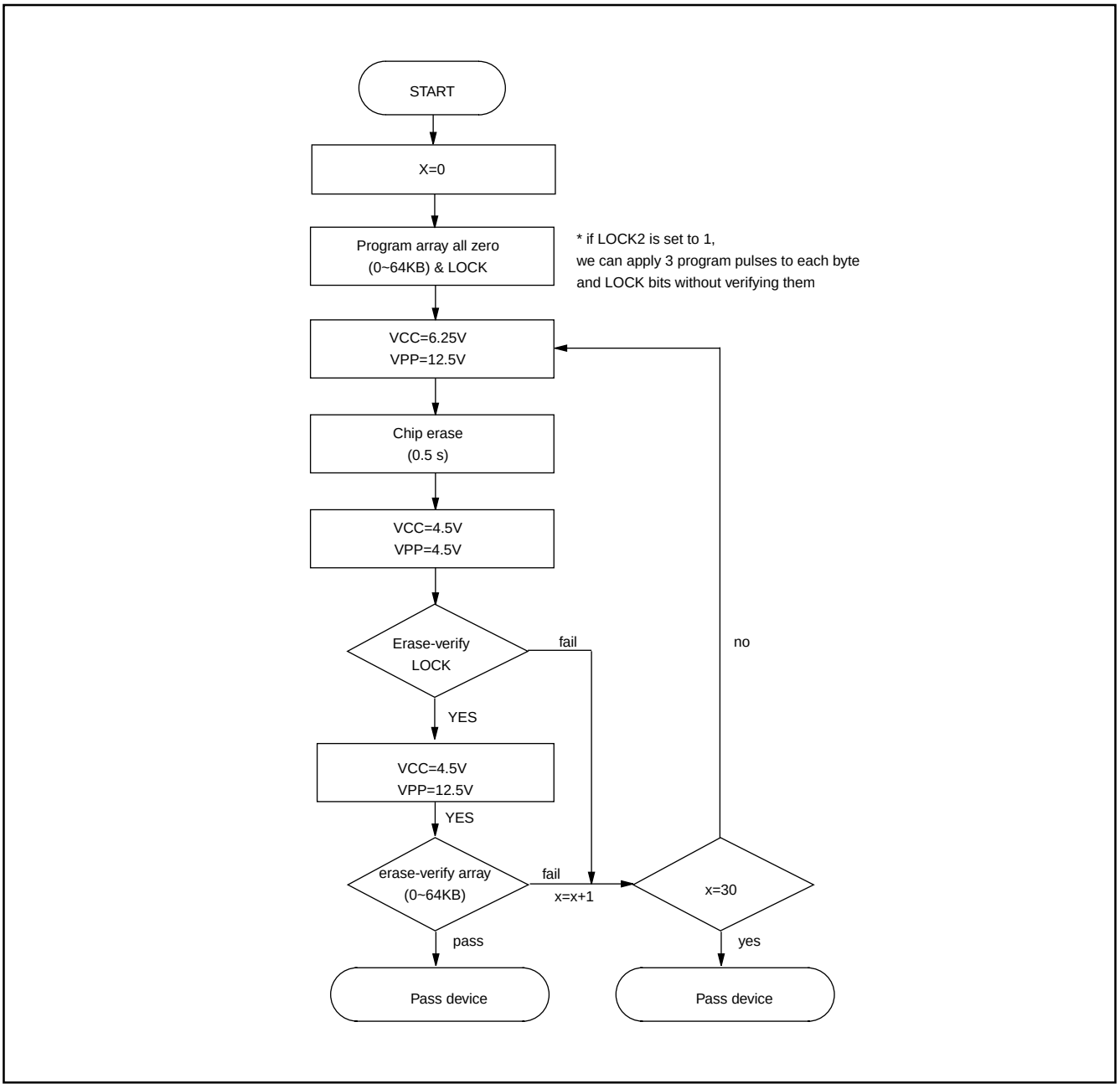
5.1.2 Timing Waveform in Parallel Programming Mode

READ SIGNATURE AND NORMAL READ WAVEFORM

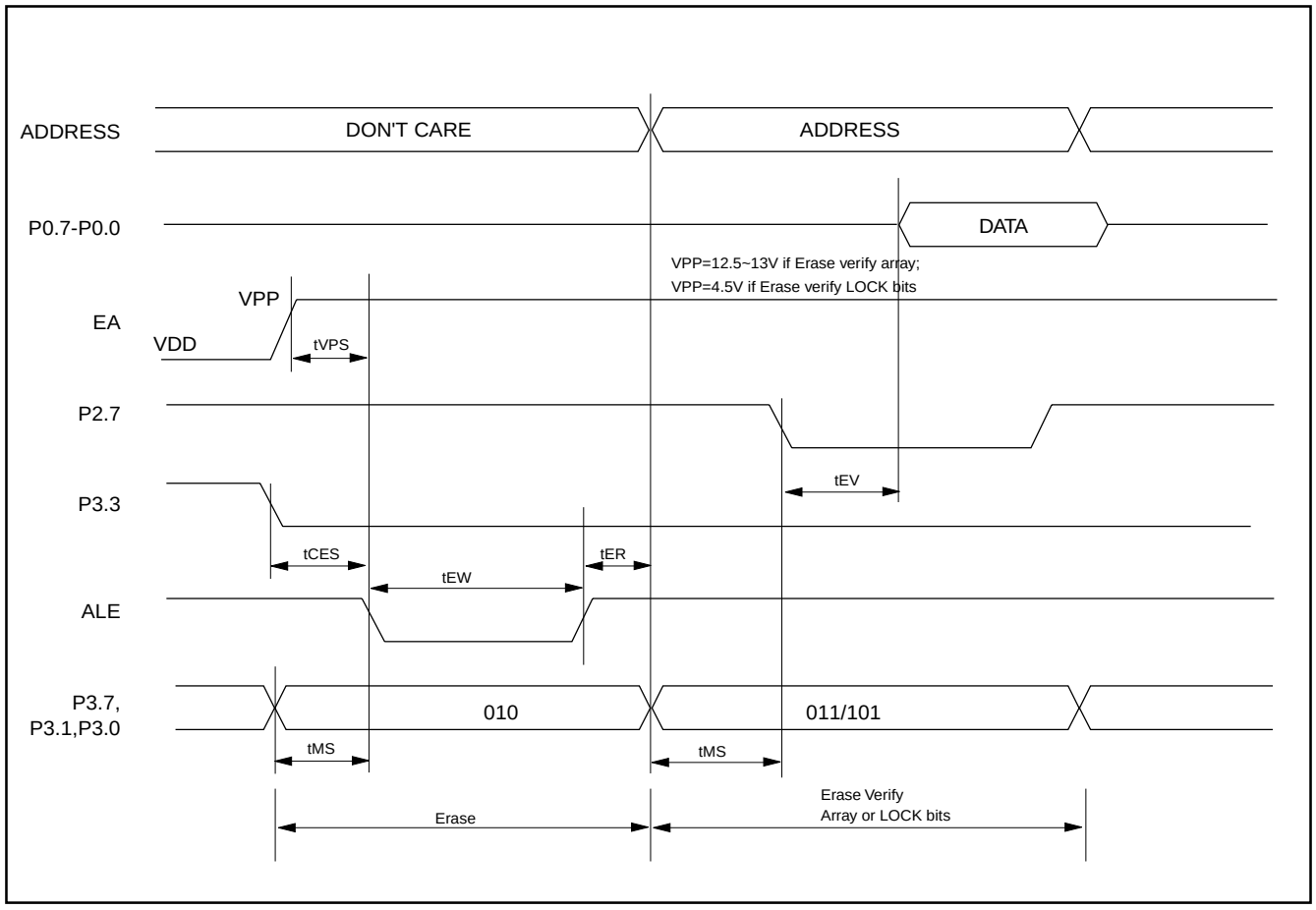


	tAA	tCE	tOE	tDF
Mim.				0
Max.	120	120	70	20
unit	ns	ns	ns	ns

ERASE AND VERIFY FLOWCHART

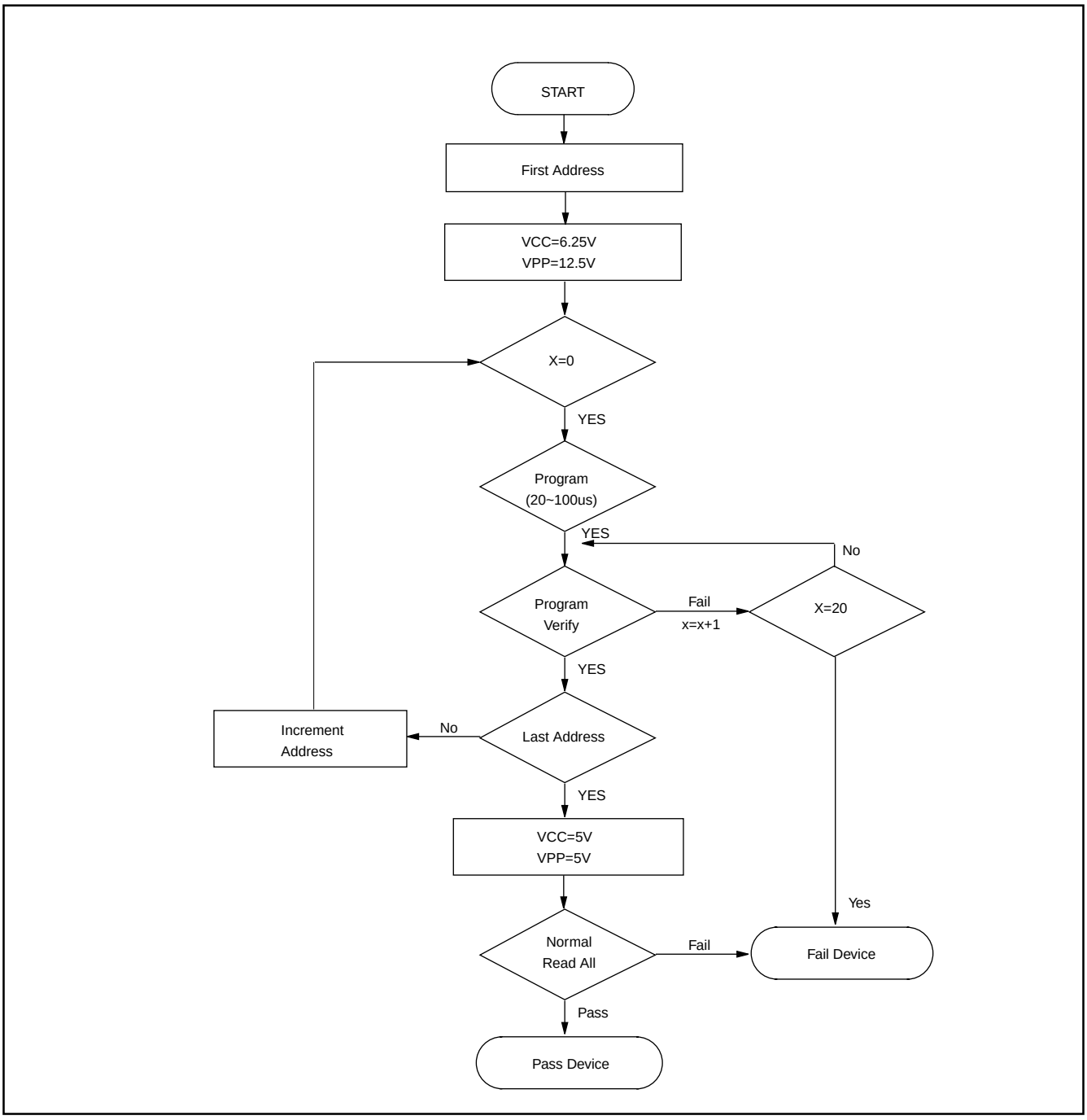


ERASE AND ERASE VERIFY WAVEFORM

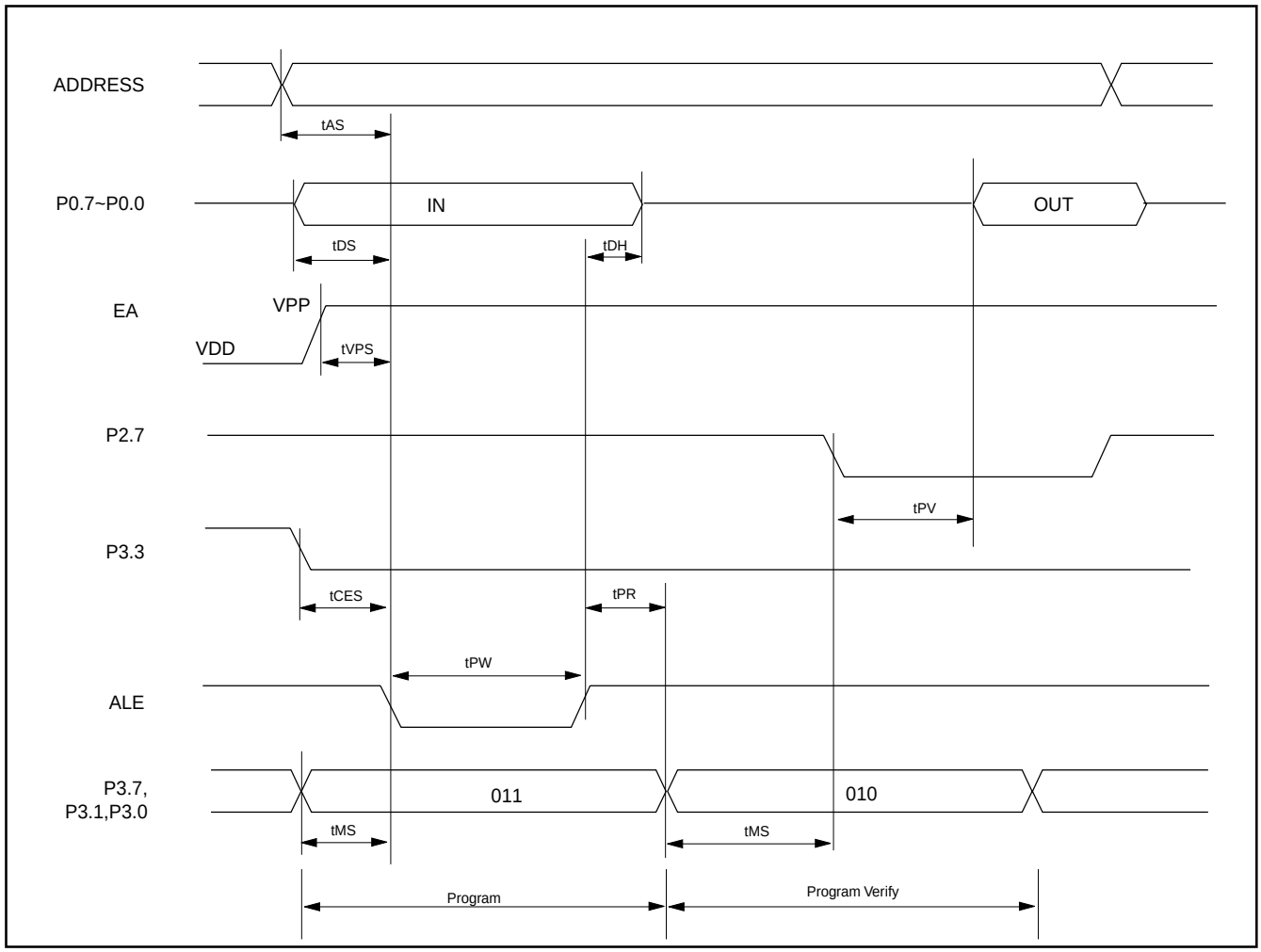


	tDS	tDH	tVPS	tMS	tCES	tER	tEW	tEV
Mim.	2	2	2	2	2	0.5	0.45	
Max.							0.55	240
unit	us	us	us	us	us	s	s	ns

PROGRAM AND PROGRAM VERIFY FLOWCHART

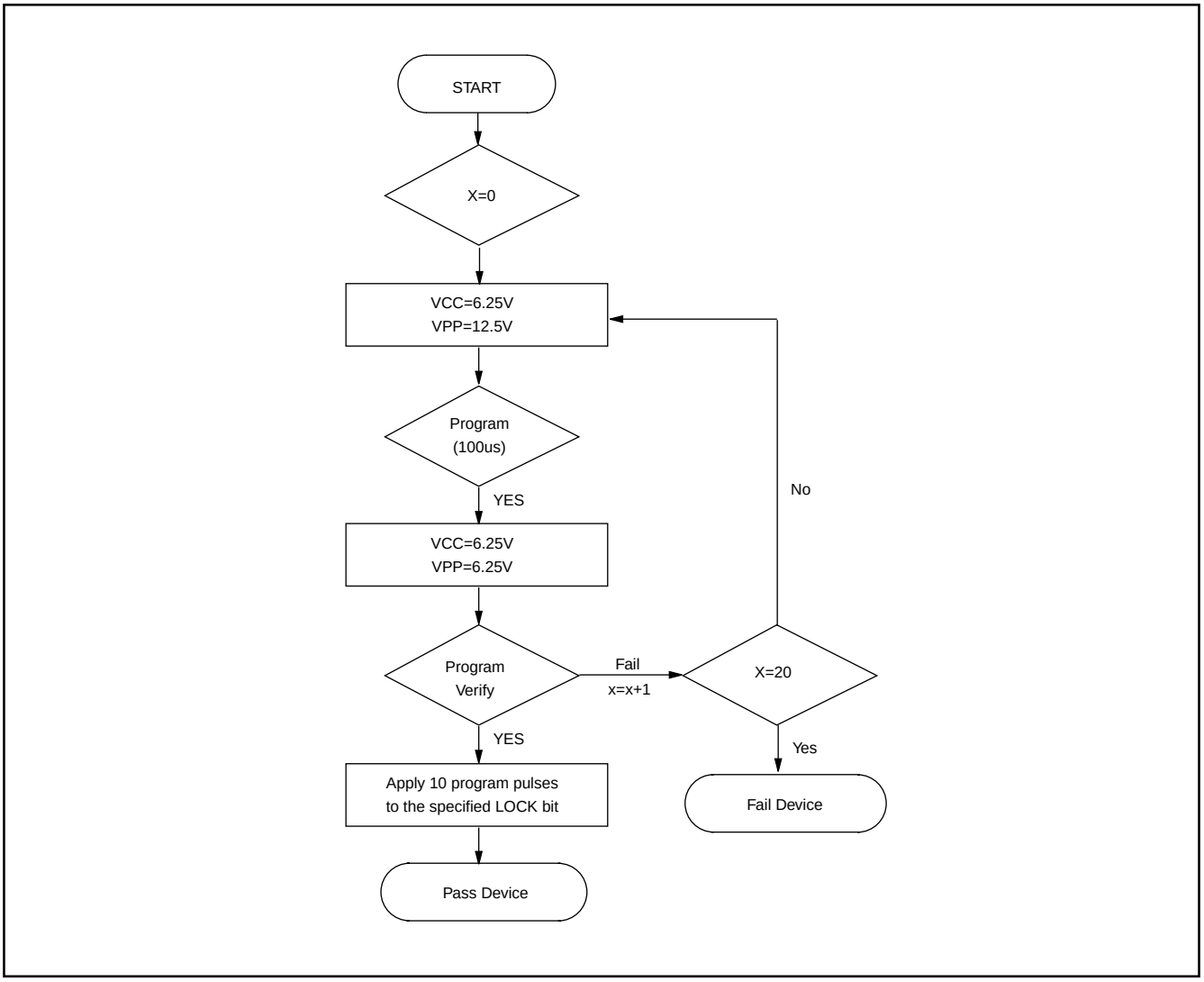


PROGRAM AND PROGRAM VERIFY FLOWCHART

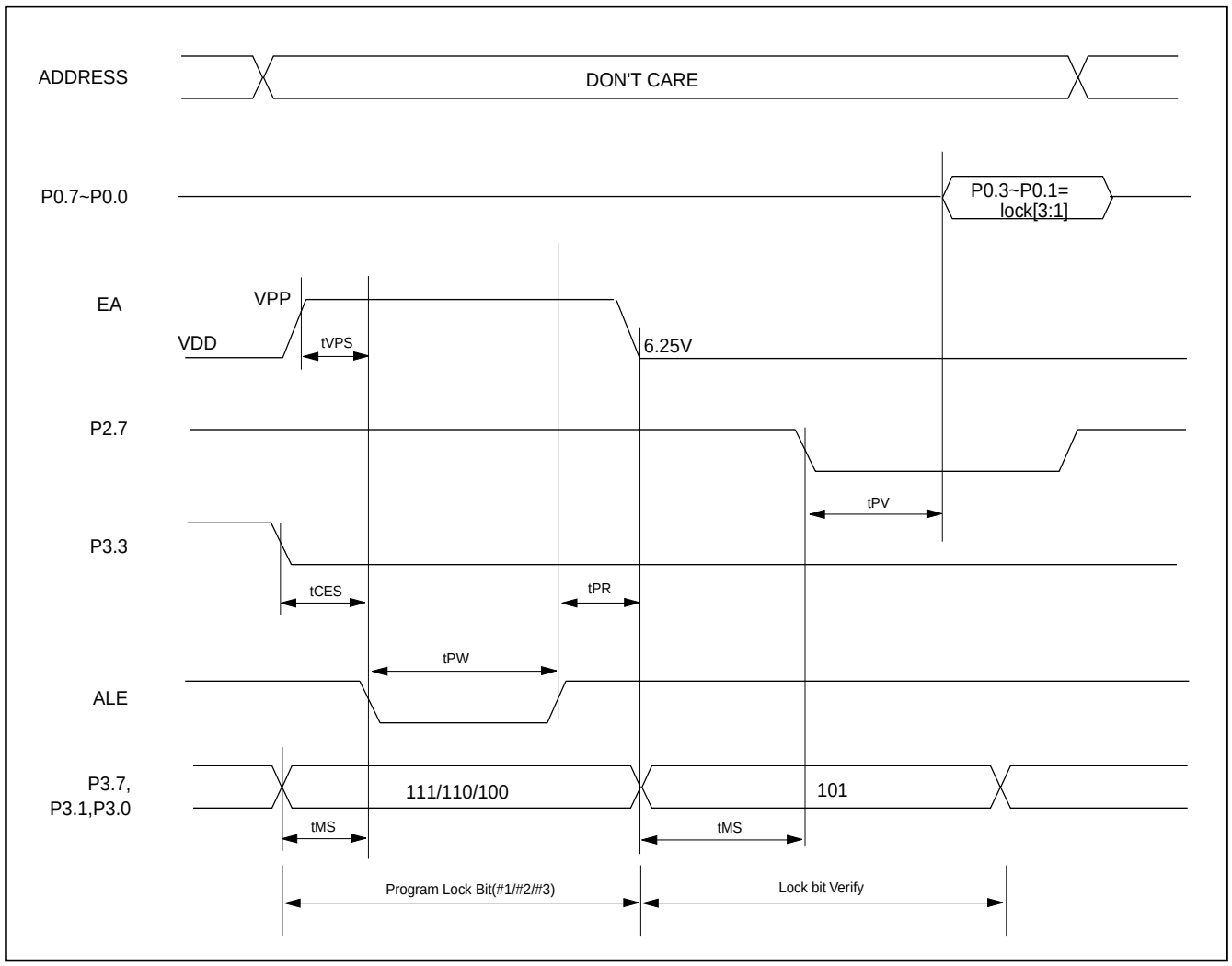


	tAS	tDS	tDH	tVPS	tCES	tMS	tPR	tPW	tPV
Mim.	2	2	2	2	2	2	2	20	
Max.								105	240
unit	us	us	us	us	us	us	us	us	ns

PROGRAM LOCK BITS AND PROGRAM VERIFY LOCK BITS FLOWCHART



PROGRAM LOCK BITS AND PROGRAM VERIFY LOCK BITS WAVEFORM



	tVPS	tCES	tMS	tPR	tPW	tPV
Mim.	2	2	2	2	20	
Max.					105	240
unit	us	us	us	us	us	ns

OPERATING CONDITIONS

Symbol	Description	Min	Max	Units
TA	Ambient Temperature Under Bias			
	Commerical	0	+70	℃
VCC		4.5	5.5	V
fOSC	Oscillator Frequency	3.5	40	MHz

DC CHARACTERISTICS (Over Operating Conditions)

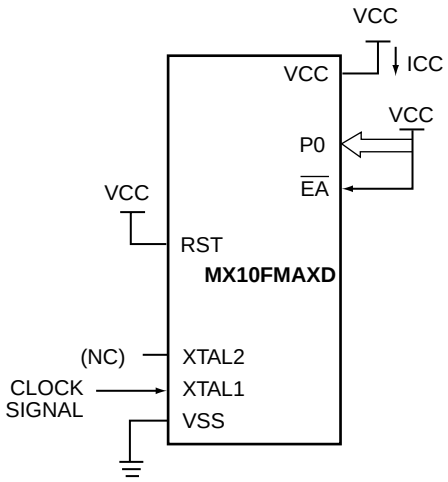
All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max (Note 4)	Unit	Test Conditions
VIL	Input Low Voltage	-0.5		0.2 VCC-0.1	V	
VIL1	Input Low Voltage $\overline{EA}$	0		0.2 VCC-0.3	V	
VIH	Input High Voltage	0.2 VCC+0.9		VCC+0.5	V	
	(Except XTAL1, RST)					
VIH1	Input High Voltage	0.7 VCC		VCC+0.5	V	
	(XTAL1, RST)					
VOL	Output Low Voltage (Note 5)					
	(Ports 1, 2, and 3)			0.4	V	IOL=1.6 mA (Note 1)
VOL1	Output Low Voltage (Note 5)					
	(Port 0, ALE, $\overline{PSEN}$)			0.4	V	IOL=3.2 mA (Note 1)
VOH	Output High Voltage	0.9 VDD			V	IOH=-10 uA
	(Port 1, 2 and 3, ALE, $\overline{PSEN}$)	0.75 VDD			V	IOH=-30 uA
		0.5 VDD			V	IOH=-60uA
VOH1	Output High Voltage	0.9 VDD			V	IOH=-80 uA
	(Port 0 in External Bus Mode)	0.75 VDD			V	IOH=-300 uA
		0.5 VDD			V	IOH=-800 uA
IIL	Logical 0 Input Current			-50	uA	VIN=0.4V
	(Ports 1, 2 and 3)					
ILI	Input leakage Current (Port 0)			±10	uA	VIN=VIL or VIH
ITL	Logical 1 to 0 Transition Current			-750	uA	VIN=2V
	(Ports 1, 2 and 3)					
	Industrial					
PRST	RST Pulldown Resistor	15		150	K ohm	
CIO	Pin Capacitance		10		pF	@1 MHz, 25℃
ICC	Power Supply Current:					(Note 3)
	Active Mode at 40 MHz			60	mA	
	Idle Mode at 40 MHz(70℃ 5.5V)			40	mA	
	Power Down Mode			100	uA	

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the VOLs of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signlas may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Triggers, or CMOS-level input logic.
2. Capacitive loading on Ports 0 and 2 cause the VOH on ALE and $\overline{\text{PSEN}}$ to drop below the 0.9 VCC specification when the address lines are stabilizing.
3. Minimum VCC for Power Down is 2V.
4. Typicals are based on a limited number of samples and are not guaranteed. The values listed are room temperature and 5V.
5. Under steady state (non-transient) conditions, IOL must be externally limited as follows:

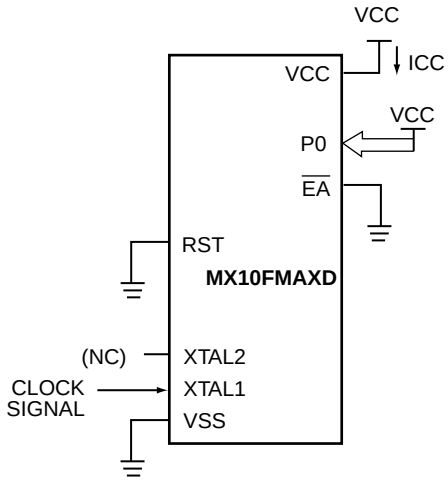
Maximum IOL per port pin:		10mA
Maximum IOL per 8-bit port:		
	Port 0:	26mA
	Ports 1, 2 and 3:	15mA
Maximum total IOL for all output pins:		71mA

If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.



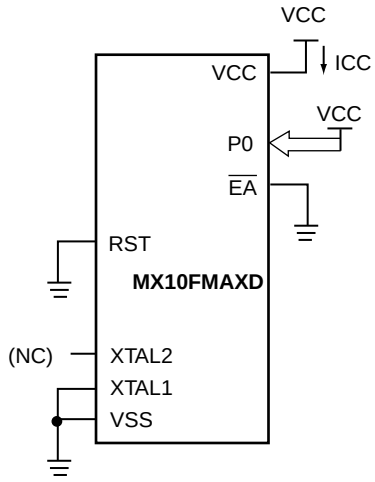
All other pins disconnected
TCLCH = TCHCL = 5ns

Figure 6. ICC Test Condition, Active Mode



All other pins disconnected
TCLCH = TCHCL = 5ns

Figure 7. ICC Test Condition Idle Mode



All other pins disconnected

Figure 8. ICC Test Condition, Power Down Mode VCC=2.0V to 6.0V

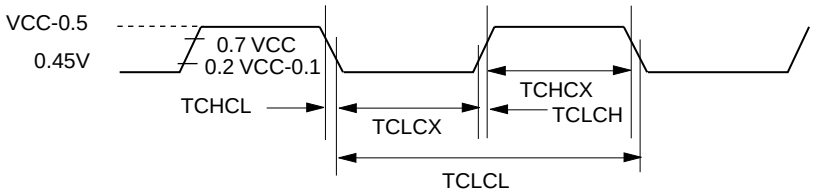


Figure 9. Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address
C: Clock
D: Input Data
H: Logic level HIGH
L: Logic level LOW, or ALE
P: $\overline{\text{PSEN}}$
Q: Output Data
R: RD signal
T: Time
V: Valid
W: $\overline{\text{WR}}$ signal
X: No longer a valid logic level
Z: Float

For example,

TAVLL = Time from Address Valid to ALE Low
TLLPL = Time from ALE Low to $\overline{\text{PSEN}}$ Low

AC CHARACTERISTICS

(Over Operating Conditions, Load Capacitance for Port 0, ALE/PROG and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

tCK min. = 1/f max. (maximum operating frequency); tCK=clock period

SYMBOL	PARAMETER	40 MHz		UNIT
		MIN	MAX	
EXTERNAL PROGRAM MEMORY				
TLHLL	ALE PULSE DURATION	20	-	NS
TAVLL	ADDRESS SET-UP TIME TO ALE	17	-	NS
TLLAX	ADDRESS HOLD TIME AFTER ALE	10	-	NS
TLLIV	TIME FROM ALE TO VALID INSTRUCTION INPUT	-	55	NS
TLLPL	TIME FROM ALE TO CONTROL PULSE $\overline{PSEN}$	17	-	NS
TPLPH	CONTROL PULSE DURATION $\overline{PSEN}$	70	-	NS
TPLIV	TIME FROM PSEN TO VALID INSTRUCTION INPUT	-	12	NS
TPXIX	INPUT INSTRUCTION HOLD TIME AFTER $\overline{PSEN}$	0	-	NS
TPXIZ	INPUT INSTRUCTION FLOAT DELAY AFTER $\overline{PSEN}$	-	20	NS
TAVIV	ADDRESS TO VALID INSTRUCTION INPUT	-	95	NS
TPLAZ	TO $\overline{PSEN}$ ADDRESS FLOAT TIME	-	10	NS
EXTERNAL DATA MEMORY				
TLHLL	ALE PULSE DURATION	20	-	NS
TAVLL	ADDRESS SET-UP TIME TO ALE	17	-	NS
TLLAX	ADDRESS HOLD TIME AFTER ALE	10	-	NS
TRLRH	RD PULSE DURATION	80	-	NS
TWLWH	WR PULSE DURATION	80	-	NS
TRLDV	RD TO VALID DATA INPUT	-	60	NS
TRHDX	DATA HOLD TIME AFTER RD	0	-	NS
TRHDZ	DATA FLOAT DELAY AFTER RD	32	-	NS
TLLDV	TIME FROM ALE TO VALID DATA INPUT	-	90	NS
TAVDV	ADDRESS TO VALID INPUT	-	105	NS
TLLWL	TIME FROM ALE TO RD OR WR	40	140	NS
TAVWL	TIME FROM ADDRESS TO RD OR WR	45	-	NS
TWHLH	TIME FROM RD OR WR HIGH TO ALE HIGH	10	55	NS
TQVWX	DATA VALID TO WR TRANSITION	10	-	NS
TQVWH	DATA SET-UP TIME BEFORE WR	125	-	NS
TWHQX	DATA HOLD TIME AFTER WR	10	-	NS
TRLAZ	ADDRESS FLOAT DELAY AFTER RD	-	0	NS

NOTE:
1. The maximun operating frequency is limited to 40 MHz and the minimum to 3.5 MHz.

External clock drive XTAL

SYMBOL	PARAMETER	VARIABLE CLOCK		UNIT
		MIN	MAX	
fCLK	clock frequency	3.5	40	MHz
tCLCL	clock period	25	285.7	ns
tCHCX	HIGH time	11	tCK-tCLCX	ns
tCLCX	LOW time	11	tCK-tCHCX	ns
tCLCH	RISE time	-	20	ns
tCHCL	FALL time	-	20	ns
tCY	cycle time (tCY = 12 tCK)	0.3	3.43	ms

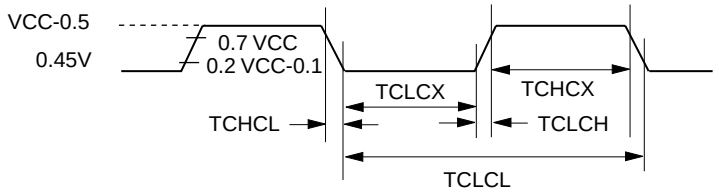
SERIAL PORT CHARACTERISTICS

Serial Port Timing : Shift Register Mode

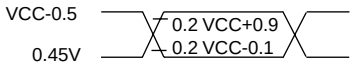
VDD = 5V±10%; VSS = 0V; Tamb=0 ℃; Load Capacitance = 80 pF

SYMBOL	PARAMETER	40 MHz OSCILLATOR		UNIT
		MIN	MAX	
tXLXL	Serial Port clock cycle time	300	-	ns
tQVXH	Output data setup to clock rising edge	138	-	ns
tXHQX	Output data hold after clock rising edge	5	-	ns
tXHDX	Input data hold after clock rising edge	0	-	ns
tXHDV	Clock rising edge to input data valid	-	138	ns

EXTERNAL CLOCK DRIVE WAVEFORM



AC TESTING INPUT, OUTPUT WAVEFORMS

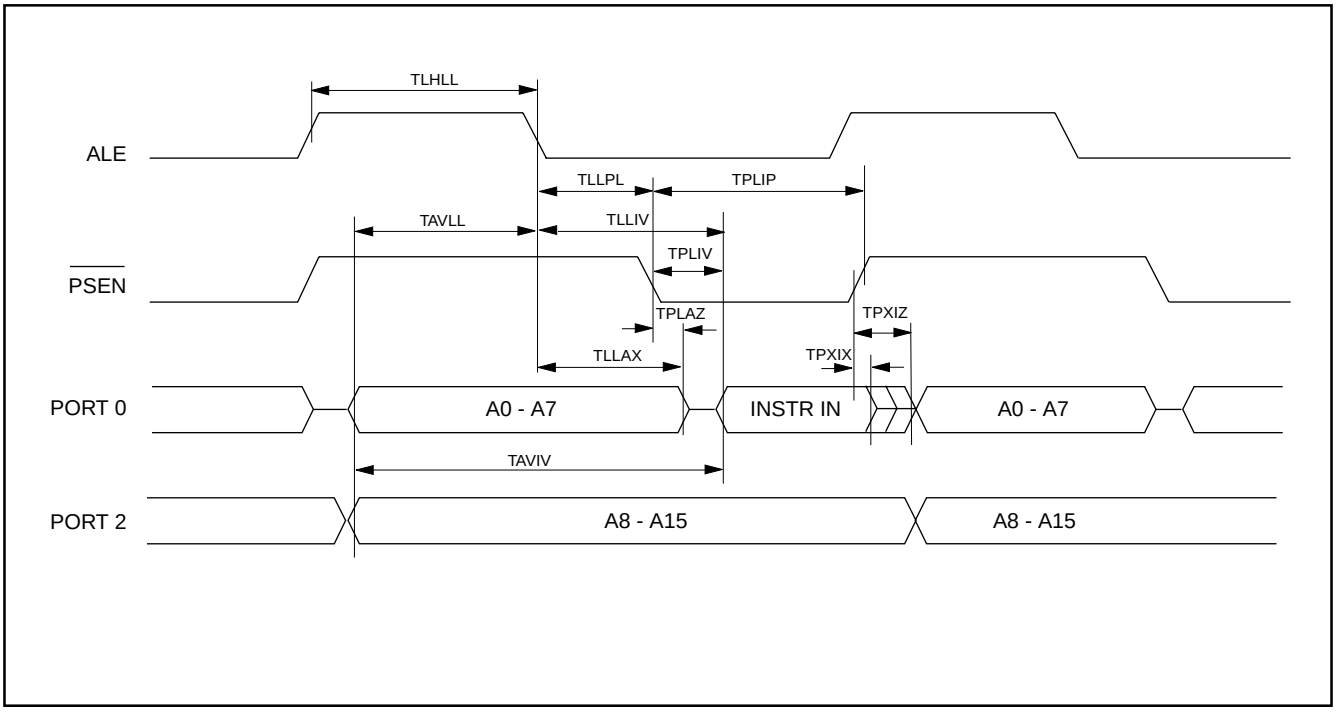


AC Inputs during testing are driven at VCC-0.5V for a Logic "1" 0.45V for a Logic "0". Timing measurements are made at VIH min for a Logic "1" and VIL max for a Logic "0".

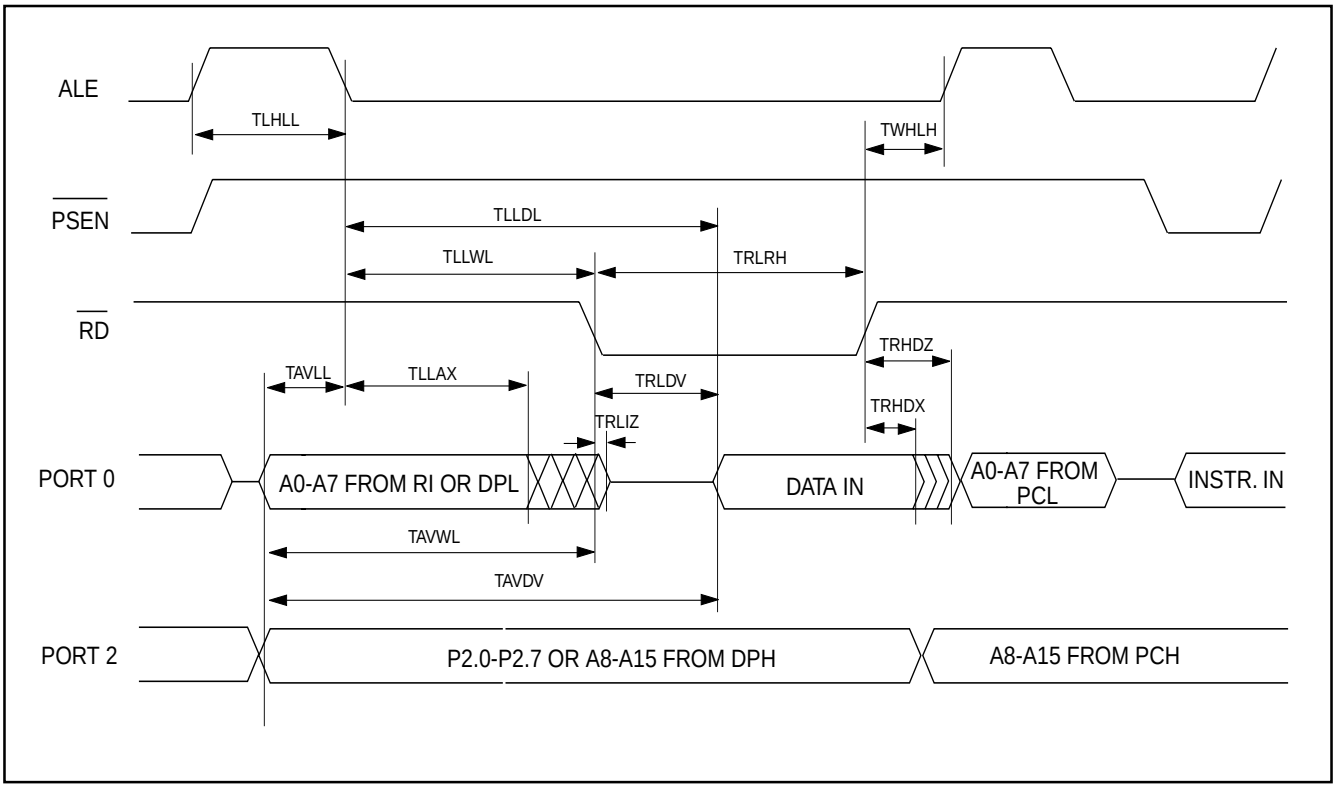
FLOAT WAVEFORM

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100mV change form the loaded VOH/VOL level occurs. IOL/IOH = ± 20 mA

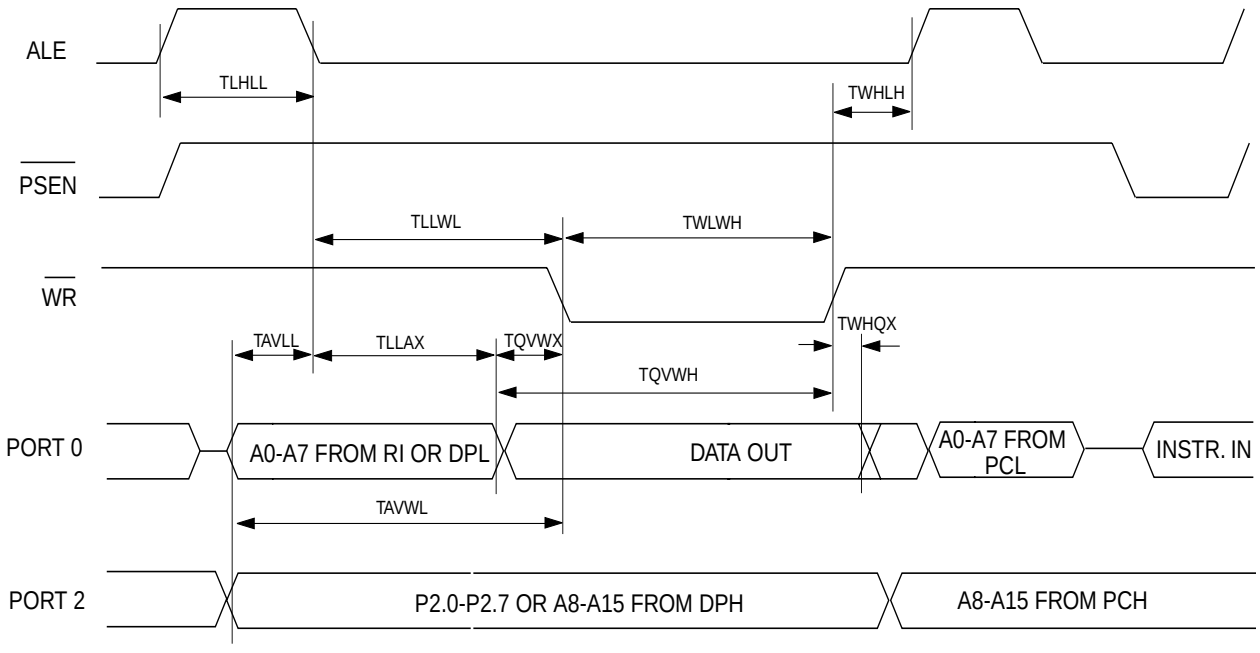
EXTERNAL PROGRAM MEMORY READ CYCLE



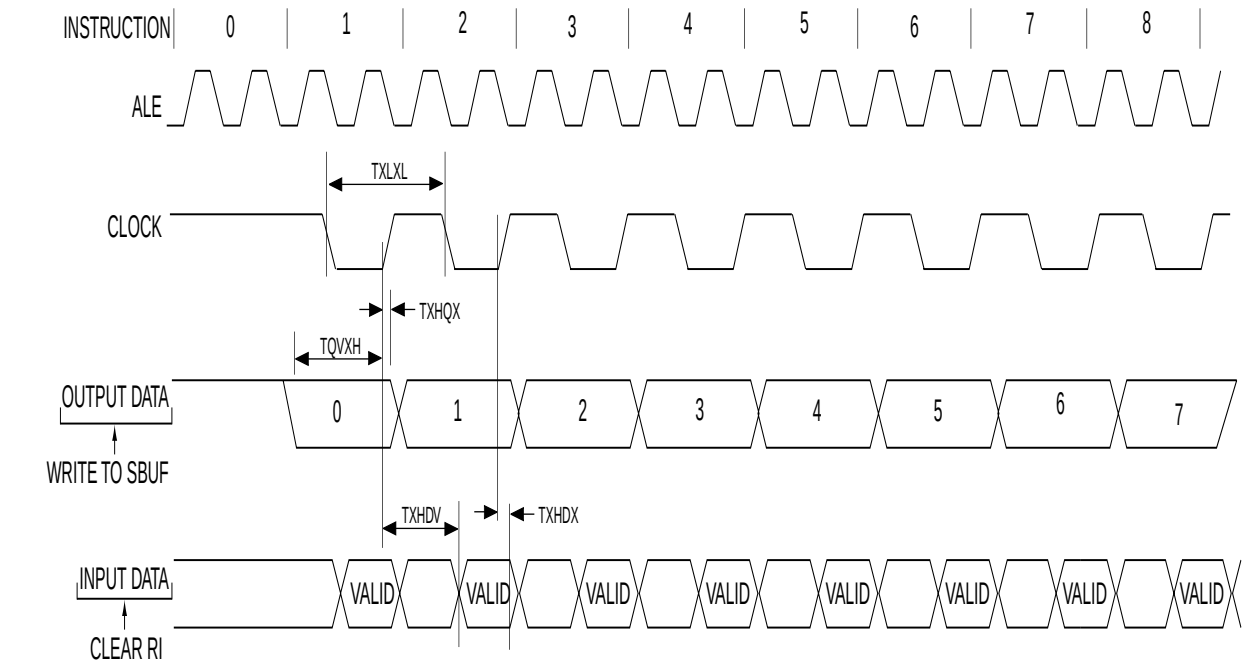
EXTERNAL DATA MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE

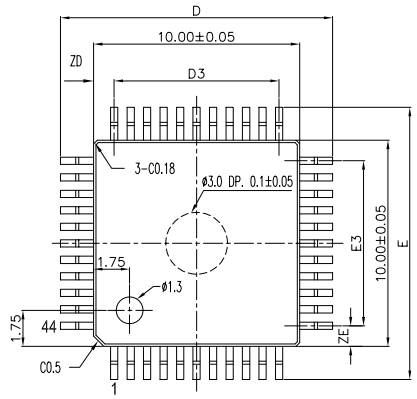


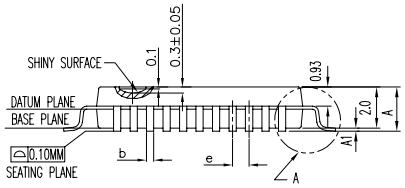
SHIFT REGISTER MODE TIMING WAVEFORMS

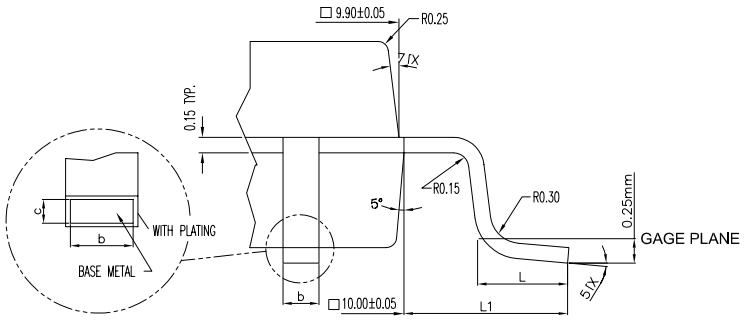


Package Information
QFP 44

Symbol	Dimension in inch (Ref.)			Dimension in mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A	0.085	0.089	0.093	2.15	2.25	2.35
A1	0.008	0.010	0.012	0.20	0.25	0.30
b	—	0.012	—	—	0.30	—
c	—	0.006	—	—	0.15	—
D	0.512	0.520	0.528	13.0	13.2	13.4
D3	—	0.315	—	—	8.00	—
e	—	0.032	—	—	0.80	—
E	0.512	0.520	0.528	13.0	13.2	13.4
E3	—	0.315		—	8.00	—
L	0.028	0.031	0.035	0.70	0.80	0.90
L1	0.059	0.063	0.067	1.5	1.6	1.7
ZD	—	0.039	—	—	1.00	—
ZE	—	0.039	—	—	1.00	—





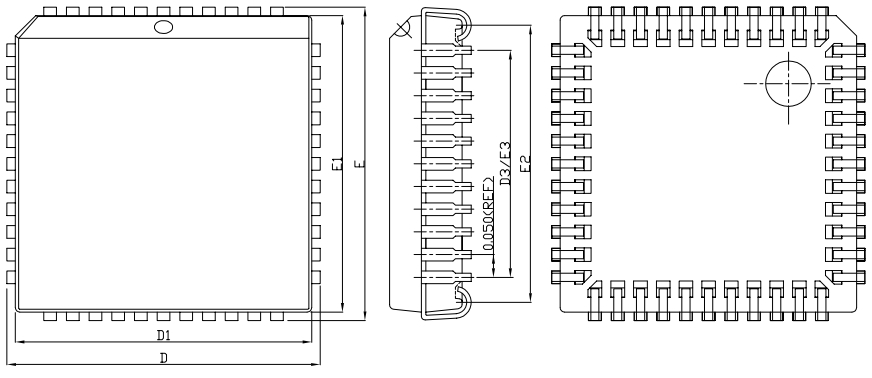


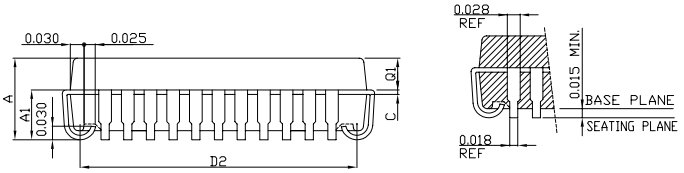
DETAIL "A"

MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd.				DWG. NO.	
				6110-0210	
TITLE PACKAGE OUTLINE FOR QFP 44L(10X10MM)				TOLERANCE .X ±. .XX ±.01 .XXX±.002	ANGLE
DRAWN	APPROVED	DATE	UNIT	REVISION	
C.L.Chiang	C.J.Weng	05-03-'01		6	

PLCC 44

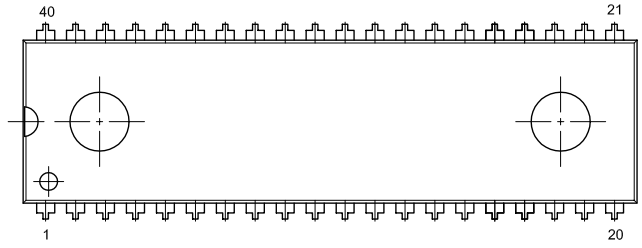
Symbol	Dimension In Inch (Ref.)			Dimension In mm (Base)		
	Min	Nom	Max	Min	Nom	Max
A			0.180			4.57
A1	0.100	0.105	0.110	2.54	2.67	2.79
Q1	0.068	0.070	0.072	1.73	1.78	1.83
c		0.010(REF)			0.25(REF)	
D	0.685	0.690	0.695	17.40	17.53	17.65
D1	0.650	0.653	0.656	16.51	16.59	16.66
D2	0.600	0.610	0.620	15.24	15.49	15.75
D3		0.500(REF)			12.70(REF)	
E	0.685	0.690	0.695	17.40	17.53	17.65
E1	0.650	0.653	0.656	16.51	16.59	16.66
E2	0.600	0.610	0.620	15.24	15.49	15.75
E3		0.500(REF)			12.70(REF)	
REFERENCE DOCUMENT : JEDEC SPEC -MS-016a						

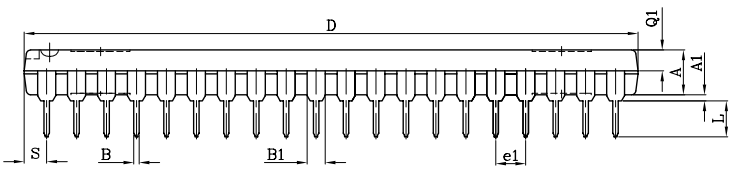


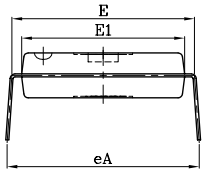


MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd.				DWG. NO.	
				6110-0209.3	
TITLE PACKAGE OUTLINE FOR PLCC 44L				TOLERANCE	
				.X ±. .XX ±.01 .XXX±.002	ANGLE ±2°
DRAWN	APPROVED	DATE	UNIT	REVISION	
C.L.Chiang	Dennis Chang	05-03-'01	inch	2	

DIP 40







UNIT / SYMBOL	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	2.05±0.005	52.07±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.075±0.005	1.0905±0.127

MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd.				DWG. NO. 6110-0202.4
TITLE PACKAGE OUTLINE FOR PDIP 40L (600 MIL)				TOLERANCE .X ±. ANGLE .XX ±.01 .XXX±.002
DRAWN	APPROVED	DATE	UNIT	REVISION
C.L.Chiang	Leo Lee	05-02-'01		4

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