Stellaris® LM3S1P51 RevB1 Errata

This document contains known errata at the time of publication for the Stellaris® LM3S1P51 microcontroller. The table below summarizes the errata and lists the affected revisions. See the data sheet for more details.

See also the ARM® Cortex™-M3 errata, ARM publication number PR326-PRDC-009450 v2.0.

Date	Revision	Description
July 2010	2.8	■ Added issue “The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled” on page 23.
June 2010	2.7	■ Added issue “Wake-up time from Hibernation may exceed specifications” on page 10. ■ Minor edits.
April 2010	2.6	■ The description of “VDD3ON mode may not be used” on page 9 was reworded. ■ The description of “Writes to Hibernation module registers sometimes fail” on page 11 was reworded. ■ Added issue “Hibernation Module 4.194304-MHz oscillator supports a limited range of crystal load capacitance values” on page 11. ■ Based on further examination of the "I^2C arbitration may be lost when operating as a master" issue, this issue has been moved to the GPIO section and renamed as “Schmitt input feature does not function correctly” on page 16. ■ Added information about items fixed on Rev C3.
March 2010	2.5	■ Added issue “The prescaler does not work correctly when counting up in periodic or one-shot mode” on page 20. ■ Added issue “Snapshot must be enabled in both Timer A and B when in 32-bit snapshot mode” on page 20. ■ Added issue “Phantom interrupts occur in Smart Card mode” on page 22. ■ Added issue "I^2C arbitration may be lost when operating as a master".

Date	Revision	Description
Mar 2010	2.4	■ Added issue “The option to force the ROM boot loader to execute at reset with an external pin does not function” on page 15. ■ Amended the workaround for issue “A spurious DMA request is generated when the timer rolls over in Input-Edge Time mode” on page 17. ■ Reworded description of issue “The value of the prescaler register is not readable in Edge-Count mode” on page 18. ■ Removed "Prescaler register must have a non-zero value in 16-bit Edge-Time mode" as it has been determined this item was included erroneously. ■ Added issue “ADC trigger and Wait-on-Trigger may assert when the timer is disabled” on page 18. ■ Added issue “Wait-on-Trigger does not assert unless the TnOTE bit is set” on page 18 . ■ Added issue “Do not enable match and timeout interrupts in 16-bit PWM mode” on page 19. ■ Added issue “Do not use µDMA with 16-bit PWM mode” on page 19. ■ Added issue “Writing the GPTMTnV register does not change the timer value when counting up” on page 19.
Feb 2010	2.3	■ Added issue “A spurious DMA request is generated when the timer rolls over the 16-bit boundary” on page 17. ■ Added issue “The value of the prescaler register is not readable in Edge-Count mode” on page 18. ■ Added issue "Prescaler register must have a non-zero value in 16-bit Edge-Time mode." ■ Added issue “The ADCSPC register does not function” on page 21.
Jan 2010	2.2	■ Modified description for “The General-Purpose Timer match register does not function correctly in 32-bit mode” on page 17 to include DMA operation. ■ Added issue “A spurious DMA request is generated when the timer rolls over in Input-Edge Time mode” on page 17.
Dec 2009	2.1	■ The status of “The Recover Locked Device sequence does not work as expected” on page 5 has been changed to "Fixed in Rev C." ■ "Hard Fault possible when waking from Sleep or Deep-Sleep modes and Cortex-M3 Debug Access Port (DAP) is enabled" has been removed and the content added to the LM3S1P51 data sheet. ■ The status of “VDD3ON mode may not be used” on page 9 has been changed to "Not fixed in Rev C." ■ Added additional APIs to “Some ROM functions are unsupported” on page 13. ■ “The µDMA controller fails to generate capture mode DMA requests from Timer A in the Timer modules” on page 15 has been added.
Nov 2009	2.0	Started tracking revision history.

Erratum Number	Erratum Title	Revision(s) Affected
1.1	JTAG INTEST instruction does not work	B1
1.2	The Recover Locked Device sequence does not work as expected	B1
2.1	Sleep and Deep-Sleep mode not usable at higher speeds when ISRs reside in Flash memory	B1
2.2	Device Capabilities registers may not accurately reflect available signals	B1
2.3	The PIOSC is not trimmed by the factory	B1
3.1	Hibernation module may have higher current draw than specified in data sheet under certain conditions	B1
3.2	Hibernate POR may not reset the Hibernation module until V_{DD} is applied	B1
3.3	Power consumption increases if V_{DD} is not restored after wake from hibernation	B1
3.4	ESD protection on the V_{BAT} pin does not meet specifications	B1
3.5	VDD3ON mode may not be used	B1, C1, C3
3.6	Hibernate module power consumption higher than expected in event wakeup configuration	B1
3.7	The Real-Time Clock gains or loses time going in and out of hibernation when using a crystal	B1
3.8	Wake-up time from Hibernation may exceed specifications	B1, C1
3.9	Low-battery detect circuit is powered down during hibernate	B1
3.10	Writes to Hibernation module registers sometimes fail	B1, C1, C3
3.11	Hibernation Module 4.194304-MHz oscillator supports a limited range of crystal load capacitance values	B1, C1, C3
4.1	Cumulative page erases may introduce bit errors in Flash memory	B1
4.2	Flash Write Buffer does not function above 50 MHz	B1
5.1	Some ROM functions are unsupported	B1
5.2	ROM mapping check for the Boot loader does not function properly	B1
5.3	ROM_I2CMasterErr function is incorrect	B1
5.4	ROM_SSIConfigSetExpClk function is incorrect	B1
5.5	The option to force the ROM boot loader to execute at reset with an external pin does not function	B1, C1
6.1	The µDMA controller fails to generate capture mode DMA requests from Timer A in the Timer modules	B1, C1, C3
7.1	Port B [1:0] pins require external pull-up resistors	B1
7.2	Schmitt input feature does not function correctly	B1, C1
8.1	The General-Purpose Timer match register does not function correctly in 32-bit mode	B1, C1, C3
8.2	A spurious DMA request is generated when the timer rolls over in Input-Edge Time mode	B1, C1, C3
8.3	A spurious DMA request is generated when the timer rolls over the 16-bit boundary	B1, C1, C3
8.4	The value of the prescaler register is not readable in Edge-Count mode	B1, C1, C3

Erratum Number	Erratum Title	Revision(s) Affected
8.5	ADC trigger and Wait-on-Trigger may assert when the timer is disabled	B1, C1, C3
8.6	Wait-on-Trigger does not assert unless the TnOTE bit is set	B1, C1, C3
8.7	Do not enable match and timeout interrupts in 16-bit PWM mode	B1, C1, C3
8.8	Do not use µDMA with 16-bit PWM mode	B1, C1, C3
8.9	Writing the GPTMTnV register does not change the timer value when counting up	B1, C1, C3
8.10	The prescaler does not work correctly when counting up in periodic or one-shot mode	B1, C1, C3
8.11	Snapshot must be enabled in both Timer A and B when in 32-bit snapshot mode	B1, C1, C3
9.1	Writes to Watchdog Timer 1 module WDTLOAD register sometimes fail	B1, C1, C3
10.1	ADC hardware averaging produces erroneous results in differential mode	B1, C1, C3
10.2	The ADCSPC register does not function	B1
11.1	UART Smart Card (ISO 7816) mode does not function	B1
11.2	When in IrDA mode, the UnRx signal requires configuration even if not used	B1
11.3	Phantom interrupts occur in Smart Card mode	B1, C1
11.4	The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled	B1, C1, C3
12.1	An interrupt is not generated when using µDMA with the SSI module if the EOT bit is set	B1
13.1	Some bits in the I2SMCLKCFG register do not function	B1
13.2	I^2S SCLK signal is inverted in certain modes	B1
14.1	PWM generation is incorrect with extreme duty cycles	B1
14.2	Sync of PWM does not trigger "zero" action	B1
14.3	PWM "zero" action occurs when the PWM module is disabled	B1
14.4	PWM Enable Update register bits do not function	B1
15.1	Momentarily exceeding V_{IN} ratings on any pin can cause latch-up	B1
15.2	Power-on event may disrupt operation	B1

1 JTAG

1.1 JTAG INTEST instruction does not work

Description:

The JTAG INTEST (Boundary Scan) instruction does not properly capture data.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

1.2 The Recover Locked Device sequence does not work as expected

Description:

If software configures any of the JTAG/SWD pins as GPIO or loses the ability to communicate with the debugger, there is a debug sequence that can be used to recover the microcontroller, called the Recover Locked Device sequence. After reconfiguring the JTAG/SWD pins, using the Recover Locked Device sequence does not recover the device.

Workaround:

To get the device unlocked, follow these steps:

1. Power cycle the board and run the debug port unlock procedure in LM Flash Programmer. DO NOT power cycle when LM Flash Programmer tells you to.
2. Go to the Flash Utilities tab in LM Flash Programmer and do a mass erase operation (check "Entire Flash" and then click the Erase button). This erase appears to have failed, but that is ok.
3. Power cycle the board.
4. Go to the Flash Utilities tab in LM Flash Programmer and do another mass erase operation (check "Entire Flash" and then click the Erase button).

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

2 System Control

2.1 Sleep and Deep-Sleep mode not usable at higher speeds when ISRs reside in Flash memory

Description:

Sleep and Deep-Sleep modes cannot be used when running the processor at 66 or 80 MHz when the Interrupt Service Routines (ISRs) and vector table reside in Flash memory. If Sleep or Deep-Sleep mode is used at those speeds, an invalid PC is sometimes returned for the interrupt vector address when exiting sleep mode.

Workaround:

There are two possible workarounds for this issue:

1. Store the ISRs and vector table in the on-chip SRAM when running the processor at 66 or 80 MHz.
2. Run the processor at 50 MHz.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

2.2 Device Capabilities registers may not accurately reflect available signals

Description:

Some of the Device Capabilities register bits reflect the presence of specific pins on the microcontroller. These bits do not always properly reflect the available signals. Bits affected include **DC3** [31:0], **DC4** [15:14], **DC5** [27:24] and [7:0], and **DC8** [31:0]. Do not rely on the value of these bits in system design.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

2.3 The PIOSC is not trimmed by the factory

Description:

The PIOSC is not trimmed by the factory prior to shipment. This errata item affects any product with date codes prior to 0946.

Workaround:

For parts that have a Hibernation module, the PIOSC can be user calibrated. The PIOSC cannot be calibrated on parts without a Hibernation module.

Silicon Revision Affected:

B1

Fixed:

Fixed for devices with date codes beginning 0946.

3 Hibernation Module

3.1 Hibernation module may have higher current draw than specified in data sheet under certain conditions

Description:

If a battery voltage is applied to the VBAT power pin prior to power being applied to the VDD power pins of the device, the current draw from the VBAT pin is greater than expected. The current may

be as high as 1.6 mA instead of the data sheet specified 17 µA. The condition exists until power is applied to the VDD pin. Once the VDD pin has been powered, the VBAT current draw functions as expected. The VDD pin can then be powered up and down as required and the VBAT pin current specification is maintained.

Workaround:

The VBAT pin higher-than-specified current draw condition can be avoided if the microcontroller's VDD power pins are powered on prior to the time a battery voltage is initially applied to the VBAT pin.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

3.2 Hibernate POR may not reset the Hibernation module until V_{DD} is applied

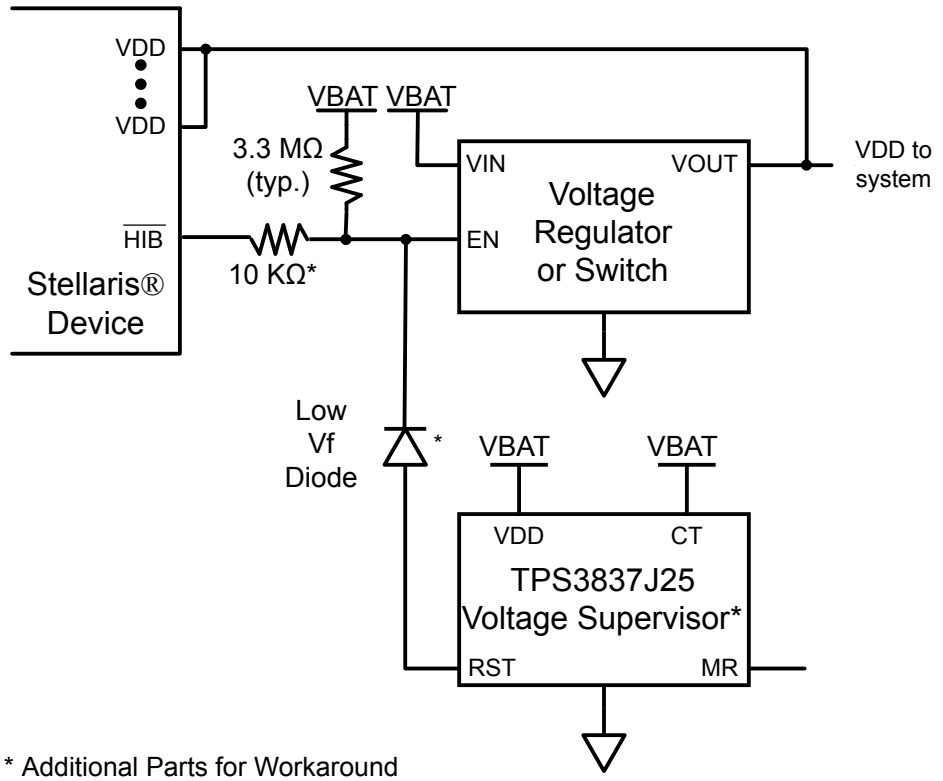
Description:

If V_{DD} is not powered when voltage is first applied to V_{BAT}, the state of the Hibernation module is indeterminate and the $\overline{\text{HIB}}$ signal may be asserted. In this indeterminate state, a lock condition can occur in which the Hibernation module waits for a power-on-reset, but that reset cannot occur until the module deasserts $\overline{\text{HIB}}$. This issue is related to the errata “Hibernation module may have higher current draw than specified in data sheet under certain conditions” on page 6.

Workaround:

The workaround implementation depends on the system-level power supply configuration. For systems that use a battery as the primary power source, an external voltage supervisor (TPS383J25DBV or similar) circuit can be added to force the V_{DD} power supply to start when the battery voltage is first applied (see Figure 1). The voltage supervisor requires only 220 nA and generates a 200-ms positive pulse to turn on the V_{DD} regulator and activate the microcontoller's internal POR circuit.

Figure 1. Workaround Circuit to Ensure Initial Power Up



Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

3.3 Power consumption increases if V_{DD} is not restored after wake from hibernation

Description:

If a wake event occurs and V_{DD} does not rise to specified levels, then the wake event is held off until V_{DD} is within specified levels. If a large delay occurs between the wake event and VDD reaching specified levels, the V_{BAT} current increases substantially to a typical value of 255 µA until V_{DD} reaches the specified levels, at which point the microcontroller comes out of hibernation and power consumption returns to expected levels.

Workaround:

Ensure that V_{DD} reaches specified levels within 250 µs after the wake event occurs.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

3.4 ESD protection on the V_{BAT} pin does not meet specifications

Description:

The ESD protection on the V_{BAT} pin fails when tested at 2 kV.

Workaround:

Extra precaution should be taken to protect the part from ESD events. Some applications may require system-level ESD protection on this pin.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

3.5 VDD3ON mode may not be used

Description:

The VDD3ON mode may not be used.

Workaround:

None. Do not use the VDD3ON mode to enter hibernation.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

3.6 Hibernate module power consumption higher than expected in event wakeup configuration

Description:

With the Hibernation module configured for an external event wakeup, the current consumption of the device is higher than expected. The Hibernation module clock does not shut down properly during the hibernate asynchronous external wake mode resulting in extra current consumption. Some devices properly shut down the clock the first time entering this mode and others do not. When waking from a hibernate event, the Hibernation module clock is always enabled. In subsequent hibernate cycles, the oscillator is not shut down properly and remains active. Hibernate module current consumption averages 21µA with the clock disabled. The current consumption averages 31µA with the Hibernation module clock enabled.

Workaround:

When the Hibernation module clock is not required during hibernation, software can disable it by clearing the CLK32EN bit in the **Hibernation Control (HIBCTL)** register before going into hibernation mode.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

3.7 The Real-Time Clock gains or loses time going in and out of hibernation when using a crystal

Description:

When using a 4.194304-MHz crystal, the Real-Time clock in the Hibernation module gains or loses a small amount of time (on the order of one second over a 24-hour period when cycling hibernate mode 4 times a minute) when going in and out of hibernation.

Workaround:

Use an external 32.768-kHz oscillator as the source for the Hibernation module clock.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

3.8 Wake-up time from Hibernation may exceed specifications

Description:

The Hibernation module is specified to resume operation after the $\overline{\text{WAKE}}$ signal is asserted within 124 µs, however operation may not resume for 30 ms in some cases. (The "Hibernation Module AC Characteristics" table in the DS indicates 10 ms.)

Workaround:

None.

Silicon Revision Affected:

B1, C1

Fixed:

Fixed in Rev C3.

3.9 Low-battery detect circuit is powered down during hibernate

Description:

The low-battery detect feature on the V_{BAT} input is only valid when V_{DD} power is present. As a result:

- Because the battery is not electrically loaded when V_{DD} is present, the low-battery detect circuit may not reflect the actual battery status.
- In Hibernate mode, a low-battery condition may prevent wake until the battery is completely depleted.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

3.10 Writes to Hibernation module registers sometimes fail

Description:

Due to a synchronization issue with the independent clock domain of the Hibernation module, writes may sometimes fail, even though the WRC bit in the **HIBCTL** register is set after the write occurs.

Workaround:

After performing a write to any Hibernation module register or non-volatile memory, read the contents back and verify that they are correct. If they are incorrect, perform the write operation again.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

3.11 Hibernation Module 4.194304-MHz oscillator supports a limited range of crystal load capacitance values

Description:

For some 4.194304-MHz crystals, the manufacturer-recommended crystal value may be outside of the capabilities of the hibernate module oscillator. If the crystal manufacturer's recommended load capacitance is used, the hibernate oscillator may fail to start.

For a parallel-resonant oscillator circuit, the total load capacitance C_L (as specified by the manufacturer) is calculated as follows:

$C_L = (C_1 * C_2) / (C_1 + C_2) + C_S$

Due to the workaround, C_1 and C_2 are limited to 20 pF. Using 3 pF for stray capacitance (C_S), the formula above shows that a crystal with C_L of 13 pF is the highest value supported due to this errata. Refer to the crystal datasheet to determine which crystals have an acceptable load capacitance (Cl) range.

Workaround:

Use load capacitors of 20 pF or less (18 pF is typical). Note that for some crystals, this value may pull the oscillator frequency slightly away from the crystal manufacturer's specified accuracy. Your crystal manufacturer can provide this information.

Alternatively, use an external 32.768-kHz oscillator as the source for the Hibernation module clock.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

4 Internal Memory

4.1 Cumulative page erases may introduce bit errors in Flash memory

Description:

Cumulative page erases anywhere in the Flash memory array may introduce bit errors. The bit error is not confined to the page being erased or the 4-KB block but could be in any page in the Flash memory. A page erase is used to erase a 1-KB page so it can be rewritten. A mass erase erases the entire Flash memory array (all pages). A bit error means that a bit may change from 0 to 1 or 1 to 0.

Workaround:

There are two possible workarounds for this issue:

1. Minimize total page erases to less than 3000 between mass erases for the lifetime of the product. After each mass erase, an additional 3000 page erase operations are allowed before bit errors may be introduced. At the rate of one page erase per week, this issue would not be seen over at least 17 years.

2. Perform CRC checks on all Flash memory after page erases to increase the chances of detecting the issue. The two CRC functions built into ROM can assist in this.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

4.2 Flash Write Buffer does not function above 50 MHz

Description:

The Flash Write Buffer does not successfully program the Flash memory at speeds above 50 MHz.

Workaround:

Lower the speed of the system clock to 50 MHz or less while programming the Flash memory.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

5 ROM

5.1 Some ROM functions are unsupported

Description:

The following functions are unsupported in ROM:

- ADCComparatorConfigure
- ADCComparatorRegionSet
- ADCComparatorReset
- ADCComparatorIntDisable
- ADCComparatorIntEnable
- ADCComparatorIntStatus
- ADCComparatorIntClear
- GPIOPinConfigure
- GPIOPinTypeI2S
- I2CSlaveIntClearEx
- I2CSlaveIntDisableEx
- I2CSlaveIntEnableEx
- I2CSlaveIntStatusEx
- I2SIntClear
- I2SIntDisable
- I2SIntEnable
- I2SIntStatus
- I2SMasterClockSelect
- I2SRxConfigSet
- I2SRxDataGet
- I2SRxDataGetNonBlocking
- I2SRxDisable
- I2SRxEnable
- I2SRxFIFOLevelGet
- I2SRxFIFOLimitGet
- I2SRxFIFOLimitSet
- I2STxConfigSet
- I2STxDataPut
- I2STxDataPutNonBlocking
- I2STxDisable
- I2STxEnable
- I2STxFIFOLevelGet
- I2STxFIFOLimitGet
- I2STxFIFOLimitSet
- I2STxRxConfigSet
- I2STxRxDisable
- I2STxRxEnable
- IntPendSet
- IntPendClear
- SSIBusy
- SysCtlDelay
- SysCtlI2SMClkSet
- UARTBusy
- UARTFIFODisable
- UARTFIFOEnable
- UARTRxErrorClear

- UARTRxErrorGet
- UARTTxIntModeGet
- UARTTxIntModeSet
- uDMAChannelSelectDefault
- uDMAChannelSelectSecondary

Workaround:

Code for these functions is included in the current version of StellarisWare, which can be downloaded from the website at http://www.ti.com/software_updates.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

5.2 ROM mapping check for the Boot loader does not function properly

Description:

Before the processor is released from the reset state, the System Control module is supposed to check offset 0x0000.0004 of Flash memory looking for a reset vector that is not 0xFFFF.FFFF. If an initialized reset vector is found, Flash memory is mapped to address 0x0000.0000, otherwise ROM is mapped to address 0x0000.0000. Currently, the System Control module errantly checks offset 0x0000.0008, which is the NMI vector. So, in situations where a valid reset vector (offset 0x0000.0004) has been programmed, but the NMI vector has not been programmed, the ROM is errantly mapped to zero preventing the application that is stored in Flash memory from being executed out of reset.

Workaround:

Ensure that the NMI vector is always programmed.

Silicon Revision Affected:

B1

Fixed:

ROM boot loader does not function in Rev C1. Address 0x0000.0000 is checked in Rev C3.

5.3 ROM_I2CMasterErr function is incorrect

Description:

The ROM_I2CMasterErr function currently assumes that bit 2 of the **I2CMCS** register is set in all error conditions and, if this bit is clear, assumes no error has occurred. Unfortunately, this bit only indicates an ACK error so the function returns I2C_MASTER_ERR_NONE if the controller loses arbitration. I2C_MASTER_ERR_ARB_LOST is expected in this case.

Workaround:

Use the StellarisWare I2CMasterErr function in Flash memory.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

5.4 ROM_SSIConfigSetExpClk function is incorrect

Description:

If a non-Motorola format was specified in a call to the ROM_SSIConfigSetExpClk function, two lower bits of a clock divisor register could be corrupted. This corruption results in a small error in the actual clock rate.

Workaround:

Use the StellarisWare SSIConfigSetExpClk function in Flash memory.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

5.5 The option to force the ROM boot loader to execute at reset with an external pin does not function

Description:

The option to force the ROM boot loader to execute at reset with an external pin does not function. Changing the `PORT` and `PIN` fields of the **Boot Configuration (BOOTCFG)** register has no effect.

Workaround:

The ROM boot loader still executes if address 0x0000.0004 contains 0xFFFF.FFFF, indicating that the Flash memory has not been programmed.

Silicon Revision Affected:

B1, C1

Fixed:

Fixed in Rev C3.

6 µDMA

6.1 The µDMA controller fails to generate capture mode DMA requests from Timer A in the Timer modules

Description:

The µDMA controller fails to generate DMA requests from Timer A in the General-Purpose Timer modules when in the Event Count and Event Time modes.

Workaround:

Use Timer B.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

7 GPIO

7.1 Port B [1:0] pins require external pull-up resistors

Description:

The internal pull-up resistors are not effective for the Port B0 and B1 pins.

Workaround:

External pull-up resistors must be used on these two pins when they are used as GPIOs.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

7.2 Schmitt input feature does not function correctly

Description:

The Schmitt input on digital inputs may generate spurious transitions when connected to low slew-rate signal sources. If the input signal has a slew rate of less than 1V/µs, a negative edge can generate several additional transitions into the microcontroller even though the input signal is still within the hysteresis band. Positive edges are not affected.

The additional transitions can cause anomalous operation in any peripherals or GPIOs that use digital inputs. Most at risk are peripherals that use pull-up resistors (I^2C, GPIOs) or that typically involve slower signals (sensor inputs). This behavior can affect the noise immunity of digital inputs. As a result, arbitration may be lost during communication when the I^2C module is the master.

Workaround:

Ensure that all signals connected to digital inputs have a slew rate of at least 1V/µs. In some applications, reducing the resistance value of pull-up and pull-down resistors may be necessary. Note that R-C filters, such as low pass, on digital input signals should only be used if the slew-rate is still above 1V/µs, or if additional transitions on the falling edge can be tolerated. Adding an external Schmitt-trigger circuit is a requirement for circuits where slow transitions are unavoidable and system noise levels are high.

Silicon Revision Affected:

B1, C1

Fixed:

Fixed in Rev C3.

8 General-Purpose Timer

8.1 The General-Purpose Timer match register does not function correctly in 32-bit mode

Description:

The **GPTM Timer A Match (GPTMTAMATCHR)** register triggers a match interrupt and a DMA request, if enabled, when the lower 16 bits match, regardless of the value of the upper 16 bits.

Workaround:

None.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.2 A spurious DMA request is generated when the timer rolls over in Input-Edge Time mode

Description:

When the timer is in Input-Edge Time mode and rolls over after the terminal count, a spurious DMA request is generated.

Workaround:

Either ignore the spurious interrupt, or capture the edge time into a buffer via DMA, then the spurious interrupt can be detected by noting that the captured value is the same as the previous capture value.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.3 A spurious DMA request is generated when the timer rolls over the 16-bit boundary

Description:

When the timer is in 32-bit periodic or one-shot mode and is enabled to generate periodic DMA requests, a spurious DMA request is generated when the timer rolls past 0x0000FFFF.

Workaround:

Only use DMA with a 16-bit periodic timer.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.4 The value of the prescaler register is not readable in Edge-Count mode

Description:

In Edge-Count mode, the prescaler is used as an 8-bit high order extension to the 16-bit counter. When reading the **GPTM Timer n (GPTMTnR)** register as a 32-bit value, the bits [23:16] always contain the initial value of the **GPTM Timer n Prescale (GPTMTnPR)** register, that is, the "load" value of the 8-bit extension.

Workaround:

None.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.5 ADC trigger and Wait-on-Trigger may assert when the timer is disabled

Description:

If the value in the **GPTM Timer n Match (GPTMTnMATCHR)** register is equal to the value of the timer counter and the TnOTE bit in the **GPTM Control (GPTMCTL)** register is set, enabling the ADC trigger, the trigger fires even when the timer is disabled (the TnEN bit in the **GPTMCTL** register is clear). Similarly, if the value in the **GPTMTnMATCHR** register is equal to the value of the timer counter and the TnWOT bit in the **GPTM Timer n Mode (GPTMTnMR)** register is set, enabling the Wait-on-Trigger mode, the trigger fires even when the timer is disabled.

Workaround:

Enable the timer before setting the TnOTE bit. Also, for the Wait-on-Trigger mode, ensure that the timers are configured in the order in which they will be triggered.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.6 Wait-on-Trigger does not assert unless the TnOTE bit is set

Description:

Wait-on-Trigger does not assert unless the TnOTE bit is set in the **GPTMCTL** register.

Workaround:

If the TnWOT bit in the **GPTM Timer n Mode (GPTMTnMR)** register is set, enabling the Wait-on-Trigger mode, the TnOTE bit must also be set in the **GPTMCTL** register in order for the Wait-on-Trigger to fire. Note that when the TnOTE bit is set, the ADC trigger is also enabled.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.7 Do not enable match and timeout interrupts in 16-bit PWM mode

Description:

16-bit PWM mode generates match and timeout interrupts in the same manner as periodic mode.

Workaround:

Ensure that any unwanted interrupts are masked in the **GPTMTnMR** and **GPTMIMR** registers.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.8 Do not use µDMA with 16-bit PWM mode

Description:

16-bit PWM mode generates match and timeout µDMA triggers in the same manner as periodic mode.

Workaround:

Do not use µDMA to transfer data when the timer is in 16-bit PWM mode.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.9 Writing the GPTMTnV register does not change the timer value when counting up

Description:

When counting up, writes to the **GPTM Timer n Value (GPTMTnV)** register do not change the timer value.

Workaround:

None.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.10 The prescaler does not work correctly when counting up in periodic or one-shot mode

Description:

When counting up, the prescaler does not work correctly in 16-bit periodic or snap-shot mode.

Workaround:

Do not use the prescaler when counting up in 16-bit periodic or snap-shot mode.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

8.11 Snapshot must be enabled in both Timer A and B when in 32-bit snapshot mode

Description:

When a periodic snapshot occurs in 32-bit periodic mode, only the lower 16-bit are stored into the **GPTM Timer A (GPTMTAR)** register.

Workaround:

If both the TASNAPS and TBSNAPS bits are set in the **GPTM Timer A Mode (GPTMTAMR)** register, the entire 32-bit snapshot value is stored in the **GPTMTAR** register.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

9 Watchdog Timer 1

9.1 Writes to Watchdog Timer 1 module WDTLOAD register sometimes fail

Description:

Due to the independent clock domain of the Watchdog Timer 1 module, writes to the **Watchdog Load (WDTLOAD)** register may sometimes fail, even though the WRC bit in the **WDTCTL1** register is set after the write occurs.

Workaround:

After performing a write to the **WDTLOAD** register, read the contents back and verify that they are correct. If they are incorrect, perform the write operation again.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

10 ADC

10.1 ADC hardware averaging produces erroneous results in differential mode

Description:

The implementation of the ADC averaging circuit does not work correctly when the ADC is sampling in differential mode and the difference between the voltages is approximately 0.0V.

Workaround:

Do not use hardware averaging in differential mode. Instead, use the FIFO to store results and average them in software.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

10.2 The ADCSPC register does not function

Description:

The **ADC Sample Phase Control (ADCSPC)** register does not function and cannot be used.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

11 UART

11.1 UART Smart Card (ISO 7816) mode does not function

Description:

The UnTX signal does not function correctly as the bit clock in Smart Card mode.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

11.2 When in IrDA mode, the UnRx signal requires configuration even if not used

Description:

When in IrDA mode, the transmitter may not function correctly if the UnRx signal is not used.

Workaround:

When in IrDA mode, if the application does not require the use of the UnRx signal, the GPIO pin that has the UnRx signal as an alternate function must be configured as the UnRx signal and pulmac High.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

11.3 Phantom interrupts occur in Smart Card mode

Description:

In Smart Card mode, after receiving a valid TX interrupt, phantom parity error interrupts occur, even though all **UARTRIS** and **UARTMIS** bits are clear.

Workaround:

Make sure to always clear the parity error interrupt in the interrupt handler, even when the PERIS and PEMIS bits are clear.

Silicon Revision Affected:

B1, C1

Fixed:

Fixed in Rev C3.

11.4 The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled

Description:

The RTRIS (UART Receive Time-Out Raw Interrupt Status) bit in the **UART Raw Interrupt Status (UARTRIS)** register should be set when a receive time out occurs, regardless of the state of the RTIM enable bit in the **UART Interrupt Mask (UARTIM)** register. However, currently the RTIM bit must be set in order for the RTRIS bit to be set when a receive time out occurs.

Workaround:

For applications that require polled operation, the RTIM bit can be set while the UART interrupt is disabled in the NVIC using the IntDisable(n) function in the StellarisWare Peripheral Driver Library, where n is 21, 22, or 49 depending on whether UART0, UART1 or UART2 is used. With this configuration, software can poll the RTRIS bit, but the interrupt is not reported to the NVIC.

Silicon Revision Affected:

B1, C1, C3

Fixed:

Not yet fixed.

12 SSI

12.1 An interrupt is not generated when using µDMA with the SSI module if the EOT bit is set

Description:

When using the primary µDMA channels with the SSI module, an interrupt is not generated on transmit µDMA completion if the EOT bit (bit 4 of the **SSICR1** register) is enabled.

Workaround:

Use the alternate µDMA channels for the SSI module.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

13 I2S

13.1 Some bits in the I2SMCLKCFG register do not function

Description:

The top 2 bits of the RXI and TXI bit fields in the **I2SMCLKCFG** register do not function (bits [29:28] of RXI and bits [13:12] of TXI). The RXI and TXI fields contain the 10-bit integer input for the receive and transmit clock generator, respectively. The remaining 8 bits in each field function correctly, so most of the possible integer input choices can be used in system design.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

13.2 I²S SCLK signal is inverted in certain modes

Description:

When the I²S controller is operating as a receiver in SCLK Master mode, the WS signal is latched on the rising edge of SCLK, not the falling edge. In addition, when the controller is operating as a transmitter in SCLK Slave mode, the data is launched on the rising edge of SCLK, not the falling edge.

Workaround:

For the transmitter, there are two possible workarounds for this issue:

1. Ensure that the I2S0TXSCK signal leads the I2S0TXWS signal by at least 4 ns.
2. Configure as I²S mode with DAC in Left-Justified audio format.

For the receiver, ensure that the CODEC is configured as the SCLK master, and the I²S receive module is configured as the SCLK slave.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

14 PWM

14.1 PWM generation is incorrect with extreme duty cycles

Description:

If a PWM generator is configured for Count-Up/Down mode, and the **PWM Load (PWMnLOAD)** register is set to a value N, setting the compare to a value of 1 or N-1 results in steady state signals instead of a PWM signal. For example, if the user configures PWM0 as follows:

- PWMENABLE = 0x00000001
  - PWM0 Enabled
- PWM0CTL = 0x00000007
  - Debug mode enabled
  - Count-Up/Down mode
  - Generator enabled
- PWM0LOAD = 0x00000063
  - Load is 99 (decimal), so in Count-Up/Down mode the counter counts from zero to 99 and back down to zero (200 clocks per period)
- PWM0GENA = 0x000000b0
  - Output High when the counter matches comparator A while counting up
  - Output Low when the counter matches comparator A while counting down
- PWM0DBCTL = 0x00000000
  - Dead-band generator is disabled

If the **PWM0 Compare A (PWM0CMPA)** value is set to 0x00000062 (N-1), PWM0 should output a 2-clock-cycle long High pulse. Instead, the PWM0 output is a constant High value.

If the **PWM0CMPA** value is set to 0x00000001, PWM0 should output a 2-clock-cycle long negative (Low) pulse. Instead, the PWM0 output is a constant Low value.

Workaround:

User software must ensure that when using the PWM Count-Up/Down mode, the compare values must never be 1 or the **PWMnLOAD** value minus one (N-1).

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

14.2 Sync of PWM does not trigger "zero" action

Description:

If the **PWM Generator Control (PWM0GENA)** register has the ActZero field set to 0x2, then the output is set to 0 when the counter reaches 0, as expected. However, if the counter is cleared by setting the appropriate bit in the **PWM Time Base Sync (PWMSYNC)** register, then the "zero" action is not triggered, and the output is not set to 0.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

14.3 PWM "zero" action occurs when the PWM module is disabled

Description:

The zero pulse may be asserted when the PWM module is disabled.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

14.4 PWM Enable Update register bits do not function

Description:

The ENUPDn bits in the **PWM Enable Update (PWMENUPD)** register do not function. As a result, enabling the PWM modules can't be synchronized.

Workaround:

None.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

15 Electrical Characteristics

15.1 Momentarily exceeding V_{IN} ratings on any pin can cause latch-up

Description:

To avoid latch-up, the maximum DC ratings of the part must be strictly enforced. The most common violation of the V_{IN} electrical specification can occur when a mechanical switch or contact is connected directly to a GPIO or special function ($\overline{RST}$, $\overline{WAKE}$, ...) pin. The circuit shown in Figure 2 on page 27 typically has stray inductance and capacitance that can cause a voltage glitch when the switch transitions, as shown in Figure 3 on page 27. The magnitude of the glitch may exceed the V_{IN} in the maximum DC ratings table in the Electrical Characteristics chapter. Figure 4 on page 27 shows an improved circuit that eliminates the glitch.

Figure 2. Incorrect Reset Circuitry

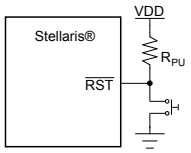
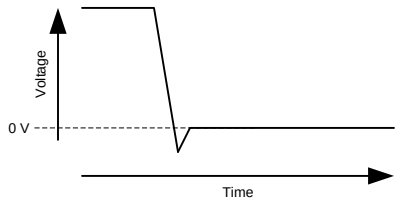


Figure 3. Excessive Undershoot Voltage on Reset

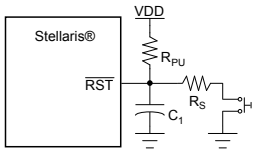


Workaround:

Use a circuit as shown in Figure 4 on page 27. In this circuit, R_S should be less than or equal to $R_{PU}/10$. C_1 should be matched to R_{PU} to achieve a suitable t_{RC} for the application. Typical values are:

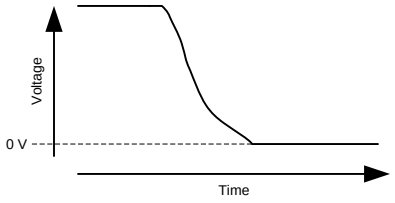
- R_{PU} = 10 kΩ
- R_S = 470 Ω
- C_1 = 0.01 µF

Figure 4. Recommended Reset Circuitry



After implementing the circuit shown in Figure 4 on page 27, confirm that the voltage on the $\overline{RST}$ input has a curve similar to the one in Figure 5 on page 28, and that the V_{IN} specification is not exceeded.

Figure 5. Recommended Voltage on Reset



Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

15.2 Power-on event may disrupt operation

Description:

Incorrect power sequencing during power up can disrupt operation and potentially cause device failure.

Workaround:

V_{DDC} must be applied approximately 50 µs before V_{DD}. Normally V_{DDC} is controlled by the part's internal LDO voltage regulator. The workaround requires the addition of an external regulator (see Figure 6) to ensure that V_{DDC} sequencing requirements are met (see Figure 7). A recommended regulator is the TI TPS73101DBVR.

This fix mitigates the on-chip power issue, but does not solve it completely. During development, the Flash memory should also be reprogrammed (using LMFlash or another programming tool) at least once a week.

Figure 6. Configuration of External Regulator

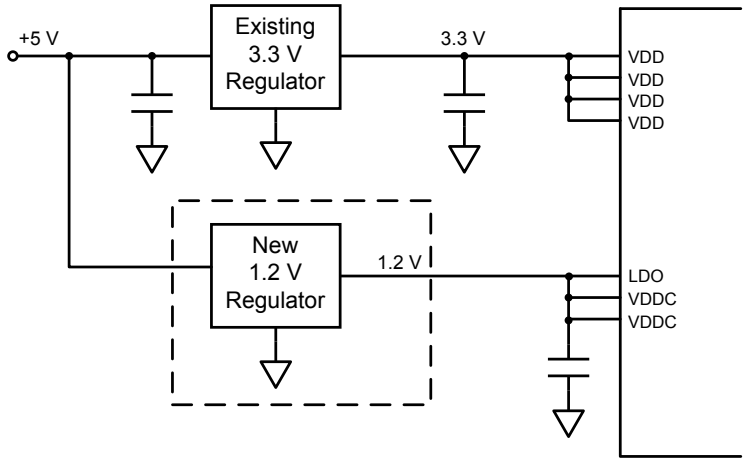
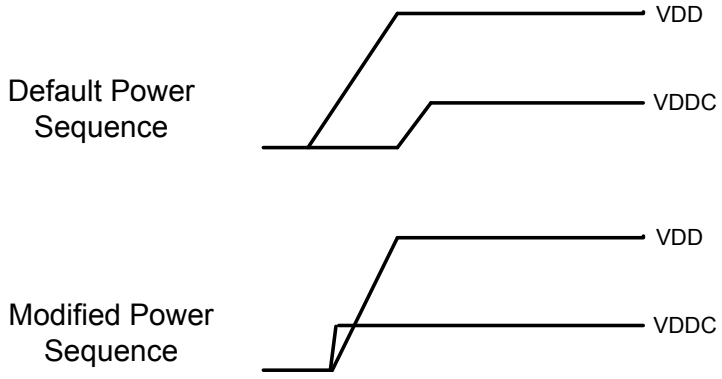


Figure 7. VDDC Sequencing Requirements



Detailed characterization is ongoing. Contact the Applications Support Team for the latest information.

Silicon Revision Affected:

B1

Fixed:

Fixed in Rev C1.

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