80C51GB, 83C51GB, 87C51GB SPECIFICATION UPDATE

Release Date: December, 1996
Order Number: 272880-003

The 80C51GB, 83C51GB, 87C51GB may contain design defects or errors known as errata. Characterized errata that may cause the 80C51GB, 83C51GB, 87C51GB's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Rev. Date	Version	Description
07/01/96	001	This is the original Specification Update document. It contains all errata identified to this date.
11/13/96	002	Deleted items from the “additions and changes to A/D converter specifications” paragraph of erratum number 9600002 (these items are reflected in the current version of the datasheet), changed status of erratum number 9600002 (fixed in B-step), and changed status of erratum number 9600003 (will be documented in the future). Clarified specification change number 001. Added specification change number 002.
12/11/96	003	Added specification clarification number 001.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270648-008
MCS® 51 Microcontroller Family User's Manual	272383-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80C51GB, 83C51GB, 87C51GB product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings			Page	Status	ERRATA
	A-1	B	B-2			
9600001	X			6	Fixed	Powerdown Current
9600002	X			6	Fixed	Analog-to-digital Converter
9600003	X	X		7	Doc	Power Off Flag

Specification Changes

Number	Steppings			Page	Status	SPECIFICATION CHANGES
	A-1	B	B-2			
001		X		5	Doc	Features Added and Changed in B-step
002			X	5	Doc	Lock Bits Moved to UPROM to Enhance Security (87C51GB)

Specification Clarifications

Number	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	A-1	B	B-2			
001	X	X	X	5	Doc	Port 1 and 3 Reset Values

Documentation Changes

Number	Document Revision	Page	Status	DOCUMENTATION CHANGES
001	272383-002	13	Doc	*MCS® 51 Microcontroller Family User's Manual,* 8XC51GB Hardware Description

IDENTIFICATION INFORMATION

Markings

No special identifier. Standard 8XC51GX product marking.

ERRATA

9600001. Powerdown Current

PROBLEM: The 87C51GB (A-1 stepping) powerdown current (Ipd) is defined as 200 µA maximum with all output pins disconnected, crystal unconnected, EA# = Vcc, Port 0 = Vcc, and RESET = Vss.

However, the 87C51GB exhibits high Ipd at high temperatures (+135°C). A typical controller draws an average of 20 – 50 µA at room temperature. The cause of the high Ipd is attributed to P624 process characteristics. Therefore, we do not specify Ipd on the A-1 stepping, so powerdown mode is restricted. We expect the problem to be resolved when the 87C51GB (B stepping) moves to process P629.

IMPLICATION: In high-temperature environments, systems may exhibit higher than expected Ipd.

WORKAROUND: None defined.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected steppings.

9600002. Analog-to-digital Converter

PROBLEM: The 87C51GB (A-1 stepping) A/D channel 4 (ACH4) has been despecified. Channel 4 does not convert correctly at combinations of high Vcc, high frequency, and low temperature. The remaining channels (ACH0–ACH3 and ACH5–ACH7) are fully functional at –45 to +135°C.

In the A-1 stepping, the input to the A/D converter is a field-effect transistor (FET), and Input resistance is 1 MΩ or greater.

IMPLICATION: Designs using ACH4 at low temperature, high Vcc, and high frequency may experience unpredictable results.

WORKAROUND: Avoid using ACH4, especially under the indicated conditions.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected steppings.

9600003. Power Off Flag

PROBLEM: The power off flag (POF) is mentioned in the *87C51GB Architectural Overview*; however, it was not included in the datasheet because it is not fully tested. The POF will be tested at Vcc=3.0V and defined in a future datasheet after the B-step.

IMPLICATION: It is unlikely that this condition will cause a system malfunction.

WORKAROUND: None.

STATUS: Doc. Refer to Summary Table of Changes to determine the affected steppings.

SPECIFICATION CHANGES

001. Features Added and Changed in B-step

PROBLEM: The 8xC51GB (B-step) is based on the FX core, with all of the FX design features. The B-step includes the following major changes and enhancements.

- Changed Features
  - — Port 1 reset state (low after reset)
  - — Reset pin polarity (active low)
  - — Third signature byte is implemented
- Added Features
  - — Third lock bit implemented
  - — Asynchronous reset
  - — Interrupts can be invoked by software (undocumented in A-step)
  - — P1.0/T2 is Timer 2 overflow output
  - — P3.3 function added for programming protection

Changed Features

This section describes the features that changed from the A-step to the B-step 87C51GB.

1. Port 1 Reset State

Port 1 is low after reset in B-step, but was high after reset in A-step. This change makes ports 1 and 4 at the same logic levels during reset and operation. (Only port 1 reset logic

level was changed.) The port 1 registers, timer functions, and timer logic levels remain the same as in A-step.

If both A-step and B-step controllers are to be used with a common PC board, software might be used during initialization to invert B-step port 1 outputs (write SFR 90H just after reset) to maintain the same logic levels for A-step and B-step controllers. This action could cause a “glitch” during reset on the B-step port 1 outputs. Unless a valid reset pulse (two machine cycles or longer) is provided, the ports will not latch their reset state.

2. Reset Polarity

The reset signal is active-low in B-step, but was active-high in A-step. This change allows designers to use a simple RC circuit to reset the controller at power-up. An internal 100Ω pullup resistor permits generating a power-on reset using only an external capacitor to ground. The capacitance should be large enough to allow the crystal oscillator time (at least two machine cycles) to start before the capacitor releases the reset signal. If the reset pin is connected to ground through a 1-µF capacitor, the B-step 87C51GB will generate an automatic reset when Vcc is turned on.

The “Power on Reset Circuitry” drawing in the 8XC51GB Hardware Description in the *MCS® 51 Microcontroller Family User’s Manual* shows the capacitor connected from the reset pin to ground.

The A-step required an inverter in the reset circuit for most regulators. The B-step does not require the inverter. When reset is held low, the B-step 87C51GB enters the reset state. When reset is driven high or released, the internal pullup resistor pulls the reset signal high and allows the processor to begin executing instructions at 0000H.

Unless a valid reset pulse (two machine cycles or longer) is provided, the ports will not latch their reset state.

If both A-step and B-step controllers are to be used with a common PC board, jumpers should be included in the reset circuit for inverter or capacitor changes. These jumpers shuld allow designers to configure the reset signal for A-step or B-step controllers with little effort. If only B-step controllers are used, the reset circuit can be designed without the jumpers.

3. Signature Bytes

A new signature byte has been added to the 83C51GB and 87C51GB B-step, increasing the number of signature bytes to three. To read the signature bytes, activate the control pins as shown in the following table and use the procedure for EPROM verification.

Task	RST	PSEN#	ALE/ PROG#	EA#/Vpp	P2.6	P2.7	P3.3	P3.6	P3.7
Read Signature Bytes	H	L	H	H	L	L	L	L	L

The following tables list the locations and contents of the signature bytes for the A-step and B-step, respectively.

Location	Contents		Description
	87C51GB A-step	83C51GB A-step	
1EH	89H	89H	Identifies the product as an Intel controller
1FH	5AH	5BH	Identifies the specific product

Location	Contents		Description
	87C51GB B-step	83C51GB B-step	
30H	89H	89H	Identifies the product as an Intel controller
31H	58H	58H	Identifies an FX-core product
60H	EBH	6BH or EBH	Identifies the specific FX-core product

Added Features

This section describes the enhancements to the B-step controller, which is based on the FX core.

1. Program Memory Lock

The 83C51GB and 87C51GB B-step feature three locks bits and a 64-byte encryption array for program security. The following table lists the lock bits and their effect on the controller. Item 5 on page 11 lists the signals required to program the lock bits and encryption array.

Security Level	Lock Bit			Protection Level
	LB3	LB2	LB1	
1	U	U	U	No program lock features are implemented. On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
2	U	U	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
3	U	P	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is disabled.
4	P	P	P	Code cannot execute from external memory. On-chip code memory verification is disabled.

U = unprogrammed; P= programmed. Other combinations of the lock bits are undefined.

2. Asynchronous Reset

The B-step 8xC51GB microcontrollers feature an asynchronous port reset. For A-step controllers, the oscillator must be be running and at least 19 oscillator periods must occur between the time that a logic 1 is applied to the RESET pin and the time that the port pins are driven to their reset states.

For B-step controllers, the oscillator need not be running. The port pins are driven to their reset states as soon as a valid logic 1 is applied to the RESET pin.

3. Interrupt Structure

Interrupts can be invoked by software as well as by the peripherals. Software can invoke an interrupt by writing to an interrupt pending register (C5H and C6H in the SFR map). This feature should enhance program development and debugging as well as normal operation. (It was not documented in the A-step.)

4. Timer 2 Clockout

A 50% duty-cycle clock output function has been added to P1.0. In addition to being a standard I/O pin, P1.0 has two alternate functions: it can input the external clock for timer/counter 2; or it can output a 50% duty-cycle clock ranging from 61 Hz to 4 MHz at operating frequencies up to 16 MHz.

To configure timer/counter 2 as a clock generator, clear the C/T2 bit in T2CON and set the T2OE bit in T2MOD. The TR2 bit in T2CON starts and stops the clock.

The frequency of the clock output depends on the oscillator frequency and the reload value of the Timer 2 capture registers (RCAP2H and RCAP2L), as shown in this equation:

$$\text{Clockout Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

5. Control Pin P3.3 Added to Programming Algorithm

A control pin (P3.3) has been added to the programming algorithm. This programming algorithm is **not** compatible with previous steppings. Hold P3.3 high to program the EPROM and low to verify it. The following table indicates the levels at which the control and program signals must be held to accomplish each programming and verification task.

Task	RST	PSEN#	ALE/ PROG#	EA#/Vpp	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code	H	L	L †	Vpp ††	L	H	H	H	H
Verify Code	H	L	H	H	L	L	L	H	H
Program Encryption Array	H	L	L †	Vpp ††	L	H	H	L	H
Program Lock Bit 1	H	L	L †	Vpp ††	H	H	H	H	H
Program Lock Bit 2	H	L	L †	Vpp ††	H	H	H	L	L
Program Lock Bit 3	H	L	L †	Vpp ††	H	L	H	H	L
Read Signature Bytes	H	L	H	H	L	L	L	L	L

† ALE/PROG# is pulsed low for 100 µs for programming.

†† Vpp = +12.5V ± 5%

002. Lock Bits Moved to UPROM to Enhance Security (87C51GB)

PROBLEM: To enhance security, the lock bits have been moved from EPROM to UPROM. The UPROM is a secure area on the device; values written to UPROM cannot be changed. The function of the lock bits, the method for programming them, and the use of the encryption array remain unchanged.

IMPLICATION: Verify that your EPROM code is correct before setting any lock bits. Because the lock bits are in UPROM, the lock bits cannot be changed after they are programmed once. If you set only LB1, you can still verify your code, but you cannot reprogram the EPROM (although you can still erase it using ultraviolet light). If you set LB2, you can no longer verify the EPROM code.

Security Level	Lock Bit			Protection Level
	LB3	LB2	LB1	
1	U	U	U	No program lock features are implemented. On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
2	U	U	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
3	U	P	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is disabled.
4	P	P	P	Code cannot execute from external memory. On-chip code memory verification is disabled.

U = unprogrammed; P= programmed. Other combinations of the lock bits are undefined.

SPECIFICATION CLARIFICATIONS

001. Port 1 and 3 Reset Values

PROBLEM: The reset value of all ports is logic “1”; however, the reset value of ports 1 and 3 is sustained by a weak pull-up. It is recommended that applications **not** use the reset value of these ports to drive external loads. If the application requires the use of the reset value of these ports, an external pull-up resistor should be added.

DOCUMENTATION CHANGES

001. MCS® 51 Microcontroller Family User’s Manual, 8XC51GB Hardware Description

ITEM: The 8XC51GB Hardware Description in the *MCS® 51 Microcontroller Family User’s Manual* contains an error. On page 6-41, the last two sentences of Section 11.1 should read as follows:

If OSCR = 0FEH, the OFD is enabled. If OSCR=0FFH, the OFD is disabled.