DS1, 2002-07-31

**C161U**

**Embedded C166 with USB, USART and SSC**

**SAF C161U-LF, Version 1.3**

Please, replace the erroneous description in the C161U Data Sheet, 2001-04-19, by the following **correct** text:

# 1 Fast External Interrupts

Page 127, second paragraph:

The pins of Port 2 (P2.1...P2.0) can individually be programmed to this fast interrupt mode, where also the trigger transition (rising, falling or both) can be selected. The External Interrupt Control register EXICON controls this feature for all **2** pins.

**EXICON ($F1C0_H$ / $E0_H$)** **ESFR** **Reset Value: $0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | | 00 | | 00 | | 00 | | 00 | | 00 | | EXI1ES | | EXI0ES | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Bit | Function |
|---|---|
| **EXIxES** | **External Interrupt x Edge Selection Field (x = 1:0)**<br>0 0 Fast external interrupts disabled: standard mode<br>0 1 Interrupt on positive edge (rising)<br>1 0 Interrupt on negative edge (falling)<br>1 1 Interrupt on any edge (rising or falling) |

Revision History: Previous Version:

Major Changes:

# 2 External Interrupt Source Control

Page 128.

EXISEL register is defined as follows:

**EXISEL ($F1DA_H$ / $ED_H$)** **ESFR-b** **Reset Value: $0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EXI7SS | | 00 | | EXI5SS | | EXI4SS | | EXI3SS | | EXI2SS | | 00 | | 00 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Bit | Function |
|---|---|
| **EXI0SS** | 0 0 Must be set to ’00’.<br>0 1 Not allowed.<br>1 0 Not allowed.<br>1 1 Not allowed. |
| **EXI1SS** | 0 0 Must be set to ’00’.<br>0 1 Not allowed.<br>1 0 Not allowed.<br>1 1 Not allowed. |
| **EXI2SS** | 0 0 Not applicable.<br>0 1 Input from source ASC_RxD @ P3.11.<br>1 0 Not allowed.<br>1 1 Not allowed. |
| **EXI3SS** | 0 0 Not applicable.<br>0 1 Input from source SSC_RxD @ P3.9.<br>1 0 Not allowed.<br>1 1 Not allowed. |
| **EXI4SS** | 0 0 Not applicable.<br>0 1 Input from source SSC_SCLK @ P3.13.<br>1 0 Not allowed.<br>1 1 Not allowed. |
| **EXI5SS** | 0 0 Not applicable.<br>0 1 Input from source USB_suspend interrupt.<br>1 0 Not allowed.<br>1 1 Not allowed. |

| Bit | Function |
|---|---|
| **EXI6SS** | 0 0 Must be set to ’00’.<br>0 1 Not allowed.<br>1 0 Not allowed.<br>1 1 Not allowed. |
| **EXI7SS** | 0 0 Not applicable.<br>0 1 Input from source RTC_INT.<br>1 0 Not allowed.<br>1 1 Not allowed. |

# 3 Interrupt Subnode Control

Page 130.

The ISNC register is defined as follows:

**ISNC ($F1DE_H$ / $EF_H$)** **ESFR-b** **Reset Value: $0000_H$**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | PLL IE | PLL IR | RTC T14 IE | RTC T14 IR |

| Bit | Function |
|---|---|
| **T14IR** | **T14 Overflow Interrupt Request Flag**<br>‘0’ No request pending<br>‘1’ This source has raised an interrupt request |
| **T14IE** | **T14 Overflow Interrupt Enable Control Bit**<br>‘0’ Interrupt request is disabled<br>‘1’ Interrupt request is enabled |
| **PLLIR** | **PLL Interrupt Request Flag (OWD Interrupt)**<br>‘0’ No request pending<br>‘1’ This source has raised an interrupt request |
| **PLLIE** | **PLL Interrupt Enable Control Bit**<br>‘0’ Interrupt request is disabled<br>‘1’ Interrupt request is enabled |

*Note: See Data Sheet, Chapter 3.3 for Clock Generation Concept.*

# 4 System Startup Configuration

Page 369.

**Table 91 C161U's Supported Modes and Related Reset Configurations**

| P0L.5: P0L.2 (SMOD) | P0L.1 (ADP) | Selected Mode |
|---|---|---|
| x x x x | 0 | Adapt Mode |
| 1 1 1 1 | 1 | Normal Mode |
| 0 0 0 1 | 1 | ~~Internal Boot-ROM Read-Out~~<br>Not applicable |
| 1 0 1 1 | 1 | Bootstrap-Loader Mode |
| 1 1 0 1 | 1 | ~~Selftest~~<br>Not applicable |

# 5 Interrupt System Structure

Page 109.

*Note:*

1. *The X-Bus interrupts xb(0), xb(1) and xb(2), known from other C16x device's, are connected to the main interrupt node of the respective X-Bus peripheral: UTXRINT (xb(0) and irq(22)), EPECINT (xb(1) and irq(40)) and IOMIOINT (xb(2) and irq(42)).*
2. *Each entry of the interrupt vector table provides space for two word instructions or one doubleword instruction. The respective vector location results from multiplying the trap number by 4 (4 bytes per entry).*
3. *One interrupt control register is provided for each interrupt node. All IC registers of the C161U can be found in the SFR list.*
4. *ISNC register controls the interrupt xb(3). See Data Sheet, Chapter 7.8.3 for further description.*

# 6 Defining the RTC Time Base

Page 296.

Correct values are indicated **blue**.

**Table 67 RTC Interrupt Periods**

| Oscillator Frequency | Divider Factor | RTC Input Frequency | Prescaler Factor | RTC_T14INT Period | |
|---|---|---|---|---|---|
| | | | | Minimum | Maximum |
| 32 kHz | 1 | 32 kHz | | 31.25 µs | 2.048 s |
| 1 MHz | 32 | **31.25 kHz** | 8 | 256.0 µs | 16.77 s |
| 4 MHz | 32 | 125 kHz | 8 | 64.0 µs | 4.194 s |
| 5 MHz | 32 | **156.25 kHz** | 8 | 51.2 µs | 3.355 s |
| 8 MHz | 32 | **250 kHz** | 8 | 32.0 µs | 2.097 s |
| 10 MHz | 32 | 312.5 kHz | 8 | 25.6 µs | 1.678 s |
| 12 MHz | 32 | 375 kHz | 8 | 21.3 µs | 1.398 s |
| 16 MHz | 32 | 500 kHz | 8 | 16.0 µs | 1.049 s |
| 20 MHz | 32 | 625 kHz | 8 | 12.8 µs | 0.839 s |
| 24 MHz | 32 | 750 kHz | 8 | 10.67 µs | 0.699 s |
| 25 MHz | 32 | 781.25 kHz | 8 | 10.24 µs | 0.671 s |
| 32 MHz | 32 | 1 MHz | 8 | 8.0 µs | 0.524 s |
| 50 MHz | 32 | 1.56 MHz | 8 | 5.12 µs | 0.336 s |

**Table 68 RTC Reload Values**

| RTC Input Frequency | Reload Value A | | Reload Value B | | Reload Value C | |
|---|---|---|---|---|---|---|
| | T14REL | Base | T14REL | Base | T14REL | Base |
| 32 kHz | $8300_H$ | 1.000 s | $F380_H$ | 100.0 ms | $FFE0_H$ | 1.000 ms |
| **31.25 kHz** | $F0BE_H$ | 0.999 s | $FE79_H$ | 100.1 ms | $FFFC_H$ | 1.024 ms |
| 125 kHz | $C2F7_H$ | 1.000 s | $F9E5_H$ | 100.0 ms | $FFF0_H$ | 1.024 ms |
| **156.25 kHz** | $B3B5_H$ | 0.999 s | $F85F_H$ | 99.9 ms | $FFEC_H$ | 1.024 ms |
| **250 kHz** | $85EE_H$ | 1.000 s | $F3CB_H$ | 100.0 ms | $FFE1_H$ | 0.992 ms |
| 312.5 kHz | $6769_H$ | 1.000 s | $F0BE_H$ | 99.9 ms | $FFD9_H$ | 0.998 ms |
| 375 kHz | $48E5_H$ | 1.000 s | $EDB0_H$ | 100.0 ms | $FFD1_H$ | 1.003 ms |
| 500 kHz | $0BDC_H$ | 1.000 s | $E796_H$ | 100.0 ms | $FFC1_H$ | 1.008 ms |

**Table 68 RTC Reload Values** (cont'd)

| RTC Input Frequency | Reload Value A | | Reload Value B | | Reload Value C | |
|---|---|---|---|---|---|---|
| | T14REL | Base | T14REL | Base | T14REL | Base |
| 625 kHz | | | $E17B_H$ | 100.0 ms | $FFB2_H$ | 0.998 ms |
| 750 kHz | | | $DB61_H$ | 100.0 ms | $FFA2_H$ | 1.003 ms |
| 781.25 kHz | | | $D9DA_H$ | 100.0 ms | $FF9E_H$ | 1.004 ms |
| 1 MHz | | | $CF2C_H$ | 100.0 ms | $FF83_H$ | 1.000 ms |
| 1.56 MHz | | | $B3B5_H$ | 99.9 ms | $FF3D_H$ | 0.998 ms |