VERSA1: FULLY INTEGRATED MICROCONTROLLER WITH DSP

Datasheet Rev 3.4

1134 Ste Catherine Street West, Suite 900, Montreal, Quebec, Canada H3B 1H4 Tel: (514) 871-2447 http://www.goalsemi.com

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FULLY INTEGRATED MICROCONTROLLER WITH DSP

Overview

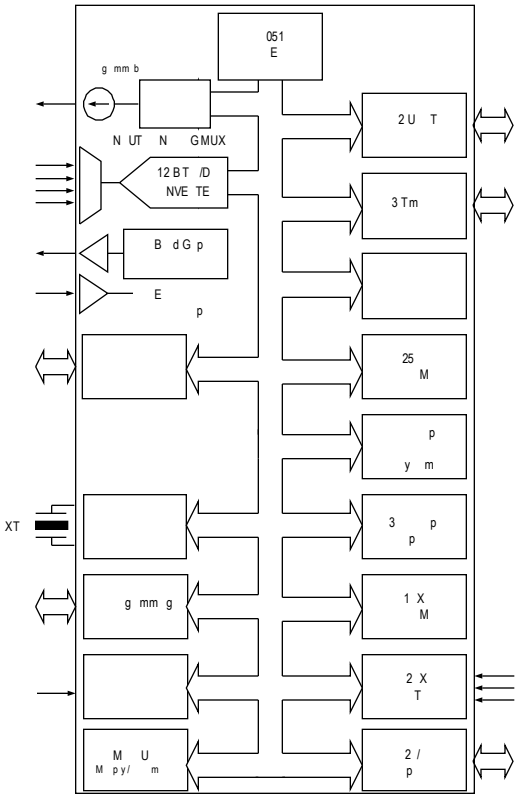
The VERSA1 is a fully integrated microcontroller based data acquisition system that includes a set of non-traditional on-chip components such as a programmable constant current source driver and a MAC block. The current source driver can be used to excite traditional components such as resistive bridges or thermistors. The MAC block allows the user to perform mathematical calculations to a much higher degree of accuracy and speed than standard microcontroller look-up table based methods.

Applications

- Automotive Applications
- Medical Devices
- Industrial Controls / Measurement Systems
- Intelligent Sensors / Instrumentation
- Consumer Products
- Battery Powered Systems (Instruments, Monitors)
- Pattern Recognition

Functional Diagram

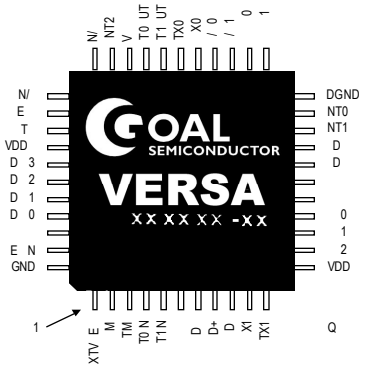
The following figure shows the functional diagram of the VERSA1.



Features

- 8051 Compatible µProcessor
  - Standard 8051 Instruction Set
  - Dual Data Pointers
  - 4 Clocks/Instruction
  - Supports industry standard compilers, assemblers, ROM monitors
- DSP Function via MAC (Multiply/Accumulate Unit)
- On-chip Flash Memory
  - 64Kx8 Program/Storage Memory
  - 2Kx8 OTPR Storage Memory Block
  - In Circuit Flash Programming
- On-chip RAM
  - 256x8 RAM Mapped into Internal RAM
  - 1Kx8 RAM Mapped into External Memory Space
- 4 Channel Calibrated 12-bit A/D Converter
  - 0-2.7 Volts Input Range
  - Programmable Continuous Free-Running Conversion with Interrupt to Processor
  - Programmable One-Shot Conversion mode
- On-Chip Temperature Calibrated Reference Voltage
- Analog Output/Reference Loop-Back
  - Programmable Current Source
- 2 Full Duplex Asynchronous UARTS
- SPI Bus (Master/Slave)
  - 3 Addressable Chip Enable Outputs for Controlling Multiple Slaves (Master Mode)
- 2 General Purpose I/Os
- 3 Interrupt Inputs
- 3 General Purpose Timers/Counters
- Power Saving Features
- Power-on Reset with Brown-Out Detect
- Availlable in Commercial and Industrial temperature versions

VERSA1 Pinout



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Pins Description

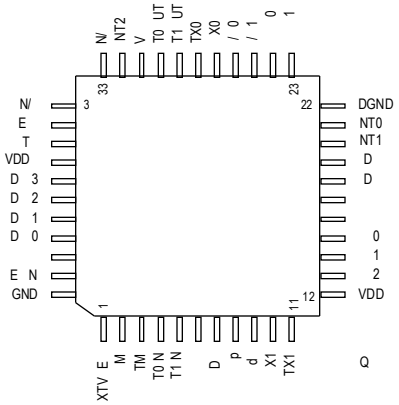
TABLE 1 PIN OUT DESCRIPTION

PIN	NAME	FUNCTION
1	XTVREF	External Reference Voltage Input (optional)
2	PM	Mode Control Input
3	FTM	Mode Control Input
4	T0IN	Timer 0 Input
5	T1IN	Timer 1 Input
6	SCL	Prog. Interface Clock Input
7	SDA	Prog. Interface Bi-directional Data Bus
8	Pup	Put 10K to 100K pull-up to VDD
9	Pdn	Put 10K to 100K pull-down to GND
10	RX1	Asynchronous UART1 Receiver Input
11	TX1	Asynchronous UART1 Transmitter Output
12	VDD	Digital Logic Supply Input
13	CS2-	SPI Chip Enable Output (Master Mode)
14	CS1-	SPI Chip Enable Output (Master Mode)
15	CS0-	SPI Chip Enable Output (Master Mode)
16	SS-	SPI Chip Enable Input (Slave Mode)
17	SCK	SPI Clock (Input in Slave Mode, Output in Master Mode)
18	SDO	SPI Data Output Bus
19	SDI	SPI Data Input Bus
20	INT1-	Interrupt Input (Negative Level Triggered)
21	INT0-	Interrupt Input (Negative Level or Edge Triggered)
22	DGND	Digital Ground
23	OSC1	Oscillator Crystal Output
24	OSC0	Oscillator Crystal Input/External Clock Source Input
25	I/O1	Programmable I/O
26	I/O0	Programmable I/O
27	RX0	Asynchronous UART0 Receiver Input
28	TX0	Asynchronous UART0 Transmitter Output
29	T1OUT	Timer 1 Output
30	T0OUT	Timer 0 Output

PIN	NAME	FUNCTION
31	VPP	Flash Programming Voltage Input
32	INT2	Interrupt Input (Positive Edge Triggered)
33	N/C	No Connection (leave pin unconnected)
34	N/C	No Connection (leave pin unconnected)
35	RES-	Hardware Reset Input
36	TA	Analog Output
37	VDDA	Analog Supply Input
38	ADCI3	Analog Input for Channel 3
39	ADCI2	Analog Input for Channel 2
40	ADCI1	Analog Input for Channel 1
41	ADCI0	Analog Input for Channel 0
42	ISRC	Programmable Current Source Output
43	RESIN	Current Source Reference Input
44	AGND	Analog Ground

Pin Configuration

FIGURE 1 VERSA1 PINOUT



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Absolute Maximum Ratings

V_{DD} to DGND	–0.3V, +6V	Digital Output Voltage to DGND	–0.3V, V_{DD}+0.3V
V_{DDA} to DGND	-0.3V, +6V	V_{PP} to DGND	+13V
AGND to DGND	–0.3V, +0.3V	Power Dissipation	
V_{DD} to V_{DDA}	-0.3V, +0.3V	○ To +75°C	1000mW
ADCI (0-3) to AGND	-0.3V, V_{DDA}+0.3V	○ Derate above +75°C	10mW/°C
XTVREF to AGND	-0.3V, V_{DDA}+0.3V	Operating Temperature range	-40° to +85°C
Digital Input Voltage to DGND	-0.3V, V_{DD}+0.3V	Storage Temperature Range	–65°C to +150°C
		Lead Temperature (soldering, 10sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

TABLE 2 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS (V_{DD} = +5V, V_{DDA} = +5V, T_A = +25°C, 16MHz input clock, unless otherwise noted.)						
Power Supply Voltage	V_{DD}		4.75	5.0	5.5	V
	V_{DDA}		4.75	5.0	5.5	V
V_{DDA} Power Supply Rejection						
Power Supply Current	I_{DD}		5.5	-	12.5	mA
	I_{DDA}		2.5	-	7.5	
Flash Programming Voltage	V_{PP}			+12		V
DIGITAL INPUTS						
Minimum High-Level Input Voltage	V_{IH}	V_{DD} = +5V		2.0		V
Maximum Low-Level Input Voltage	V_{IL}	V_{DD} = +5V		0.8		V
Input Current	I_{IN}			±0.05		µA
Input Capacitance	C_{IN}			5	10	pF
DIGITAL OUTPUTS						
Minimum High-Level Output Voltage	V_{OH}	I_{SOURCE} = 4mA		4.2		V
Maximum Low-Level Output Voltage	V_{OL}	I_{SINK} = 4mA		0.2		V
Output Capacitance	C_{OUT}			10	15	pF
Tri-state Output Leakage Current	I_{OZ}				0.25	µA
POWER SUPPLY MONITOR						
V_{DD} Trip Point	V_{TRIP}			3.75		V
ANALOG INPUTS						
ADCI(0-3) Input Voltage Range	V_{ADCI}		0		2.7	V
ADCI(0-3) Input Resistance	R_{ADCI}			100		MOhms
ADCI(0-3) Input Capacitance	C_{ADCI}			5		pF
ADCI(0-3) Input Leakage Current	I_{ADCI}			TBD		nA
Channel-to-Channel Crosstalk				TBD		dB

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ANALOG OUTPUT						
TA Output Voltage (Note 1)	$V_{TA=}V_{BGH}$		1.179		1.23	V
TA Output Drive Capabilities (Maximum Load Resistance)	$V_{TA=}V_{BGH)}$		10			kOhms
CURRENT SOURCE						
ISRC Current Drive	I_{ISRC}	(Note 2, Note 3)		33/133	530uA	µA
ISRC Output Resistance	R_{ISRC}			50		MOhms (Design)
ISRC Output Capacitance	C_{ISRC}			25		PF (Design)
RESIN Input Ref Resistance	R_{RESIN}			100		MOhms (Design)
ISRC Reference Voltage (low)	$V_{resinLow}$		195	200	205	MV (Design)
ISRC Reference Voltage (high)	$V_{resinHigh}$		792	800	808	MV (Design)
RESIN Input Reference Capacitance	C_{RESIN}			7		PF (Design)
INTERNAL REFERENCE						
Bandgap Reference Voltage (1st order)			1.05		1.21	V
Bandgap Reference Voltage (2st order) (Calibration value)			1.07		1.24	V
Bandgap Reference Tempco			10		20	ppm/°C
EXTERNAL REFERENCE						
Input Impedance	R_{XTVREF}			100		MOhms (Design)
PGA						
PGA Gain adjustment			2.15		2.35	

PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG TO DIGITAL CONVERTER						
ADC Resolution				12		Bits
Differential Non linearity	DNL				±10	LSB
Integral Non linearity	INL				±1	LSB
Full-Scale Error (Gain Error)		All channels, ADCI(0-3)		±4		LSB
Offset Error		All channels, ADCI(0-3)		±0.5		LSB
Channel-to-Channel Mismatch		All channels, ADCI(0-3)		±0.5		LSB
Conversion Time		4 channels			1.75	ms
		Single Channel			0.5	

Note 1: TA is the output of an analog multiplexer that can be programmed to switch through one of eight analog inputs -$V_{ADCI(0-3)}$, V_{BGI}, V_{BGH}, V_{ADC} and V_{SR}, which correspond to the 4 analog inputs to the VERSA1, on-chip Bandgap reference, a buffered on-chip reference, on-chip ADC reference and current source reference, respectively.

Note 2: The on-chip current source can be programmed to provide 2 current values using the calibrated internal Bandgap reference and a 6.00k precision feedback resistor between RESIN and analog Ground.

Note 3: The Feedback resistor between RESIN and analog Ground can be lowered to 1.5k resulting in an ISRC maximum output of about 530uA. In such conditions, the resistive element between ISRC output and RESIN should have > 1k in value.

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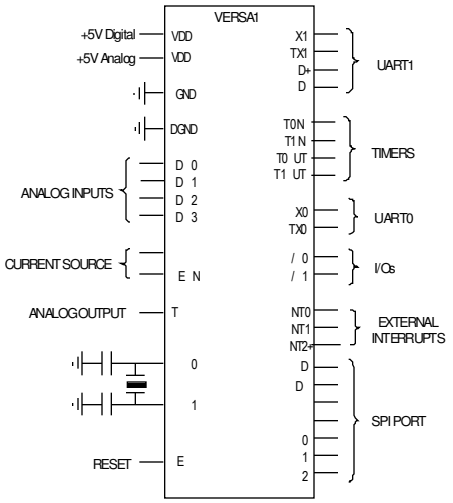
Detailed Description

The following sections will describes the VERSA1 Architecture and peripherals.

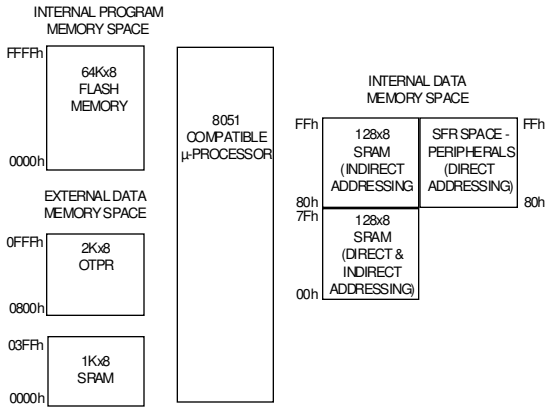
FIGURE 2 OPERATIONAL DIAGRAM FOR THE VERSA1



Memory Organization

The following figure shows the memory organization of the VERSA1.

FIGURE 3 MEMORY ORGANIZATION OF THE VERSA1

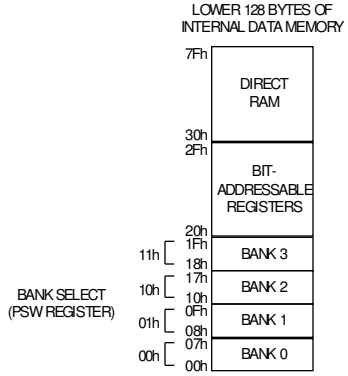


At power-up/reset code is executed from the 64Kx8 Flash memory mapped into the processor's internal ROM space. An extra 2Kx8 of Secondary Flash memory is mapped into the external data memory space.

Note that 0000–0005h and 0195–0210h are reserved in the OTPR. A 1Kx8 block of SRAM is also mapped into the external data memory of the VERSA1. This block can be used as general-purpose scratch pad or storage memory. A 256x8 block of SRAM is mapped to the internal data memory space. This block of RAM is broken into 2 sub-blocks, with the upper block accessible via indirect addressing only, and the lower block accessible via both direct and indirect addressing.

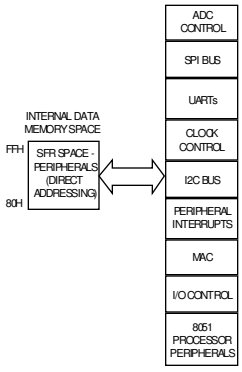
The following figure describes access to the lower block of 128 bytes.

FIGURE 4 LOWER BLOCK INTERNAL MEMORY MAP



The SFR (Special Function Register) space is also mapped into the upper 128 bytes of internal data memory space. This SFR space is accessible via direct-access only. The SFR space provides the interface to all the on-chip peripherals. The following figure describes this interface.

FIGURE 5 SFR SPACE ORGANIZATION



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Dual Data Pointers

The VERSA1 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The VERSA1 maintains the standard data pointer as DPTR0 at SFR locations 82h and 83h. It is not necessary to modify the code to use DPTR0.

The VERSA1 adds a second data pointer (DPTR1) at SFR locations 84h and 85h. The SEL bit in the DPTR Select register, DPS (SFR 86h), selects the active pointer. When SEL = 0, instructions that use the DPTR will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL 1 and DPH1. SEL is the bit 0 of SFR location 86h. No other bits of SFR location 86h are used.

All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address; saving application code from having to save source and destination addresses when doing a block move. Using dual data pointers provides significantly increased efficiency when moving large blocks of data. The SFR locations related to the dual data pointers are:

TABLE 3 DUAL DATA POINTER SFR ADDRESSES

SFR Address	Mnemonic	Description
82h	DPL0	DPTR0 low byte
83h	DPH0	DPTR0 high byte
84h	DPL1	DPTR 1 low byte
85h	DPH1	DPTR 1 high byte
86h	DPS	DPTR Select (LSB)

Programming interface

The Flash Programming Interface on the VERSA1 is a slave based and has 3 specific functions

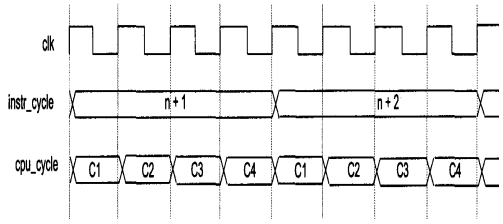
- Act as a port where all the on-chip peripherals (not including the processor) can be accessed for debugging and test purposes.
- Act as a slave port for applications where the processor is not needed and only the VERSA1 peripherals are used and accessed.

CPU Timing

As previously stated, a VERSA1 instruction cycle consists of 4 clock cycles. Each system clock cycle forms a CPU cycle. Therefore, an instruction cycle consists of 4 CPU cycles: C1, C2, C3, and C4, as illustrated in **Figure 7**, various events occur in each CPU cycle, depending on the type of instruction being executed. Throughout this datasheet, the labels C1, C2, C3, and C4 in timing descriptions refer to the 4 CPU cycles within a particular instruction cycle.

Note that a system clock (clk) is referred as (Fosc / 2).

FIGURE 7 CPU TIMING FOR SINGLE-CYCLE INSTRUCTION



Instruction Timing

Instruction cycles in the VERSA1 are 4 system clock cycles in length, as opposed to the 12 clock cycles per instruction cycle in the standard 8051. This translates to a 3X improvement in execution time for most instructions. However, some instructions require a different number of instruction cycles on the VERSA1 than they do on the standard 8051. In the standard 8051, all instructions except for `MUL` and `DIV` take one or two instruction cycles to complete. In the VERSA1 architecture, instructions can take between one and five instruction cycles to complete.

For example, in the standard 8051, the instructions `MOVX A, @DPTR` and `MOV direct, direct` each take 2 instruction cycles (24 clock cycles) to execute. In the VERSA1 architecture, `MOVX A, @DPTR` takes two instruction cycles (8 system clock cycles) and `MOV direct, direct` takes three instruction cycles (12 clock cycles). Both instructions execute faster on the VERSA1 than they do on the standard 8051, but require different numbers of clock cycles.

For timing of real-time events, use the number of instruction cycles from **Table 5** to calculate the timing of software loops. The size column of **Table 5** indicates the number of memory accesses (bytes) needed to execute the instruction. In most cases, the number of bytes is equal to the number of instruction cycles required to complete the instruction. However, as indicated in **Table 5**, there are some instructions (for example, `DIV` and `MUL`) that require a greater number of instruction cycles than memory accesses.

By default, the VERSA1 timer/counters run at 12 system clock cycles per increment so that timer-based events have the same timing as with the standard 8051. The timers can be configured to run at 4 system clock cycles per increment to take advantage of the higher speed of the VERSA1.

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Performance Overview

The VERSA1 provides increased performance by executing instructions in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the standard 8051. The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures.

The average speed improvement for the entire instruction set is approximately 2.5X, calculated as follows:

Number of Op codes	Speed Improvement
150	3.0X
51	1.5X
43	2.0X
2	2.4X
Total: 255	Average: 2.5X
Note: Comparison is for VERSA1 and standard 8051 running at the same system clock frequency.	

There is not an exact 3X improvement in speed because some instructions require a different number of instruction cycles on the VERSA1 than they do on the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the VERSA1 architecture, instructions can take between one and five instruction cycles to complete. However, because of the 3X faster instruction cycle time, the average speed improvement for all instructions is 2.5X.

Instruction Set

All VERSA1 instructions are binary code compatible and perform the same functions that they do in the industry standard 8051. The effects of these instructions on bits, flags, and other status functions are identical to the industry standard 8051. However, the timing of the instructions is different, both in terms of number of clock cycles per instruction cycle and timing within the instruction cycle.

Table* 4** defines the symbols and mnemonics used in ***Table 5

Table 5 lists the VERSA1 instruction set and the number of system clock cycles required to complete each instruction.

TABLE 4 LEGEND FOR INSTRUCTION SET TABLE

Symbol	Function
A	Accumulator
Rn	Register R0-R7
Direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

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TABLE 5 VERSA1 INSTRUCTION SET

Mnemonic	Description	Size (bytes)	Instr. Cycles	Hex Code
Arithmetic instructions				
ADD A, Rn	Add register to A	1	1	28-2Fh
ADD A, direct	Add direct byte to A	2	2	25h
ADD A, @Ri	Add data memory to A	1	1	26-27h
ADD A, #data	Add immediate to A	2	2	24h
ADDC A, Rn	Add register to A with carry	1	1	38-3Fh
ADDC A, direct	Add direct byte to A with carry	2	2	35h
ADDC A, @Ri	Add data memory to A with carry	1	1	36-37h
ADDC A, #data	Add immediate to A with carry	2	2	34h
SUBB A, Rn	Subtract register from A with borrow	1	1	98-9Fh
SUBB A, direct	Subtract direct byte from A with borrow	2	2	95h
SUBB A, @Ri	Subtract data memory from A with borrow	1	1	96-97h
SUBB A, #data	Subtract immediate from A with borrow	2	2	94h
INC A	Increment A	1	1	04h
INC Rn	Increment register	1	1	08-0Fh
INC direct	Increment direct byte	2	2	05h
INC @Ri	Increment data memory	1	1	06-07h
DEC A	Decrement A	1	1	14h
DEC Rn	Decrement register	1	1	18-1Fh
DEC direct	Decrement direct byte	2	2	15h
DEC @Ri	Decrement data memory	1	1	16-17h
INC DPTR	Increment data pointer	1	3	A3h
MUL AB	Multiply A by B	1	5	A4h
DIV AB	Divide A by B	1	5	84h
DA A	Decimal adjust A	1	1	D4h

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Mnemonic	Description	Size (bytes)	Instr. Cycles	Hex Code
Logical Instructions				
ANL A, Rn	AND register to A	1	1	58-5Fh
ANL A, direct	AND direct byte to A	2	2	55h
ANL A, @Ri	AND data memory to A	1	1	56-57h
ANL A, #data	AND immediate to A	2	2	54h
ANL direct, A	AND A to direct byte	2	2	52h
ANL direct, #data	AND immediate data to direct byte	3	3	53h
ORL A, Rn	OR register to A	1	1	48-4Fh
ORL A, direct	OR direct byte to A	2	2	45h
ORL A, @Ri	OR data memory to A	1	1	46-47h
ORL A, #data	OR immediate to A	2	2	44h
ORL direct, A	OR A to direct byte	2	2	42h
ORL direct, #data	OR immediate data to direct byte	3	3	43h
XRL A, Rn	Exclusive-OR register to A	1	1	68-6Fh
XRL A, direct	Exclusive-OR direct byte to A	2	2	65h
XRL A, @Ri	Exclusive-OR data memory to A	1	1	66-67h
XRL A, #data	Exclusive-OR immediate to A	2	2	64h
XRL direct, A	Exclusive-OR A to direct byte	2	2	62h
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3	63h
CLR A	Clear A	1	1	E4h
CPL A	Compliment A	1	1	F4h
SWAP A	Swap nibbles of A	1	1	C4h
RLA	Rotate A left	1	1	23h
RLC A	Rotate A left through carry	1	1	33h
RRA	Rotate A right	1	1	03h
RRCA	Rotate A right through carry	1	1	13h

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Mnemonic	Description	Size (bytes)	Instr. Cycles	Hex Code
Data Transfer Instructions				
MOV A, Rn	Move register to A	1	1	E8-EFh
MOV A, direct	Move direct byte to A	2	2	E5h
MOV A, @Ri	Move data memory to A	1	1	E6-E7h
MOV A, #data	Move immediate to A	2	2	74h
MOV Rn, A	Move A to register	1	1	F8-FFh
MOV Rn, direct	Move direct byte to register	2	2	A8-AFh
MOV Rn, #data	Move immediate to register	2	2	78-7Fh
MOV direct, A	Move A to direct byte	2	2	F5h
MOV direct, Rn	Move register to direct byte	2	2	88-8Fh
MOV direct, direct	Move direct byte to direct byte	3	3	85h
MOV direct, @Ri	Move data memory to direct byte	2	2	86-87h
MOV direct, #data	Move immediate to direct byte	3	3	75h
MOV @Ri, A	Move A to data memory	1	1	F6-F7h
MOV @Ri, direct	Move direct byte to data memory	2	2	A6-A7h
MOV @Ri, #data	Move immediate to data memory	2	2	76-77h
MOV DPTR, #data	Move immediate to data pointer	3	3	90h
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3	93h
MOVC A, @A+PC	Move code byte relative PC to A	1	3	83h
MOVX A, @Ri	Move external data (A8 or A16 if MPAGE) to A	1	3	E2-E3h
MOVX A, @DPTR	Move external data (A 16) to A	1	3	E0h
MOVX @Ri, A	Move A to external data (A8 or A16 if MPAGE)	1	3	F2-F3h
MOVX @DPTR, A	Move A to external data (A 16)	1	3	F0h
PUSH direct	Push direct byte onto stack	2	2	C0h
POP direct	Pop direct byte from stack	2	2	D0h
XCH A, Rn	Exchange A and register	1	1	C8-CFh
XCH A, direct	Exchange A and direct byte	2	2	C5h
XCH A, @Ri	Exchange A and data memory	1	1	C6-C7h
XCHD A, @Ri	Exchange A and data memory nibble	1	1	D6-D7h

Mnemonic	Description	Size (bytes)	# Cycles	Hex Code
Branching Instructions				
ACALL addr 11	Absolute call to subroutine	2	3	11-F1h
LCALL addr 16	Long call to subroutine	3	4	12h
RET	Return from subroutine	1	4	22h
RETI	Return from interrupt	1	4	32h

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Mnemonic	Description	Size (bytes)	# Cycles	Hex Code
AJMP addr 11	Absolute jump unconditional	2	3	01-E1h
LJMP addr 16	Long jump unconditional	3	4	02h
SJMP rel	Short jump (relative address)	2	3	80h
JC rel	Jump on carry = 1	2	3	40h
JNC rel	Jump on carry = 0	2	3	50h
JB bit, rel	Jump on direct bit = 1	3	4	20h
JNB bit, rel	Jump on direct bit = 0	3	4	30h
JBC bit, rel	Jump on direct bit = 1 and clear	3	4	10h
JMP @A+DPTR	Jump indirect relative DPTR	1	3	73h
JZ rel	Jump on accumulator = 0	2	3	60h
JNZ rel	Jump on accumulator 1= 0	2	3	70h
CJNE A, direct, rel	Compare A, direct JNE relative	3	4	B5h
CJNE A, #d, rel	Compare A, immediate JNE relative	3	4	B4h
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	4	B8-BFh
CJNE @Ri, #d, rel	Compare ind, immediate JNE relative	3	4	B6-B7h
DJNZ Rn, rel	Decrement register, JNZ relative	2	3	D8-DFh
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4	D5h
Miscellaneous Instruction				
NOP	No operation	1	1	00h
There is an additional reserved opcode (A5) that performs the same function as NOP.				
All mnemonics are copyright © Intel Corporation 1980.				

Mnemonic	Description	Size (bytes)	# Cycles	Hex Code
Boolean Instructions				
CLR C	Clear carry	1	1	C3h
CLR bit	Clear direct bit	2	2	C2h
SETB C	Set carry	1	1	D3h
SETB bit	Set direct bit	2	2	D2h
CPL C	Complement carry	1	1	B3h
CPL bit	Complement direct bit	2	2	B2h
ANL C, bit	AND direct bit to carry	2	2	82h
ANL C, /bit	AND direct bit inverse to carry	2	2	B0h
ORL C, bit	OR direct bit to carry	2	2	72h
ORL C, /bit	OR direct bit inverse to carry	2	2	A0h
MOV C, bit	Move direct bit to carry	2	2	A2h
MOV bit, C	Move carry to direct bit	2	2	92h

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Peripheral Interfaces

Special Function Registers

The Special Function Registers (SFRs) control several of the features of the VERSA1. Most of the VERSA1 SFRs are identical to the standard 8051 SFRs. However, there are additional SFRs that control features that are not available in the standard 8051.

Table 6 lists the VERSA1 SFRs and indicates which SFRs are not included in the standard 8051 SFR space. When writing software for the VERSA1, use equate statements to define the SFRs that are specific to the VERSA1. SFR bit positions that contain a 0 or a 1 cannot be written to and, when read, always return the value shown (0 or 1). SFR bit positions that contain "-" are available but not used. The last column of **Table 6** shows the reset value of VERSA1 SFRs.

TABLE 6 SPECIAL FUNCTION REGISTERS

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
SP	81h	-	-	-	-	-	-	-	-	0000 0111b
DPL0	82h	-	-	-	-	-	-	-	-	0000 0000b
DPH0	83h	-	-	-	-	-	-	-	-	0000 0000b
DPL1	84h	-	-	-	-	-	-	-	-	0000 0000b
DPH1	85h	-	-	-	-	-	-	-	-	0000 0000b
DPS	86h	0	0	0	0	0	0	0	SEL	0000 0000b
PCON	87h	SMOD0	0	1	1	GF1	GF0	0	0	0011 0000b
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0000 0000b
TMOD	89h	GATE	C/!T	M1	M0	GATE	C/!T	M1	M0	0000 0000b
TL0	8Ah	-	-	-	-	-	-	-	-	0000 0000b
TL1	8Bh	-	-	-	-	-	-	-	-	0000 0000b
TH0	8Ch	-	-	-	-	-	-	-	-	0000 0000b
TH1	8Dh	-	-	-	-	-	-	-	-	0000 0000b
CKCON	8Eh	0	0	T2M	T1M	T0M	0	0	1	0000 0001b
SPC_FNC	8Fh	0	0	0	0	0	0	0	WRS	0000 0000b
EXIF	91h	-	-	IE3	IE2	1	0	0	0	0000 1000b
MPAGE	92h	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	0000 0000b
ADCCTRL	94h	SV0	MANUAL	ONESHOT	ADCENABLE	ADCIC	ADCIE	CONT	BGENABLE	0000 0000b
BGAPCAL	95h	-	-	-	-	-	-	-	-	0000 0000b
ADCALADR	96h	0	0	0	CALDSBL	CALADR3	CALADR2	CALADR1	CALADR0	0000 0000b
ADCALDAT	97h	0	0	0	DTBL4	DTBL3	DTBL2	DTBL1	DTBL0	0000 0000b
SCON0	98h	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	0000 0000b
SBUF0	99h	-	-	-	-	-	-	-	-	0000 0000b
ADCSTAT	9Ch	0	0	0	0	0	0	0	ADCINT	0000 0000b
ADCD0LO	A4h	ADCD7_0	ADCD6_0	ADCD5_0	ADCD4_0	ADCD3_0	ADCD2_0	ADCD1_0	ADCD0_0	0000 0000b
ADCD0HI	A5h	0	0	0	0	ADCD11_0	ADCD10_0	ADCD9_0	ADCD8_0	0000 0000b
ADCD1LO	A6h	ADCD7_1	ADCD6_1	ADCD5_1	ADCD4_1	ADCD3_1	ADCD2_1	ADCD1_1	ADCD0_1	0000 0000b
ADCD1HI	A7h	0	0	0	0	ADCD11_1	ADCD10_1	ADCD9_1	ADCD8_1	0000 0000b
IE	A8h	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	0000 0000b
ADCD2LO	ACh	ADCD7_2	ADCD6_2	ADCD5_2	ADCD4_2	ADCD3_2	ADCD2_2	ADCD1_2	ADCD0_2	0000 0000b
ADCD2HI	ADh	0	0	0	0	ADCD11_2	ADCD10_2	ADCD9_2	ADCD8_2	0000 0000b
ADCD3LO	AEh	ADCD7_3	ADCD6_3	ADCD5_3	ADCD4_3	ADCD3_3	ADCD2_3	ADCD1_3	ADCD0_3	0000 0000b
ADCD3HI	AFh	0	0	0	0	ADCD11_3	ADCD10_3	ADCD9_3	ADCD8_3	0000 0000b
SPICTRL	B4h	0	0	SPICSS_1	SPI_CSS_0	SPIMCLK_1	SPIMCLK_0	SPICLKP	SPIMA_SL	0000 0000b
SPIRX	B5h	-	-	-	-	-	-	-	-	0000 0000b
SPITX	B6h	-	-	-	-	-	-	-	-	0000 0000b
SPIIE	B7h	0	0	0	0	0	SPIRXOVIE	SPIRXDAIE	SPITXEMPIE	0000 0000b
IP	B8h	1	0	0	PS0	PT1	PX1	PT0	PX0	1000 0000b
IOCTRL	BAh	0	0	0	0	IODIRCTRL 1	IOOUT1	IODIRCTRL0	IOOUT0	0000 0000b

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SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Value
IOREAD	BBh	0	0	0	0	0	0	IOREAD1	IOREAD0	0000 0000b
SPIINTSTAT	BCh	0	0	0	0	0	SPIRXOV	SPIRXDA	SPITXEMP	0000 0000b
SPIRXOVC	BDh	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	0000 0000b
SCON1	C0h	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	0000 0000b
SBUF1	C1h	-	-	-	-	-	-	-	-	0000 0000b
MACACC0*	C4h	-	-	-	-	-	-	-	-	0000 0000b
MACACC1*	C5h	-	-	-	-	-	-	-	-	0000 0000b
MACACC2*	C6h	-	-	-	-	-	-	-	-	0000 0000b
MACACC3*	C7h	-	-	-	-	-	-	-	-	0000 0000b
T2CON	C8h	TF2	FIRQT2	RCLK	TCLK	0	TR2	0	-RL2	0000 0000b
RCAP2L	CAh	-	-	-	-	-	-	-	-	0000 0000b
RCAP2H	CBh	-	-	-	-	-	-	-	-	0000 0000b
TL2	CCh	-	-	-	-	-	-	-	-	0000 0000b
TH2	CDh	-	-	-	-	-	-	-	-	0000 0000b
PSW	D0h	CY	AC	F0	RS1	RS0	OV	F1	P	0000 0000b
S1ACTIVATEL	D7h	S1EN	0	0	0	0	1	0	0	0000 0100b
EICON	D8h	SMOD1	1	EPFI	PFI	EXT2	0	0	0	0100 0000b
Reserved	D9h	-	-	-	-	-	-	-	-	0000 0000b
Reserved	DAh	-	-	-	-	-	-	-	-	1111 1111b
Reserved	DBh	-	-	-	-	-	-	-	-	1111 1111b
Reserved	DCh	-	-	-	-	-	-	-	-	1111 1111b
Reserved	DDh	-	-	-	-	-	-	-	-	0000 0000b
Reserved	DEh	0	0	0	0	-	-	-	-	0000 0000b
Reserved	DFh	0	0	-	-	-	-	-	-	0000 0000b
ACC	E0h	-	-	-	-	-	-	-	-	0000 0000b
INTSRC	E4h	-	-	-	-	-	-	-	-	0000 0000b
CLKDIV	E5h	0	0	0	0	DIVCTL_2	DIVCTL_1	DIVCTL_0	NORMSPD	0000 0000b
MACA0*	E6h	-	-	-	-	-	-	-	-	0000 0000b
MACA1*	E7h	-	-	-	-	-	-	-	-	0000 0000b
EIE	E8h	1	1	1	EIE2	0	0	EX3	EX2	1110 0000b
MACRES0*	EAh	-	-	-	-	-	-	-	-	0000 0000b
MACRES1*	EBh	-	-	-	-	-	-	-	-	0000 0000b
MACRES2*	ECh	-	-	-	-	-	-	-	-	0000 0000b
MACRES3*	EDh	-	-	-	-	-	-	-	-	0000 0000b
MACB0*	EEh	-	-	-	-	-	-	-	-	0000 0000b
MACB1*	EFh	-	-	-	-	-	-	-	-	0000 0000b
B	F0h	-	-	-	-	-	-	-	-	0000 0000b
CONVRLO	F5h	-	-	-	-	-	-	-	-	0000 0000b
CONVRMED	F6h	-	-	-	-	-	-	-	-	0000 0000b
CONVRHI	F7h	-	-	-	-	-	-	-	-	0000 0000b
EIP	F8h	1	1	1	PEI2	0	0	PEX3	PEX2	1110 0000b
PGACTRL	F9h	DPGA6	DPGA5	DPGA4	DPGA3	DPGA2	DPGA1	DPGA0	PGAENABLE	0000 0000b
ISRC1	FAh	C1_6	C1_5	C1_4	C1_3	C1_2	C1_1	C1_0	ISRCENABLE	0000 0000b
ISRC2	FBh	C4_6	C4_5	C4_4	C4_3	C4_2	C4_1	C4_0	SV1	0000 0000b
INMUX	FCh	BGAPORDER	MUXCTRL_2	MUXCTRL_1	MUXCTRL_0	IBUFEN_3	IBUFEN_2	IBUFEN_1	IBUFEN_0	0000 0000b
OUTMUX	FDh	0	0	0	-	MUXB_2	MUXB_1	MUXB_0	TAENABLE	0000 0000b
ADCCkDIV	FEh	-	-	-	-	-	-	-	-	0000 0000b

Notes: *These registers are write only, **These registers are read only

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The following SFRs are related to CPU operation and program execution:

81h	SP	Stack Pointer
D0h	PSW	Program Status Word (**Table 7**)
E0h	ACC	Accumulator Register
F0h	B	B Register

Table 7 lists the functions of the bits in the PSW SFR. Detailed descriptions of the remaining SFRs appear with the associated hardware descriptions in Chapter 3 of this datasheet.

TABLE 7 PSW REGISTER -SFR D0H

Bit #	Mnemonic	Function
7	CY	Carry flag. Set to 1 when the last arithmetic operation resulted in a carry (during addition) or borrow (during subtraction), otherwise cleared to 0 by all arithmetic operations.
6	AC	Auxiliary carry flag. Set to 1 when the last arithmetic operation resulted in a carry into (during addition) or borrow from (during subtraction) the high order nibble, otherwise cleared to 0 by all arithmetic operations.
5	F0	User flag 0. Bit-addressable, general purpose flag for software control.
4	RS1	Register bank select bits used to select a register bank in internal RAM RS1 RS0 0 0 Register bank 0, addresses 00h-07h 0 1 Register bank 0, addresses 08h-0Fh 1 0 Register bank 0, addresses 10h-17h 1 1 Register bank 0, addresses 18h-1Fh
3	RS0	
2	OV	Overflow flag. Set to 1 when the last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide). Otherwise, the bit cleared to 0 by all arithmetic operations.
1	F1	User flag 1. Bit-addressable, general purpose flag for software control.
0	P	Parity flag. Set to 1 when the modulo-2 sum of the 8-bits in the accumulator is 1 (odd parity), cleared to 0 on even parity.

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Timers/Counters

The VERSA1 includes three timer/counters (Timer 0, Timer 1and Timer 2). Timer 0 and Timer 1 can operate as either a timer with a clock rate based on the system clock, or as an event counter clocked by the T0IN (Timer 0) and T1IN (Timer 1). Timer 2 can only operate in 16-bits timer mode. It can serve as serial port baud rate generator.
Each timer/counter consists of a 16-bit register that is accessible by software as two SFRs:

- **Timer 0** -TL0 and TH0
- **Timer 1** -TL1 and TH1
- **Timer2** -TL2 and TH2

Timers 0 and 1

Timers 0 and 1 each operate in four modes, as controlled through the TMOD SFR (**Table 8**) and the TCON SFR (**Table 10**). The four modes are:

- **13-bit** timer/counter (mode 0)
- **16-bit** timer/counter (mode 1)
- **8-bit** counter with auto-reload (mode 2)
- **Two** 8-bit counters (mode 3)

TABLE 8 TMOD REGISTER -SFR 89H

Bit #	Mnemonic	Function
7	GATE_1	Timer 1 gate control. When GATE_1 = 1, Timer 1 will clock only when INT1- = 1 and TR1 (TCON.6) = 1. When GATE_1 = 0, Timer 1 will clock only when TR1 = 1, regardless of the state of INT1-.
6	C/!T_1	Counter/Timer select. When C/!T_1 = 0, Timer 1 is clocked by clk/4 or clk/12, depending on the state of T1M (CKCON.4). When C/!T_1 = 1, Timer 1 is clocked by T1IN.
5	M1_1	Timer 1 mode select bit 1
4	M0_1	Timer 1 mode select bit 0
3	GATE_0	Timer 0 gate control. When GATE_0 = 1, Timer 0 will clock only when intperiph_n = 1 and TR0 (TCON.4) = 1. When GATE_0 = 0, Timer 0 will clock only when TR0 = 1, regardless of the state of intperiph_n.
2	C/!T_0	Counter/Timer select. When C/!T_0 = 0, Timer 0 is clocked by clk/4 or clk/12, depending on the state of T0M (CKCON.3). When C/!T_0 = 1, Timer 0 is clocked by T0IN.
1	M1_0	Timer 0 mode select bit 1
0	M0_0	Timer 0 mode select bit 0

The following table describes the different modes of operation for M1_x and M0_x mode select pins for Timer 0 and Timer 1.

TABLE 9 TIMER0 / TIMER 1 MODES

M1_x	M0_x	Mode
0	0	Mode 0: 13-bit counter
0	1	Mode 1: 16-bit counter
1	0	Mode 2: 8-bit counter with auto-reload
1	1	Mode 3: Two 8-bit counters

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TABLE 10 TCON REGISTER SFR 88H

Bit #	Mnemonic	Function
7	TF1	Timer 1 overflow flag. This flag is set to 1 when the Timer 1 count overflows. It is cleared when the microcontroller executes the interrupt service routine.
6	TR1	Timer 1 run control bit. Set this bit to 1 to enable Timer 1 counting.
5	TF0	Timer 0 overflow flag. This flag is set to 1 when the Timer 0 count overflows. It is cleared when the microcontroller executes the interrupt service routine.
4	TR0	Timer 0 run control bit. Set this bit to 1 to enable Timer 0 counting.
3	IE1	Interrupt 1 edge detect. If external interrupt 1 is configured to be edge-sensitive (IT1 = 1), IE1 is set by hardware when a negative edge is detected on the INT1- pin and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In edge-sensitive mode, IE1 can also be cleared by software. If external interrupt 1 is configured to be level-sensitive (IT1 = 0), IE1 is set when the INT1- pin is low and cleared when the INT1- pin is high. In level-sensitive mode, software cannot write to IE1.
2	IT1	Interrupt 1 type select. When IT1 = 1, the VERSA1 detects INT1- on the falling edge (edge-sensitive). When IT1 = 0, the VERSA1 detects INT1- as a low level (level-sensitive).
1	IE0	Peripheral Interrupt edge detect. If peripheral interrupt is configured to be edge-sensitive (IT0 = 1), IE0 is set by hardware when a negative edge is detected on the intperiph_n input and is automatically cleared when the CPU vectors to the corresponding interrupt service routine. In edge-sensitive mode, IE0 can also be cleared by software. If peripheral interrupt is configured to be level-sensitive (IT0 = 0), IE0 is set when the intperiph_n input is low and cleared when the intperiph_n input is high. In level-sensitive mode, software cannot write to IE0.
0	IT0	Peripheral Interrupt type select. When IT0 = 1, the VERSA1 detects intperiph_n on the falling edge (edge-sensitive). When IT0 = 0, the VERSA1 detects intperiph_n as a low level (level-sensitive).

Mode 0

Mode 0 operation, illustrated in **Figure 8**, is the same for Timer 0 and Timer 1. In mode 0, the timer is configured as a 13-bit counter that uses bits 0-4 of TL0 (or TL 1) and all 8-bits of TH0 (or TH1). The timer enable bit (TR0/TR1) in the TCON SFR starts the timer. The C/!T bit selects the timer/counter clock source, clk or T0IN/T1IN.

The timer counts transitions from the selected source as long as the GATE bit is 0, or the GATE bit is 1 and the corresponding interrupt pin (intperiph_n or INT1-) is deasserted. Please refer to the Interrupts section for a better understanding of how the interrupts are handled in the VERSA1.

When the 13-bit count increments from 1FFFh (all ones), the counter rolls over to all zeros, the TF0 (or TF1) bit is set in the TCON SFR, and the T0OUT (or T1OUT) pin goes high for one clock cycle.

The upper 3 bits of TL0 (or TL1) are indeterminate in mode 0 and must be masked when the software evaluates the register.

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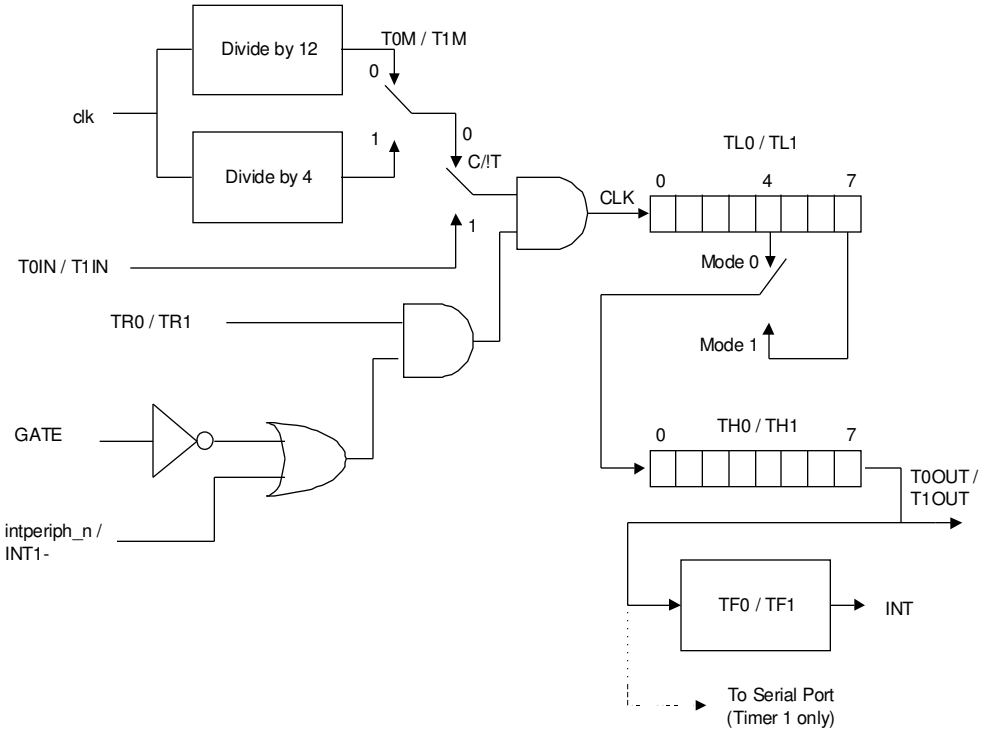
Mode1

Mode 1 operation is the same for Timer 0 and Timer 1. In mode 1, the timer is configured as a 16-bit counter. As illustrated in **Figure 8**, all 8 bits of the LSB register (TL0 or TL1) are used. The counter rolls over to all zeros (0000h) upon surpassing FFFFh. Otherwise, mode 1 operation is the same as mode 0. Please refer to the Interrupts section for a better understanding of how the interrupts are handled in the VERSA1.

FIGURE 8 TIMER 0 / TIMER 1 -MODES 0 AND 1



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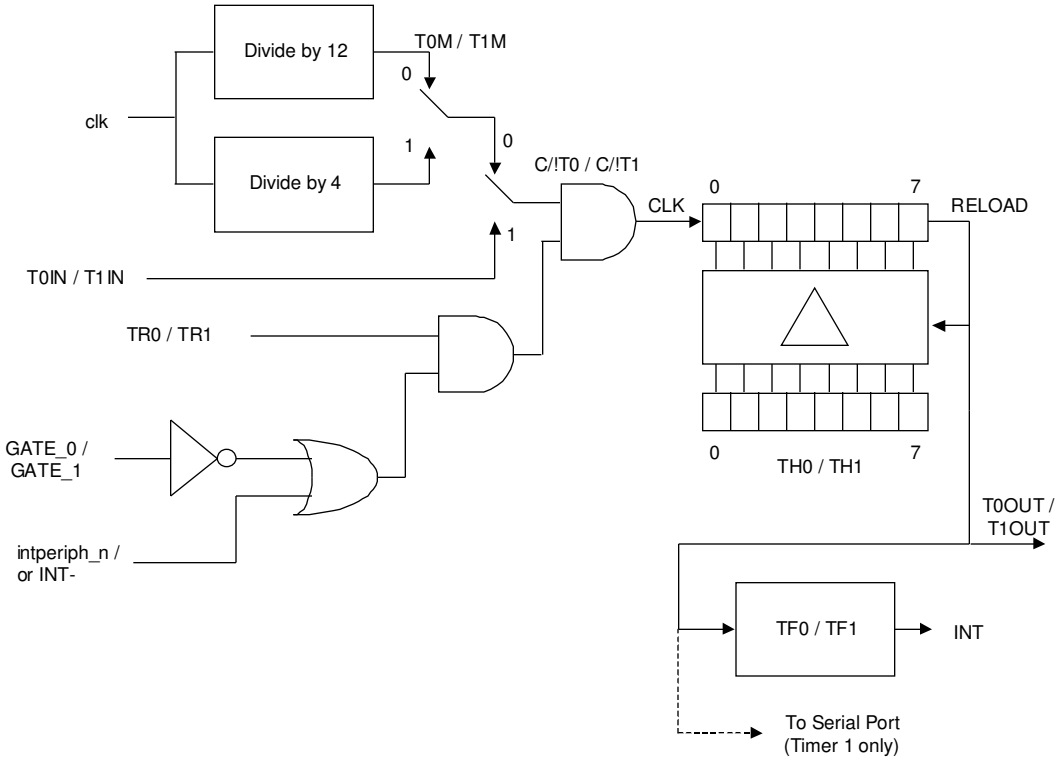
Mode 2

Mode 2 operation is the same for Timer 0 and Timer 1. In mode 2, the timer is configured as an 8-bit counter, with automatic reload of the start value. The LSB register (TL0 or TL1) is the counter and the MSB register (TH0 or TH1) stores the reload value. Please refer to the Interrupts section for a better understanding of how the interrupts are handled in the VERSA1.

As illustrated in **Figure 9**, mode 2 counter control is the same for mode 0 as for mode 1. However, in mode 2, when TLn surpasses FFh, the value stored in THn is reloaded into TLn.

FIGURE 9 TIMER 0 / TIMER 1 -MODE 2



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Mode 3

In mode 3, Timer 0 operates as two 8-bit counters and Timer 1 stops counting and holds its value.

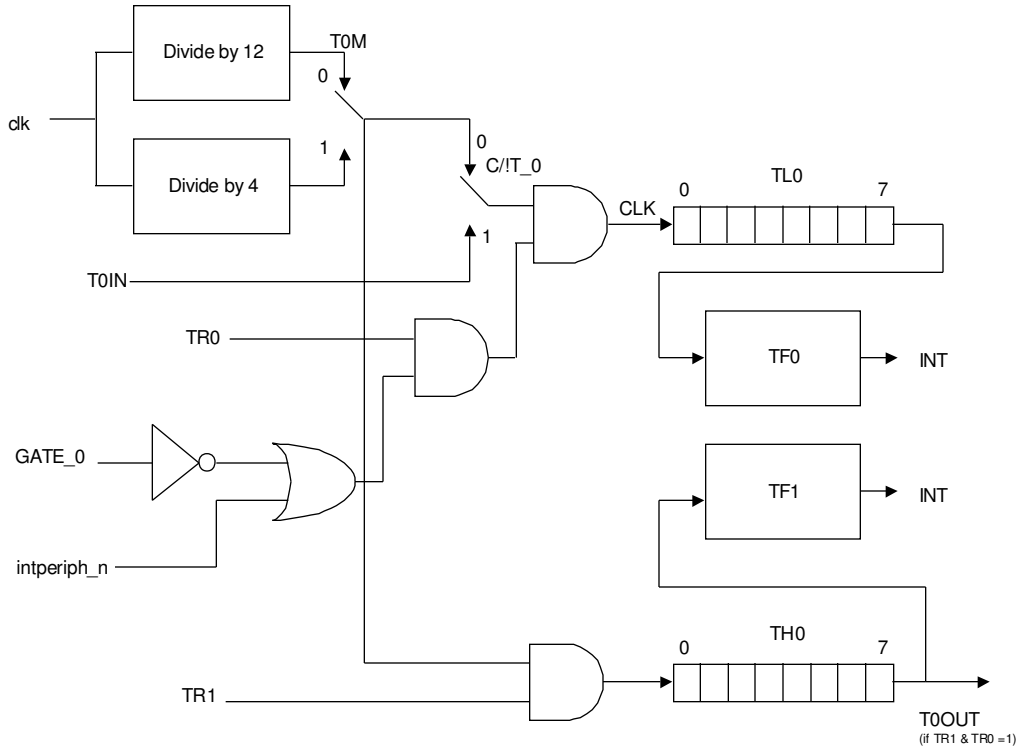
As shown in **Figure 10**, TL0 is configured as an 8-bit counter controlled by the normal Timer 0 control bits. TL0 can either count *clk* cycles (divided by 4 or by 12) or high-to-low transitions on T0IN, as determined by the C/!T_0 bit. The GATE_0 function can be used to give counter enable control to the intperiph_n signal. Please refer to the Interrupts section for a better understanding of how the interrupts are handled in the VERSA1.

TH0 functions as an independent 8-bit counter. However, TH0 can only count *clk* cycles (divided by 4 or by 12). The Timer 1 control and flag bits (TR1 and TF1) are used as the control and flag bits for TH0.

When Timer 0 is in mode 3, Timer 1 has limited usage because Timer 0 uses the Timer 1 control bit (TR1) and interrupt flag (TF1). Timer 1 can still be used for baud rate generation and the Timer 1 count values are still available in the TL1 and TH1 registers.

Control of Timer 1 when Timer 0 is in mode 3 is through the Timer 1 mode bits. To turn Timer 1 on, set Timer 1 to mode 0, 1, or 2. To turn Timer 1 off, set it to mode 3. The Timer 1 C/!T_1 bit and T1 M bit are still available to Timer 1. Therefore, Timer 1 can count *clk/4, clk/12,* or high-to-low transitions on the T1IN pin. The Timer 1 GATE_1 function is also available when Timer 0 is in mode 3

FIGURE 10 TIMER 0 -MODE 3



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Timers 0, 1, 2 Rate Control

The default timer clock scheme for the VERSA1 timers is 12 *clk* cycles per increment, the same as in the standard 8051. However, in the VERSA1, the instruction cycle is 4 *clk* cycles.

Using the default rate (12 system clocks per timer increment) allows existing application code with real-time dependencies, such as baud rate, to operate properly. However, applications that require fast timing can set the timers to increment every 4 *clk* cycles by setting bits in the Clock Control register CKCON at SFR location 8Eh (see **Table 11**)

The CKCON bits that control the timer clock rates are:

CKCON bit	Counter/Timer
5	Timer 2
4	Timer 1
3	Timer 0

When a CKCON register bit is set to 1, the associated counter increments at *4-clk* intervals. When a CKCON register bit is set to 1, the associated counter increments at *12-clk* intervals. The timer controls are independent of each other. The default setting for all three timers is 0 *(12-clk* intervals). These bits have no effect in counter mode.

TABLE 11 CKCON REGISTER SFR 8EH

Bit #	Mnemonic	Function
7-6	Reserved	Not implemented
5	T2M	Timer 2 clock select. When T2 M = 0, Timer 2 uses clk/12 (for compatibility with 80C32); when T2M = 1, Timer 2 uses clk/4. This bit has no effect when Timer2 is configured for baud rate generation.
4	T1M	Timer 1 clock select. When T1 M = 0, Timer 1 uses clk/12 (for compatibility with 80C32); when T1 M = 1, Timer 1 uses clk/4.
3	T0M	Timer 0 clock select. When T0M = 0, Timer 0 uses clk/12 (for compatibility with 80C32); when T0M = 1, Timer 0 uses clk/4.
2-0	Reserved	

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Timer 2

Timer 2 runs only in 16-bit modes and offers the following functionalities:

- 16-bit timer
- 16-bit auto-reload timer
- 16-bit precision Baud rate generator

Using Timer 2 as a baud rate generator for serial port 0 permits the generation of a larger range of baud rates. Note that Timer 2 can only run from internal clock signal. It is not possible to capture external events using Timer 2.

The SFRs associated with Timer 2 are:

- CKCON SFR 8Eh (See **Table 11**)
- T2CON SFR C8h (See **Table 12**)
- RCAP2L SFR CAh LSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.
- RCAP2H SFR CBh MSB of the 16-bit reload value when Timer 2 is configured for auto-reload mode.
- TL2 SFR CCh Lower 8 bits of the 16-bit count.
- TH2 SFR CDh Upper 8 bits of the 16-bit count.

TABLE 12 T2CON REGISTER – SFR C8H

Bit#	Mnemonic	Function
7	TF2	Timer 2 overflow flag. Hardware will set TF2 when Timer 2 overflows from FFFFh. TF2 must be cleared to 0 by the software. TF2 will only be set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
6	FIRQT2	Timer 2 external flag. There is no external interface to Timer 2 on VERSA1. FIRQT2 must be cleared to 0 by the software. Writing a 1 to FIRQT2 forces a Timer 2 interrupt if enabled.
5	RCLK	Receive clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of received data in serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the receive clock. RCLK = 0 selects Timer 1 overflow as the receive clock.
4	TCLK	Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in serial mode 1 or 3. TCLK = 1 selects Timer 2 overflow as the transmit clock. TCLK = 0 selects Timer 1 overflow as the transmit clock.
3	0	Always write 0 to this location
2	TR2	Timer 2 run control flag. TR2 = 1 starts Timer 2. TR2 = 0 stops Timer 2.
1	T2=0	Always write 0 to this register to set Timer 2 in timer mode. Timer 2 runs at 4 clocks per increment or 12 clocks per increment as programmed by CKCON.5, in all modes except baud rate generator mode. When used in baud rate generator mode, Timer 2 runs at 2 clocks per increment, independent of the state of CKCON.5.
0	-RL2	Writing 0 to this location will make Timer 2 auto-reloads occur when Timer 2 overflows.

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Timer 2 Mode Control

Table 13 summarizes how the SFR bits determine the Timer 2 mode.

TABLE 13 TIMER 2 MODE CONTROL SUMMARY

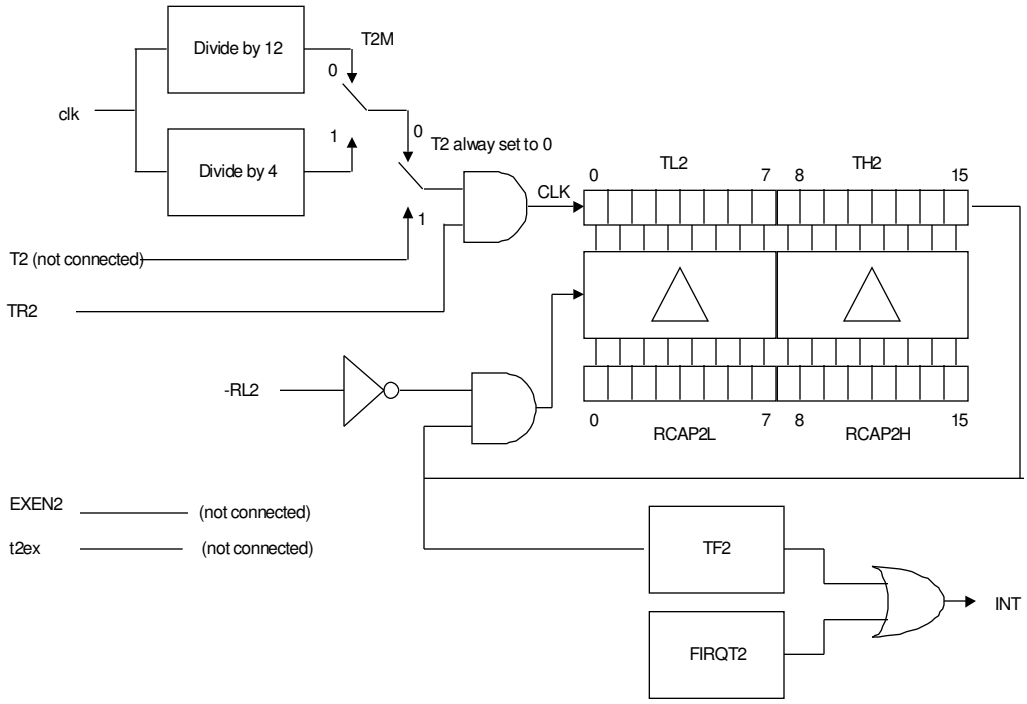
RCLK	TCLK	-RL2	TR2	Mode
0	0	1	1	16 bits Timer
0	0	0	1	16 bits Timer with Auto Reload
1	X	X	1	Baud Rate Generator
X	1	X	1	Baud Rate generator
X	X	X	0	OFF

Timer 2 16-bit Timer Modes

Figure 11 illustrates how Timer 2 operates in timer modes. Clocking of Timer 2 is only possible through the system clock, which is divided by 4 or by 12 depending on the value of the T2M bit. Make sure that T2CON.1 (T2 bit in std 8052) is always set to 0. There is no output pin for Timer 2. Setting the TR2 bit permits the start of Timer 2.

When the Timer 2 count overflows from FFFFh, the TF2 flag is set, raising a Timer 2 interrupt if enabled.
When -RL2 = 0, Timer 2 is configured for the auto-reload mode illustrated in Figure 12. Control of counter input is the same as for the other 16-bit counter modes. When the count increments from FFFFh, Timer 2 sets the TF2 flag and the starting value is reloaded into TL2 and TH2. The software must preload the starting value into the RCAP2L and RCAP2H registers.

FIGURE 11 TIMER 2 STRUCTURE IN TIMER MODES



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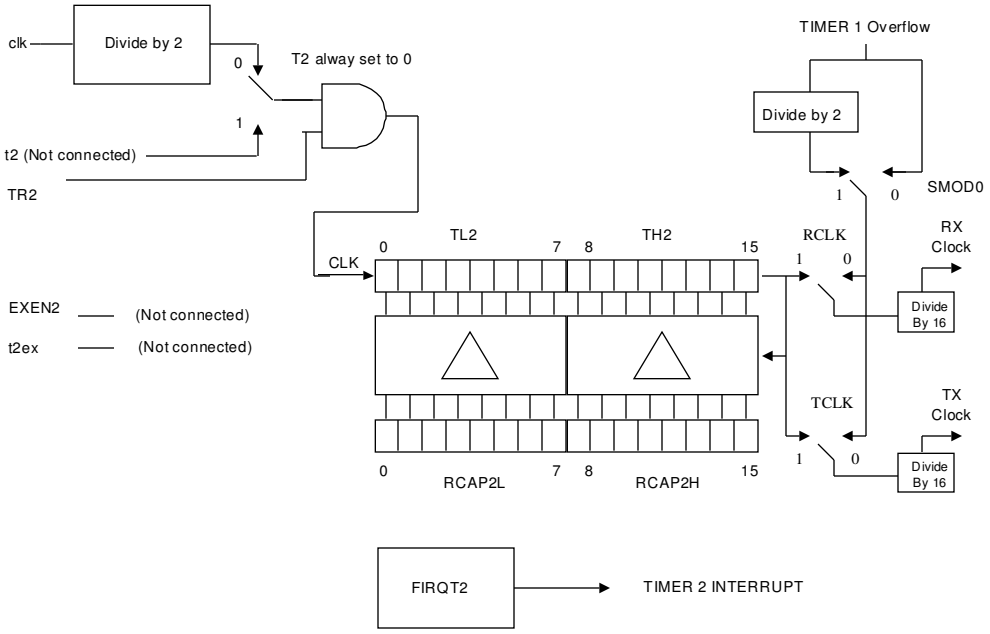
Timer 2 Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial Port 0 in serial mode 1 or 3. In baud rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow generates a shift clock for the serial port function. As in normal auto-reload mode, the overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation, regardless of the state of the CP/RL2 bit.

When operating as a baud rate generator, Timer 2 does not set the TF2 bit. In this mode the counter time base in baud rate generator mode is clk/2.

FIGURE 12 TIMER 2 – BAUD RATE GENERATOR MODE



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Serial Interface

The VERSA1 provides two serial ports: Serial Port 0 and Serial Port 1.

Both serial ports operate in full duplex asynchronous mode. The VERSA1 buffers receive data in a holding register, enabling the UART to receive an incoming word before the software has read the previous value.

The clock source for serial port 0 can be provided by both Timer 1 and Timer 2. In the case of serial port 1, only Timer 1 can be used as the clock source. Note that it is possible to use an external clock source to drive Timer 0 and Timer 1 through T0IN and T1IN pin respectively. In that case, the maximum frequency of this external Clock source must be < (Oscillator freq / 8).

Note: To use the Serial Port1, the S1EN of the S1ACTIVATE register must be set to 0. (SFR D7h).

The following tables provide a summary of the registers involved in the configuration of the VERSA1 serial ports.

TABLE 14 SFR USED FOR SERIAL PORT 0 AND SERIAL PORT 1 CONTROL

Register	SFR Address	Use
SCON0	98h	Serial port 0 control
SBUF0	99h	Serial port 0 buffer
SCON1	C0h	Serial port 1 control
SBUF1	C1h	Serial port 1 buffer
PCON	87h	Serial port 0 rate doubler
EICON**	D8h	Serial port 1 rate doubler
IE**	A8h	Serial ports interrupt control
IP**	B8h	Serial ports interrupt priority control

Register	SFR Address	Use
TMOD*	89h	Timer 1 control register
TCON*	88h	Timer 1 start/stop control TR1
CKCON*	8Eh	Timer 1 & Timer 2 control
T2CON*	C8h	Timer 2 control register
TH1*	8Dh	Reload of Timer 1 in mode 2
RCAP2H*	CAh	Reload value of Timer 2 in mode 2
RCAP2L*	CBh	

* See previous section on Timers description
**See next section on Interrupt description

TABLE 15 SCON0 REGISTER -SFR 98H

Bit #	Mnemonic	Function
7	SM0_0	Serial Port 0 mode bit 0.
6	SM1_0	Serial Port 0 mode bit 1, decoded as: **SM0_0 SM1_0 Mode** 0 1 1 1 0 2 1 1 3
5	SM2_0	Multiprocessor communications enable. In modes 2 and 3, SM2_0 enables the multiprocessor communication feature. If SM2_0 = 1 in mode 2 or 3, RI_0 will not be activated if the received 9th bit is 0. If SM2_0 = 1 in mode 1, RI_0 will only be activated if a valid stop is received.
4	REN_0	Receive enable. When REN_0 = 1, reception is enabled.
3	TB8_0	Defines the state of the 9th data bit transmitted in modes 2 and 3.
2	RB8_0	In modes 2 and 3, RB8_0 indicates the state of the 9th bit received. In mode 1, RB8_0 indicates the state of the received stop bit.
1	TI_0	Transmit interrupt flag. Indicates that the transmit data word has been shifted out. TI_0 is set when the stop bit is placed on the TX0 pin. TI_0 must be cleared by the software.
0	RI_0	Receive interrupt flag. Indicates that a serial data word has been received. In mode 1, RI_0 is set after the last sample of the incoming stop bit, subject to the state of SM2_0. In modes 2 and 3, RI_0 is set at the end of the last sample of RB8_0. The software must clear RI_0.

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TABLE 16 SCON1 REGISTER -SFR C0H

Bit #	Mnemonic	Function
7	SM0_1	Serial Port 1 mode bit 0.
6	SM1_1	Serial Port 1 mode bit 1, decoded as: **SM0_0 SM0_1 Mode** 0 1 1 1 0 2 1 1 3
5	SM2_1	Multiprocessor communications enable. In modes 2 and 3, SM2_1 enables the multiprocessor communication feature. If SM2_0 = 1 in mode 2 or 3, RI_0 will not be activated if the received 9th bit is 0. If SM2_1 = 1 in mode 1, RI_1 will only be activated if a valid stop is received.
4	REN_1	Receive enable. When REN_1 = 1, reception is enabled.
3	TB8_1	Defines the state of the 9th data bit transmitted in modes 2 and 3.
2	RB8_1	In modes 2 and 3, RB8_1 indicates the state of the 9th bit received. In mode 1, RB8_1 indicates the state of the received stop bit.
1	TI_1	Transmit interrupt flag. Indicates that the transmit data word has been shifted out. TI_1 is set when the stop bit is placed on the TX0 pin. TI_1 must be cleared by the software.
0	RI_1	Receive interrupt flag. Indicates that a serial data word has been received. In mode 1, RI_1 is set after the last sample of the incoming stop bit, subject to the state of SM2_1. In modes 2 and 3, RI_1 is set at the end of the last sample of RB8_1. The software must clear RI_1.

As it can be seen in two previous tables, the VERSA1 serial ports 0 and serial port 1 can operate in three distinct asynchronous modes, as outlined in **Table 17**

TABLE 17 SERIAL PORT MODES

Mode	Baud Clock	Data Bits	Start/Stop	9th Bit Function
1	Timer 1 or Timer 2	8	1 start, 1 stop	None
2	clk/32 or clk/64	9	1 start, 1 stop	0, 1, parity
3	Timer 1 or Timer 2	9	1 start, 1 stop	0, 1, parity

Serial port Interrupt mapping

Both serial ports 0 and serial port 1 have a dedicated interrupt line which informs the processor of the completion of a byte transmission or reception. When such an interrupt takes place, the software must check the status of the RI and TI bits of the appropriate SCON register to determine the source of the interrupt (transmission end or reception)

The interrupt signals from both serial port 0 and serial port 1 are controlled respectively by Bit ES0 (IE.3), ES1 (IE.7) of the IE register (SFR A8h). Note that EA bit (IE.7) must also be set to 1 for these interrupt, and other enabled interrupts to be taken into account.

It is also possible to change the priority of the interrupts generated by both serial ports by setting to 1 PS0 and/or PS1 bits of the interrupt priority register IP (SFR B8h)

TABLE 18 INTERRUPT VECTORS ASSIGNED TO SERIAL PORT 0 AND SERIAL PORT 1

Interrupt	Description	Priority	Interrupt Vector
TI_0 or RI_0	Serial port 0 transmit or receive interrupt	5	23h
TI_1 or RI_1	Serial port 1 transmit or receive interrupt	7	3Bh

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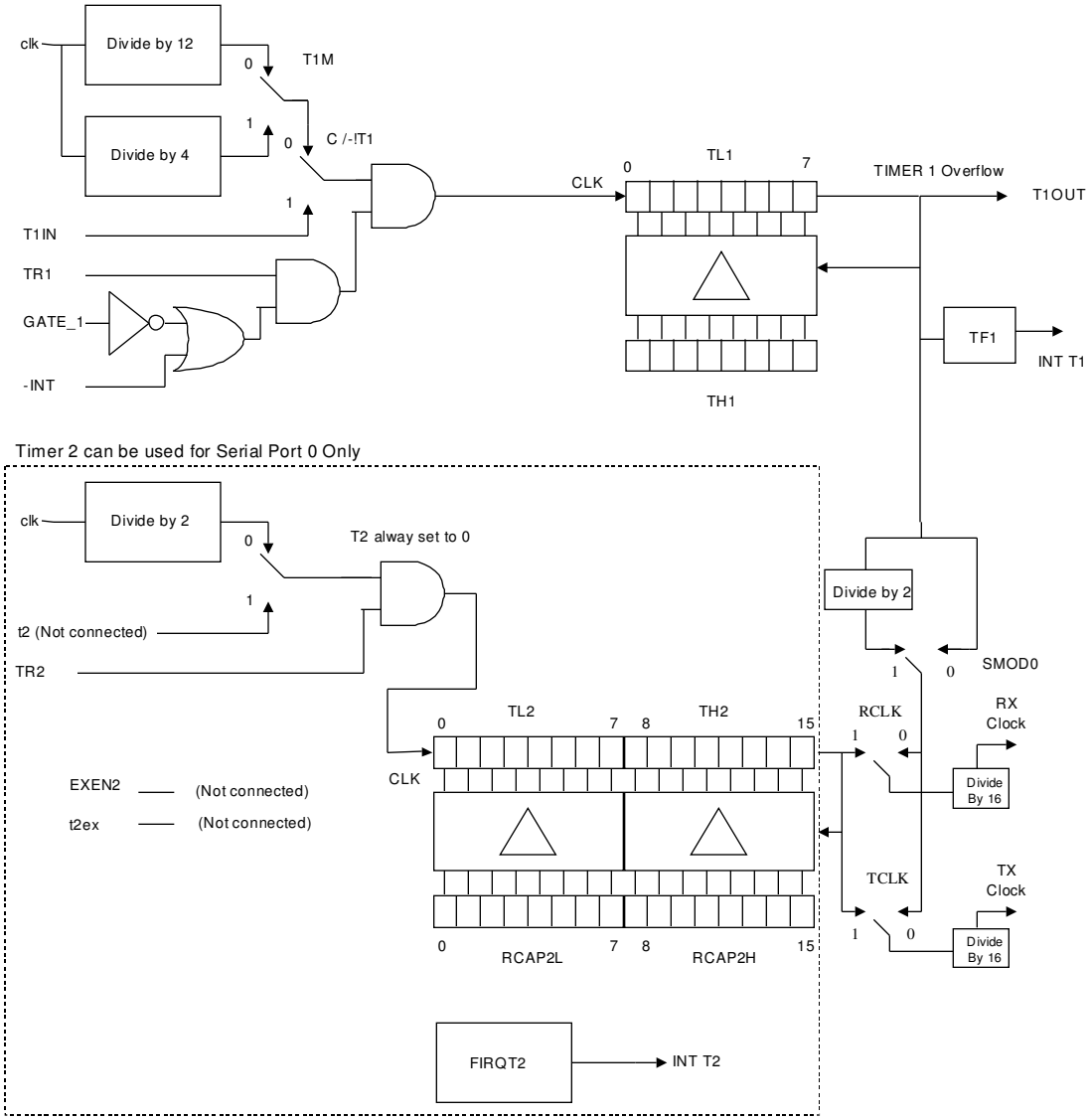
Mode 1

Mode 1 provides standard asynchronous, full-duplex communication, using a total of 10 bits: 1 start bit, 8 data bits, and 1 stop bit. For receive operations, the stop bit is stored in RB8_0 (or RB8_1). Data bits are received and transmitted LSB first.

Figure 13 provides a summary view of the relations between Timer 1 and Timer 2 and serial ports when configured in mode 1. In this representation, we take into account that timers are configured in auto-reload. For special cases it is possible to disable this feature.

FIGURE 13 TIMER 1 AND TIMER 2 INTERFACE TO SERIAL PORTS CONFIGURED IN MODE 1



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Mode 1 Baud Rate Using Timer 1

The mode 1 baud rate is a function of timer overflow. Both Serial Ports can use Timer 1 to generate baud rates. Each time the timer increments from its maximum count, a clock is sent to the baud rate circuit. The clock is then divided by 16 to generate the baud rate. When using Timer 1, the SMOD0/1 bit selects whether or not to divide the Timer 1 rollover rate by 2. Therefore, when using Timer 1, the baud rate is determined by the equation:

$$\text{Baud Rate} = \frac{2^{SMOD0/1}}{32} \times \text{Timer 1 Overflow}$$

For serial port 0 use SMOD0 (SFR bit PCON.7)
For serial port 1 use SMOD1 (SFR bit EICON.7)

To use Timer 1 as the baud rate generator, it is best to use Timer 1 in mode 2 (8-bit counter with auto-reload), although any counter mode can be used. The Timer 1 reload value is stored in the TH 1 register, which makes the complete formulas for Timer 1. **Table 19** shows the formulas to calculate baud rate or TH1 register value when using Timer 1 in mode 2:

TABLE 19 EQUATION TO CALCULATE BAUD-RATE OR TIMER 1 RELOAD VALUE (IN MODE 2)

For TM1 = 0 (standard mode)	For TM1 = 1 (Fast Mode)
$\text{Baud Rate} = \frac{2^{SMOD0/1}}{32} \times \frac{clk}{12 \times (256 - TH1)}$	$\text{Baud Rate} = \frac{2^{SMOD0/1}}{32} \times \frac{clk}{4 \times (256 - TH1)}$
$TH1 = 256 - \frac{2^{SMOD0/1} \times clk}{384 \times \text{Baud Rate}}$	$TH1 = 256 - \frac{2^{SMOD0/1} \times clk}{128 \times \text{Baud Rate}}$

**Where clk = system clock which is Fosc / 2 (clk divider = reset value)*

You can also achieve very low baud rates from Timer 1 by enabling the Timer 1 interrupt, configuring Timer 1 to mode 1, and using the Timer 1 interrupt to initiate a 16-bit software reload. **Table 20** lists sample reload values for a variety of common serial port baud rates.

TABLE 20 TIMER 1 RELOAD VALUES FOR COMMON SERIAL PORT MODE 1 BAUD RATES

Desired Baud Rate	SMODx	C/!T_1	Timer 1 Mode	T1M	TH1 @ 11.0592 MHz osc	TH1 @ 14.746 MHz osc	TH1 @ 16.000 MHz osc
115.2 Kbp/s	1	0	2	1	N/A	FFh	N/A
57.6 Kb/s	1	0	2	1	N/A	FEh	N/A
19.2 Kb/s	1	0	2	1	N/A	FAh	N/A
9.6 Kb/s	1	0	2	1	F7h	F4h	F3h
2.4 Kb/s	1	0	2	1	DCh	D0h	CBh
1.2 Kb/s	1	0	2	1	B8h	A0h	96h

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Mode 1 Baud Rate Using Timer 2 (serial port 0 only)

Timer 2 can be used to generate baud rates for serial port 0 only. When used as the baud rate generator Timer 2 increment rate is defined as clk/2. Each time Timer 2 overflows a clock pulse is sent to the serial port interface. This clock is then divided by 16 to generate the baud rate.

To use Timer 1 as the baud rate generator, it is best to use Timer 2 in 16-bits auto-reload. The 16-bits Timer 2 reload value is stored in the RCAP2H and RCAP2L registers.

TABLE 21 EQUATIONS TO CALCULATE BAUD-RATE OR TIMER 2 RELOAD VALUE

Baud Rate = _____clk_____ 32 x (65536 – **RCAP2H, 2L**)
RCAP2H, 2L = _____clk_____ 32x (65536 - **Baud Rate**)

**Where clk = system clock which is Fosc / 2 (clk divider = reset value)*

Having 16-bits resolution for baud rate adjustment permits wider baud rate adjustment for a given oscillator frequency. **Table 22** lists a sample of reload values for a variety of common serial port baud rates and oscillator frequencies

TABLE 22 TIMER 2 RELOAD VALUES FOR COMMON SERIAL PORT 0 BAUD RATES

Desired Baud Rate	RCAP2H, 2L @ 11.0592 MHz osc	RCAP2H, 2L @ 14.746 MHz osc	RCAP2H, 2L @ 16.000 MHz osc
115.2 Kbps	N/A	FFFEh	N/A
57.6 Kbs	FFFDh	FFFCh	N/A
19.2 Kbs	FFF7h	FFF4h	FFF3h
9.6 Kbs	FFEEh	FFE8h	FFE6h
2.4 Kbs	FFB8h	FFA0h	FF98h
1.2 Kbs	FF70h	FF3Fh	FF30h
300 bps	FDC0h	FCFFh	FCBFh

Mode 1 Transmit

Figure 14, illustrates the mode 1 transmit timing. In mode 1, the UART begins transmitting after the first rollover of the divide-by-16 counter after the software writes to the SBUF0 (or SBUF1) register. The UART transmits data on the TX0 pin in the following order: start bit, 8 data bits (LSB first), stop bit. The TI_0 (or TI_1) bit is set 2 *clk* cycles after the stop bit is transmitted.

Mode 1 Receive

Figure 15 illustrates the mode 1 receive timing. Reception begins at the falling edge of a start bit received on RX0, when enabled by the REN_0 (or REN_1) bit. For this purpose, RX0 is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on RX0 (or RX1) is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on RX0 (or RX1).

At the middle of the stop bit time, the serial port checks for the following conditions:

- RI_0 (or RI_1) = 0, and
- If SM2_0 (or SM2_ 1) = 1, the state of the stop bit is 1.
- (If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.

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If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) register, loads the stop bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set.

After the middle of the stop bit time, the serial port waits for another high-to-low transition on the RX0 pin.

Mode 1 operation is identical to that of the standard 8051 when Timers 1 and 2 use *clk/12* (the default).

FIGURE 14 SERIAL PORT MODE 1 TRANSMIT TIMING

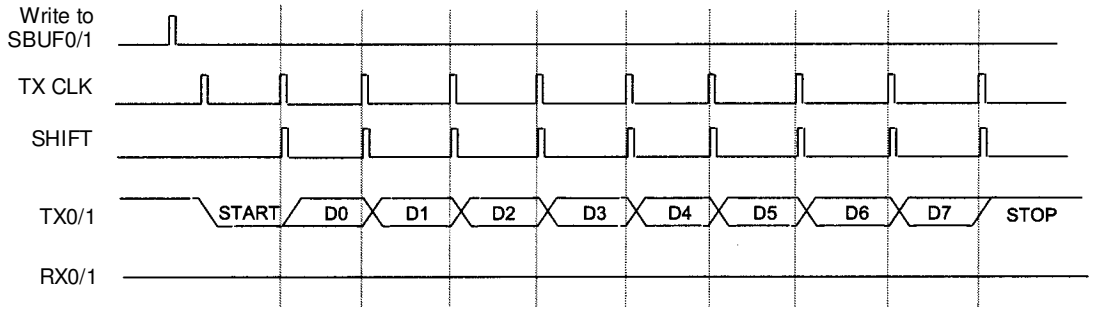
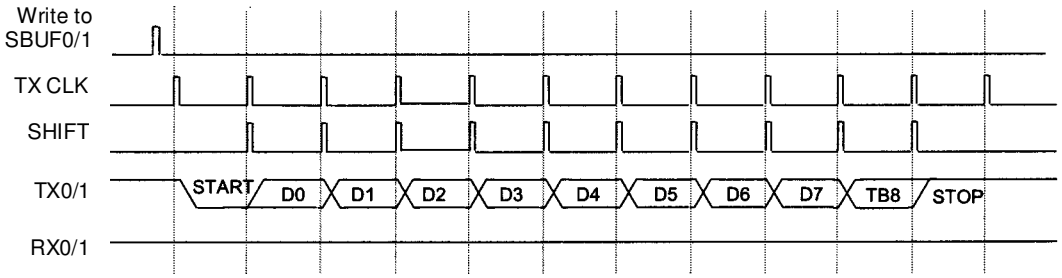


FIGURE 15 SERIAL PORT MODE 1 RECEIVE TIMING



Mode 2

Mode 2 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first. For transmission, the 9th bit is determined by the value in TB8_0 (or TB8- 1). To use the 9th bit as a parity bit, move the value of the P bit (SFR PSW.0) to TB8_0 (or TB8_1).

The mode 2 baud rate is either *clk/32* or *clk/64,* as determined by the SMOD0 (or SMOD1) bit. The formula for the mode 2 baud rate is:

$$\text{Baud Rate} = \frac{2^{SMOD0} \times clk}{64}$$

**Where clk = system clock (which is Fosc / 2)*

Mode 2 operation is identical to the standard 8051.

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Mode 2 Transmit

Figure 16 illustrates the mode 2 transmit timing. Transmission begins after the first rollover of the divide-by-16 counter following a software write to SBUF0 (or SBUF1). The UART shifts data out on the TX0 (or TX1) pin in the following order: start bit, data bits (LSB first), 9th bit, stop bit. The TI_0 (or TI_1) bit is set when the stop bit is placed on the TX0 (or TX1) pin.

Mode 2 Receive

Figure 17 illustrates the mode 2 receive timing. Reception begins at the falling edge of a start bit received on RX0, when enabled by the REN_0 (or REN_1) bit. For this purpose, RX0 (or RX1) is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receive clock is reset to align the counter rollover to the bit boundaries.

For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on RX0 (or RX1) is not verified by a majority decision of 3 consecutive samples (low), then the serial port stops reception and waits for another falling edge on RX0 (or RX1).

At the middle of the stop bit time, the serial port checks for the following conditions:

- **RI_0** (or RI_1) = 0, and
- **If** SM2_0 (or SM2_ 1) = 1, the state of the stop bit is 1. (If SM2_0 (or SM2_1) = 0, the state of the stop bit doesn't matter.)

If the above conditions are met, the serial port then writes the received byte to the SBUF0 (or SBUF1) register, loads the 9th received bit into RB8_0 (or RB8_1), and sets the RI_0 (or RI_1) bit. If the above conditions are not met, the received data is lost, the SBUF register and RB8 bit are not loaded, and the RI bit is not set. After the middle of the stop bit time, the serial port waits for another high-to-low transition on the RX0 (or RX1) pin.

FIGURE 16 SERIAL PORT MODE 2 TRANSMIT TIMING

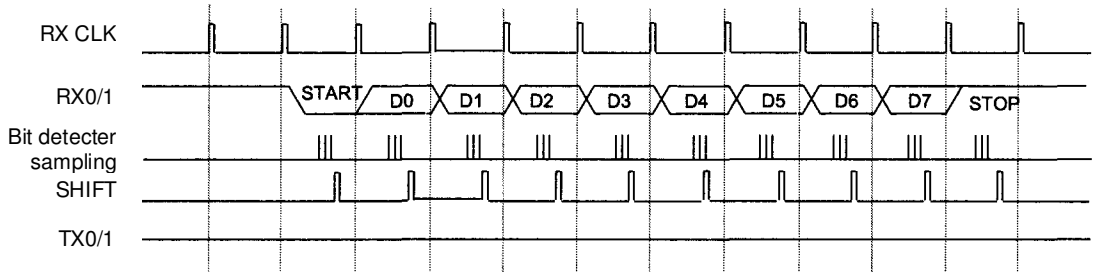

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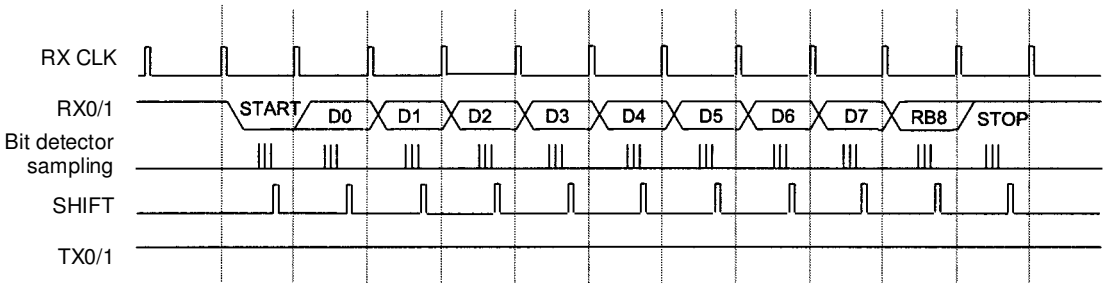
FIGURE 17 SERIAL PORT MODE 2 RECEIVE TIMING



Mode 3

Mode 3 provides asynchronous, full-duplex communication, using a total of 11 bits: 1 start bit, 8 data bits, a programmable 9th bit, and 1 stop bit. The data bits are transmitted and received LSB first.

The mode 3 transmit and receive operations are identical to mode 2. The mode 3 baud rate generation is identical to mode 1. That is, mode 3 is a combination of mode 2 protocols and mode 1 baud rate. **Figure 18** illustrates the mode 3 transmit timing. Figure 3-16 illustrates the mode 3 receive timing.

Mode 3 operation is identical to that of the standard 8051 when Timers 1 and 2 use *clk/12* (the default).

FIGURE 18 SERIAL PORT MODE 3 TRANSMIT TIMING

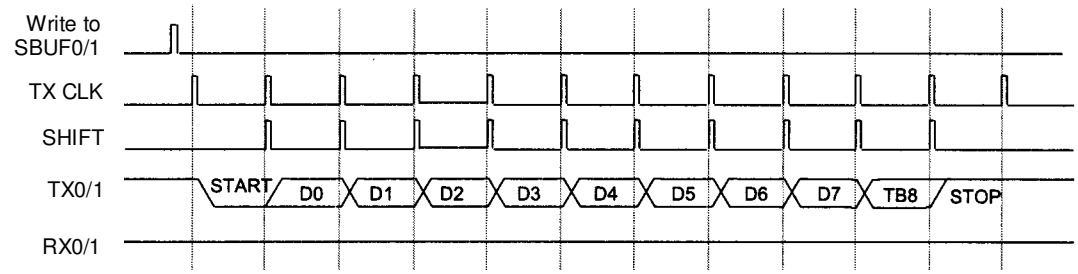
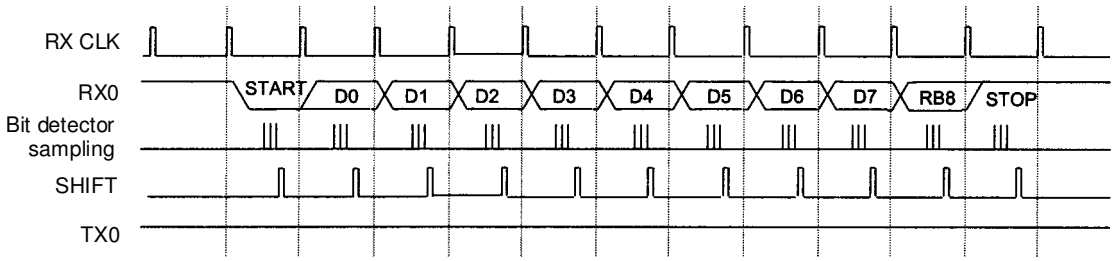


FIGURE 19 SERIAL PORT MODE 3 RECEIVE TIMING



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Multiprocessor Communications

The multiprocessor communication feature is enabled in modes 2 and 3 when the SM2 bit is set in the SCAN SFR for a serial port (SM2_0 for Serial Port 0, SM2- 1 for Serial Port 1). In multiprocessor communication mode, the 9th bit received is stored in RB8_0 (or RB8_1) and, after the stop bit is received, the serial port interrupt is activated only if RB8_0 (or RB8_1) = 1.

A typical use for the multiprocessor communication feature is when a master wants to send a block of data to one of several slaves. The master first transmits an address byte that identifies the target slave. When transmitting an address byte, the master sets the 9th bit to 1; for data bytes, the 9th bit is 0.

When SM2_0 (or SM2_1) = 1, no slave will be interrupted by a data byte. However, an address byte interrupts all slaves so that each slave can examine the received address byte to determine whether that slave is being addressed. Address decoding must be done by software during the interrupt service routine. The addressed slave clears its SM2_0 (or SM2_1) bit and prepares to receive the data bytes. The slaves that are not being addressed leave the SM2_0 (or SM2- 1) bit set and ignore the incoming data bytes.

Bit Addressing

Bit addressing in SFR space is available at all SFR addresses that end with 0 or 8. For example, the PSW SFR at address D0h is bit- addressable. **Table 23** lists the bit-addressable SFRs and their usage.

TABLE 23 BIT-ADDRESSABLE SFRS

SFR Address	Usage
80h	-
88h	TCON
90h	-
98h	SCON0
A0h	-
A8h	IE
B0h	-
88h	IP
C0h	-
C8h	-
D0h	PSW
D8h	EICON
E0h	ACC
E8h	EIE
F0h	B
F8h	EIP

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Analog Signal Path Overview

On the analog side, the VERSA1 provides the following features:

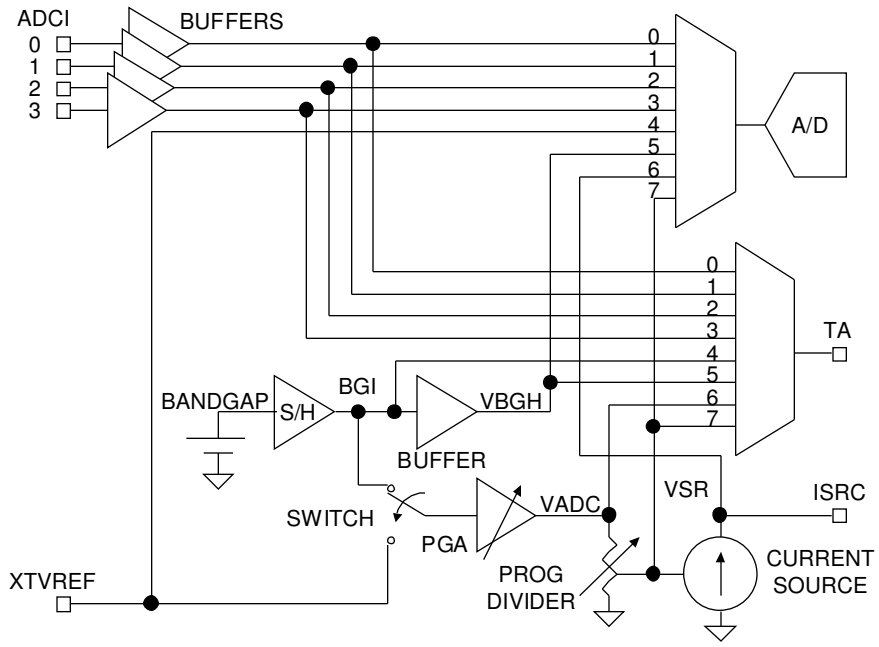
- 4 external input channels for A/D converter
- Internal Bandgap reference and Programmable Gain Amplifier (PGA)
- Programmable current source
- Input multiplexer
- Multiplexed analog output

This permits the VERSA1 to be used as a single chip acquisition system incorporating a complete analog acquisition circuitry coupled with a powerful 8051 microcontroller core backed by MAC unit and plenty of RAM memory. With the VERSA1, it is possible to perform signal acquisition as well as advanced data analysis.

Figure 20 shows the analog block of the VERSA1. The choice of an on-chip calibrated Bandgap or an external reference (XTVREF pin) provides the basis for all the derived on-chip voltages. These derived voltages are used as the reference signals for the A/D and the current source.

Four external analog inputs ($ADCI_{(0-3)}$) are buffered and applied to the A/D via an 8 to 1 multiplexer. The remaining four inputs to the multiplexer connect to the internal derived voltages (this enables a test comparison to be made with the external signals). A second 8 to 1 multiplexer provides the ability to drive the buffered $ADCI_{(0-3)}$ signals and the internal derived voltages outside of the VERSA1 (through the TA pin) for applications that require external use of those voltages.

FIGURE 20 ANALOG SIGNAL PATH OF THE VERSA1



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A/D converter

The A/D converter of the VERSA1 can be configured for a number of different operating modes to meet the specific application requirements. Basically the ADC supports two operating modes:

- Continuous conversion
- Single shot conversion

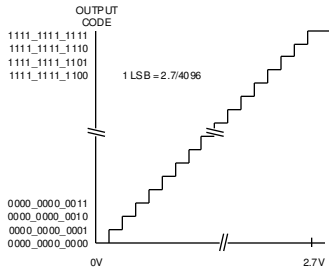
The continuous conversion mode sets the ADC to perform timed conversions of 1 or 4 channels and the single shot conversion sets the ADC to perform one conversion of 1 or 4 channels at a given time. The operation mode of the ADC is controlled by the ONESHOT and CONT bits of the ADC Control register (**See table 29**).

The bit MANUAL of the ADC Control Register (**see table 29**) value, defines whether the conversion will be performed on 1 or 4 channels.

When the ADC is configured to perform 4 channels conversions, the converted data will be available in a set of four 12-bit registers mapped into the processor's SFR space. When the ADC is configured to perform conversion on one channel, the conversion result is always placed into the ADC channel 0 registers **(See tables 32 and 33)**.

The analog input voltage range for the ADC is 0 to 2.7V and the output coding is binary with 1 LSB = Full Scale / 4096. The following describes the ideal transfer function for the VERSA1

FIGURE 21 IDEAL A/D CONVERTER TRANSFER FUNCTION



When configured in Continuous conversion, the rate of conversions is controlled by the value written into the three conversion rate registers (**see tables 26, 27, 28**). The 24 bit CONV_RATE [23:0] register is used to set the conversion rate when in continuous conversion mode and is governed by the following formula:

$$\text{Conversion Rate registers value (24bits)} = (\text{External Clock} / 2) / (\text{CONV\_RATE})$$

The continuous conversion rate is programmable from about 0.5Hz to 2kHz for one channel assuming a 16MHz oscillator clock. For 4 channels continuous conversion, the maximum conversion rate is about 570Hz.

To perform a single shot conversion at a given time, the bit ONESHOT (bit 5 of the ADC Control Register) must be set. At the end of the conversion, the bit ADCINT (bit 0 of the ADC Status Register to go to 1) will be set. It is possible to generate an interrupt from this bit or to monitor its status by polling. Note that once this bit is set, the ADCIC bit (bit 3 of the ADC control register) must be set to clear the ADCINT bit.

To get the best possible acquisitions and save power, it is recommended to lower the processor clock speed or to shut it down completely by using the CLKDIVIDER register during the conversion process. If the processor's clock is completely stopped during the conversion, the ADC can be configured to generate an interrupt (by setting to 1 the bit ADCIE of the ADC Control Register) that will wake-up the processor at the end of the conversion. Before using the ADC, it is mandatory to set the clock reference to the ADC by writing the appropriate value into the ADC Clock divider register. This reference clock must be as close to 250KHz as possible. The equation to get the appropriate value is as follows:

$$\text{ADC Clk ref} = (\text{External Clock} / 2) / [(2 * \text{ADCCDIV}) + 2]$$

For example if the External Clock is 16MHz, then ADCCDIV should be set to 15 (0Fh).

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Setting up the VERSA1 ADC

The following list of operations describes the required steps needed to initialise the ADC to perform continuous conversion of the 4 analog input channels:

- Enable PGA
- Retrieve calibration vectors from the OTPR for Bandgap, PGA
- Set Bandgap order
- Enable all input buffers and select the input buffers feeding the ADC inputs
- Enable the output analog multiplexer and route TA on BGI.
- Set the 250 kHz reference clock of the ADC
- Set the Conversion Rate registers
- Set the ADC for continuous conversion, Enable ADC, Enable the Bandgap.
- Enable ADC interrupt
- Put the processor in Clock stop mode and wait for ADC interrupt
- As soon as a conversion is completed, the ADC will raise an interrupt that will wake-up the processor.
- The ADC conversion value can then be read and processed.

See the "VERSA1's Analog Signal Path control SFRs" section for a complete description of the SFR involved with the ADC operation.

Internal Bandgap Reference and PGA

The VERSA1 provides an internal temperature stable Bandgap reference coupled to a programmable gain amplifier. These two units provide the reference voltage for the A/D converter and the internal programmable current source.

By default, at power-up, both Bandgap and PGA are in power down and must be enabled.

- To enable Bandgap internal reference: Set BGENABLE (bit 0) of the ADC control register (SFR 94h)
- To enable PGA: Set PGAENABLE (bit 0) of the PGA control Register (SFR F9h)

Both Bandgap and PGA are calibrated during production time. The associated calibration vectors are stored in the OTPR memory and must be loaded into the appropriate register during the program initialisation.

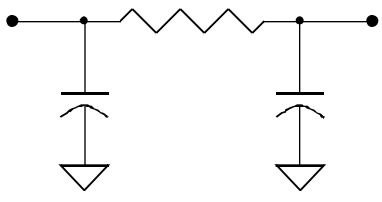
Using the factory calibration vector requires that the BGAPORDER bit (bit 7 of the ADC Input Mux Register) be set to 1.

It is possible to use an external reference instead of using the Bandgap, but in that case both PGA and the programmable current source will need to be recalibrated according to the external reference value.

The control of the internal versus external reference, the multiplexer current source drive, the ADC and their respective power downs are all done via µ-Processor control through SFR registers.

To improve noise rejection in noisy environments, it is recommended to buffer the internal Bandgap reference with a PI-filter. The user will also have to set MUXB [2:0] = 4h (output Mux control register bit 7) so that the Bandgap voltage is sent out through the TA pin of the VERSA1. Also the user will need to set SV0 bit to 1 (ADC control register bit 7) so that XTVREF will be used as the voltage reference. The following diagram outlines the circuit necessary.

FIGURE 22 RECOMMENDED PI FILTER FOR INTERNAL BANDGAP REFERENCE



See the "VERSA1's Analog Signal Path control SFRs" section for a complete description of the SFR involved with the Bandgap reference operation.

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Programmable current source

The VERSA1 is equipped with an on board current source that can be used to drive resistive sensors or bridges connected between the ISRC output and the RESIN input.

The current source can also be used as an external reference voltage or a voltage comparator.

The current source includes a feedback loop circuit that controls the current source output and stability. This feedback is provided by an external resistor that must be connected between RESIN and the analog ground. The feedback voltages that will be present at RESIN input are 200mV and 800mV.

This feedback voltage is essentially independent of the feedback resistor connected between RESIN and the analog ground. But the current source output depends on the feedback resistance value. For example, using a 6K feedback resistor, the VERSA1 current source output will be 33uA or 133uA depending of the Feedback voltage selection.

However, it is possible to use different resistor values to adjust the current source output to a specific application. However the maximum output current should be limited to 500uA.

The Programmable current source of the VERSA1 has been tested and calibrated during production time. The calibration vectors for the current source are stored into the OTPR memory.

Before using the programmable current source, the initialisation routine of the embedded program must perform the following operations:

- Enable internal Bandgap and set Bandgap order to 1
- Enable PGA
- Enable Programmable current source
- Copy Bandgap, PGA and Current source calibration vectors from the OTPR to the appropriate SFRs

Note that the programmable current source requires that the A/D be running when it is used.

See the “VERSA1’s Analog Signal Path control SFRs” section for a complete description of the SFR involved with the programmable current source operation.

OTPR Memory calibration Vectors

Each VERSA1 produced goes through an extensive test and calibration process during which functional tests are done on each peripheral as well as on the Bandgap, the PGA and the programmable current source. These calibration parameters, called “Calibration Vectors”, are stored in the OTPR memory of each VERSA1. They can be retrieved using MOVX instructions and then stored in the appropriate SFRs.

When the ADC and/or ISRC are to be used in conjunction with the Internal Bandgap reference, these calibration vectors must be retrieved and written to the appropriate SFR registers before these peripherals are used.

TABLE 24 BANDGAP, PGA AND ISRC CALIBRATION VECTORS LOCATION IN OTPR

B01h	Bg p D
B05h	G D T
B07h	200mV v
B09h	00mV v

In the case where an external reference is used, it will be necessary to perform a calibration of the PGA and the current source at production time. For this purpose the TA output can be used to monitor the PGA output as well as the RESIN for current source calibration. See the Electrical Characteristics table (**Table 2**) for admissible values.

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VERSA1's Analog Signal Path control SFRs

The following tables describe the SFR interface to the ADC Control Block, the Bandgap reference, the programmable current source, the PGA and the input and output multiplexers.

TABLE 25 ADC CLOCK DIVIDER REGISTER - SFR FEH

Bit #	Mnemonic	Function
7-0	ADCCDIV [7:0]	This 8-bit number controls the clock reference required for the correct operation of the ADC. The user should ensure that the clock reference to the A/D is as close to 250KHz as possible.

TABLE 26 CONVERSION RATE HIGH REGISTER - SFR F7H

Bit #	Mnemonic	Function
7-0	CONVRHI [7:0]	This register and the CONVRMED [7:0] & CONVRLO [7:0] registers for a 24-bit word that is used to set the time between continuous conversions of the ADC.

TABLE 27 CONVERSION RATE MED REGISTER - SFR F6H

Bit #	Mnemonic	Function
7-0	CONVRMED[7:0]	This register and the CONVRHI [7:0] & CONVRLO [7:0] registers for a 24-bit word that is used to set the time between continuous conversions of the ADC.

TABLE 28 CONVERSION RATE LOW REGISTER - SFR F5H

Bit #	Mnemonic	Function
7-0	CONVRLO[7:0]	This register and the CONVRHI [7:0] & CONVRMED [7:0] registers for a 24-bit word that is used to set the time between continuous conversions of the ADC.

TABLE 29 ADC CONTROL REGISTER - SFR 94H

Bit #	Mnemonic	Function
7	SV0	Controls switch for reference to PGA. 0 selects on-chip Bandgap. 1 selects external XTVREF input.
6	MANUAL	When MANUAL = 1, the conversion will be performed on the channel whose address is defined by the value of MUXA [2:0]. When MANUAL = 0, conversions will be performed on the 4 upper or lower channels of the Input multiplexer depending on the state of the MUXA [2] bit.
5	ONESHOT	When set to 1 to the ADC will implement an immediate single conversion of 1 or 4 channels.
4	ADCENABLE	When set to 0, this will power down the ADC.
3	ADCIC	When set to 1, this signal clears the ADC Interrupt.
2	ADCIE	When set to 1, this enables the ADC Interrupt to be driven to the Interrupt Control block.
1	CONT	When set to 1, this signal enables continuous ADC conversions of 1 or 4 channels.
0	BGENABLE	When set to 0, this signal powers down the on-chip Bandgap.

TABLE 30 ADC STATUS REGISTER - SFR BCH

Bit #	Mnemonic	Function
7-1	Not Used	
0	ADCINT	This signal provides the status of the ADC Interrupt and signals the end of an ADC conversion

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TABLE 31 ADC INPUT MUX CONTROL REGISTER - SFR FCH

Bit #	Mnemonic	Function
7	BGAPORDER	Controls order of on-chip Bandgap correction. When 0, correction is 1st order when 1, correction is 2nd order.
6-4	MUXA [2:0]	When the ADC runs in automatic 4 channel mode continuous or single shot Bit 6 = 0 ADC source channels are the 4 ADCIN inputs, MUXA [1:0] are ignored. Bit 6 = 1 ADC source channels are the 4 upper inputs of the multiplexer. MUXA [1:0] bits are ignored. When in single channel mode, all MUXA [2:0] bits must be initialised to define the source channel input to the A/D.
3-0	IBUFEN [3:0]	These signals each provide an active low power down for the input channel buffers.

TABLE 32 ADC CHANNEL 0 LOW REG - SFR A4H

Bit #	Mnemonic	Function
7-0	ADCD0LO [7:0]	This provides a read back of the 8 LSBs of the ADCD0 [11:0] register. Data corresponds to last ADC conversion.

TABLE 33 ADC CHANNEL 0 HIGH REG - SFR A5H

Bit #	Mnemonic	Function
7-4	Not Used	
3-0	ADCD0HI [11:8]	This provides a read back of the 4 MSBs of the ADCD0 [11:0] register. Data corresponds to the last ADC conversion.

TABLE 34 ADC CHANNEL 1 LOW REG - SFR A6H

Bit #	Mnemonic	Function
7-0	ADCD1LO [7:0]	This provides a read back of the 8 LSBs of the ADCD1 [11:0] register. Data corresponds to the last ADC conversion.

TABLE 35 ADC CHANNEL 1 HIGH REG - SFR A7H

Bit #	Mnemonic	Function
7-4	Not Used	
3-0	ADCD1HI [11:8]	This provides a read back of the 4 MSBs of the ADCD1 [11:0] register. Data corresponds to the last ADC conversion.

TABLE 36 ADC CHANNEL 2 LOW REG - SFR ACH

Bit #	Mnemonic	Function
7-0	ADCD2LO [7:0]	This provides a read back of the 8 LSBs of the ADCD2 [11:0] register. Data corresponds to the last ADC conversion.

TABLE 37 ADC CHANNEL 2 HIGH REG - SFR ADH

Bit #	Mnemonic	Function
7-4	Not Used	
3-0	ADCD2HI [11:8]	This provides a read back of the 4 MSBs of the ADCD2 [11:0] register. Data corresponds to the last ADC conversion.

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TABLE 38 ADC CHANNEL 3 LOW REG - SFR AEH

Bit #	Mnemonic	Function
7-0	ADCD3LO [7:0]	This provides a read back of the 8 LSBs of the ADCD3 [11:0] register. Data corresponds to the last ADC conversion.

TABLE 39 ADC CHANNEL 3 HIGH REGISTER - SFR AFH

Bit #	Mnemonic	Function
7-4	Not Used	
3-0	ADCD3HI [11:8]	This provides a read back of the 4 MSBs of the ADCD3 [11:0] register. Data corresponds to the last ADC conversion.

TABLE 40 ADC CALIBRATE DISABLE REGISTER - SFR 96H

Bit #	Mnemonic	Function
7-5	Not Used	
4	CALDSBL	Skip the auto calibration phase of ADC if set to 1
3-0	CALADR [3:0]	Calibration table address register

TABLE 41 BANDGAP CALIBRATE DATA REGISTER - SFR 95H

Bit #	Mnemonic	Function
7-0	BGCAL	Bandgap Calibration Data

TABLE 42 ANALOG OUTPUT MUX CONTROL REGISTER - SFR FDH

Bit #	Mnemonic	Function
7-4	Not Used	
3-1	MUXB [2:0]	This controls the signal that is selected to be driven out on the TA pin.
0	TAENABLE	A low on this signal disables the TA analog output.

TABLE 43 PGA CONTROL REGISTER - SFR F9H

Bit #	Mnemonic	Function
7-1	DPGA [6:0]	Calibration data for the Programmable Gain Amplifier (PGA)
0	PGAENABLE	When set to 0, this signal powers down the PGA.

TABLE 44 CURRENT SOURCE CONTROL REGISTER 1 - SFR FAH

Bit #	Mnemonic	Function
7-1	C1 [6:0]	Calibration data for the programmable divider used by the 33 A current source
0	ISRCENABLE	When set to 0, this signal powers down the current source circuitry.

TABLE 45 CURRENT SOURCE CONTROL REGISTER 2 - SFR FBH

Bit #	Mnemonic	Function
7-1	C4 [6:0]	Calibration data for the programmable divider used by the 133 A current source
0	SV1	When set to 0, the programmable current source provides a 33µA signal and when set to 1, it provides 133µA signal.

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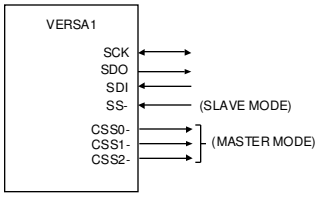
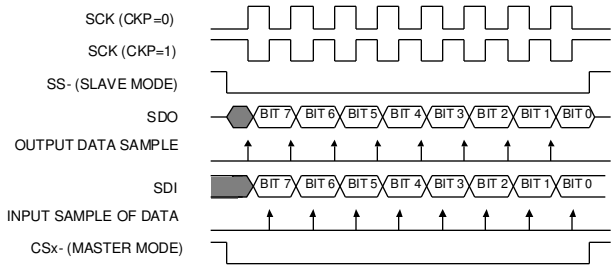
SPI Interface

FIGURE 23 SPI PIN INTERFACE



The VERSA1 SPI interface can operate as a master or slave device. In master mode, there are an additional 3 chip enable signals that can be used to allow 3 slave devices to share the SPI bus. The SPI interface is not affected by the clock divider. **Figure 24** describes the SPI bus timing:

FIGURE 24 SPI SLAVE/MASTER MODE TIMING



The following describes the SFR interface to the SPI control registers.

TABLE 46 SPI CONTROL REGISTER - SFR B4H

Bit #	Mnemonic	Function
7-6	Not Used	
5-4	CSSB [1:0]*	In master mode, this controls which chip enable is active during the SPI transfer.
3-2	MCLK [1:0]	In master mode, this signal is used to select the clock speed of the SPI's clock (SCK)
1	SPICLKP	In slave or master mode, this signal controls the polarity of the SPI clock.
0	SPIMA_SL	When set to 0, the SPI will function as a slave device. When set to 1, the SPI will function as a master.

* The following table describes the relationship between CSS_LCHOICE and the SPI chip enables in master mode:

TABLE 47 CSSB VS. MASTER MODE CHIP ENABLES FOR THE SPI

CSSB [1:0]	CS2-	CS1-	CS0-
00b	1	1	0
01b	1	0	1
10b	0	1	1
11b	1	1	1

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The following table describes the relationship between the external clock and the SPI clock (SCK) when in master mode:

TABLE 48 RELATIONSHIP BETWEEN SYSTEM CLOCK AND SPI CLOCK (SCK)

MCLK [1:0]	SCK (DIVIDE RATIO)
00b	External Clock ÷ 8
01b	External Clock ÷ 16
10b	External Clock ÷ 32
11b	External Clock ÷ 64

TABLE 49 SPI RECEIVE REGISTER - SFR B5H

Bit #	Mnemonic	Function
7-0	SPIRX [7:0]	This register is used to read the receive data from the SPI interface.

TABLE 50 SPI TRANSMIT REGISTER - SFR B6H

Bit #	Mnemonic	Function
7-0	SPITX [7:0]	Data written to this register will be transmitted out to the SPI bus.

TABLE 51 SPI INTERRUPT ENABLE REGISTER - SFR B7H

Bit #	Mnemonic	Function
7-3	Not Used	
2	SPIRXOVIE	When set to 1, this signal enables the receiver overrun interrupt to the processor.
1	SPIRXDAIE	When set to 1, this signal enables the receiver data available interrupt to the processor.
0	SPITXEMPIE	When set to 1, this signal enables the transmitter empty interrupt to the processor.

TABLE 52 SPI INTERRUPT STATUS REGISTER - SFR BCH

Bit #	Mnemonic	Function
7-3	Not Used	
2	SPIRXOV	When set to 1, this signal indicates that the data in the SPI Receive register has been over-written.
1	SPIRXDA	When set to 1, this signal indicates that an SPI transaction has occurred and there is data available in the SPI Receive register.
0	SPITXEMP	When set to 1, this signal indicates that the SPI Transmit register is empty and is ready to receive data to be transmitted.

TABLE 53 SPI RECEIVE OVERRUN CLEAR - SFR BDH

Bit #	Mnemonic	Function
7-0	SPIRXOVC	A write to this register will clear the SPIRXOV. Data written is a don't care.

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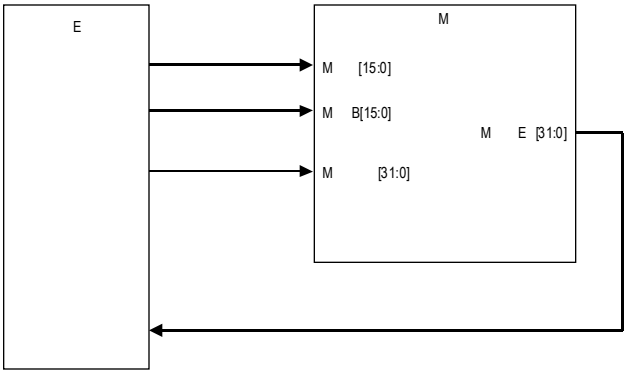
MAC

The VERSA1 includes a multiply-accumulator that can be used to significantly speed up arithmetic operations. This block allows the following calculation to be done:

(MACA * MACB) + MACACC = MACRESULT

Where MACA (multiplier), MACB (multiplicand), MACACC (accumulate) and MACRESULT (result) are 16, 16, 32 and 32 bits, respectively.

FIGURE 26 MAC CONNECTION TO THE PROCESSOR



Using the MAC

All arguments of the MAC block are all mapped into the SFR data space in byte-wise fashion, the processor must move each sub byte of each of the MACA, MACB and MACACC fields to the corresponding byte address. Once this is done, the processor can immediately read back the result in the byte fields of the MACRES.

Please note that the

- MACA, MACB and MACACC sets of registers are Write Only
- MACRES sets of registers are Read Only

The following tables describe the SFR interface to the MAC registers.

TABLE 62 MACA LSB REGISTER - SFR E6H

Bit #	Mnemonic	Function
7-0	MACA0 [7:0]	Lower 8 bits of the multiplier.

TABLE 63 MACA MSB REGISTER - SFR E7H

Bit #	Mnemonic	Description
7-0	MACA1 [15:8]	Upper 8 bits of the multiplier.

Note: MACA1 & MACA0 make up the full 16 bit MACA [15:0] argument.

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TABLE 64 MACB LSB REGISTER - SFR EEH

Bit #	Mnemonic	Function
7-0	MACB0[7:0]	Lower 8 bits of the multiplicand.

TABLE 65 MACB MSB REGISTER - SFR EFH

Bit #	Mnemonic	Function
7-0	MACB1[15:8]	Upper 8 bits of the multiplicand.

Note: MACB1[7:0] & MACB0[7:0] make up the full 16 bit MACB[15:0] argument.

TABLE 66 MACACC LSB REGISTER - SFR C4H

Bit #	Mnemonic	Function
7-0	MACACC0[7:0]	Least Significant Byte of the accumulator argument.

TABLE 67 MACACC UPPER BYTE OF THE LSDW REGISTER - SFR C5H

Bit #	Mnemonic	Function
7-0	MACACC1[15:8]	Upper byte of the Least Significant Data Word of the accumulator argument.

TABLE 68 MACACC LOWER BYTE OF THE MSDW REGISTER - SFR C6H

Bit #	Mnemonic	Function
7-0	MACACC2[23:16]	Lower byte of the Most Significant Data Word of the accumulator argument.

TABLE 69 MACACC MSB REGISTER - SFR C7H

Bit #	Mnemonic	Function
7-0	MACACC3[31:24]	Most Significant Byte of the accumulator argument.

Note: MACACC3, MACACC2, MACACC1 & MACACC0 registers make up the full 32 bits of the MACACC [31:0] argument.

TABLE 70 MACRESULT LSB REGISTER - SFR EAH

Bit #	Mnemonic	Function
7-0	MACRES0[7:0]	Least Significant Byte of the result.

TABLE 71 MACRESULT UPPER BYTE OF THE LSDW REGISTER - SFR EBH

Bit #	Mnemonic	Function
7-0	MACRES1[15:8]	Upper byte of the Least Significant Data Word of the result.

TABLE 72 MACRESULT LOWER BYTE OF THE MSDW REGISTER - SFR ECH

Bit #	Mnemonic	Function
7-0	MACRES2[23:16]	Lower byte of the Most Significant Data Word of the result.

TABLE 73 MACRESULT_HI_HI REGISTER - SFR EFH

Bit #	Mnemonic	Function
7-0	MACRES3[31:24]	Most Significant Byte of the result.

Note: MACRES3, MACRES2, MACRES1 & MACRES0 make up the full 32 bits of the MACRES [31:0] argument.

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General Purpose I/O

There are 2 general purposes, digital I/Os on the VERSA1. These can be set as inputs or outputs via software control. The following describes the SFR interface to the I/O control block.

TABLE 74 I/O CONTROL REGISTER - SFR BAH

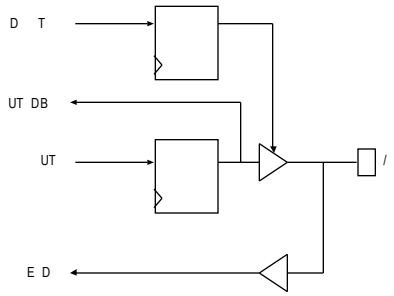
Bit #	Mnemonic	Function
7-4	Not Used	
3	DIRCTRL1	When set to 1, this signal configures I/O1 as an output. If set to 0, it is configured as an input.
2	IOOUT1	When I/O1 is configured as an output, setting this bit to 1 will drive a logic high on the I/O1 pin. Setting this bit to a 0 will drive a logic 0 on the I/O1 pin.
1	DIRCTRL0	When set to 1, this signal configures I/O0 as an output. If set to 0, it is configured as an input.
0	IOOUT0	When I/O0 is configured as an output, setting this bit to 1 will drive a logic high on the I/O0 pin. Setting this bit to a 0 will drive a logic 0 on the I/O0 pin.

TABLE 75 I/O READ BACK REGISTER - SFR BBH

Bit #	Mnemonic	Function
7-2	Not Used	
1	IOREAD1	This provides a read back of the logic level at pin I/O1
0	IOREAD0	This provides a read back of the logic level at pin I/O0

The following figure describes the general purpose I/O signals and their relationship with the I/O related registers.

FIGURE 27 GENERAL PURPOSE I/O BLOCK DIAGRAM



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Interrupts

The VERSA1 is a highly integrated device incorporating a vast number of peripherals for which a comprehensive set of 10 interrupt sources ease systems program development. Nearly all active peripherals in the VERSA1 can generate an interrupt to the MCU core indicating that an event occurred or a task is complete.

The following table summarizes the interrupt sources, natural priority and associated interrupt vector

TABLE 76 INTERRUPT SOURCES, VECTORS AND NATURAL PRIORITIES.

Interrupt	Description	Natural Priority	Interrupt Vector
Intperiph_n	SPI peripheral interrupt. Internal. Active low and configurable as edge-or level-sensitive. It is recommended that Intperiph_n interrupt be configured as level-sensitive, active low.	1	03h*
TF0	Timer 0 interrupt. Parts of VERSA1 MCU.	2	0Bh
INT1-	External interrupt 1, configurable as edge or level sensitive, active low.	3	13h
TF1	Timer 1 interrupt. Parts of VERSA1 MCU.	4	1Bh
TI_0 or RI_0	Serial Port 0 transmit or receive. Parts of VERSA1 MCU.	5	23h
TF2 or EXF2	Timer 2 interrupt. . Parts of VERSA1 MCU.	6	2Bh
TI_1 or RI_1	Serial Port 1 transmit or receive. Parts of VERSA1 MCU.	7	3Bh
Intadc	A/D Converter interrupt	8	43h
INT0-	External interrupt 0, edge sensitive, active low	9	4Bh
INT2	External interrupt 2, edge sensitive, active high	10	63h

Figure 28 describes the VERSA1 interrupt system architecture. Note that SPI uses the Intperiph_n interrupt vector. The VERSA1 includes an interrupt priority encoder for these interrupts. Therefore upon activation of Intperiph_n, the processor, in its interrupt service routine, can read from the Interrupt Source register (SFR E4h) in order to make a decision on which interrupt to deal with first.

Table 77 describes the SPI interrupt source priority and the corresponding value read back from the Interrupt Source Register.

FIGURE 28 INTERRUPT CONNECTION DIAGRAM

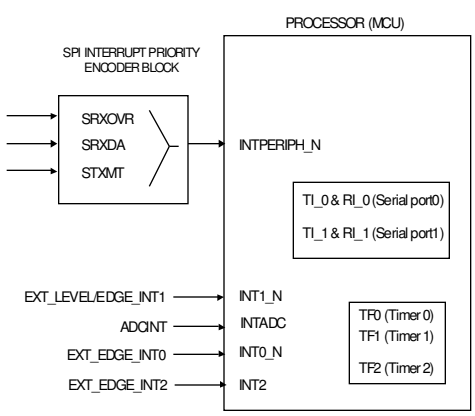

TABLE 77 PRIORITIES FOR INTPERIPH_N INTERRUPT AND INTERRUPT SOURCE REGISTER (SFR E4H) ASSOCIATED VALUE.

Interrupt Source	Priority	Value Read
SPI RX OVER RUN	1	01h
SPI TX EMPTY	2	03h
SPI RX DATA AVAIL	3	05h
NO INTERRUPTS	-	00h

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Interrupt Priorities

There is two stages of interrupt priority assignment: interrupt level and natural priority. The interrupt level (highest, high, or low) takes precedence over natural priority. The Peripheral Interrupt always has highest natural priority.

In addition to an assigned priority level (high or low), each interrupt has a natural priority, as listed in **Table 76** Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. For example, if *intperiph_n* and *intadc* are both programmed as high priority, *inperiph_n* takes precedence.

Once an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.

It is possible to give an interrupt a higher priority by setting the corresponding IP or EIP register bit.

Table 78, summarises the interrupt flags, interrupt enabling bits, and priority control bits.

TABLE 78 INTERRUPT FLAGS, ENABLES, AND PRIORITY CONTROL

Interrupt	Description	Flag	Enable	Priority Control
Intperiph_n*	SPI Peripheral interrupt	TCON.1	IE.0	IP.0
TF0	Timer 0 interrupt	TCON.5	IE.1	IP.1
INT1-	External interrupt 1	TCON.3	IE.2	IP.2
TF1	Timer 1 interrupt	TCON.7	IE.3	IP.3
TI_0 or RI_0	Serial Port 0 transmit or receive	SCON0.0 (RI_0), SCON0.1 (TI_0)	IE.4	IP.4
TF2 or EXF2	Timer 2 Interrupt	T2CON.7 (TF2) T2CON.6 (EXF2)	IE.5	IP 5
TI_1 or RI_1	Serial Port 1 transmit or receive	SCON1.0 (RI_1) SCON1.1 (TI_1)	IE.6	IP.6
Intadc	A/D Converter interrupt	EXIF.4	EIE.0	EIP.0
INT0-	External interrupt 0	EXIF.5	EIE.1	EIP.1
INT2	External interrupt 2	EICON.3	EIE.4	EIP.4

*See **Table 77** for priority order or SPI interrupts that are combined to generate intperiph_n interrupt

Interrupt Processing

When an enabled interrupt occurs, the CPU vectors to the address of the interrupt service routine (ISR) associated with that interrupt, as listed in **Table 76**. The CPU executes the ISR to completion unless another interrupt of higher priority occurs. Each ISR ends with a RETI (return from interrupt) instruction. After executing the RETI, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An ISR for a low-level interrupt can only be interrupted by high-level interrupt. An ISR for a high-level interrupt can only be interrupted by the power-fail interrupt (extended interrupt unit only). The VERSA1 always completes the instruction in progress before servicing an interrupt. If the instruction in progress is RETI, or a write access to any of the IP, IE, EIP, or EIE SFRs, the VERSA1 completes one additional instruction before servicing the interrupt.

Interrupt Masking

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts. When EA = 1, each interrupt is enabled/masked by its individual enable bit. When EA = 0, all interrupts are masked. The only exception is the power-fail interrupt, which is not affected by the EA bit.

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Interrupt SFRs

The following SFRs are associated with interrupt control:

- IE -SFR A8h (**Table 79**))
- IP -SFR B8h (**Table 80**)
- EXIF -SFR 91h **(Table 81**)
- EICON -SFR D8h (***Table 82***))
- EIE -SFR E8h (**Table 83**)
- EIP -SFR F8h (**Table 84**)
- INTSRC – SFR E4h (**Table 85**)

The IE and IP SFRs provide interrupt enable and priority control for the standard interrupt unit, as with the standard 8051. The EXIF, EICON, EIE, and EIP registers provide flags, enable control, and priority control for extended interrupt unit integrated in the VERSA1 MCU.

TABLE 79 IE REGISTER -SFR A8H

Bit #	Mnemonic	Function
7	EA	Global interrupt enable. EA = 0 disables all interrupts (EA overrides individual interrupt enable bits). When EA = 1, each interrupt is enabled or masked by its individual enable bit.
6	ES1	Enable Serial Port 1 interrupt. ES1 = 0 disables Serial Port 1 interrupts (TI_1 and RI_1). ES1 = 1 enables interrupts generated by the TI_1 or RI_1 flag.
5	ET2	Enable Timer 2 interrupt. ET2 = 0 disable Timer 2 interrupt (TF2). ET2 = 1 enables interrupts generated by the TI_0 or RI_0 flag.
4	ES0	Enable Serial Port 0 interrupt. ES0 = 0 disables Serial Port 0 interrupts (TI_0 and RI_0). ES0 = 1 enables interrupts generated by the TI_0 or RI_0 flag.
3	ET1	Enable Timer 1 interrupt. ET1 = 0 disables Timer 1 interrupt (TF1). ET1 = 1 enables interrupts generated by the TF1 flag.
2	EX1	Enable external interrupt 1. EX1 = 0 disables external interrupt 1 (INT1-). EX1 = 1 enables interrupts generated by the INT1- pin.
1	ET0	Enable Timer 0 interrupt. ET0 = 0 disables Timer 0 interrupt (TF0). ET0 = 1 enables interrupts generated by the TF0 flag.
0	EX0	Enable Peripheral interrupt. EX0 = 0 disables Peripheral interrupt (intperiph_n). EX0 = 1 enables interrupts generated by the intperiph_n pin.

TABLE 80 IP REGISTER -SFR B8H

Bit #	Mnemonic	Function
7		Reserved. Read as 1.
6	PS1	Serial Port 1 interrupt priority control. PS1 = 0 sets Serial Port 1 interrupt (TI_1 or RI_1) to low priority. PS1 = 1 sets Serial Port 1 interrupt to high priority
5	PT2	Timer 2 interrupt priority control. PT2 = 0 sets timer 2 interrupt (TF2) to low priority. PT2 = 1 sets Timer 2 interrupt to high priority.
4	PS0	Serial Port 0 interrupt priority control. PS0 = 0 sets Serial Port 0 interrupt (TI_0 or RI_0) to low priority. PS0 = 1 sets Serial Port 0 interrupt to high priority.
3	PT1	Timer 1 interrupt priority control. PT1 = 0 sets Timer 1 interrupt (TF1) to low priority. PT1 = 1 sets Timer 1 interrupt to high priority.
2	PX1	External interrupt 1 priority control. PX1 = 0 sets external interrupt 1 (INT1-) to low priority. PT1 = 1 sets external interrupt 1 to high priority.
1	PT0	Timer 0 interrupt priority control. PT0 = 0 sets Timer 0 interrupt (TF0) to low priority. PT0 = 1 sets Timer 0 interrupt to high priority.
0	PX0	External interrupt 0 priority control. PX0 = 0 sets external interrupt 0 (INT0-) to low priority. PT0 = 1 sets external interrupt 0 to high priority.

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TABLE 81 EXIF REGISTER- SFR 91H

Bit #	Mnemonic	Function
7-6		Reserved
5	IE3	External interrupt 0 flag. IE3 = 1 indicates that a falling edge was detected at the INT0- pin. IE3 must be cleared by software. Setting IE3 in software generates an interrupt, if enabled.
4	IE2	A/D Converter interrupt flag. IE2 = 1 indicates that a rising edge was detected at the intadc pin. IE2 must be cleared by software. Setting IE2 in software generates an interrupt, if enabled.
3		Reserved. Read as 1.
2-0		Reserved. Read as 0.

TABLE 82 EICON REGISTER -SFR D8H

Bit #	Mnemonic	Function
7	SMOD1	Serial Port 1 baud rate doubler enable. When SMOD1 = 1, the baud rate for Serial Port 1 is doubled.
6		Reserved. Read as 1.
5-4		Reserved
3	EXT2	External interrupt 2 flag. EXT2 = 1 indicates an interrupt was detected at the INT2 pin. EXT2 must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting EXT2 in software generates an external interrupt 2, if enabled.
2-0		Reserved. Read as 0.

TABLE 83 EIE REGISTER- SFR E8H

Bit #	Mnemonic	Function
7-5		Reserved. Read as 1.
4	EIE2	Enable external interrupt 2. EIE2 = 0 disables external interrupt 2 (INT2). EIE2 = 1 enables interrupts generated by INT2 pin.
3-2		Reserved
1	EX3	Enable external interrupt 0. EX3 = 0 disables external interrupt 0 (INT0-). EX3 = 1 enables interrupts generated by the int3_n pin.
0	EX2	Enable A/D Converter interrupt. EX2 = 0 disables A/D Converter interrupt (intadc). EX2 = 1 enables interrupts generated by the intadc pin.

TABLE 84 EIP REGISTER- SFR F8H

Bit #	Mnemonic	Function
7-5		Reserved. Read as 1.
4	PEI2	Enable external interrupt 2 priority control. PEI2 = 0 sets external interrupt 2 (INT2) to low priority. PEI2 = 1 sets external interrupt 2 to high priority.
3-2		Reserved.
1	PEX3	Enable external interrupt 0 priority control. PEX3 = 0 sets external interrupt 0 (INT0-) to low priority. PEX3 = 1 sets external interrupt 0 to high priority.
0	PEX2	Enable A/D Converter interrupt priority control. PEX2 = 0 sets A/D Converter interrupt (intadc) to low priority. PEX2 = 1 sets A/D Converter interrupt to high priority.

TABLE 85 INTERRUPT SOURCE REGISTER - SFR E4H

Bit #	Mnemonic	Function
7-0	INTSRC [7:0]	Interrupt priority encoder output for SPI based interrupts.

Interrupt Sampling

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The internal timers and serial ports generate interrupts by setting their respective SFR interrupt flag bits. The VERSA1 samples external interrupts once per instruction cycle, at the rising edge of *clk* at the end of cycle C4 of system clock.

INT0- and INT2 interrupts are edge-sensitive only. INT2 is active high and INT0- is active low.

External INT1- is active low and can be programmed to be either edge-sensitive or level-sensitive, through the IT1 bit in the TCON SFR. For example, when IT1 = 0., INT1- is level-sensitive and the VERSA1 sets the IE1 flag when the INT1- pin is sampled low. When IT1 = 1, INT1- is edge-sensitive and the VERSA1 sets the IE1 flag when the INT1- pin is sampled high then low on consecutive samples.

To ensure that edge-sensitive interrupts are detected they should be held high for 4 *clk cycles* and then low for 4 *clk* cycles. Level-sensitive interrupts are not latched and must remain active until serviced.

Interrupt Latency

Interrupt response time depends on the current state of the VERSA1. The fastest response time is 5 instruction cycles: 1 to detect the interrupt, and 4 to perform the *LCALL* to the ISR.

The maximum latency (13 instruction cycles) occurs when the VERSA1 is currently executing a RETI instruction followed by a MUL or DIV instruction. The 13 instruction cycles in this case are: 1 to detect the interrupt, 3 to complete the RETI, 5 to execute the DIV or MUL, and 4 to execute the LCALL to the ISR. For the maximum latency case, the response time is 13 x 4 = 52 *clk* cycles.

Single-Step Operation

The VERSA1 interrupt structure provides a way to perform single-step program execution. When exiting an ISR with an RETI instruction, the VERSA1 will always execute at least one instruction of the task program. Therefore, once an ISR is entered, it cannot be re-entered until at least one program instruction is executed.

To perform single-step execution, program one of the external interrupts (for example, *int1)* to be level-sensitive and write an ISR for that interrupt that terminates as follows:

```
INT1_SERV_ROUTINE:

WAIT_INT1_HI:                JNB     TCON.3,WAIT_INT1_HI          ; wait for high on INT1-
WAIT_INT1_LO:                JB      TCON.3,WAIT_INT1_LO          ; wait for low on INT1-
                             RETI                                 ; return from ISR
```

The CPU enters the ISR when INT1- goes low, then waits for a pulse on INT1-. Each time INT1- *is* pulsed, the CPU exits the ISR, executes one program instruction then re-enters the ISR.

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Reset

The VERSA1 provides two resets, *por_n* and RES-. *por_n* is the power-on reset which is generated internally by the Power-On-Reset/Brown-Out device. RES- provides the functionality of the standard 8051 RST input.

For either reset source, the VERSA1 remains in the reset state until the reset signal is removed. Both sources of reset initialize the SFRs to their reset values, as listed in **Table 6**. The internal RAM is not affected by either *por_n* or *RES-*. When the activated reset signal is removed, the VERSA1 exits the reset state and begins program execution at the standard reset vector address 0000h.

Power On Reset

The internal *por_n* input will be driven low for at least 10ms to ensure proper initialization.

Standard Reset

RES- provides the same functionality as the standard 8051 RST input, with inverse polarity. RES- must be asserted (active low) for at least 2 instruction cycles (8 system clk cycles). Shorter pulses on RES- may be ignored.

Power Saving Modes

Clock Control Circuitry

The VERSA1 clock allows the user to slow down or completely shut off the on-board clocks that drive all the digital logic. This is useful for applications that require low power operation. In addition to this, there is also a feature whereby if the clock has been turned off or slowed down and an interrupt occurs that is associated with specific on-board peripherals, then the clock will return to running at the full speed until the interrupt is cleared. The interrupts associated with this mechanism are:

- ADC
- SPI interrupt (through intperiph_n)
- External INT0-
- External INT1-
- External INT2

The following describes the SFR interface to the clock control circuitry.

TABLE 86 CLOCK DIVIDER CONTROL REGISTER - SFR E5H

Bit #	Mnemonic	Function
7-4	Not Used	
3-1	DIVCTL [2:0]*	This signal controls the digital logic clock speed.
0	NORMSPD	When set to 1, upon detection of an interrupt, the digital logic clock speed will return to the maximum until the associated interrupt is cleared.

*The following table describes the relationship between the external clock frequency and the system clock that drives the internal processor and logic as controlled by DIVCTL [2:0].

TABLE 87 RESULTS OF DIVCTL SETTINGS

DIVCTL [2:0]	Internal Clock	System Clk for Ext Clock = 16MHz
000b	External Clock ÷ 2	8 MHz
001b	External Clock ÷ 4	4 MHz
010b	External Clock ÷ 8	2 MHz
011b	External Clock ÷ 16	1 MHz
100b	External Clock ÷ 32	500 kHz
101b	External Clock ÷ 64	250 kHz
110b	External Clock ÷ 128	125 kHz
111b	0MHz (clock stopped)	0 Hz (clock stopped)

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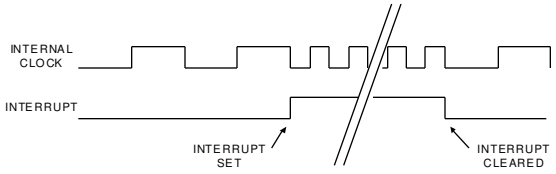
The following figure describes the internal clock timing relationship when an interrupt occurs and is cleared when NORMSPD bit is set to 1.

FIGURE 29 CLOCK TIMING WHEN AN INTERRUPT OCCURS



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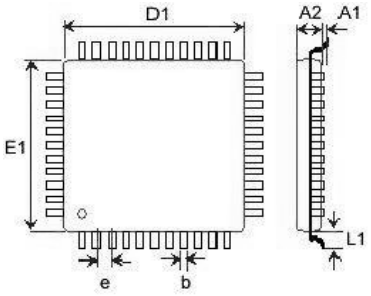
Package Information

The VERSA1 is available in the industry standard QFP-44 pins package.

FIGURE 31 VERSA1 PACKAGE PARAMETERS



Stand-off	A1	0.25 to 0.50
Body thickness	A2	2.00 max
Lead length	L1	1.60
Lead width	b	0.35
Lead thickness	-	0.17
Lead pitch	e	0.8
Body size	D1	10
Body size	E1	10

Ordering Information

Goal Part Number	Package	Operating voltage	Temperature Range	Speed
VRS1001-QAC20	QFP-44	4.75V – 5.5V	0°C to +70°C	20MHz
VRS1001-QAI20	QFP-44	4.75V – 5.5V	-40°C to +85°C	20MHz

Disclaimer

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