FUJITSU SEMICONDUCTOR
DATA SHEET

DS706-00043-2v0-E

32-bit ARM™ Cortex™-M3 based Microcontroller

FM3 MB9A130LA Series

MB9AF131KA/LA, MB9AF132KA/LA

■ DESCRIPTION

The MB9A130LA Series are highly integrated 32-bit microcontrollers that dedicated for embedded controllers with low-power consumption mode and competitive cost.
The MB9A130LA Series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I^2C).

The products which are described in this data sheet are placed into TYPE3 product categories in "FM3 Family PERIPHERAL MANUAL".

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ARM™

2012.10

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■ FEATURES

● 32-bit ARM Cortex-M3 Core

- Processor version: r2p1
- Up to 20MHz Operation Frequency
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 channel NMI (non-maskable interrupt) and 32 channels' peripheral interrupts and 8 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

● On-chip Memories

[Flash memory]

- Up to 128 Kbytes
- Read cycle: 0 wait-cycle
- Security function for code protection

[SRAM]

This series contains 8Kbyte on-chip SRAM memories. This is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus or D-code bus of Cortex-M3 core. SRAM1 is connected to System bus of Cortex-M3 core.

- SRAM0: None
- SRAM1: 8 Kbytes

● Multi-function Serial Interface (Max 8channels)

Operation mode is selectable from the followings for each channel.

- UART
- CSIO
- I^2C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[I^2C]

Standard mode (Max 100kbps) / High-speed mode (Max 400Kbps) supported

● A/D Converter (Max 8channels)

[12-bit A/D Converter]

- Successive Approximation type
- Conversion time: Min. 1.0µs
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

● Base Timer (Max 8channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

● General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 52 fast general purpose I/O Ports@64pin Package
- Some pins are 5V tolerant I/O
  See "■ LIST OF PIN FUNCTIONS" and "■ I/O CIRCUIT TYPE" to confirm the corresponding pins.

● Multi-function Timer

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch.
- Input capture × 4ch.
- Output compare × 6ch.
- A/D activating compare × 3ch.
- Waveform generator × 3ch.
- 16-bit PPG timer × 3ch.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

● Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

● External Interrupt Controller Unit

- Up to 8 external interrupt input pins
- Include one non-maskable interrupt (NMI) input pin

● Watchdog Timer (2channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by built-in low-speed CR oscillator. Therefore, "Hardware" watchdog is active in any low power consumption mode except RTC and STOP and Deep stand-by RTC and Deep stand-by STOP.

● Clock and Reset

[Clocks]

Five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL) that are dynamically selectable.

- Main Clock : 4 MHz to 20MHz
- Sub Clock : 32.768kHz
- Built-in high-speed CR Clock : 4MHz
- Built-in low-speed CR Clock : 100kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

● Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external clock failure (clock stop) is detected, reset is asserted.
- If external frequency anomaly is detected, interrupt or reset is asserted.

● Low Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage has been set, Low Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

● Low Power Consumption Mode

Six low power consumption modes supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep stand-by RTC
- Deep stand-by STOP

Back up register is 16bytes.

- **Debug**
  Serial Wire JTAG Debug Port (SWJ-DP)

- **Power Supply**
  Wide range voltage : VCC = 1.8V to 5.5V

■ PRODUCT LINEUP

● Memory size

Product name		MB9AF131KA/LA	MB9AF132KA/LA
On-chip Flash		64Kbytes	128Kbytes
On-chip SRAM	SRAM1	8Kbytes	8Kbytes

● Function

Product name			MB9AF131KA MB9AF132KA	MB9AF131LA MB9AF132LA
Pin count			48	64
CPU			Cortex-M3	
	Freq.		20MHz	
Power supply voltage range			1.8V to 5.5V	
MF Serial Interface (UART/CSIO/I^{2}C)			4ch. (Max) (CSIO and I^{2}C is Max 3ch.)	8ch. (Max)
Base Timer (PWC/ Reload timer/PWM/PPG)			8ch. (Max)	
MF-Timer	A/D activation compare	3ch.	1 unit (Max)	
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
Real-time clock			1 unit	
Watchdog timer			1ch. (SW) + 1ch. (HW)	
External Interrupts			6pins (Max) + NMI × 1	8pins (Max) + NMI × 1
general purpose I/O ports			37pins (Max)	52pins (Max)
12-bit A/D converter			6ch. (1 unit)	8ch. (1 unit)
CSV (Clock Super Visor)			Yes	
LVD (Low Voltage Detector)			2ch.	
Internal CR	High-speed		4MHz (± 2%)	
	Low-speed		100kHz (Typ)	
Debug Function			SWJ-DP	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.

■ PACKAGES

Package \ Product name	MB9AF131KA MB9AF132KA	MB9AF131LA MB9AF132LA
LQFP: FPT-48P-M49 (0.5mm pitch)	❍	-
QFN: LCC-48P-M73	❍	-
LQFP: FPT-64P-M24/M38 (0.5mm pitch)	-	❍
LQFP: FPT-64P-M39 (0.65mm pitch)	-	❍
QFN: LCC-64P-M24	-	❍

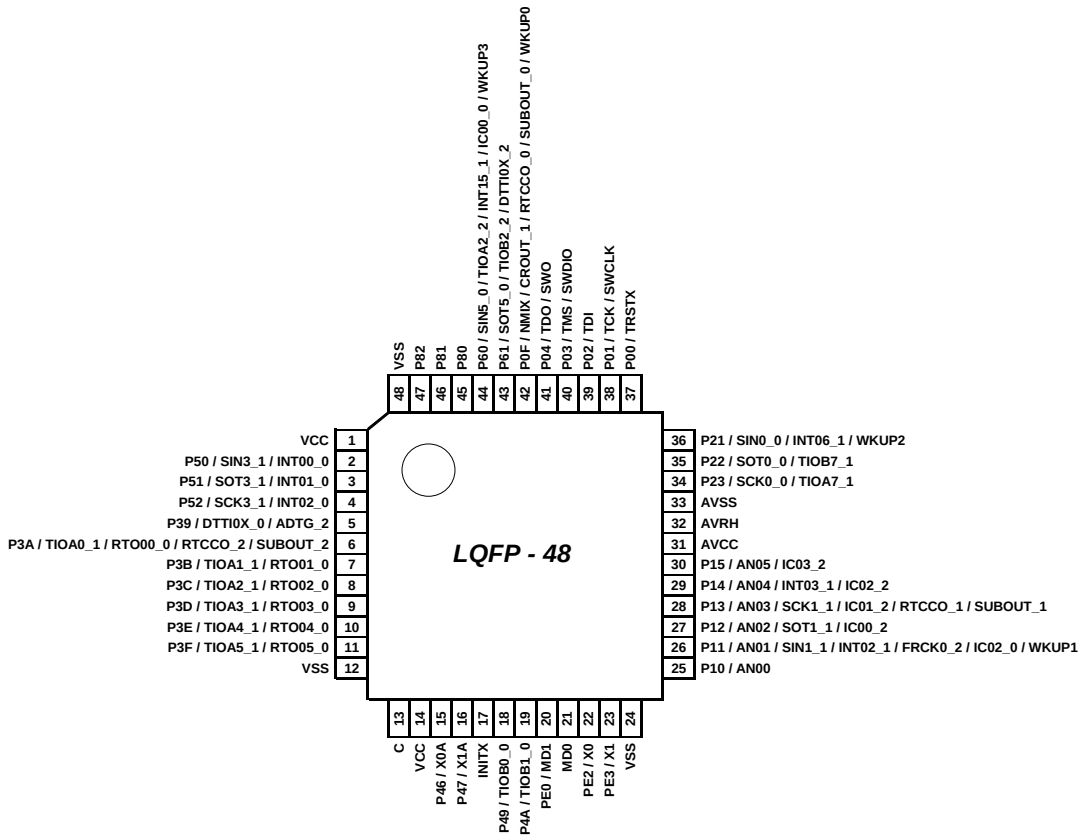
❍ : Supported

Note : See "■PACKAGE DIMENSIONS" for detailed information on each package.

■ PIN ASSIGNMENT

• FPT-48P-M49

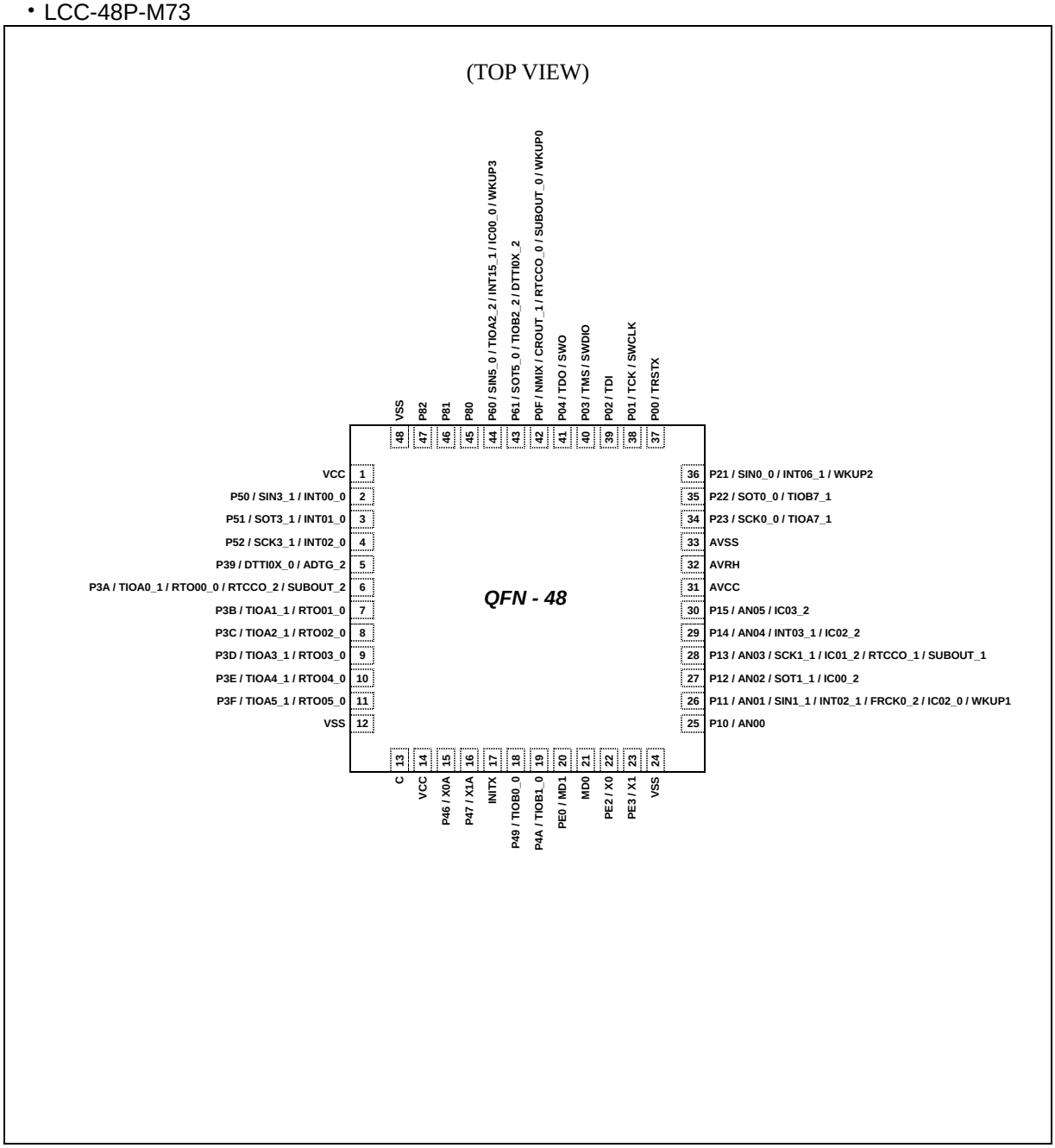
(TOP VIEW)



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

• LCC-48P-M73



<Note>

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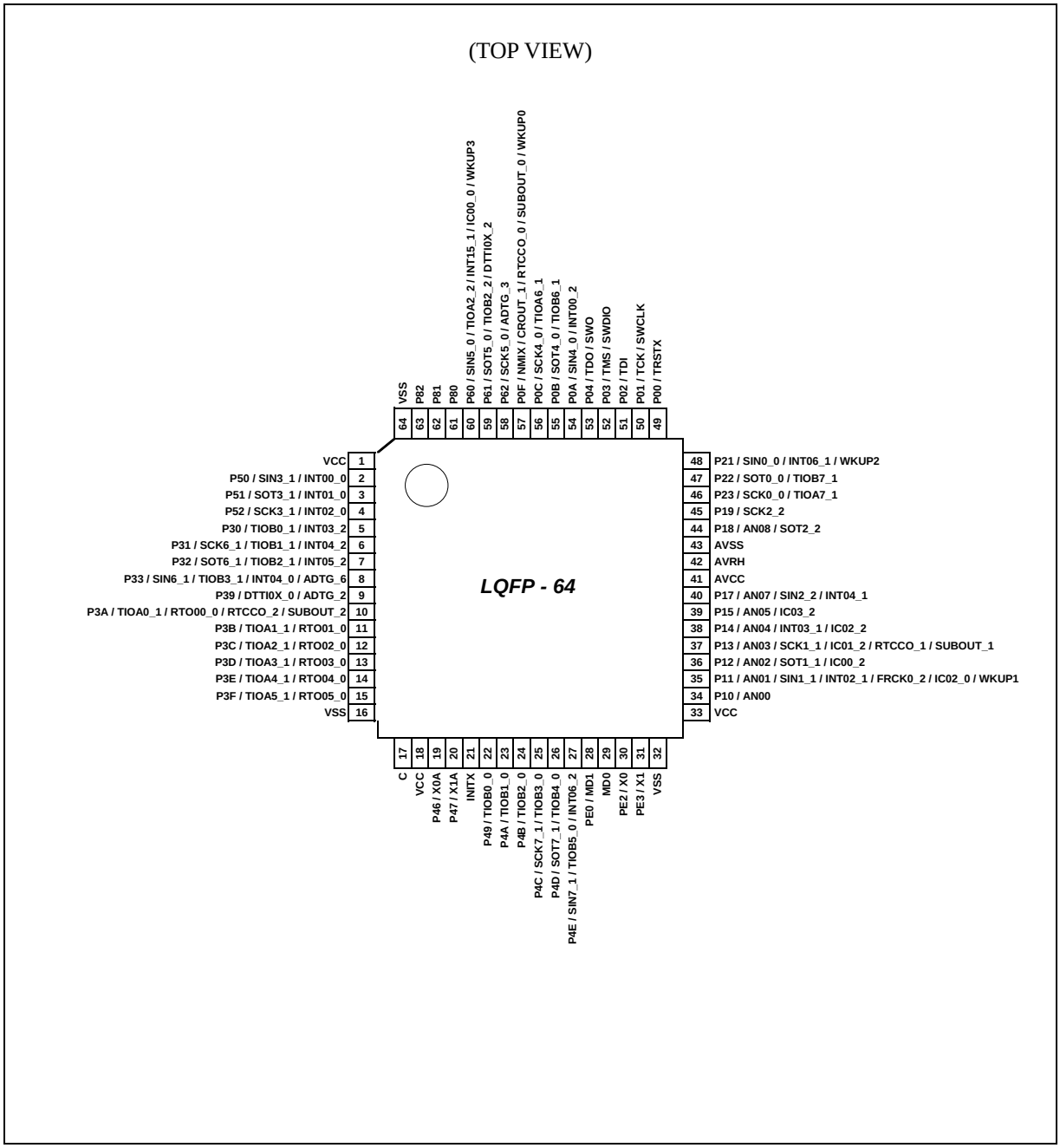
• FPT-64P-M24/M38/M39



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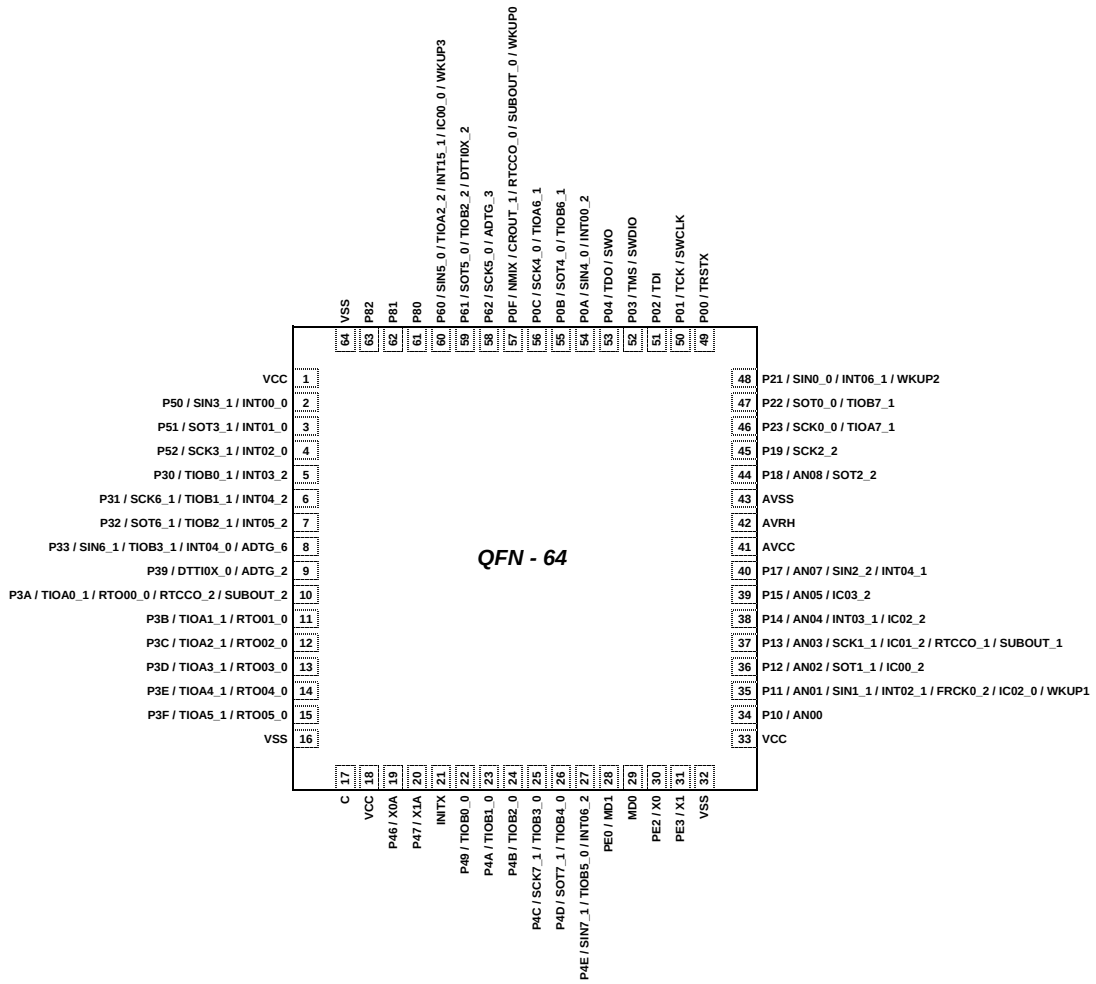
• LCC-64P-M24

(TOP VIEW)



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The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ LIST OF PIN FUNCTIONS

- List of pin numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48			
1	1	VCC	-	
2	2	P50	G	F
		INT00_0		
		SIN3_1		
3	3	P51	G	F
		INT01_0		
		SOT3_1 (SDA3_1)		
4	4	P52	G	F
		INT02_0		
		SCK3_1 (SCL3_1)		
5	-	P30	E	F
		TIOB0_1		
		INT03_2		
6	-	P31	E	F
		TIOB1_1		
		SCK6_1 (SCL6_1)		
		INT04_2		
7	-	P32	E	F
		TIOB2_1		
		SOT6_1 (SDA6_1)		
		INT05_2		
8	-	P33	E	F
		INT04_0		
		TIOB3_1		
		SIN6_1		
		ADTG_6		
9	5	P39	E	H
		DTTI0X_0		
		ADTG_2		
10	6	P3A	E	H
		RTO00_0 (PPG00_0)		
		TIOA0_1		
		RTCCO_2		
		SUBOUT_2		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48			
11	7	P3B	E	H
		RTO01_0 (PPG00_0)		
		TIOA1_1		
12	8	P3C	E	H
		RTO02_0 (PPG02_0)		
		TIOA2_1		
13	9	P3D	E	H
		RTO03_0 (PPG02_0)		
		TIOA3_1		
14	10	P3E	E	H
		RTO04_0 (PPG04_0)		
		TIOA4_1		
15	11	P3F	E	H
		RTO05_0 (PPG04_0)		
		TIOA5_1		
16	12	VSS	-	
17	13	C	-	
18	14	VCC	-	
19	15	P46	D	M
		X0A		
20	16	P47	D	N
		X1A		
21	17	INITX	B	C
22	18	P49	E	H
		TIOB0_0		
23	19	P4A	E	H
		TIOB1_0		
24	-	P4B	E	H
		TIOB2_0		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48			
25	-	P4C	E	H
		TIOB3_0		
		SCK7_1 (SCL7_1)		
26	-	P4D	E	H
		TIOB4_0		
		SOT7_1 (SDA7_1)		
27	-	P4E	E	F
		TIOB5_0		
		INT06_2		
		SIN7_1		
28	20	PE0	C	P
		MD1		
29	21	MD0	H	D
30	22	PE2	A	A
		X0		
31	23	PE3	A	B
		X1		
32	24	VSS	-	
33	-	VCC	-	
34	25	P10	F	J
		AN00		
35	26	P11	F	L
		AN01		
		SIN1_1		
		INT02_1		
		FRCK0_2		
		IC02_0		
		WKUP1		
36	27	P12	F	J
		AN02		
		SOT1_1 (SDA1_1)		
		IC00_2		
37	28	P13	F	J
		AN03		
		SCK1_1 (SCL1_1)		
		IC01_2		
		RTCCO_1		
		SUBOUT_1		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48			
38	29	P14	F	K
		AN04		
		INT03_1		
		IC02_2		
39	30	P15	F	J
		AN05		
		IC03_2		
40	-	P17	F	K
		AN07		
		SIN2_2		
		INT04_1		
41	31	AVCC	-	
42	32	AVRH	-	
43	33	AVSS	-	
44	-	P18	F	J
		AN08		
		SOT2_2 (SDA2_2)		
45	-	P19	E	H
		SCK2_2 (SCL2_2)		
46	34	P23	G	H
		SCK0_0 (SCL0_0)		
		TIOA7_1		
47	35	P22	G	H
		SOT0_0 (SDA0_0)		
		TIOB7_1		
48	36	P21	G	G
		SIN0_0		
		INT06_1		
		WKUP2		
49	37	P00	E	E
		TRSTX		
50	38	P01	E	E
		TCK		
		SWCLK		
51	39	P02	E	E
		TDI		

Pin No		Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-48 QFN-48			
52	40	P03	E	E
		TMS		
		SWDIO		
53	41	P04	E	E
		TDO		
		SWO		
54	-	P0A	E	F
		SIN4_0		
		INT00_2		
55	-	P0B	E	H
		SOT4_0 (SDA4_0)		
		TIOB6_1		
56	-	P0C	E	H
		SCK4_0 (SCL4_0)		
		TIOA6_1		
57	42	P0F	E	I
		NMIX		
		CROUT_1		
		RTCCO_0		
		SUBOUT_0		
		WKUP0		
58	-	P62	I	H
		SCK5_0 (SCL5_0)		
		ADTG_3		
59	43	P61	I	H
		SOT5_0 (SDA5_0)		
		TIOB2_2		
		DTTI0X_2		
60	44	P60	I	G
		SIN5_0		
		TIOA2_2		
		INT15_1		
		IC00_0		
		WKUP3		
61	45	P80	G	O
62	46	P81	G	O
63	47	P82	G	O
64	48	VSS	-	

- List of pin functions

  The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
ADC	ADTG_2	A/D converter external trigger input pin	9	5
	ADTG_3		58	-
	ADTG_6		8	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	34	25
	AN01		35	26
	AN02		36	27
	AN03		37	28
	AN04		38	29
	AN05		39	30
	AN07		40	-
	AN08		44	-
Base Timer 0	TIOA0_1	Base timer ch.0 TIOA pin	10	6
	TIOB0_0	Base timer ch.0 TIOB pin	22	18
	TIOB0_1		5	-
Base Timer 1	TIOA1_1	Base timer ch.1 TIOA pin	11	7
	TIOB1_0	Base timer ch.1 TIOB pin	23	19
	TIOB1_1		6	-
Base Timer 2	TIOA2_1	Base timer ch.2 TIOA pin	12	8
	TIOA2_2		60	44
	TIOB2_0	Base timer ch.2 TIOB pin	24	-
	TIOB2_1		7	-
	TIOB2_2		59	43
Base Timer 3	TIOA3_1	Base timer ch.3 TIOA pin	13	9
	TIOB3_0	Base timer ch.3 TIOB pin	25	-
	TIOB3_1		8	-
Base Timer 4	TIOA4_1	Base timer ch.4 TIOA pin	14	10
	TIOB4_0	Base timer ch.4 TIOB pin	26	-
Base Timer 5	TIOA5_1	Base timer ch.5 TIOA pin	15	11
	TIOB5_0	Base timer ch.5 TIOB pin	27	-
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	56	-
	TIOB6_1	Base timer ch.6 TIOB pin	55	-
Base Timer 7	TIOA7_1	Base timer ch.7 TIOA pin	46	34
	TIOB7_1	Base timer ch.7 TIOB pin	47	35
Debugger	SWCLK	Serial wire debug interface clock input pin	50	38
	SWDIO	Serial wire debug interface data input / output pin	52	40
	SWO	Serial wire viewer output pin	53	41
	TRSTX	J-TAG reset Input pin	49	37
	TCK	J-TAG test clock input pin	50	38
	TDI	J-TAG test data input pin	51	39
	TMS	J-TAG test mode state input/output pin	52	40
	TDO	J-TAG debug data output pin	53	41

Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2
	INT00_2		54	-
	INT01_0	External interrupt request 01 input pin	3	3
	INT02_0	External interrupt request 02 input pin	4	4
	INT02_1		35	26
	INT03_1	External interrupt request 03 input pin	38	29
	INT03_2		5	-
	INT04_0	External interrupt request 04 input pin	8	-
	INT04_1		40	-
	INT04_2		6	-
	INT05_2	External interrupt request 05 input pin	7	-
	INT06_1	External interrupt request 06 input pin	48	36
	INT06_2		27	-
	INIT15_1	External interrupt request 15 input pin	60	44
	NMIX	Non-Maskable Interrupt input pin	57	42
GPIO	P00	General-purpose I/O port 0	49	37
	P01		50	38
	P02		51	39
	P03		52	40
	P04		53	41
	P0A		54	-
	P0B		55	-
	P0C		56	-
	P0F		57	42
	P10	General-purpose I/O port 1	34	25
	P11		35	26
	P12		36	27
	P13		37	28
	P14		38	29
	P15		39	30
	P17		40	-
	P18		44	-
	P19		45	-
	P21	General-purpose I/O port 2	48	36
	P22		47	35
	P23		46	34

Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
GPIO	P30	General-purpose I/O port 3	5	-
	P31		6	-
	P32		7	-
	P33		8	-
	P39		9	5
	P3A		10	6
	P3B		11	7
	P3C		12	8
	P3D		13	9
	P3E		14	10
	P3F		15	11
	P46	General-purpose I/O port 4	19	15
	P47		20	16
	P49		22	18
	P4A		23	19
	P4B		24	-
	P4C		25	-
	P4D		26	-
	P4E		27	-
	P50	General-purpose I/O port 5	2	2
	P51		3	3
	P52		4	4
	P60	General-purpose I/O port 6	60	44
	P61		59	43
	P62		58	-
	P80	General-purpose I/O port 8	61	45
	P81		62	46
	P82		63	47
	PE0	General-purpose I/O port E	28	20
	PE2		30	22
	PE3		31	23

Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	48	36
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I^2C (operation mode 4).	47	35
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I^2C (operation mode 4).	46	34
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	35	26
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I^2C (operation mode 4).	36	27
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I^2C (operation mode 4).	37	28
Multi-function Serial 2	SIN2_2	Multi-function serial interface ch.2 input pin	40	-
	SOT2_2 (SDA2_2)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I^2C (operation mode 4).	44	-
	SCK2_2 (SCL2_2)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I^2C (operation mode 4).	45	-

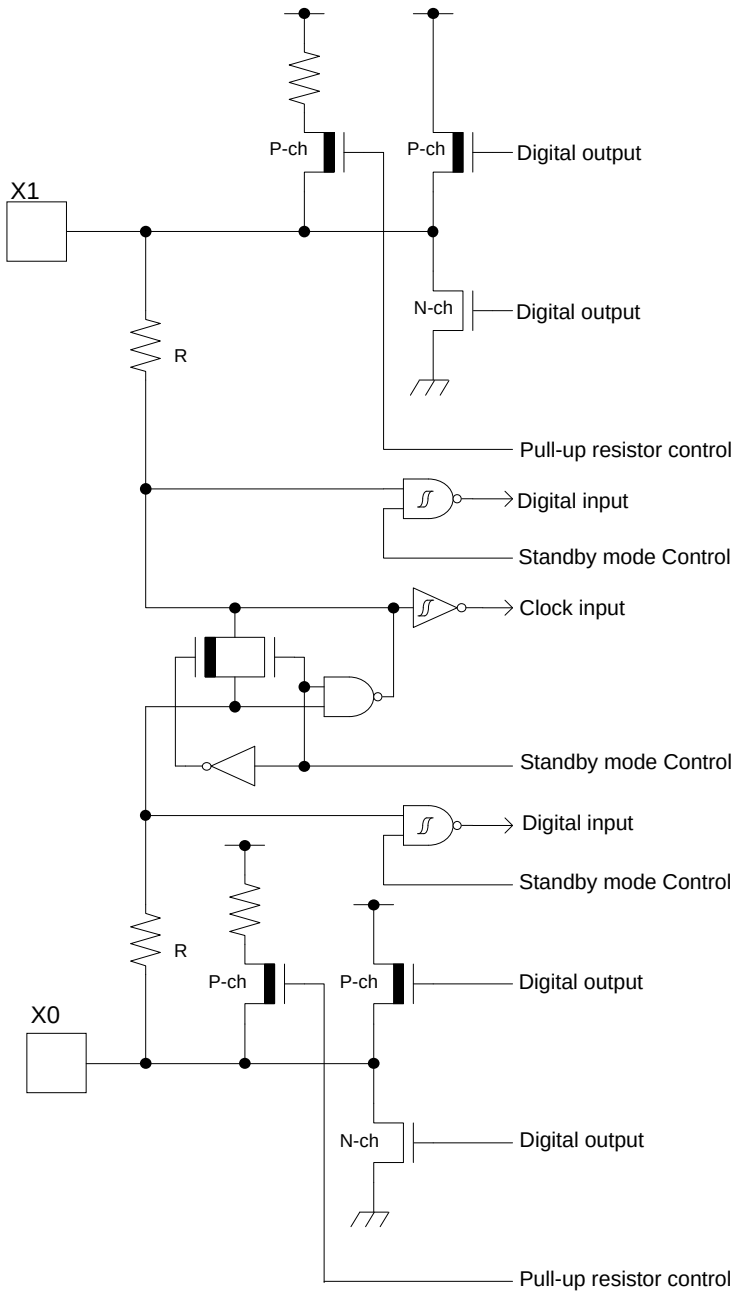
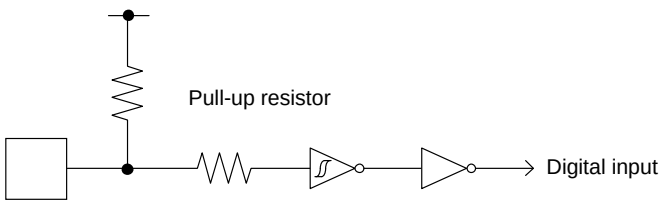
Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	2
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I^2C (operation mode 4).	3	3
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I^2C (operation mode 4).	4	4
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	54	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I^2C (operation mode 4).	55	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I^2C (operation mode 4).	56	-
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	60	44
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I^2C (operation mode 4).	59	43
	SCK5_0 (SCL5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I^2C (operation mode 4).	58	-

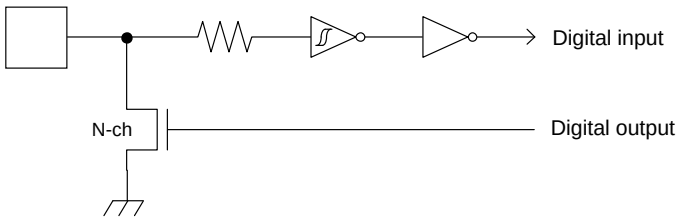
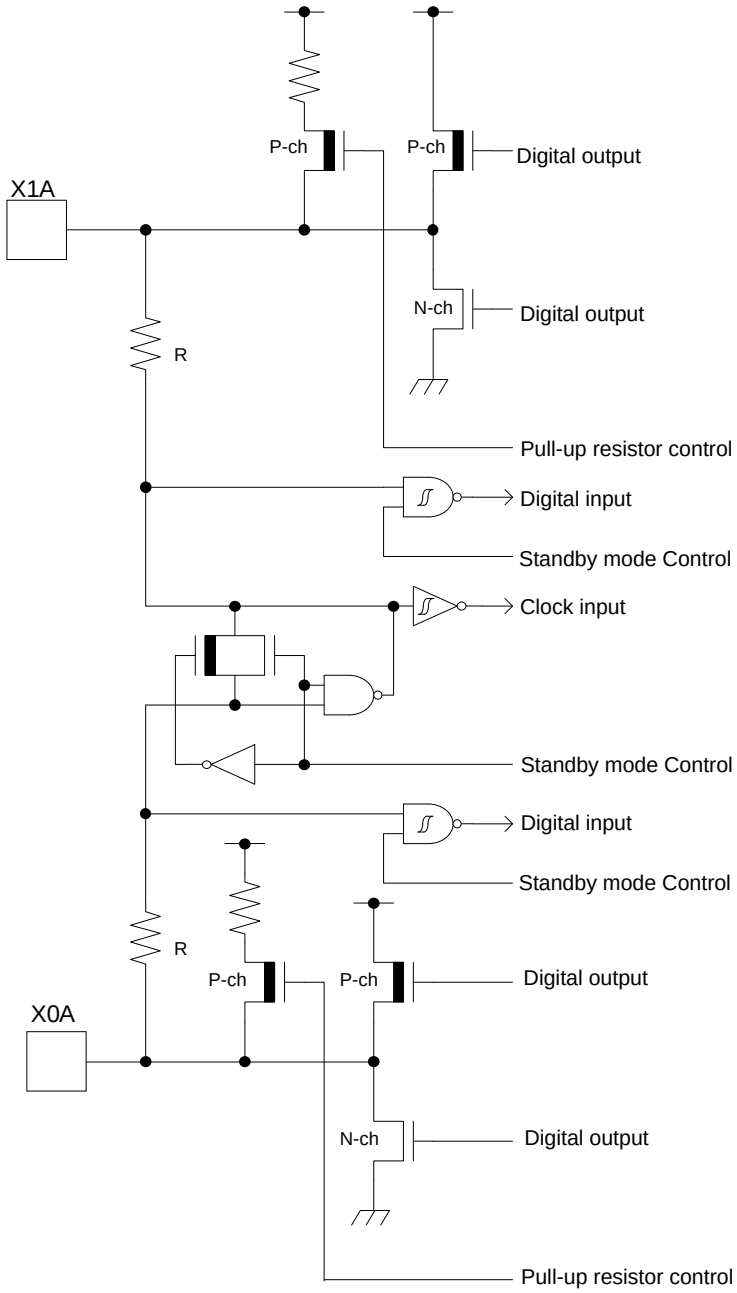
Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Serial 6	SIN6_1	Multi-function serial interface ch.6 input pin	8	-
	SOT6_1 (SDA6_1)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I^2C (operation mode 4).	7	-
	SCK6_1 (SCL6_1)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I^2C (operation mode 4).	6	-
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	27	-
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I^2C (operation mode 4).	26	-
	SCK7_1 (SCL7_1)	Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I^2C (operation mode 4).	25	-

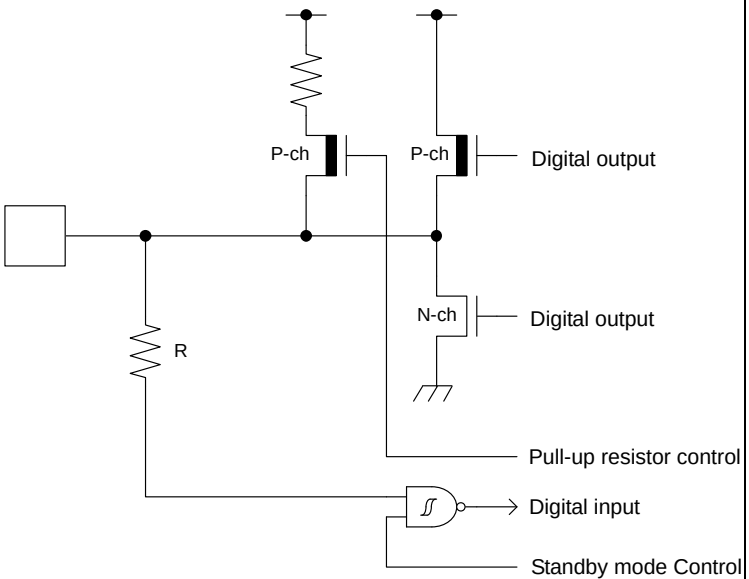
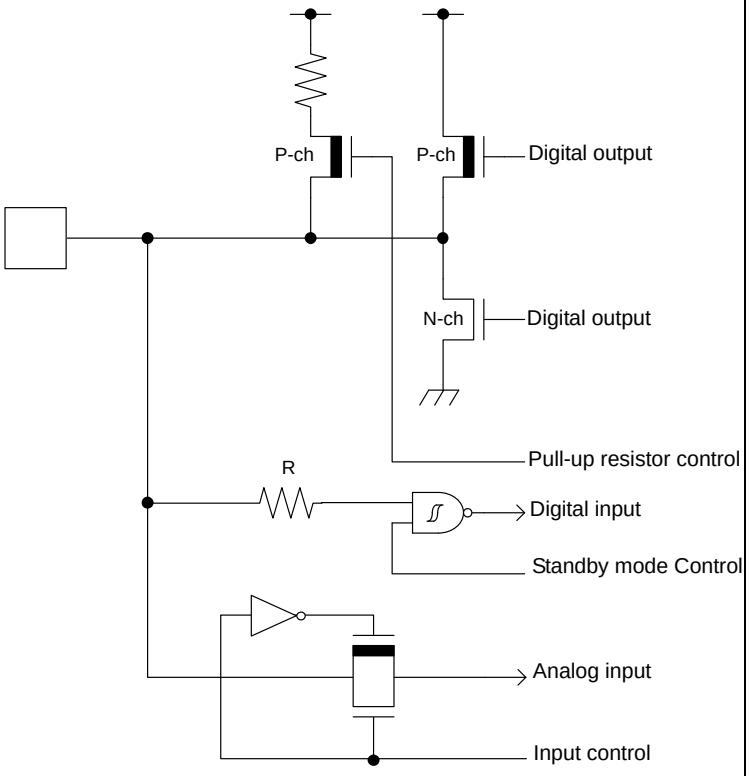
Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0	9	5
	DTTI0X_2		59	43
	FRCK0_2	16-bit free-run timer ch.0 external clock input pin	35	26
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes a channel number.	60	44
	IC00_2		36	27
	IC01_2		37	28
	IC02_0		35	26
	IC02_2		38	29
	IC03_2		39	30
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	10	6
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	11	7
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	12	8
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	13	9
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	14	10
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	15	11
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	57	42
	RTCCO_1		37	28
	RTCCO_2		10	6
	SUBOUT_0	Sub clock output pin	57	42
	SUBOUT_1		37	28
	SUBOUT_2		10	6
Low Power Consumption Mode	WKUP0	Deep stand-by mode return signal input pin 0	57	42
	WKUP1	Deep stand-by mode return signal input pin 1	35	26
	WKUP2	Deep stand-by mode return signal input pin 2	48	36
	WKUP3	Deep stand-by mode return signal input pin 3	60	44

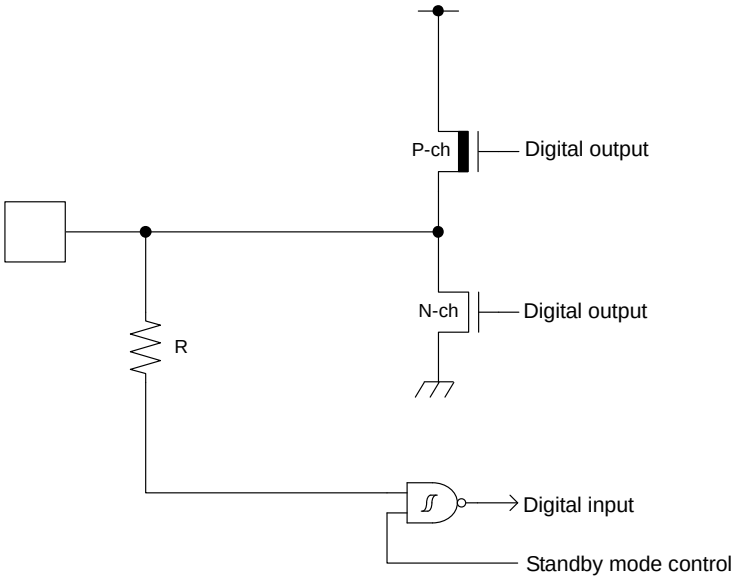
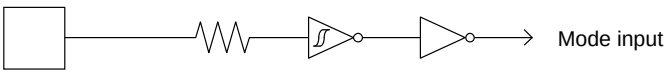
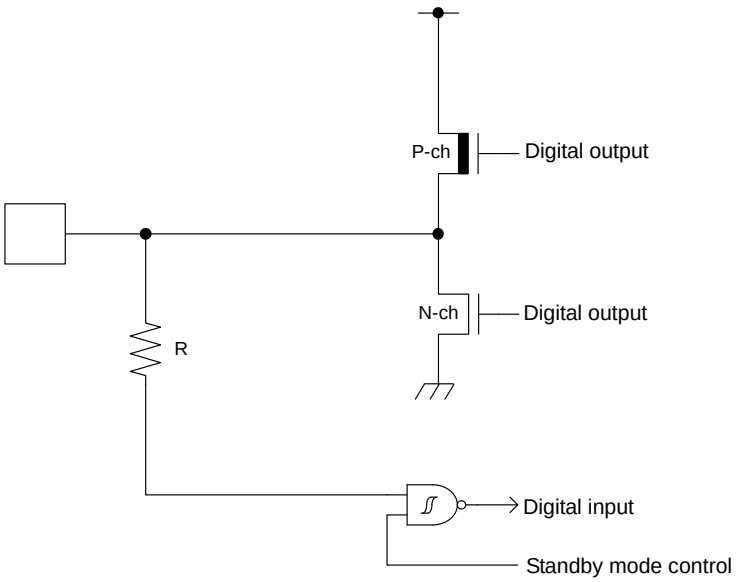
Pin function	Pin name	Function description	Pin No	
			LQFP-64 QFN-64	LQFP-48 QFN-48
RESET	INITX	External Reset Input pin. A reset is valid when INITX = L.	21	17
Mode	MD0	Mode 0 pin. During normal operation, MD0 = L must be input During serial programming to flash memory, MD0 = H must be input.	29	21
	MD1	Mode 1 pin. During normal operation, input is not needed During serial programming to flash memory, MD1 = L must be input.	28	20
POWER	VCC	Power supply pin	1	1
			18	14
			33	-
GND	VSS	GND pin	16	12
			32	24
			64	48
CLOCK	X0	Main clock (oscillation) input pin	30	22
	X0A	Sub clock (oscillation) input pin	19	15
	X1	Main clock (oscillation) I/O pin	31	23
	X1A	Sub clock (oscillation) I/O pin	20	16
	CROUT_1	Internal CR-osc clock output port	57	42
ADC POWER	AVCC	A/D converter analog power pin	41	31
	AVRH	A/D converter analog reference voltage input pin	42	32
ADC GND	AVSS	A/D converter GND pin	43	33
C pin	C	Power stabilization capacity pin	17	13

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function. When the main oscillation is selected. ・ Oscillation feedback resistor : Approximately 1MΩ ・ With Standby control When the GPIO is selected. ・ CMOS level output. ・ CMOS level hysteresis input ・ With pull-up resistor control ・ With standby control ・ Pull-up resistor : Approximately 50kΩ ・ I_{OH} = -4mA, I_{OL} = 4mA
B		・ CMOS level hysteresis input ・ Pull-up resistor : Approximately 50kΩ

Type	Circuit	Remarks
C		・ Open drain output ・ CMOS level hysteresis input
D		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. ・ Oscillation feedback resistor : Approximately 5MΩ ・ With Standby control When the GPIO is selected. ・ CMOS level output. ・ CMOS level hysteresis input ・ With pull-up resistor control ・ With standby control ・ Pull-up resistor : Approximately 50kΩ ・ I_{OH} = -4mA, I_{OL} = 4mA

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With standby control • 5 V tolerant input • I_{OH} = -4mA, I_{OL} = 4mA • Available to control of PZR registers. Only P22, P23, P51, P52
H		CMOS level hysteresis input
I		• CMOS level output • CMOS level hysteresis input • With standby control • I_{OH} = -4mA, I_{OL} = 4mA

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
  Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- Fail-Safe Design

  Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- Precautions Related to Usage of Devices

  FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

  CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- Lead Insertion Type

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- Surface Mount Type

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- Lead-Free Packaging

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.
http://edevice.fujitsu.com/fj/handling-e.pdf

■ HANDLING DEVICES

- Power supply pins

  In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

  Moreover, connect the current supply source with each Power supply pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between each Power supply pins and GND pins near this device.

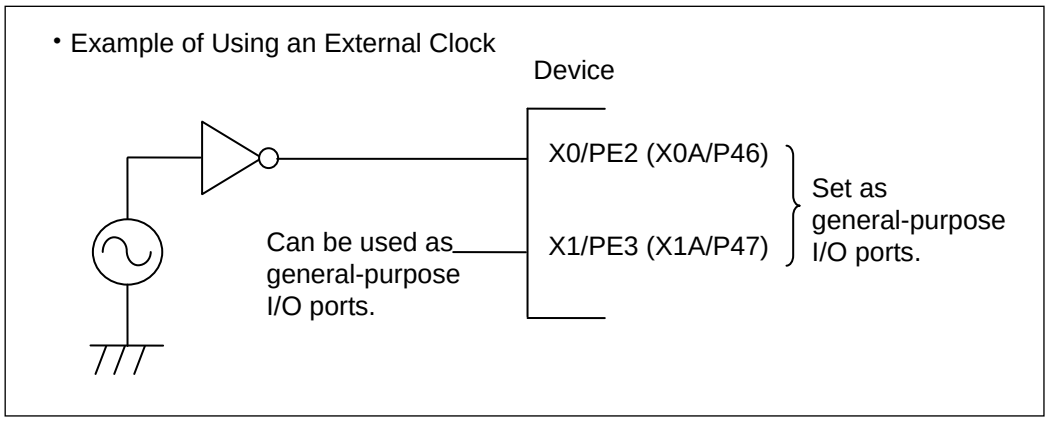
- Crystal oscillator circuit

  Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

  It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

- Using an external clock

  To use the external clock, set general-purpose I/O ports to input the clock to X0/PE2 and X0A/P46 pins.

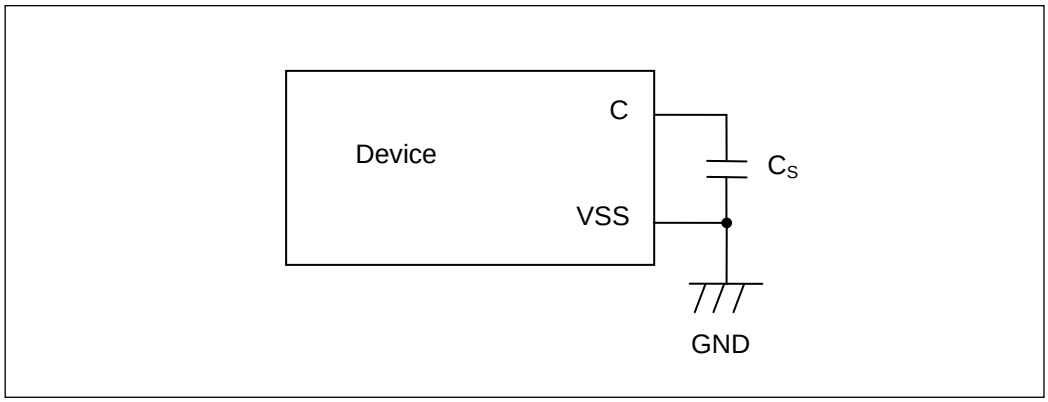


- Handling when using Multi-function serial pin as I^2C pin

  If it is using the Multi-function serial pin as I^2C pins, P-ch transistor of digital output is always disable. However, I^2C pins need to keep the electrical characteristic like other pins and not to connect to external I^2C bus system with power OFF.

- C Pin

  This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
  However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.



- Mode pins (MD0, MD1)

  Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on

  Turn power on/off in the following order or at the same time.
  If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

  Turning on : VCC → AVCC → AVRH

  Turning off : AVRH → AVCC → VCC

- Serial Communication

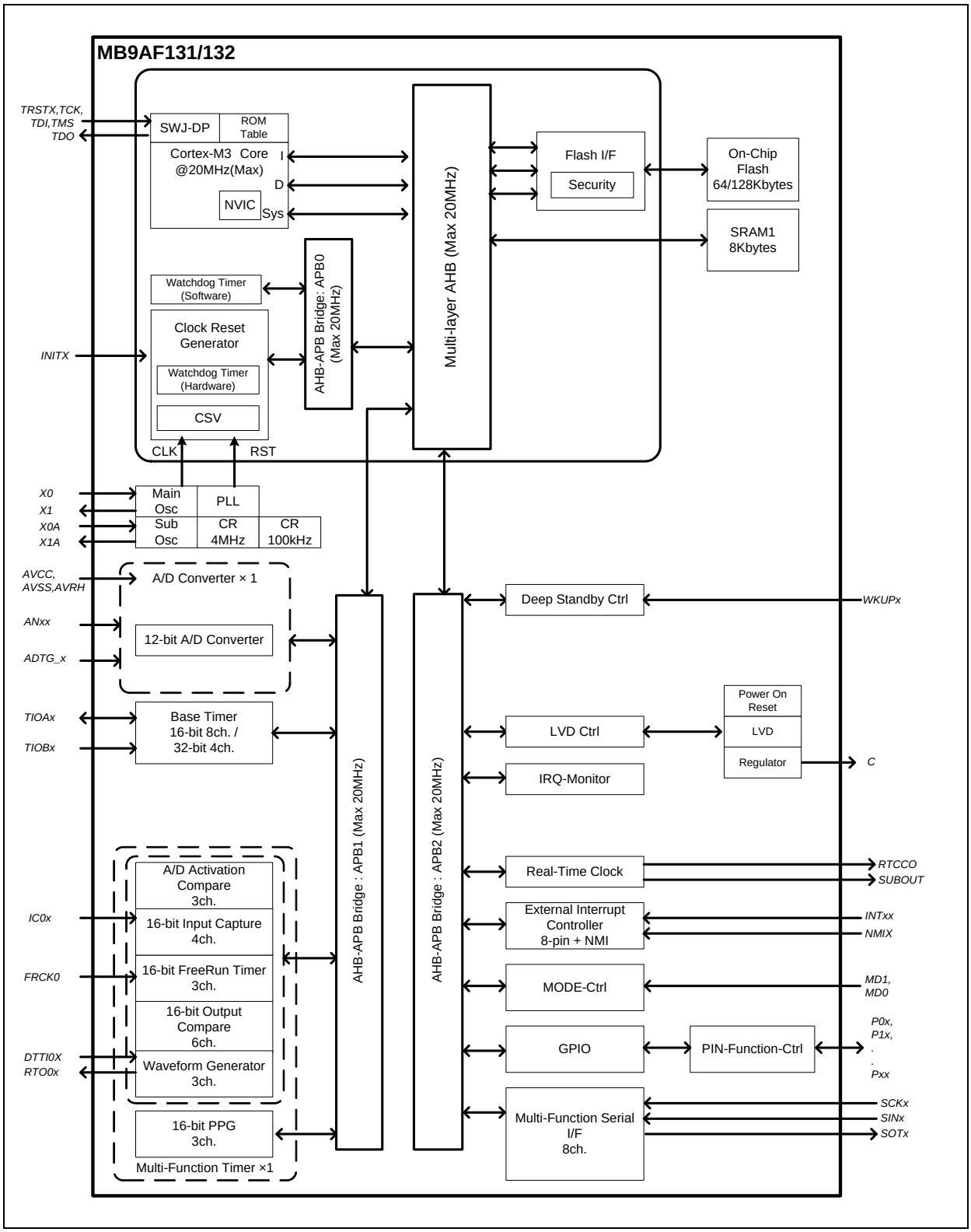
  There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
  Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

- Differences in features among the products with different memory sizes and between Flash products and MASK products

  The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

  If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

■ BLOCK DIAGRAM

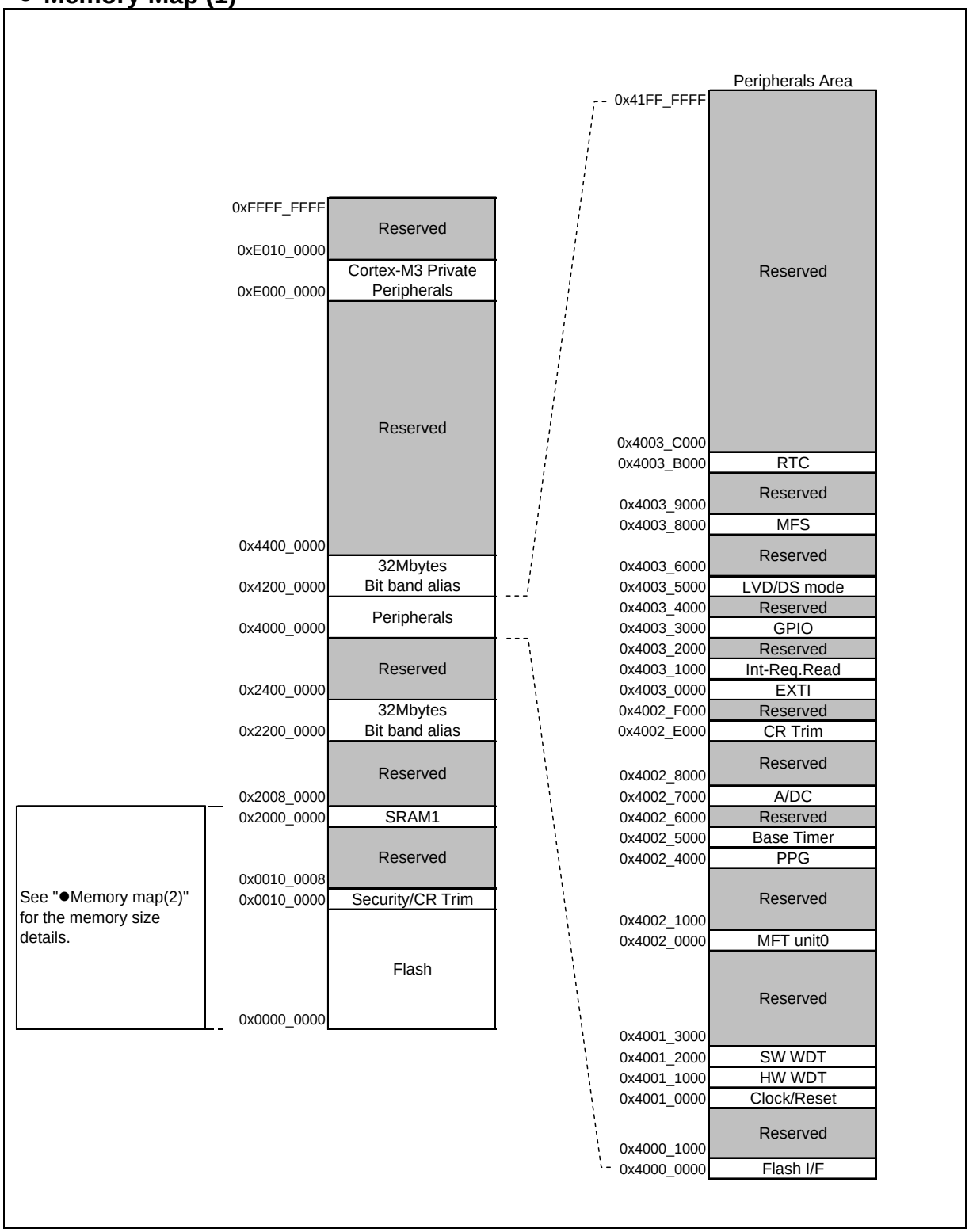


■ MEMORY SIZE

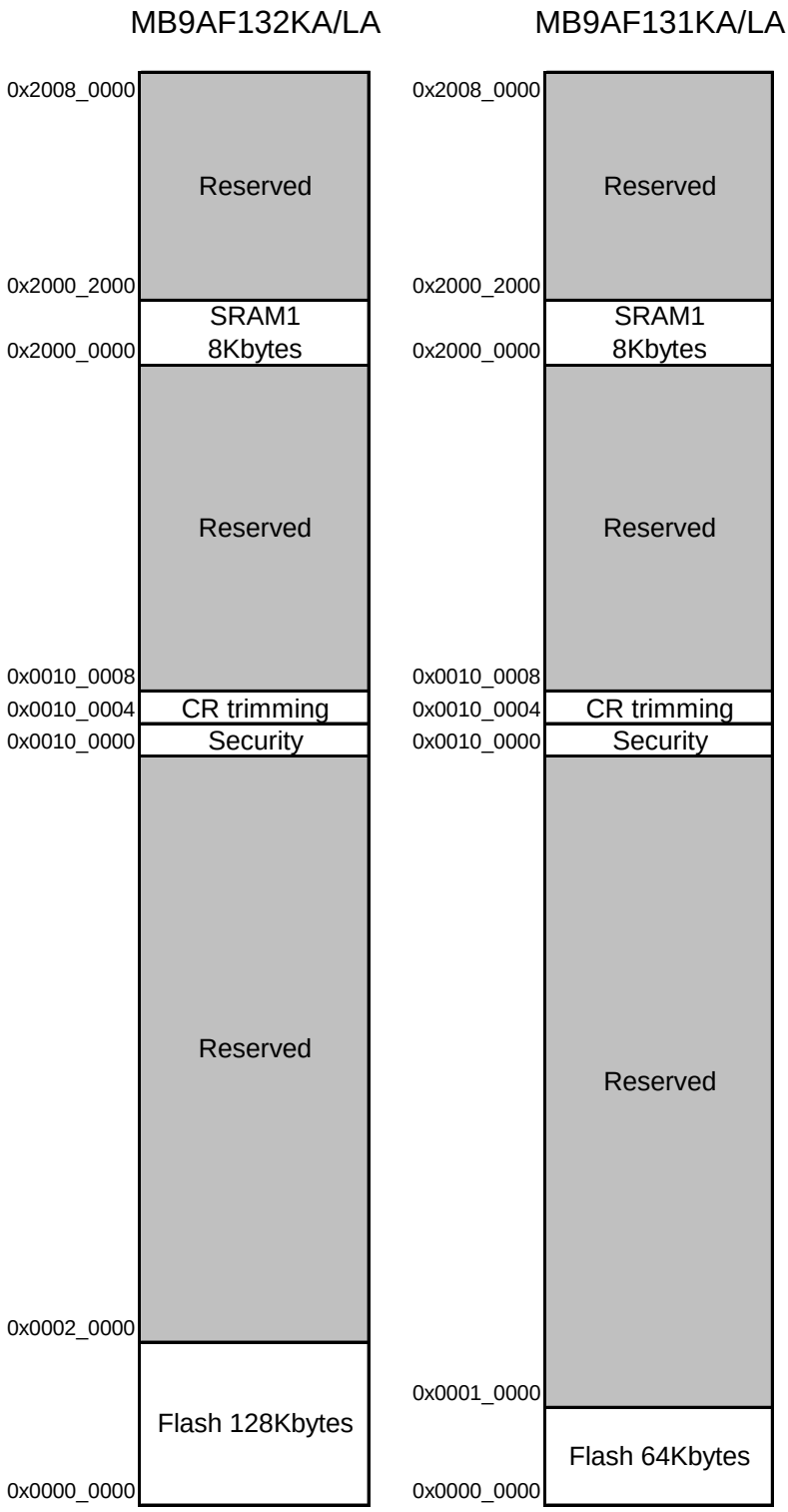
See "• Memory size" in "■PRODUCT LINEUP" to confirm the memory size.

■ MEMORY MAP

● Memory Map (1)



- **Memory Map (2)**


MB9AF132KA/LA
MB9AF131KA/LA
0x2008_0000
Reserved
0x2000_2000
SRAM1
8Kbytes
0x2000_0000
Reserved
0x0010_0008
0x0010_0004
CR trimming
0x0010_0000
Security
Reserved
0x0002_0000
Flash 128Kbytes
0x0000_0000
0x2008_0000
Reserved
0x2000_2000
SRAM1
8Kbytes
0x2000_0000
Reserved
0x0010_0008
0x0010_0004
CR trimming
0x0010_0000
Security
Reserved
0x0001_0000
Flash 64Kbytes
0x0000_0000

● Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Reserved
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Reserved
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Reserved
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Built-in CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_50FF		Low Voltage Detector
0x4003_5100	0x4003_5FFF		Deep stand-by mode Controller
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		Reserved
0x4003_A000	0x4003_AFFF		Reserved
0x4003_B000	0x4003_BFFF		Real-time clock
0x4003_C000	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		Reserved
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		Reserved
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x41FF_FFFF		Reserved

■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- INITX = 0
  This is the period when the INITX pin is the "L" level.
- INITX = 1
  This is the period when the INITX pin is the "H" level.
- SPL = 0
  This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "0".
- SPL = 1
  This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "1".
- Input enabled
  Indicates that the input function can be used.
- Internal input fixed at "0"
  This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z
  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled
  Indicates that the setting is disabled.
- Maintain previous state
  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.
- Analog input is enabled
  Indicates that the analog input is enabled.
- Trace output
  Indicates that the trace function can be used.
- GPIO selected
  In Deep stand-by mode, pins switch to the general-purpose I/O port.

● List of Pin Status

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or STOP mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stop*1, output maintain previous state / Internal input fixed at "0"	Hi-Z / Input enabled / When oscillation stop*1, Hi-Z / Internal input fixed at "0"	Output maintain previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintain previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Output maintain previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state
B	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z output / Internal input fixed at "0"	Maintain previous state / When oscillation stop*1, Hi-Z output / Internal input fixed at "0"
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or STOP mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at "0"		Hi-Z / Internal input fixed at "0"	
F	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected							Maintain previous state		Maintain previous state
G	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled			Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected							Maintain previous state		Maintain previous state
H	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected							Maintain previous state		Maintain previous state

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or STOP mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
I	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at "0"			
	GPIO selected									Maintain previous state
J	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	GPIO selected							Maintain previous state		Maintain previous state
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected							Maintain previous state		Maintain previous state

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or STOP mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled	Hi-Z / Internal input fixed at "0" / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected						Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at "0"	
	Resource other than above selected						Hi-Z / Internal input fixed at "0"			
	GPIO selected							Maintain previous state		Maintain previous state
M	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stop*2, output maintain previous state / Internal input fixed at "0"	Hi-Z / Input enabled / When oscillation stop*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stop*2, output maintain previous state / Internal input fixed at "0"	Hi-Z / Input enabled / When oscillation stop*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When Return from Deep Stand-by STOP mode, GPIO selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintain previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Output maintain previous state / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode, RTC mode, or STOP mode state		Deep stand-by RTC mode or Deep stand-by STOP mode state		Return from Deep stand-by mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
N	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at "0"
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state	Hi-Z / Internal input fixed at "0"	Maintain previous state
O	GPIO	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at "0"	GPIO/ Internal input fixed at "0"	Hi-Z / Internal input fixed at "0"	Maintain previous state
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	Maintain previous state	Hi-Z / Input enabled	Maintain previous state

*1 : Oscillation is stopped at Sub run mode, Low-speed CR run mode, Sub sleep mode, Low-speed CR sleep mode, Sub timer mode, Low-speed CR timer mode, RTC mode, STOP mode, Deep standby RTC mode, and Deep standby STOP mode.

*2 : Oscillation is stopped at STOP mode and Deep stand-by STOP mode.

■ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	Vcc	Vss - 0.5	Vss + 6.5	V	
Analog power supply voltage*1,*3	AVcc	Vss - 0.5	Vss + 6.5	V	
Analog reference voltage*1,*3	AVRH	Vss - 0.5	Vss + 6.5	V	
Input voltage*1	V_I	Vss - 0.5	Vcc + 0.5 (≤ 6.5V)	V	
		Vss - 0.5	Vss + 6.5	V	5V tolerant
Analog pin input voltage*1	V_{IA}	Vss - 0.5	AVcc + 0.5 (≤ 6.5V)	V	
Output voltage*1	V_O	Vss - 0.5	Vcc + 0.5 (≤ 6.5V)	V	
"L" level maximum output current*4	I_{OL}	-	10	mA	
"L" level average output current*5	I_{OLAV}	-	4	mA	
"L" level total maximum output current	$\sum I_{OL}$	-	60	mA	
"L" level total average output current*6	$\sum I_{OLAV}$	-	30	mA	
"H" level maximum output current*4	I_{OH}	-	-10	mA	
"H" level average output current*5	I_{OHAV}	-	- 4	mA	
"H" level total maximum output current	$\sum I_{OH}$	-	-60	mA	
"H" level total average output current*6	$\sum I_{OHAV}$	-	-30	mA	
Power consumption	P_D	-	400	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1 : These parameters are based on the condition that Vss = AVss = 0.0V.
*2 : Vcc must not drop below Vss - 0.5V.
*3 : Be careful not to exceed Vcc + 0.5 V, for example, when the power is turned on.
*4 : The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
*5 : The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.
*6 : The total average output current is defined as the average current value flowing through all of corresponding pins for a 100ms.

<WARNING>

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(Vss = AVss = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		Vcc	-	1.8	5.5	V	
Analog power supply voltage		AVcc	-	1.8	5.5	V	AVcc = Vcc
Analog reference voltage		AVRH	-	AVss	AVcc	V	
Smoothing capacitor		C_S	-	1	10	µF	For Regulator *
Operating Temperature	FPT-48P-M49, LCC-48P-M73, FPT-64P-M24, FPT-64P-M38, FPT-64P-M39, LCC-64P-M24	Ta	-	- 40	+ 85	°C	

* : See "•C Pin" in "■HANDLING DEVICES" for the connection of the smoothing capacitor.

<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(1) Current Rating

(Vcc = AVcc = 1.8V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ*4	Max		
Power supply current	Icc	VCC	Normal operation (PLL)	-	20	25	mA	CPU : 20MHz, Peripheral : 20MHz, Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
				-	10	15	mA	CPU : 20MHz, Peripheral : clock stoped, NOP operation *1
			Normal operation (built-in high-speed CR)	-	4.5	5	mA	CPU / Peripheral : 4MHz*2 Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
			Normal operation (sub oscillation)	-	0.25	0.35	mA	CPU / Peripheral : 32kHz Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
			Normal operation (built-in low-speed CR)	-	0.3	0.45	mA	CPU / Peripheral : 100kHz Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
	Iccs		SLEEP operation (PLL)	-	9	13	mA	Peripheral : 20MHz *1
			SLEEP operation (built-in high-speed CR)	-	2	2.5	mA	Peripheral : 4MHz*2 *1
			SLEEP operation (sub oscillation)	-	0.1	0.2	mA	Peripheral : 32kHz *1
			SLEEP operation (built-in low-speed CR)	-	0.2	0.35	mA	Peripheral : 100kHz *1

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ*4	Max		
Power supply current	I_{CCR}	VCC	RTC mode	-	1.8	7.5	µA	Ta = + 25°C, When LVD is off *1, *3, *4
				-	7	62	µA	Ta = + 85°C, When LVD is off *1, *3, *4
	I_{CCRD}		Deep stand-by RTC mode	-	1.6	3	µA	Ta = + 25°C, When LVD is off *1, *3, *4
				-	3.6	14.5	µA	Ta = + 85°C, When LVD is off *1, *3, *4
	I_{CCH}		STOP mode	-	0.7	7	µA	Ta = + 25°C, When LVD is off *1, *4
				-	6	60	µA	Ta = + 85°C, When LVD is off *1, *4
	I_{CCHD}		Deep stand-by STOP mode	-	0.5	2.5	µA	Ta = + 25°C, When LVD is off *1, *4
				-	2.5	12.5	µA	Ta = + 85°C, When LVD is off *1, *4
Low voltage detection circuit (LVD) power supply current	I_{CCLVD}		For occurrence of reset or for occurrence of interrupt in normal mode operation	-	10	42	µA	When not detected
			For occurrence of reset and for occurrence of interrupt in normal mode operation	-	14	56	µA	
			For occurrence of interrupt in low power mode operation	-	0.3	2	µA	When not detected

*1: When all ports are fixed.
*2: When setting it to 4MHz by trimming.
*3: When using sub crystal oscillator.
*4: When Vcc=3.3V

(2) Pin Characteristics

(Vcc = AVcc = 1.8V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	MD0, MD1, PE0, PE2, PE3, P46, P47, INITX	-	Vcc × 0.8	-	Vcc + 0.3	V	
		P21, P22, P23, P50, P51, P52, P80, P81, P82	-	Vcc× 0.7	-	Vss + 5.5	V	5V tolerant
		CMOS hysteresis input pins other than the above	-	Vcc × 0.7	-	Vcc + 0.3	V	
"L" level input voltage (hysteresis input)	V_{ILS}	MD0, MD1, PE0, PE2, PE3, P46, P47, INITX	-	Vss - 0.3	-	Vcc× 0.2	V	
		CMOS hysteresis input pins other than the above	-	Vss - 0.3	-	Vcc× 0.3	V	
"H" level output voltage	V_{OH}	Pxx	Vcc ≥ 4.5 V I_{OH} = - 4mA	Vcc - 0.5	-	Vcc	V	
			Vcc < 4.5 V I_{OH} = - 1mA	Vcc - 0.5	-	Vcc		
"L" level output voltage	V_{OL}	Pxx	Vcc ≥ 4.5 V I_{OL} = 4mA	Vss	-	0.4	V	
			Vcc < 4.5 V I_{OL} = 2mA					
Input leak current	I_{IL}	-	-	- 5	-	+5	µA	
Pull-up resistance value	R_{PU}	Pull-up pin	Vcc ≥ 4.5 V	25	50	100	kΩ	
			Vcc < 4.5 V	40	100	400		
Input capacitance	C_{IN}	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

4. AC Characteristics

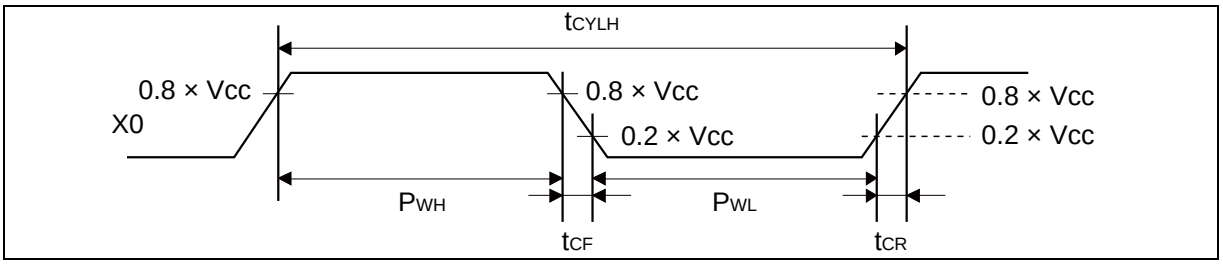
(1) Main Clock Input Characteristics

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F_{CH}	X0, X1	Vcc ≥ 2.0V	4	20	MHz	When crystal oscillator is connected
			Vcc < 2.0V	4	4	MHz	
			Vcc ≥ 4.5V	4	20	MHz	When using external clock
			Vcc < 4.5V	4	16	MHz	
Input clock cycle	t_{CYLH}		Vcc ≥ 4.5V	50	250	ns	When using external clock
			Vcc < 4.5V	62.5	250	ns	
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	F_{CM}	-	-	-	20	MHz	Master clock
	F_{CC}	-	-	-	20	MHz	Base clock (HCLK/FCLK)
	F_{CP0}	-	-	-	20	MHz	APB0 bus clock*2
	F_{CP1}	-	-	-	20	MHz	APB1 bus clock*2
	F_{CP2}	-	-	-	20	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	50	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	50	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	50	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	50	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

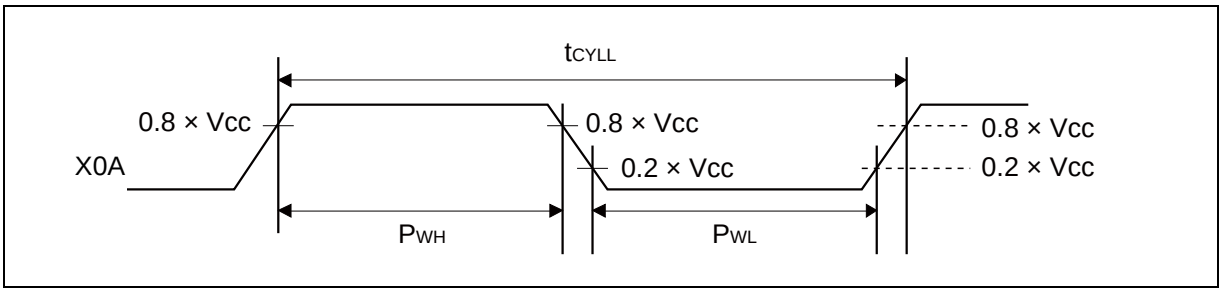
*2: For about each APB bus which each peripheral is connected to, see "■BLOCK DIAGRAM" in this data sheet.



(2) Sub Clock Input Characteristics

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F_{CL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



(3) Built-in CR Oscillation Characteristics

- Built-in high-speed CR

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions		Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CRH}	Vcc ≥ 2.2 V	Ta = + 25°C	3.92	4	4.08	MHz	When trimming*
			Ta = - 40°C to + 85°C	3.8	4	4.2		
			Ta = - 40°C to + 85°C	2.3	-	7.03		When not trimming
		Vcc < 2.2 V	Ta = + 25°C	3.4	4	4.6	MHz	When trimming*
			Ta = - 40°C to + 85°C	3.16	4	4.84		
			Ta = - 40°C to + 85°C	2.3	-	7.03		When not trimming

*: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

- Built-in low-speed CR

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F_{CRL}	-	50	100	150	kHz	

(4-1) Operating Conditions of Main PLL (In the case of using main clock for input of PLL)

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	F_{PLLI}	4	-	20	MHz	
PLL multiplication rate	-	1	-	5	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	10	-	20	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	20	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock(CLKPLL), see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

(4-2) Operating Conditions of Main PLL (In the case of using built-in high-speed CR clock)

(Vcc = 2.2V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	F_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	3	-	4	multiplier	
PLL macro oscillation clock frequency	F_{PLLO}	11.4	-	16.8	MHz	
Main PLL clock frequency*2	F_{CLKPLL}	-	-	16.8	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock(CLKPLL), see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

Note: Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency has been trimmed.

(5) Reset Input Characteristics

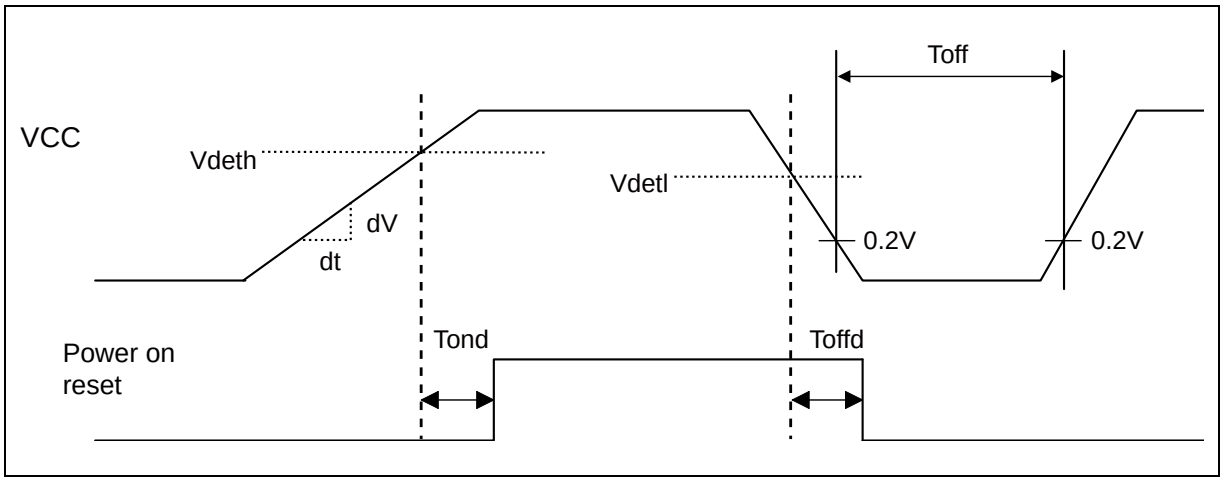
(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	
				1.5	-	ms	When RTC mode or STOP mode
				1.5	-	ms	When deep stand-by mode

(6) Power-on Reset Timing

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	VCC	0.1	-	-	V/ms	
Power supply shut down time	Toff		1	-	-	ms	
Reset release voltage	Vdeth		1.44	1.60	1.76	V	When voltage rises
Reset generation voltage	Vdetl		1.39	1.55	1.71	V	When voltage drops
Reset release delay time	Tond		-	-	10	ms	dV/dt ≥ 0.1mV/µs
Reset detection delay time	Toffd		-	-	0.4	ms	dV/dt ≥ -0.04mV/µs

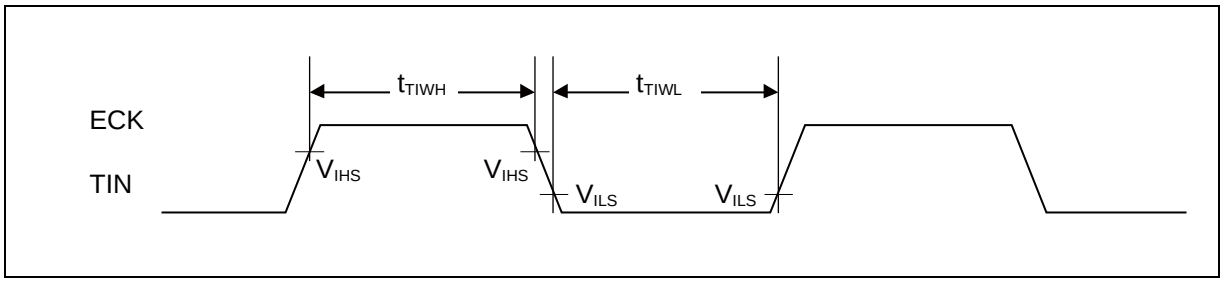


(7) Base Timer Input Timing

- Timer input timing

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

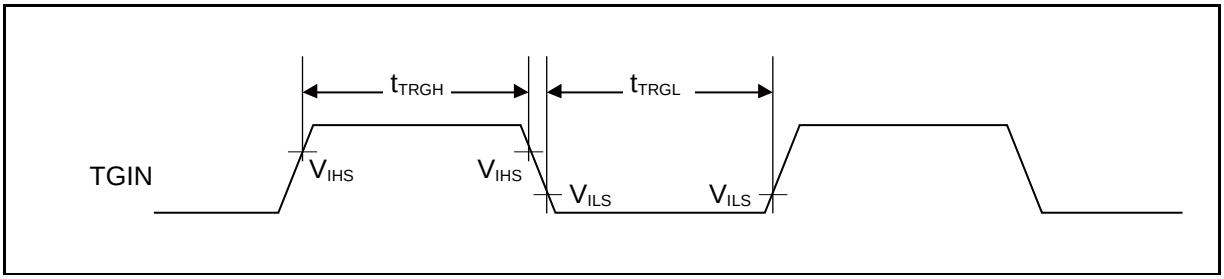
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK,TIN)	-	$2t_{CYCP}$	-	ns	



- Trigger input timing

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note: t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.

(8) UART Timing

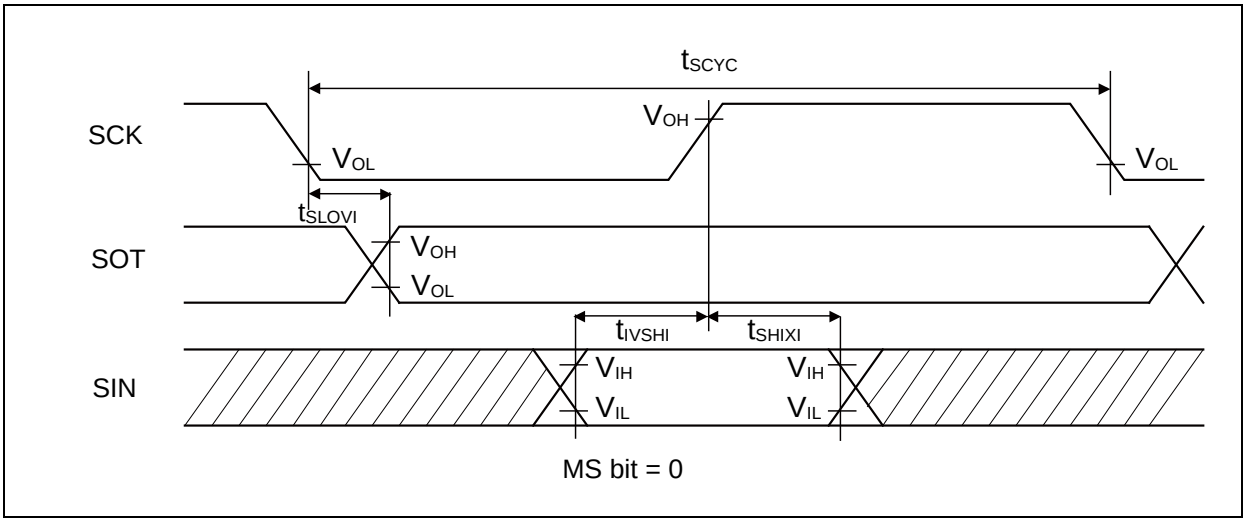
- Synchronous serial (SPI = 0, SCINV = 0)

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

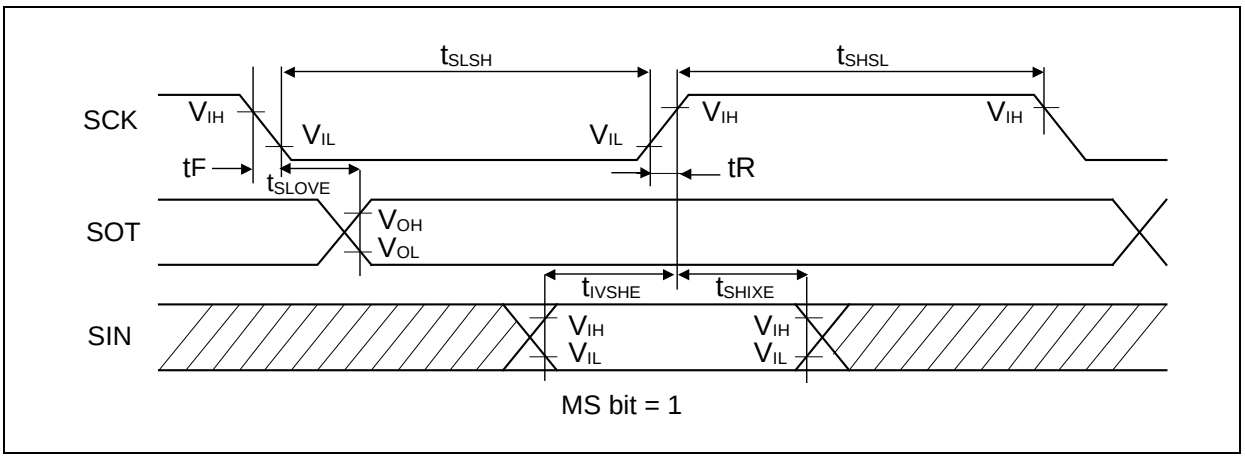
Parameter	Symbol	Pin name	Conditions	Vcc < 2.7V		2.7V ≤ Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30*1 40*2	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	-	5	ns

*1 When PZR=0.
*2 When PZR=1.

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 50pF.



MS bit = 0



MS bit = 1

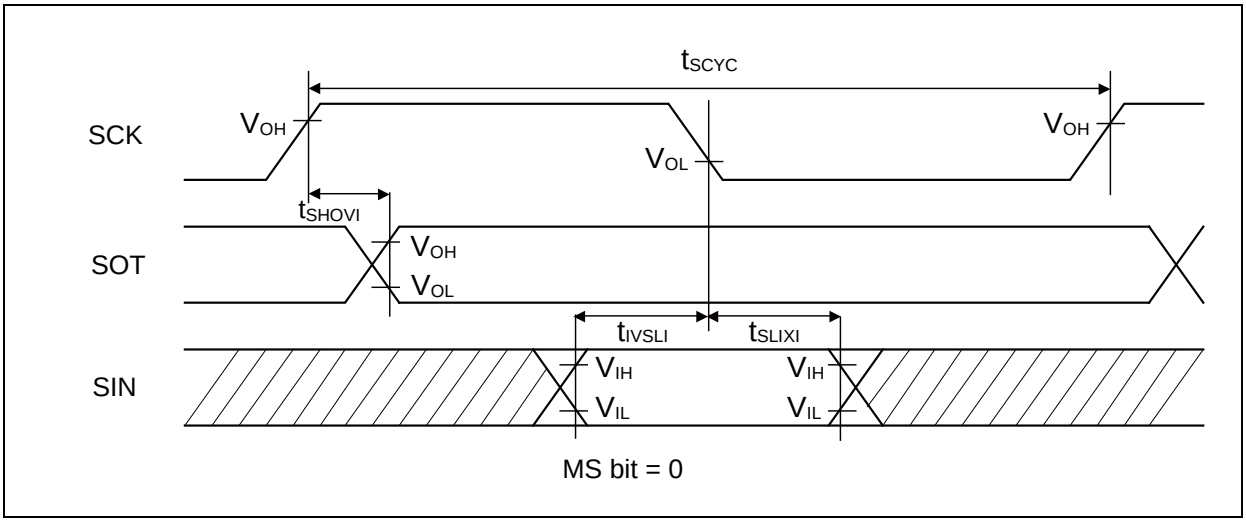
- Synchronous serial (SPI = 0, SCINV = 1)

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

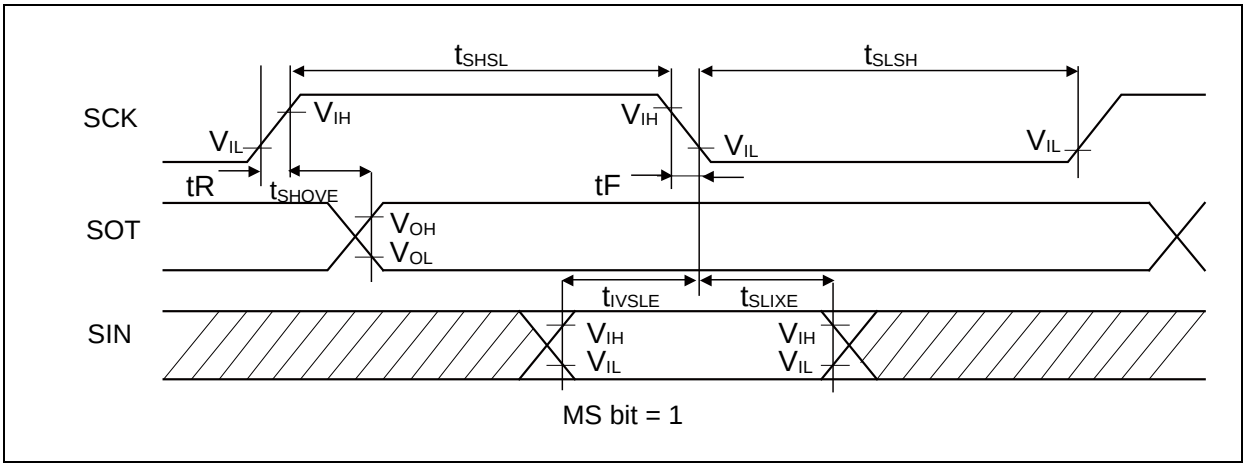
Parameter	Symbol	Pin name	Conditions	Vcc < 2.7V		2.7V ≤ Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	75	-	50	-	30*1 40*2	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	-	5	ns

*1 When PZR=0.
*2 When PZR=1.

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 50pF.



MS bit = 0



MS bit = 1

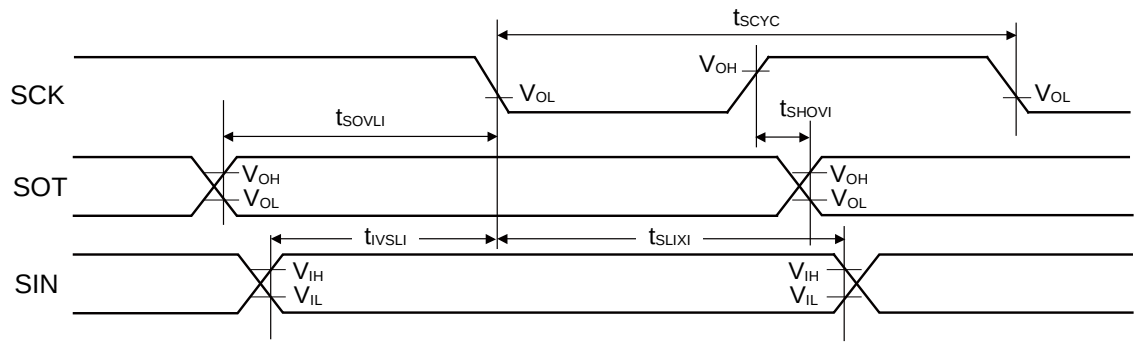
- Synchronous serial (SPI = 1, SCINV = 0)

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

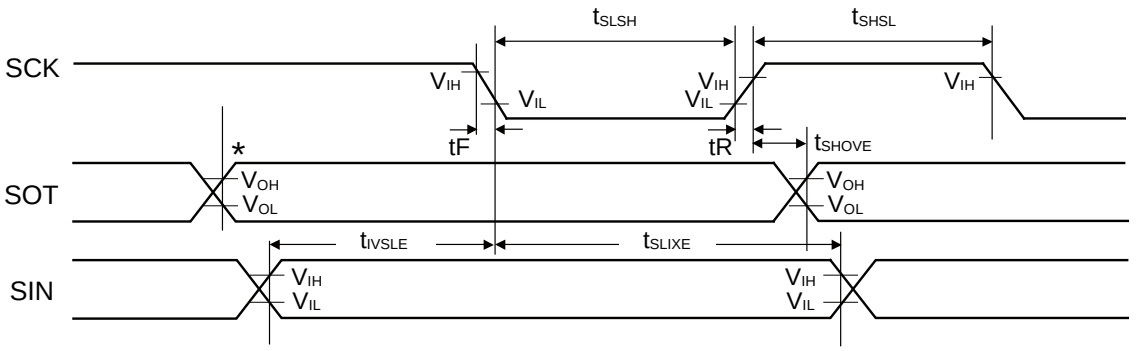
Parameter	Symbol	Pin name	Conditions	Vcc < 2.7V		2.7V ≤ Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↓ → SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		-	75	-	50	-	30*1 40*2	ns
SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↓ → SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	-	5	ns

*1 When PZR=0.
*2 When PZR=1.

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 50pF.



MS bit = 0



MS bit = 1

* : Changes when writing to TDR register

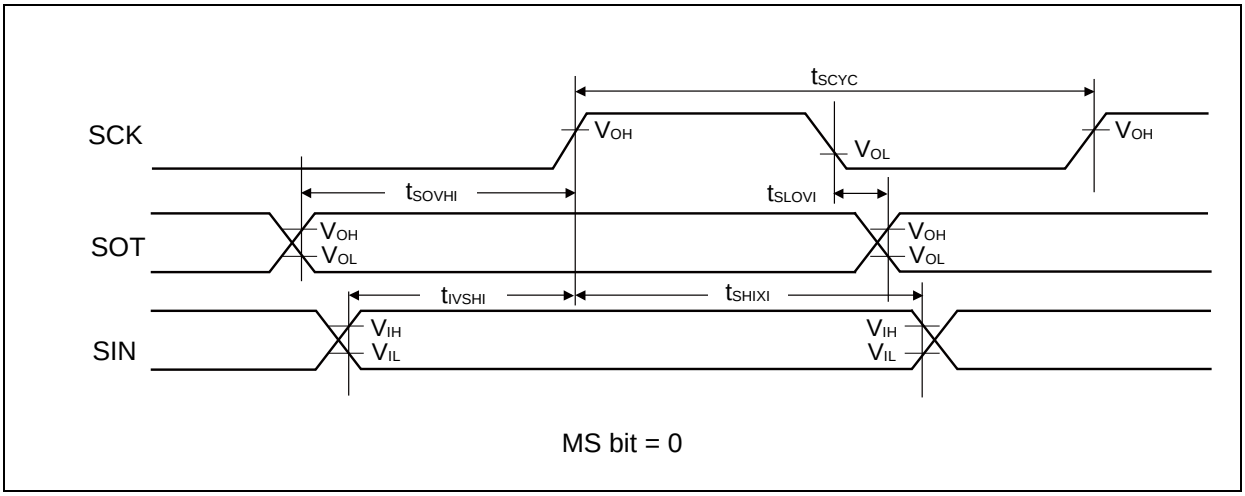
- Synchronous serial (SPI = 1, SCINV = 1)

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

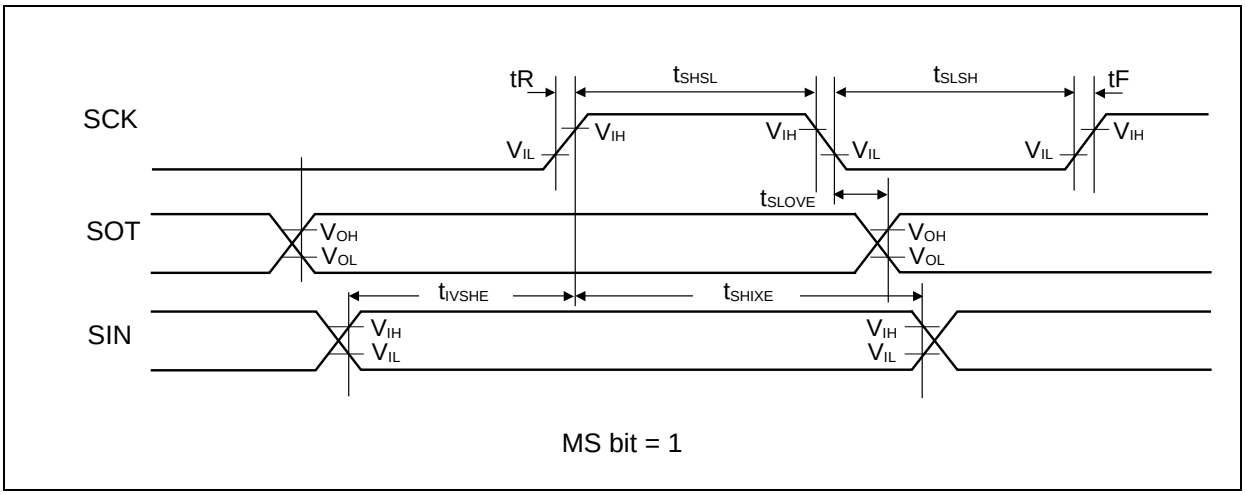
Parameter	Symbol	Pin name	Conditions	Vcc < 2.7V		2.7V ≤ Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		-	75	-	50	-	30*1 40*2	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	-	5	ns

*1 When PZR=0.
*2 When PZR=1.

Notes:
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time.
  About the APB bus number which UART is connected to, see "■BLOCK DIAGRAM" in this data sheet.
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 50pF.



MS bit = 0

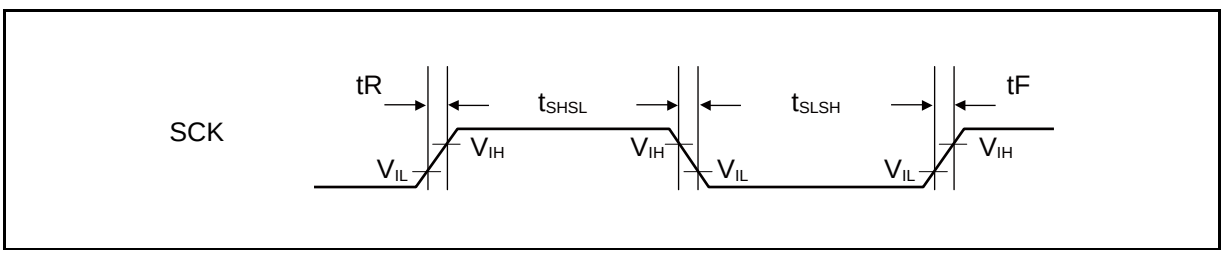


MS bit = 1

- External clock (EXT = 1) : asynchronous only

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 50pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK fall time	tF		-	5	ns	
SCK rise time	tR		-	5	ns	



(9) External Input Timing

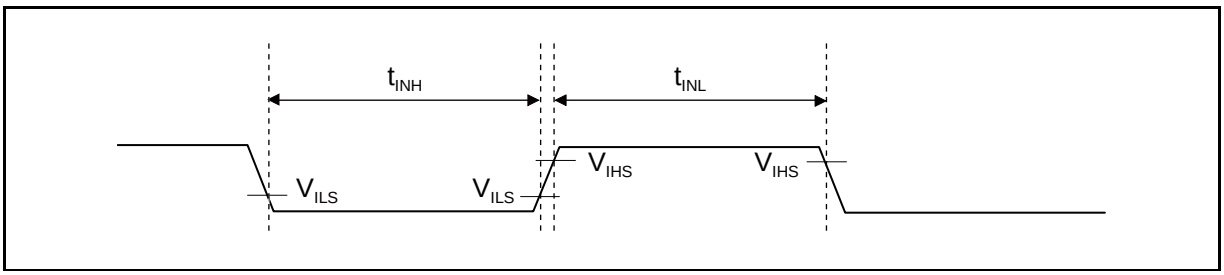
(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT15, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep stand-by wake up

*1 : t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode, etc.
About the APB bus number which A/D converter, Multi-function Timer, External interrupt, Deep stand-by mode Controller is connected to, see "■BLOCK DIAGRAM" in this data sheet.

*2 : When in stop mode, in timer mode.

*3 : When in deep stand-by STOP mode, in deep stand-by RTC mode.



(10) I^2C Timing

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

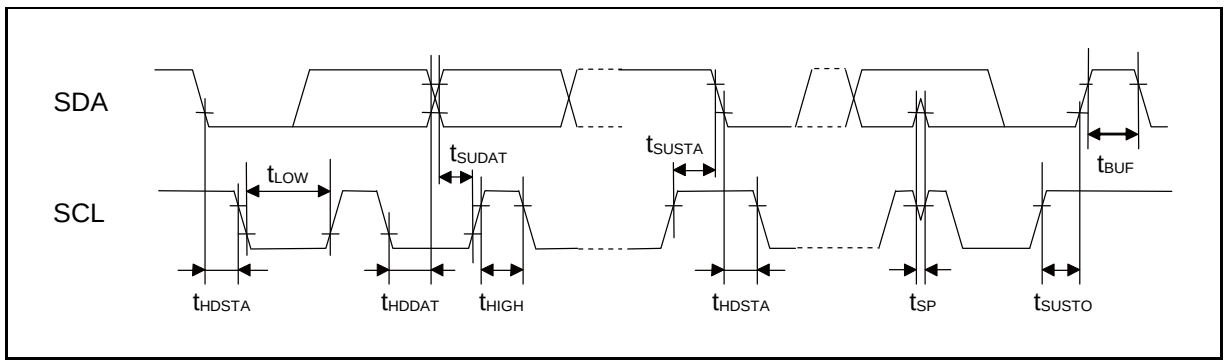
Parameter	Symbol	Conditions	Typical mode		High-speed mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 50pF, R = (Vp/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-	2 t_{CYCP}*4	-	2 t_{CYCP}*4	-	ns	

*1 : R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4 : t_{CYCP} is the APB bus clock cycle time. About the APB bus number which I^2C is connected to, see "■BLOCK DIAGRAM" in this data sheet. To use I^2C, set the peripheral bus clock at 8 MHz or more.

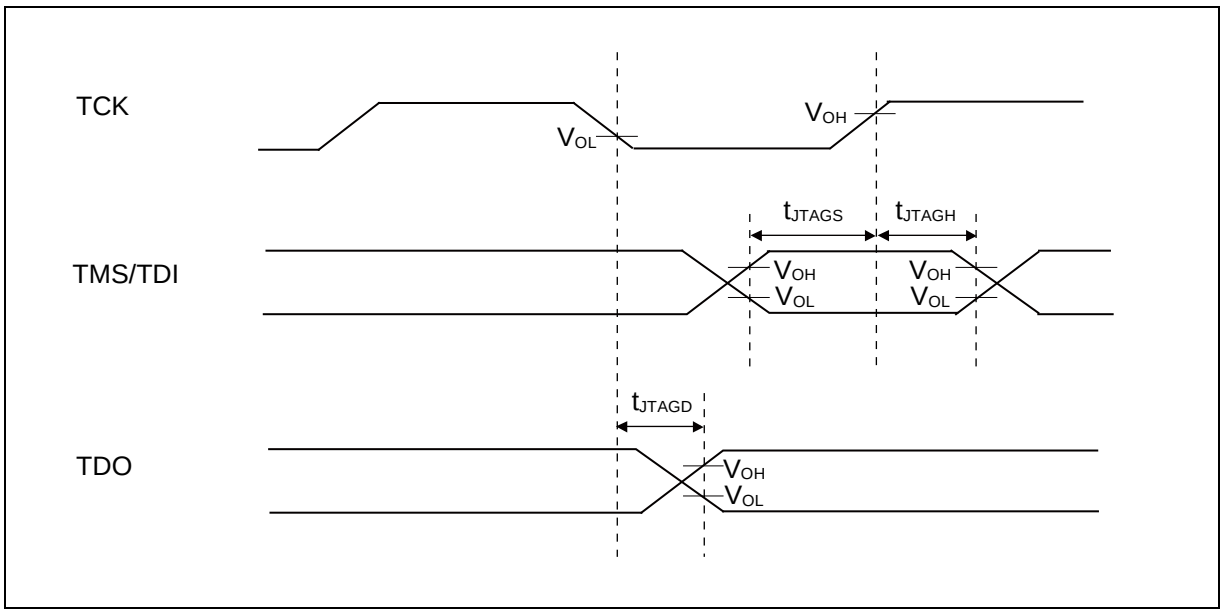


(11) JTAG Timing

(Vcc = 1.8V to 5.5V, Vss = 0V, Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t_{JTAGS}	TCK, TMS,TDI	Vcc ≥ 4.5V	15	-	ns	
			Vcc < 4.5V				
TMS,TDI hold time	t_{JTAGH}	TCK, TMS,TDI	Vcc ≥ 4.5V	15	-	ns	
			Vcc < 4.5V				
TDO delay time	t_{JTAGD}	TCK, TDO	Vcc ≥ 4.5V	-	30	ns	
			2.7V ≤ Vcc < 4.5V	-	45		
			Vcc < 2.7V	-	60		

Note: When the external load capacitance C_L = 50pF.



5. 12-bit A/D Converter

- Electrical characteristics for the A/D converter

(Vcc = AVcc = 1.8V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 85°C)

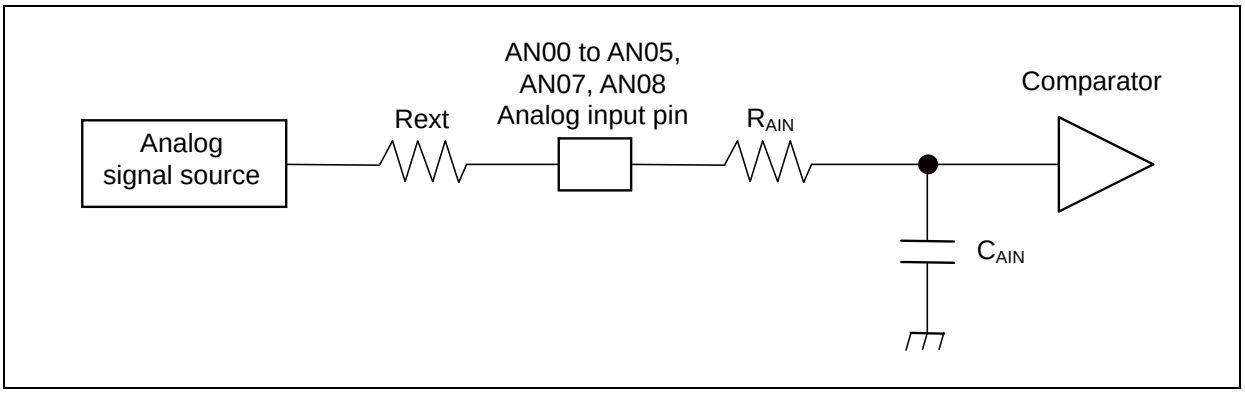
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Non linearity error	-	-	- 3.0	-	+ 3.0	LSB	$AV_{CC} \geq 2.7V$
			- 5.0	-	+ 5.0	LSB	$AV_{CC} < 2.7V$
Differential linearity error	-	-	- 1.9	-	+ 1.9	LSB	$AV_{CC} \geq 2.7V$
			- 2.9	-	+ 2.9	LSB	$AV_{CC} < 2.7V$
Zero transition voltage	V_{0T}	AN00 to AN05, AN07, AN08	- 20	-	+ 20	mV	
Full-scale transition voltage	V_{FST}	AN00 to AN05, AN07, AN08	AVRH-20	-	AVRH+20	mV	
Conversion time	-	-	1.0*1	-	-	µs	AVcc ≥ 2.7V
Sampling time	Ts	-	*2	-	10	µs	
Compare clock cycle*3	Tcck	-	50	-	1000	ns	AVcc ≥ 2.7V
			200				AVcc < 2.7V
Period of operation enable state transitions	Tstt	-	1	-	-	µs	
Power supply current (analog + digital)	-	AVCC	-	1.4	2.5	mA	A/D operation
			-	0.1	0.35	µA	A/D stop
Reference power supply current (between AVRH and AVSS)	-	AVRH	-	0.8	1.5	mA	A/D operation AVRH=5.5V
			-	0.1	0.3	µA	A/D stop
Analog input capacity	C_{AIN}	-	-	-	15	pF	
Analog input resistance	R_{AIN}	-	-	-	0.9	kΩ	AVcc ≥ 4.5V
					1.6		2.7V ≤ AVcc < 4.5V
					4.0		AVcc < 2.7V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input current	-	AN00 to AN05, AN07, AN08	-	-	0.3	µA	
Analog input voltage	-	AN00 to AN05, AN07, AN08	AVSS	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AVCC	V	$AV_{CC} \geq 2.7V$
			AVCC				AVcc < 2.7V

*1: Conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is, the value of sampling time: 300ns, the value of compare time: 700ns. (AVcc ≥ 2.7V)
Ensure that it satisfies the value of sampling time (Ts) and compare clock cycle (Tcck).
For setting*4 of sampling time and compare clock cycle, see "Chapter: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".

*2: A necessary sampling time changes by external impedance.
Ensure to set the sampling time to satisfy (Equation 1).

*3: Compare time (Tc) is the value of (Equation 2).

*4: The register setting of the A/D Converter is reflected by the timing of the APB bus clock.
Sampling clock and compare clock are set with the base clock (HCLK).
About the APB bus number which A/D Converter is connected to, see "■BLOCK DIAGRAM" in this data sheet.



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

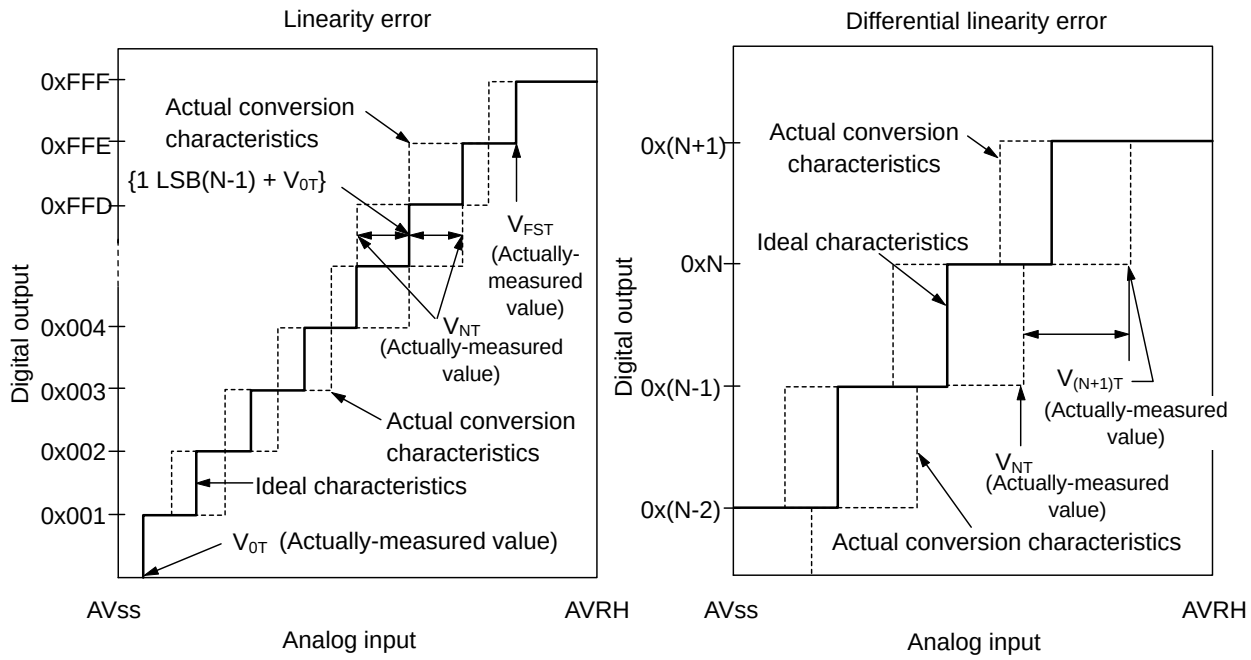
Ts : Sampling time
R_{AIN} : input resistance of A/D = 0.9kΩ at $4.5 \leq AVCC \leq 5.5$
input resistance of A/D = 1.6kΩ at $2.7 \leq AVCC < 4.5$
input resistance of A/D = 4.0kΩ at $1.8 \leq AVCC < 2.7$
C_{AIN} : input capacity of A/D = 15pF at $1.8 \leq AVCC \leq 5.5$
Rext : Output impedance of external circuit

(Equation 2) $Tc = Tcck \times 14$

Tc : Compare time
Tcck : Compare clock cycle

・Definition of 12-bit A/D Converter Terms

- ・Resolution : Analog variation that is recognized by an A/D converter.
- ・Linearity error : Deviation of the line between the zero-transition point (0b000000000000←→0b000000000001) and the full-scale transition point (0b111111111110←→0b111111111111) from the actual conversion characteristics.
- ・Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{0T}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{0T}}{4094}$$

N : A/D converter digital output value.
V_{0T} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

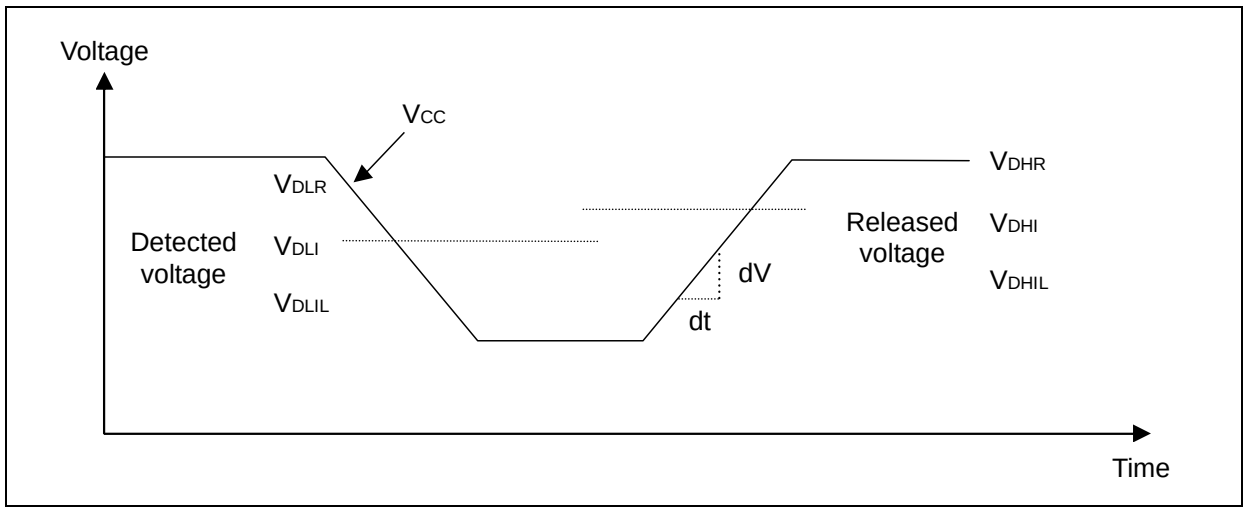
6. Low-Voltage Detection Characteristics

(1) Low-Voltage Detection Reset

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLR}	SVHR = 0001	1.43	1.53	1.63	V	When voltage drops
Released voltage	V_{DHR}		1.53	1.63	1.73	V	When voltage rises
Detected voltage	V_{DLR}	SVHR = 0100	1.80	1.93	2.06	V	When voltage drops
Released voltage	V_{DHR}		1.90	2.03	2.16	V	When voltage rises
LVD stabilization wait time	T_{LVDRW}	-	-	-	633 × t_{CYCP} *	µs	
Detection delay time	T_{LVDRD}	dV/dt ≥ -4mV/µs	-	-	60	µs	

* : t_{CYCP} indicates the APB2 bus clock cycle time.



(2) Interrupt of Low-voltage Detection

- Normal mode

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLI}	SVHI = 0000	1.87	2.00	2.13	V	When voltage drops
Released voltage	V_{DHI}		1.97	2.10	2.23	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0001	1.96	2.10	2.24	V	When voltage drops
Released voltage	V_{DHI}		2.06	2.20	2.34	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0010	2.05	2.20	2.35	V	When voltage drops
Released voltage	V_{DHI}		2.15	2.30	2.45	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0011	2.15	2.30	2.45	V	When voltage drops
Released voltage	V_{DHI}		2.25	2.40	2.55	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0100	2.24	2.40	2.56	V	When voltage drops
Released voltage	V_{DHI}		2.34	2.50	2.66	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0101	2.33	2.50	2.67	V	When voltage drops
Released voltage	V_{DHI}		2.43	2.60	2.77	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0110	2.43	2.60	2.77	V	When voltage drops
Released voltage	V_{DHI}		2.53	2.70	2.87	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 0111	2.61	2.80	2.99	V	When voltage drops
Released voltage	V_{DHI}		2.71	2.90	3.09	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1000	2.80	3.00	3.20	V	When voltage drops
Released voltage	V_{DHI}		2.90	3.10	3.30	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1001	2.99	3.20	3.41	V	When voltage drops
Released voltage	V_{DHI}		3.09	3.30	3.51	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1010	3.36	3.60	3.84	V	When voltage drops
Released voltage	V_{DHI}		3.46	3.70	3.94	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1011	3.45	3.70	3.95	V	When voltage drops
Released voltage	V_{DHI}		3.55	3.80	4.05	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1100	3.73	4.00	4.27	V	When voltage drops
Released voltage	V_{DHI}		3.83	4.10	4.37	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1101	3.83	4.10	4.37	V	When voltage drops
Released voltage	V_{DHI}		3.93	4.20	4.47	V	When voltage rises
Detected voltage	V_{DLI}	SVHI = 1110	3.92	4.20	4.48	V	When voltage drops
Released voltage	V_{DHI}		4.02	4.30	4.58	V	When voltage rises
LVD stabilization wait time	T_{LVDIW}	-	-	-	633 × t_{CYCP}*	µs	
Detection delay time	T_{LVDID}	dV/dt ≥ -4mV/µs	-	-	60	µs	

* : t_{CYCP} indicates the APB2 bus clock cycle time.

- Low power mode

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V_{DLIL}	SVHI = 0000	1.80	2.00	2.20	V	When voltage drops
Released voltage	V_{DHIL}		1.90	2.10	2.30	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0001	1.89	2.10	2.31	V	When voltage drops
Released voltage	V_{DHIL}		1.99	2.20	2.41	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0010	1.98	2.20	2.42	V	When voltage drops
Released voltage	V_{DHIL}		2.08	2.30	2.52	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0011	2.07	2.30	2.53	V	When voltage drops
Released voltage	V_{DHIL}		2.17	2.40	2.63	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0100	2.16	2.40	2.64	V	When voltage drops
Released voltage	V_{DHIL}		2.26	2.50	2.74	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0101	2.25	2.50	2.75	V	When voltage drops
Released voltage	V_{DHIL}		2.35	2.60	2.85	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0110	2.34	2.60	2.86	V	When voltage drops
Released voltage	V_{DHIL}		2.44	2.70	2.96	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 0111	2.52	2.80	3.08	V	When voltage drops
Released voltage	V_{DHIL}		2.62	2.90	3.18	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1000	2.70	3.00	3.30	V	When voltage drops
Released voltage	V_{DHIL}		2.80	3.10	3.40	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1001	2.88	3.20	3.52	V	When voltage drops
Released voltage	V_{DHIL}		2.98	3.30	3.62	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1010	3.24	3.60	3.96	V	When voltage drops
Released voltage	V_{DHIL}		3.34	3.70	4.06	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1011	3.33	3.70	4.07	V	When voltage drops
Released voltage	V_{DHIL}		3.43	3.80	4.17	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1100	3.60	4.00	4.40	V	When voltage drops
Released voltage	V_{DHIL}		3.70	4.10	4.50	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1101	3.69	4.10	4.51	V	When voltage drops
Released voltage	V_{DHIL}		3.79	4.20	4.61	V	When voltage rises
Detected voltage	V_{DLIL}	SVHI = 1110	3.78	4.20	4.62	V	When voltage drops
Released voltage	V_{DHIL}		3.88	4.30	4.72	V	When voltage rises
LVD stabilization wait time	T_{LVDILW}	-	-	-	8039 × t_{CYCP} *	µs	
Detection/Release delay time	T_{LVDILD}	dV/dt ≥ -0.4mV/µs	-	-	800	µs	

* : t_{CYCP} indicates the APB2 bus clock cycle time.

7. Flash Memory Write/Erase Characteristics

(Vcc = 2.0V to 5.5V, Ta = - 40°C to + 85°C)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.6	3.1	s	Excludes write time prior to internal erase
	Small Sector		0.3	1.6		
Half word (16-bit) write time		-	25	400	µs	Not including system-level overhead time.
Chip erase time		-	1.8	9.4	s	Excludes write time prior to internal erase

Write cycles and data hold time

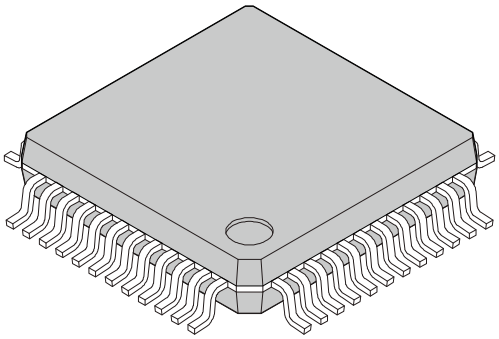
Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20*	
10,000	10*	
100,000	5*	

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

■ ORDERING INFORMATION

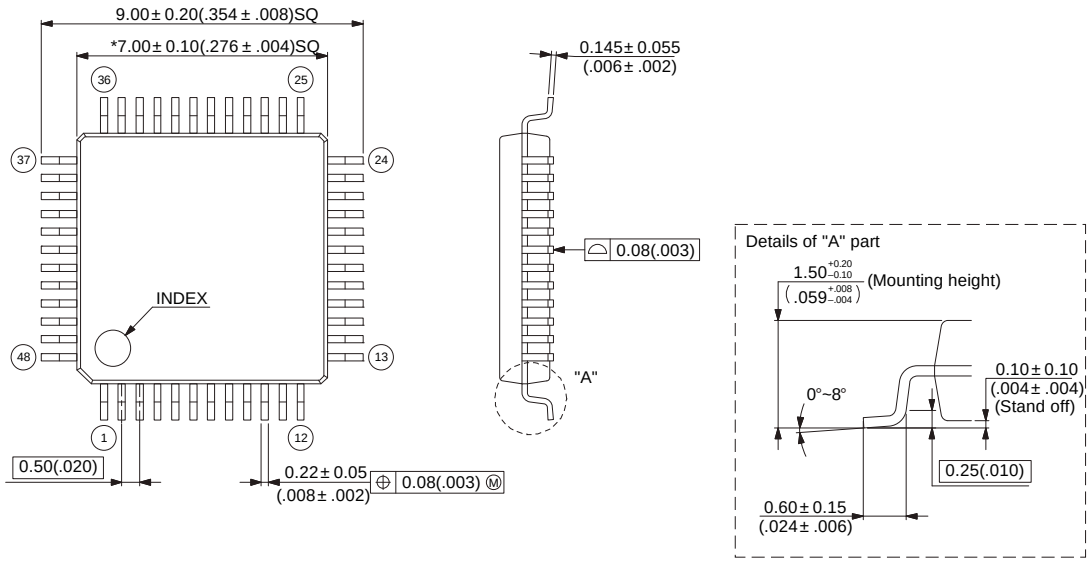
Part number	Package
MB9AF131KAPMC	Plastic・LQFP(0.5mm pitch), 48-pin (FPT-48P-M49)
MB9AF132KAPMC	
MB9AF131KAQN	Plastic・QFN(0.5mm pitch), 48-pin (LCC-48P-M73)
MB9AF132KAQN	
MB9AF131LAPMC1	Plastic・LQFP(0.5mm pitch), 64-pin (FPT-64P-M24/M38)
MB9AF132LAPMC1	
MB9AF131LAPMC	Plastic・LQFP(0.65mm pitch), 64-pin (FPT-64P-M39)
MB9AF132LAPMC	
MB9AF131LAQN	Plastic・QFN(0.5mm pitch), 64-pin (LCC-64P-M24)
MB9AF132LAQN	

■ PACKAGE DIMENSIONS

48-pin plastic LQFP		
 (FPT-48P-M49)	Lead pitch	0.50 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g

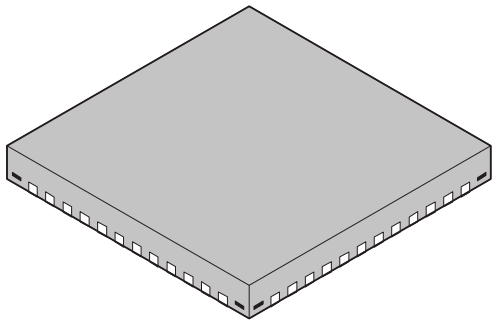
48-pin plastic LQFP
(FPT-48P-M49)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

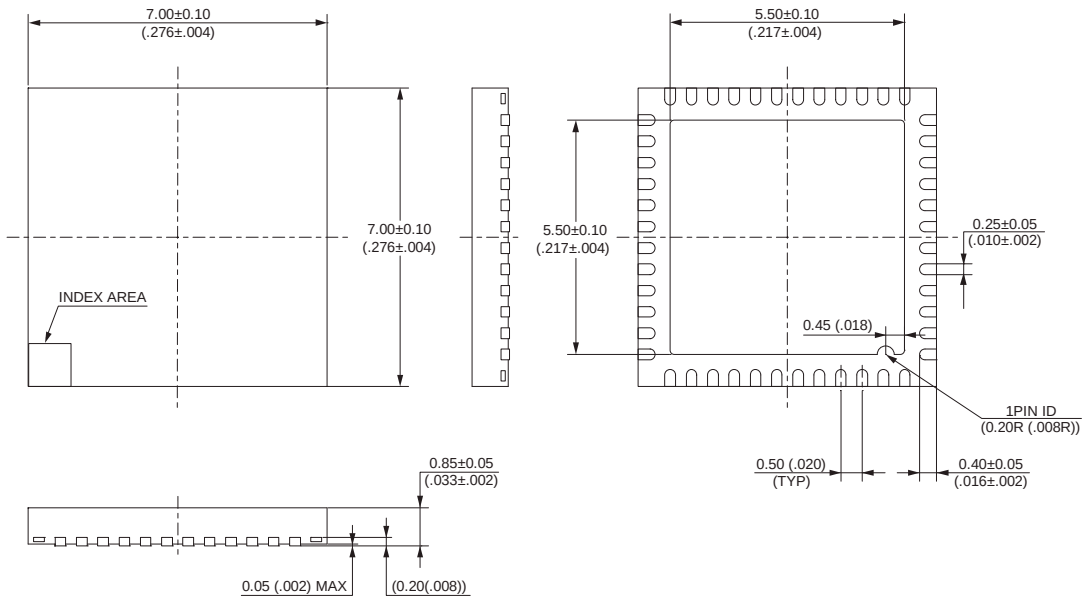


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

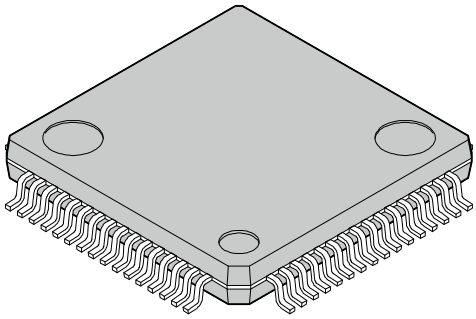
48-pin plastic QFN		
	Lead pitch	0.5 mm
	Package width × package length	7.00 mm × 7.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	–
(LCC-48P-M73)		

48-pin plastic QFN
(LCC-48P-M73)



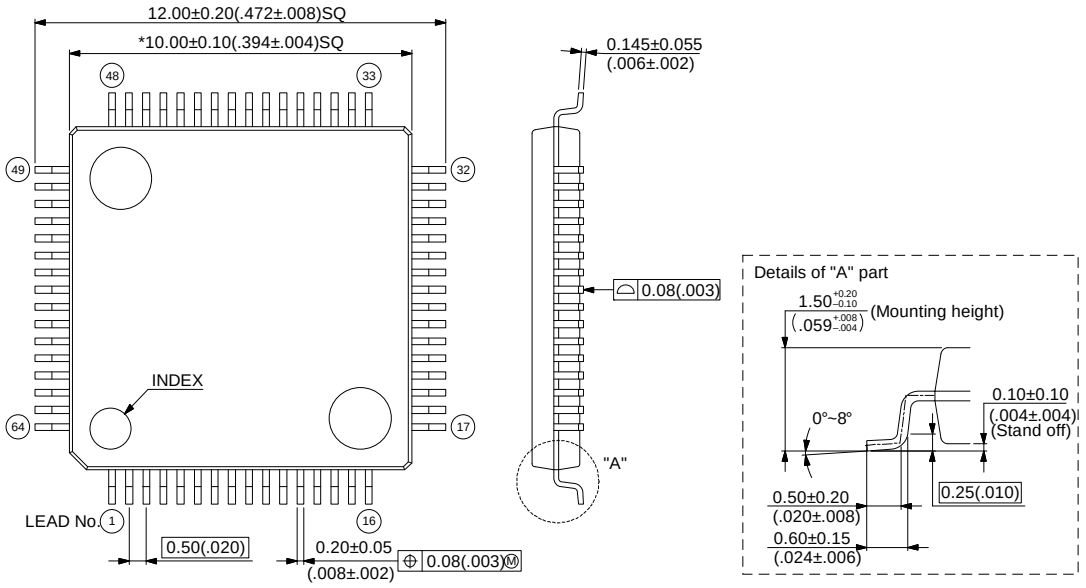
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-64P-M24)	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

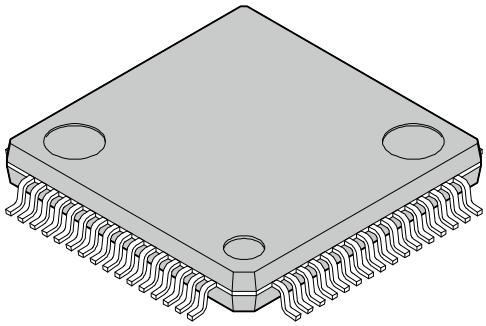
Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

64-pin plastic LQFP

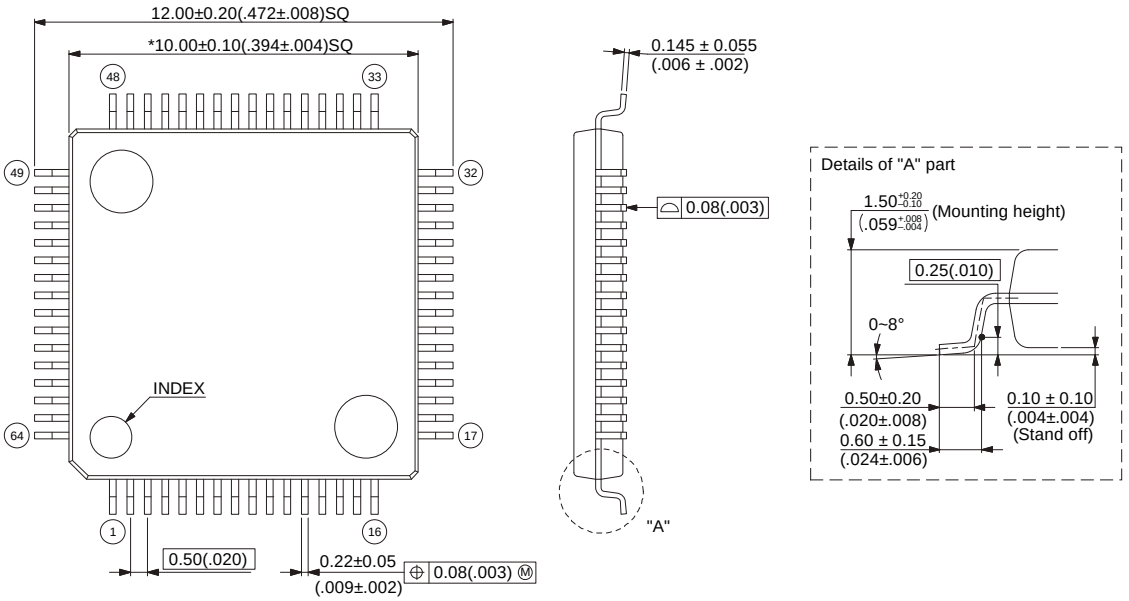


(FPT-64P-M38)

Lead pitch	0.50 mm
Package width × package length	10.00 mm × 10.00 mm
Lead shape	Gullwing
Lead bend direction	Normal bend
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.32 g

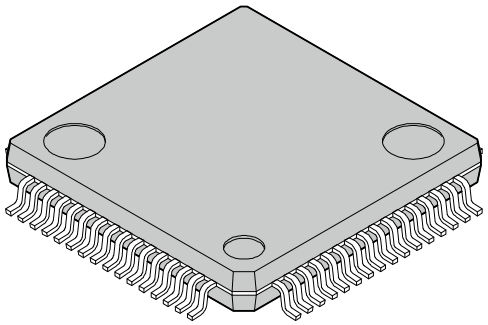
64-pin plastic LQFP
(FPT-64P-M38)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



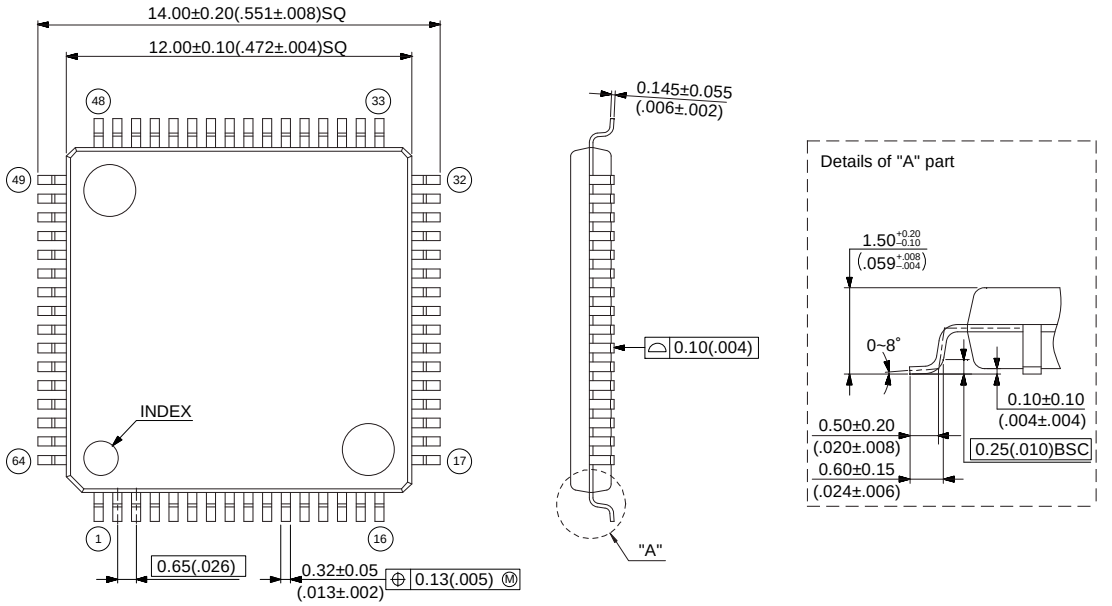
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.00 mm × 12.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
(FPT-64P-M39)		

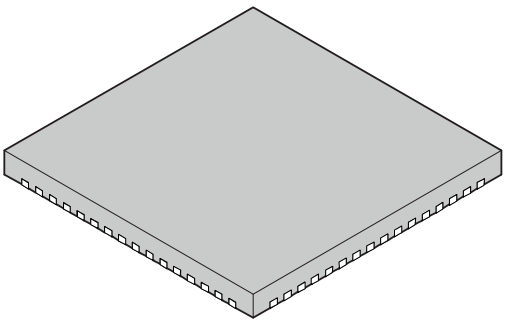
64-pin plastic LQFP
(FPT-64P-M39)

Note 1) Pins width and pins thickness include plating thickness.

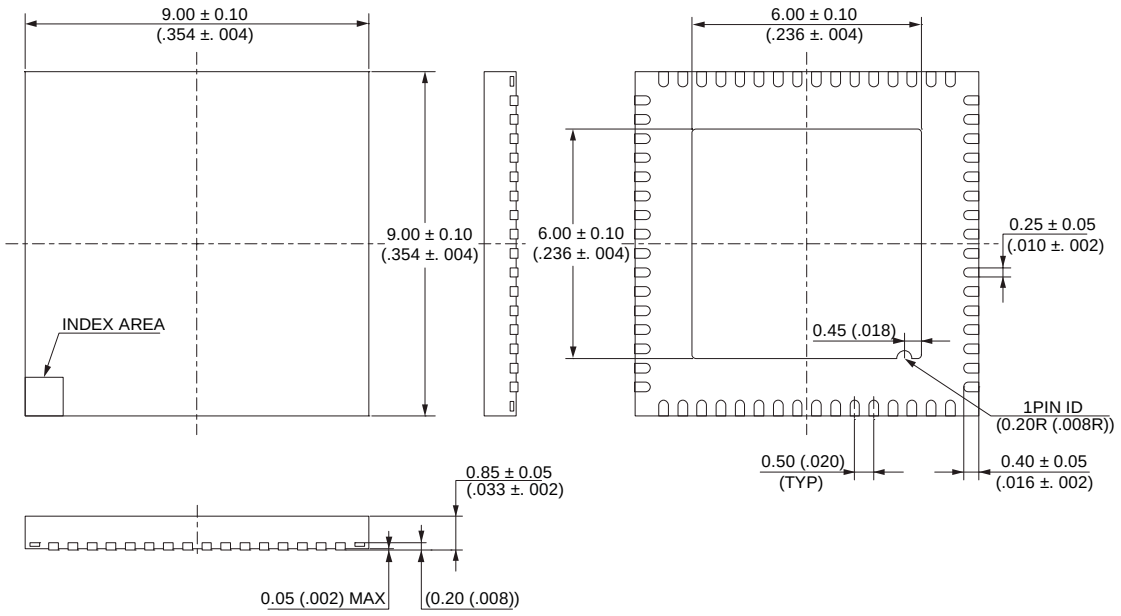


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

64-pin plastic QFN		
	Lead pitch	0.50 mm
	Package width × package length	9.00 mm × 9.00 mm
	Sealing method	Plastic mold
	Mounting height	0.90 mm MAX
	Weight	-
(LCC-64P-M24)		

64-pin plastic QFN
(LCC-64P-M24)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
34	■HANDLING DEVICES	Revised the description of "•C pin".
35	■BLOCK DIAGRAM	Corrected the figure. • TIOA: input → input/output • TIOB: output → input
40 to 44	■PIN STATUS IN EACH CPU STATE • List of Pin Status	Corrected the Pin status conditions. "Timer mode, RTC mode, or sleep mode state" → "Timer mode, RTC mode, or STOP mode state"
46	■ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	• Added the "Smoothing capacitor (C_S)". • Added the footnote.
50	4. AC Characteristics (1) Main Clock Input Characteristics	Added "Internal operating clock frequency (F_{CM}): Master clock".
52	(4-1) Operating Conditions of Main PLL (In the case of using main clock for input of PLL)	Added "Main PLL clock frequency (F_{CLKPLL})".
	(4-2) Operating Conditions of Main PLL (In the case of using high-speed internal CR)	
66	5. 12-bit A/D Converter • Electrical characteristics for the A/D converter	• Added the Symbol. • Deleted the following Pin name. - "Sampling time" - "Compare clock cycle" - "State transition time to operation permission" - "Analog input capacity" - "Analog input resistance" • Corrected the value of "Period of operation enable state transitions (Tstt)". Min: 10µs → 1µs
72	7. Flash Memory Write/Erase Characteristics Write cycles and data hold time	Added the Condition of " Erase/Write cycles "

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FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
902 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fsk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://sg.fujitsu.com/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
30F, Kerry Parkside, 1155 Fang Dian Road,
Pudong District, Shanghai 201204, China
Tel : +86-21-6146-3688 Fax : +86-21-6146-3660
http://cn.fujitsu.com/fss/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
2/F, Green 18 Building, Hong Kong Science Park,
Shatin, N.T., Hong Kong
Tel : +852-2736-3232 Fax : +852-2314-4207
http://cn.fujitsu.com/fsp/

Edited: Sales Promotion Department