Peripheral 8051 System on a Chip

The P-51 "Peripheral 8051" is a new concept: An 8051 with built-in (E)ISA or PC-104 interface and supporting subsystems. These include downloadable Code RAM, dual port RAM, and all eleven IRQs to the host. Unlike classical 8051s, the P-51 naturally and easily interfaces to a host through simple standard buses, and its microsecond timing can provide real-time response to Windows applications.

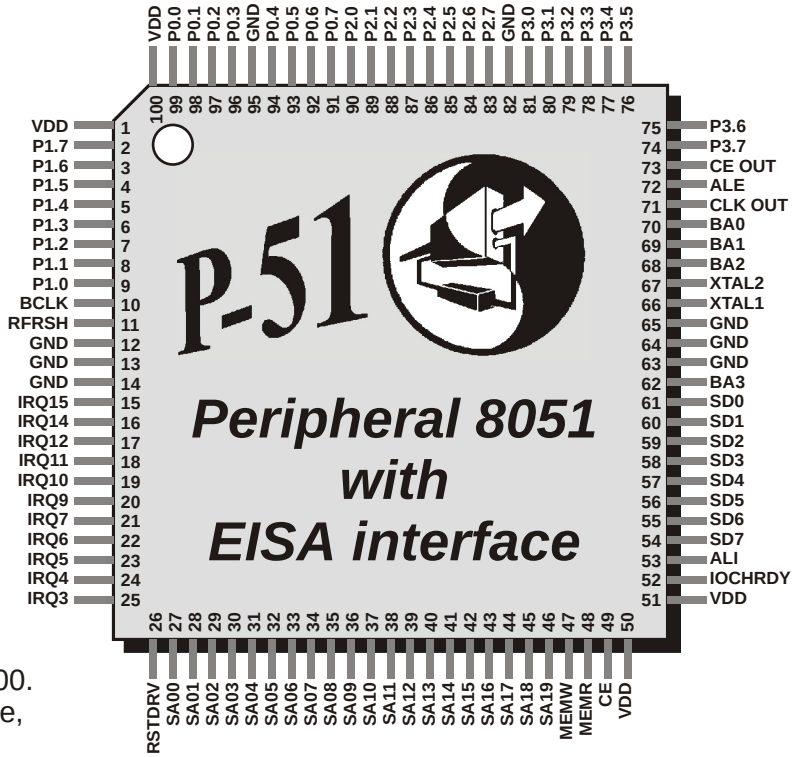
P-51 Features

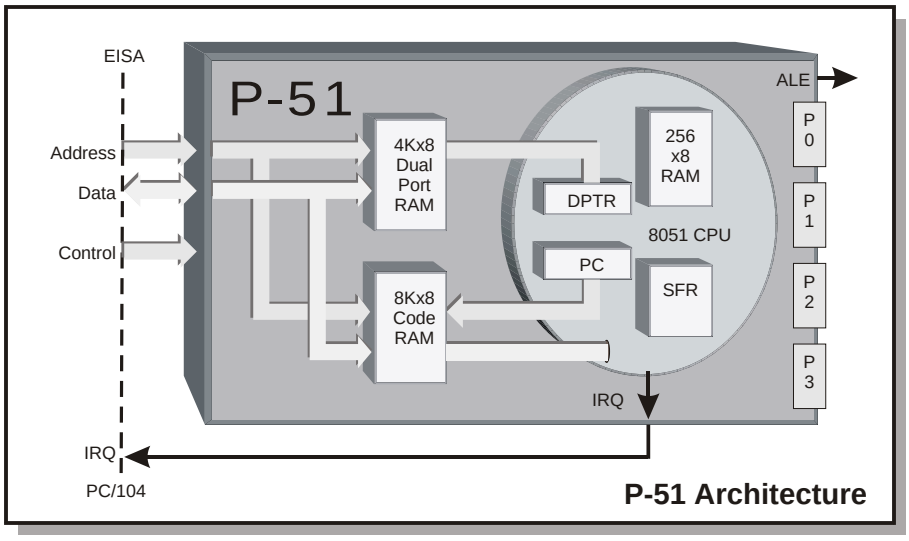
All 8051/52 resources:

- 8K bytes downloadable Code RAM.
- 256 bytes internal Data RAM.
- Timers 0, 1, and 2.
- Ports 0, 1, 2, and 3.
- All 8051 Instructions.
- All 8051-equivalent Pins.
- Download Code RAM while reset.
- Execute Code when released.

EISA/PC-104 interface:

- 45 EISA signals supported.
- Uses one of 11 IRQ pins.
- Software selectable IRQ 3…15.
- 20 ISA Address pins.
- 8 ISA Data Bus pins.
- Hardware or software Reset.
- Select Segment Addr 0 and A400 to EC00.
- Uses 16K bytes of system memory space, normally in an Upper Memory Block.





P-51 Architecture

Special Features:

- 4K byte dual port RAM shared by host and P-51.
- Dual Data Pointer.
- Six new P-51 Control Registers mapped into dual port RAM.
- Square Root function.
- Debug capability.
- Breakpoint and single-step.
- Software interrupt generation.
- 3.3v 100-pin QFP.
- 5v I/O tolerant.
- 51 MHz operation

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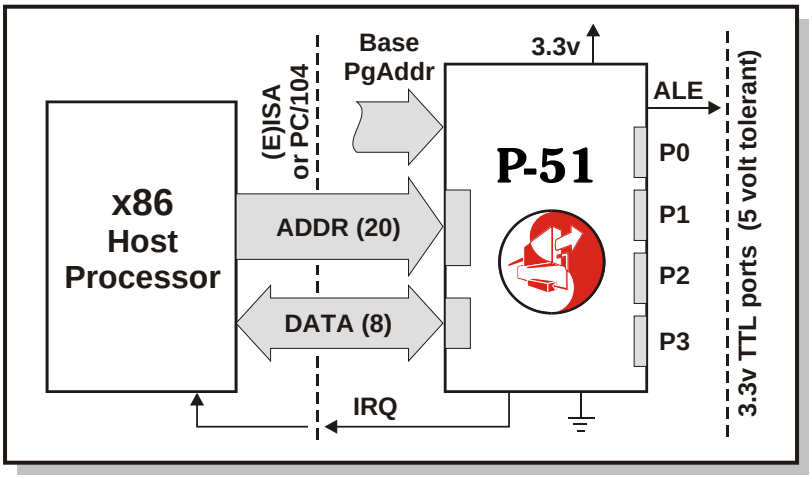
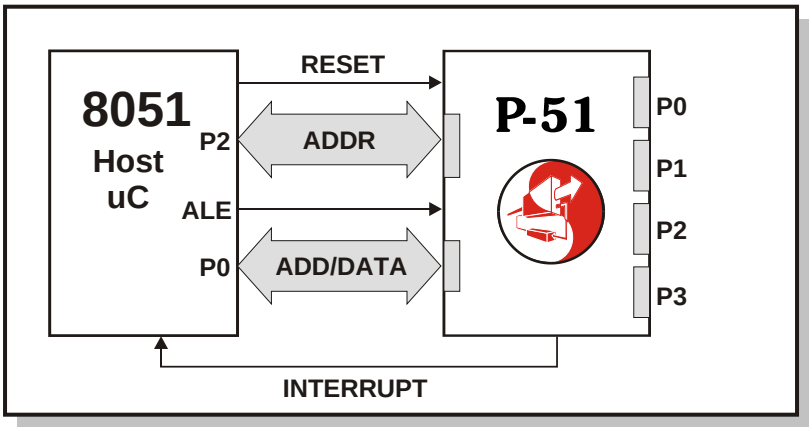
Think of the P-51 as the ultimate peripheral. You've used programmable timers, counters, interrupt controllers, and other special purpose peripherals. Now the P-51 allows you to directly connect a general purpose 8051 computer, with all its hardware and software resources, to almost any bus: ISA, PC/104, or micro-controller. You can drive a P-51 directly from an 8051, 386EX, or Z80. Via the P-51 chip select pin you can even hang multiple P-51s on a single bus.

P-51 Peripheral to an x86



In the case of the 20-bit address presented by the EISA bus, the high order bits are compared to the Base Page address pins, and the P-51 is enabled when addresses match, thereby allowing the P-51 to be located at a specific range in x86 address space. By writing to a P-51 control register, the x86 can select (and enable) an IRQ signal (from IRQ3 to IRQ15).

P-51 Peripheral to an 8051



In this example a standard 8051 uses P0, P2, and control strobes to control a P-51, effectively doubling 8051 resources. The internal dual port RAM serves as a mailbox for communicating between the two and also can be used as 4K RAM data for a standard 8051. The standard 8051 can download code to the P51 while holding it in reset, then release the P51 to run the code. Think of the possibilities!

Breakpoint and Single Stepping

The P-51 supports breakpoints and single stepping. When the P-51 encounters a breakpoint in the code, the P-51 copies its program counter into dual port RAM, interrupts the host with a breakpoint interrupt, and then waits for the host. The host performs any action that is appropriate, then releases the P-51 by clearing a "wait" bit in a dual port RAM-mapped control register. The host can set a single-step bit in the control register, which causes the P-51 to interrupt the host after every instruction execution. The combination of break and step provides features that would require an in-circuit emulator in a standard 8051

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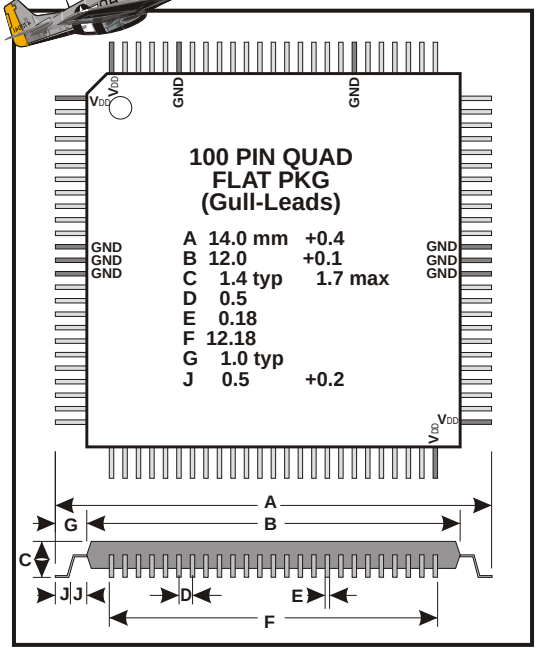
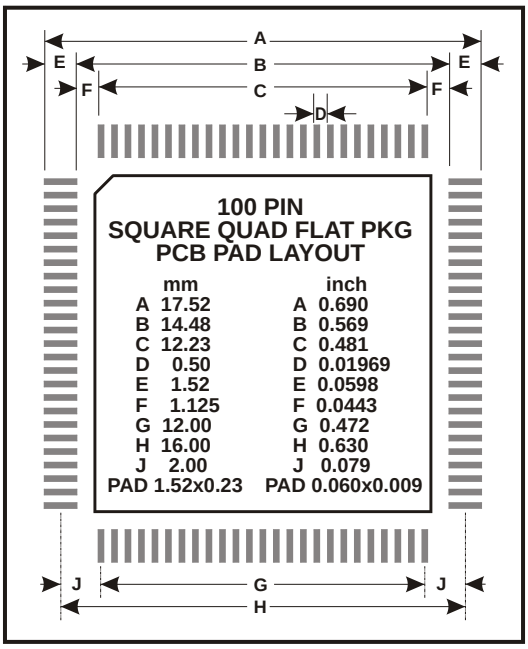
Physical Specifications





Electrical Specifications

Absolute Maximum Ratings:

Ambient Temperature under bias .. 0ºC to 70ºC
Storage Temperature.....–55ºC to +125ºC
Vdd Supply Voltage.....–0.3V to +4.0V
Voltage on any I/O pin from GND..–0.3V to +6.0V
Power Dissipation.....500 mW

DC and Operating Characteristics:

Temperature Range..... 0ºC to 70ºC
Vdd Supply Voltage.....+3.0V to +3.6V

A Peripheral Device

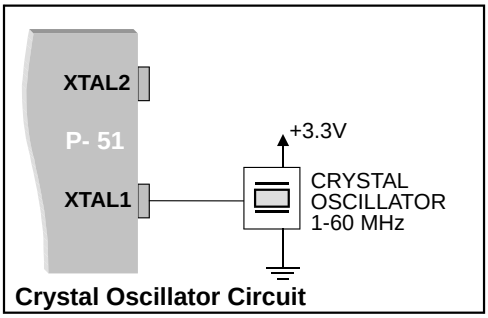
The P-51 name is a reminder that this device is a Peripheral 8051 processor, not a standalone processor. The name P-51 focuses on this unique aspect of the device: A peripheral 8051 requires a host to which it is peripheral.

Clock Circuits

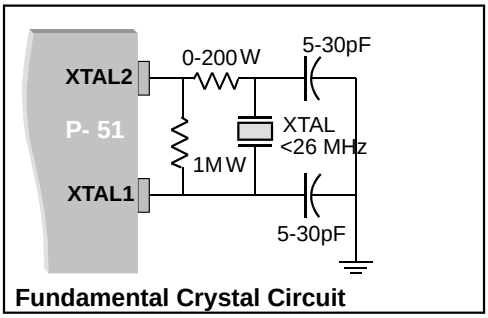
An external Clock Oscillator between 1 and 60 MHz is used on XTAL1, and must use the same VDD voltage as the P-51.

The frequency range for the Crystal circuit is 4 to 51 MHz. The circuitry differs for fundamental vs. third-overtone crystals. The boundary between the two types is approx 26 MHz (consult crystal manufacturer specs).

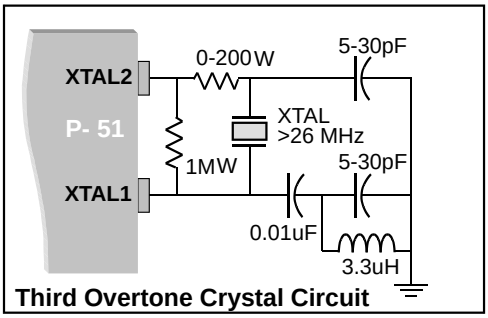
Like standard 8051 devices, the internal P-51 serial baud rates assume an 11.059 MHz clock and multiples thereof.



Crystal Oscillator Circuit



Fundamental Crystal Circuit



Third Overtone Crystal Circuit

Sym	Parameter	Min	Typ	Max	Unit	Remarks
Icc	pwr supply current		46	80	mA	60 MHz
			20	40	mA	40 MHz
			16	35	mA	11 MHz
Vih	input high voltage	2.0		5.5	V	5 Volt tolerant inputs, TTL compatible
Vil	input low voltage	-0.2		0.8	V	TTL compatible
Iih	input high current	-10		+10	uA	Vin = Vdd
Iil	input low current	-10		+10	uA	Vin = GND
Voh	output high voltage	2.4			V	Ioh = -4 mA
Vol	output low voltage			0.4	V	Iol = 4 mA
				0.4	V	Iol = 8 mA on IoChRdy
Ioz	Tri-state leakage current	10		+10	uA	Vin = GND to Vdd
Ipu	Pull-up current	22	66	160	uA	Vin = GND, R ~ 50KW
Fcy	crystal frequency	4		51	MHz	see clock circuits
Fos	oscillator frequency	1		60	MHz	see clock circuits

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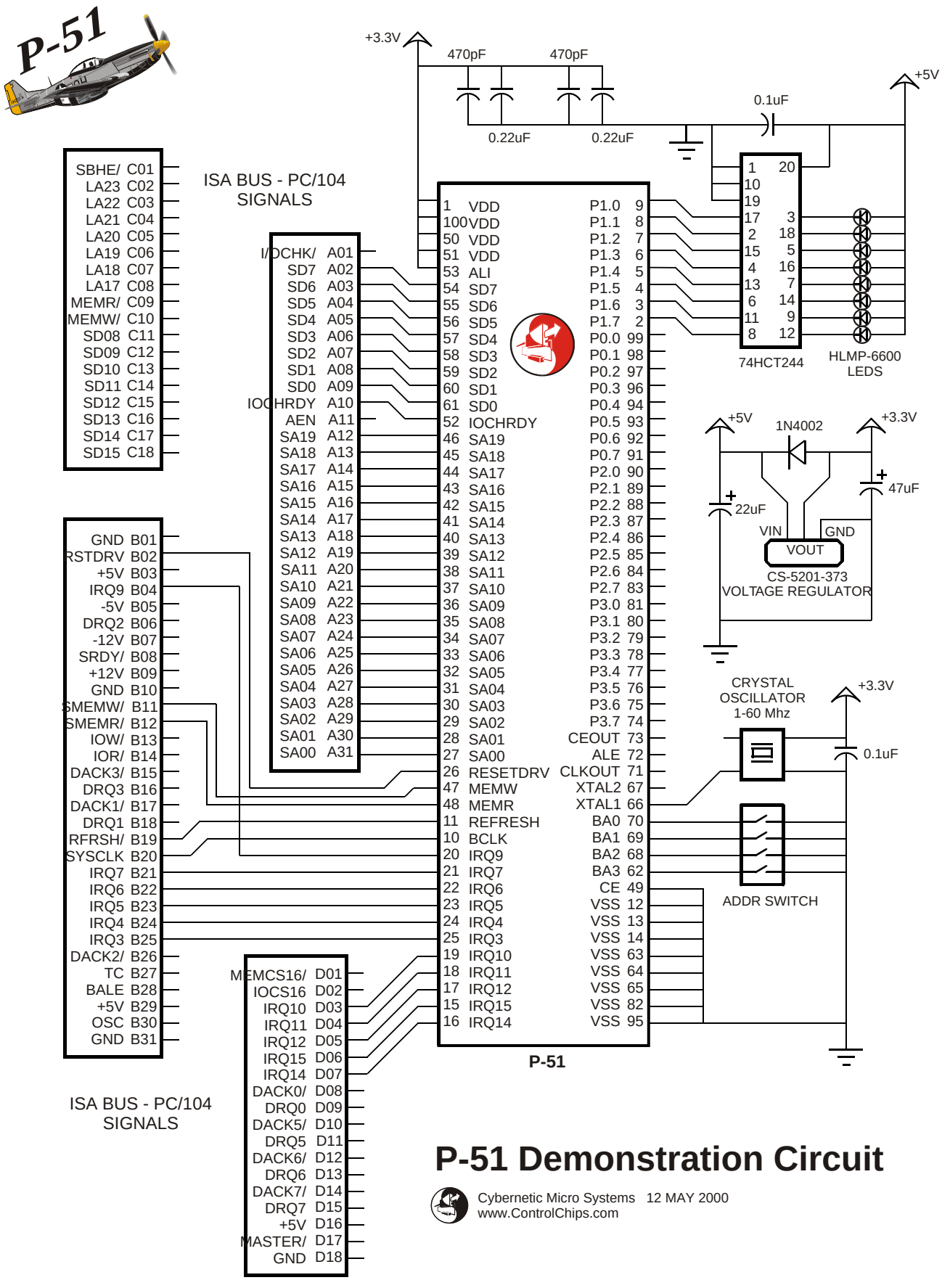

P-51 Demonstration Circuit

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