R8051XC

Configurable 8-Bit Microcontroller Core

The R8051XC is a configurable, single-chip, 8-bit microcontroller core that can implement a variety of fast processor variations executing the MCS® 51 instruction set.

The efficient core design runs an average of 8.1 times faster than the 80C51. A rich set of optional features and peripherals enable designers to closely match the core with their specific application and hardware requirements (FPGA, ASIC, or structured ASIC). These options include hardware interrupts, interfaces for serial communication, I2C and SPI interfaces, a timer system, I/O ports, a power management unit, a multiplication-division unit, a watchdog timer, DMA controller and a real-time clock. Integrated on-chip debugging using either the native OCDS or FS2's OCI is also available.

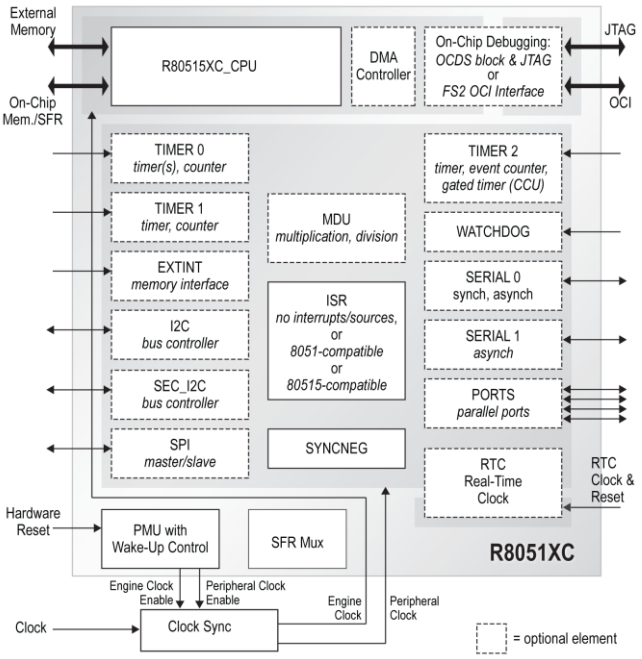
The R8051XC is an extension of our proven 8051 family of processor cores, which have been successfully implemented in a hundred different customer products. Designers can purchase a custom configuration by selecting a set of options that best meets their needs, or choose from these three prepackaged versions of the core:

- R8051XC-F is the fully-configurable version of the core, with all options included. This is the only version that allows the user to configure the core with any of the available options.
- R8051XC-A matches our earlier R8051, with a set of peripherals making it compatible with the Intel 80C31 (see details in the Configurations section).
- R80515XC-B matches our earlier R80515 core, with a set of peripherals making it compatible with the Siemens 80C515 and 80C517.

Representative ASIC implementation results for the different configurations range from under 9,000 gates for the R8051XC-A to under 47,000 for all available options (except debug). Speed ranges from 250 to 350 MHz and above, depending on the technology.

Developed for easy reuse in ASIC and FPGA implementations, the core is strictly synchronous, with positive-edge clocking, no internal tri-states, and a synchronous reset.

Block Diagram



Features

- Eight-bit instruction decoder for MCS® 51 instruction set
- Executes instructions with one clock per cycle (versus twelve for standard 80C51) for an average 8.1 times speed increase
- ALU performs 8-bit arithmetic and logical operations and Boolean manipulations; additional 8-bit multiplication and division are optional
- Flexible external memory interface can address up to 8 MB of Program Memory and 8 MB of Data Memory Space (when using memory banking)
- SFR interface services 40 to 118 external Special Function Registers (depending on peripherals configuration)
- Extensive core configurability: choose options as needed, or get fully-configurable version

Optional Functions and Peripherals in the –F Version

- Direct Memory Access (DMA) Controller
  - Up to eight independent channels
  - Read/Write Access to all memory spaces (incl. SFR)
  - Linear addressing (up to 8MB)
  - Address auto-increment/decrement
  - Synchronous/asynchronous Mode
  - Software Trigger/Hardware Trigger
- Register Control Unit
  - Interfaces for 128 B or 256 B internal Data Memory Space
  - Interface for extra on-chip SFRs
- Program memory write mode allows writes to external program memory space
- External Memory Interface
  - Addresses up to 8 MB of Program Memory and up to 8 MB of Data Memory
  - One, two, or eight Data Pointers for fast data block transfer
- Interrupt Controller: four priority levels with eighteen interrupt sources, or two priority levels with six sources

Features continue

Features, continued

- Power Management Unit with power-down modes (IDLE and STOP). Interface for on-chip debug: native On-Chip Debug Support (OCDS) or FS2 On-Chip Instrumentation (OCI)
- Multiplication-Division Unit
  - 16 x 16-bit multiplication
  - 32/16- and 16/16-bit division
  - 32-bit normalization and L/R shifting
- 16-bit Timer/Counters:
  80C51-like Timers 0 and 1, or the 80C515-like Timer 2
- Timer 2 includes a Compare/Capture Unit with four 16-bit Compare registers for Pulse Width Modulation; four external Capture inputs for Pulse Width Measuring; and a 16-bit Reload register for Pulse Generation
- Input/Output ports
  - Up to four (configurable) 8-bit I/O ports
  - Alternate port functions, such as external interrupts and the serial interface are separated, providing extra port pins when compared with the standard 8051
- Serial 0: a full-duplex serial interface (80C51-like)
- Serial 1: an asynchronous-only version of Serial 0
- 15-bit programmable Watchdog timer
- I2C™ and one or two SPI interfaces
- Sophisticated self-checking Testbench (Verilog versions use Verilog 2001)

Applications

With numerous options for features and capabilities, designers can readily configure a version that best matches their particular needs, from fitting in the smallest device to controlling complex systems. Suitable application areas include: embedded microcontroller systems; communication systems; data computation and transfer functions; and professional audio and video products.

Functional Description

The core is partitioned into modules as shown in the block diagram and described below.

Central Processing Unit

The CPU fetches instructions from program memory and uses RAM or SFRs as operands. Provides the ALU for 8-bit arithmetic, logic, multiplication and division operations, and Boolean manipulations. The RAM and SFR interface can address up to 256 bytes of Read/Write Data Memory Space and built-in and off-core Special Function Registers. The memory interface can address from 64KB to 8MB of Program and Data Memory.

DMA Controller

The Direct Memory Access (DMA) Controller contains up to eight individual channels, each capable of transferring data from or to any addressable location (program memory, internal or external data memory, or SFR). Each channel can work in synchronous mode (when just one byte is transferred at each trigger) or asynchronous mode (when all the data is transferred at once). Transfers can be triggered by software or by a specified interrupt source.

External Memory Interface

The flexible external memory interface can address up to 8 MB of Program Memory and 8 MB of Data Memory Space. It uses a HOLD interface to support any external DMA controller, and it eases the connection to memories using a demultiplexed address/data bus. The EMI uses variable-length code fetch and MOVC to access fast or slow program memory, and similarly uses a variable-length MOVX to access fast or slow RAM or peripherals.

Ports

The parallel I/O port controller serves up to four parallel 8-bit I/O ports to be used with off-core buffers. It is compatible with the classic Intel™ 80C51, but lacks the multiplexed memory feature and alternate functions. (These could be combined off-core if required).

Timers 0 and 1

Timers 0 and 1 are nearly identical, and they each have these three modes: 13-bit timer/counter, 16-bit timer/counter, and 8-bit timer/counter with auto reload. Timer 0 has an additional mode: two 8-bit timers. Each timer can also count external pulses (1 to 0 transition) on the corresponding `t0` or `t1` pin. Another option is to gate the timer/counter using an external control signal, which allows it to measure the pulse width of external signals.

Timer 2

Operates as a timer, event counter, or compare/capture unit.

In timer mode, Timer 2 can be incremented every machine cycle or every second machine cycle, depending on the 2:1 prescaler. In event counter mode, Timer 2 is incremented when an external signal changes from 1 to 0 (sampled every machine cycle). Timer 2 is incremented in the cycle following the one in which that transition was detected. In gated timer mode, Timer 2's incrementing is gated by an external signal.

A Timer 2 reload can be executed in two modes. In Mode 0, the reload signal is generated by a Timer 2 overflow (auto reload), while in Mode 1 it is generated by a negative transition at the corresponding input pin `t2ex`.

Compare/Capture Unit

The CCU within Timer2 performs Compare and Capture functions. For the Compare function, values stored in four 16-bit compare/capture registers are compared with the contents of the Timer 2 register. The results are signaled and interrupts are generated.

For the Capture function, actual timer/counter contents can be saved into one of four 16-bit registers upon an external event (Mode 0) or software write operation (Mode 1).

Multiplication Division Unit

This on-chip arithmetic unit performs these unsigned integer operations:

- 16 x 16-bit multiplication
- 32/16-bit division and 16/16-bit division
- 32-bit normalization and L/R shifting

The MDU allows operations to occur concurrently to and independent of the engine activity.

Serial 0 and 1

The core includes two independent serial ports for simultaneous communication over two channels. They can operate in identical or different modes and at different communication speeds. Serial 0 is capable of both synchronous and asynchronous transmission, while Serial 1 provides asynchronous mode only.

In synchronous mode, the microcontroller generates a clock and operates in half-duplex mode. In asynchronous mode, full-duplex operation is available. Received data is buffered in a holding register, which allows the serial ports to receive an incoming word before the software has read the previous value.

Serial 0 offers the following communication protocols:

- Synchronous mode, fixed baud rate
- 8- and 9-bit UART modes, variable baud rate
- 9-bit UART mode, fixed baud rate

Serial 1 has two operating modes:

- 8- and 9-bit UART mode, variable baud rate

Both include an additional Baud Rate Generator.

Power Management Unit (PMU) & Reset Control

Generates clock enable signals for the main CPU and for peripherals; serves Power Down Modes IDLE and STOP; and generates an internal synchronous reset signal (upon external reset or watchdog timer overflow).

IDLE mode leaves the clock of the internal peripherals running. Power consumption drops because the CPU is not active. Any interrupt or reset will wake the CPU.

STOP mode turns off all internal clocks. The CPU will exit this state with an external interrupt or reset. Internally generated interrupts (timer, serial port, watchdog, ...) are disabled since they require clock activity.

Wake-up Control

The Wake-up From Power-Down Mode Control Unit services two external interrupts during power-down modes.

Real-Time Clock

The RTC generates a real-time count with a resolution of 1/256th second and range of 179 years. It can set and read seconds, minutes, hours, day of the week, and the date, represented by a 16-bit number interpreted by software. An alarm function can generate interrupts periodically or at a specific time, and these may be used to wake up from IDLE/STOP mode.

SFR Mux

The SFR Multiplexer provides a common bus multiplexer for all the internal and external Special Function Registers.

On-Chip Debugging

Serves as the interface for On-Chip Debug Support using an IEEE1149.1 (JTAG) port. Implements either native On-Chip Debug Support (OCDS) or FS2's On-Chip Instrumentation (OCI). See their respective datasheets for details.

Watchdog Timer

A 15-bit counter that is incremented every 24 or 384 clock cycles. After an external reset, it is disabled and all registers are set to zeros. It can be started by applying an active input during reset (hardware automatic start) or by setting the enable bit by software. Once started, it cannot be stopped unless the internal reset signal becomes active. This occurs when the Watchdog enters the state 7CFFh, and it can be avoided by refreshing the Watchdog with software before it reaches 7CFFh.

Interrupt Service Routine Unit

The R8051XC provides two types of interrupt controllers: an 8051-compatible with up to six interrupt sources and two priority levels, or an 80515-compatible with up to eighteen interrupt sources and four priority levels. Each source has its own request flag(s) located in a dedicated SFR. Each interrupt requested by the corresponding flag can be individually enabled or disabled by dedicated enable bits in the SFRs.

Primary and Secondary I2C™ Interfaces

The primary (I2C) and secondary (SEC_I2C) I2C Bus Controllers each provide a serial interface that meets the Philips I2C bus specification and supports all master/slave receiver/transmitter modes. Each is a true multi-master bus controller, including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer. They perform 8-bit oriented, bi-directional data transfers up to 100 kbit/s in the standard mode, or up to 400 kbit/s in the fast mode

Serial Peripheral Interface (SPI) Interface

Provides full-duplex, synchronous communication between the core and other peripheral devices, including other MCUs. It can operate either as Master or Slave, with programmable clock rate, phase, and polarity. The maximum data rate is ¼ of the system clock. Write collision and overrun detection protect data, and Master mode fault detection for multi-master systems prevents bus conflict.

Configuring the R8051XC-F

A spreadsheet-like Design Configurator is available to help in the selection of the core's many options. The configurable options include:

- Size of external data/program memory: 64 KB to 8 MB
- Number of DPTR registers: 1, 2 or 8
- Two types of interrupt controller: Type 51 Type 515
  - Interrupt sources: 0 to 6 0 to 18
  - External interrupts: 0 to 2 0 to 13
  - Priority levels: 2 4
- Number of 8-bit I/O ports: 0 to 4
- Number of 16-bit timers: 0 to 3
- Number or serial ports: 0, 1, or 2
- Watchdog timer: yes or no
- Multiplication-Division unit: yes or no
- DMA Channels: 0 to 8
- I2C master-slave interface: 0, 1, or 2
- SPI master-slave interface: yes or no
- On-chip debug support: OCDS, FS2 OCI, or none
- For OCDS:
  - Number of hardware breakpoints: 2 to 8
  - Program trace: yes or no
  - Data & program trace: yes or no
- Rarely used instructions MUL, DIV, DA: yes or no
- Software Reset: yes or no
- Support for external DMA operations: yes or no
- Real Time Clock: yes or no

The 8051-like prepackaged R8051XC-A core includes: two timers, one serial port, four parallel I/O Ports, and a two-level interrupt controller.

The 80515-like prepackaged R8051XC-B core includes: three timers, two serial ports, four parallel I/O ports, a watchdog timer, a multiplication-division unit, and two DPTR registers.

Implementation Results

R8051XC reference designs have been evaluated in a variety of technologies. The following sample R8051XC-F configuration ASIC results use typical-case conditions, exclude memories, and were optimized for the speed shown.

ASIC Technology	Cell Area	NAND2 Area	Approx. Area	Frequency
TSMC 0.09µ	67,258	2.8224	23,830 gates	350 MHz
TSMC 0.13µ	132,288	5.0922	25,978 gates	300 MHz
TSMC 0.18µ	263,357	9.9792	26,390 gates	250 MHz

Configuration Notes:

R8051XC-A – Two timers/counters; one serial interface; 2-priority/5-source interrupt controller.

R8051XC-B – Three timers/counters; two serial interface; 4-priority/13-source interrupt controller; MDU; Watchdog Timer.

R8051XC-F – Includes all functions, except the DMA. The DMA will add about 20,000 gates.

No configurations include on-chip debug: OCDS or OCI implemented with two hardware breakpoints will add about 5,000 gates.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support is available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements. All subcomponents were functionally verified with an HDL testbench using their individual test suites. The CPU and ALU have been verified against a proprietary hardware modeler and behavioral models. The peripherals have also been verified in their own testbenches, based on either hardware or behavioral models.

The core satisfies the requirements of the Reuse Methodology Manual and the VSIA Quality IP Metric.

Deliverables

The core is available in ASIC (synthesizable HDL) or FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sample implementation with a sample system
- Sophisticated self-checking HDL Testbench including everything needed to test the core (Verliog versions use Verilog 2001)
- Simulation scripts, vectors, and expected results
- Synthesis script
- Options configuration tool for the R8051XC-F
- Comprehensive user documentation, including detailed specification and a system integration guide

CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 07677 USA
tel 201-391-8300 fax 201-391-8694

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we turn engineering into art
This core developed by the processor and interface experts at Evatronix SA.