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This Errata Sheet refers to:

AT91RM3400 devices packaged in 100-lead PQFP with the marking AT91RM3400-AI and the product number at the bottom left of the package being 58A06R or 58A06S

ARM7TDMI®-based Microcontroller

AT91RM3400

Errata Sheet

6058B–ATARM–08/04

30. AC Characteristics: PLL Frequency Limitation

The maximum PLL output frequency is limited to 70 MHz.

Problem Fix/Workaround

None.

29. ROM Bootloader: SRAM Download Limitation

The maximum size to download in the internal SRAM when using the upload feature of the Boot ROM is 64K and does not verify the generic equation:

Max size = SRAM size - 4 K Bytes

This problem is solved on the AT91RM3400 revision 58A06S.

Problem Fix/Workaround

None.

28. MCI: Data Endianess inversion from the MCI to MMC or SD Card

The data endianess is inverted when writing or reading to or from an MMC or SD card. If the MCI interface is exclusively used to read/write from/to a dedicated card the inversion is not visible (two inversions). Furthermore, if the card is shared with other systems then endianess will not match. This endianess inversion concerns only data sectors and not command and response.

Problem Fix/Workaround

A software workaround consists of swapping the order of word bytes before writing and doing so also after reading.

27. TC: Wrong Compare at restart if Burst Low

If the counter was stopped or disabled, unwanted Compare RA, RB or RC may occur at restart if the clock selected by the counter is masked by a low selected burst input when the trigger event is recognized at the selected clock active edge. All compare effects are affected, as the flags are set incorrectly and CPC trigger, CPC stop or CPC disable may occur.

Problem Fix/Workaround

None

26. TC: Wrong 0 Captured before Compare RC Trigger

A wrong 0 is captured in RA or RB during the last selected counter clock period if CPCTRG is active and the capture event occurred at least one Master Clock cycle after the last counter value update.

Problem Fix/Workaround

None

25. TC: Erroneous Capture with Burst Low

The value captured is not equal to the Counter Value if the selected burst input is low at capture time, i.e., at the selected clock active edge where the capture event is recognized.

The captured value may be 0; otherwise, it is the Counter Value plus one instead of the Counter Value.

Problem Fix/Workaround

None

24. TC: Bad Capture at restart if Burst Low

The captured value is not zero if burst is low when the preceding trigger event is recognized. Instead, the captured value is the Counter Value before the trigger.

Problem Fix/Workaround

None

23. TC: TIOA and TIOB outputs Stuck in case of Simultaneous Events

In the TC_CMR register, if at least one of the fields; ASWTRG or AEEVT or ACPC is set to 0x0 (none), the event programmed by ACPA is not carried out.

In the TC_CMR register, if at least one of the fields; ASWTRG or AEEVT is set to 0x0 (none), the event programmed by ACPC is not carried out.

In the TC_CMR register, if the ASWTRG field is set to 0x0 (none), the event programmed by AEEVT is not carried out.

The same problem exists on the TIOB output with the fields; BSWTRG, BEEVT, BCPC and BCPB.

Problem Fix/Workaround

An order of priority for TIOA and/or TIOB events must be defined depending on the user application.

22. TC: TIMER_CLOCK2 not sampled on same edge as TIMER_CLOCK0 and TIMER_CLOCK1

TIMER_CLOCK2/TIMER_CLOCK5 are sampled on the system clock falling edge of Master Clock, whereas TIMER_CLOCK0/TIMER_CLOCK3 and TIMER_CLOCK1/TIMER_CLOCK4 are sampled on the rising edge of Master Clock. This should not have any effect on the functional operations of the Timer Counter unless the Timer Counter is used at its speed limit.

Problem Fix/Workaround

None

21. TC: Triggers do not clear the counter in Up/Down Mode

When the WAVESEL field in TC_CMR is at value 0x1 or 0x3, the triggers do not reset the counter value. The counter value can be reset only by modifying the WAVESEL field.

Problem Fix/Workaround

None

20 TC: Triggers in Up/Down Mode are lost when burst signal is active

When the WAVESEL field in TC_CMR is at value 0x1 or 0x3, the triggers occurring while the selected burst signal is active (clock disabled) are not taken into account.

Problem Fix/Workaround

None

19. TC: Clock Selection Limitation in Up/Down Mode

Selecting the Master Clock or the Master Clock divided by 2 as the Timer Counter Clock may lead to unpredictable result when the field WAVESEL in TC_CMR is at value 0x2 or 0x3.

Problem Fix/Workaround

None.

18. TC: Spurious counter overflow in Up/Down Mode.

When the WAVESEL field in TC_CMR is at value 0x1 or 0x3 and when the counter reaches the value 0xFFFF, it inverts its sense and decrements to 0xFFFE. At the same time, the OVF bit in TC_SR is set.

Problem Fix/Workaround

None.

17. PIO: Output Data Status Register is always Read/Write.

The programming of the register PIO_OWSR register has no effect on the read/write features of PIO_ODSR, which is always read/write accessible.

Problem Fix/Workaround

None.

16. SPI: Slave Mode Receiver does not mask the Highest Data Bits.

If the SPI receives a frame followed by 8 bits of data, the user needs to mask the highest byte of the Receive Holding Register, as this data may be incorrect and not 0.

Problem Fix/Workaround

The user should implement the PDC. If the PDC is not implemented, the user should mask the highest byte of the Receive Holding Register.

15. SPI: No chip select configuration change before end of current transfer.

If the SPI is programmed in Master Mode and in Fixed Peripheral Mode, and data is being sent to a slave, the user has to wait for completion of the transfer before changing the slave number. Programming a new slave number (PCS) and/or a new DLYBCS field locks the SPI on the current slave.

Problem Fix/Workaround

The user should use the Variable Peripheral Mode.

14. SPI: Warning. NPCSx rises if no data is to be transmitted.

If the SPI has sent all the data written in the SPI_TDR, the current NPCS rises immediately. This might be disruptive in the case of several SPI peripherals requiring their chip select line to remain active until a complete data buffer has been transmitted. The PDC channel may be late in providing data to be transmitted when bus latencies are too high.

Problem Fix/Workaround

For high-speed applications, the relevant PIO pins can be used to manage the data transmission.

13. SSC: Receiver does not take into account a start condition while receiving data.

The SSC receiver does not support reception of the last data sequence of a frame that overlaps a new start of a frame, regardless of the mode of detection of the start condition. For example, this prevents reception of the last data of a TDM bus.

Problem Fix/Workaround

None

12. SSC: RXSYN and TXSYN not cleared when read

The status bits RXSYN and TXSYN are active during a complete serial clock period and are not immediately cleared when SSC_SR is read.

Problem Fix/Workaround

The user must enable the interrupt relevant to RXSYN and TXSYN.

11. SSC: Receiver Speed Limitations

If RF is programmed as an input, the maximum clock frequency is MCK divided by 2.

If RF is programmed as an output and RK is programmed as an input, the maximum clock frequency is MCK divided by 6.

If RF and RK are both programmed as outputs, the maximum clock frequency is MCK divided by 4.

Problem Fix/Workaround

None

10. SSC: Transmitter Speed Limitations

If both TF and TK are programmed as outputs, the maximum clock frequency is MCK divided by 4.

If TF is programmed as an output and TK is programmed as an input, the maximum clock frequency is MCK divided by 8.

If both TF and TK are programmed as inputs, the maximum clock frequency is MCK divided by 8.

If TF is programmed as an input and TK is programmed as an output, the maximum clock frequency is MCK divided by 4.

Problem Fix/Workaround

None

9. SSC: Disabling the SSC does not stop the Frame Synchronization signal generation.

Generating RF can be stopped only by programming the FSOS field in SSC_RFMR to 0x0.

Generating TF can be stopped only by programming the FSOS field in SSC_TFMR to 0x0.

Problem Fix/Workaround

None

8. SSC: No delay when start condition overlays data transmit.

When transmission of data is programmed at the end of a frame and the start condition of the following frame is detected at the end of the current frame, the delay programmed by the STTDLY bit (in the SSC_RCMR and in the SSC_TCMR registers) is not performed on the next frame. Transmission starts immediately regardless of the programming of the field STTDLY.

Problem Fix/Workaround

None

7. TWI: Disabling does not operate correctly.

Any transfer in progress is immediately frozen if the Control Register (TWI_CR) is written with the MSDIS bit at 1. Furthermore, the status bits TXCOMP and TXRDY in the Status Register (TWI_SR) are not reset.

Problem Fix/Workaround

The user must wait for the end of transfer before disabling the TWI. In addition, the interrupts must be disabled before disabling the TWI.

6. TWI: NACK Status Bit lost

During a master frame, if TWI_SR is read between the Non Acknowledge condition detection and the TXCOMP bit rising in the TWI_SR, the NACK bit is not set.

Problem Fix/Workaround

The user must wait for the TXCOMP status bit by setting an interrupt and must not read the TWI_SR as long as transmission is not completed.

Note: TXCOMP and NACK fields are set simultaneously and the NACK field is reset after the read of the TWI_SR.

5. TWI: Possible Receive Holding Register Corruption

When loading the TWI_RHR, the transfer direction is ignored. The last data byte received in the TWI_RHR is corrupted at the end of the first subsequent transmit data byte. Neither RXRDY nor OVERRUN status bits are set if this occurs.

Problem Fix/Workaround

The user must be sure that received data is read before transmitting any new data.

4. TWI: Clock Divider Limitation

The CKDIV field on the Clock Waveform Generator (TWI_CWGR) has a maximum value of 0x5.

Problem Fix/Workaround

None

3. PMC: Constraints on the Master Clock selection sequence

The PMC_MCKR register must not be programmed in a single write operation.

Problem Fix/Workaround

The preferred programming sequence for the PMC_MCKR register is as follows:

1. Program the CSS field in the PMC_MCKR.
2. Wait for the MCKRDY bit to be set in the PMC_SR register.
3. Program the PRES field (in the PMC_MCKR).

An exception to this sequence occurs when the processor clock frequency is greater than the master clock frequency. In this case, the PRES field should be written first.None

2. PMC: MCKRDY does not rise in some cases.

When reprogramming the Master Clock Register, if both PRES and CSS fields are written with the same values as the ones already stored, or if both fields are written with different values than the ones already stored, the status bit MCKRDY does not rise. When one and only one of the PRES or CSS fields is changed, the MCKRDY bit operates normally.

Problem Fix/Workaround

If both fields must be reprogrammed, carry out the change in two steps.

1. PMC: Bad switching when writing PLL registers with the same MUL and DIV values.

When the MUL and DIV fields in the PMC_PLLBR register are written with the same values as already programmed, the Master Clock signal switches to Main Clock (output of the Main Oscillator) until a different value is programmed in the register.

When the MUL and DIV fields in the PMC_PLLAR register are written with the same values as already programmed, the Master Clock signal switches to Slow Clock (output of the 32768 Hz Oscillator) until a different value is programmed in the register.

Problem Fix/Workaround

None

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